Zetta eMMC Product Family

eMMC Specification

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1 General Description

ZETTA eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.1 which is a industry standard.

eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply. voltage (VDD or VCCQ) is supported for the MMC controller. ZETTA eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance.

There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.

The embedded flash management software of eMMC manages Wear Leveling, Bad Block Management and ECC.

2 Product List

Part Number	Density	Flash Type	PackageType	Package size
ZDEMDCM004G-BG25	4GB	MLC	FBGA153	11.5x13x1.0 (mm)
ZDEMDCM008G-CG25	8GB	MLC	FBGA153	11.5x13x1.0 (mm)

3 Key Features

- e•MMC v5.1 compatible. Detail description is referenced by JEDEC Standard

- (Backward compatible to e•MMC v4.5 to v5.0)

- Bus mode

- Data bus width: 1bit(default), 4bit and 8bit

- Data transfer rate: up to 400MB/s (HS400) @ 200MHz DDR with 8bit bus width
- MMC I/F Clock Frequency: 0~200MHz
- MMC I/F Boot Frequency: 0~52MHz

- Operating Voltage Range

- VCC (NAND/Core): 2.7V ~ 3.6V

- VCCQ (CTRL/IO): 1.7V ~ 1.95V / 2.7V ~ 3.6V

- Temperature

- Operation (-25℃ ~ 85℃)

- Storage without operation (-40℃ ~ 85℃)

➢ **Device type values (EXT_CSD Register：DEVICE_TYPE [196])**

Bit	Device Type	Supportability
7	HS400 Dual Data Rate e•MMC @ 200 MHz - 1.2V I/O	Not support
6	HS400 Dual Data Rate e•MMC @ 200 MHz - 1.8V I/O	Support
5	HS200 Single Data Rate e•MMC @ 200 MHz - 1.2V I/O	Not support
4	HS200 Single Data Rate e•MMC @ 200 MHz - 1.8V I/O	Support
3	High-Speed Dual Data Rate e•MMC @ 52MHz - 1.2V I/O	Not support
2	High-Speed Dual Data Rate e•MMC @ 52MHz - 1.8V or 3V I/O	Support
1	High-Speed e•MMC @ 52MHz - at rated device voltage(s)	Support
0	High-Speed e•MMC @ 26MHz - at rated device voltage(s)	Support

Note： It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

➢ **Extended CSD revisions (EXT_CSD Register：EXT_CSD_REV [192])**

Value	Timing Interface	EXT_CSD Register Value
255–9	Reserved	-
8	Revision 1.8 (for MMC v5.1)	Support
7	Revision 1.7 (for MMC V5.0)	-
6	Revision 1.6 (for MMC V4.5, V4.51)	-
5	Revision 1.5 (for MMC V4.41)	-
4	Revision 1.4 (Obsolete)	-
3	Revision 1.3 (for MMC V4.3)	-
2	Revision 1.2 (for MMC V4.2)	-
1	Revision 1.1 (for MMC V4.1)	-
0	Revision 1.0 (for MMC V4.0)	-

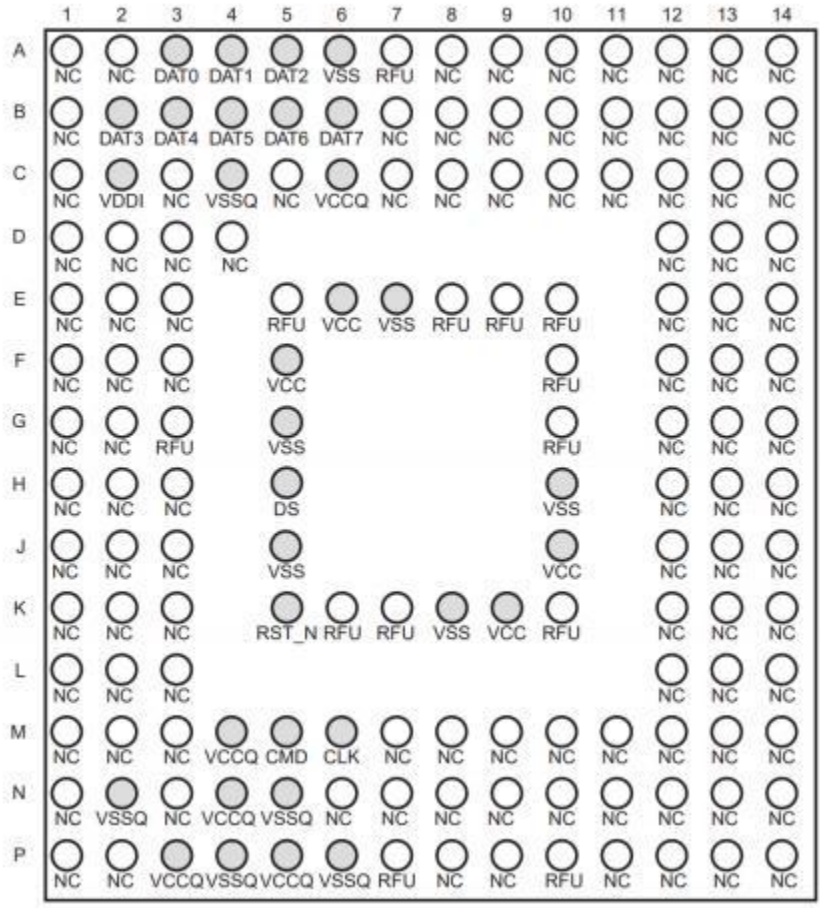
Note： Current e•MMC standard defined by JEDEC supports up to 0x08 for EXT_CSD_REV value.

➢ **High Speed timing values (EXT_CSD Register: HS_TIMING [185])**

Value	Timing Interface	Supportability
0x0	Selecting backwards compatibility interface timing	Support
0x1	High Speed	Support
0x2	HS200	Support
0x3	HS400	Support

4 Pin Description

4.1 eMMC 153 Ball Pin Assignment



Ball No.	Name	Ball No.	Name	Ball No.	Name	Ball No.	Name
A3	DAT0	C2	VDDi	J5	V_{SS}	N4	V_{CCQ}
A4	DAT1	C4	V_{SSQ}	J10	V_{CC}	N5	V_{SSQ}
A5	DAT2	C6	V_{CCQ}	K5	RST_n	P3	V_{CCQ}
A6	V_{SS}	E6	V_{CC}	K8	V_{SS}	P4	V_{SSQ}
B2	DAT3	E7	V_{SS}	K9	V_{CC}	P5	V_{CCQ}
B3	DAT4	F5	V_{CC}	M4	V_{CCQ}	P6	V_{SSQ}
B4	DAT5	G5	V_{SS}	M5	CMD	--	--
B5	DAT6	H5	DS	M6	CLK	--	--
B6	DAT7	H10	V_{SS}	N2	V_{SSQ}	--	--

Note:

NC: No Connect, can be connected to ground or left floating.

RFU: Reserved for Future Use, should be left floating for future use.

VSF: Vendor Specific Function, shall be left floating.

4.2 eMMC Pin Description

Signal	Ball No.	Description
CLOCK (CLK)	M6	Each cycle of the clock directs a transfer on the command line and on the data lines.
COMMAND (CMD)	M5	This signal is a bidirectional command channel used for device initialization and command transfer. The CMD Signal has 2 operation modes: open drain for initialization, and push-pull for fast command transfer.
DATA (DAT0-DAT7)	A3~A5 B2~B6	These are bidirectional data channels. The DAT signals operate in push-pull mode.
RST_n	K5	Hardware Reset Input
DS	H5	Data Strobe: Return Clock signal used in HS400 mode
V_{CCQ}	C6,M4,N4,P3,P5	Power supply for MMC interface and Controller, have two power mode: High power mode:2.7V~3.6V; Lower power mode:1.7V~1.95V
V_{CC}	E6,F5,J10,K9	Power supply for NAND flash memory, its power voltage range is: 2.7V~3.6V
VDDi	C2	VDDi is internal power mode. Connect 1uF or 2.2uF capacitor from VDDi to ground
V_{SS},V_{SSQ}	A6, E7, G5, H10, J5, J8,C4,N2,P4,P6	Ground lines

Note： All other pins are not connected [NC] and can be connected to GND or left floating.

5 DC Electrical Characteristics

5.1 General operating conditions

7 Parameter	Symbol	Min	Max	Unit	Remarks
Peak voltage on all lines	--	-0.5	V_{CCQ}+0.5	V	--
All Inputs					
Input Leakage Current (before initialization sequence and/or the internal pull up resistors connected)	--	-100	100	uA	--
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)	--	-2	2	uA	--
All Outputs					
Output Leakage Current (before initialization sequence)	--	-100	100	uA	--
Output Leakage Current (after initialization sequence)	--	-2	2	uA	--

Note： Initialization sequence is defined in Power-Up chapter of JEDEC/MMCA Standard.

5.2 Operating Current (RMS)

➢ Active Power Consumption during operation

Power Consumption	4GB	8GB	Units
HS400 Read VCC	50	61	mA
HS400 Read VCCQ	162	189	mA
HS400 Write VCC	20	26	mA
HS400 Write VCCQ	83	92	mA

Note:

- Temperature: 25℃
- V_{CC}=3.3V, V_{CCQ}=1.8V
- Not 100% tested

5.3 Power supply voltage

Parameter	Symbol	Test Conditions	Min	Max	Unit
Supply voltage1 （NAND/Core）	V_{CC}	--	2.7	3.6	V
Supply voltage 2 （CTRL/IO）	V_{CCQ}	--	1.7	1.95	V
			2.7	3.6	V

5.4 Standby Power Consumption

Power Consumption	4GB	8GB	Units
Standby(VCCQ & VCC on)	150	170	uA

Note:

- Power measurement conditions: Bus configuration =x8, No CLK
- V_{CC}=3.3V, V_{CCQ}=1.8V
- Not 100% tested

5.5 Sleep Power Consumption

Sleep Power Consumption in Sleep State

Power Consumption	4GB	8GB	Units
Sleep (VCCQ on, VCC off)	90	90	uA

Note:

- Power measurement conditions: Bus configuration = x8, No CLK
- Enter sleep state by CMD5, V_{CC} power is switched off, V_{CCQ}=1.8V
- Not 100% tested

5.6 Bus Signal Line Loading

The total capacitance C_L of each line of the e•MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the e•MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

Bus Signal Line Load

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	--	100	kΩ	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10	--	100	kΩ	to prevent bus floating
Internal pull up resistance DAT1–DAT7	R_{int}	10	--	150	kΩ	to prevent unconnected lines floating
Bus signal line capacitance	C_L	--	--	30	pF	Single Device
Single Device capacitance	C_{DEVICE}	--	--	12	pF	Single Device capacitance
Maximum signal line inductance	--	--	--	16	nH	$f_{PP} \leq 52$ MHz

6 eMMC Register Description

Software designers should refer to the particular implementation to do the programming. This section introduces the registers in eMMC and the values that are used in ZETTA eMMC. The following table is the register list of current specification. The detail functionality is not described here; please reference to latest eMMC specifications.

6.1 Operation Conditions Register (OCR) Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

OCR bit	V_{CCQ} voltage window	e.MMC
[6:0]	Reserved	000 0000b
[7]	1.7–1.95	1b
[14:8]	2.0–2.6	000 0000b
[23:15]	2.7–3.6	1 1111 1111b
[28:24]	Reserved	000 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)
[31]	Card power up status bit (busy)*	

Note*： This bit is set to LOW if the e•MMC has not finished the power up routine. The supported voltage range is coded as shown in table.

6.2 SD Card Identification Register (CID)

The Device IDentification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (e•MMC protocol). Every individual flash or I/O Device shall have a unique identification number. Every type of e•MMC Deviceshall have a unique identification number. Table 75 lists these identifiers. The structure of the CID register is defined in this section.

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	E7h
Reserved	-	6	[119:114]	0
Card/BGA	CBX	2	[113:112]	01
OEM/Application ID	OID	8	[111:104]	11h
Product name	PNM	48	[103:56]	ZD008G
Product revision	PRV	8	[55:48]	FFh
Product serial number	PSN	32	[47:16]	Serial number
Manufacturing date	MDT	8	[15:8]	Manufacturing date
CRC7 checksum	CRC	7	[7:1]	0
Not used, always ‘1’	-	1	[0:0]	1

6.3 Driver Stage Register (DSR)

The 16-bit driver stage register (DSR) is optionally used to improve the bus performance for extended operating conditions. The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

6.4 Relative Card Address Register (RCA)

The writable 16-bit relative Device address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the Stand-by State with CMD7.

6.5 Card Specific Data Register (CSD)

The Card-Specific Data register provides information on how to access the e•MMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:

- R:Read only
- W: One time programmable and not readable.
- R/W: One time programmable and readable.
- W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
- R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
- R/W/E_P:Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
- W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Name	Field	Width	Cell Type	CSD-slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
System specification version	SPEC_VERS	4	R	[125:122]	4h
Reserved	-	2	R	[121:120]	0h
Data read access-time 1	TAAC	8	R	[119:112]	2Fh
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	2Ah
Card command classes	CCC	12	R	[95:84]	5F5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved	-	2	R	[75:74]	0h
Device size	C_SIZE	12	R	[73:62]	FFFh
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	6h
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	6h
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	6h
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	6h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	1Fh
Write protect group enable	WP_GRP_MULT	1	R	[31:31]	1h
Manufacturer default	ECC DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	1h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved	-	4	R	[20:17]	0h
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy flag(OTP)	COPY	1	R/W	[14:14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h
CRC	CRC	7	R/W/E	[7:1]	8h
Not used, always '1'	-	1	-	[0:0]	1h

6.6 Extended CSD register

The Extended CSD register defines the e•MMC properties and selected modes. It is 512 bytes long.

The most significant 320 bytes are the Properties segment, which defines the e•MMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the e•MMC is working in. These modes can be changed by the host by means of the SWITCH command.

- R: Read only
- W: One time programmable and not readable.
- R/W: One time programmable and readable.
- W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
- R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
- R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
- W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Properties Segment					
Reserved	-	6	TBD	[511:506]	0h
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0h
Supported Command Sets	S_CMD_SET	1	R	[504]	1h
HPI features	HPI_FEATURES	1	R	[503]	3h
Background operations support	BKOPS_SUPPORT	1	R	[502]	1h
Max packed read commands	MAX_PACKED_READS	1	R	[501]	5h
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	3h
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	1h
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	1h
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0h
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	5h
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0h
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	3h
Supported modes	SUPPORTED_MODES	1	R	[493]	1h
FFU features	FFU_FEATURES	1	R	[492]	1h
Operation codes timeout	OPERATION_CODE_TIME OUT	1	R	[491]	17h
FFU Argument	FFU_ARG	4	R	[490:487]	0h
Barrier support	BARRIER_SUPPORT	1	R	[486]	0h

Reserved	-	177	TBD	[485:309]	All ”0”
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	0h
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	0h
Reserved	-	1	TBD	[306]	0h
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	0h
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	1h
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	1h
Name	**Field**	**Size (Bytes)**	**Cell Type**	**CSD-slice**	**Value**
Pre EOL information	PRE_EOL_INFO	1	R	[267]	1h
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	8h
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	8h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	8h
Device version	DEVICE_VERSION	2	R	[263:262]	0h
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	0h
Power class for 200MHz, DDR at V_{CC}= 3.6V	PWR_CL_DDR_200_360	1	R	[253]	0h
Cache size	CACHE_SIZE	4	R	[252:249]	80h
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	32h
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	3Ch
Background operations status	BKOPS_STATUS	1	R	[246]	0h
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0h
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	1Eh
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0h
Power class for 52MHz, DDR at V_{CC} = 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0h
Power class for 52MHz, DDR at V_{CC} = 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0h
Power class for 200MHz at V_{CCQ} =1.95V, V_{CC} = 3.6V	PWR_CL_200_195	1	R	[237]	0h
Power class for 200MHz, at V_{CCQ}=1.3V, V_{CC} = 3.6V	PWR_CL_200_130	1	R	[236]	0h
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0h
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0h
Reserved		2	TBD	[233]	0h
TRIM Multiplier	TRIM_MULT	1	R	[232]	2h
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	55h
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	1Bh
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	11h
Boot information	BOOT_INFO	1	R	[228]	7h
Reserved		1	TBD	[227]	0h
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	20h
Access size	ACC_SIZE	1	R	[225]	1h

High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	1h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	18h
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	1h
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	20h
Sleep current [Vcc]	S_C_VCC	1	R	[220]	7h
Sleep current [Vccq]	S_C_VCCQ	1	R	[219]	7h
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	17h
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	17h
Name	**Field**	**Size (Bytes)**	**Cell Type**	**CSD-slice**	**Value**
Sleep Notification Timout1	SLEEP_NOTIFICATION_TIME	1	R	[216]	11h
Sector Count	SEC_COUNT	4	R	[215:212]	4GB：73A000h 8GB：E74000h
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0h
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0h
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0h
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0h
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0h
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0h
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0h
Reserved		1	TBD	[204]	0h
Power class for 26MHz at 3.6 V 1 R	PWR_CL_26_360	1	R	[203]	0h
Power class for 52MHz at 3.6 V 1 R	PWR_CL_52_360	1	R	[202]	0h
Power class for 26MHz at 1.95 V 1 R	PWR_CL_26_195	1	R	[201]	0h
Power class for 52MHz at 1.95 V 1 R	PWR_CL_52_195	1	R	[200]	0h
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	5h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	19h
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	Fh
Device type	DEVICE_TYPE	1	R	[196]	57h
Reserved		1	TBD	[195]	0h
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	2h
Reserved		1	TBD	[193]	0h
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	8h
Modes Segment					
Command Set	CMD_SET	1	R/W/E_P	[191]	0h
Reserved		1	TBD	[190]	0h
Command set revision	CMD_SET_REV		R	[189]	0h
Reserved		1	TBD	[188]	0h
Power class	POWER_CLASS		R/W/E_P	[187]	0h
Reserved		1	TBD	[186]	0h
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0h

Strobe Support	STROBE_SUPPORT	1	R	[184]	0h
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0h
Reserved		1	TBD	[182]	0h
Erased memory range	ERASE_MEM_CONT	1		[181]	0h
Reserved		1	TBD	[180]	0h
Partition Configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0h
Boot Config protection	BOOT_CONFIG_PROT	1	R/W &R/W/C_P	[178]	0h
Name	**Field**	**Size (Bytes)**	**Cell Type**	**CSD-slice**	**Value**
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0h
Reserved		1	TBD	[176]	0h
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0h
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0h
Boot area write protect register	BOOT_WP	1	R/W &R/W/C_P	[173]	0h
Reserved		1	TBD	[172]	0h
User area write protect register	USER_WP	1	R/W,R/W/ C_P &R/W/E_P	[171]	0h
Reserved		1	TBD	[170]	0h
FW configuration	FW_CONFIG	1	R/W	[169]	0h
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	20h
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0h
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	15h
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0h
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0h
Enable background operations handshake	BKOPS_EN	1	R/W & R/W/E	[163]	0h
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0h
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0h
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	7h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	E7h
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0h
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0h
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0h
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0h
Reserved		1	TBD	[135]	0h
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0h
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0h
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0h
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0h
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	1h
Reserved		2	TBD	[129:128]	0h

Vendor Specific Fields	NATIVE_SECTOR_SIZE	1	<vendor specific>	[127:64]	0h
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0h
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0h
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0h
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0h
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0h
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0h
Name	**Field**	**Size (Bytes)**	**Cell Type**	**CSD-slice**	**Value**
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0h
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0h
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0h
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0h
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0h
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0h
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0h
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0h
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0h
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0h
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0h
Reserved		2	TBD	[28:27]	0h
FFU status	FFU_STATUS	1	R	[26]	0h
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0h
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	4GB：3A0200h 8GB：740400h
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	3h
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	9h
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0h
Reserved		15	TBD	[14:0]	0h

Note： Reserved bits should be read as “0”.

7 Production Specifications

7.1 Performance

HS400 Performance	4GB	8GB	Units
Sequential Read	188	230	MB/s
Sequential Write	64	121	MB/s
Random Read	3419	3674	IOPS
Random Write	2154	1980	IOPS

7.2 Power Consumption

Operating Current

Power Consumption	4GB	8GB	Units
HS400 Read VCC	50	61	mA
HS400 Read VCCQ	162	189	mA
HS400 Write VCC	20	26	mA
HS400 Write VCCQ	83	92	mA

Note:

- Power measurement conditions: Bus configuration =x8 @200MHz DDR
- Max RMS current is the average RMS current consumption over a period of 100ms.
- Temperature: 25℃
- V_{CC}=3.3V, V_{CCQ}=1.8V
- Not 100% tested

Standby Power Consumption

Power Consumption	4GB	8GB	Units
Standby(VCCQ & VCC on)	150	170	uA

Note:

- Power measurement conditions: Bus configuration =x8, No CLK
- V_{CC}=3.3V, V_{CCQ}=1.8V
- Not 100% tested

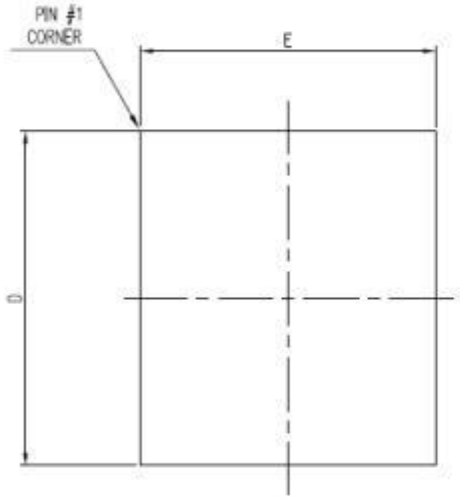
Sleep Power Consumption

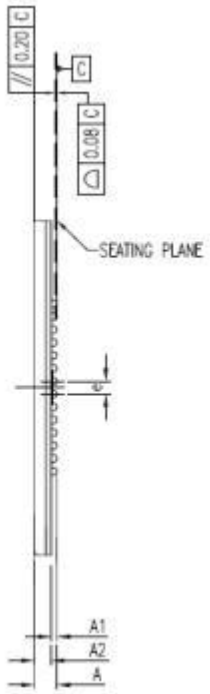
Power Consumption	4GB	8GB	Units
Sleep (VCCQ on, VCC off)	90	90	uA

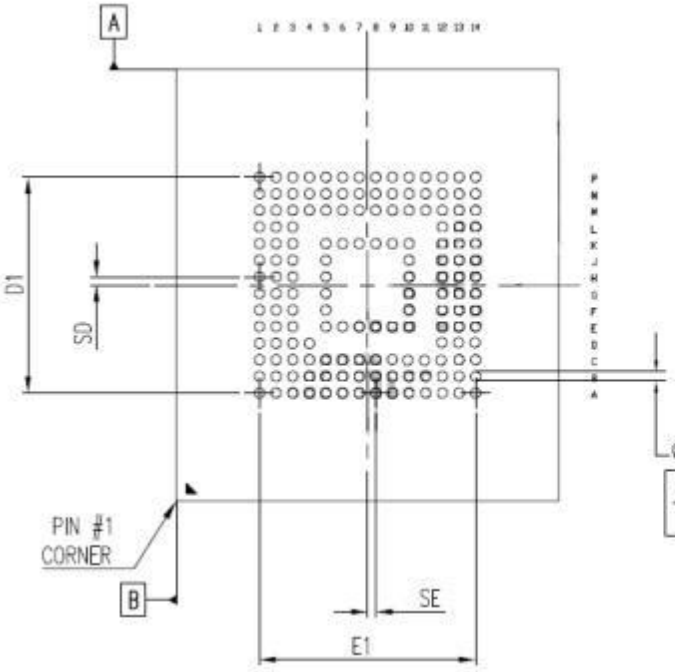
Note:

- Power measurement conditions: Bus configuration = x8, No CLK
- Enter sleep state by CMD5, V_{CC} power is switched off, V_{CCQ}=1.8V
- Not 100% tested

8 Package Dimension







SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	---	---	1.00	---	---	0.039
A1	0.15	---	---	0.006	---	---
A2	---	---	0.71	---	---	0.028
b	0.25	0.30	0.35	0.010	0.012	0.014
D	12.90	13.00	13.10	0.508	0.512	0.516
E	11.40	11.50	11.60	0.449	0.453	0.457
e	0.5 BSC.			0.020 BSC.		
JEDEC	MO-276					

9 Partition Configuration

9.1 Partition Management

The memory configuration initially consists (before any partitioning operation) of the User Data Area and RPMBArea Partitions and two Boot Area Partitions.

The embedded device also offers the host the possibility to configure additional local memory partitions with independent address spaces, starting from logical address 0x00000000, for different usage models.

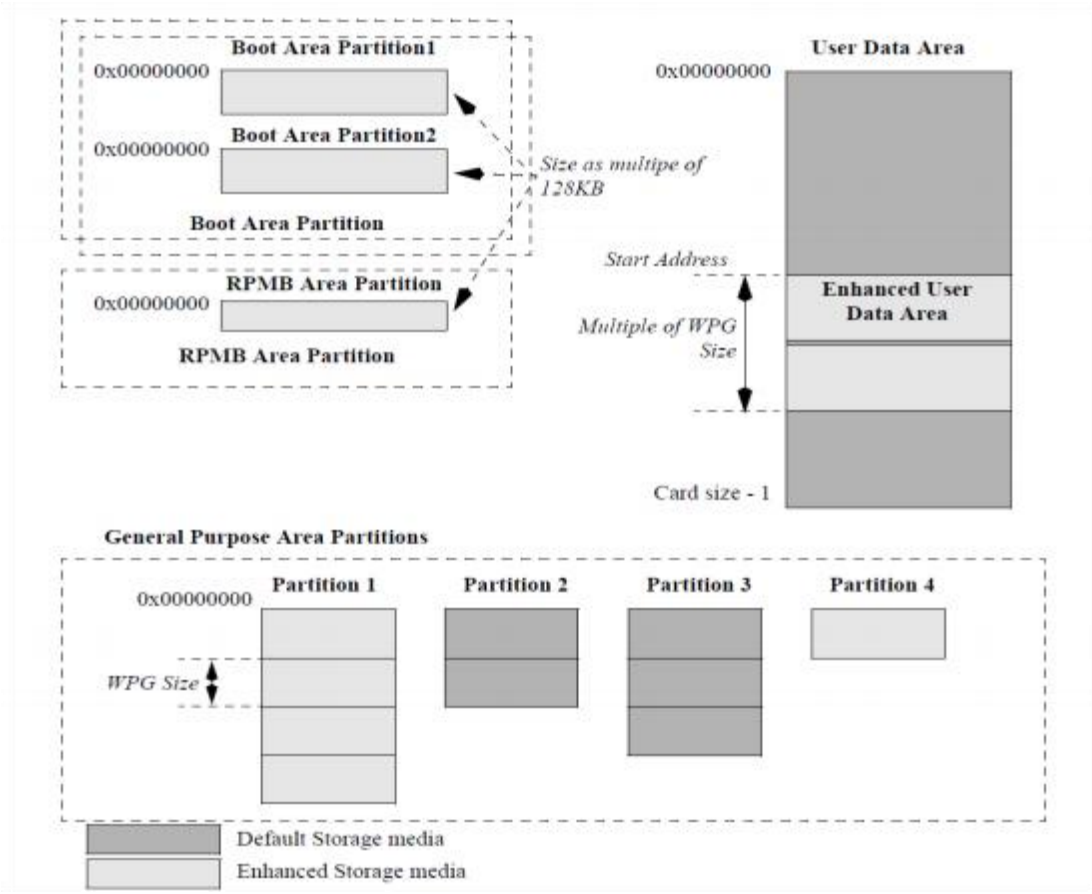
Therefore, the memory block areas can be classified as follows:

- Two Boot Area Partitions, whose size is multiple of 128 KB and where booting from e•MMC can be performed.
- One RPMB Partition accessed through a trusted mechanism, whose size is defined as multiple of 128 KB.
- Four General Purpose Area Partitions to store sensitive data or for other host usage models, whose sizes are a multiple of a Write Protect Group.

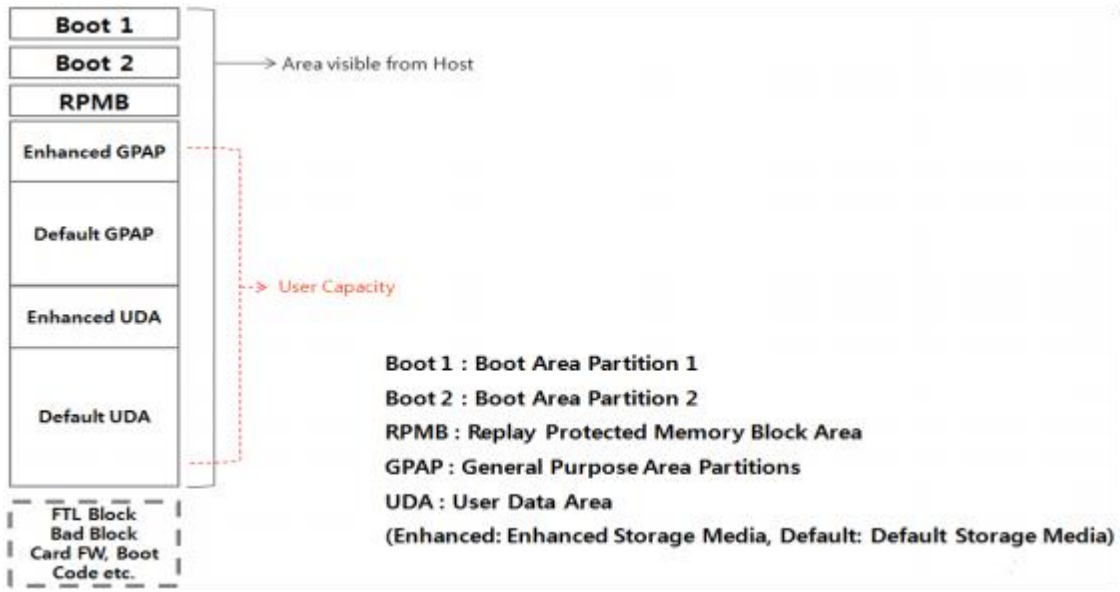
Boot and RPMB Area Partitions' sizes and attributes are defined by the memory manufacturer (read-only), while General Purpose Area Partitions'sizes and attributes can be programmed by the host only once in the device life-cycle (one-time programmable).

Moreover, the host is free to configure one segment in the User Data Area to be implemented as enhanced storage media, and to specify its starting location and size in terms of Write Protect Groups. The attributes of this Enhanced User Data Area can be programmed only once during the device life-cycle (one-time programmable).

A possible final configuration can be the following:



9.2 User Density



- **Boot and RPMB Size**

Capacity	Boot1 Size	Boot2 Size	RPMB Size
4GB/8GB	4MB	4MB	4MB

- **User Density Size**

Capacity	User Area Capacity	SEC_COUNT in Extended CSD
4GB	3700MB	0X73A000
8GB	7400MB	0XE74000

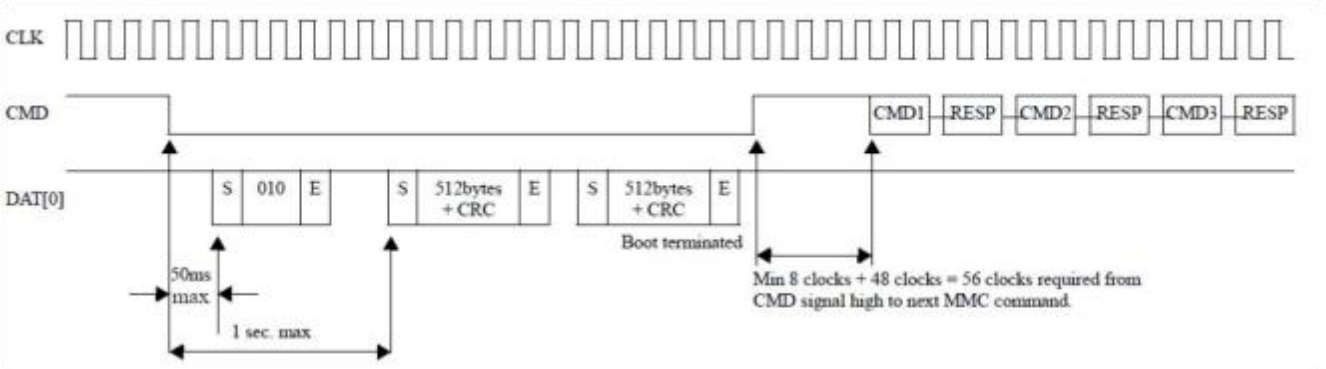
- **Maximum Enhanced Partition Size**

Capacity	Max. Enhanced Partition Size	MAX_ENH_SIZE_MULT	HC_WP_GRP_SIZE	HC_ERASE_GRP_SIZE
4GB	1840MB	0X73	0X20	0X01
8GB	3696MB	0XE7	0X20	0X01

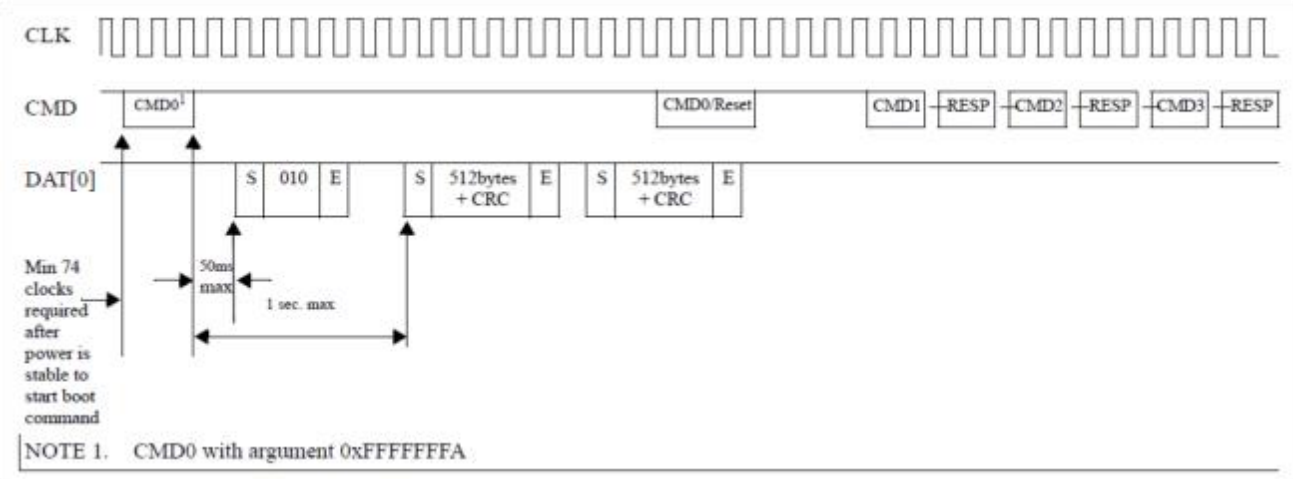
Max Enhanced Area = MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes

9.3 Boot Operation Mode

In boot operation mode, the master can read boot data from the slave (device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting.



Boot operation complete Clock = 400 kHz
(Compatible with the description which ≤400kHz)



Revision History

Version	Date	Description
Rev 1.0	2023/12/10	Released