ZD25Q128C

Serial Multi I/O Flash Memory Datasheet

Performance Highlight

- Voltage supply range from 2.7V to 3.6V for Read, Erase and Program
- x1, x2 and x4 Multi I/O Support
- High reliability with 100K cycling endurance and 20-year data retention

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1. OVERVIEW

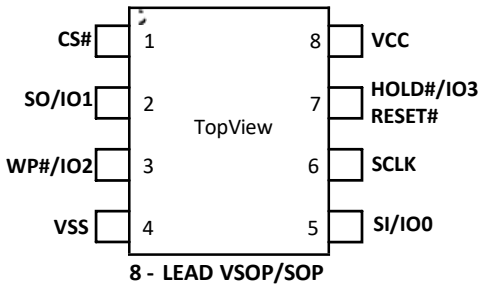
The ZD25Q128C (128M-Bit) serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI and QPI : Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1(SO), I/O2 (WP#), and I/O3 (HOLD#/RESET#).The Dual I/O & Dual output data is transferred with speed of 266Mbits/s and the Quad I/O & Quad output data is transferred with speed of 532Mbits/s.

1.1. Performance

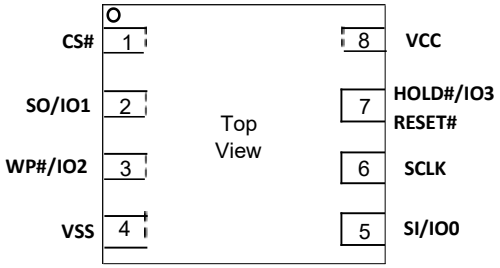
- **SPI Flash Memories**
  - Standard SPI: SCLK, CS#, SI, SO
  - Dual SPI: SCLK, CS#, IO0, IO1
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
  - QPI: SCLK, CS#, IO0, IO1, IO2, IO3
  - SPI/QPI DTR(Double Transfer Rate) Read
- . **Highest Performance Serial Flash**
  - 1 I/O 133MHz for fast read
  - 2 I/O Dual I/O Data transfer up to 266Mbits/s
  - 4 I/O Quad I/O Data transfer up to 532Mbits/s
  - QPI Mode Data transfer up to 532Mbits/s
- **Flexible Architecture for Code and Data Storage**
  - Uniform 4K-byte Sector Erase
  - Uniform 64K-byte Block Erase
  - Program 1 to 256 byte per programmable page
  - Minimum 100,000 Program/Erase Cycles
  - More than 20-year data retention
- **Package Information**
  - SOP8 208mil
  - WSON8 (6x5mm)
  - SOP16 300mil
  - Contact ZETTA for KGD and other options
- **Power Supply and Low Power consumption**
  - Single 2.7V to 3.6V supply
  - 15μA standby current
  - 1μA typical deep power down current
- **Fast Program and Erase Speed**
  - 0.5ms page program time
  - 43ms 4K-byte sector erase time
  - 0.23s 64K-byte block erase time
  - 48s chip erase time
- **Advanced Security Features**
  - 128-Bit Unique ID for each device
  - 3* 1024-Byte Security Registers with OTP Locks
  - Discoverable parameters (SFDP) register

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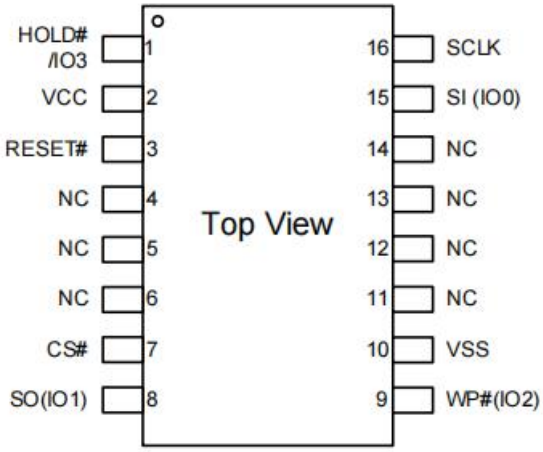
1.2. Pin Definition



8 - LEAD VSOP/SOP



8 - LEAD WSON/USON



16-LEAD SOP

Table-1. Pin Description for SOP8/USON8/WSON8 package

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	HOLD#/RESET# (IO3)	I/O	Hold Input (Data Input Output 3)
8	VCC		Power Supply

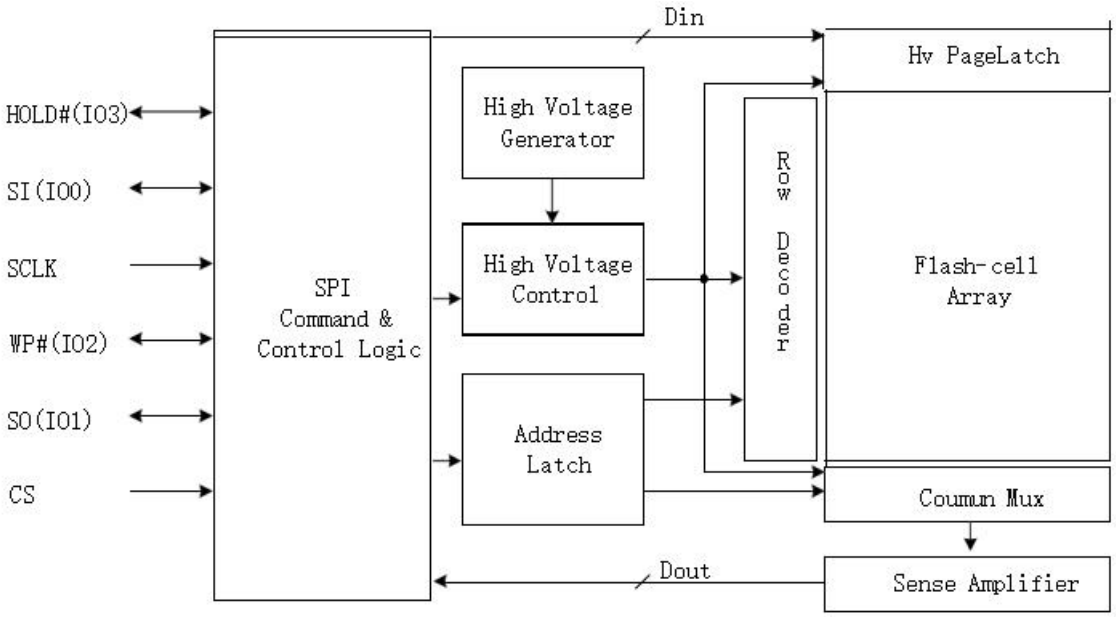
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Table-2. Pin Description for SOP16 Package

Pin No.	Pin Name	I/O	Description
1	IO3	I/O	Data Input Output 3
2	VCC		Power Supply
3	RESET#	I	Reset Input
7	CS#	I	Chip Select Input
8	SO (IO1)	I/O	Data Output (Data Input Output 1)
9	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
10	VSS		Ground
15	SI (IO0)	I/O	Data Input (Data Input Output 0)
16	SCLK	I	Serial Clock Input
4~6,11~14	NC		No Connection

2. DESCRIPTION

2.1 Block diagram



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2.2 Memory organization

Table-3. ZD25Q128C Array Organization

Each device has	Each block has	Each sector has	Each page has	
16M	64/32K	4K	256	Bytes
64K	256/128	16	-	Pages
4K	16/8	-	-	Sectors
256/512	-	-	-	Blocks

Table-4. ZD25Q128C Uniform Block Sector Architecture

Block	Sector	Address range	
255	4095	FFF000H	FFFFFFH
	.....	.....	.....
	4080	FF0000H	FF0FFFH
254	4079	FEF000H	FEFFFFH
	.....	.....	.....
	4064	FE0000H	FE0FFFH
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
2	47	02F000H	02FFFFH
	.....	.....	.....
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	.....	.....	.....
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	.....	.....	.....
	0	000000H	000FFFH

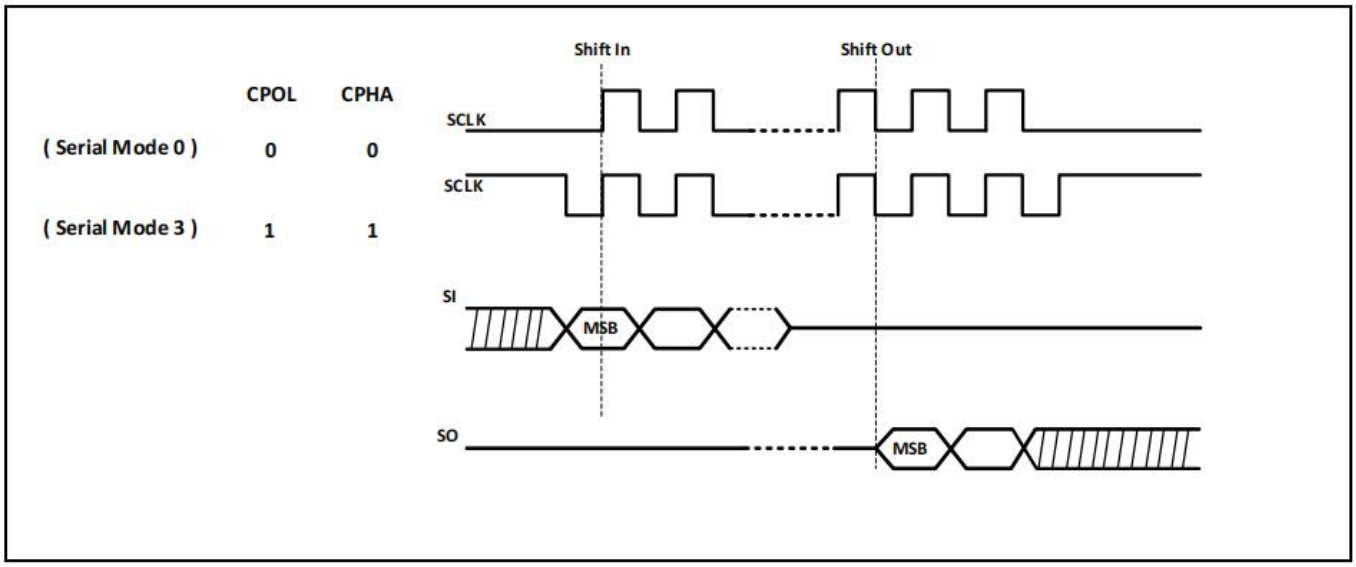
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3. DEVICE OPERATION

3.1 Mode0 and Mode3

1. Before a command is issued, the status register should be checked to ensure the device is ready for the intended operation.
2. When an incorrect command is input, the device enters standby mode and remains in standby mode until the next CS# falling edge. In standby mode, the SO pin of the device is in High-Z.
3. When the correct command is input, the device enters active mode and remains in active mode until the next rising edge of CS#.
4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference between Serial mode 0 and mode 3 is shown in Figure-1.

Figure-1. Serial Modes Supported (for Normal Serial Mode)



Standard SPI

The ZD25Q128C features a serial peripheral interface on 4 signals: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and is data shifted out on the falling edge of SCLK.

Dual SPI

The ZD25Q128C supports Dual SPI operation when using the “Dual Output Fast Read” (3BH), “Dua l I/O Fast Read” (BBH) commands. These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI command, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The ZD25Q128C supports Quad SPI operation when using the “Quad Output Fast Read” (6BH), “Quad I/O Fast Read” (EBH) and “Quad Input Page Program” (32H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the

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Quad SPI command, the SI, SO, WP# and HOLD# pins become bidirectional I/O pins: IO0, IO1, IO2 and IO3, respectively. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

QPI

The ZD25Q128C supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the "Enable the QPI (38H)" command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/QuadSPI mode and QPI mode are exclusive. Only one mode can be active at any given times. "Enable the QPI (38H)"and "Disable the QPI (FFH)" commands are used to switch between these two modes. Upon power-up and after software reset using "Reset (99H)" command, the default state of the device is Standard/Dual/Quad SPI mode. The QPI mode requires the non-volatile Quad Enable bit (QE) in Status Register to be set.

SPI / QPI DTR Read

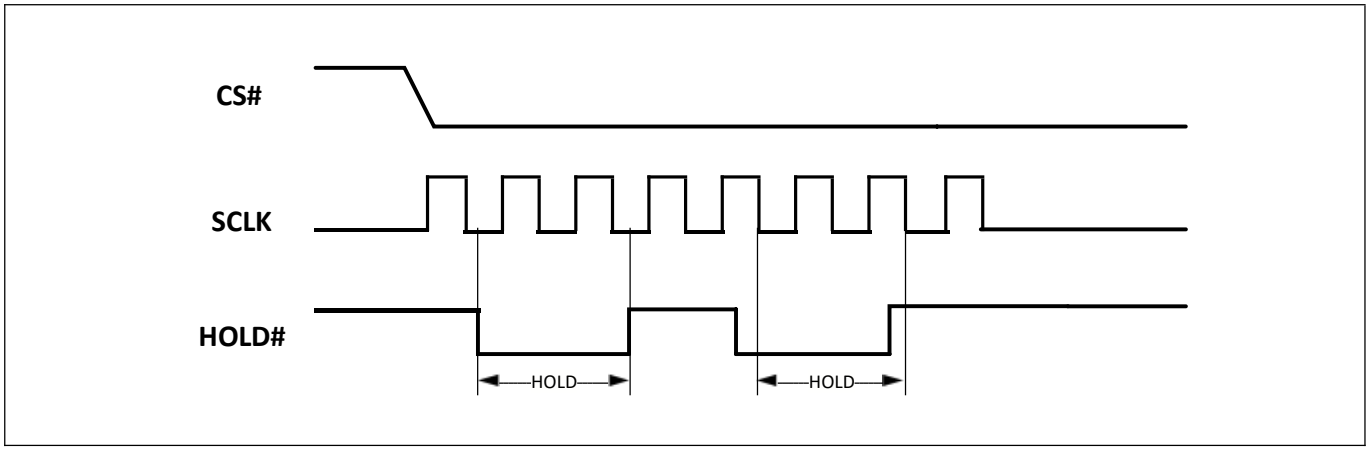
To effectively improve the read operation throughput without increasing the serial clock frequency, ZD25Q128C introduces multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

Hold

Driving the HOLD# pin low will pause any serial communications with the device. The HOLD feature will not stop the following operations if already in progress when the HOLD# pin goes low: status register write, program, or erase.

The operation of HOLD requires Chip Select (CS#) to remain low and begins on the falling edge of HOLD# pin signal while the Serial Clock (SCLK) signal is low (if the Serial Clock signal is not low, the HOLD operation will not start until the Serial Clock signal is low). The HOLD condition ends on the rising edge of HOLD# pin signal while the Serial Clock (SCLK) signal is low (if the Serial Clock signal is not low, the HOLD operation will not end until the Serial Clock is low).

Figure-2. Hold Condition



During the HOLD operation, the Serial Data Output (SO) is in a high impedance state when the HOLD# pin goes low and will remain in a high impedance state until the HOLD# pin goes high. The Serial Data Input (SI) is ignored (don't care) if both the Serial Clock (SCLK) and HOLD# pin go low and will remain in this state until the SCLK goes low and the HOLD# pin goes high. If Chip Select (CS#) is driven high during the HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be driven high and CS# must be at a logic low.

Note: The HOLD feature is disabled in Quad I/O and QPI mode.

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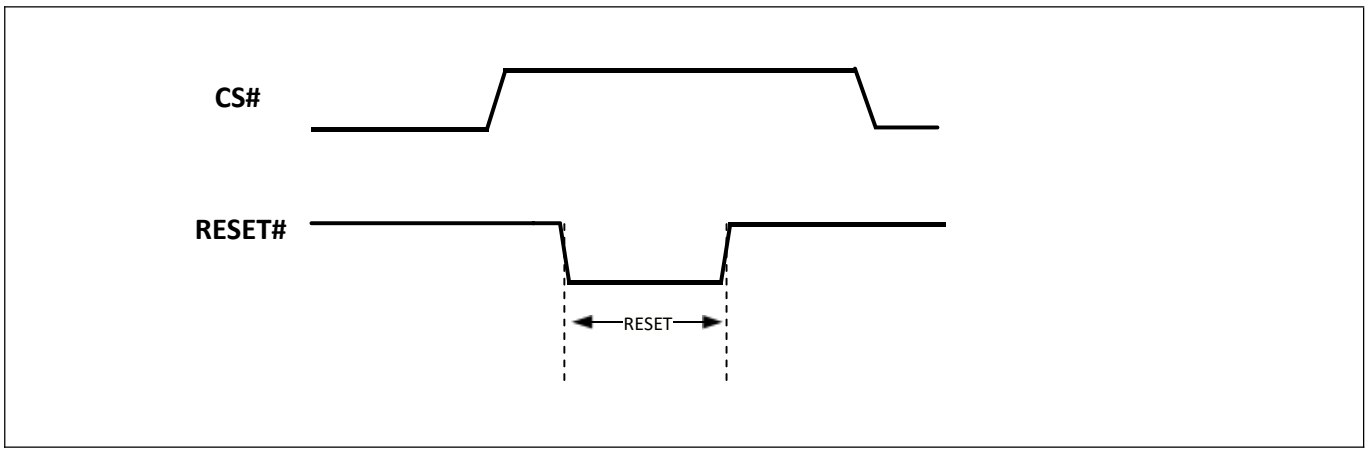
RESET Function

The HOLD/RST bit is used to determine whether HOLD or RESET function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=1, the HOLD#/RESET# pin acts as RESET# pin. The hardware RESET function is available when QE=0. If QE=1, The RESET function is disabled, and the HOLD#/RESET# pin acts as dedicated data I/O pin. For 16-pin and 24-ball packages, a dedicated RESET# is used to do the hardware RESET and it is independent of QE bit setting. The RESET# pin goes low for a minimum period of tRLRH will reset the flash. After reset cycle, the flash is at the following states:

-Standby mode

-All the volatile bits will return to the default status as power on.

Figure-3. RESET Condition



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3.2 Status Register (SR)

Table-5. Status Register 2

S15	S14	S13	S12	S11	S10	S9	S8
SUS1	CMP	LB3	LB2	LB1	SUS2	QE	SRP1
Read-only	Non-volatile	Non-volatile OTP			Read-only	Non-volatile	Non-volatile

Table-6. Status Register 1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP
Non-volatile	Non-volatile					Read-only	Read-only

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the device is busy executing a program/erase/write status register operation. When the Write in Progress (WIP) bit is set to 1, a program/erase/write status register operation is in progress. When the Write in Progress (WIP) bit is set to 0, the device does not have a program/erase/write status register operation in progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset, and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area software protected against Program and Erase commands. These bits are written with the Write Status Register (01H) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to the target value, the relevant memory area (as defined in Table-9.X) becomes protected against Page Program (02H), Sector Erase (20H) and Block Erase (D8H) commands. The Chip Erase (60H or C7H) command is executed, only if the Block Protect bits are set to “None protected”. The Block Protect bits can be written if the Hardware Protection Mode has not been set.

SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one-time programmable protection.

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Table-7. Status Register Protection Bits

SRP1	SRP0	#WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1. (Default)
0	1	0	Hardware Protected	WP#=0, the Status Register is locked and cannot be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down (1)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program (2)	Status Register is permanently protected and cannot be written to.

Notes:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact ZETTA for details.

QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the device is set to Standard SPI operation and both WP# and HOLD# pins are enabled. When the QE bit is set to 1, the Quad IO2 and IO3 pins are enabled and the WP# pin function is not available since this pin is used for IO2. (Set the QE bit to 0 to avoid short issue if the WP# or HOLD# pin is tied directly to the power supply or ground.)

LB3, LB2, LB1 bits

The LB3, LB2, LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S13-S11) that provide the write protect control and status for the Security Registers. The default state of LB3-LB1 is 0, with the security registers unprotected. The LB3-LB1 bits can be set to 1 individually using the Write Register (01H or 31H) command. The LB3-LB1 bits are One Time Programmable, once setting to 1, the corresponding Security Registers will become read-only permanently.

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the memory array protection. Please see the Table-9.X for protect area details. The default setting is CMP=0.

SUS1, SUS2 bit

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing a Program/Erase Suspend (75H or B0H) command. (The Erase Suspend will set the SUS1 to 1, and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by the Program/Erase Resume (7AH or 30H) command, the Software Reset (66H+99H) command as well as a power-down, power-up cycle.

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3.3 Configuration Register (CR)

Table-8. Status Register 3

S23	S22	S21	S20	S19	S18	S17	S16
HOLD/RST	DRV1	DRV0	Reserved	Reserved	Reserved	Reserved	DC
Non-volatile	Non-volatile	Non-volatile					Non-volatile

HOLD/RST bit

The HOLD/RST bit is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0, the pin acts as HOLD#, When the HOLD/RST=1, the pin acts as RESET#. However, the HOLD# or RESET# function are only available when QE=0, If QE=1, The HOLD# and RESET# functions are disabled, the pin acts as dedicated data I/O pin.

DRV1 & DRV0 bit

The DRV1 & DRV0 bits are non-volatile Read/Write bits which are used to determine the output driver strength for the Read operations.

DRV1,DRV0	Drive Strength
0,0(default)	100%
0,1	75%
1,0	50%
1,1	25%

DC bit

The Dummy Configuration (DC) bit is non-volatile, which selects the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional dummy cycles as the SCLK frequency increases.

The following dummy cycle tables provide different dummy cycle settings that are configured.

Command	DC bit	Numbers of Dummy Cycles	Freq.(MHz)
BBH	0 (default)	4	104
	1	8	133R
EBH	0 (default)	6	104
	1	10	133R

Note:

1. “R” means VCC range=3.0V~3.6V.

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3.4. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset to standby mode automatically during power up. In addition, the control register architecture of the device ensures that the memory contents can only be changed after specific command sequences have completed successfully.

- In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (06H) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits define the section of the memory array that can be read but not changed.
- Hardware Protection Mode: WP# going low to protect the CMP, BP0~BP4 bits and SRP0~1 bits.
- Deep Power-Down Mode: By entering deep power down mode, the flash device is ignores all commands until the Release from Deep Power-Down Mode (B9H) command.

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Table-9.1 ZD25Q128C Protected Area Size (CMP bit=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 to 255	FC0000H-FFFFFFH	256KB	Upper 1/64
0	0	0	1	0	248 to 255	F80000H-FFFFFFH	512KB	Upper 1/32
0	0	0	1	1	240 to 255	F00000H-FFFFFFH	1MB	Upper 1/16
0	0	1	0	0	224 to 255	E00000H-FFFFFFH	2MB	Upper 1/8
0	0	1	0	1	192 to 255	C00000H-FFFFFFH	4MB	Upper 1/4
0	0	1	1	0	128 to 255	800000H-FFFFFFH	8MB	Upper 1/2
0	1	0	0	1	0 to 3	000000H-03FFFFH	256KB	Lower1/64
0	1	0	1	0	0 to 7	000000H-07FFFFH	512KB	Lower1/32
0	1	0	1	1	0 to 15	000000H-0FFFFFH	1MB	Lower1/16
0	1	1	0	0	0 to 31	000000H-1FFFFFH	2MB	Lower 1/8
0	1	1	0	1	0 to 63	000000H-3FFFFFH	4MB	Lower 1/4
0	1	1	1	0	0 to 127	000000H-7FFFFFH	8MB	Lower 1/2
X	X	1	1	1	0 to 255	000000H-FFFFFFH	16MB	ALL
1	0	0	0	1	255	FFF000H-FFFFFFH	4KB	Top Block
1	0	0	1	0	255	FFE000H-FFFFFFH	8KB	Top Block
1	0	0	1	1	255	FFC000H-FFFFFFH	16KB	Top Block
1	0	1	0	X	255	FF8000H-7FFFFFH	32KB	Top Block
1	0	1	1	0	255	FF8000H-7FFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H - 000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H - 001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H - 003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H - 007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H - 007FFFH	32KB	Bottom Block

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Table-9.2 ZD25Q128C Protected Area Size (CMP bit=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	ALL	000000H- FFFFFFH	ALL	ALL
0	0	0	0	1	0 to 251	000000H- FBFFFFH	16128KB	Lower 63/64
0	0	0	1	0	0 to 247	000000H- F7FFFFH	15872KB	Lower 31/32
0	0	0	1	1	0 to 239	000000H- EFFFFFH	15MB	Lower15/16
0	0	1	0	0	0 to 223	000000H- DFFFFFH	14MB	Lower 7/8
0	0	1	0	1	0 to 191	000000H- BFFFFFH	12MB	Lower 3/4
0	0	1	1	0	0 to 127	000000H- 7FFFFFH	8MB	Lower 1/2
0	1	0	0	1	4 to 255	040000H- FFFFFFH	16128KB	Upper 63/64
0	1	0	1	0	8 to 255	080000H- FFFFFFH	15872KB	Upper 31/32
0	1	0	1	1	16 to 255	100000H- FFFFFFH	15MB	Upper 15/16
0	1	1	0	0	32 to 255	200000H- FFFFFFH	14MB	Upper 7/8
0	1	1	0	1	64 to 255	400000H- FFFFFFH	12MB	Upper 3/4
0	1	1	1	0	128 to 255	800000H- FFFFFFH	8MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 255	000000H-FFEFFFH	16380KB	L-4095/4096
1	0	0	1	0	0 to 255	000000H- FFDFFFH	16376KB	L-2047/2048
1	0	0	1	1	0 to 255	000000H-FFBFFFH	16368KB	L-1023/1024
1	0	1	0	X	0 to 255	000000H-FF7FFFH	16352KB	L-511/512
1	0	1	1	0	0 to 255	000000H-FF7FFFH	16352KB	L-511/512
1	1	0	0	1	0 to 255	001000H-FFFFFFH	16380KB	U-4095/4096
1	1	0	1	0	0 to 255	002000H-FFFFFFH	16376KB	U- 2047/2048
1	1	0	1	1	0 to 255	004000H-FFFFFFH	16368KB	U- 1023/1024
1	1	1	0	X	0 to 255	008000H-FFFFFFH	16352KB	U- 511/512
1	1	1	1	0	0 to 255	008000H-FFFFFFH	16352KB	U- 511/512

Notes:

1. X=don't care
2. If any erase or program command specifies a memory that contains protected data portion, this command will be ignored.

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4. COMMAND DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted into the device starting with the most significant bit on SI. Each bit is latched on the rising edge of SCLK.

The commands supported by ZD25Q128C are listed in Table-10. Every command sequence starts with a one-byte command code. Depending on the command, it might be followed by address or data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the commands of Read, Fast Read, Read Status Register, Release from Deep Power- Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read commands can be completed after any bit of the data-out sequence is shifted out, and then CS# must be driven high to return to deselected status.

For the Page Program , Sector Erase, Block Erase , Chip Erase , Write Status Register , Write Enable , Write Disable or Deep Power-Down commands, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That means CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if CS# is driven high at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table-10. Commands (Standard/Dual/Quad SPI)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Write Enable	06H								
Write Disable	04H								
Volatitle SR Write Enable	50H								
Read Status Register-1	05H	(S7-S0)	(cont.)						
Read Status Register-2	35H	(S15-S8)	(cont.)						
Read Status Register-3	15H	(S23-S16)	(cont.)						
Write Status Register-1	01H	S7-S0							
Write Status Register-1&2	01H	S7-S0	S15-S8						
Write Status Register-2	31H	S15-S8							
Write Status Register-3	11H	S23-S16							
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)			
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Dual I/O Fast Read	BBH	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)	(cont.)		
Quad I/O Fast Read	EBH	A23-A16	A15-A8	A7-A0	M7-M0	dummy	dummy	(D7-D0)	(cont.)

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Commands (Standard/Dual/Quad SPI)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte8	Byte 9	Byte 10
Set Burst with Wrap	77H	dummy	dummy	dummy	W7-W0					
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte				
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte				
Sector Erase	20H	A23-A16	A15-A8	A7-A0						
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0						
Chip Erase	C7/60H									
Read Manufacturer/Device ID	90H	dummy	dummy	A7-A0	(MID7-MID0)	(ID7-ID0)	(cont.)			
Read Identification	9FH	(MID7-MID0)	(ID15-ID8)	(ID7-ID0)	(cont.)					
Read Unique ID	4BH	dummy	dummy	dummy	dummy	(UID7-UID0)	(cont.)			
Erase Security Registers	44H	A23-A16	A15-A8	A7-A0						
Program Security Registers	42H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte				
Read Security Registers	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)			
Enable Reset	66H									
Reset	99H									
Program/Erase Suspend	75H									
Program/Erase Resume	7AH									
Deep Power-Down	B9H									
Release From Deep Power-Down	ABH									
Release From Deep Power-Down and Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)	(cont.)				
Read Serial Flash Discoverable Parameter	5AH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)			
Enable QPI	38H									

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Command set (QPI)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	(0,1)	(2,3)	(4,5)	(6,7)	(8,9)	(10,11)	(12,13)	(14,15)
Write Enable	06H							
Write Disable	04H							
Read Status Register-1	05H	(S7-S0)	(cont.)					
Read Status Register-2	35H	(S15-S8)	(cont.)					
Read Status Register-3	15H	(S23-S16)	(cont.)					
Write Status Register-1	01H	S7-S0						
Write Status Register-1&2	01H	S7-S0	S15-S8					
Write Status Register-2	31H	S15-S8						
Write Status Register-3	11H	S23-S16						
Volatile SR Write Enable	50H							
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)	(cont.)
Quad I/O Fast Read	EBH	A23-A16	A15-A8	A7-A0	M7-M0	dummy	(D7-D0)	(cont.)
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte		
Sector Erase	20H	A23-A16	A15-A8	A7-A0				
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0				
Chip Erase	C7/60H							
Set Read Parameters	C0H	P7-P0						
Manufacturer/Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(ID7-ID0)	(cont.)	
Read Identification	9FH	MID7-MID0	ID15-ID8	ID7-ID0	(cont.)			
Enable Reset	66H							
Reset	99H							
Burst Read with Wrap	0CH	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)	(cont.)
Program/Erase Suspend	75H							
Program/Erase Resume	7AH							
Deep Power-Down	B9H							
Release from Deep Power-Down Release From Deep	ABH							
Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)	(cont.)		
Disable QPI	FFH							
Read Serial Flash Discoverable Parameter	5AH	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)	(cont.)

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Command set (DTR with SPI)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock	8	4	4	4	6	4	4
DTR Fast Read	0DH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)
Number of Clock	8	2	2	2	6	2	2
DTR Fast Read Dual I/O	BDH	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)	(cont.)
Number of Clock	8	1	1	1	8	1	1
DTR Fast Read Quad I/O	EDH	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)	(cont.)

Command set (DTR with QPI)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock	2	1	1	1	8	1	1
DTR Read with Wrap	0EH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)
DTR Fast Read	0DH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)
DTR Fast Read Quad I/O	EDH	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)	(cont.)

Notes:

1. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)

2. Dual Input Address
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3,…..)

4. Quad Input Address
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Fast Read Quad I/O Dummy Bits and Data
   IO0 = (x, x, x, x, D4, D0,…)
   IO1 = (x, x, x, x, D5, D1,…)
   IO2 = (x, x, x, x, D6, D2,…)
   IO3 = (x, x, x, x, D7, D3,…)

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6. Security Registers Address:

Security Register1: A23-A16=00H, A15-A12=1H, A11-A10 = 00b, A9-A0= Byte Address;
Security Register2: A23-A16=00H, A15-A12=2H, A11-A10 = 00b, A9-A0= Byte Address;
Security Register3: A23-A16=00H, A15-A12=3H, A11-A10 = 00b, A9-A0= Byte Address;

7. Dummy bits and Wrap Bits

IO0 = (x, x, x, x, x, x, W4, x)
IO1 = (x, x, x, x, x, x, W5, x)
IO2 = (x, x, x, x, x, x, W6, x)
IO3 = (x, x, x, x, x, x, x, x)

8. QPI Command, Address, Data input/output format:

CLK #0 1 2 3 4 5 6 7 8 9 10 11
IO0= C4, C0, A20, A16, A12, A8, A4, A0, D4, D0, D4, D0
IO1= C5, C1, A21, A17, A13, A9, A5, A1, D5, D1, D5, D1
IO2= C6, C2, A22, A18, A14, A10, A6, A2, D6, D2, D6, D2
IO3= C7, C3, A23, A19, A15, A11, A7, A3, D7, D3, D7, D3

Tables of ID Definition:

Table-11 ZD25Q128C

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	BA	40	18
90H	BA		17
ABH			17

4.1 Write Enable (WREN) (06H)

The Write Enable (06H) command sets the Write Enable Latch (WEL) bit. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Register command. The WREN command is entered by driving Chip Select (CS#) Low, sending the command code, and then driving CS# High.

Figure-4. Write Enable Sequence Diagram

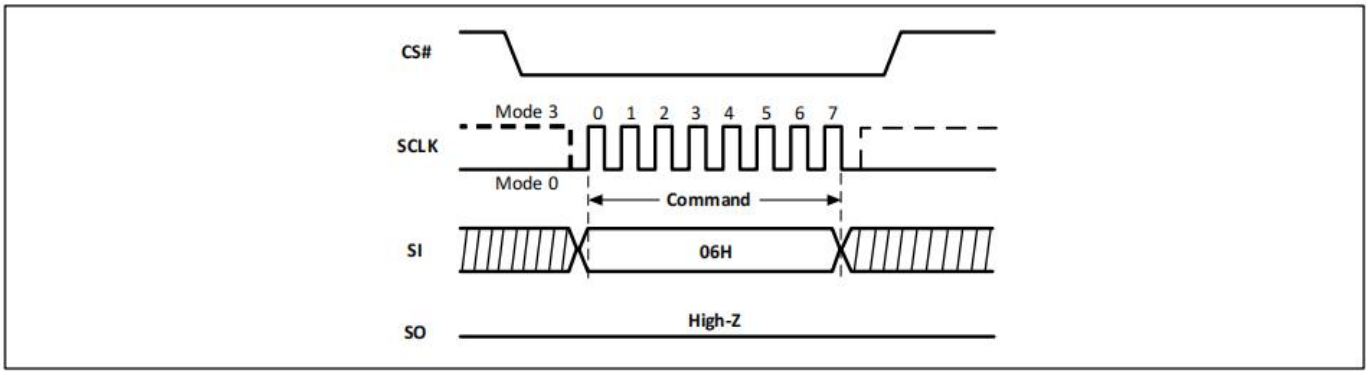
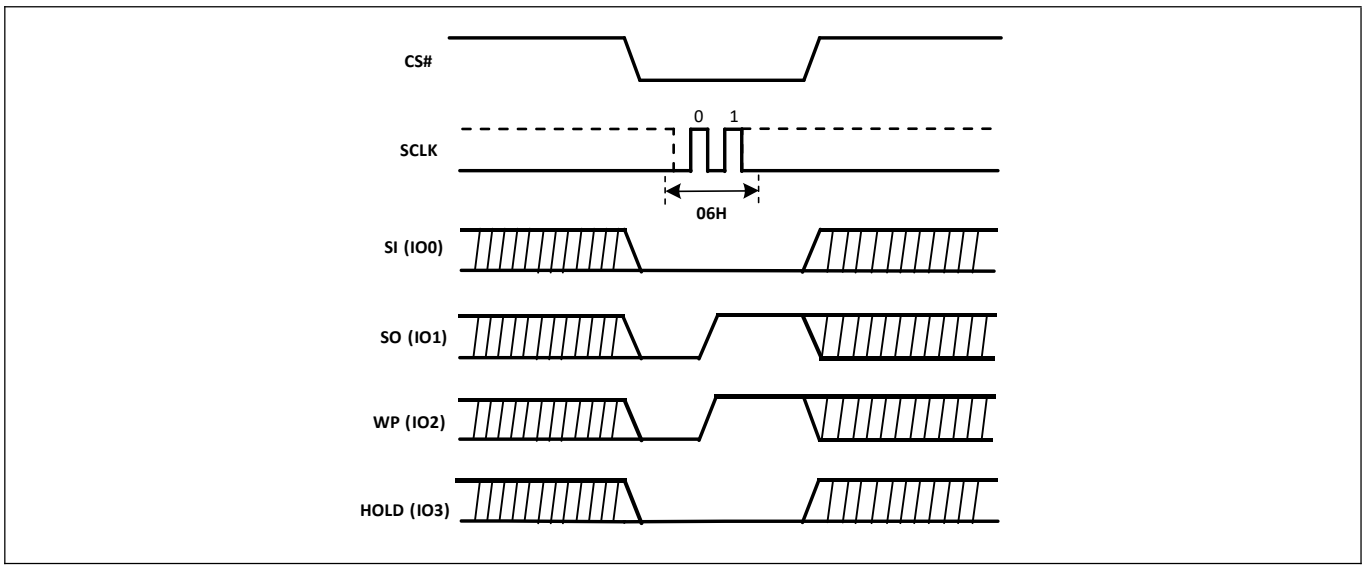


Figure-5. Write Enable (WREN) Sequence (QPI)



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4.2 Write Disable (WRDI) (04H)

The Write Disable (04H) command resets the Write Enable Latch (WEL) bit in the Status Register to 0. The WRDI command is entered by driving Chip Select (CS#) low, shifting the command code "04h" into the SI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase, Chip Erase, Erase/Program Security Register and Reset commands.

Figure-6. Write Disable Sequence Diagram

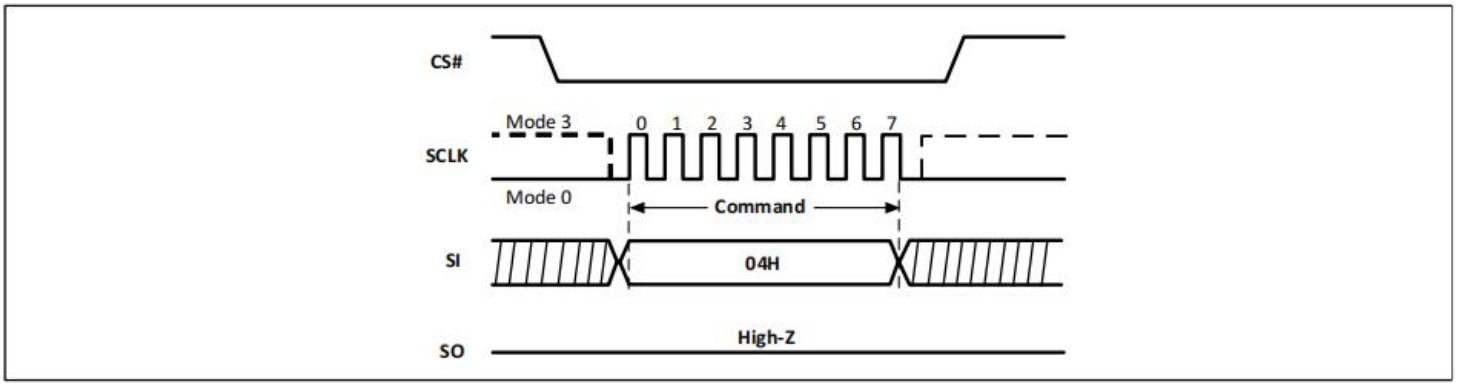
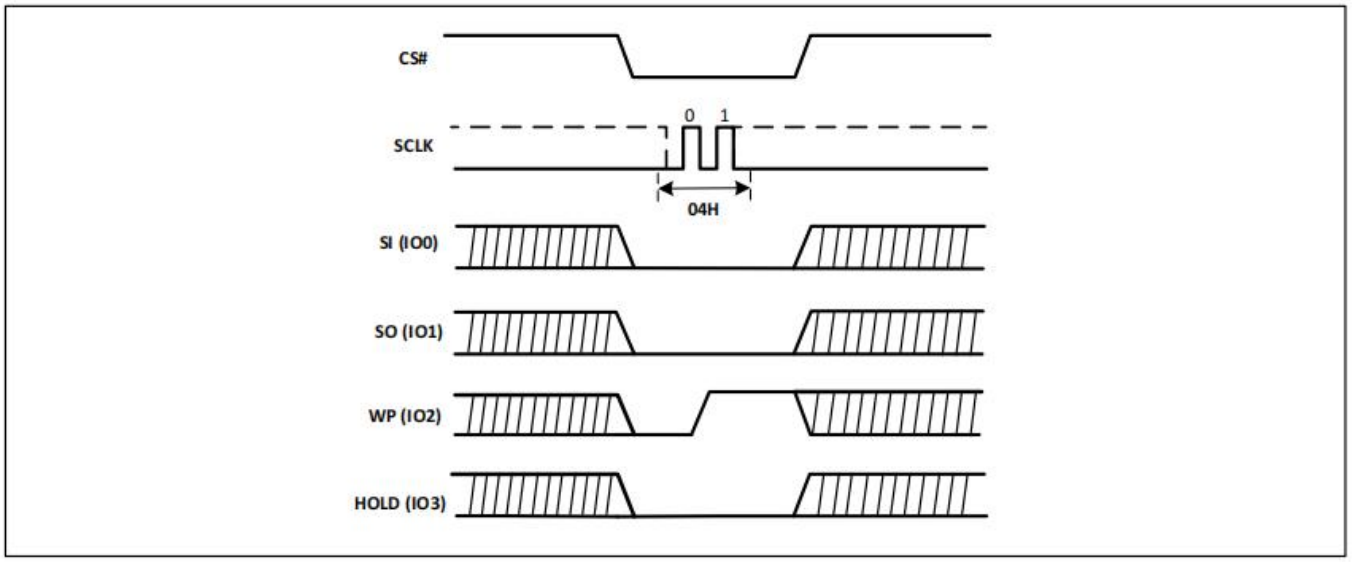


Figure-7. Write Disable Sequence Diagram (QPI)



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4.3 Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. During power up reset, the non-volatile Status Register bits are copied to a volatile version of the Status Register that is used during device operation. This provides more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits.

To write the volatile version of the Status Register bits, the Write Enable for Volatile Status Register (50H) command must be issued and immediately followed by the Write Status Register (01H/11H/31H) command. Write Enable for Volatile Status Register command (Figure-8) will not set the Write Enable Latch (WEL) bit, it is only valid for the next Write Status Register command, to change the volatile Status Register bit values.

Figure-8. Write Enable for Volatile Status Register Sequence Diagram

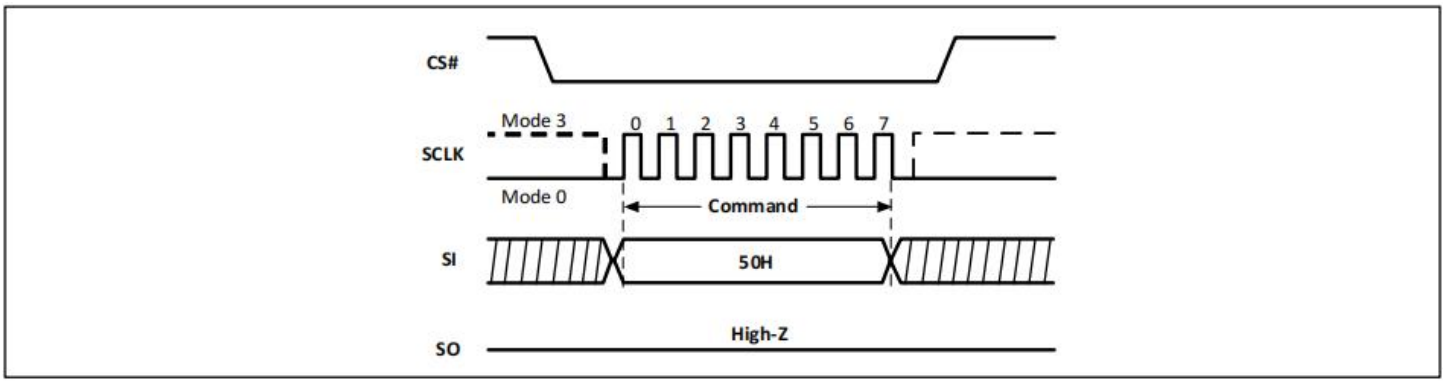
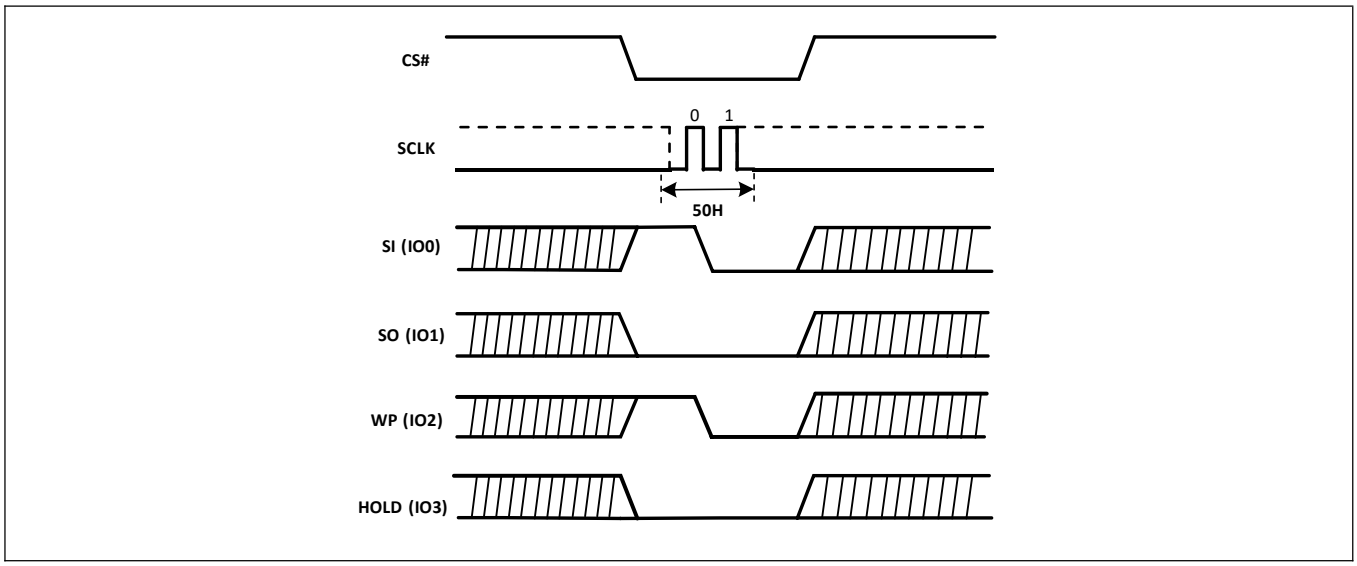


Figure-9. Write Enable for Volatile Status Register Sequence Diagram (QPI)



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4.4 Read Status Register (RDSR) (05H or 35H or 15H)

The Read Status Register (05H/35H/15H) command allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code of “05H” / “35H” / “15H”, the SO will output Status Register bits S7~S0 / S15~S8 / S23~S16.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Figure-10. Read Status Register Sequence Diagram

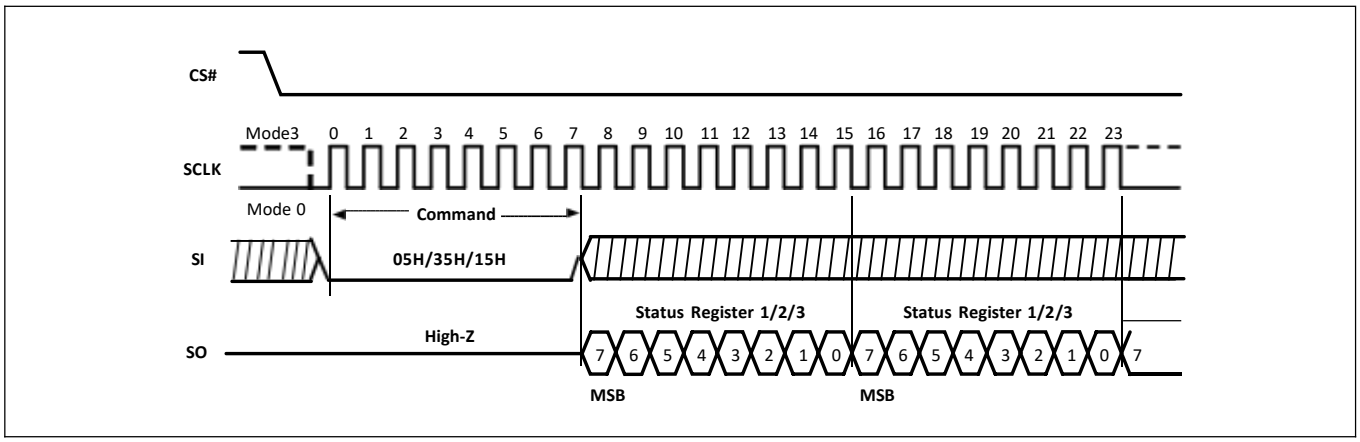
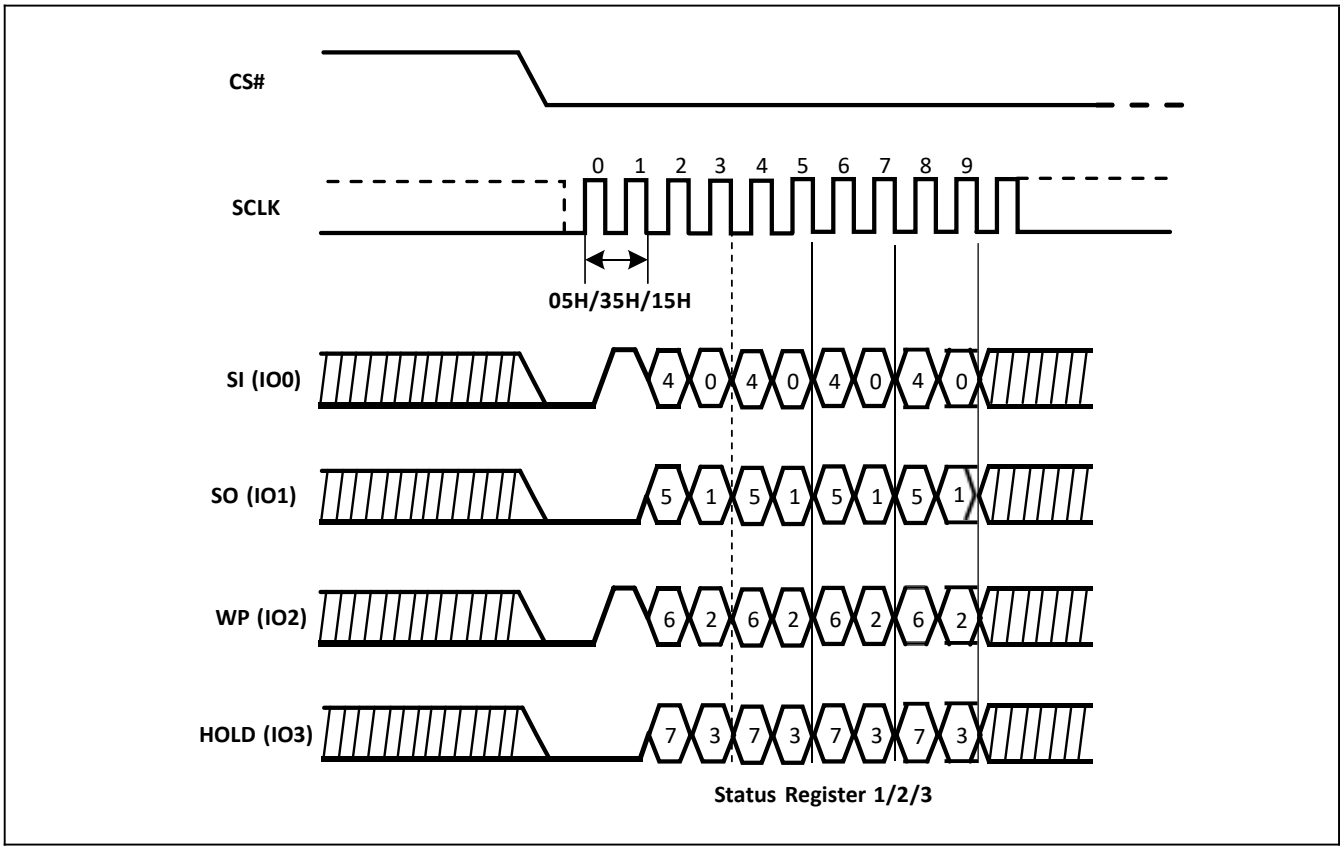


Figure-11. Read Status Register Sequence Diagram (QPI)



4.5 Write Status Register (WRSR) (01H or 31H or 11H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15, S10, S1 and S0 of the Status Register. For command code of “01H” / “31H” / “11H”, the Status Register bits S7~S0 / S15~S8 / S23~S16 would be written. CS# must be driven high after the eighth bit of the data byte has been latched in. Otherwise, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

Figure-12. Write Status Register Sequence Diagram

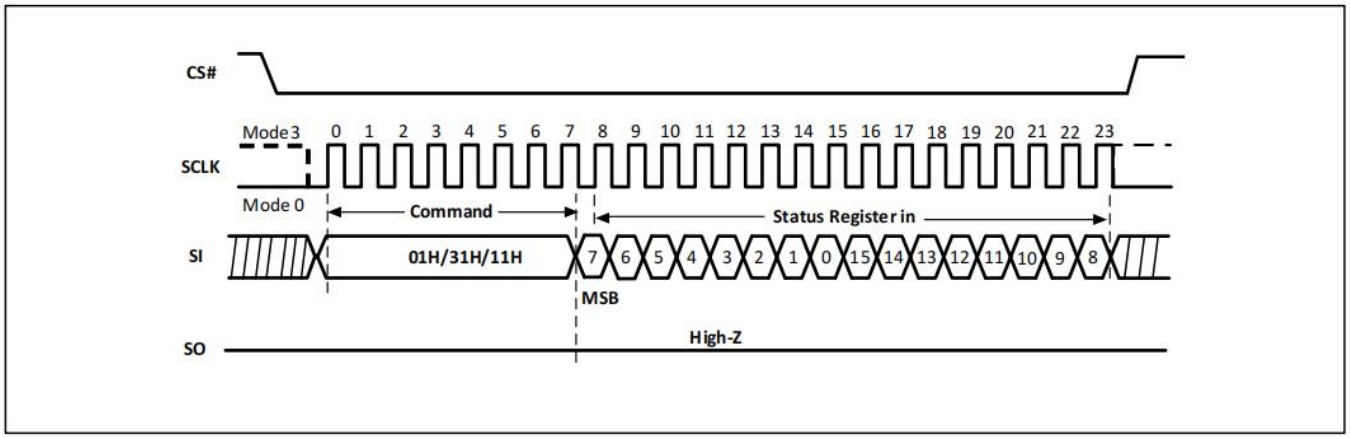
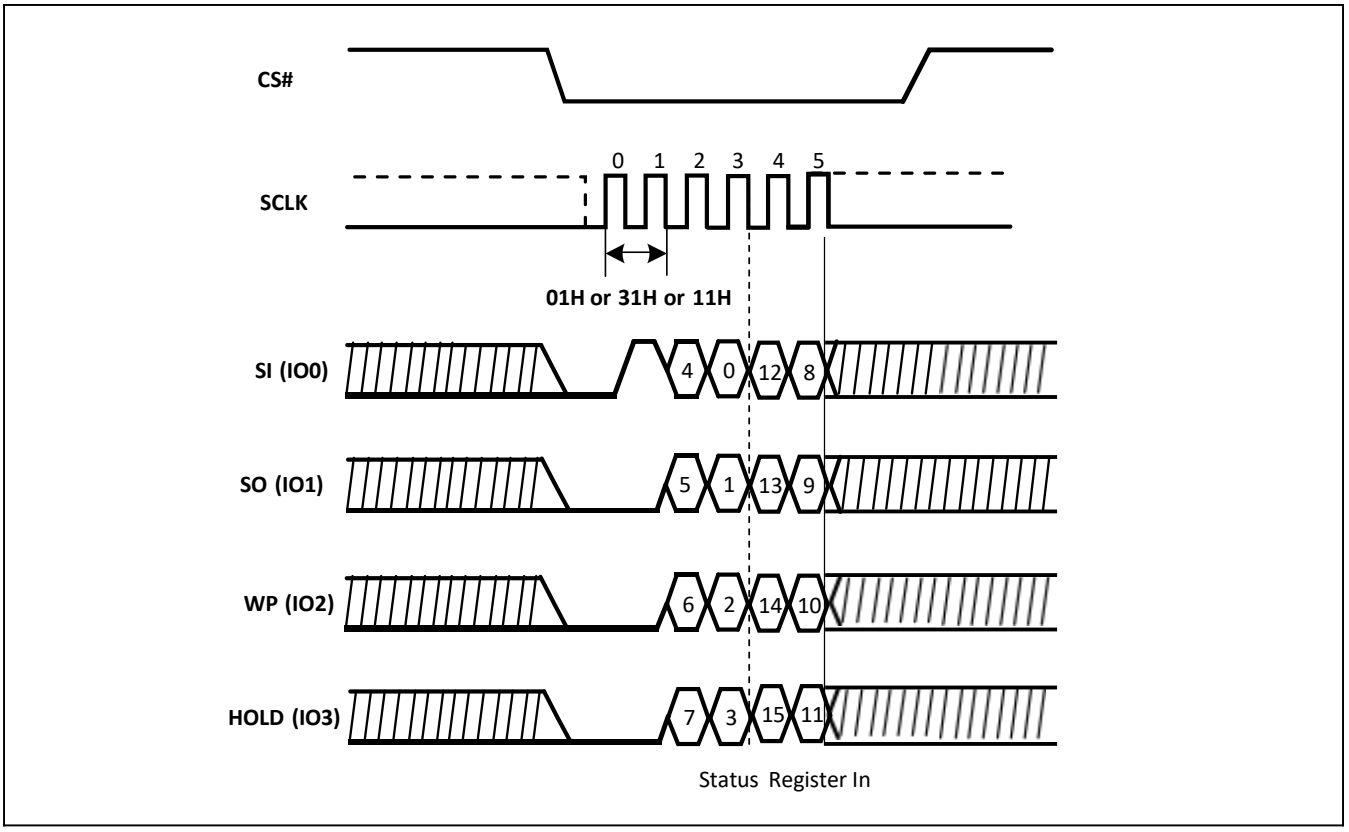


Figure-13. Write Status Register Sequence Diagram（QPI）



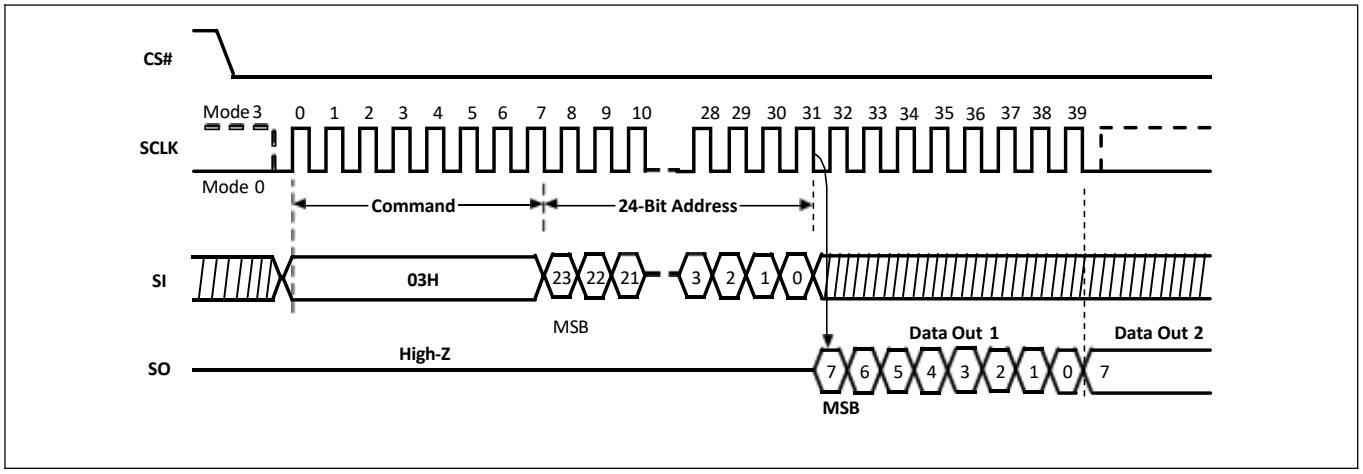
4.6 Read Data Bytes (READ) (03H)

The device is first selected by driving Chip Select (CS#) Low. The command code for the Read Data Bytes (03H) command is followed by a 3-byte address (A23-A0), with each bit latched-in on the rising edge of Serial Clock (SCLK). Then the memory contents, at that address, is shifted out on Data Output (SO), with each bit shifted out at a maximum frequency fR on the falling edge of SCLK.

The command sequence is shown in Figure-14. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single READ command. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The READ command is terminated by driving CS# High. CS# can be driven High at any time during data output. Any READ command to the memory array, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure-14. Read Data Bytes Sequence Diagram



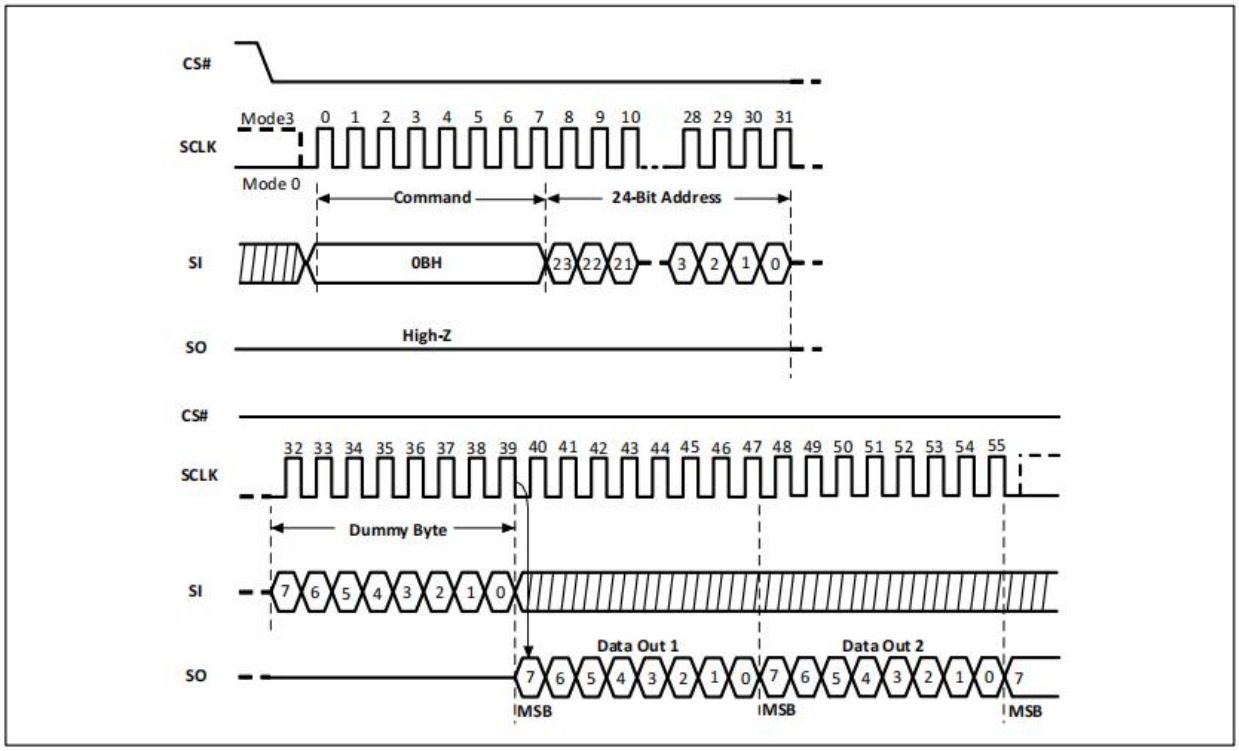
4.7 Read Data Bytes at Higher Speed (FAST_READ) (0BH)

The device is first selected by driving Chip Select (CS#) Low. The command code for the Read Data Bytes at Higher Speed (0BH) command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in on the rising edge of Serial Clock (SCLK). Then the memory contents, at that address, is shifted out on Data Output (SO), with each bit shifted out at a maximum frequency fC on the falling edge of SCLK.

The command sequence is shown in Figure-15. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single FAST_READ command. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The FAST_READ command is terminated by driving CS# High. CS# can be driven High at anytime during data output. Any FAST_READ command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

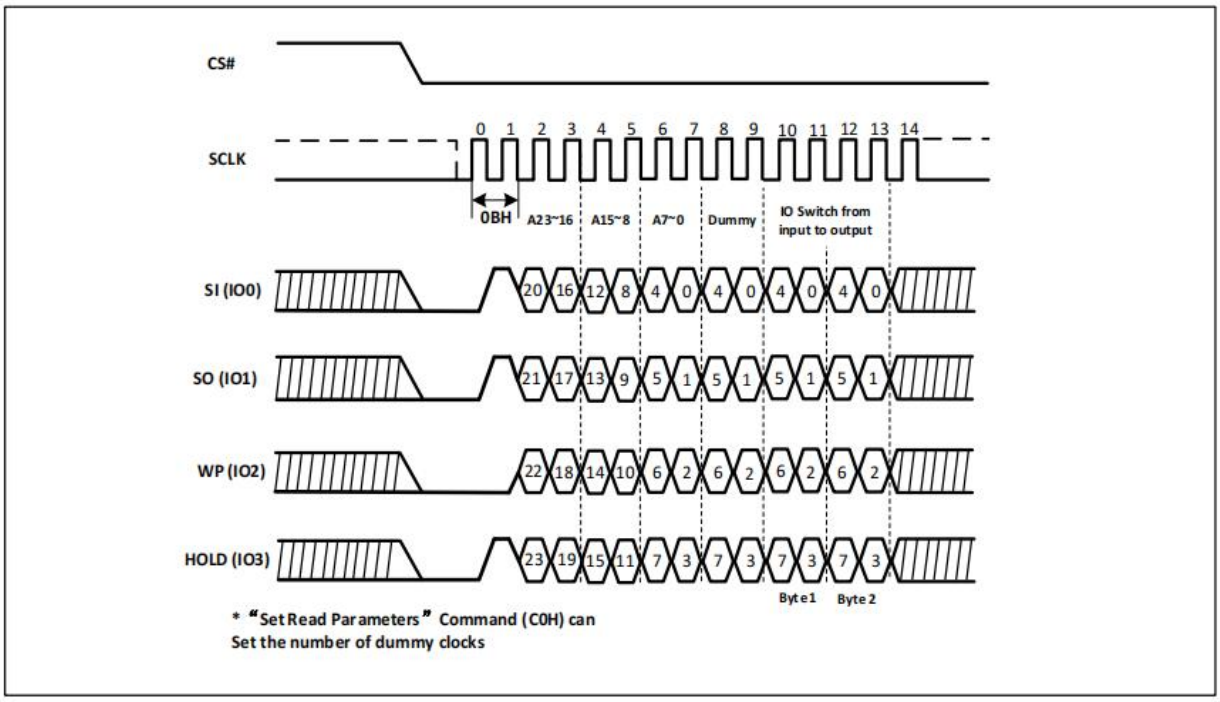
Figure-15. Read Data Bytes at Higher Speed Sequence Diagram



Read Data Bytes at Higher Speed in QPI mode

The Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the “Set Read Parameters (C0H)” command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8.

Figure-16. Read Data Bytes at Higher Speed Sequence Diagram (QPI)



4.8 DTR Fast Read (0Dh)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24-bit address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding six “dummy” clocks after the 24-bit address as shown in Figure-17. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

Figure-17. DTR Fast Read Sequence Diagram (SPI)

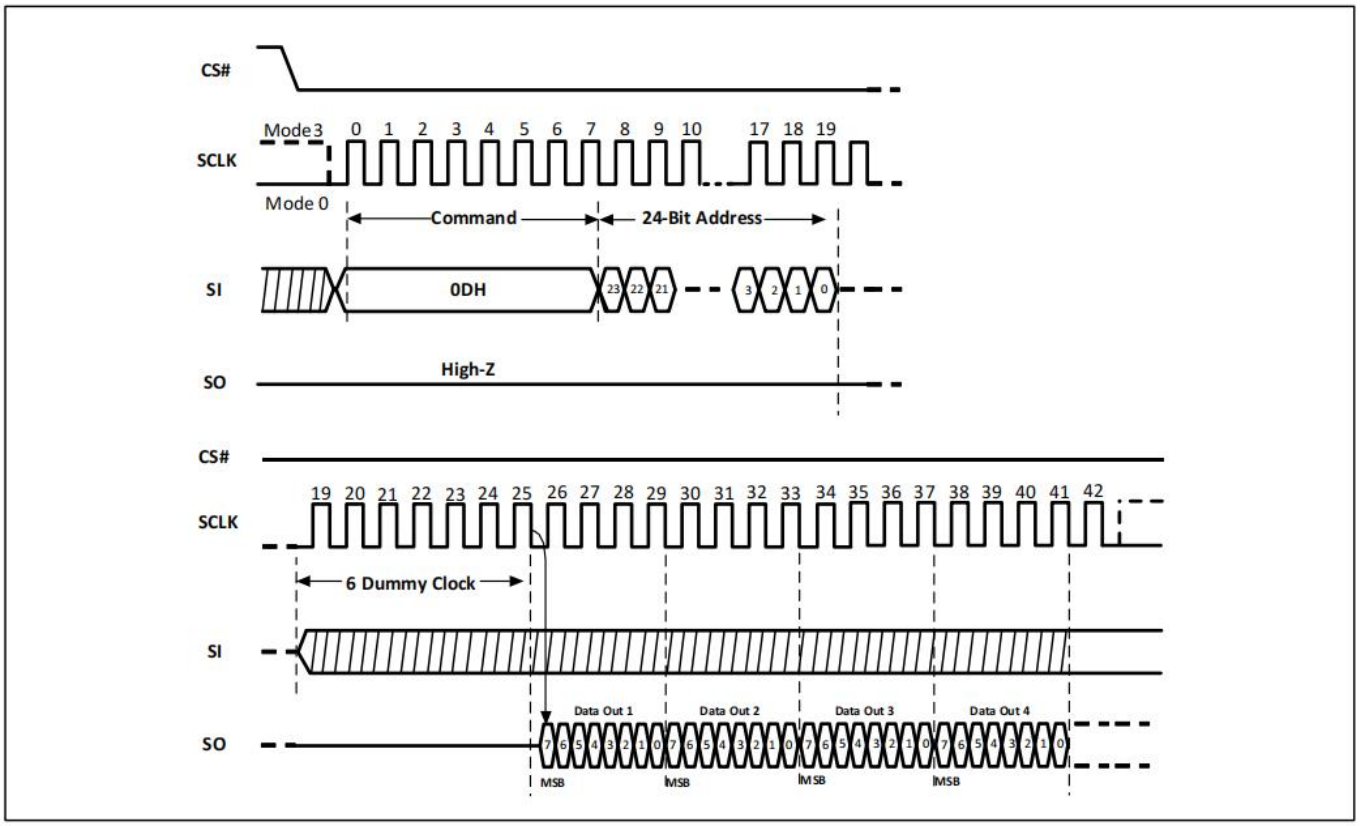
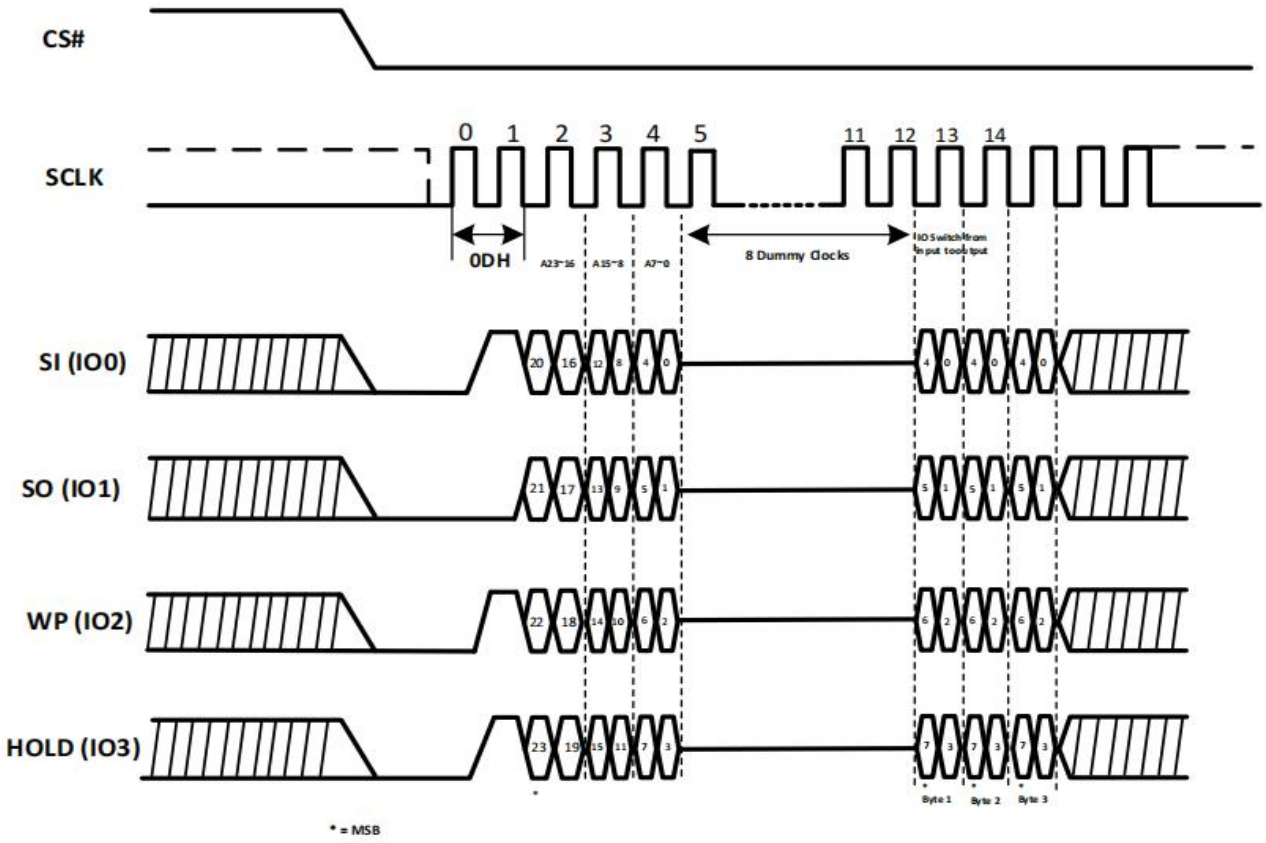


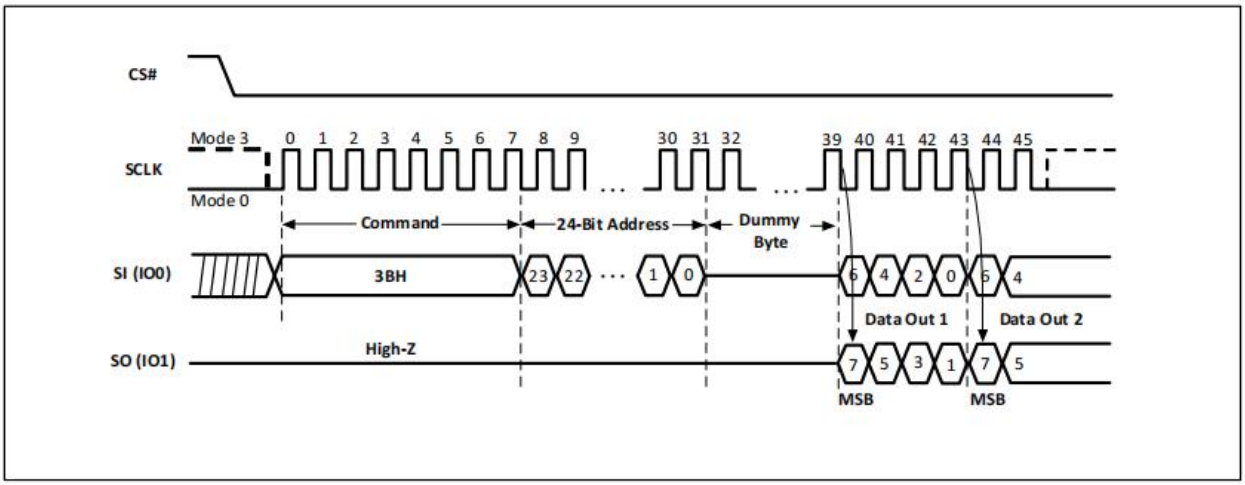
Figure-18. DTR Fast Read Sequence Diagram (QPI)



4.9 Dual Output Fast Read (DREAD) (3BH)

The Dual Output Fast Read (3BH) is similar to the standard Fast Read (0BH) command except that data is output on two pins, SI (IO0) and SO (IO1), instead of just SO. This allows data to be transferred from the ZD25Q128 at twice the rate of standard SPI devices. The DREAD command is ideal for quickly downloading code from the flash to RAM upon power-up or for applications that cache code-segments to RAM for execution. Like the Fast Read command, the DREAD command can operate at the highest possible frequency of fT. This is accomplished by adding eight “dummy clocks after the 24-bit address as shown in Figure-19. The dummy clocks allow the device’s internal circuits the time required for setting up the initial address. The input data during the dummy clock is “don’t care”. However, the SI pin should be in a high-impedance state prior to the falling edge of SLCK for the first data out.

Figure-19. Dual Output Fast Read Sequence Diagram

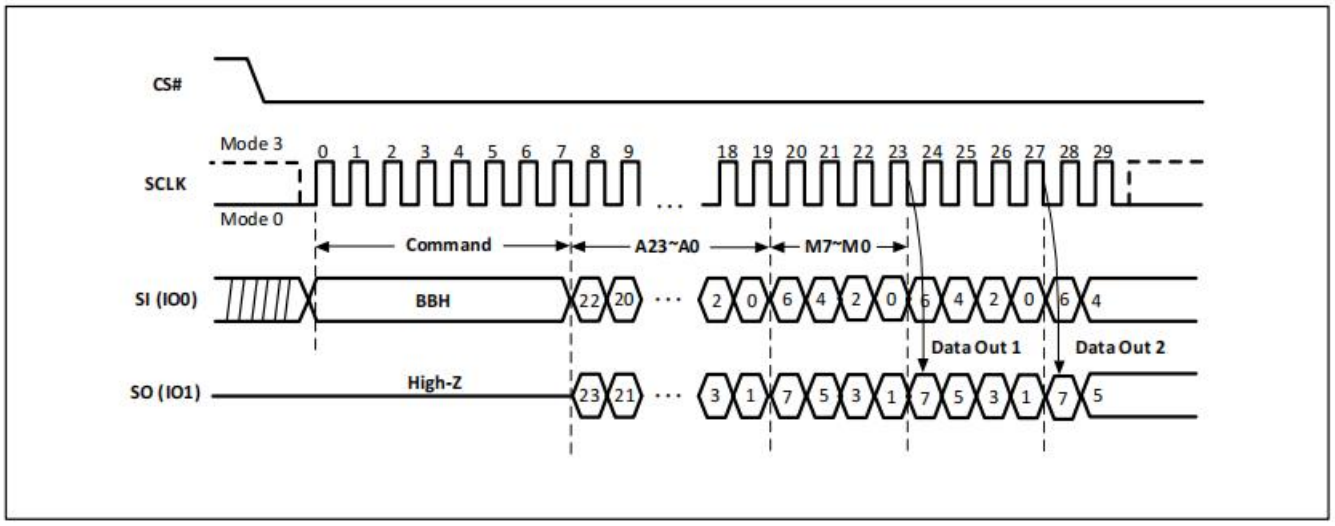


4.10 Dual I/O Fast Read (2READ) (BBH)

The Dual I/O Fast Read (BBH) command allows for improved random access while maintaining two IO pins, SI (IO0) and SO (IO1). It is similar to the Dual Output Fast Read (3BH) command but with the ability to input the address bits (A23-0) two bits per clock. This reduced command overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The 2READ command enables double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and two bits of data (interleave 2 I/O pins) are shifted out on the falling edge of SCLK at a maximum frequency fT. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out with a single 2READ command. The address counter rolls over to 0 when the highest address has been reached. The 2READ command is shown in Figure-20.

Figure-20. Dual I/O Fast Read Sequence Diagram (M5-4 ≠ (1,0))

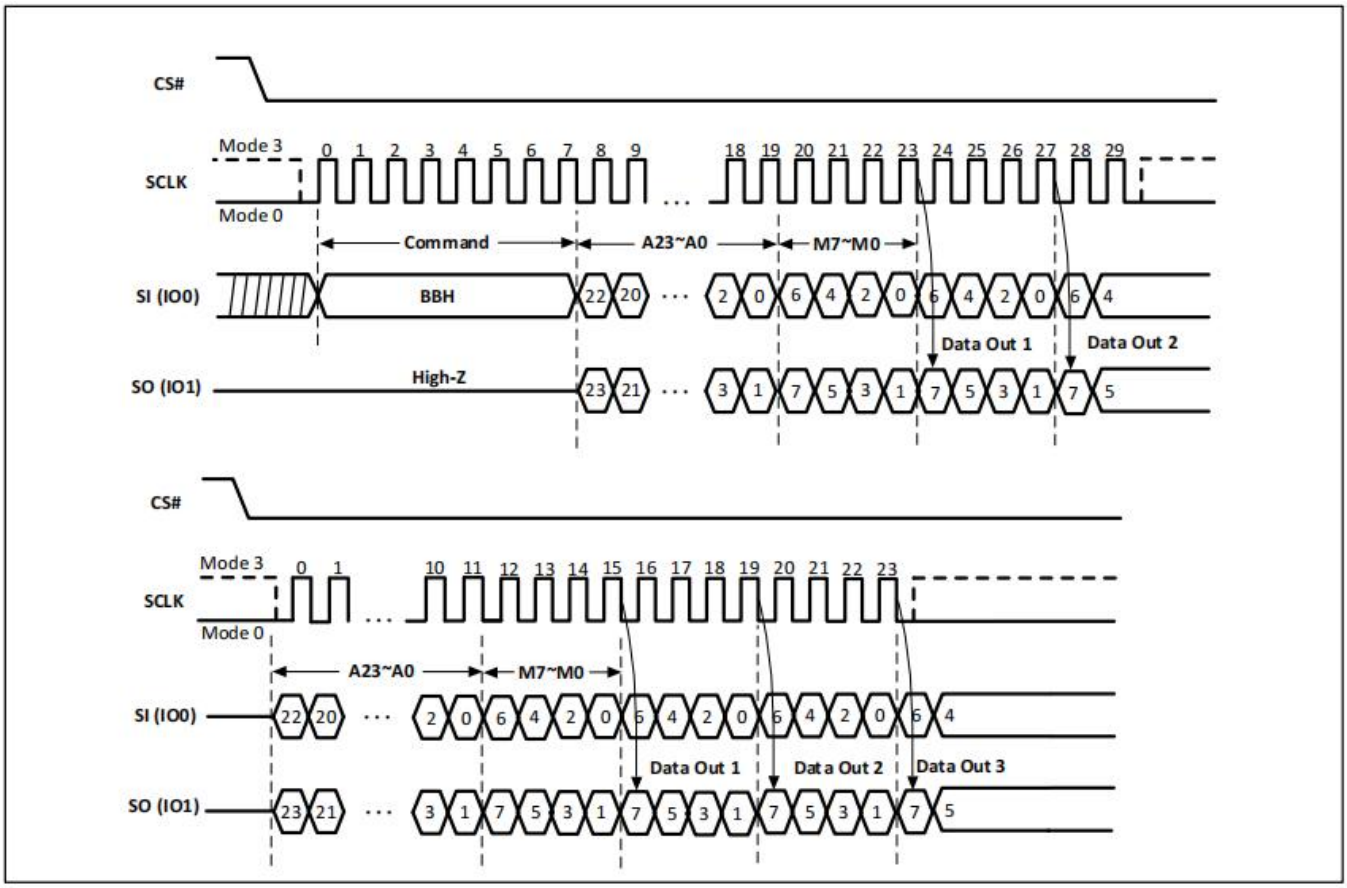


Dual I/O Fast Read with "Continuous Read Mode" (BBH)

The Dual I/O Fast Read (BBH) command supports Dual I/O Fast Read with "Continuous Read Mode" which can further reduce command overhead by setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code.

If the "Continuous Read Mode" bits (M5-4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing a normal command.

Figure-21. Dual I/O Fast Read with "Continuous Read Mode" Sequence Diagram (M5-4 = (1,0))



Note: Dual I/O Fast Read with "Continuous Read Mode", if (M5-4)=(1,0). If not using "Continuous Read Mode" recommend setting (M5-4)≠(1,0).

4.11 DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/O (BDh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

DTR Fast Read Dual I/O with "Continuous Read Mode"

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure-22. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure-23. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh/FFFFFh on IO0 for the next instruction (16/20 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure-22. DTR Fast Read Dual I/O Sequence Diagram (M5-4 ≠ (1,0))

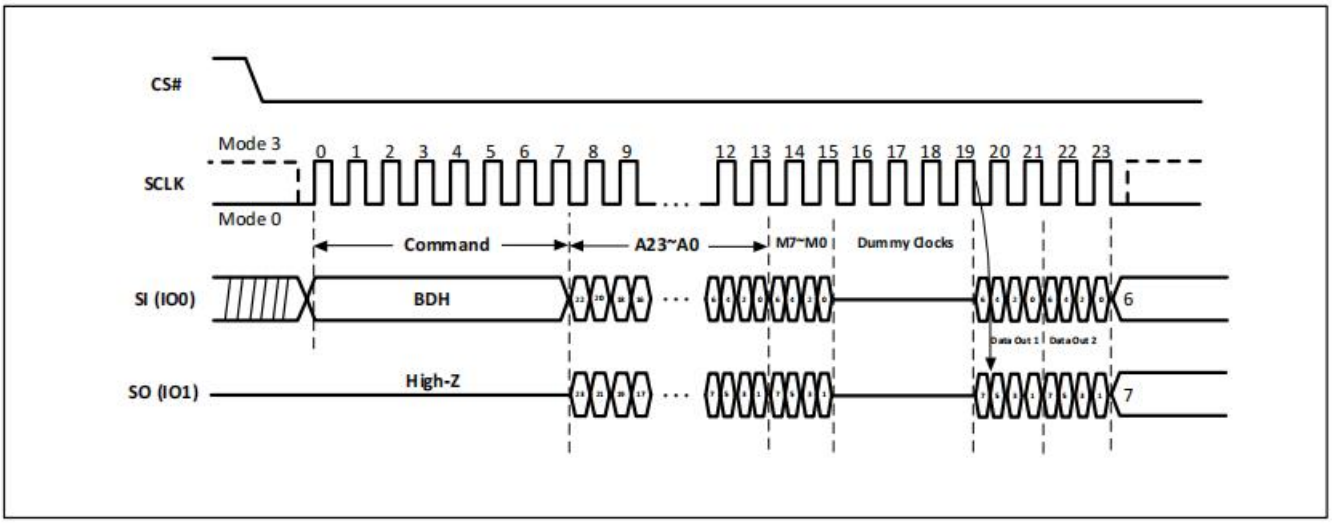
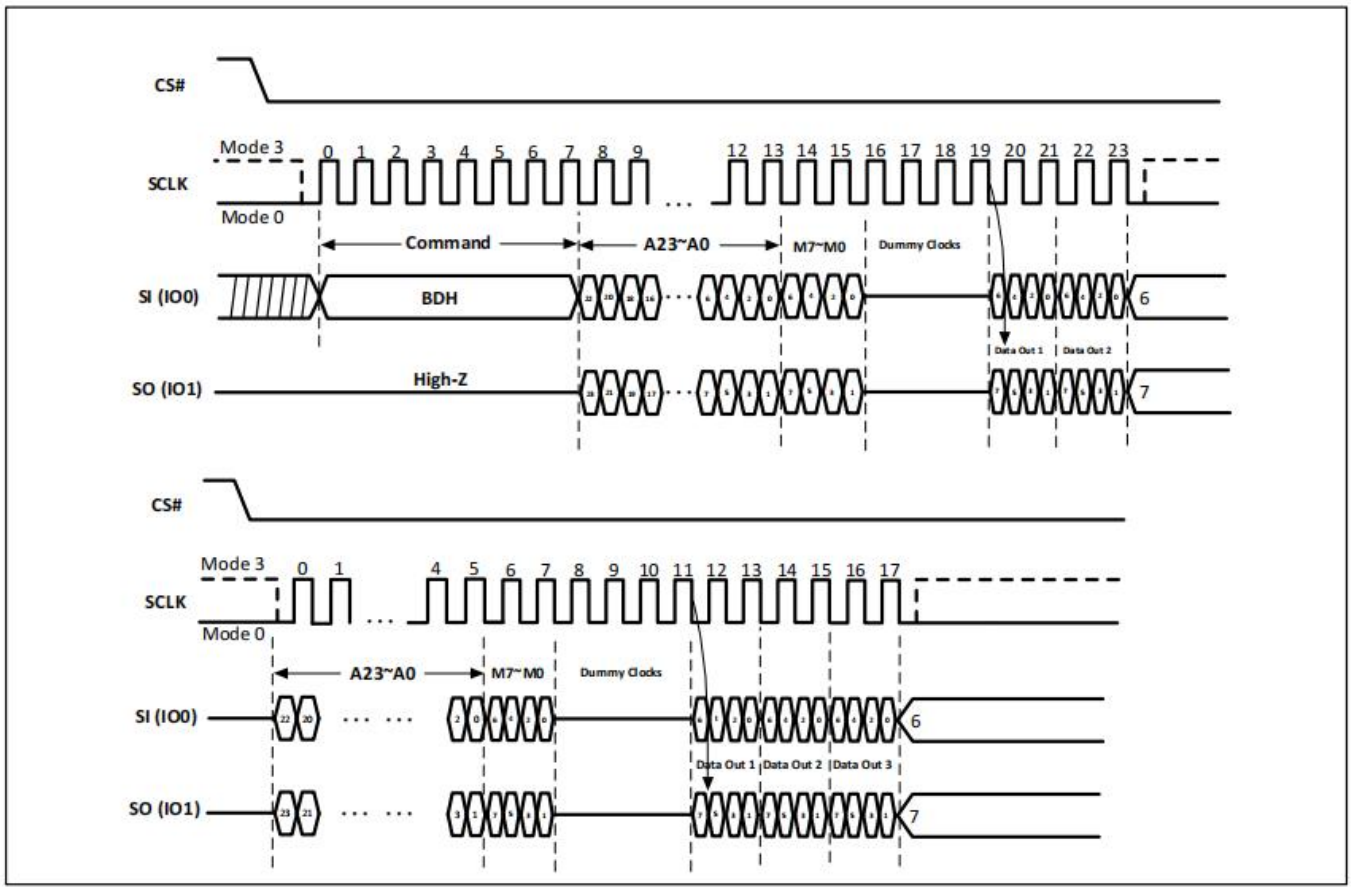


Figure-23. DTR Fast Read Dual I/O with "Continuous Read Mode" Sequence Diagram (M5-4 = (1,0))



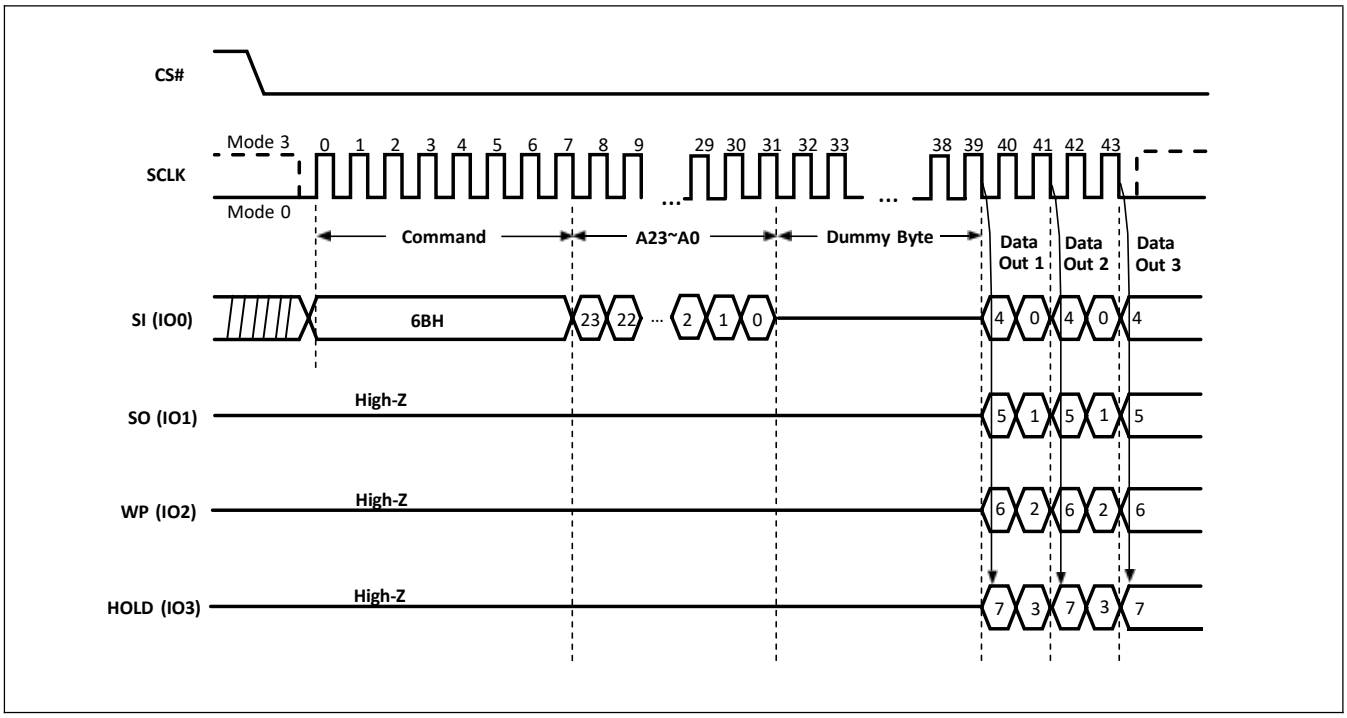
4.12 Quad Output Fast Read (QREAD) (6BH)

The Quad Output Fast Read (6BH) command is similar to the Dual Output Fast Read (3BH) command except that data is output on four pins, IO0, IO1, IO2, and IO3. A Quad Enable (QE) of Status Register-2 must be executed before the device will accept the QREAD Command. (The QE bit must equal "1"). The QREAD Command allows data to be transferred at four times the rate of standard SPI devices.

The QREAD command can operate at a higher frequency than the traditional Read Data command. This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure-24. The dummy clocks allow the device's internal circuits the time required for setting up the initial address. The input data during the dummy clocks is "don't care." However, the IO pins should be in a high-impedance state prior to the

falling edge of SCLK for the first data out.

Figure-24. Quad Output Fast Read Sequence Diagram



4.13 Quad I/O Fast Read (4READ) (EBH)

The Quad I/O Fast Read (EBH) command is similar to the Dual I/O Fast Read (BBH) command except that address and data bits are input and output through four pins, SI (IO0), SO (IO1), WP (IO2) and HOLD (IO3). Six dummy clocks are required prior to the data output. A Quad Enable (QE) of Status Register-2 must be executed before the device will accept the 4READ Command. (The QE bit must equal “1”). The Quad I/O dramatically reduces command overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The 4READ command enables quad throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data four bits of data (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out with a single 4READ command. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ command, the following address / dummy / data out will transfer 4-bits per clock cycle instead of the previous 1-bit.

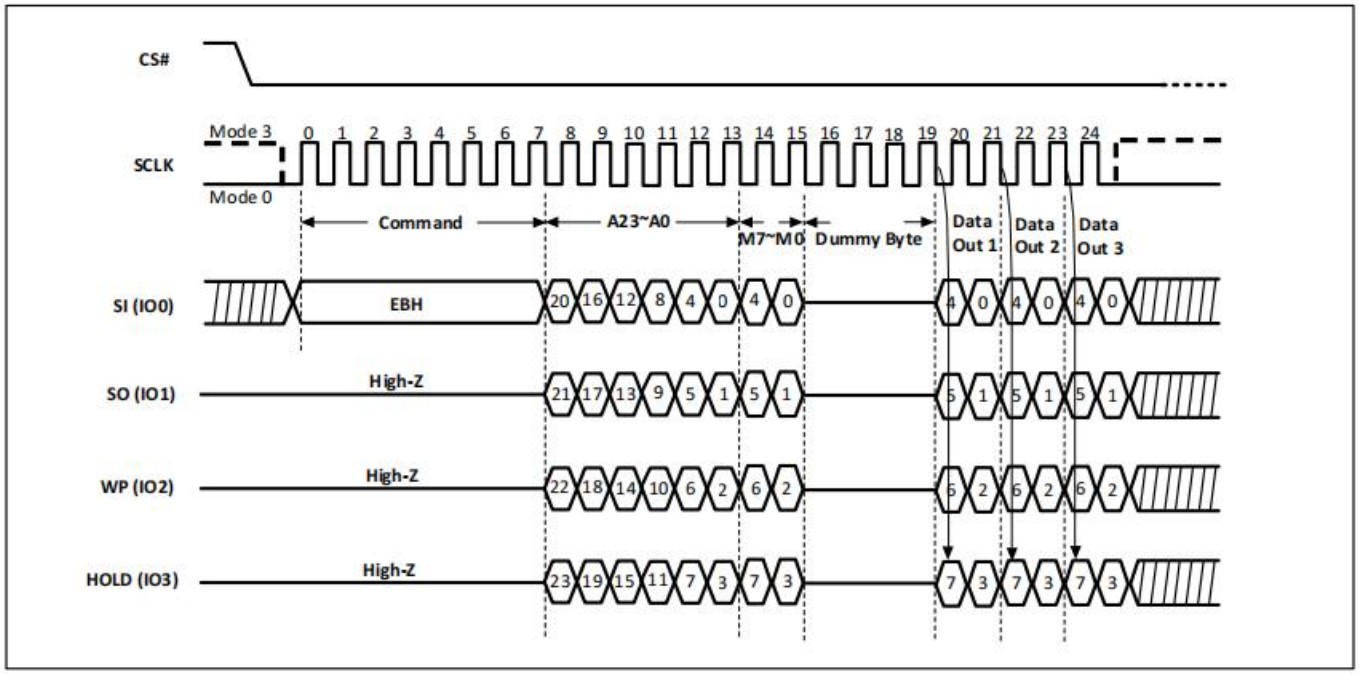
The sequence of issuing 4READ command is: CS# goes low -> send Quad I/O Fast Read (EBH) command -> 24-bit address interleave on IO3, IO2, IO1 and IO0 -> 2+4 dummy cycles -> data out interleave on IO3, IO2, IO1 and IO0 -> end 4READ operation by driving CS# high at any time during data out, as shown in Figure-25.

Another sequence of issuing 4READ command especially useful in random access is: CS# goes low -> send Quad I/O Fast Read (EBH) command -> 24-bit address interleave on IO3, IO2, IO1 and IO0 -> “Continuous Read Mode” byte M[7:0] -> 4 dummy cycles -> data out until CS# goes high -> CS# goes low (reduce 4READ command) -> 24-bit random access address.

In the Continuous Read Mode, the “Continuous Read Mode” bits M[5:4] = (1,0) can make this mode continue and reduce the next 4READ command. Once M[5:4] ≠ (1,0) and after CS# is raised and then lowered, the system then will escape from the enhanced performance mode and return to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5-4) before issuing normal commands. While

Program/Erase/Write Status Register cycle is in progress, the 4READ command is rejected without any impact on the Program/Erase/Write Status Register operation.

Figure-25. Quad I/O Fast Read Sequence Diagram (M5-4 ≠ (1,0))

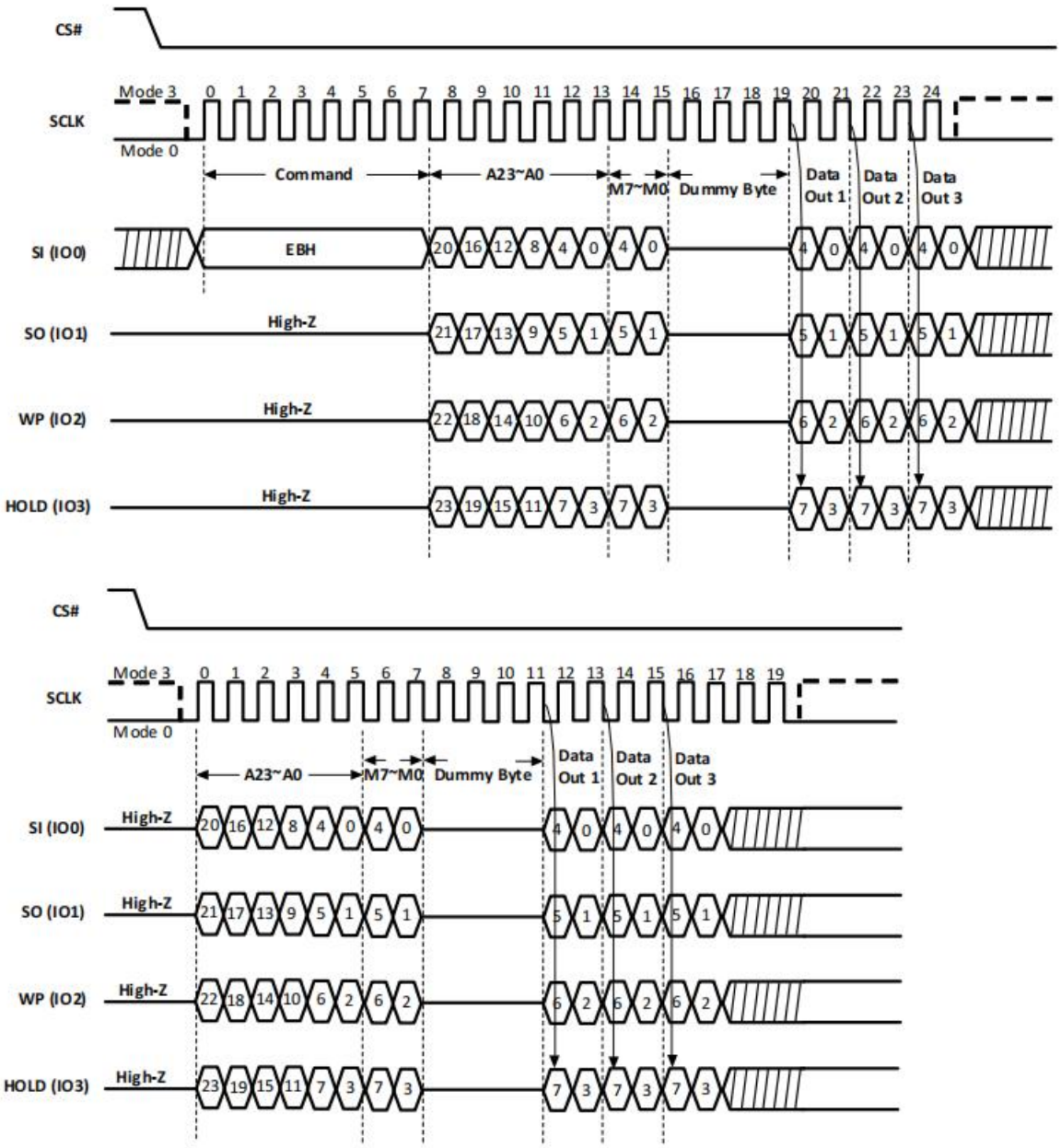


Quad I/O Fast Read with "Continuous Read Mode" (EBH)

The Quad I/O Fast Read (EBH) command supports Quad I/O Fast Read with "Continuous Read Mode" which can further reduce command overhead by setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read (EBH) command (after CS# is raised and then lowered) does not require the EBH command code.

If the "Continuous Read Mode" bits (M5-4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing a normal command.

Figure-26. Quad I/O Fast Read with "Continuous Read Mode" Sequence Diagram (M5-4 = (1,0))

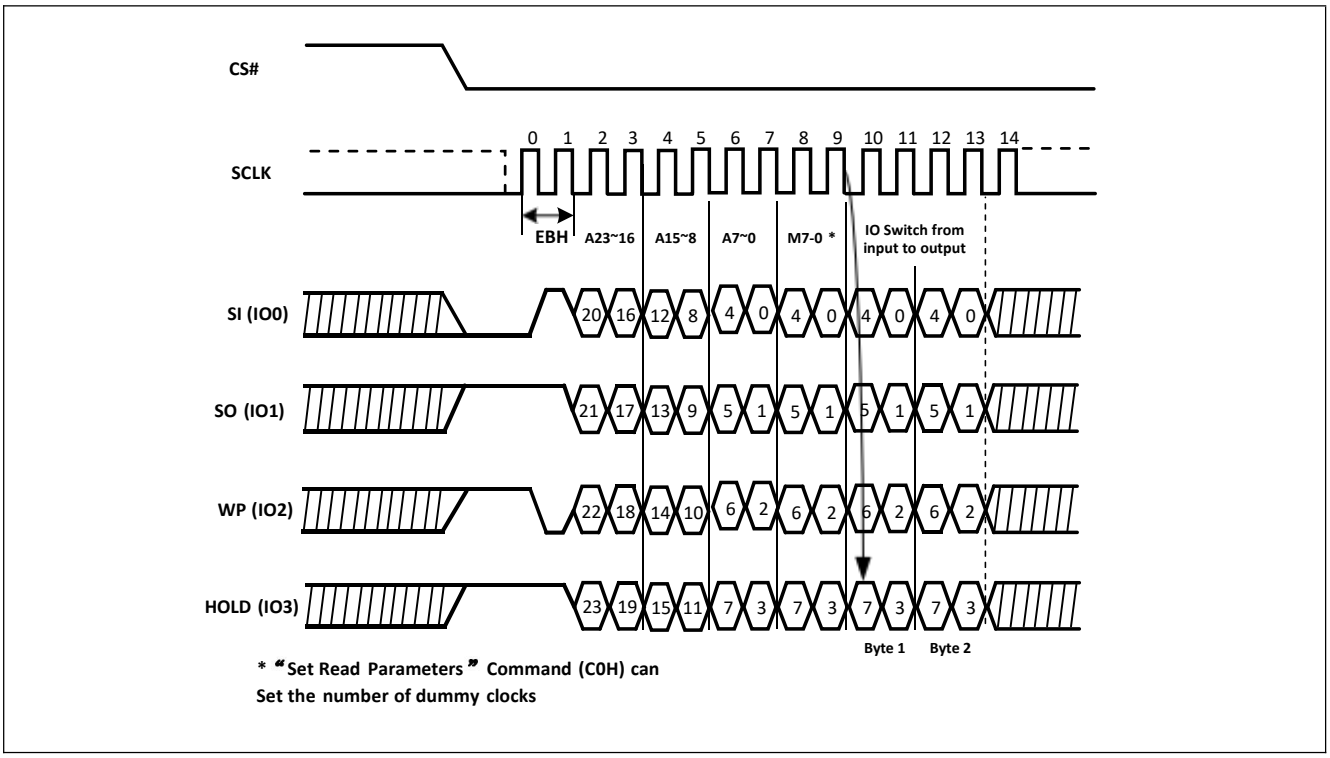


Note: Quad I/O Fast Read with "Continuous Read Mode", if (M5-4)=(1,0). If not using "Continuous Read Mode" recommend setting (M5-4)≠(1,0).

Quad I/O in QPI mode

The Quad I/O Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8. In QPI mode, the "Continuous Read Mode" bits M7-M0 are also considered as dummy clocks. "Continuous Read Mode" feature is also available in QPI mode for Quad I/O Fast Read command. "Wrap Around" feature is not available in QPI mode for Quad I/O Fast Read command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0CH) command must be used.

Figure-27. Quad I/O Read in QPI Mode Sequence (M5-4 ≠ (1,0))



Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH. The "Set Burst with Wrap" (77H) command can either enable or disable the "WrapAround" feature for the following EBH commands. When "WrapAround" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "WrapAround" operation while W6-W5 is used to specify the length of the wrap around section within a page.

4.14 DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and eight dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

DTR Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23/A31-0), as shown in Figure-28. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care

("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure-29. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh/3FFh on IO0 for the next instruction (8/10 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure-28. DTR Fast Read Quad I/O Sequence Diagram (M5-4 ≠ (1,0))

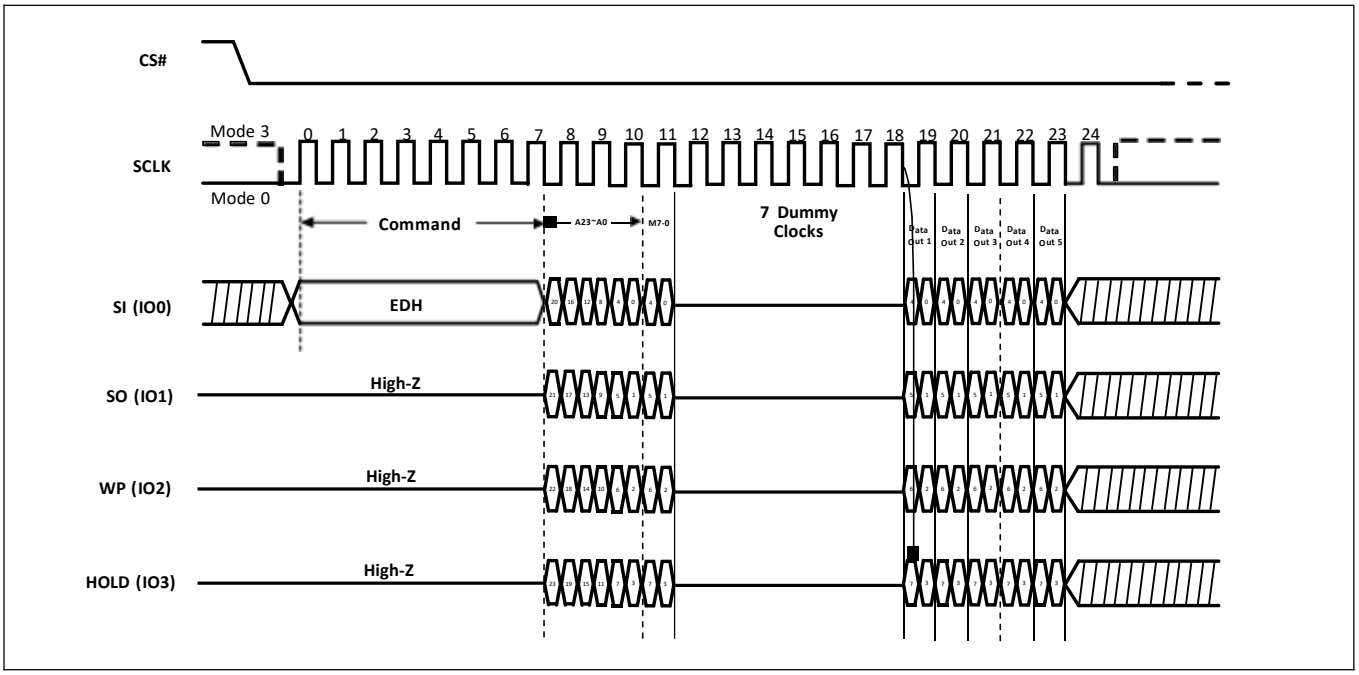
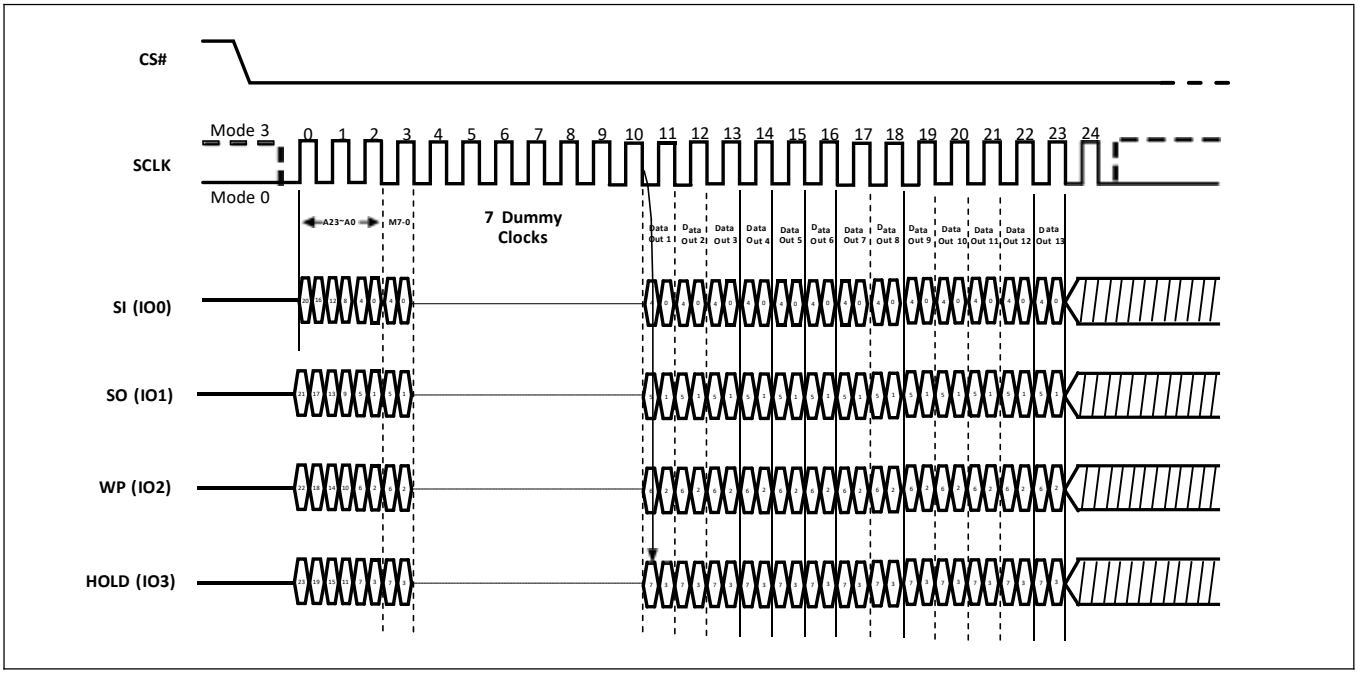


Figure-29. Quad I/O Fast Read with "Continuous Read Mode" Sequence Diagram (M5-4 = (1,0))



DTR Fast Read Quad I/O with "8/16/32/64-Byte WrapAround" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EDh. The "Set Burst with Wrap" (77h) command can either enable or disable the "WrapAround" feature for the following EDh commands. When "WrapAround" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "WrapAround" operation while W6-5 are used to specify the length of the wrap around section within a page.

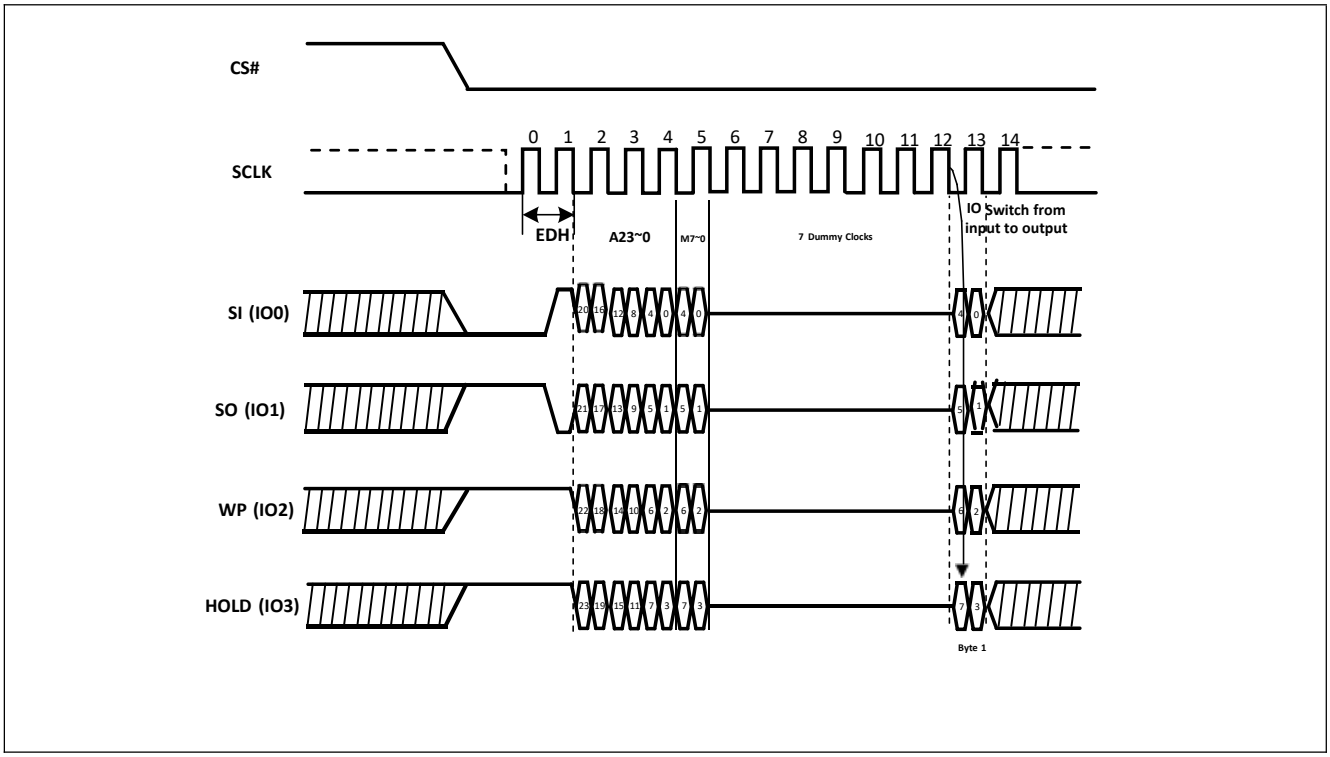
DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure-30. In QPI mode, the "Continuous Read Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

"WrapAround" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used.

Figure-30. DTR Fast Read Quad I/O in QPI Mode Sequence (M5-4 ≠ (1,0))



4.15 Set Read Parameters (C0H)

In QPI mode the “Set Read Parameters (C0H)” command can be used to configure the number of dummy clocks for “Fast Read (0BH)”, “Quad I/O Fast Read (EBH)” ,“Read SFDP Mode (5AH)”and “Burst Read with Wrap (0CH)” command, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0CH)” command.

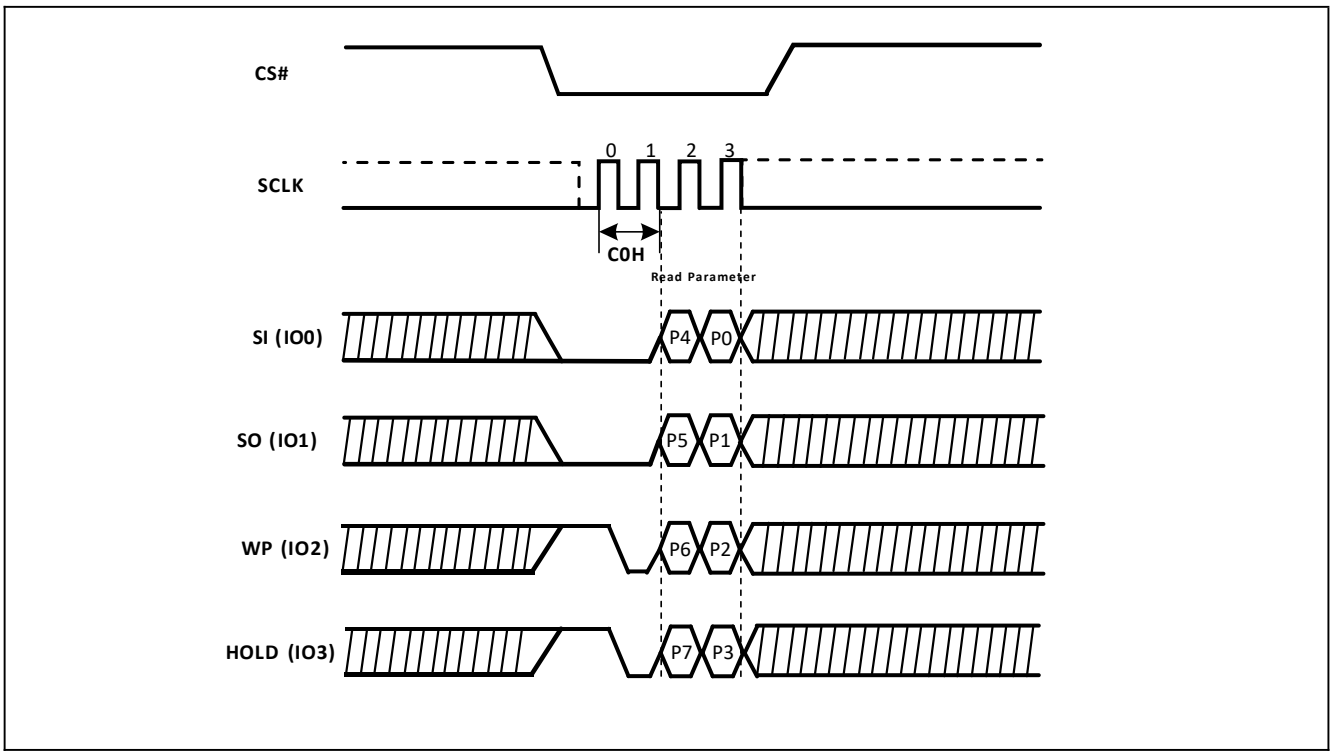
In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. The dummy clocks for various Fast Read instructions in Dual/Quad SPI mode are configured by DC bit. The “Wrap Length” is set by W5-4 bit in the “Set Burst with Wrap (77h)” instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 2. The number of dummy clocks is only programmable for “Fast Read (0Bh)”, “4IO Read (EBh)” & “Burst Read with Wrap (0Ch)” instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again, prior to any 0Bh, EBh or 0Ch instructions.

P5-P4	Dummy Clocks	Maximum Read Freq.(2.7~3.0V)	Maximum Read Freq.(3.0~3.6V)	P1-P0	Wrap Length
0,0	2	33MHz	50MHz	0,0	8-byte
0,1	4	50MHz	80MHz	0,1	16-byte
1,0	6	80MHz	104MHz	1,0	32-byte
1,1	8	104MHz	133MHz	1,1	64-byte

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Email:sales@manduic.com

Figure-31. Set Read Parameters (QPI)

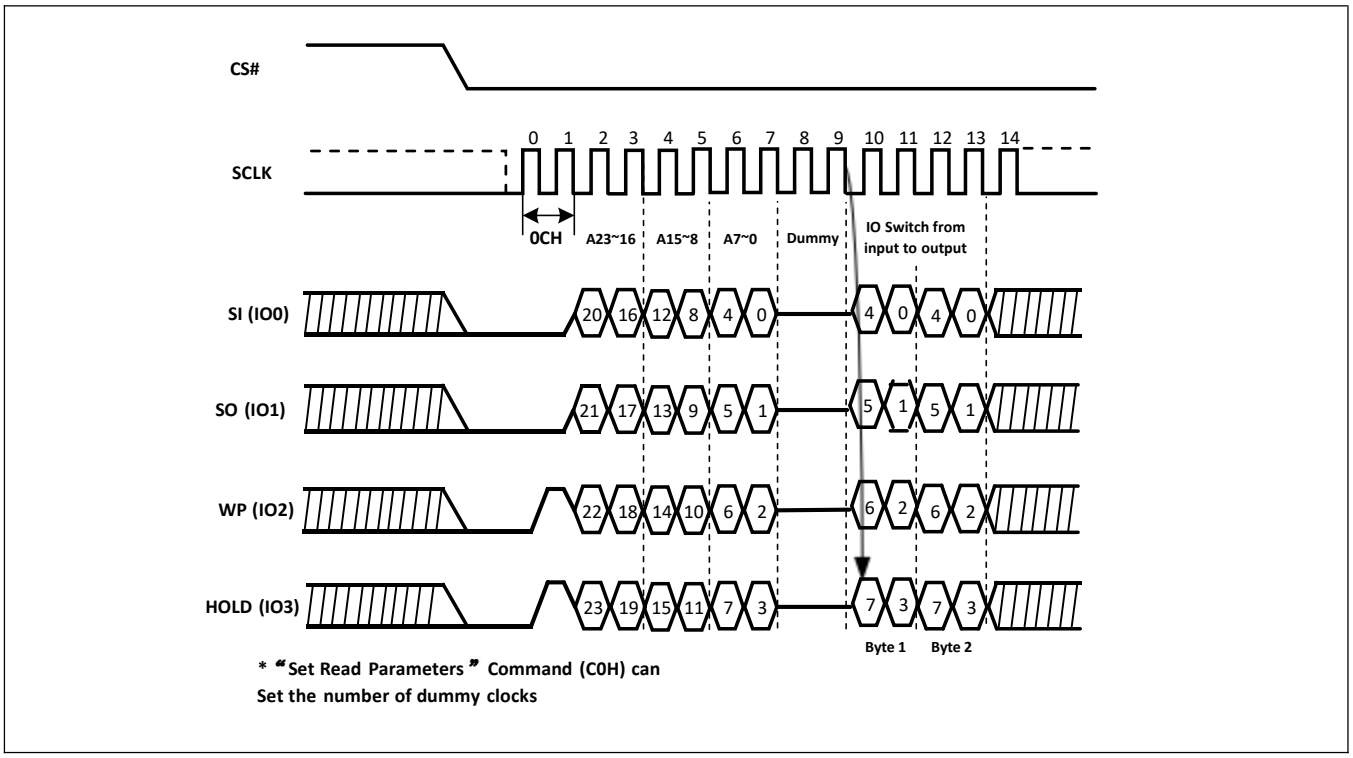


4.16 Burst Read with Wrap (0CH)

The “Burst Read with Wrap (0CH)” command provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. This command is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “WrapAround” to the beginning boundary of the “WrapAround” once the ending boundary is reached. The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0H)” command.

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Figure-32. Burst Read with Wrap Sequence (QPI)

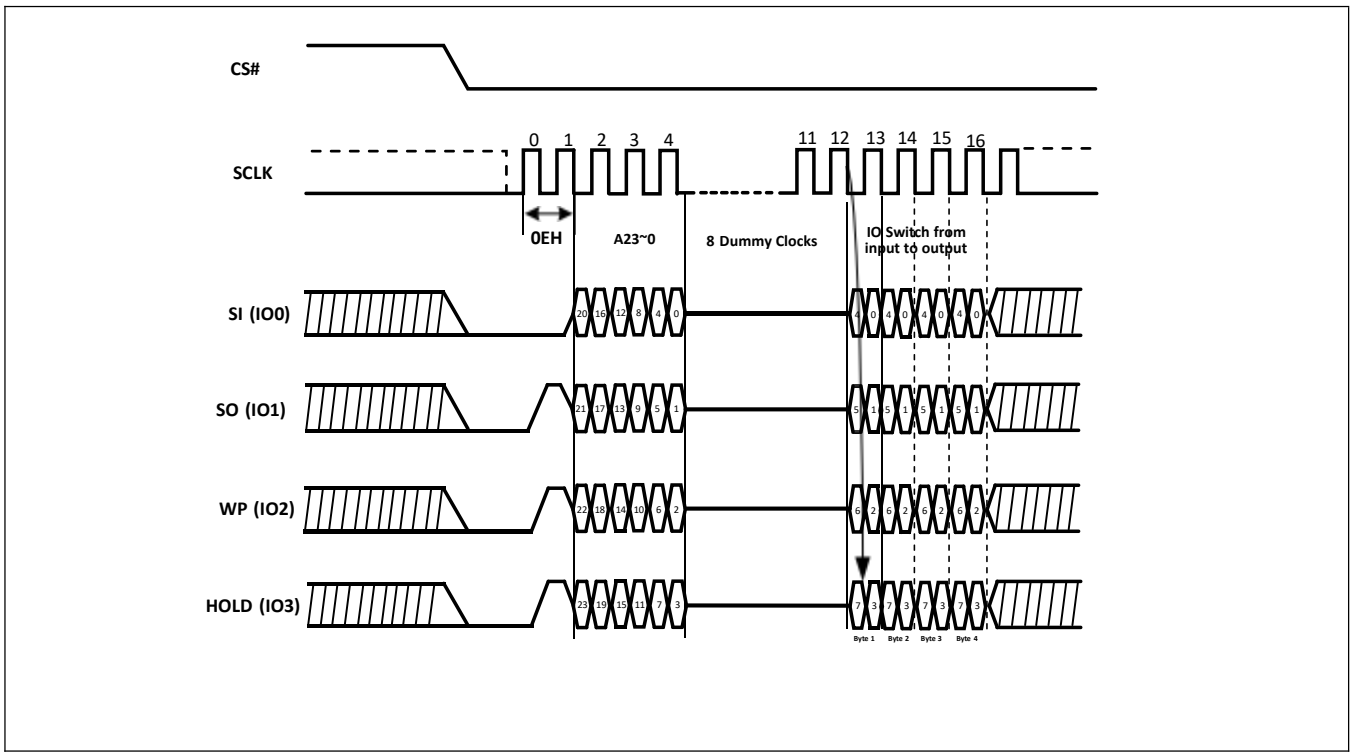


4.17 DTR Burst Read with Wrap (0Eh)

The "DTR Burst Read with Wrap (0Eh)" instruction provides an alternative way to perform the read operation with "WrapAround" in QPI mode. The instruction is similar to the "Fast Read (0Bh)" instruction in QPI mode, except the addressing of the read operation will "WrapAround" to the beginning boundary of the "Wrap Length" once the ending boundary is reached. The "Wrap Length" can be configured by the "Set Read Parameters (C0h)" instruction.

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Figure-33. DTR Burst Read with Wrap Sequence (QPI)



4.18 Set Burst with Wrap (77H)

The Set Burst with Wrap (77h) command is used in conjunction with Quad I/O Fast Read (EBH) command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: CS# goes low -> Send Set Burst with Wrap (77h) command -> Send 24 dummy bits-> Send 8 bits “Wrap bits” -> CS# goes high.

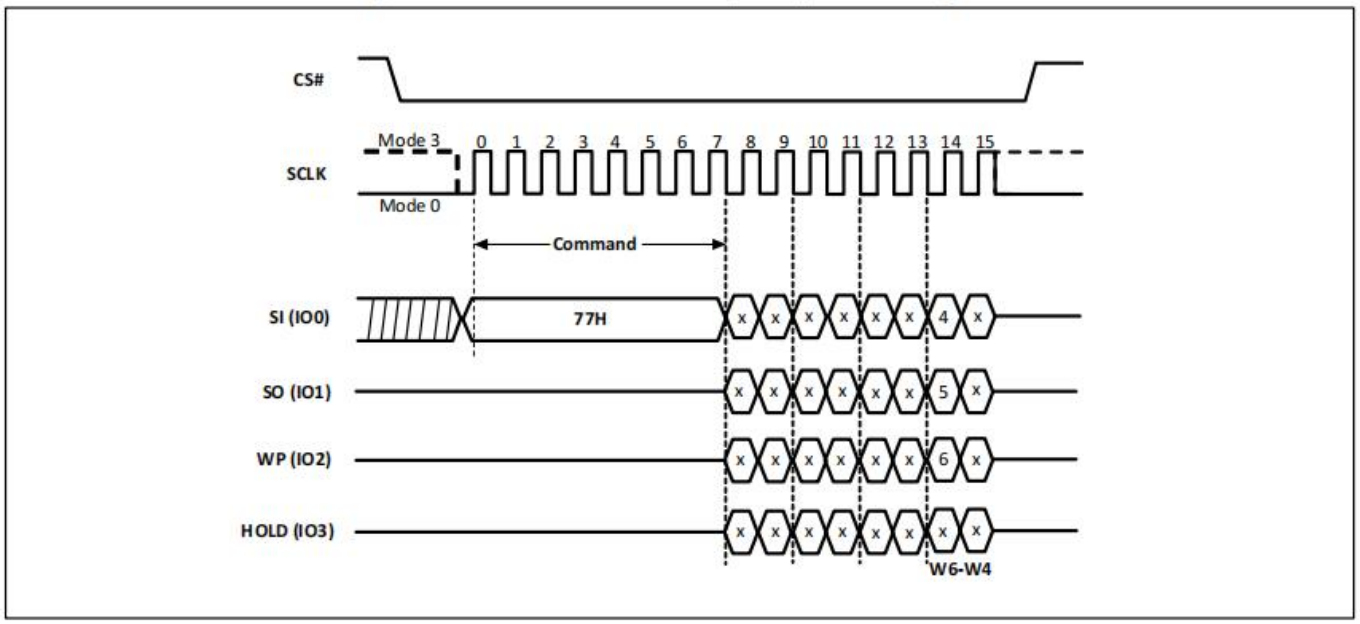
If the W6-W4 bits are set by the Set Burst with Wrap command, all the following Quad I/O Fast Read commands will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

Table-12. Burst Length and Wrap

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0,0	Yes	8-byte	No	N/A
0,1	Yes	16-byte	No	N/A
1,0	Yes	32-byte	No	N/A
1,1	Yes	64-byte	No	N/A

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Figure-34. Set Burst with Wrap Sequence Diagram



4.19 Sector Erase (SE) (20H)

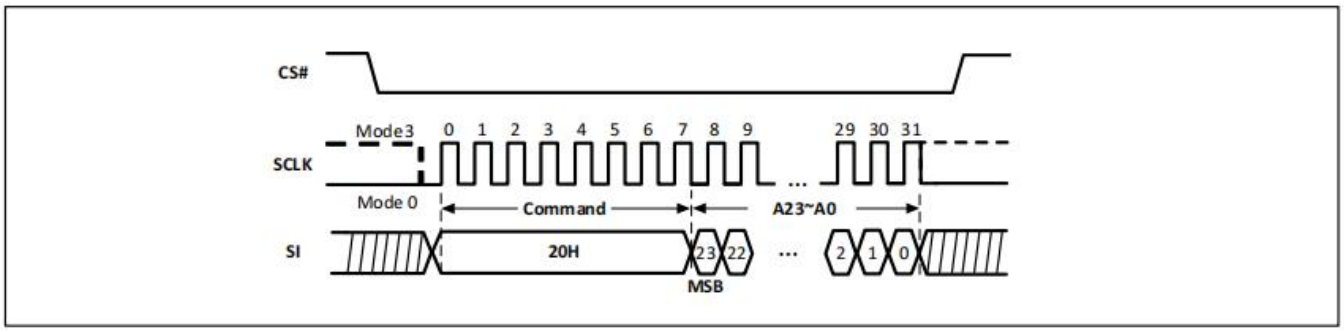
The Sector Erase (20H) command sets all bits to 1 (FFH) inside the chosen sector. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The SE command is entered by driving Chip Select (CS#) Low, followed by the command code, and three address bytes on Data Input (SI). Any address inside the sector is a valid address for the SE command. CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-35. The CS# must go high exactly at the byte boundary (after the least significant bit of the third address byte is latched-in); otherwise, the command will be rejected and not executed. As soon as CS# is driven High, the self-timed Sector Erase cycle (with duration tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Sector Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

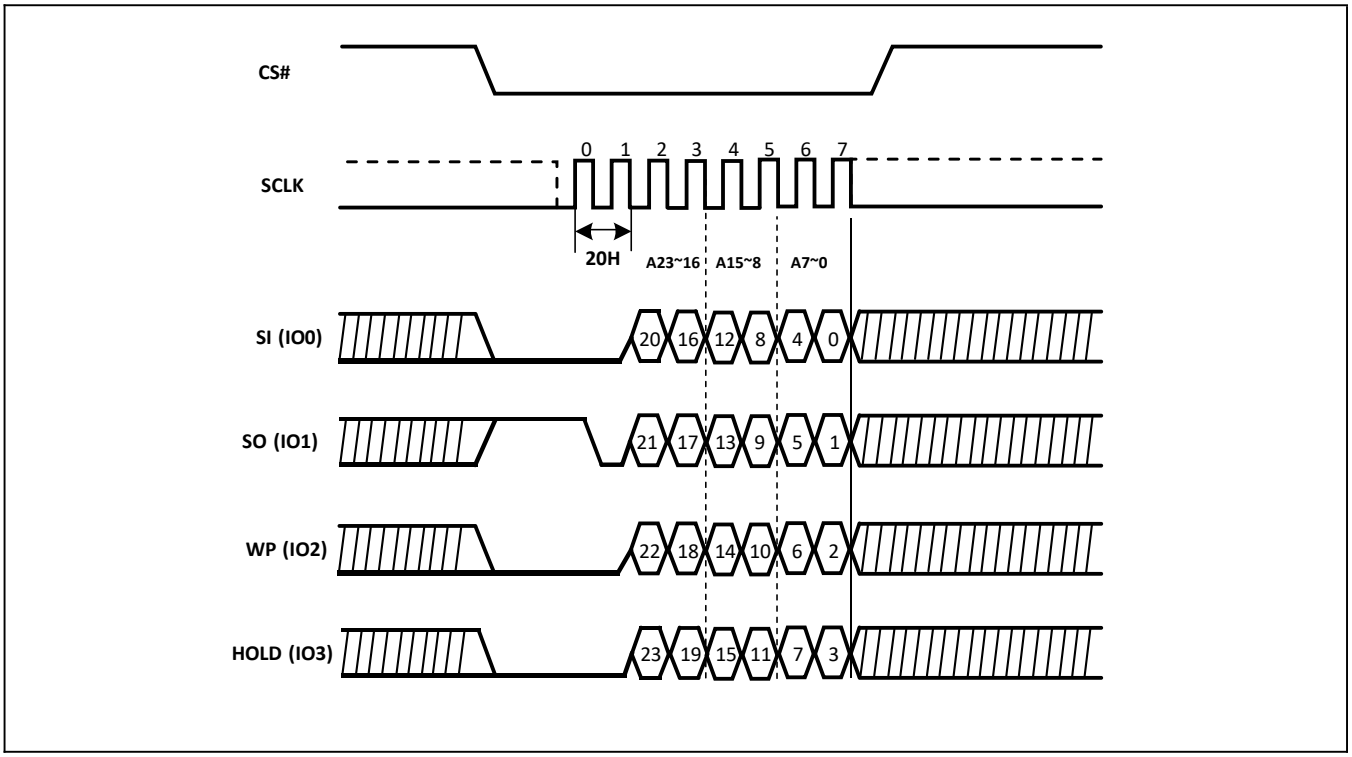
A SE command may be applied only to a sector which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

Figure-35. Sector Erase Sequence Diagram



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Figure-36. Sector Erase Sequence Diagram (QPI)



The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP4, BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector

4.20 Block Erase (BE) (D8H)

The Block Erase (D8H) command sets all bits to 1 (FFH) inside the chosen block. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable 06H command has been decoded, the device sets the Write Enable Latch (WEL).

The BE command is entered by driving Chip Select (CS#) Low, followed by the command code, and three address bytes on Data Input (SI). Any address inside the block is a valid address for the BE command. CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-37. CS# must be driven High after the least significant bit of the third address byte is latched in, otherwise the BE command is not executed. As soon as CS# is driven High, the self-timed Block Erase cycle (whose duration is tBE2) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Block Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A BE command may be applied only to a block which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

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Figure-37. Block Erase Sequence Diagram

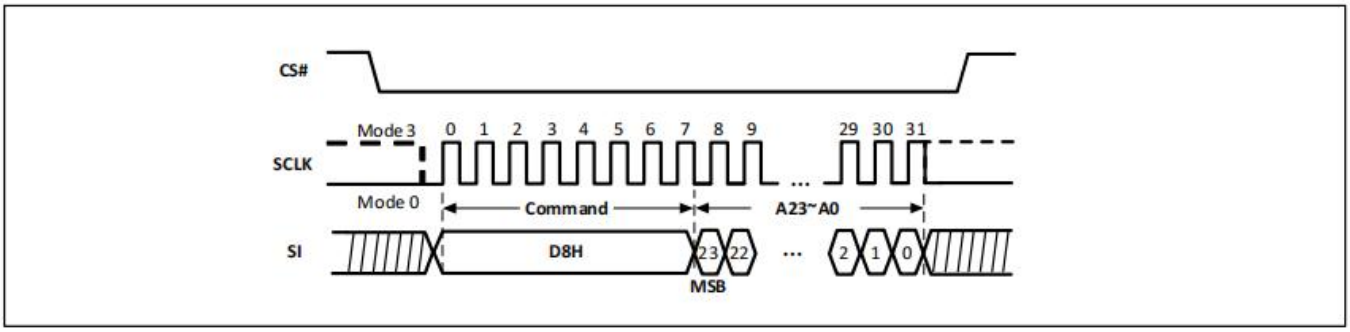
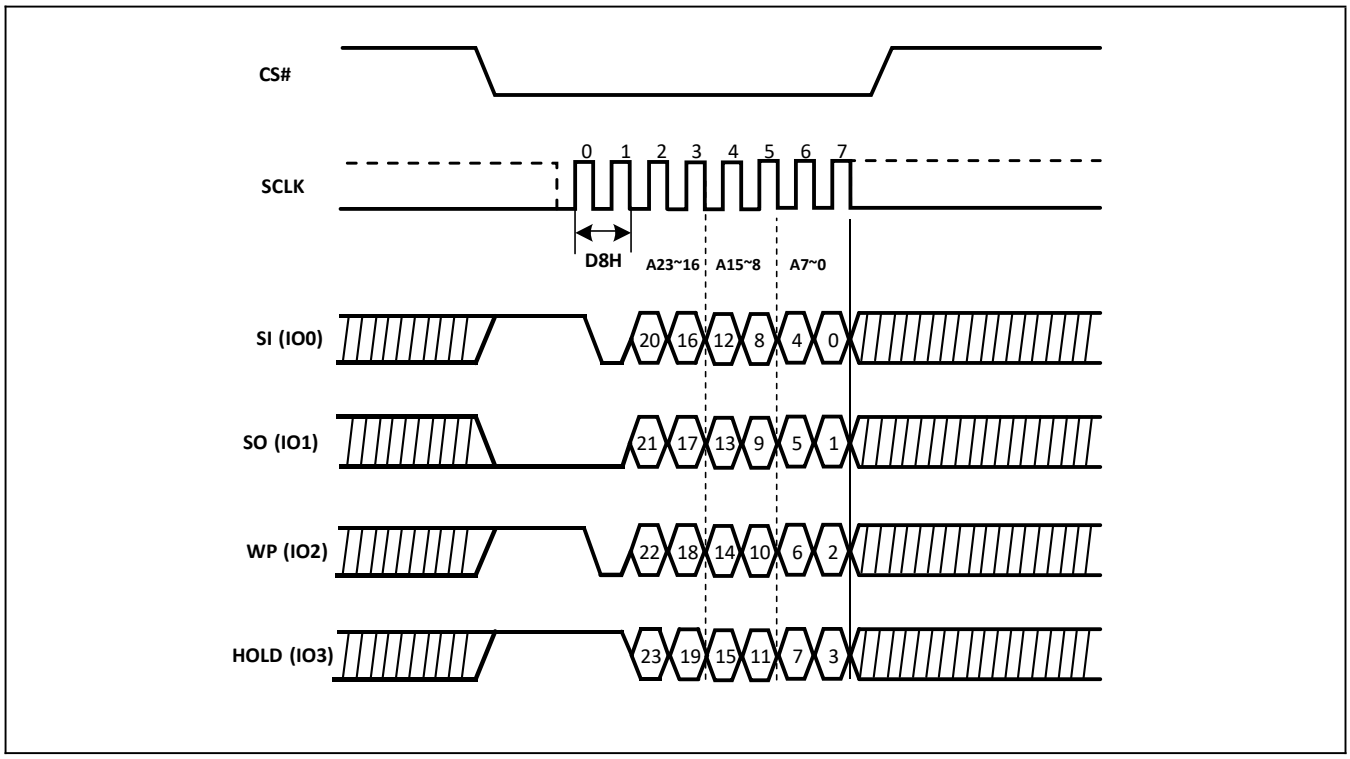


Figure-38. Block Erase Sequence Diagram (QPI)



4.21 Chip Erase (CE) (60H or C7H)

The Chip Erase (60H or C7H) command sets all bits to 1 (FFH). Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The CE command is entered by driving Chip Select (CS#) Low, followed by the command code on Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-39. CS# must be driven High after the eighth bit of the command code is latched in, otherwise the CE command is not executed. As soon as CS# is driven High, the self-timed Chip Erase cycle (with duration tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The WIP bit is 1 during the self-timed Chip Erase cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

The CE command is executed only if all Block Protect (BP4, BP3, BP2, BP1, BP0) bits are 0. The CE command is ignored if one, or more blocks are protected.

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Figure-39. Chip Erase Sequence Diagram

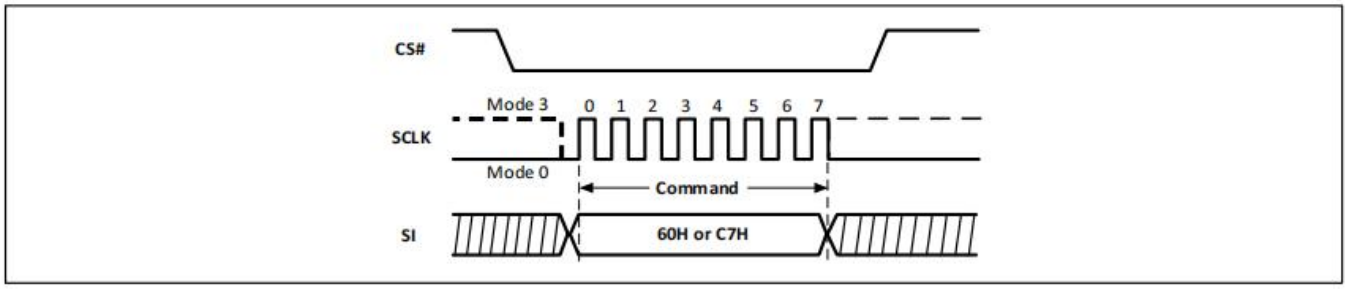
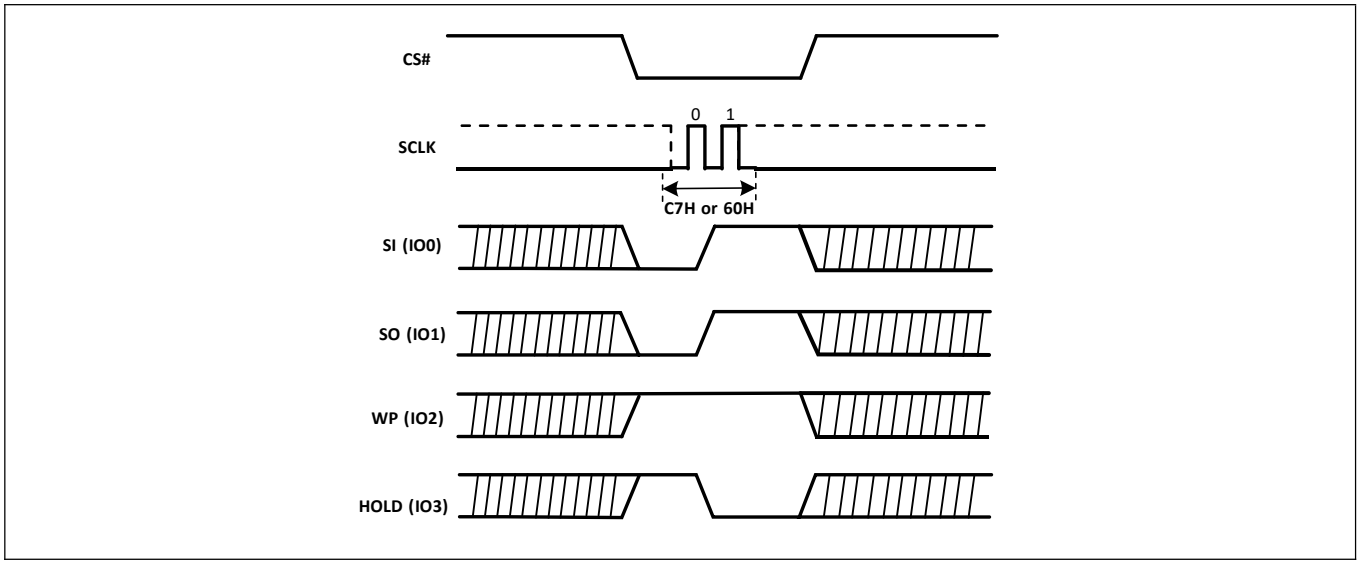


Figure-40. Chip Erase Sequence Diagram (QPI)



4.22 Page Program (PP) (02H)

The Page Program (02H) command allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (06H) command must have previously been executed. After the Write Enable command has been decoded, the device sets the Write Enable Latch (WEL).

The PP command is entered by driving Chip Select (CS#) Low, followed by the command code, three address bytes and at least one data byte on Data Input (SI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the starting address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-41. If more than 256 bytes are sent to the device, previously latched data are discarded, and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

CS# must be driven High after the eighth bit of the last data byte has been latched in, otherwise the PP command is not executed.

As soon as CS# is driven High, the self-timed Page Program cycle (with duration tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the WIP bit. The WIP bit is 1 during the self-timed Page Program cycle and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

APP command may be applied only to a page which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

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Figure-41. Page Program Sequence Diagram

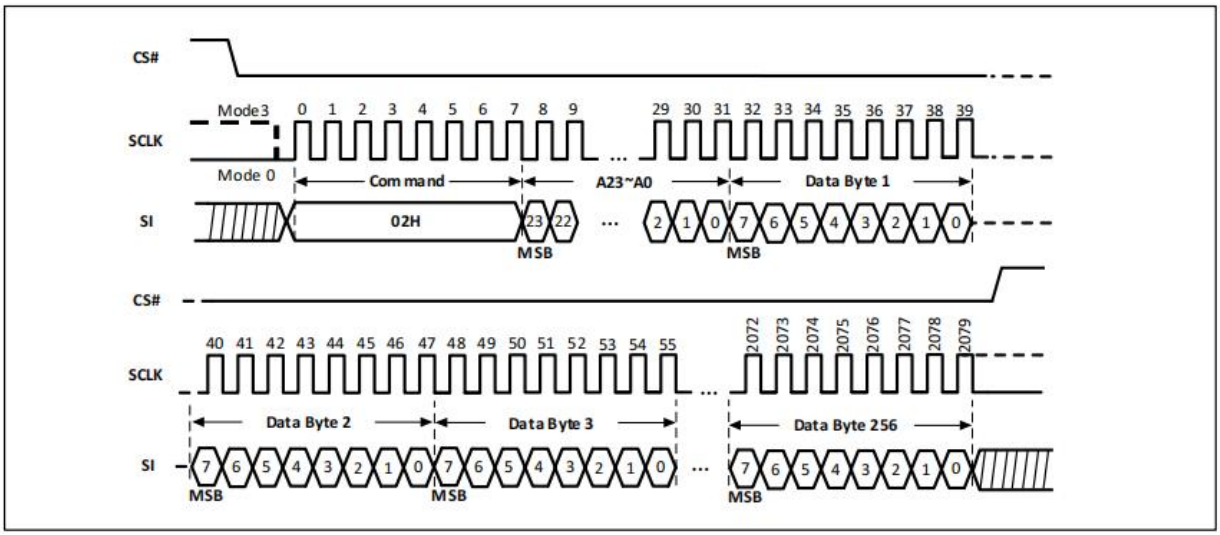
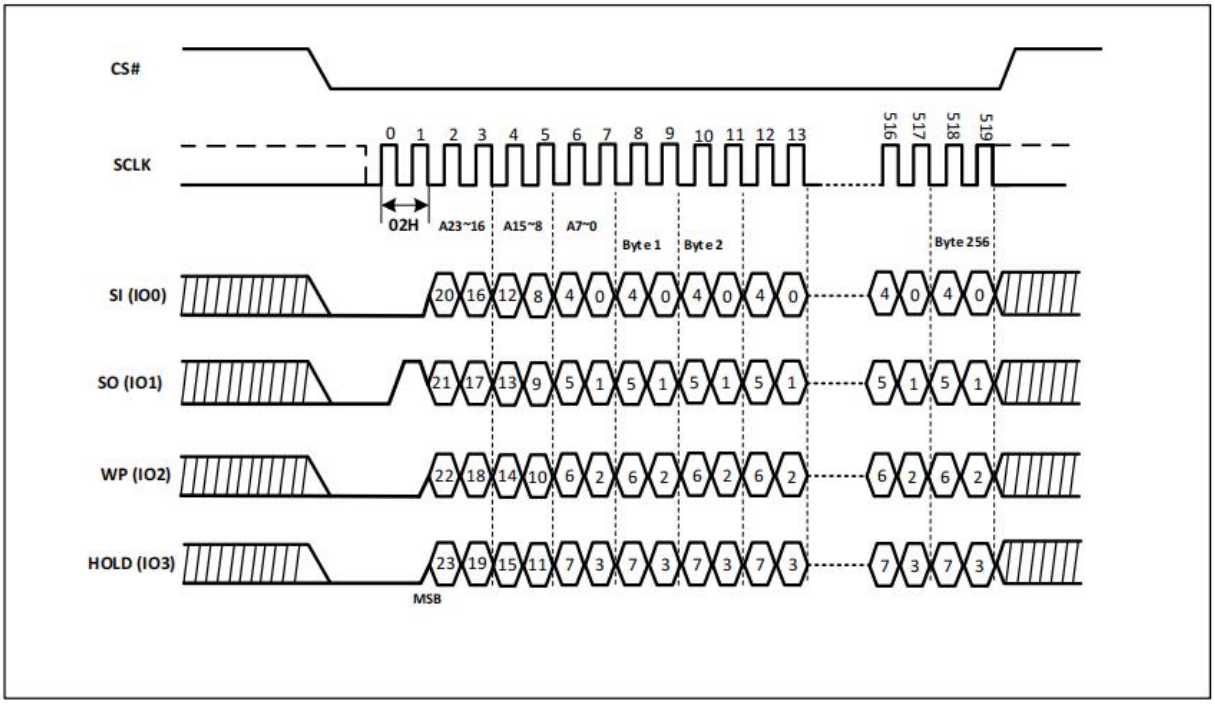


Figure-42. Page Program Sequence Diagram (QPI)



4.23 Quad Input Page Program (QPP) (32H)

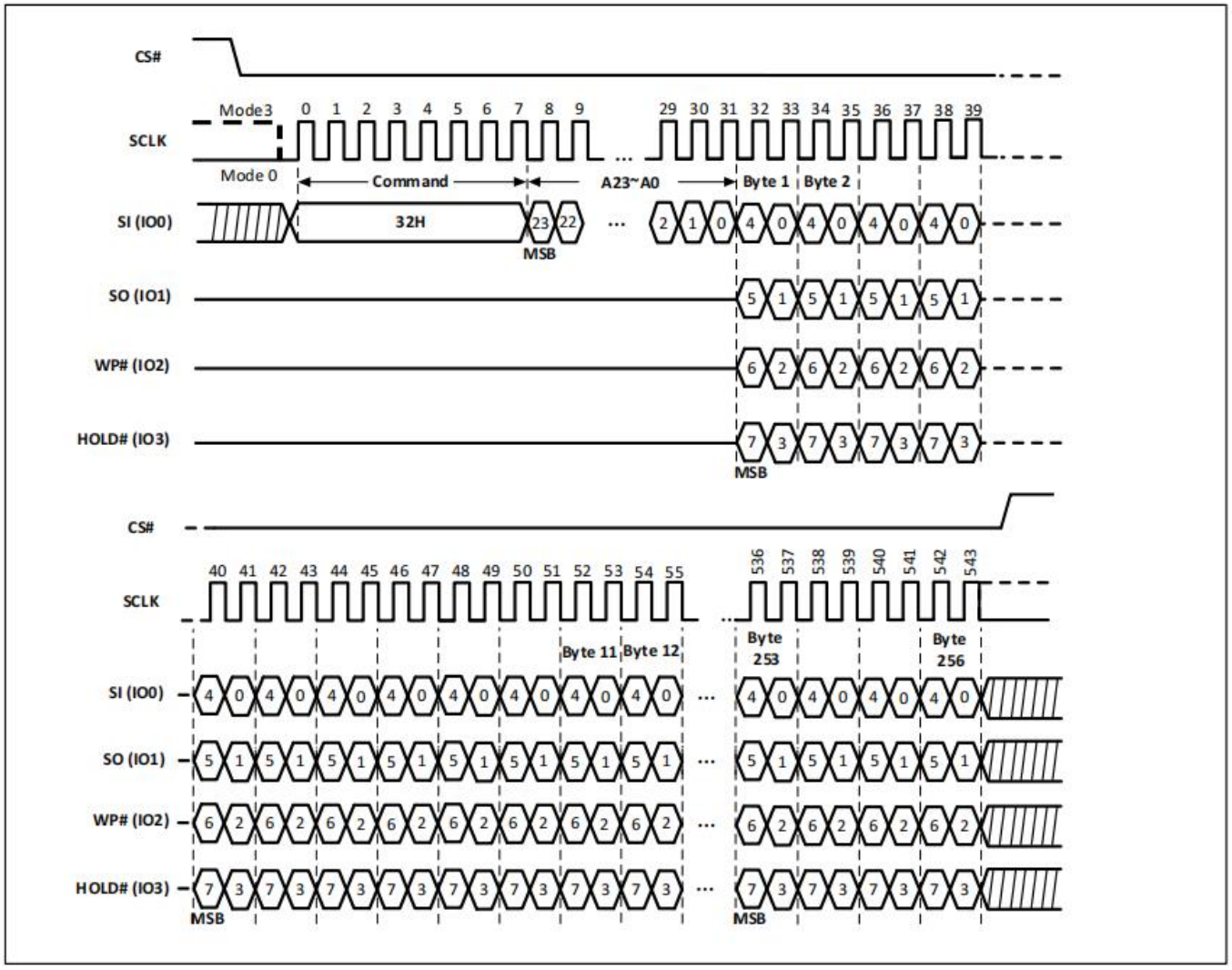
The Quad Input Page Program (32H) command is for programming the memory to be "0". AWrite Enable command must be executed to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit to "1" before sending the QPP command. The Quad Input Page Programming uses four pins: IO0, IO1, IO2, and IO3 as data input, which can improve programmer as well as in-system application performance. The QPP operation supports frequencies as fast as fQPP. The other function descriptions are as same as standard page program.

The sequence of issuing QPP command is: CS# goes low -> send Quad Input Page Program (32H) command code -> 3-byte address on IO0 -> at least 1-byte on data on IO[3:0] -> CS# goes high.

A QPP command may be applied only to a page which is not protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits.

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Figure-43. Quad Input Page Program Sequence Diagram



4.24 Erase Security Register (ERSCUR) (44H)

There are three 1024-byte Security Registers which can be erased and programmed individually. These registers may be used by system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register (44H) command is like the Sector Erase (20H) command. A Write Enable command must be executed before the device will accept the ERSCUR Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the command code “44H” followed by a 24-bit address (A23-A0) to erase one of the security registers.

The ERSCUR command sequence is shown in Figure-44. The CS# pin must be driven high after the eighth bit of the last address byte is latched. If this is not done, the command will not be executed. After CS# is driven high, the self-timed ERSCUR operation will commence for a time duration of tSE.

While the Erase Security Register cycle is in progress, the Read Status Register command (05H) may still be accessed for checking the value of the Write in Progress (WIP) bit. The WIP bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Erase Security Register cycle has finished, the WEL bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register are OTP and can be used to protect the security registers. Once the LB bit is set to 1, the corresponding security register will be permanently locked, and an ERSCUR

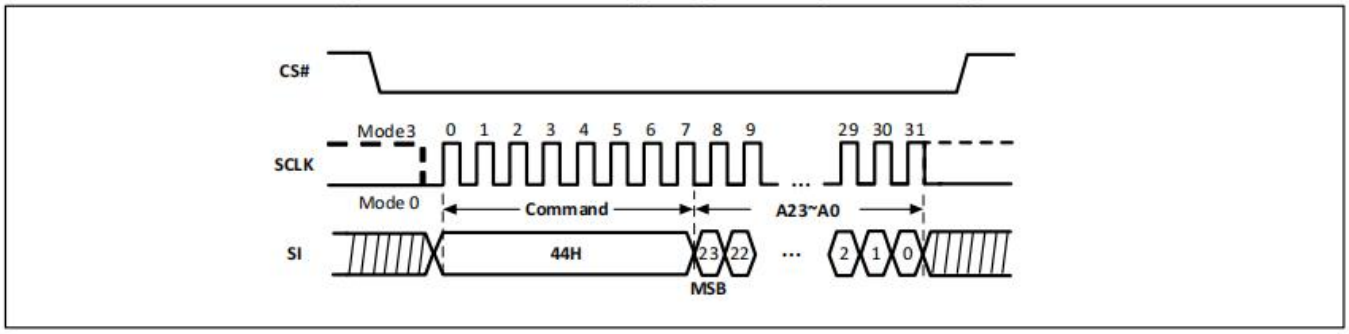
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command to that register will be ignored.

Table-13.1 Erase Security Register Address

ADDRESS	A23-16	A15-12	A11-10	A9-0
Security Register #1	00h	0001	00	Don't care
Security Register #2	00h	0010	00	Don't care
Security Register #3	00h	0011	00	Don't care

Figure-44. Erase Security Register Sequence Diagram



4.25 Program Security Register (PRSCUR) (42H)

The Program Security Register (42H) command is similar to the Page Program (02H) command. It allows from one byte to 1024 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable (06H) command must be executed before the device will accept the PRSCUR Command (Status Register bit WEL= 1). The command is initiated by driving the CS# pin low then shifting the command code "42H" followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device.

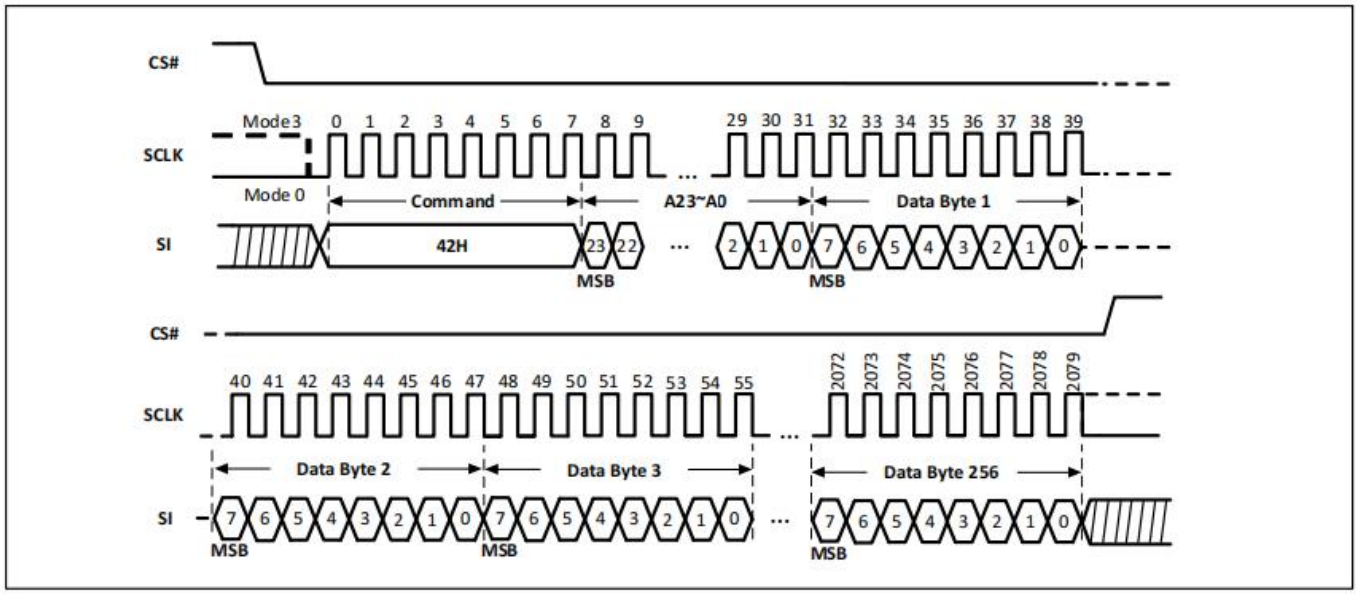
The PRSCUR command sequence is shown in Figure-45. The Security Register Lock Bits (LB3-1) in the Status Register are OTP can be used to protect the security registers. Once Security Register Lock Bit (LB3-1) is set to 1, the corresponding security register will be permanently locked, and a PRSCUR command to that register will be ignored.

Table-13.2 Program Security Register Address

ADDRESS	A23-16	A15-12	A11-10	A9-0
Security Register #1	00h	0001	00	Byte Address
Security Register #2	00h	0010	00	Byte Address
Security Register #3	00h	0011	00	Byte Address

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Figure-45. Program Security Register Sequence Diagram



4.26 Read Security Register (RDSCUR) (48H)

The Read Security Register (48H) command is similar to the Fast Read (0BH) command and allows one or more data bytes to be sequentially read from one of the three security registers. The command is initiated by driving the CS# pin low and then shifting the command code “48H” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the SI pin. The code and address bits are latched on the rising edge of the SCLK pin. After the address is received, and following the eight dummy cycles, the data byte of the addressed memory location will be shifted out on the SO pin on the falling edge of SCLK with the most significant bit (MSB) first. The first byte addressed can be at any location. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will reset to 00h, the first byte of the register, and continue to increment. The command is completed by driving CS# high.

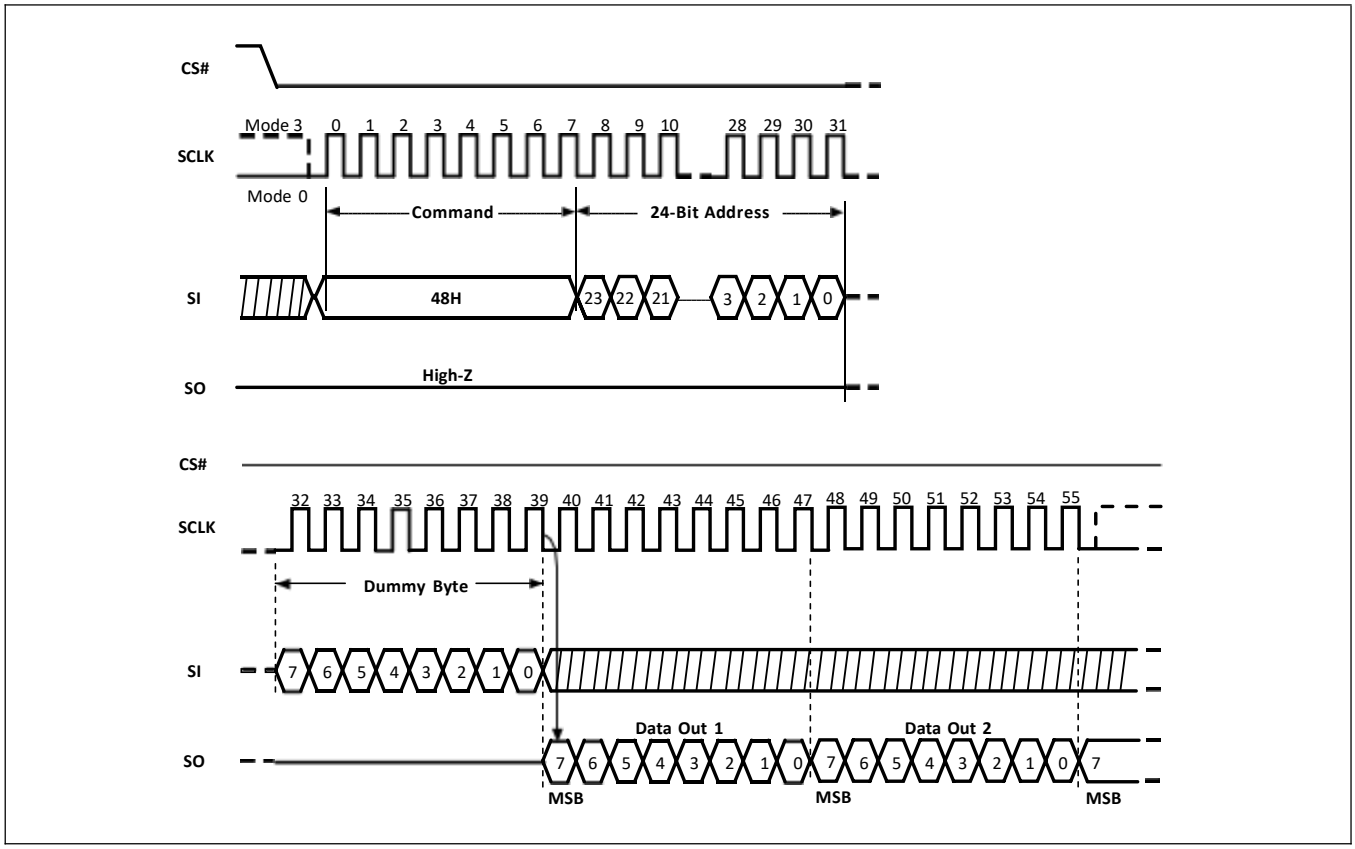
The RDSCUR command sequence is shown in Figure-46. If a RDSCUR command is issued while an Erase, Program, or Write cycle is in process (Write in Progress (WIP)=1), the command is ignored and will not have any effect on the current cycle. The RDSCUR command allows each bit being shifted out on SO pin at a Max frequency fC, on the falling edge of SCLK.

Table-13.3 Read Security Register Address

ADDRESS	A23-16	A15-12	A11-10	A9-0
Security Register #1	00h	0001	00	Byte Address
Security Register #2	00h	0010	00	Byte Address
Security Register #3	00h	0011	00	Byte Address

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Figure-46. Read Security Register Sequence Diagram



4.27 Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (B9H) command is the only way to place the device in the lowest power consumption mode (the Deep Power-Down mode). It can also be used as an extra software protection mechanisms the device is not in active use, all Write, Program and Erase commands are ignored.

Driving Chip Select (CS#) High deselects the device and puts the device in the Standby mode (if there is no internal cycle currently in progress). However, Standby mode is not the Deep Power-Down mode. The Deep Power-Down mode can only be entered by executing the DP command, to reduce the standby current (from ISB1 to ISB2).

Once the device has entered the Deep Power-Down mode, all commands are ignored except the Release from Deep Power-Down, Read Electronic Signature (ABH) command. This command releases the device from this mode and also outputs the Device ID on Data Output (SO).

The Deep Power-Down mode automatically stops at Power-Down, and the device always Powers-up in the Standby mode. The DP command is entered by driving CS# Low, followed by the command code on Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The command sequence is shown in Figure-47. CS# must be driven High after the eighth bit of the command code has been latched in, otherwise the Deep Power-Down (B9H) command is not executed. As soon as CS# is driven High, a delay of tDP occurs before the supply current is reduced to ISB2 and the Deep Power-Down mode is entered.

Any DP command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

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Figure-47. Deep Power-Down Sequence Diagram

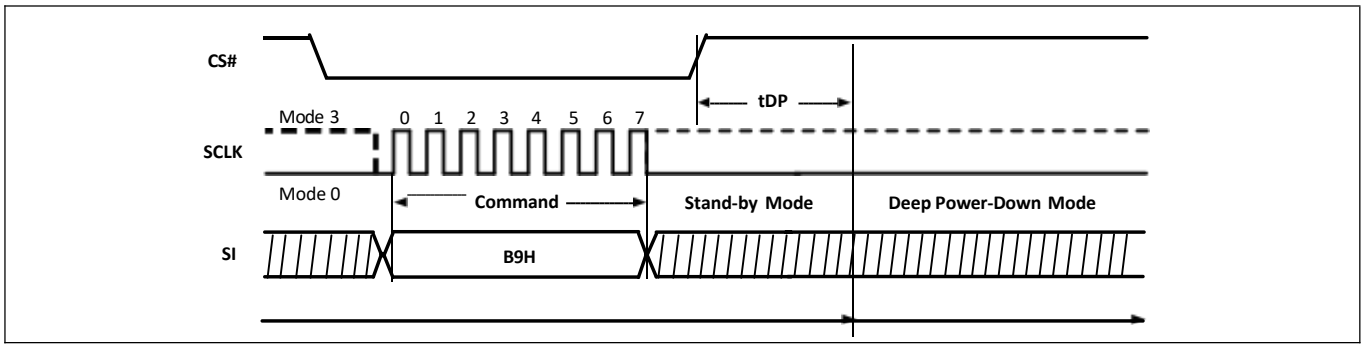
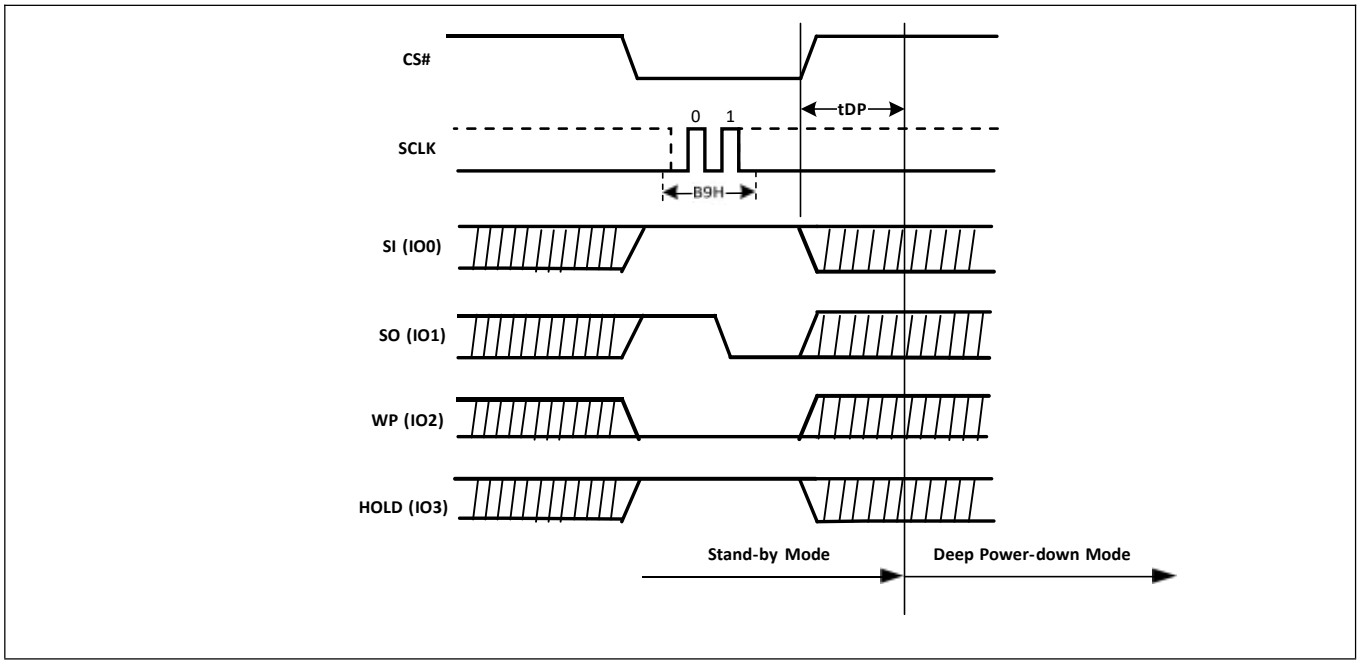


Figure-48. Deep Power-Down Sequence Diagram (QPI)



4.28 Release form Deep Power-Down (RDP), Read Electronic Signature (RES) (ABH)

Once the device has entered the Deep Power-Down mode, all commands are ignored except the Release from Deep Power-Down, Read Electronic Signature (ABH) command. Executing this command takes the device out of the Deep Power-Down mode.

Please note that this is not the same as or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identification (9FH) command. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identification command.

When used only to release the device from the power-down state, the command is issued by driving the Chip Select (CS#) pin low, shifting the command code “ABH” and driving CS# high as shown in Figure-49. After the time duration of tRES1 the device will resume normal operation and other commands will be accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the command is initiated by driving the CS# pin low and shifting the command code “ABH” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of SCLK with the most significant bit (MSB) first as shown in Figure-51. The Device ID values are listed in "Tables of ID Definition" (Table-11). The Device ID can be read continuously. The command is completed by driving CS# high.

When CS# is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-Down mode, the transition to the Stand-by Power mode is immediate. If the device was

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previously in the Deep Power-Down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and CS# must remain High for at least tRES2 (max). Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute commands.

Except while an Erase, Program or Write Status Register cycle is in progress, the RDP, RES command always provides access to the 8-bit Device ID of the device and can be applied even if the Deep Power-Down mode has not been entered.

Any RDP, RES command issued to the device while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

Figure-49. Release from Deep Power-Down (RDP) Sequence Diagram

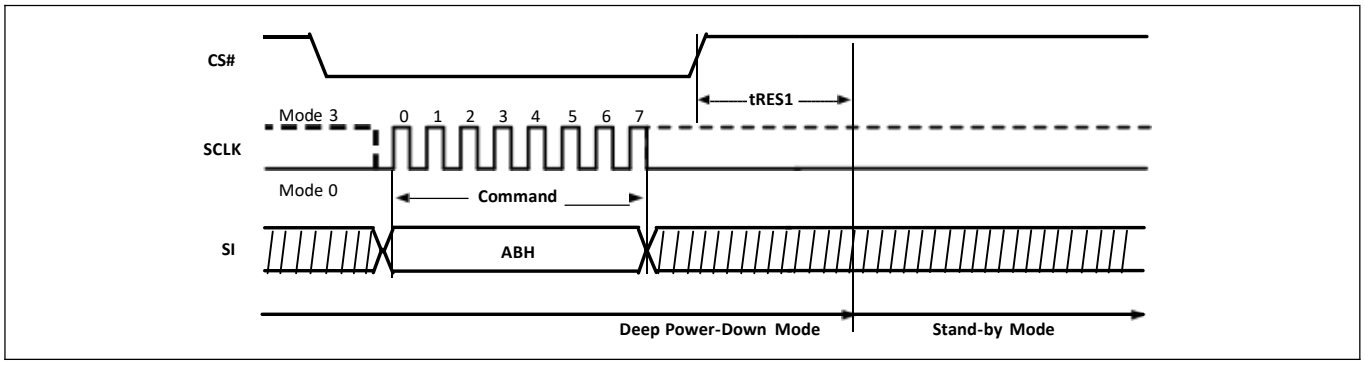
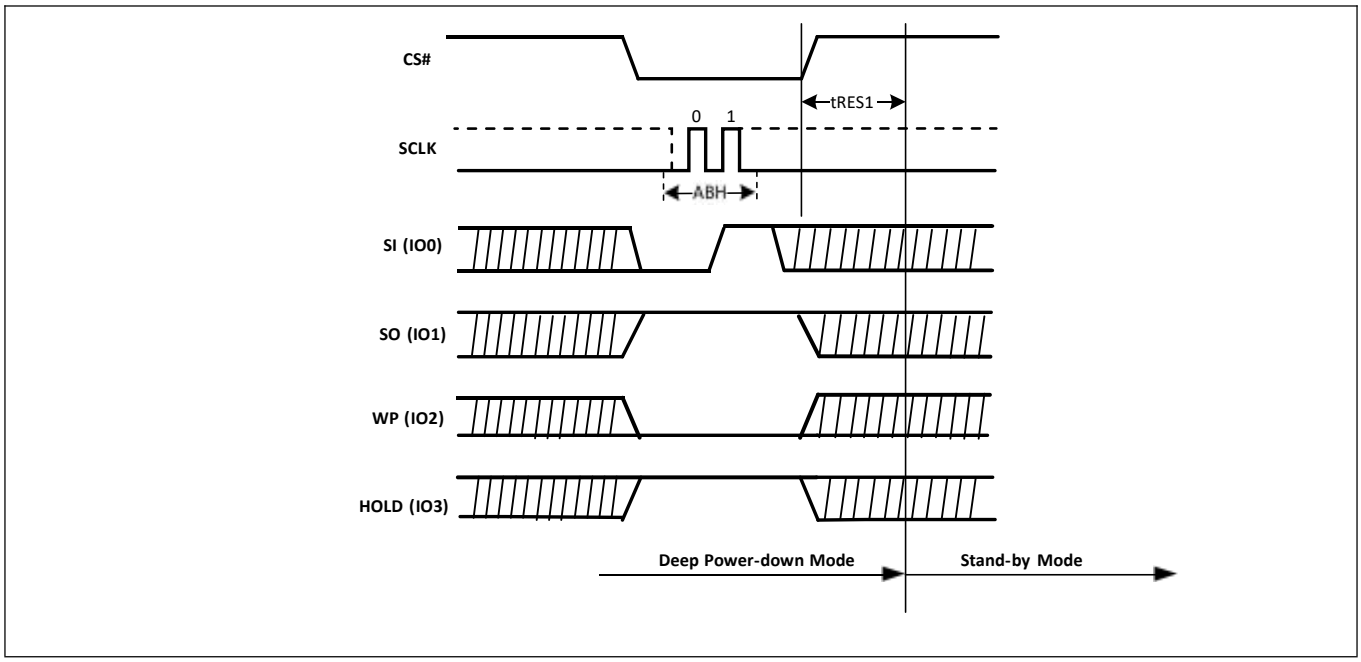


Figure-50. Release from Deep Power-Down (RDP) Sequence Diagram (QPI)



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Figure-51. Read Electronic Signature (RES) Sequence Diagram

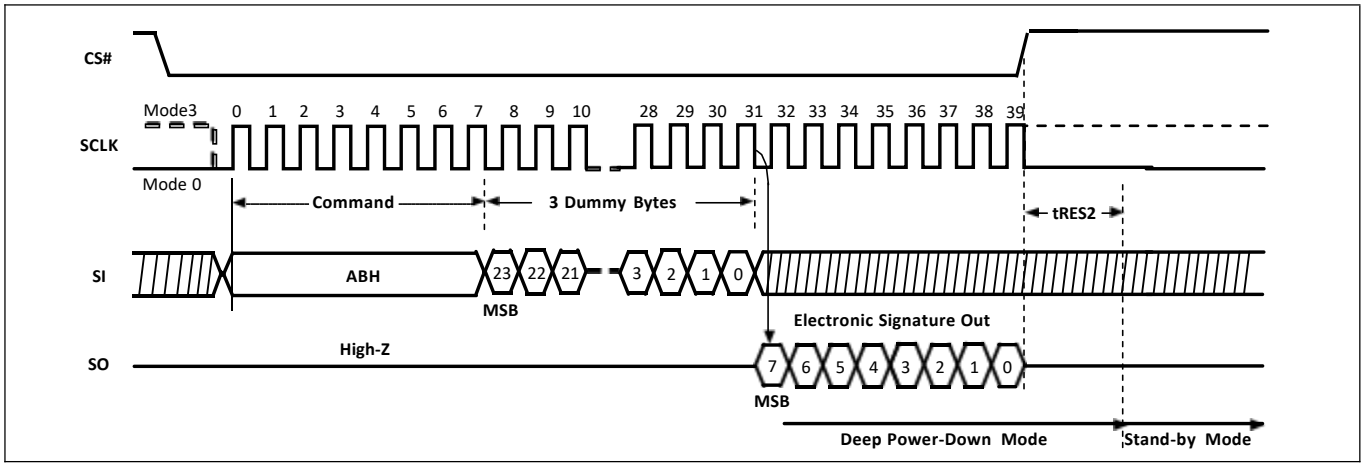
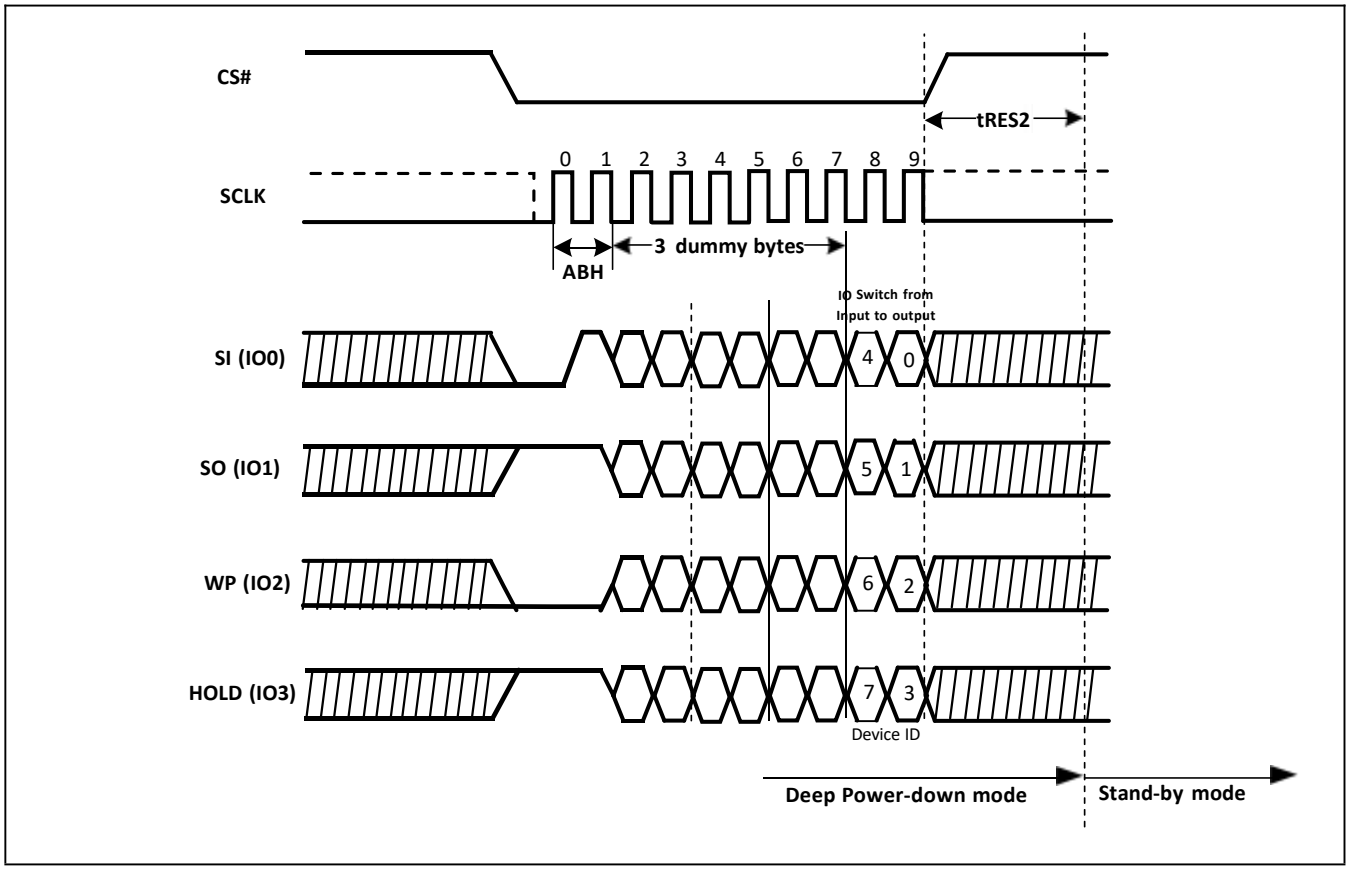


Figure-52. Read Electronic Signature (RES) Sequence Diagram (QPI)



4.29 Read Electronic Manufacturer ID & Device ID (REMS) (90H)

The Read Electronic Manufacturer & Device ID (90H) command provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The REMS command is initiated by driving the CS# pin low and shifting the command code “90H” followed by two dummy bytes and one address byte (A7~A0). After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first as shown in Figure-53. The Device ID values are listed in "Tables of ID Definition" (Table-11). If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high.

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Figure-53. Read Electronic Manufacturer ID & Device ID Sequence Diagram

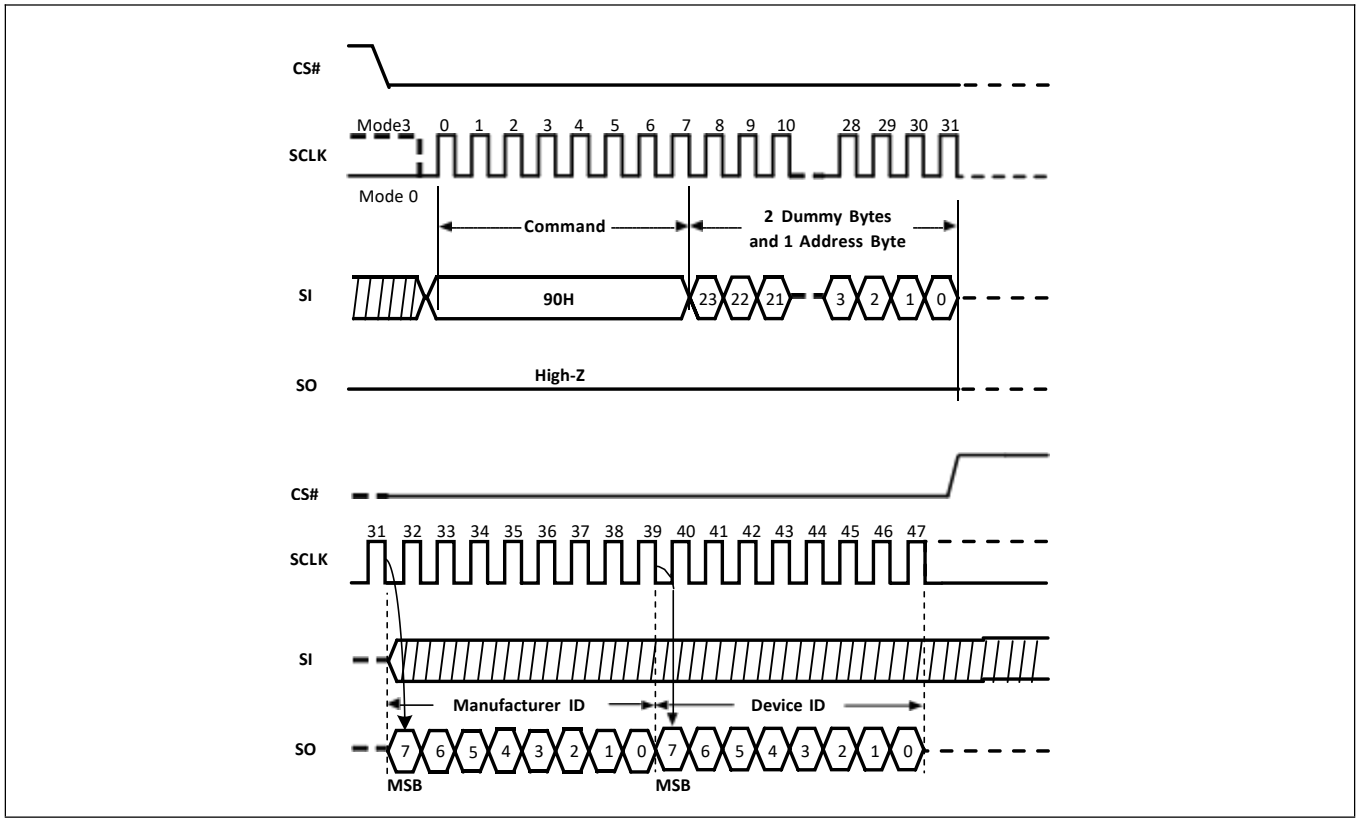
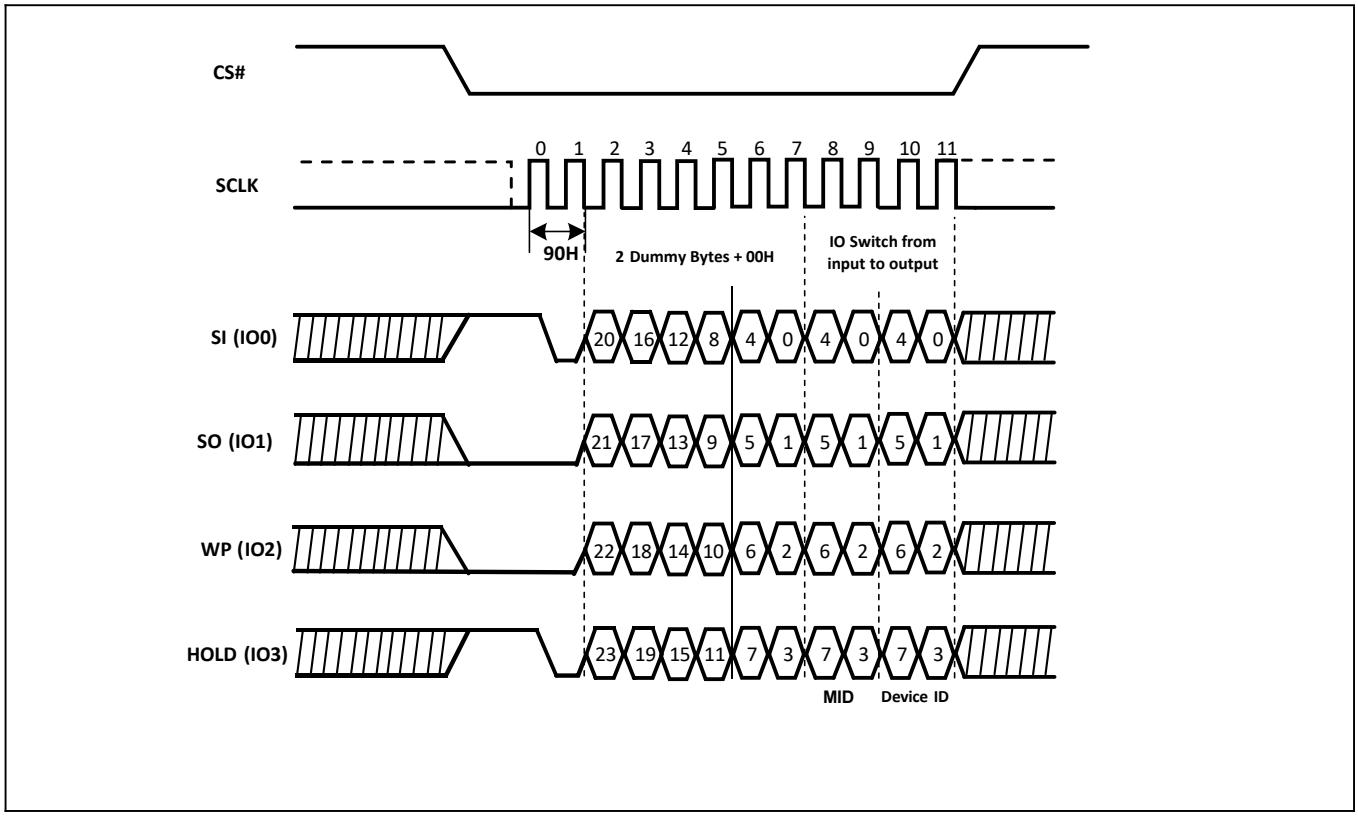


Figure-54. Read Electronic Manufacturer ID & Device ID Sequence Diagram (QPI)



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4.30 Read Identification (RDID) (9FH)

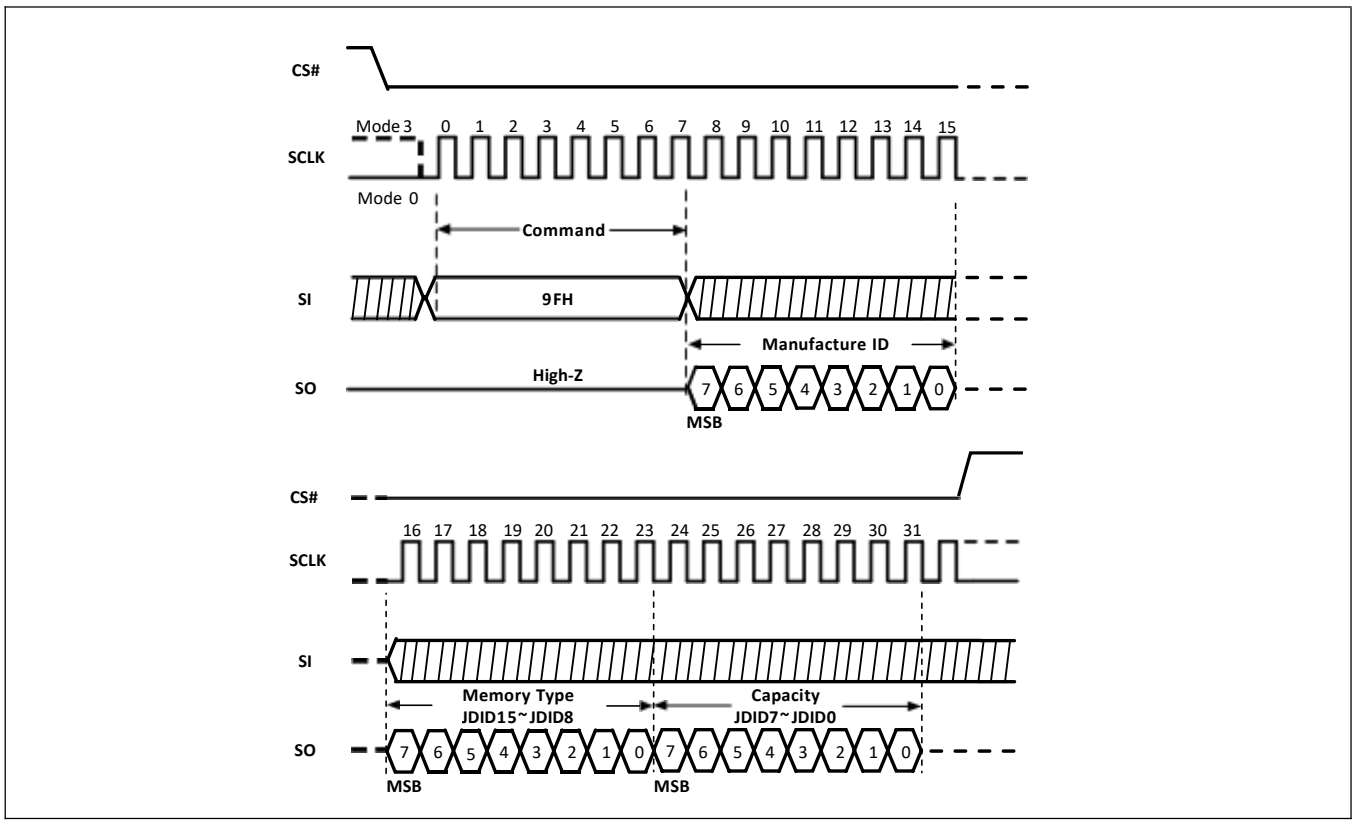
The Read Identification (9FH) command allows the 8-bit Manufacturer ID to be read, followed by two bytes of Device ID. The Device ID indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The ZETTA Manufacturer ID and Device ID are list as "Tables of ID Definition" (Table-11).

Any RDID command issued while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The RDID command should not be issued while the device is in Deep Power down mode.

The device is first selected by driving the CS# Low. Then the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification stored in the memory, shifted out on the SO pin on the falling edge of SCLK. The command sequence is shown in Figure-55. The RDID command is terminated by driving CS# High at any time during data output.

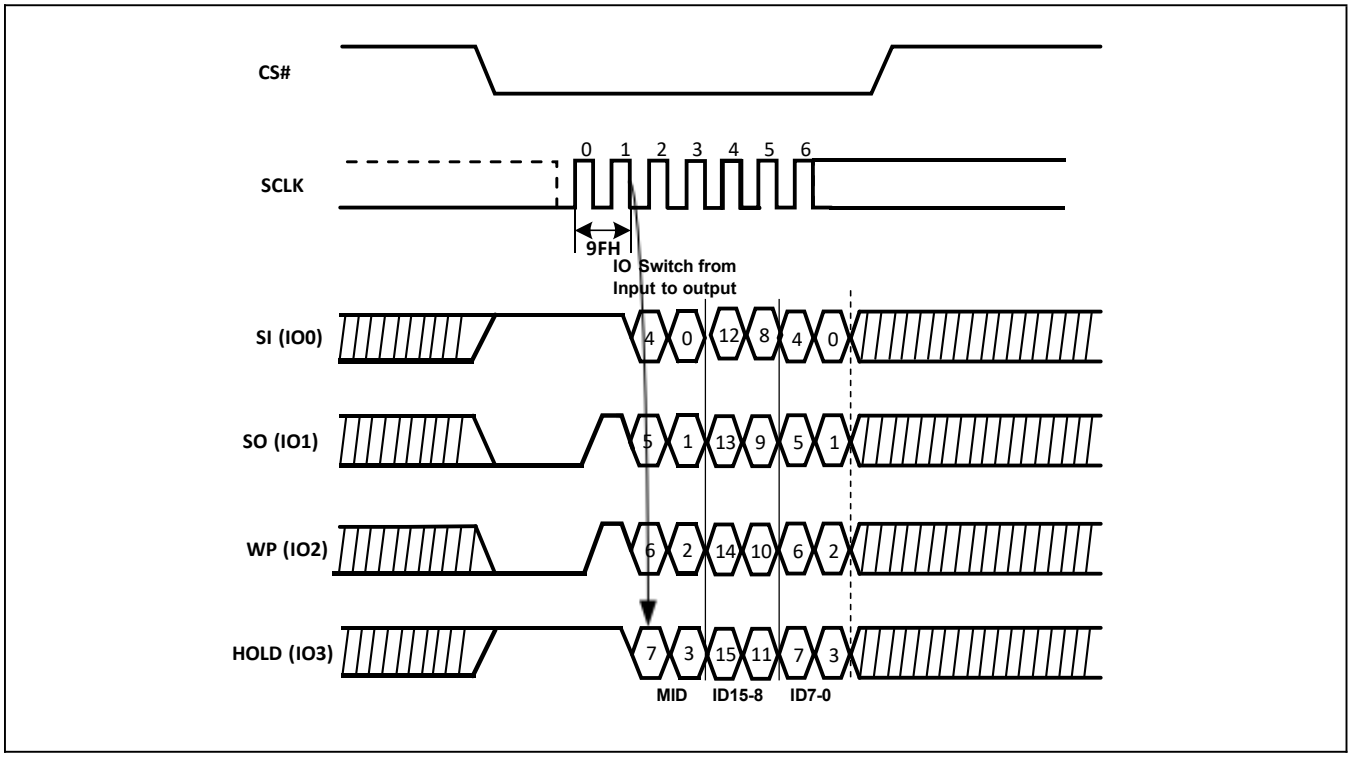
When CS# is driven High, the device is placed in the standby mode. Once in the standby stage, the device waits to be selected, so that it can receive, decode and execute commands.

Figure-55. Read Identification Sequence Diagram



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Figure-56. Read Identification Sequence Diagram (QPI)



4.31 Program/Erase Suspend/Resume (75H)

The Program/Erase Suspend command “75H”, allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H, 31H, 11H) and Erase/Program Security Registers command (44H, 42H) and Erase commands (20H, 52H, D8H, C7H, 60H) and Page Program command (02H, 32H) are not allowed during Program suspend. The Write Status Register command (01H, 31H, 11H) and Erase Security Registers command (44H) and Erase commands (20H, 52H, D8H, C7H, 60H) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS1/SUS2 bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS1/SUS2 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within “tsus” and the SUS1/SUS2 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state.

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Figure-57. Program/Erase Suspend Sequence Diagram (SPI)

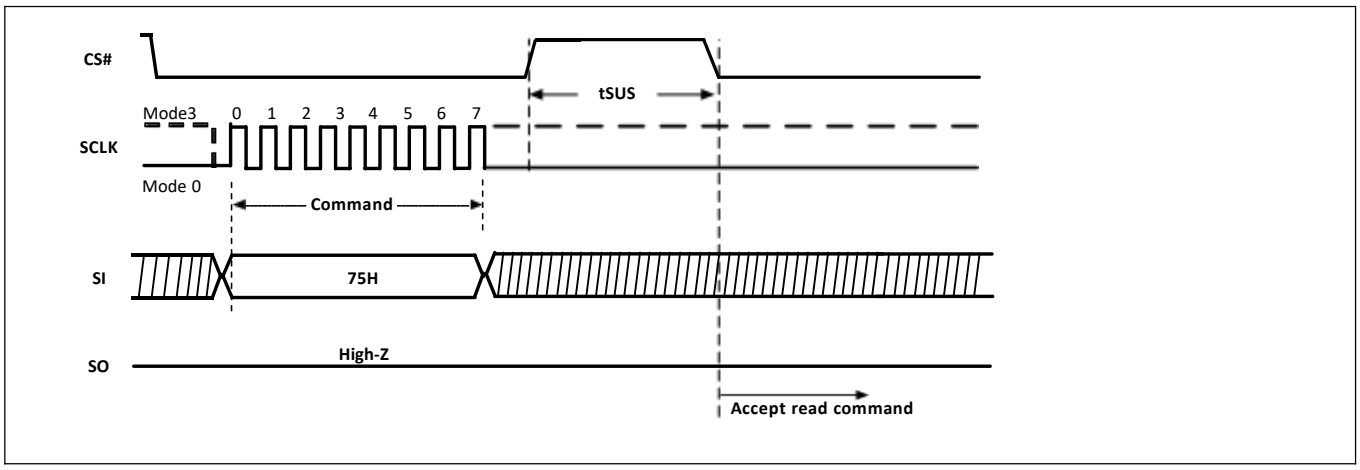
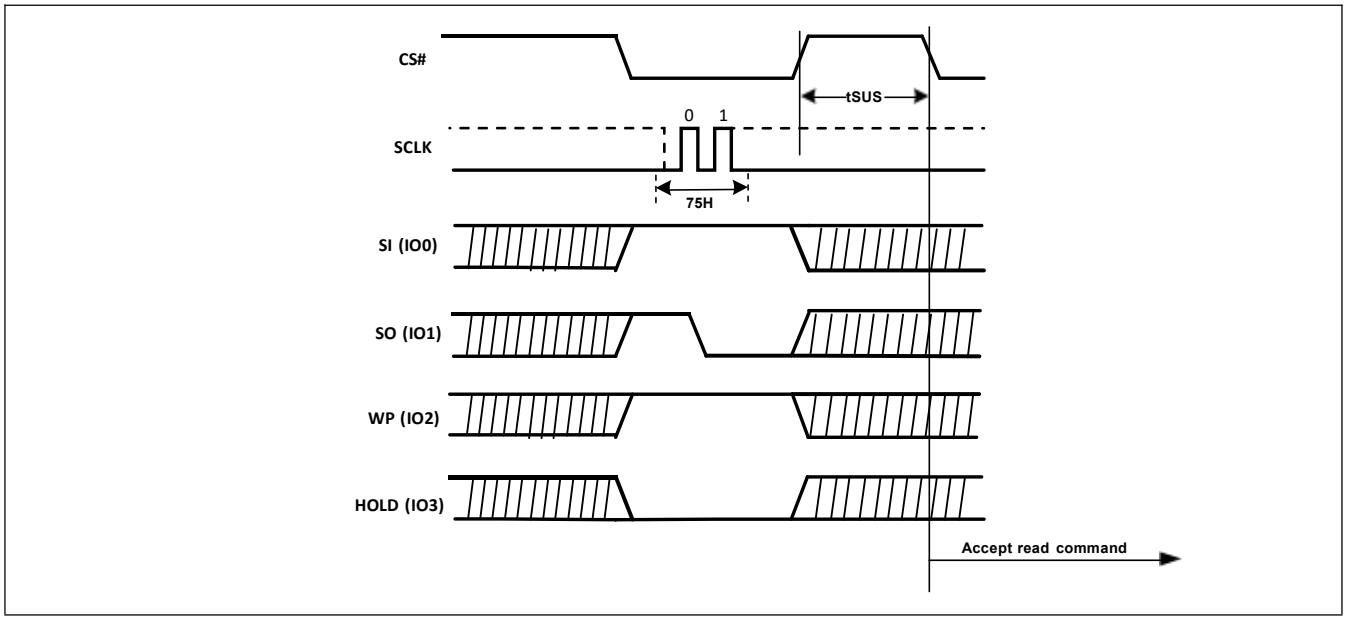


Figure-58. Program/Erase Suspend Sequence Diagram (QPI)



4.32 Program Resume and Erase Resume (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the SUS1/SUS2 bit equal to 1 and the WIP bit equal to 0. After issued the SUS1/SUS2 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

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Figure-59. Program/Erase Resume Sequence Diagram

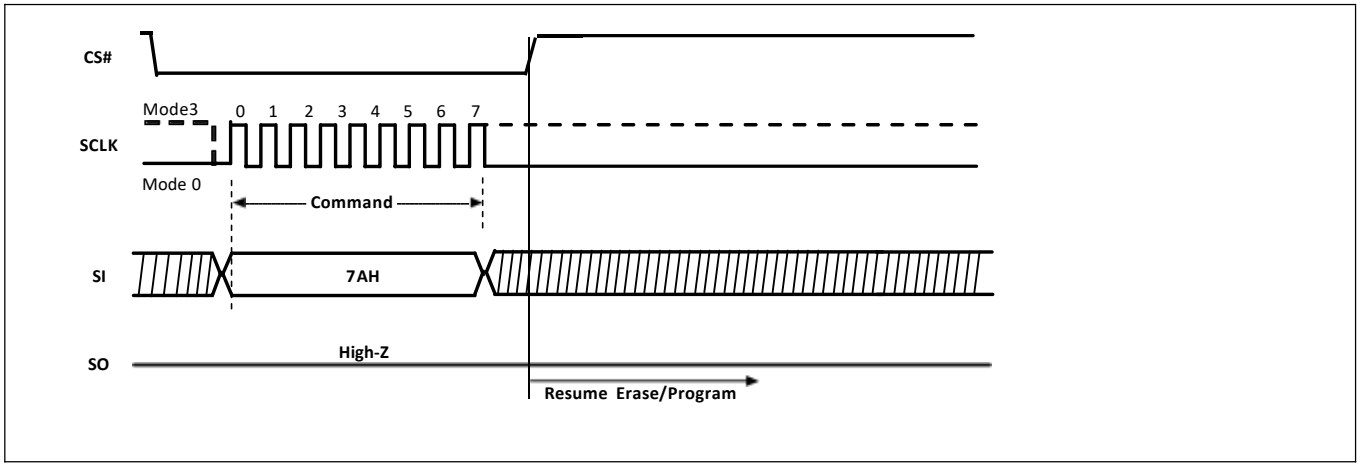
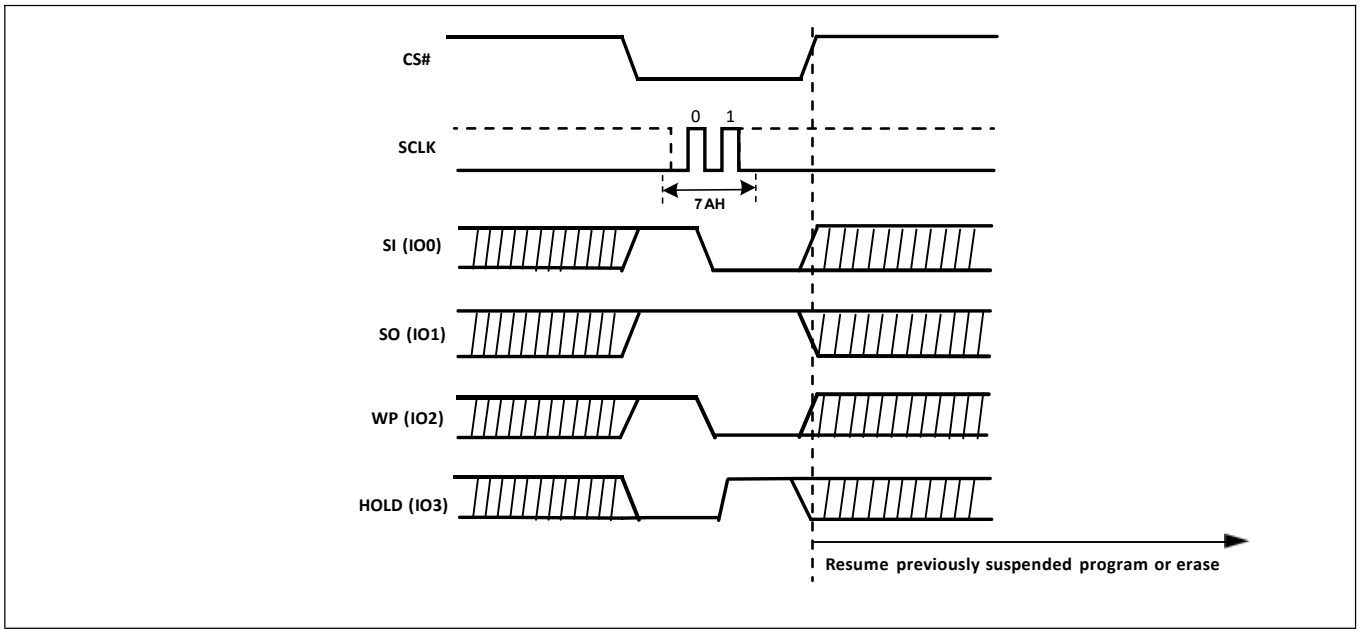


Figure-60. Program Resume and Erase Resume Sequence Diagram (QPI)



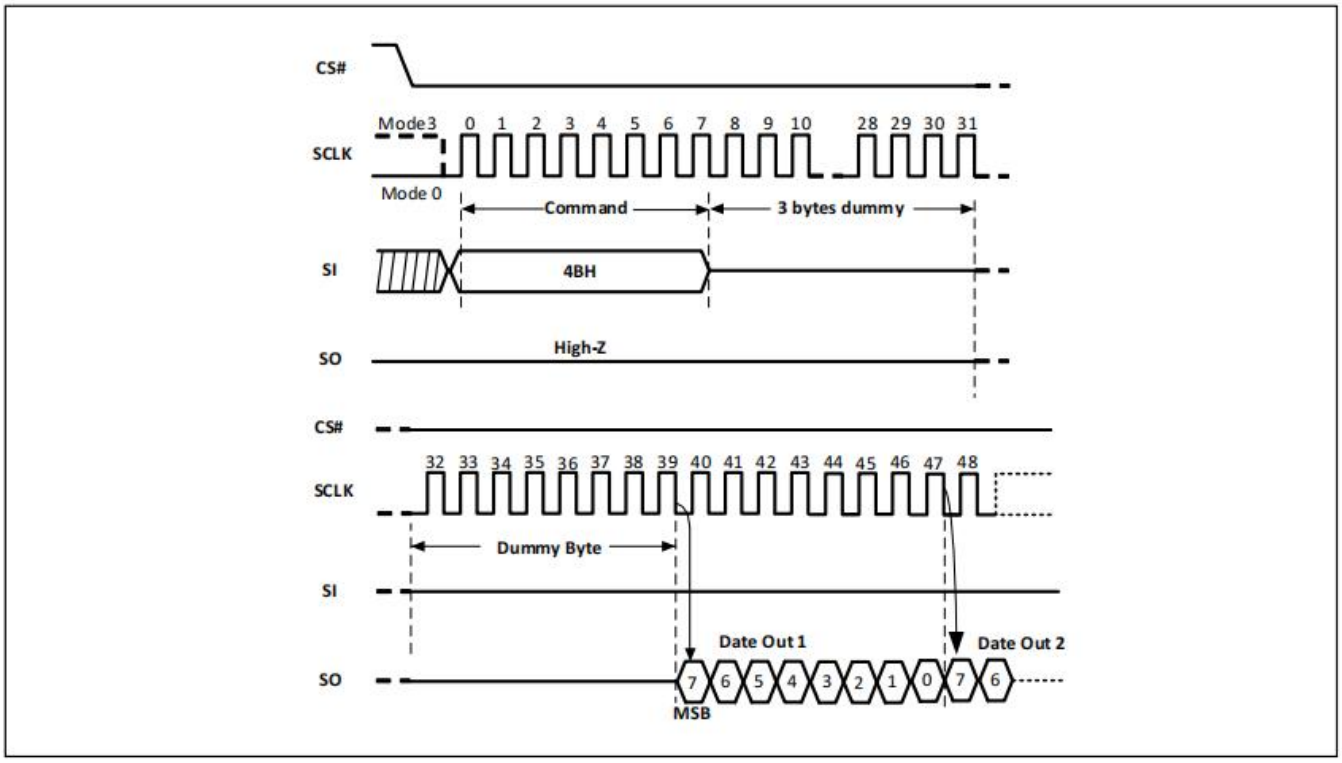
4.33 Read Unique ID (RUID) (4BH)

The Read Unique ID (4BH) command accesses a factory-set read-only 128-bit number that is unique to each ZD25Q128C device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The RUID command is initiated by driving the CS# pin low and shifting the command code “4BH” followed by four dummy bytes. Then, the 128-bit ID is shifted out on the falling edge of SCLK as shown in Figure-61.

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Figure-61. Read Unique ID Sequence Diagram



4.34 Read SFDP Mode (RDSFDP) (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be queried by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a JEDEC Standard, JESD216B.

ZD25Q128C features the Read SFDP Mode (5AH) command. The host system can retrieve the operating characteristics, structure and vendor specified information such as identifying information, memory size, operating voltage and timing information of this device by SFDP mode.

The device is first selected by driving Chip Select (CS#) Low. The command code for the RDSFDP is followed by a 3-byte address (A23~A0) and a dummy byte, with each bit latched-in on the rising edge of Serial Clock (SCLK). Then the memory contents, at the specified address, is shifted out on Data Output (SO) at a maximum frequency fC on the falling edge of SCLK.

The command sequence is shown in Figure-62. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The entire SFDP table can, therefore, be read with a single RDSFDP command. When the highest address is reached, the address counter rolls over to 0x00h, allowing the read sequence to be continued indefinitely. The RDSFDP command is terminated by driving CS# High. CS# can be driven High at any time during data output. Any RDSFDP commands issued, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure-62. Read Serial Flash Discoverable Parameter Sequence Diagram

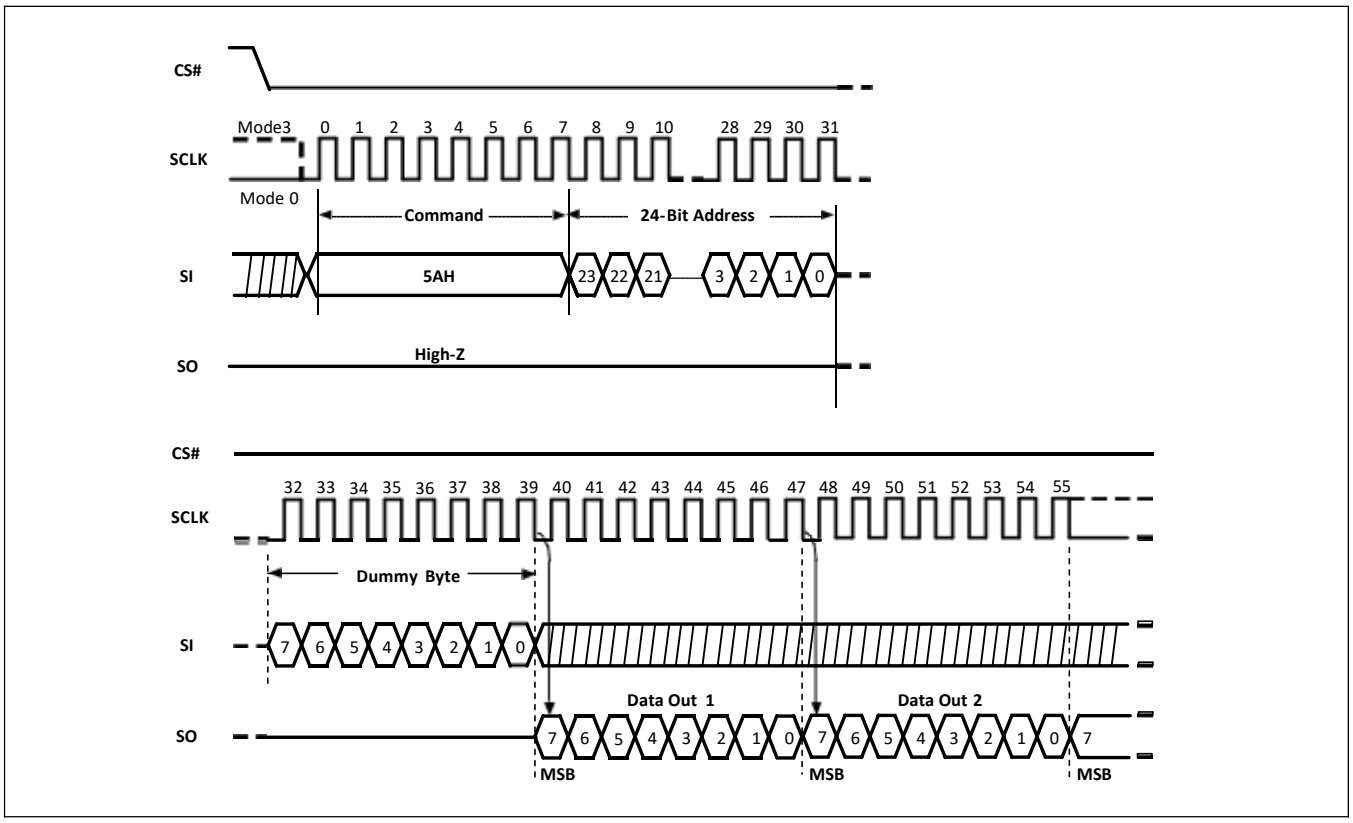


Figure-63. Read Serial Flash Discoverable Parameter Sequence Diagram (QPI)

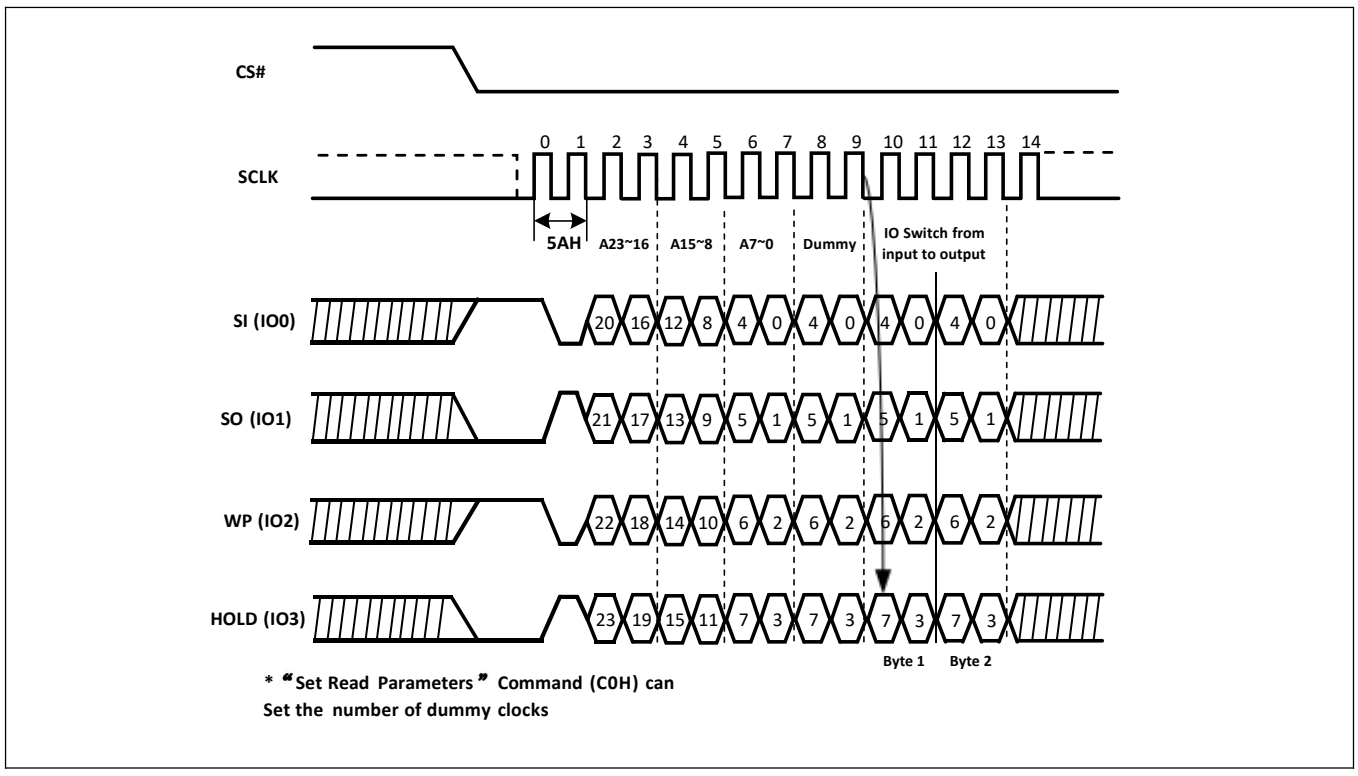


Table-14. Serial Flash Discoverable Parameter (SFDP) Table

Description	Comment	Add (H) (Byte)	DW Add (Bit)	Data
SFDP Signature	Fixed: 50444653H	00H	07:00	53H
		01H	15:08	46H
		02H	23:16	44H
		03H	31:24	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	00H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	00H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H
		0DH	15:08	00H
		0EH	23:16	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH
ID Number (ZETTA Device Manufacturer ID)	It is indicates manufacturer ID	10H	07:00	----
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H
Parameter Table Pointer (PTP)	First address of ZETTA Flash Parameter table	14H	07:00	60H
		15H	15:08	00H
		16H	23:16	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH

Description	Comment	Add (H) (Byte)	DW Add (Bit)	Data	
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	
(1-1-2) Fast Read	0=Not support, 1=Support	32H	16	1b	F9H
Address Bytes Number used in addressing flash array	00: 3 Byte only, 01: 3 or 4 Byte, 10: 4 Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	1b	
(1-2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1-4-4) Fast Read	0=Not support, 1=Support		21	1b	
(1-1-4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	03FFFFFFH	
(1-4-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1-4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	010b	
(1-4-4) Fast Read Opcode		39H	15:08	EBH	EBH
(1-1-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1-1-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3BH	31:24	6BH	
(1-1-2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H

Description	Comment	Add (H) (Byte)	DW Add (Bit)	Data	
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support	3CH	07:05	000b	08H
(1-1-2) Fast Read Opcode		3DH	15:08	3BH	
(1-2-2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3EH	20:16	00000b	80H
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	100b	
(1-2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43H:41H	31:08	FFH	FFH
Unused		45H:44H	15:00	FFH	FFH
(2-2-2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	FFH	FFH
(4-4-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	4AH	20:16	00000b	00H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type doesn't exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type doesn't exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type doesn't exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type doesn't exist	52H	23:16	08H	08H
Sector Type 4 erase Opcode		53H	31:24	81H	81H

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Description	Comment	Add (H) (Byte)	DW Add (Bit)	Data	
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	61H:60H	15:00	3600H	
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2350H=2.350V 2700H=2.700V	63H:62H	31:16	2700H	
HW Reset# pin	0=not support 1=support	65H:64H	00	1b	F99FH
HW Hold# pin	0=not support 1=support		01	1b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable (66H) before Reset cmd.		11:04	1001 1001b (99H)	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	1b	
Wrap-Around Read mode Opcode		66H	23:16	77H	77H
Wrap-Around Read data length	08H:support 8B Wrap-Around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	67H	31:24	64H	64H
Individual block lock	0=not support 1=support	6BH:68H	00	0b	CBFCH
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFH	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

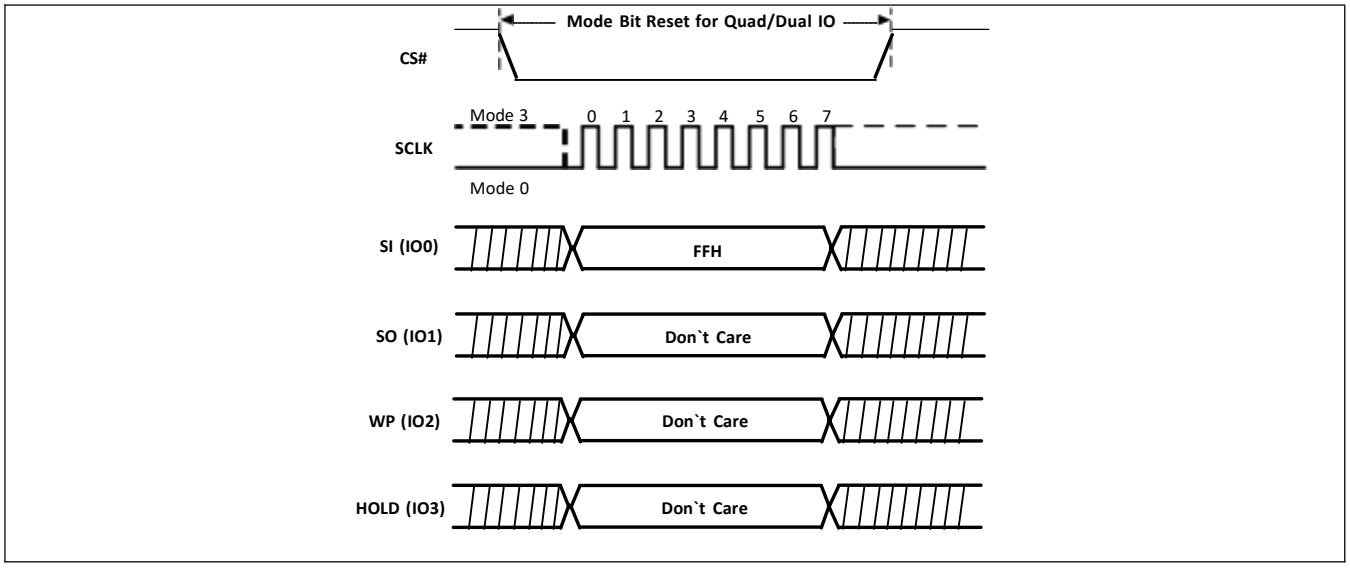
4.35 Continuous Read Mode Reset (CRMR) (FFH)

The “Continuous Read Mode” bits are used in conjunction with Dual I/O Fast Read (BBH) and Quad I/O Fast Read (EBH) commands to provide the highest random Flash memory access rate with minimum SPI command overhead, thus allowing more efficient XIP (execute in place) with this device family. A device that is in a continuous high performance read mode may not recognize any normal SPI command or the Software Reset (66H, 99H) command. It is recommended to use the Continuous Read Mode Reset (FFH) command after a system Power on Reset or, before sending a Software Reset, to ensure the device is released from “Continuous Read Mode”.

The “Continuous Read Mode” bits M7-0 are set by the Dual/Quad I/O Fast Read (BBH or EBH) commands. M5-4 are used to control whether the 8-bit SPI command code (BBH or EBH) is needed or not for the next command. When M5-4 = (1,0), the next command will be treated the same as the current Dual/Quad I/O Fast Read command without requiring the 8-bit command code; when M5-4 do not equal (1,0), the device returns to normal SPI command mode, in which all commands can be accepted. M7-6 and M3-0 are reserved bits for future use, either 0 or 1 values can be used.

Because the ZD25Q128 has no hardware reset pin, if Continuous Read Mode bits are set to (1,0), the ZD25Q128 will not recognize any standard SPI commands. The Continuous Read Mode Reset (FFH) will release the “Continuous Read Mode” and return to normal SPI operation (if in QPI mode, then exit QPI mode together). The command sequence is shown in Figure-64.

Figure-64. Continuous Read Mode Reset Sequence Diagram

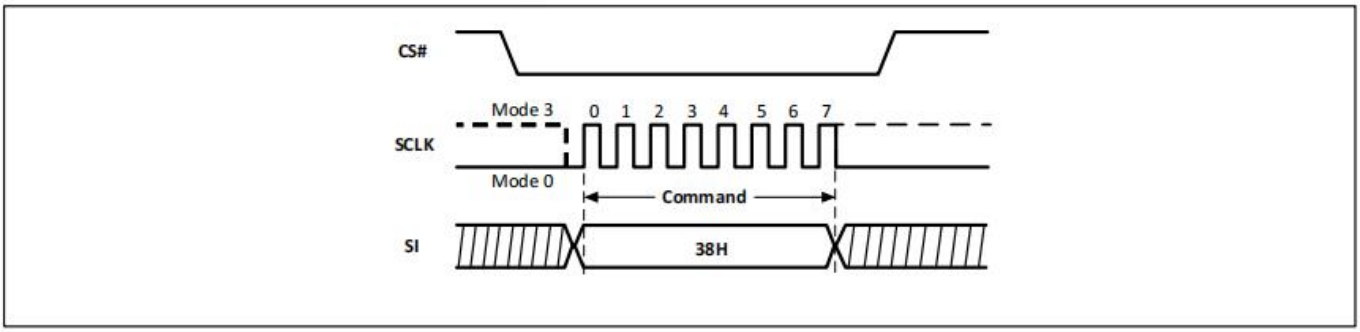


4.36 Enable QPI (38H)

The device support both Standard/Dual/Quad SPI and QPI mode. The “Enable QPI (38H)” command can switch the device from SPI mode to QPI mode. See the command Table 8 for all support QPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-1 must be set to 1 first, and “Enable QPI (38H)” command must be issued. If the QE bit is 0, the “Enable QPI (38H)” command will be ignored and the device will remain in SPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

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Figure-65. Enable QPI (QPI)

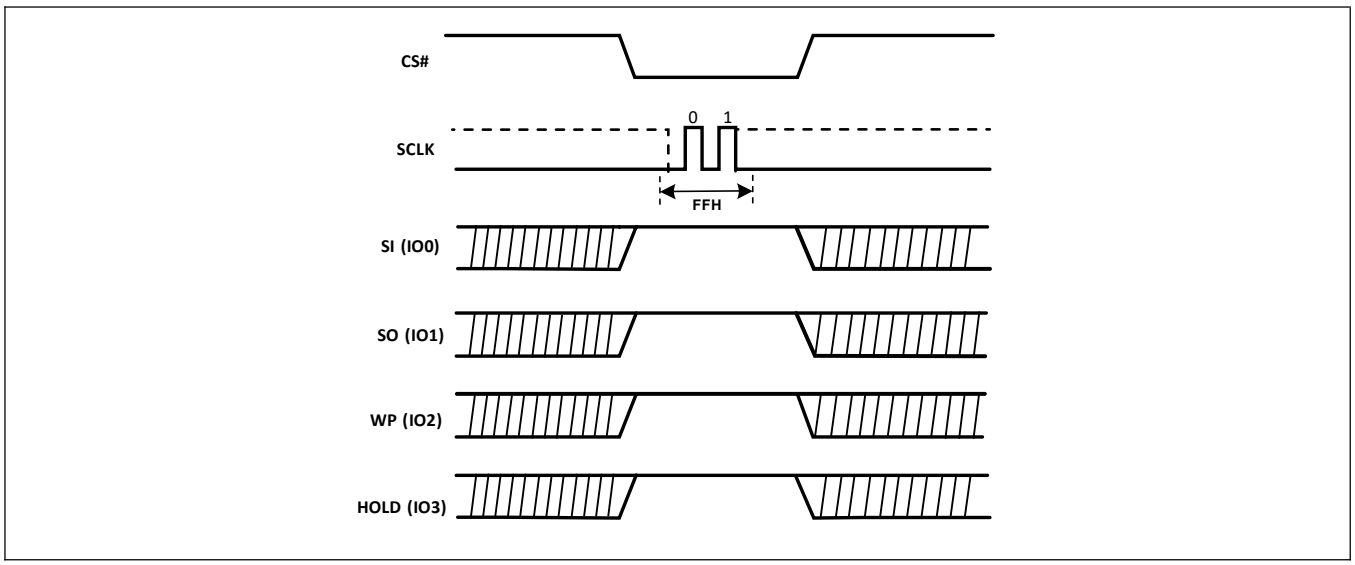


4.37 Disable QPI (FFH)

To exit the QPI mode and return to Standard/Dual/Quad SPI mode, 1) Using "Disable QPI (FFH)" command . 2) Setting QE bit =0, the QPI mode will switch to SPI mode. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Note：this command will exit "Continue read mode" together See **9.41**

Figure-66. Disable QPI (QPI)



4.38 Reset Enable (RSTEN) (66H) and Reset (RST) (99H)

The Software Reset operation combines two commands: Reset Enable (66H) command and Reset (99H) command. It returns the device to standby mode. All the volatile bits and settings will be cleared which returns the device to the same default status as power on. The Reset command immediately following a Reset Enable command, initiates the Software Reset process. Any command other than Reset following the Reset Enable command, will clear the reset enable condition and prevent a later Reset command from being recognized.

If the Reset command is executed during a program or erase operation, the operation will be disabled and the data under processing could be damaged or lost.

Figure-67. Reset Enable and Reset Sequence Diagram

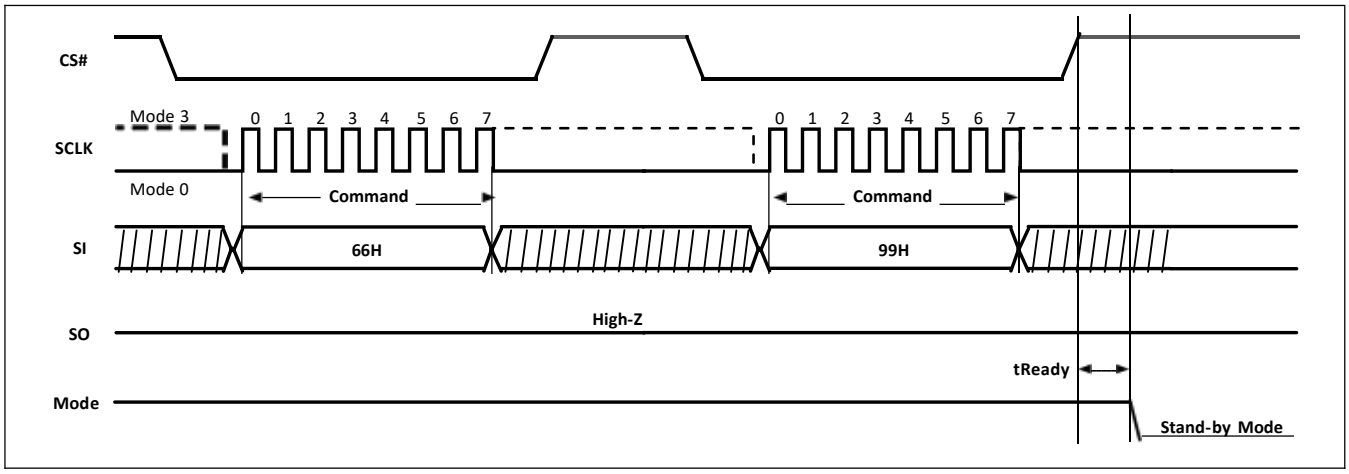
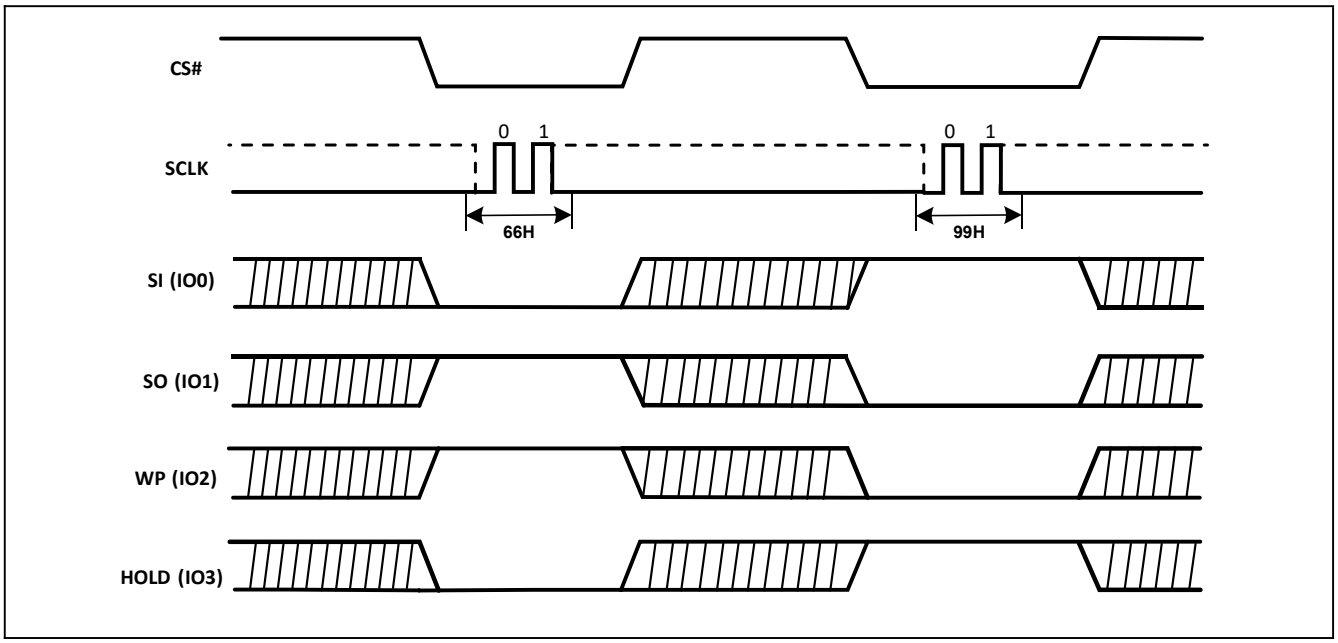


Figure-68. Reset Enable and Reset Sequence Diagram (QPI)



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5.ELECTRICAL SPECIFICATIONS

5.1 Power-On Timing

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure-69. AC Timing at Device Power-Up

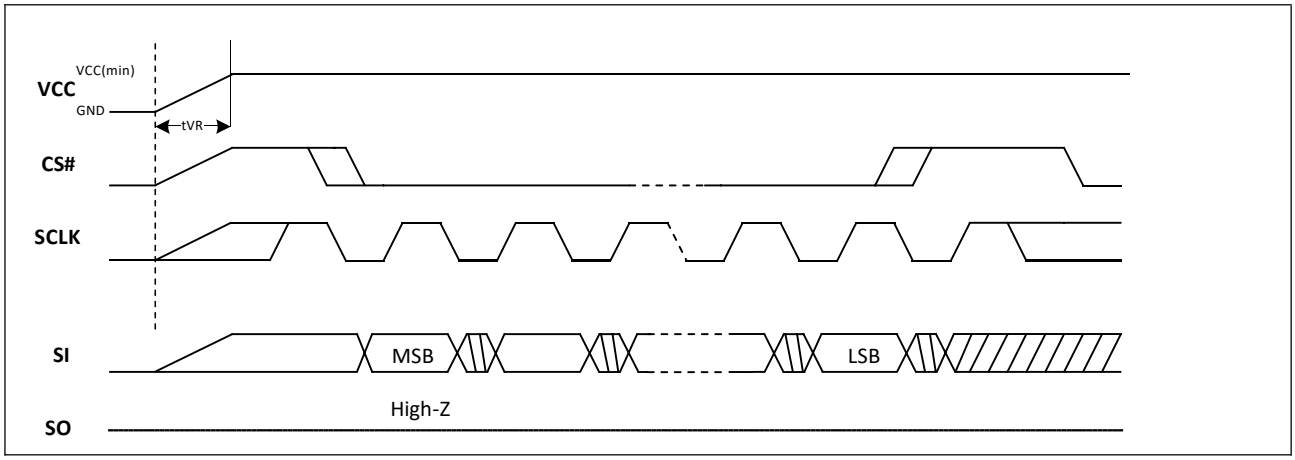


Figure-70. Power-On Timing Sequence Diagram

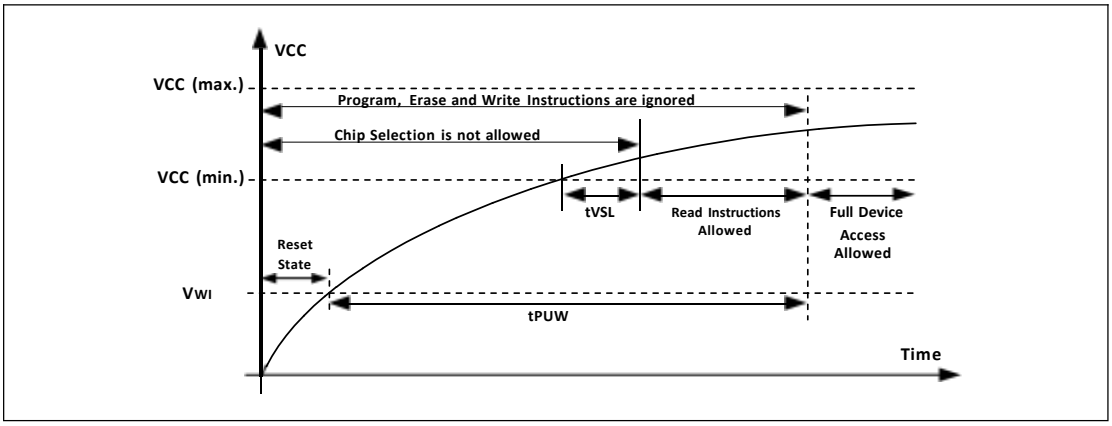
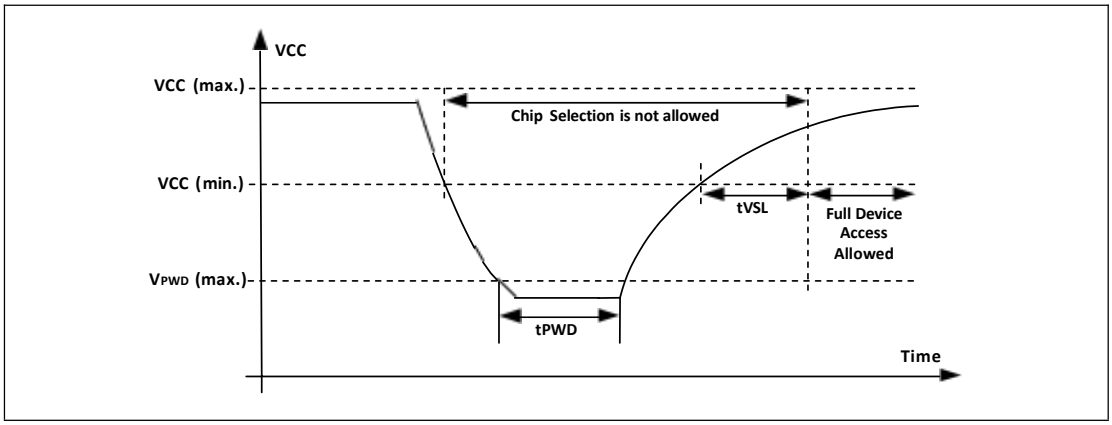


Figure-71. Power-Down and Voltage Drop



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Table-15 Power-Up Timing and Write Inhibit Threshold

Sym.	Parameter	Min.	Max.	Unit
tVSL	VCC(min.) to device operation	20		us
VWI	Write Inhibit Voltage	1.5	2.5	V
tPUW	Time Delay Before Write Instruction	5		ms
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.9	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVR	Vcc Rise Time	1	500000	us/V

5.2 Initial Delivery State

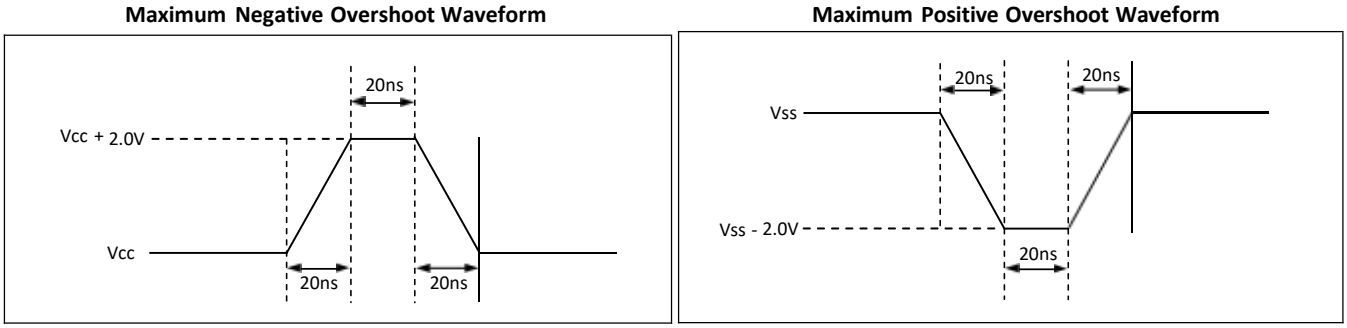
The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0)

5.3 Absolute Maximum Ratings

Table-16 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 105	°C
Storage Temperature	-65 to 150	°C
Applied Input / Output Voltage	-0.6 to VCC+0.4	V
Transient Input / Output Voltage(note: overshoot)	-2.0 to VCC+2.0	V
VCC	-0.6 to 4.2	V

Figure-72. Maximum Negative/positive Overshoot Diagram



5.4 AC Measurement Conditions

Table-17. AC Measurement Conditions

Sym.	Parameter	Min.	Typ.	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN = GND
COUT	Output Capacitance			8	pF	VOUT = GND
CL	Load Capacitance		30		pF	
	Input			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC				

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Figure-73. Data Input Test Waveforms and Measurement Level

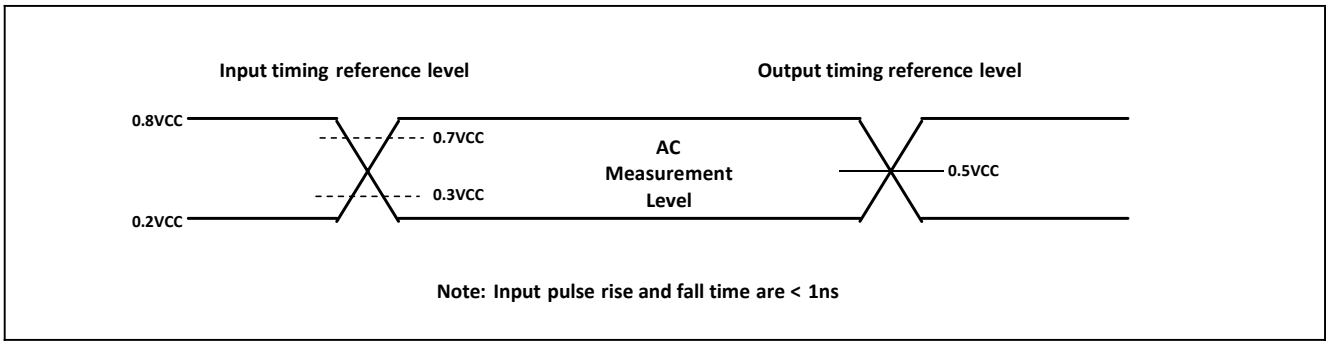
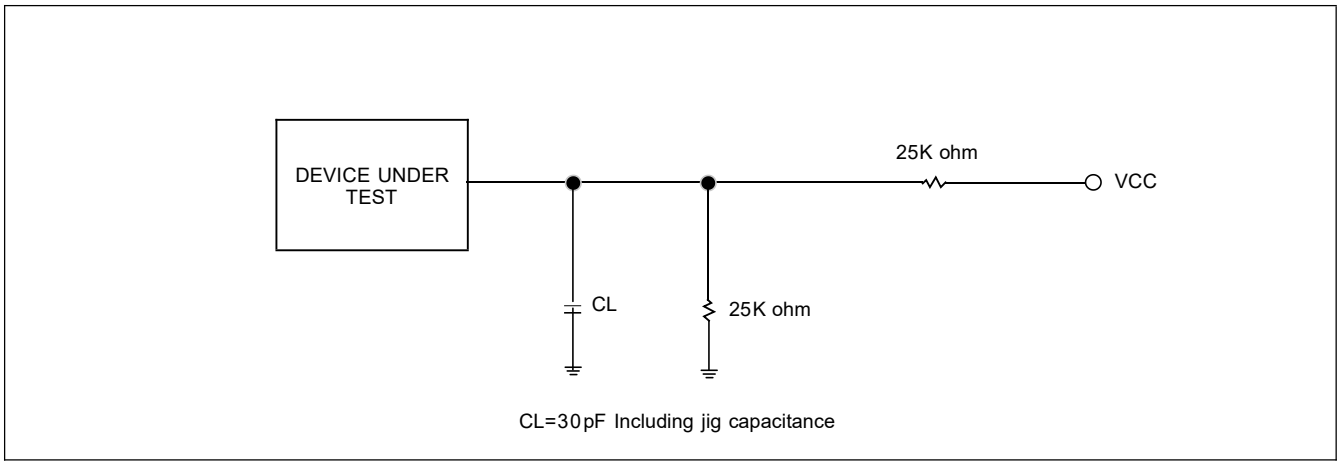


Figure-74. OUTPUT LOADING



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5.5 DC Characteristics

Table-18. DC Parameters (Ta=-40。C to +85。C)

Symbol	Parameter	Conditions	2.7V to 3.6V			Units
			Min.	Typ.	Max.	
$I_{DPD(Icc2)}$	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc		1	6	uA
$I_{SB(Icc1)}$	Standby current	CS#, HOLD#, WP#=Vcc all inputs at CMOS levels		12	55	uA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(*1,*2,*4 I/O)		10	18	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		9	15	mA
I_{CC4}	Program current	CS#=Vcc		16	20	mA
I_{CC5}	Write SR current	CS#=Vcc		16	20	mA
I_{CC6}	Erase current	CS#=Vcc		16	20	mA
I_{LI}	Input load current	All inputs at CMOS level			±2	uA
I_{LO}	Output leakage	All inputs at CMOS level			±2	uA
V_{IL}	Input low voltage				0.2Vcc	V
V_{IH}	Input high voltage		0.7Vcc			V
V_{OL}	Output low voltage	IOL=100uA			0.2	V
V_{OH}	Output high voltage	IOH=-100uA	Vcc-0.2			V

Note:

1. Typical values measured at VCC = 3.3V , T = 25°C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

Table-19. DC Parameters (Ta=-40。C to +105。C)

Symbol	Parameter	Conditions	2.7V to 3.6V			Units
			Min.	Typ.	Max.	
$I_{DPD(Icc2)}$	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc		1	22	uA
$I_{SB(Icc1)}$	Standby current	CS#, HOLD#, WP#=Vcc all inputs at CMOS levels		15	75	uA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(*1,*2,*4 I/O)		14	23	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		9	20	mA
I_{CC4}	Program current	CS#=Vcc		15	35	mA
I_{CC5}	Write SR current	CS#=Vcc		16	32	mA
I_{CC6}	Erase current	CS#=Vcc		14	31	mA
I_{LI}	Input load current	All inputs at CMOS level			±2	uA
I_{LO}	Output leakage	All inputs at CMOS level			±2	uA
V_{IL}	Input low voltage				0.2Vcc	V
V_{IH}	Input high voltage		0.7Vcc			V
V_{OL}	Output low voltage	IOL=100uA			0.2	V
V_{OH}	Output high voltage	IOH=-100uA	Vcc-0.2			V

Note:

1. Typical values measured at VCC = 3.3V, T = 25°C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

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5.6 AC Characteristics

Table-20. AC Parameters (Ta=-40。C to +85。C)

Symbol	Alt.	Parameter	2.7V~3.6V			Unit
			min	typ	max	
FR	fC1	Clock frequency except for Read Data (03h) & DTR instructions (3.0V-3.6V)			133	MHz
FR	fC1	Clock frequency except for Read Data (03h) & DTR instructions(2.7V-3.0V)			100	MHz
FR	fC1	Clock frequency DTR instructions(3.0V-3.6V)			65	MHz
FR	fC1	Clock frequency DTR instructions (2.7V-3.0V)			50	MHz
fR		Clock frequency for Read Data instruction (03h)			50	MHz
tCH(1)	tCLH	Clock High Time	3.5			ns
tCL(1)	tCLL	Clock Low Time (fSCLK) 45% x (1fSCLK)	4.0			ns
tCLCH(2)		Clock Rise Time (peak to peak)	0.1			v/ns
tCHCL(2)		Clock Fall Time (peak to peak)	0.1			v/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	6			ns
tDVCH	tDSU	Data In Setup Time	2			ns
tCHDX	tDH	Data In Hold Time	3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	5			ns
tSHSL	tCSH	CS# Deselect Time From Read to next Read	11			ns
		CS# Deselect Time From Write,Erase,Program to Read Status Register	50			ns
		Volatile Status Register Write Time	50			ns
tSHQZ(2)	tDIS	Output Disable Time			7	ns
tCLQV	tV	Clock Low to Output Valid Loading 30pF			8	ns
		Clock Low to Output Valid Loading 15pF			6	ns
tCLQX	tHO	Output Hold Time	1.5			ns
tHLCH		HOLD# Active Setup Time (relative to SCLK)	5			ns
tCHHH		HOLD# Active Hold Time (relative to SCLK)	5			ns
tHHCH		HOLD# Not Active Setup Time (relative to SCLK)	6			ns
tCHHL		HOLD# Not Active Hold Time (relative to SCLK)	5			ns
tHHQX	tLZ	HOLD# to Output Low-Z			7	ns
tHLQZ	tHZ	HOLD# to Output High-Z			11	ns
tWHSL(3)		Write Protect Setup Time	20			ns
tSHWL(3)		Write Protect Hold Time	100			ns
tDP		CS# High to Deep Power-down Mode			3	us
tRES1		CS# High To Standby Mode Without Electronic Signature Read			22	us
tRES2		CS# High To Standby Mode With Electronic Signature Read			20	us
tSUS		CS# High To Next Command After Suspend			20	us
tRS		Latency Between Resume And Next Suspend	100			us
tRST		CS# High to next Instruction after Reset			31	us
tW		Write Status Register Cycle Time		10	15	ms
tBP1		Byte Program Time (First Byte)		40	70	us
tBP2		Additional Byte Program Time (After First Byte)		2.5	12	us

tPP		Page Program Time		0.5	3	ms
tSE		Sector Erase Time (4KB)		43	280	ms
tBE		Block Erase Time (64K Bytes)		0.23	1.8	s
tCE		Chip Erase Time		48	120	s

Note:

1. Typical value at T = 25℃.

2. Value guaranteed by design and/or characterization, not 100% tested in production.

3. Only applicable as a constraint for a Write Status Register instruction when SRP=1.

Table-21. AC Parameters (Ta=-40。C to +105。C)

Symbol	Alt.	Parameter	2.7V~3.6V			Unit
			min	typ	max	
F_R	f_{C1}	Clock frequency except for Read Data (03h) & DTR instructions (3.0V-3.6V)			133	MHz
F_R	f_{C1}	Clock frequency except for Read Data (03h) & DTR instructions(2.7V-3.0V)			104	MHz
F_R	f_{C1}	Clock frequency DTR instructions(3.0V-3.6V)			66	MHz
F_R	f_{C1}	Clock frequency DTR instructions (2.7V-3.0V)			52	MHz
f_R		Clock frequency for Read Data instruction (03h)			50	MHz
tCH(1)	tCLH	Clock High Time	4.0			ns
tCL(1)	tCLL	Clock Low Time (fSCLK) 45% x (1fSCLK)	4.0			ns
tCLCH(2)		Clock Rise Time (peak to peak)	0.1			v/ns
tCHCL(2)		Clock Fall Time (peak to peak)	0.1			v/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5			ns
tDVCH	tDSU	Data In Setup Time	2			ns
tCHDX	tDH	Data In Hold Time	3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	5			ns
tSHSL	tCSH	CS# Deselect Time From Read to next Read	10			ns
		CS# Deselect Time From Write,Erase,Program to Read Status Register	50			ns
		Volatile Status Register Write Time	50			ns
tSHQZ(2)	tDIS	Output Disable Time			7	ns
tCLQV	tV	Clock Low to Output Valid Loading 30pF			7	ns
		Clock Low to Output Valid Loading 15pF			6	ns
tCLQX	tHO	Output Hold Time	1.5			ns
tHLCH		HOLD# Active Setup Time (relative to SCLK)	5			ns
tCHHH		HOLD# Active Hold Time (relative to SCLK)	5			ns
tHHCH		HOLD# Not Active Setup Time (relative to SCLK)	5			ns
tCHHL		HOLD# Not Active Hold Time (relative to SCLK)	5			ns
tHHQX	tLZ	HOLD# to Output Low-Z			7	ns
tHLQZ	tHZ	HOLD# to Output High-Z			12	ns
tWHSL(3)		Write Protect Setup Time	20			ns
tSHWL(3)		Write Protect Hold Time	100			ns
tDP		CS# High to Deep Power-down Mode			3	us
tRES1		CS# High To Standby Mode Without Electronic Signature Read			20	us
tRES2		CS# High To Standby Mode With Electronic Signature Read			20	us
t_{SUS}		CS# High To Next Command After Suspend			20	us
t_{RS}		Latency Between Resume And Next Suspend	100			us
tRST		CS# High to next Instruction after Reset			30	us
tW		Write Status Register Cycle Time		5	30	ms
t_{BP1}		Byte Program Time (First Byte)		40	140	us
t_{BP2}		Additional Byte Program Time (After First Byte)		2.5	25	us

tPP		Page Program Time		0.5	4	ms
tSE		Sector Erase Time (4KB)		45	500	ms
tBE		Block Erase Time (64K Bytes)		0.25	3.0	s
tCE		Chip Erase Time		50	200	s

Note:

1. Typical value at T = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP=1.

Figure-75. Serial Input Timing

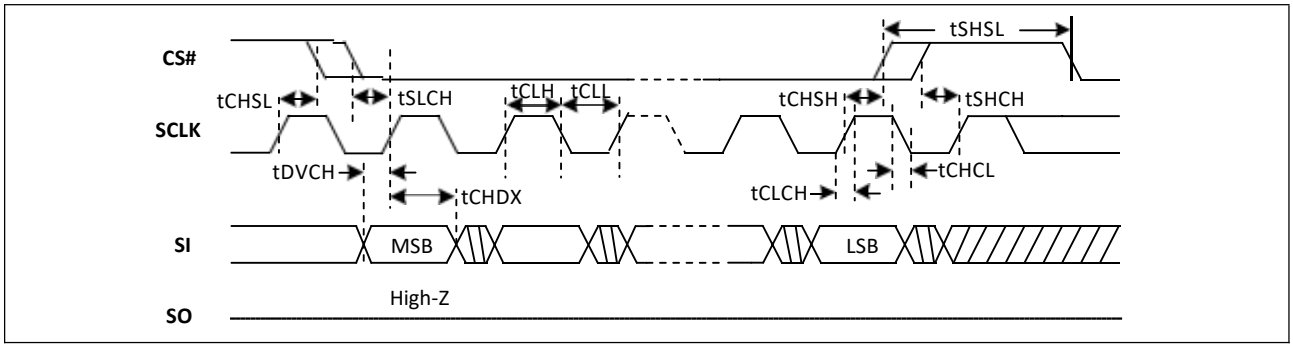


Figure-76. Output Timing

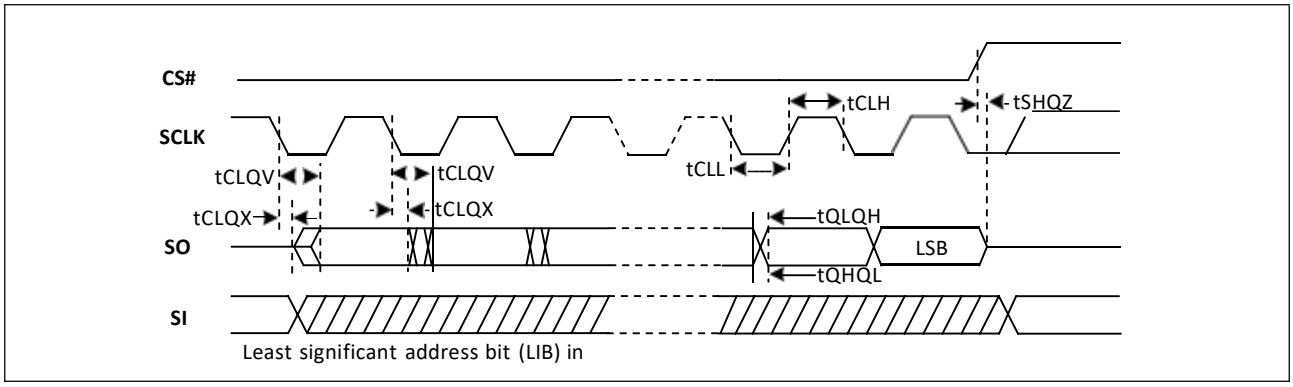
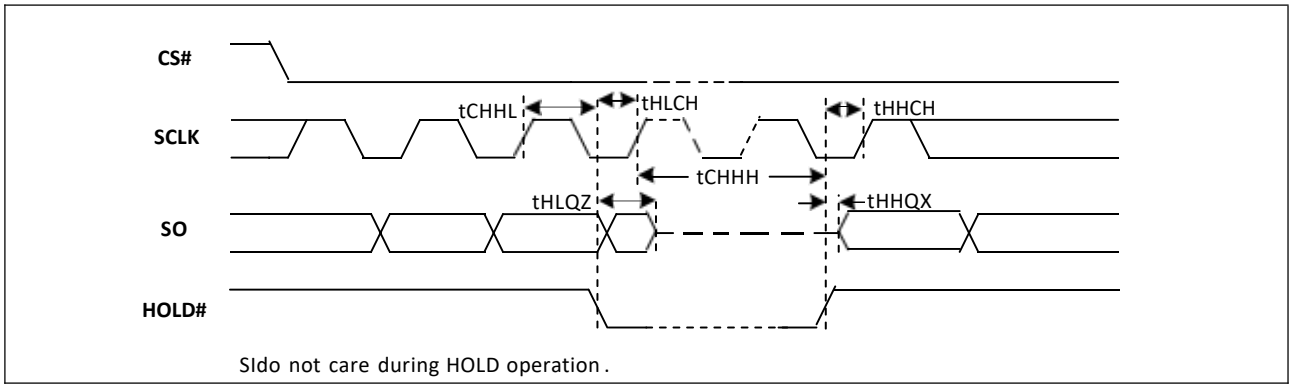


Figure-77. Hold Timing



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Figure-78. WP Timing

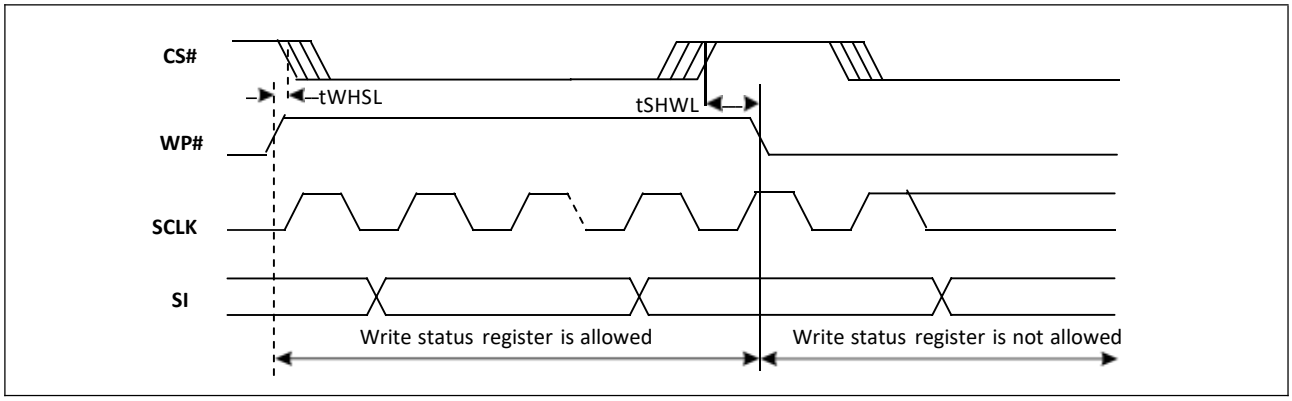


Figure-79. Resume to Suspend Timing Diagram

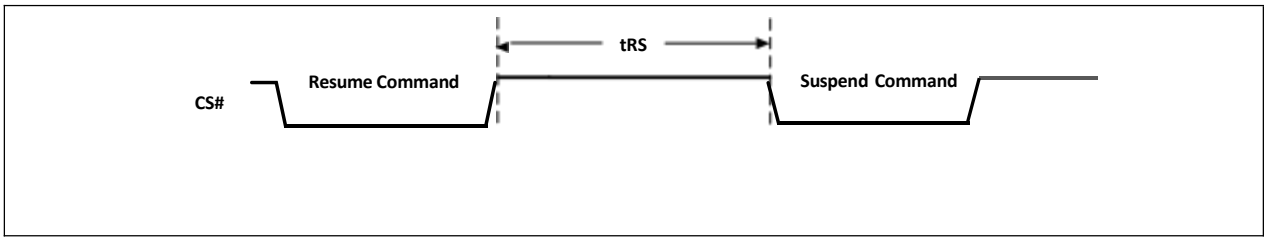


Figure-80. RESET Timing

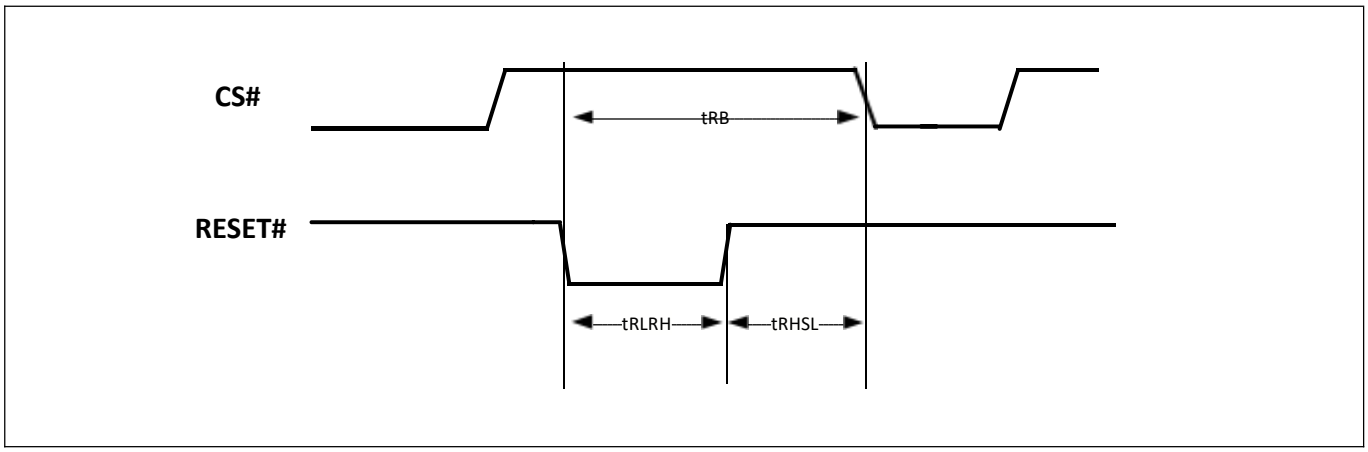
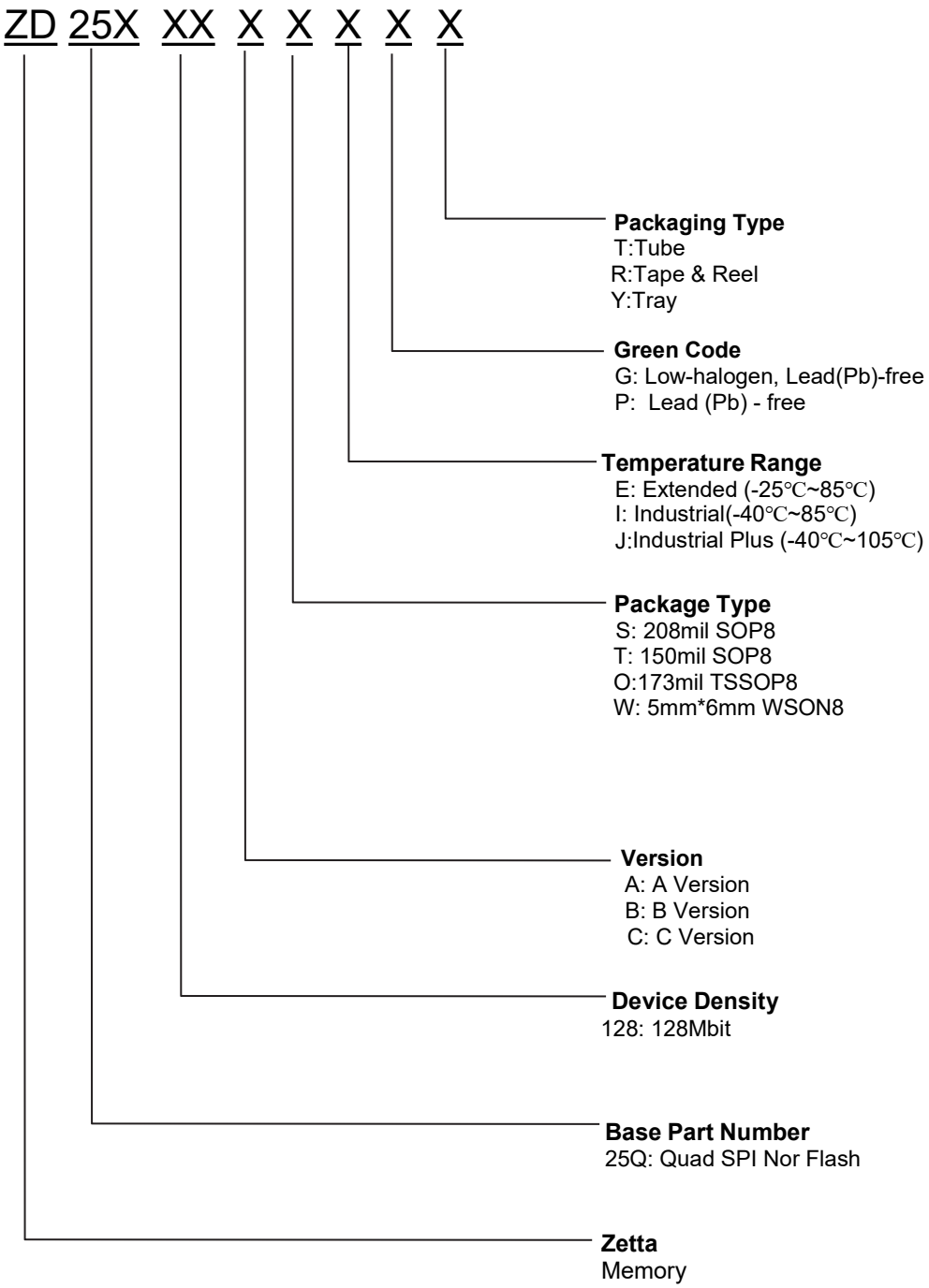


Table-22. Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tRLRH	Reset Pulse Width	1			us
tRHRL	Reset High Time Before Read	50			ns
tRB	Reset Recovery Time			12	ms

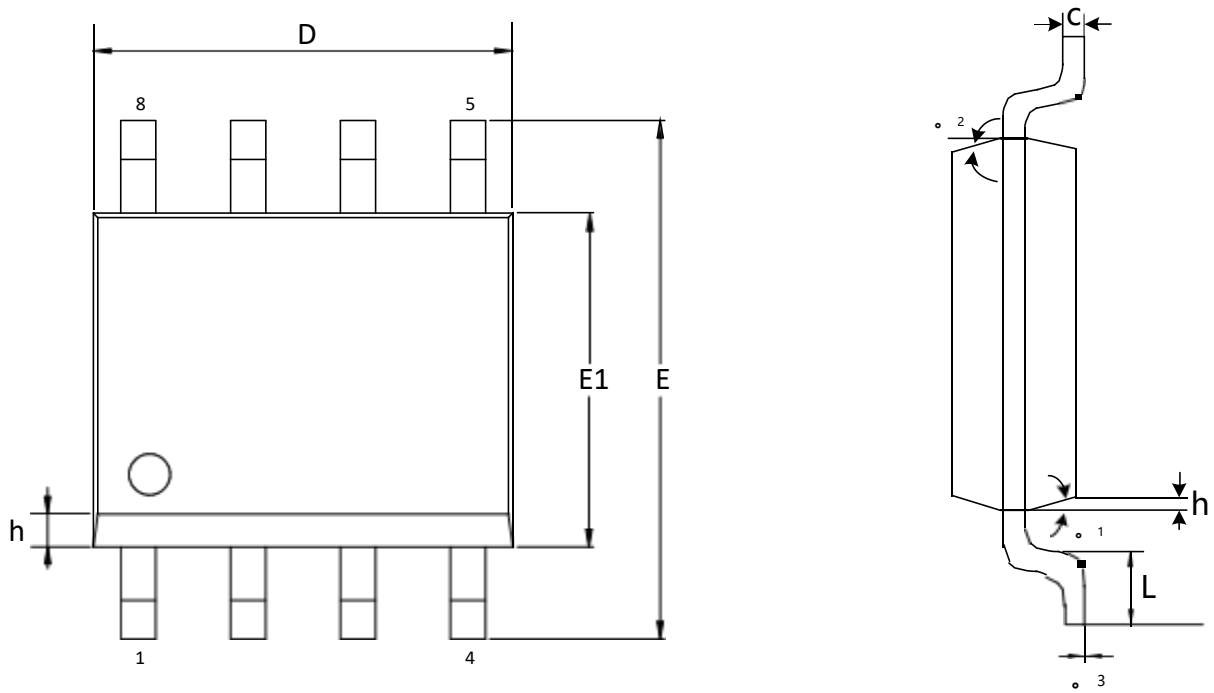
6.ORDERING INFORMATION

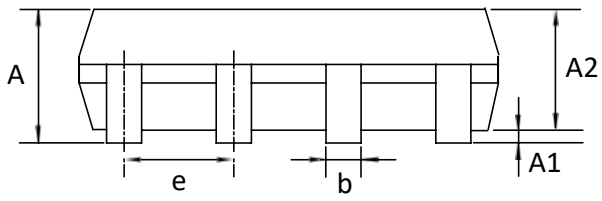


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7.PACKAGE INFORMATION

7.1 Package SOP8 208MIL





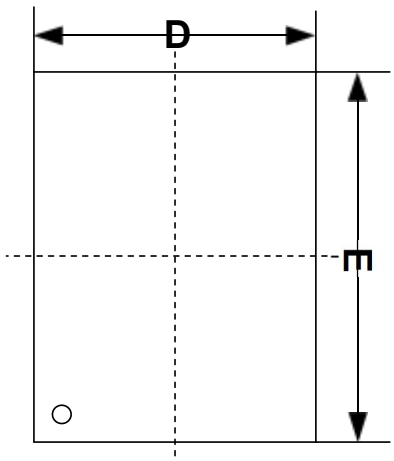
Dimensions

Symbol / Unit		A	A1	A2	b	c	D	E	E1	e	L	h	θ1	θ2	θ3
mm	Min	1.75	0.05	1.70	0.40	0.19	5.13	7.70	5.10	1.17	0.50	0.30			
	Nom	1.95	0.15	1.80	0.45	0.20	5.23	7.90	5.25	1.27	0.65	0.40	-	-	-
	Max	2.15	0.25	1.90	0.50	0.21	5.33	8.10	5.40	1.37	0.80	0.50			

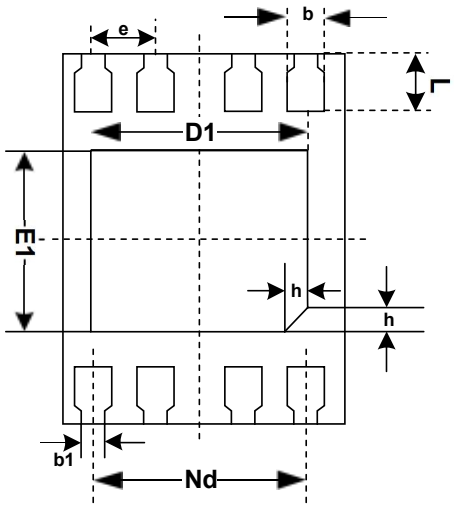
Note:

1. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
2. ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
3. ALL DIMENSIONS MEET JEDEC STANDRAD MS-012F

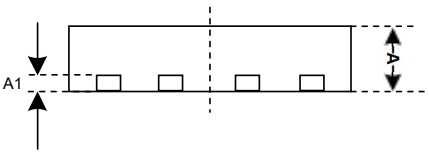
7.2 Package WSON8 (5*6mm)



TOP VIEW



BOTTOM VIEW



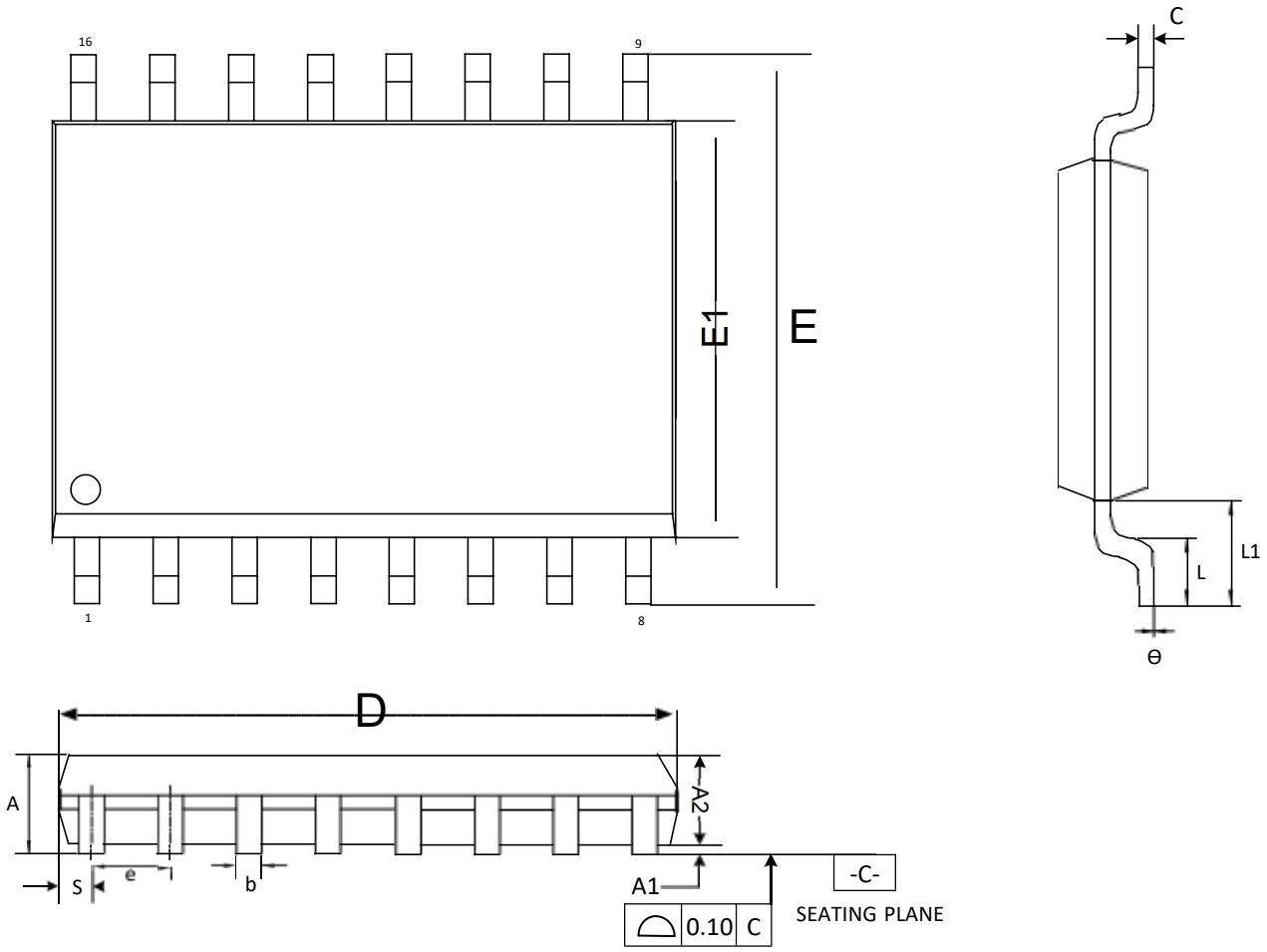
SIDE VIEW

Dimensions

Symbol		A	A1	b	b1	D	D1	e	Nd	E	E1	L	h
mm	Min	0.70	0.203 REF	0.35	0.25 REF	4.90	3.90	1.27BSC	3.81BSC	5.90	3.30	0.55	0.30
	Nom	0.75		0.40		5.00	4.00			6.00	3.40	0.60	0.35
	Max	0.80		0.45		5.10	4.10			6.10	3.50	0.65	0.40

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7.3 16-pin SOP (300mil)



. **Dimensions**

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min	-	0.10	2.25	0.31	0.20	10.10	10.10	7.42	-	0.40	1.31	0.51	0°
	Nom	-	0.20	2.35	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5°
	Max	2.65	0.30	2.45	0.51	0.3	10.50	10.50	7.60	-	1.27	1.57	0.77	8°
Inch	Min	-	0.004	0.089	0.012	0.008	0.397	0.397	0.292	-	0.016	0.052	0.020	0°
	Nom	-	0.008	0.093	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5°
	Max	0.104	0.012	0.096	0.018	0.012	0.413	0.413	0.299	-	0.050	0.062	0.03	8°

8.REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial Release	All	2023-7-11