XT26G02D

3.3V 2G-BIT

SPI NAND FLASH MEMORY

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1. Overview

The XT26G02D is a 2G-bit (256M-byte) SPI (Serial Peripheral Interface) NAND Flash memory, with advanced write protection mechanisms. The XT26G02D supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O option.

2. Features

2G-bit NAND Flash memory
- Single-level cell (SLC) technology
- Page size: 2176 bytes (2048 + 128 bytes)
- Block size: 64 pages (128K + 8K bytes)
- Device size: 2Gb (2048 blocks)

Serial Interface
- Standard SPI: CLK, CS#, SI, SO, WP#
- Dual SPI: CLK, CS#, SIO0, SIO1, WP#
- Quad SPI: CLK, CS#, SIO0, SIO1, SIO2, SIO3

High Performance
- 120MHz for fast read
- Quad I/O data transfer up to 480Mbits/s
- 2K-Byte cache for fast random read

Advanced Security Features
- Write protect all/portion of memory via software
- Lockable 8K-Byte OTP region
- 128-Bit Unique ID for each device
- Parameter Page

Program/Erase/Read Speed
- Page Program time: 360us typical
- Block Erase time: 3.5ms typical
- Page Read time: 130us typical (with ECC)

Single Supply Voltage: 2.7V~3.6V

Advanced Security Features
- 8bit ECC, per 528 bytes (ECC always on)
- Internal data move by page with ECC
- Promised golden block0

Moisture Sensitivity Level: MSL3

Package
- WSON8 (8x6mm)
- LGA8 (6x5mm)
- BGA24 (8x6mm)(6x4 Ball Array)
- All Packages are RoHS Compliant and Halogen-free

Data retention: 10 years

Endurance: 60,000 PROGRAM/ERASE cycles with 8bit/528bytes ECC

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3. Available Ordering OPN

OPN	Temperature	Package Type	Package Carrier
XT26G02DWSIGA	-40℃~85℃	WSON8 8x6mm	Tray
XT26G02DBGIGA	-40℃~85℃	BGA24 8x6mm	Tray
XT26G02DLAIGA	-40℃~85℃	LGA8 6x5mm	Tray

4. Packaging Type and Pin Configurations

XT26G02D is offered in an 8-pin WSON 8x6 mm^2 or an 8-pin LGA 6x5 mm^2 as shown below. Package diagram and dimension are illustrated at the end of this datasheet.

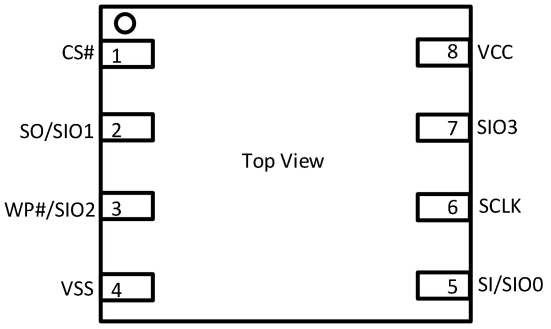


Figure1. Connection Diagram

Pin Description

PIN NO.	PIN NAME	I/O	FUNCTION
1	CS#	I	Chip Select Input
2	SO (SIO_1)	I/O	Data Output (Data Input Output 1) (1)(2)
3	WP# (SIO_2)	I/O	Write Protect Input (Data Input Output 2)(2)(3)
4	VSS		Ground
5	SI (SIO_0)	I/O	Data Input (Data Input Output 0)(1)(2)
6	CLK	I	Serial Clock Input
7	SIO_3	I/O	Data Input Output 3(2)
8	VCC		Power Supply

Notes:

1. SIO0 and SIO1 are used for Dual SPI instructions.
2. SIO0 – SIO3 are used for Quad SPI instructions.
3. The WP# pin is pull up to VCC internally.

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XT26G02D is offered in a BGA24 8x6 mm^2 as shown below. Package diagram and dimension are illustrated at the end of this datasheet.

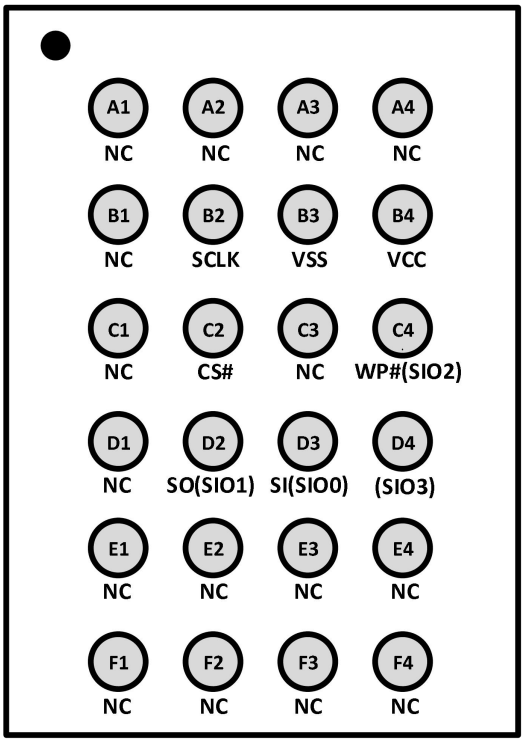


Figure2. BGA24 8x6mm (6x4 Ball Array) Connection Diagram

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BGA24 8x6mm (6x4 Ball Array) Pin Description

Pin No.	Pin Name	I/O	Description
A1	NC		No Connection
A2	NC		No Connection
A3	NC		No Connection
A4	NC		No Connection
B1	NC		No Connection
B2	SCLK	I	Serial Clock Input
B3	VSS		Ground
B4	VCC		Power Supply
C1	NC		No Connection
C2	CS#	I	Chip Select Input
C3	NC		No Connection
C4	WP#/SIO2	I/O	Write Protect Input/Data Input Output2[2][3]
D1	NC		No Connection
D2	SO/SIO1	I/O	Data Output/Data Input Output1[1][2]
D3	SI/SIO0	I/O	Data Input /Data Input Output0[1][2]
D4	SIO3	I/O	Data Input Output3[2]
E1	NC		No Connection
E2	NC		No Connection
E3	NC		No Connection
E4	NC		No Connection
F1	NC		No Connection
F2	NC		No Connection
F3	NC		No Connection
F4	NC		No Connection

Notes:

1. SIO0 and SIO1 are used for Dual SPI instructions.
2. SIO0 – SIO3 are used for Quad SPI instructions.
3. The WP# pin is pull up to VCC internally.

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5. Block Diagram

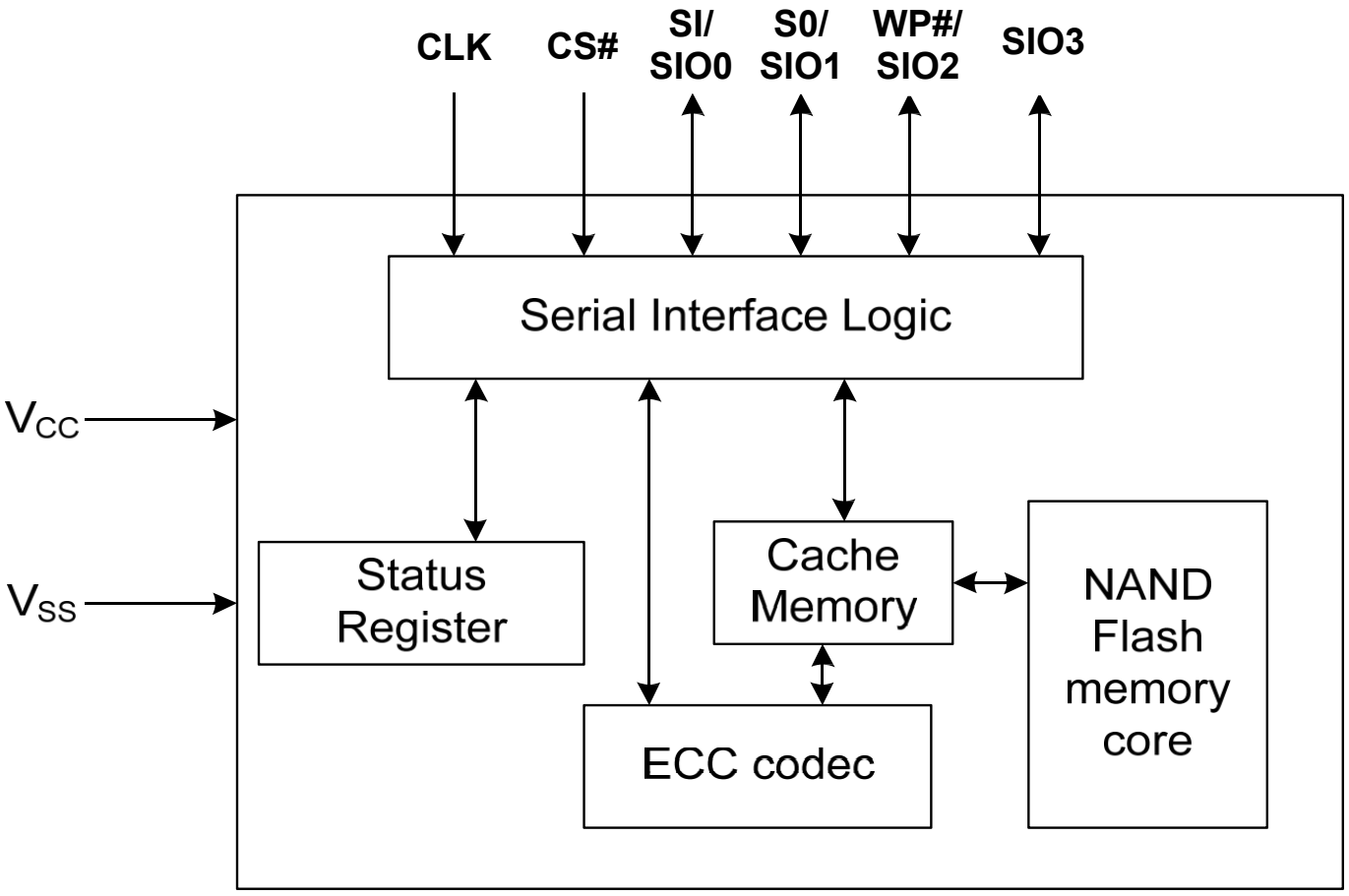
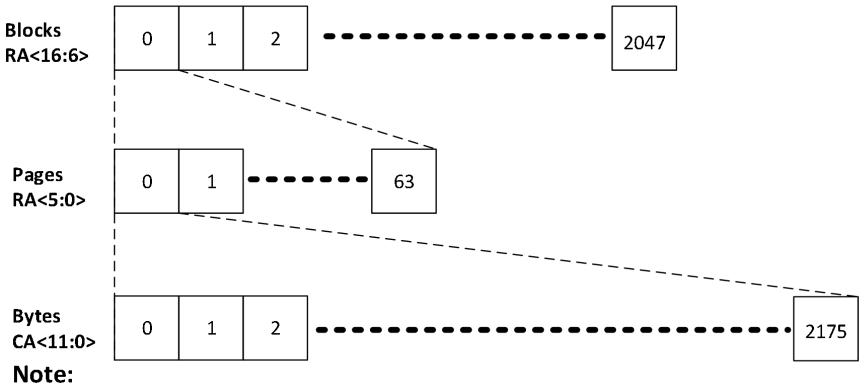


Figure3. Block Diagram

6. Memory Mapping



Note:

1.CA：Column Address. The 12-bit column address is capable of addressing from 0 to 4095 bytes; However, only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are “out of bounds”, do not exist in the device, and cannot be addressed.

2. RA：Row Address. RA<5:0> selects a page inside a block, and RA<16:6> selects a block.

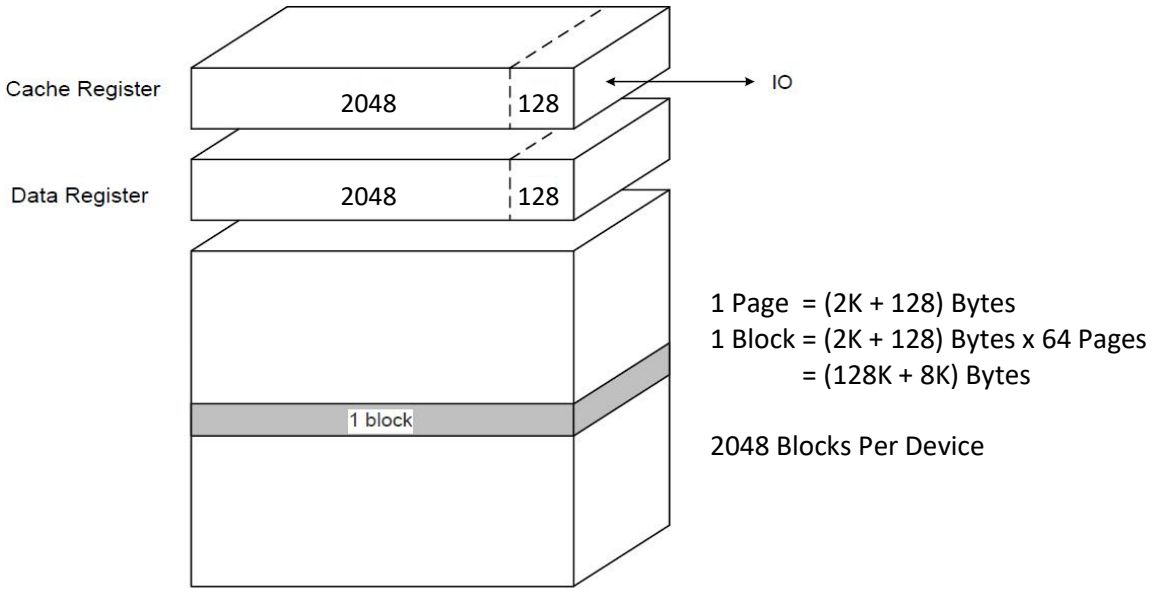
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7. Array Organization

Table1. Array Organization

Each device has	Each block has	Each page has	Unit
128M + 16M	128K + 8K	2K + 128	bytes
2048 x 64	64	-	Pages
2048	-	-	Blocks

Figure4. Array Organization



1 Page = (2K + 128) Bytes
1 Block = (2K + 128) Bytes x 64 Pages
= (128K + 8K) Bytes

2048 Blocks Per Device

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8. Device Operation

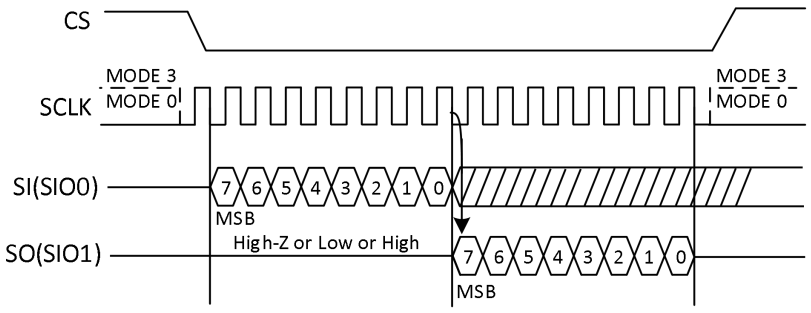
8.1 SPI Modes

8.1.1 Standard SPI

The device is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI instructions use the SI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The SO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

Figure5. SPI SDR Modes Supported



8.1.2 Dual SPI

The device supports Dual SPI operation when using the x2 and dual IO instructions. These instructions allow data to be transferred to or from the device at two times the rate of ordinary Serial Flash devices. When using Dual SPI instructions, the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

8.1.3 Quad SPI

The device supports Quad SPI operation when using the x4 and Quad IO instructions. These instructions allow data to be transferred to or from the device four times the rate of ordinary Serial Flash. When using Quad SPI instructions the SI and SO pins become bidirectional SIO0 and SIO1 and the WP# pin become SIO2 respectively. Quad SPI instructions require the Quad Enable bit (QE) to be set.

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8.2 Pin Description

8.2.1 CS#

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (SIO0, SIO1, SIO2, SIO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

8.2.2 CLK

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the CLK signal. Data output changes after the falling edge of CLK.

8.2.3 Serial Input (SI) / SIO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial CLK clock signal.

SI becomes SIO0 – an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

8.2.4 Serial Output (SO) / SIO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial CLK clock signal.

SO becomes SIO1 -an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial CLK clock Signal) as well as shifting out data (on the falling edge of CLK).

8.2.5 Write Protect (WP#) / SIO2

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

When WP# is driven Low (VIL), during a SET FEATURES command and while the BRWD bit of the Status Register is set to a 1, it is not possible to write to the Status Registers. This prevents any alteration of the Block Protect (BP2, BP1, BP0), INV and CMP bits of the Status Register. As a consequence, all the data bytes in the memory area that are protected by the Block Protect(BP2, BP1,BP0), INV and CMP bits, are also hardware

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protected against data modification if WP# is Low during a SET FEATURES command.

The WP# function is replaced by SIO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the CLK signal) as well as shifting out data (on the falling edge of CLK).

8.2.6 SIO3

For Standard and Dual SPI Command Sets ,keep SIO3 pin always high level. For Quad SPI Command Sets, keep SIO3 pin high level when SIO3 is not in input and output state.

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8.3 Command Set Tables

Table2. Standard SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
Write Enable	**06h**					
Write Disable	**04h**					
Get Features	**0Fh**	A7-A0	(D7-D0)	wrap	wrap	wrap
Set Features	**1Fh**	A7-A0	D7-D0			
Page Read	**13h**	A23-A16	A15-A8	A7-A0		
Read From Cache	**03h/0Bh**	A15-A8(1)	A7-A0	dummy	(D7-D0)	Byte N
Read ID	**9Fh**	00	(MID)(6)	(DID)(6)		
Read UID	**13h**	00	00	00		
Read Parameter Page	**13h**	00	00	01		
Program Load	**02h**	A15-A8(1)	A7-A0	D7-D0	Next byte	Byte N
Program Load Random Data(7)	**84h**	A15-A8(1)	A7-A0	D7-D0	Next byte	Byte N
Program Execute	**10h**	A23-A16	A15-A8	A7-A0		
Block Erase	**D8h**	A23-A16	A15-A8	A7-A0		
Reset	**FFh**					

Note:

Get Features (0FH), address = 0XC0, wrap function

Table3. Dual SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
Read From Cache x2	**3Bh**	A15-A8(1)	A7-A0	dummy	(D7-D0)x2	-
Read From Cache Dual IO	**BBh**	A15-A0(2)	dummy(3)	(D7-D0)x2	Next byte	-

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Table4. Quad SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
Read From Cache x4	**6Bh**	A15-A8[1]	A7-A0	dummy	(D7-D0)x4	Byte N
Read From Cache Quad IO	**EBh**	A15-A0[4]	(D7-D0)x4	Next byte	Next byte	Byte N
Program Load x4	**32h**	A15-A8[1]	A7-A0	(D7-D0) x4	Next byte	Byte N
Program Load Random x4[7]	**C4h/34h**	A15-A8[1]	A7-A0	(D7-D0) x4	Next byte	Byte N
Program Load Random Data Quad IO[7]	**72h**	A15-A0[5]	(D7-D0) x4	Next byte	Next byte	Byte N

Notes:

1. The x8 clock = dummy <3:0>, A11-A8
2. The x8 clock = dummy <3:0>, A11-A0
3. The x8 clock = dummy <7:0>, D7-D0
4. The x8 clock = dummy <3:0>, A11-A0,dummy<7:0>,D7-D0
5. The x8 clock = dummy <3:0>, A11-A0,D7-D0,D7-D0
6. MID is Manufacture ID, DID is Device ID
7. Only available in Internal Data Move operation

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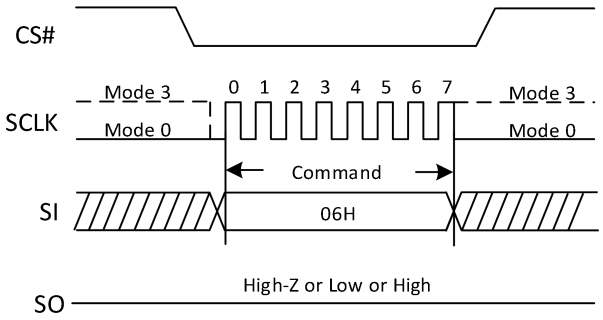
8.4 Write Operations

8.4.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page Program
- OTP Program
- OTP Protect
- Block Erase

Figure6. Write Enable Sequence Diagram



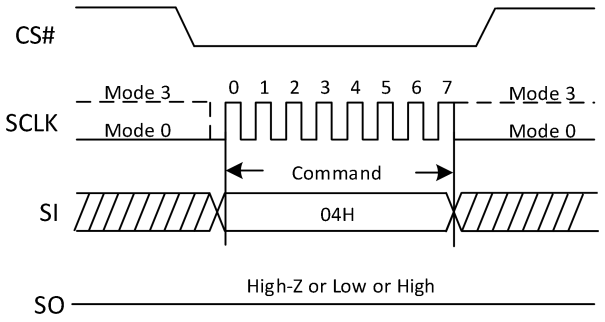
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8.4.2 Write Disable (WRDI) (04h)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is also reset by following condition:

- Page Program
- OTP Program
- OTP Protect
- Block Erase

Figure7. Write Disable Sequence Diagram



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8.5 Feature Operations

8.5.1 Get Features (0FH) and Set Features (1FH)

The Get Features (0Fh) and Set Features (1Fh) commands are used to monitor the device status and alter the device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific bits in feature address A0h and B0h (shown the following table). The status register is mostly read, except WEL, which is writable bit with the WREN (06h) command.

When a feature is set, it remains active until he deice is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a Reset (FFh) command is issued.

Table5. Features Settings

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block Lock	A0H	BRWD (R/W)	Reserved	BP2 (R/W)	BP1 (R/W)	BP0 (R/W)	INV (R/W)	CMP (R/W)	Reserved
Feature	B0H	OTP_PRT	OTP_EN (R/W)	Reserved	ECC_EN	CRM	Reserved	HSE (R/W)	QE (R/W)
Status	C0H	ECCS3 (R)	ECCS2 (R)	ECCS1 (R)	ECCS0 (R)	P_FAIL (R)	E_FAIL (R)	WEL (R)	OIP (R)
Drive Strength	D0H	Reserved	DS_IO[1] (R/W)	DS_IO[0] (R/W)	Reserved	Reserved	Reserved	Reserved	Reserved

Note:

1. If BRWD is enabled and WP# is low, then the block lock register (BP2-BP0, INV and CMP) cannot be changed.
2. If QE is enabled, the quad IO operations can be executed.
3. All the reserved bits must be held low when the feature is set.
4. The features in the feature byte B0H are all volatile except OTP_PRT bit.
5. Internal ECC is always on, when ECC_EN is disabled, the ECC status is default value (0000b: ECCS3/ECCS2/ ECCS1/ECCS0) and do not reflect the real ECC status
6. Continuous Read Mode bit, Default CRM=0, Normal read mode, If need Continuous Read function, please contact XTX.
7. (R/W): Read / Write, (R): Read only

DS_IO[1]	DS_IO[0]	I/O drive strength
0	0	25%
0	1	50% (Default)
1	0	75%
1	1	100%

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Figure8. Get Features Sequence Diagram

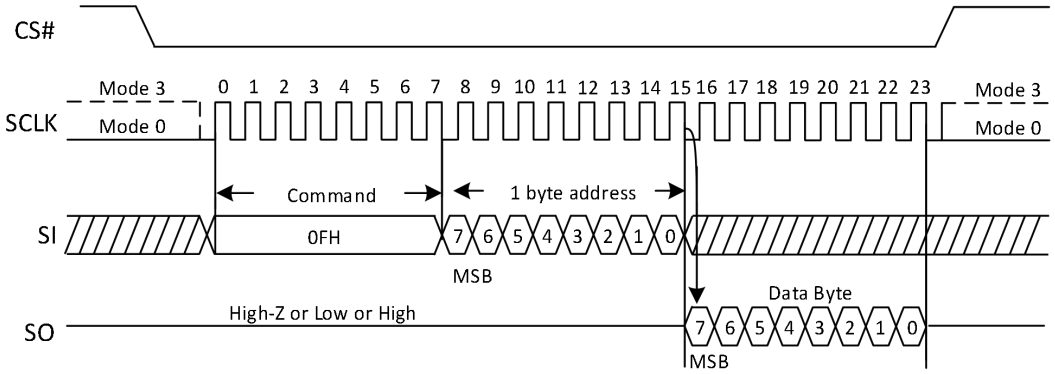
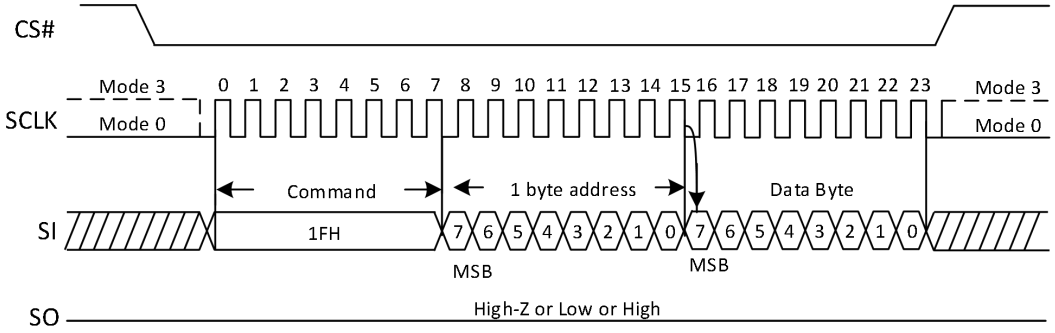


Figure9. Set Features Sequence Diagram



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8.6 Read Operations

8.6.1 Page Read

The Page Read (13h) command transfers the data from the NAND Flash array to the cache register. The command sequence is follows:

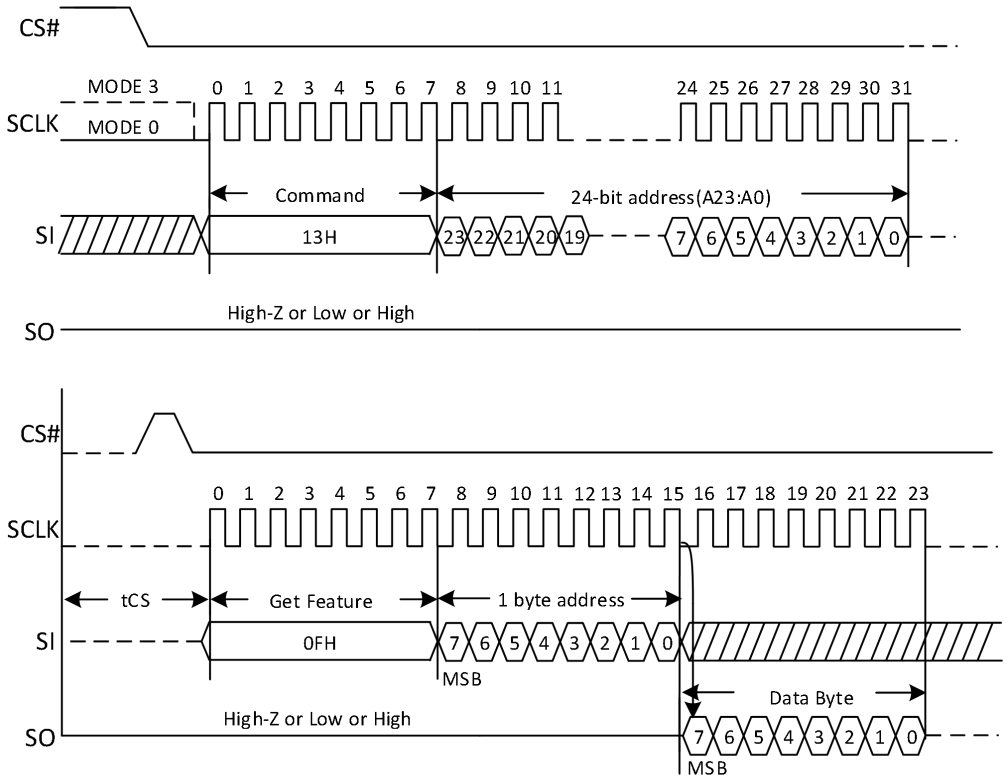
1. 13h (Page Read To Cache)
2. 0Fh (Get Features command to read the status)
   Monitor whether the status of the operation is finished
3. 0Bh or 03h (Read From Cache)
   Requires mode configure bits, followed by 12-bit column address for the starting byte address
   Other Operation：
   - 3Bh (Read From Cache x2)
   - 6Bh (Read From Cache x4)
   - BBh (Read From Cache Dual IO)
   - EBh (Read From Cache Quad IO)

The Page Read command requires a 24-bit address consisting of 8 dummy bits followed by a 16-bit block/page address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During this time, the Get Features (0Fh) command can be issued to monitor the status of the operation (refer to the Status Register section). Following a status of successful completion, the Read From Cache (03h/0Bh/3Bh/6Bh/BBh/EBh) command must be issued in order to read the data out of the cache.The device supports pre-read function. When reading multiple pages continuously, the average tRD is shortened.

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8.6.2 Page Read to Cache (13H)

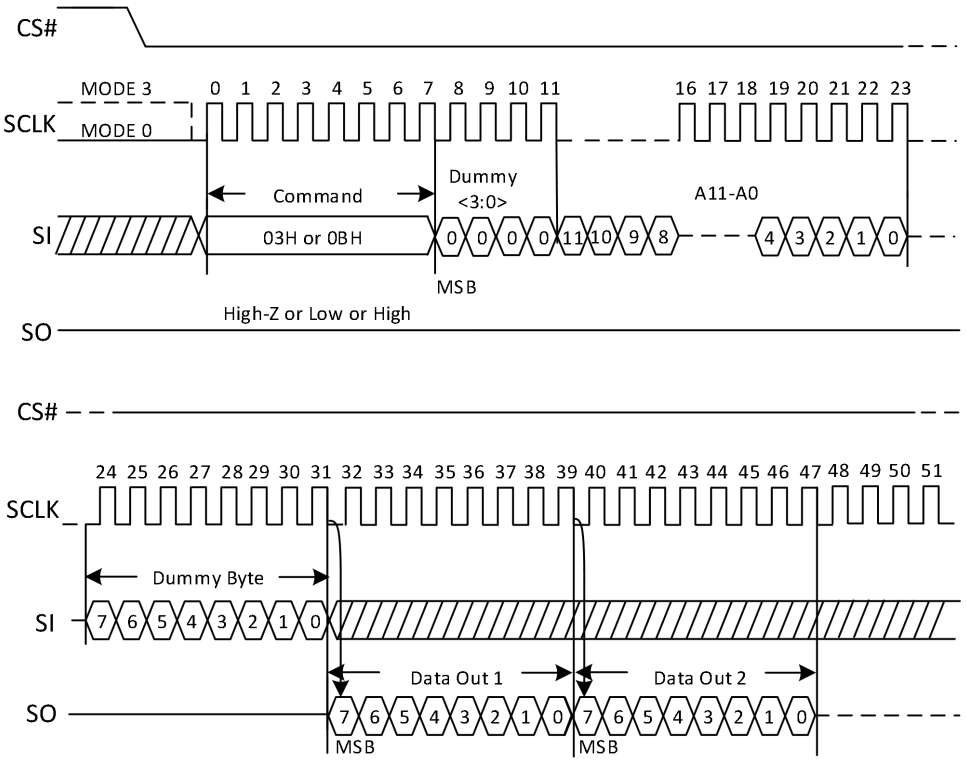
Figure10. Page Read to Cache Sequence Diagram



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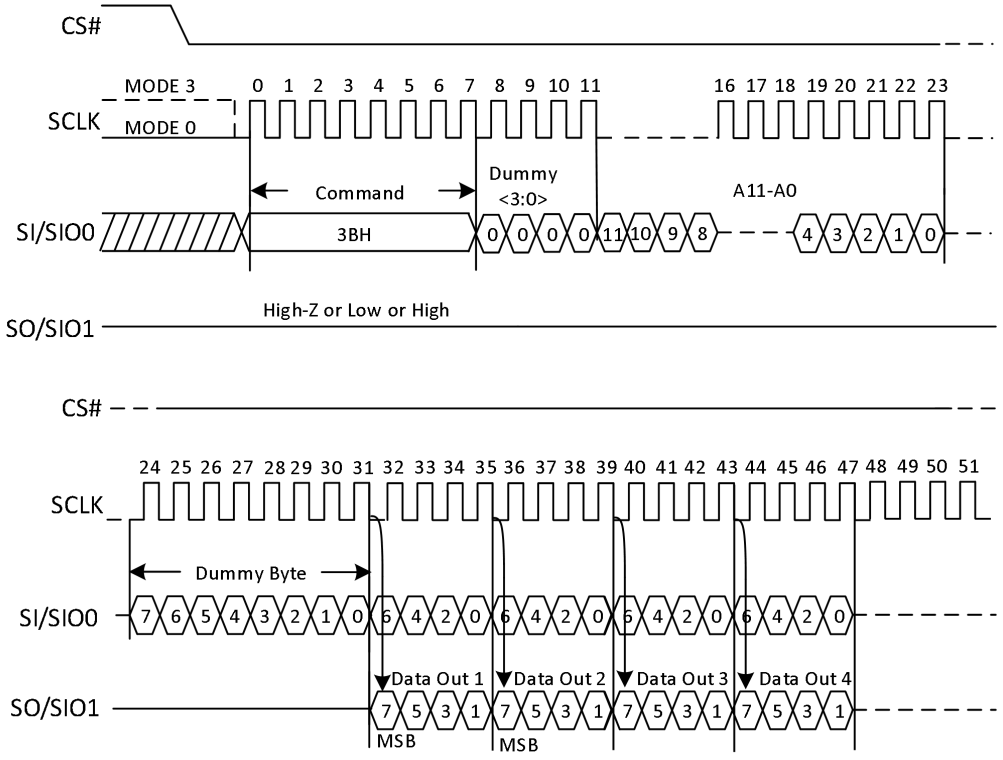
8.6.3 Read From Cache (03H or 0BH)

Figure11. Read From Cache Sequence Diagram



8.6.4 Read From Cache x2 (3BH)

Figure12. Read From Cache x2 Sequence Diagram

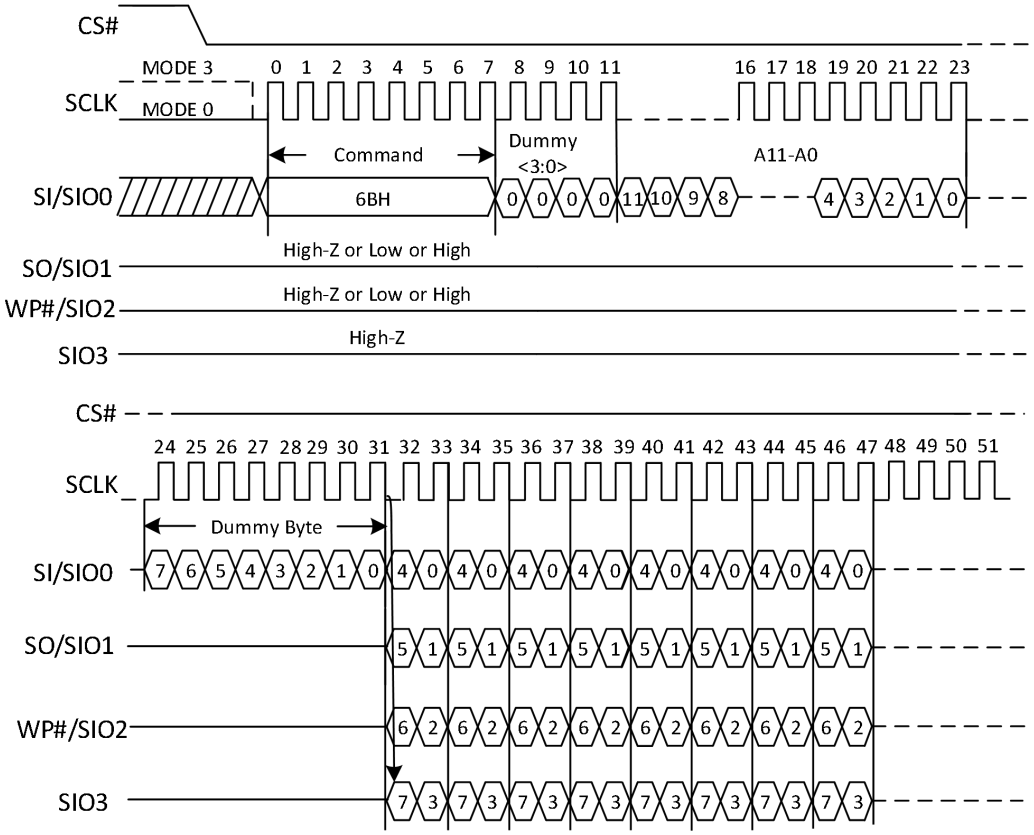


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8.6.5 Read From Cache x4 (6BH)

The Quad Enable bit (QE) of feature (B0 [0]) must be set to enable for the read from cache x4 command.

Figure13. Read From Cache x4 Sequence Diagram

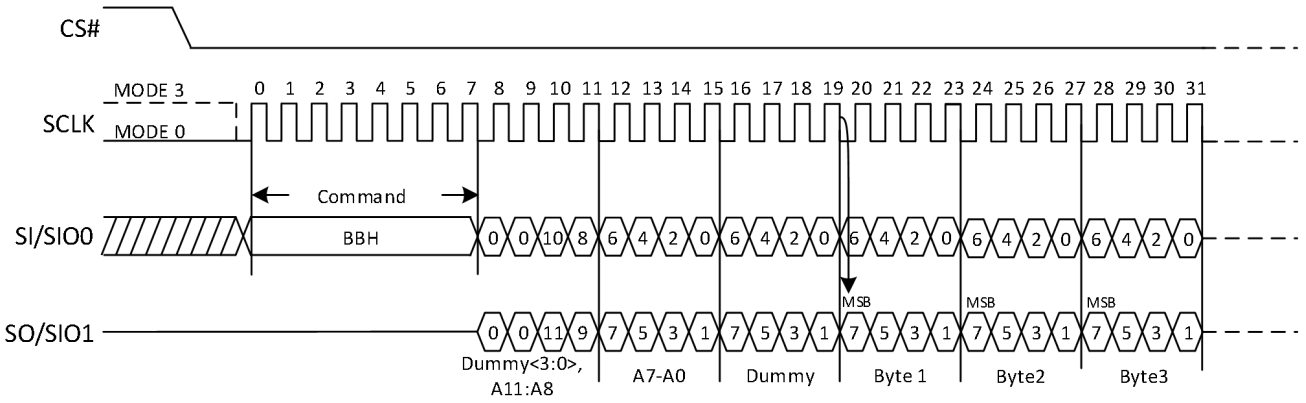


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8.6.6 Read From Cache Dual IO (BBH)

The Read from Cache Dual I/O command (BBH) is similar to the Read form Cache x2 command (3BH) but with the capability to input the 4 dummy bits, followed by a 12-bit column address for the starting byte address and a dummy byte by SIO0 and SIO1, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 2-bit per clock cycle from SIO0 and SIO1. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out until the boundary byte.

Figure14. Read From Cache Dual IO Sequence Diagram

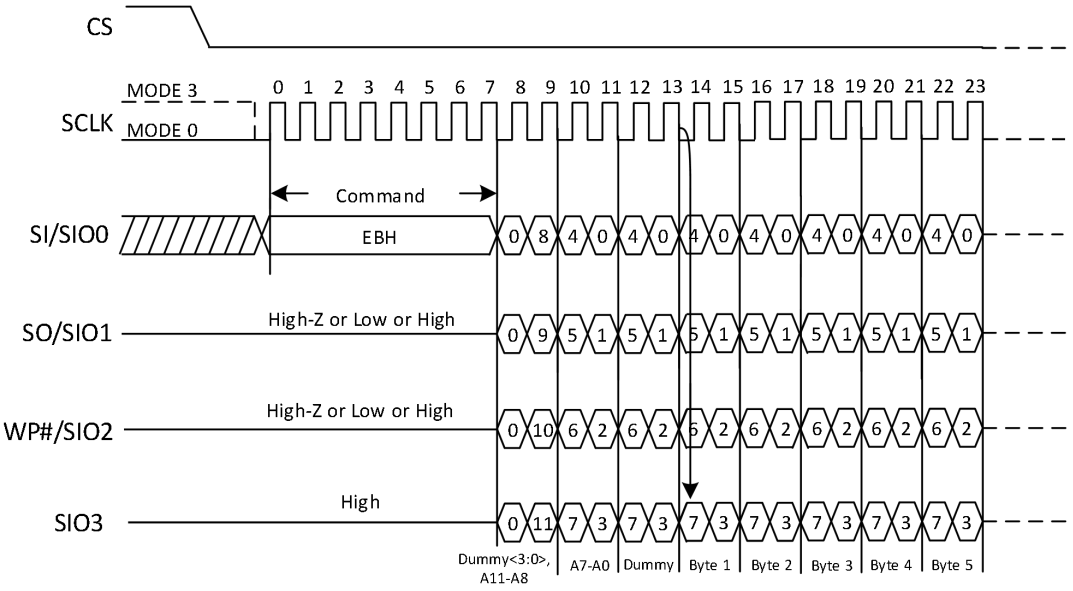


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8.6.7 Read From Cache Quad IO (EBH)

The Read from Cache Quad IO command is similar to the Read from Cache x4 command but with the capability to input the 4 dummy bits, followed a 12-bit column address for the starting byte address and a dummy byte by SIO0, SIO1, SIO2, SIO3, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 4-bit per clock cycle from SIO0, SIO1, SIO2, SIO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out until the boundary byte. The Quad Enable bit (QE) of feature (B0 [0]) must be set to enable for the read from cache quad IO command.

Figure15. Read From Cache Quad IO Sequence Diagram



8.6.8 Page Read Operation (High Speed Mode)

The device has a high speed mode for sequential read operation. When high speed mode is enabled, the average tRD is shortened. The command sequence is the same as the Page Read operation. The users set or clear the HSE bit which enables or disables the high speed mode in the feature table as shown in Table 5. High speed mode is enabled (HSE bit is set to 1) in the default condition. When the users switching the HSE bit, the users have to issue the Set Features command just before the Page Read (13h) command. When the users use the random page read, the recommended setting of the HSE bit is 0 (disable) since tRD becomes longer.

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8.6.9 Read ID (9FH)

The Read ID command is used to read the 2 bytes of identifier code programmed into the NAND Flash device. The Read ID command reads a 2-byte table (see below) that includes the Manufacturer ID and the Device ID.

Figure16. Read ID Sequence Diagram

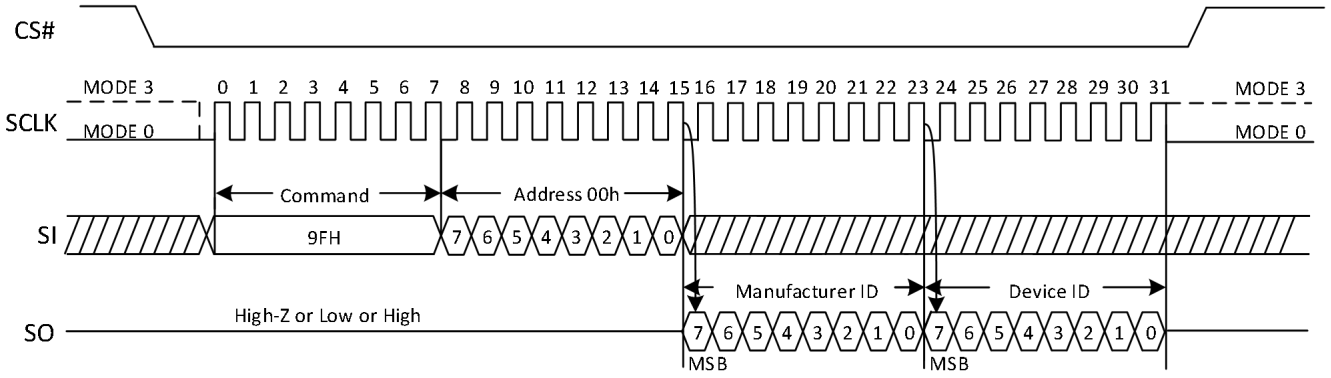


Table6. READ ID Table

Address	Value	Description
Byte 0	0BH	Manufacture ID (XTX)
Byte 1	32H	Device ID (SPI NAND 3.3V 2Gbit)

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8.6.10 Read UID

The Read Unique ID function is used to retrieve the 16 byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique. The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid. To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement are stored by the target. For example, reading bytes 32-63 returns to the host another copy of the UID and its complement.

Table7. READ UID Table

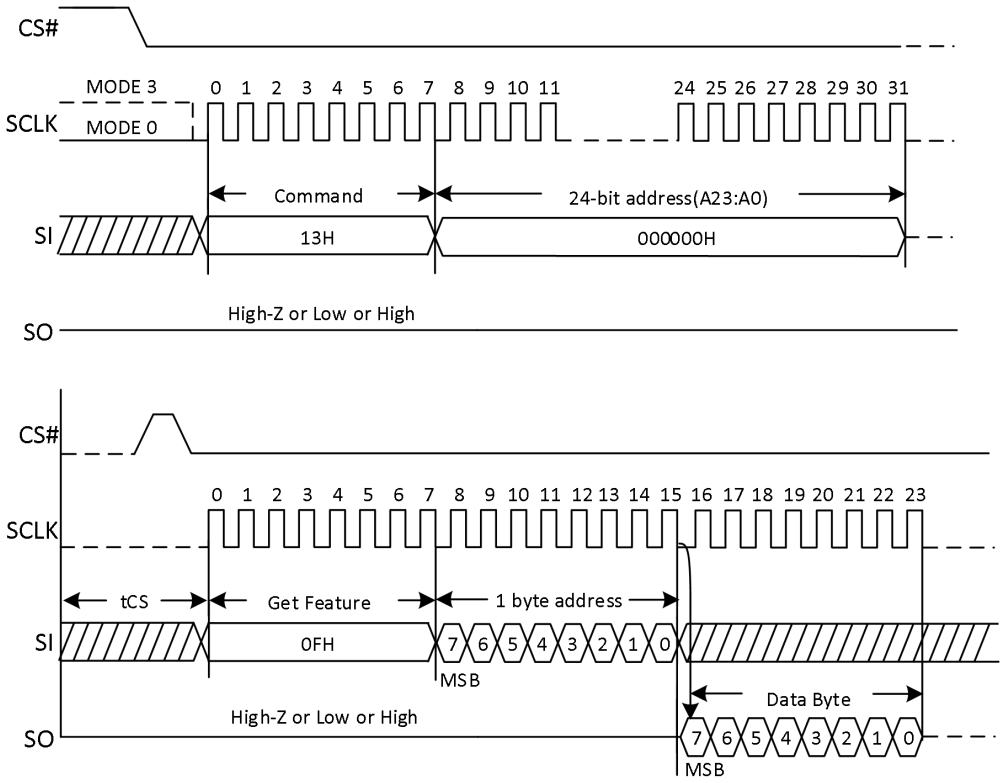
Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

The following command flow as follows:

1. Use Set Features command (1FH) to set B0 register, to enable OTP_EN.
2. Use Get Features command (0FH) to get data from B0 register and check if the OTP_EN is enable.
3. Use Page Read to cache (13H) command with address 24'h000000h, read data from array to cache.
4. Use 0FH (Get Features command) read the status.
5. User can use Read From Cache command (03H/0BH/3BH/BBH/6BH/EBH), read 16 bytes UID from cache.

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Figure17. Read UID to cache and Get Feature Command Sequence Diagram



8.6.11 Read Parameter Page

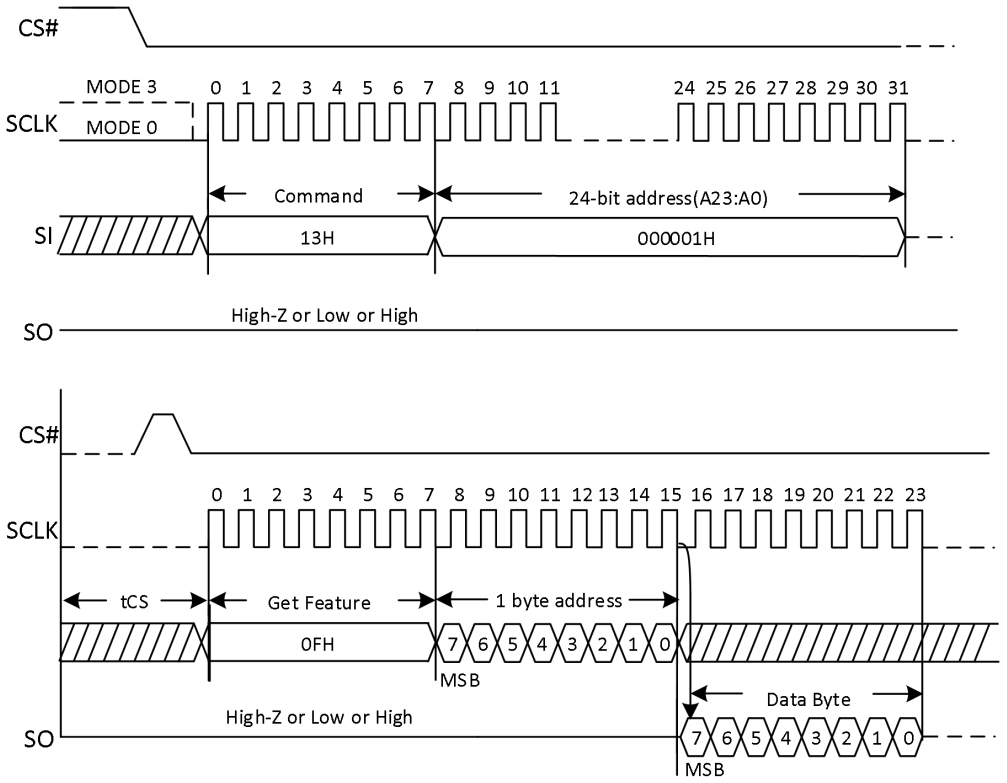
The following command flow must be issued by the memory controller to access the parameter page.

Sequence is as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use page read to cache (13h) command with address 24'h000001h, read data from array to cache.
4. Use 0FH (GET FEATURES command) read the status.
5. User can use Read from cache command (03H/0BH/3BH/6BH/BBH/EBH), read parameter page from cache.

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Figure18. Read Parameter Page to cache and Get Feature Command Sequence Diagram



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Parameter Page table as below:

Byte	Description		Value
0-3	Parameter page signature	ONFI	4Fh, 4Eh, 46h, 49h
4-5	Revision number		00h, 00h
6-7	Features supported		00h, 00h
8-9	Optional commands supported		00h, 00h
10-31	Reserved (0)		All 00h
32-43	Device manufacturer (12 ASCII characters)	XTX Tech	58h, 54h, 58h, 54h, 45h, 43h, 48h, 20h, 20h, 20h, 20h, 20h
44-63	Device model (20 ASCII characters)	XT26G02D	58h, 54h, 32h, 36h, 47h, 30h, 32h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	0Bh	0Bh
65-66	Date code		00h, 00h
67-79	Reserved (0)		All 00h
80-83	Number of data bytes per page	2048Byte	00h, 08h, 00h, 00h
84-85	Number of spare bytes per page	128Byte	80h, 00h
86-89	Number of data bytes per partial page	512Byte	00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page	32Byte	20h, 00h
92-95	Number of pages per block	64	40h, 00h, 00h, 00h
96-99	Number of blocks per logical unit (LUN)	2048	00h, 08h, 00h, 00h
100	Number of logical units (LUNs)	1	01h
101	Number of address cycles (N/A)		00h
102	Number of bits per cell	1	01h
103-104	Bad blocks maximum per LUN	40	28h, 00h
105-106	Block endurance	50K	05h, 04h
107	Guaranteed valid blocks at beginning of target		01h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of programs per page		04h
111	Partial programming attributes		00h
112	Number of bits ECC correctability	The number of bits that the host should be able to correct per code word	00h
113	Number of interleaved address bits		00h
114	Interleaved operation attributes		00h
115-127	Reserved (0)		All 00h
128	I/O pin capacitance		08h
129-130	Timing mode support		00h, 00h
131-132	Program cache timing mode support		00h, 00h
133-134	t_{PROG} Maximum page program time (µs)	700µs	BCh,02h
135-136	t_{ERS} Maximum block erase time (µs)	10ms	10h, 27h
137-138	t_{RD} Maximum page read time (µs)	185us	B9h, 00h

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139-163	Reserved (0)		All 00h
164-165	Vendor specific Revision number		00h, 00h
166-253	Vendor specific		All 00h
254-255	Integrity CRC		SET AT TEST (Note)
256-511	Value of bytes 0-255		Same as 0-255 Byte
512-767	Value of bytes 0-255		Same as 0-255 Byte
768+	Additional redundant parameter pages		FFh

Note:

1. The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. The CRC shall be calculated using the following 16-bit generator polynomial: $G(X) = X^{16} + X^{15} + X^2 + 1$

2. The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Device model	CRC Value (Byte 254/Byte 255)
XT26G02D	A3h/36h

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8.7 Program Operations

8.7.1 Page Program

The Page Program operation sequence programs 1 byte to 2176 bytes of data within a page. The page program sequence is as follows:

- 02H (Program Load)/32H (Program Load x4)
- 06H (Write Enable)
- 10H (Program Execute)
- 0FH (Get Features command to read the status)

The 1st step is to issue a Program Load (02H/32H) command. Program Load consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address, then the data bytes to be programmed. The data bytes are loaded into a cache register which is 2176 bytes long. If more than 2176 bytes are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH.

The 2nd step, prior to performing the Program Execute operation, is to issue a Write Enable (06H) command. As with any command that changes the memory contents, the Write Enable must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

The 3rd step is to issue a Program Execute (10h) command to initiate the transfer of data from the cache register to the main array. Program Execute consists of an 8-bit Op code, followed by a 24-bit address (8 dummy bits and a 16-bit page/block address). After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time.

During this busy time, the status register can be polled to monitor the status of the operation (refer to the Status Register section). When the operation completes successfully, the next series of data can be loaded with the Program Load command.

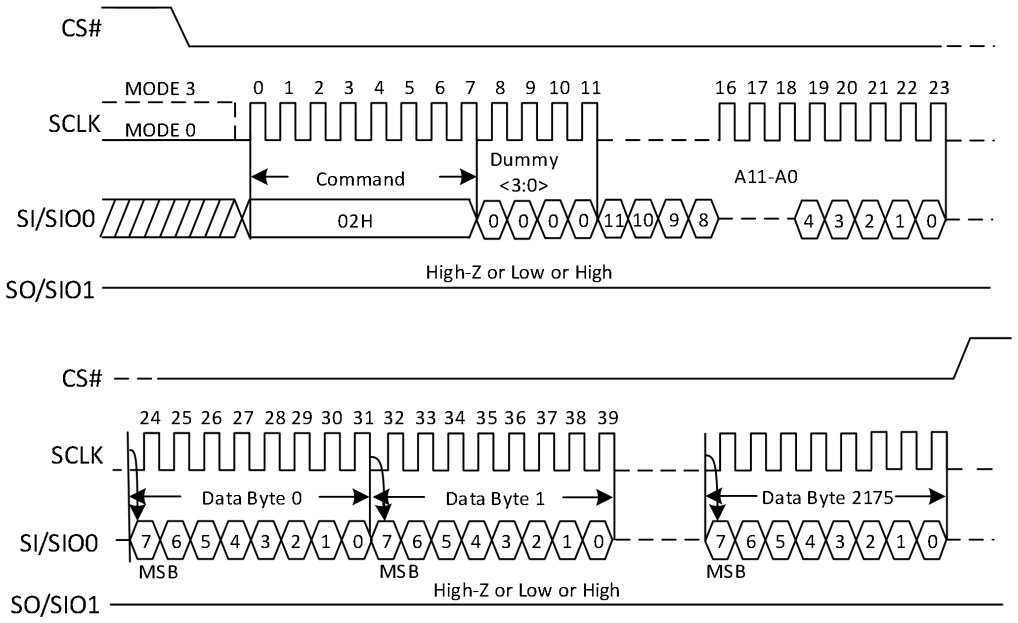
Note :

The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. In addition, pages must be sequentially programmed within a block.

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8.7.2 Program Load (PL)(02H)

Figure19. Program Load Sequence Diagram

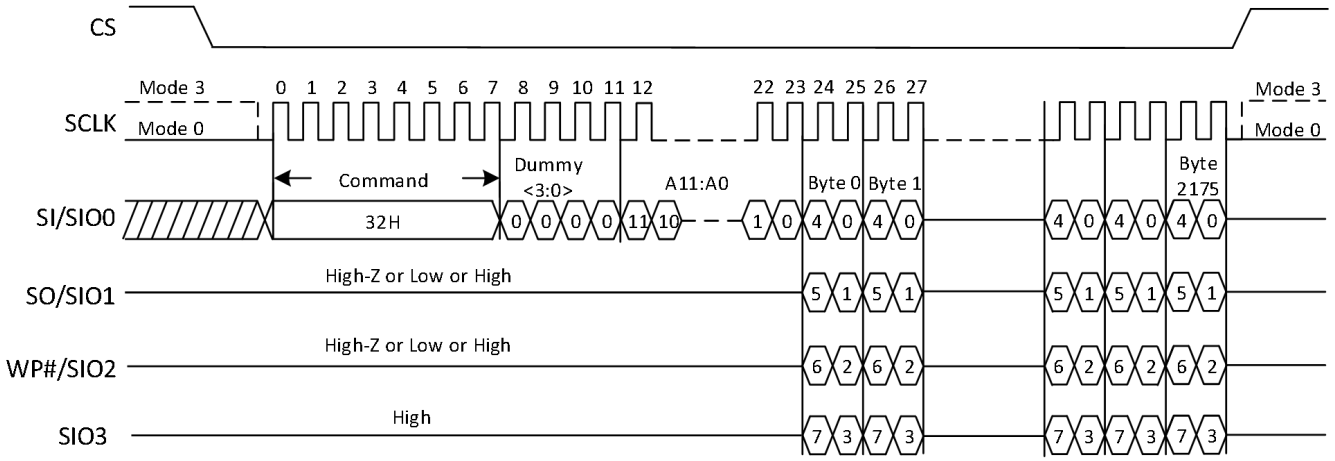


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8.7.3 Program Load x4 (PL x4) (32H)

The Program Load x4 command (32H) is similar to the Program Load command (02H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0 [0]) must be set to enable for the Program Load x4 command.

Figure20. Program Load x4 Sequence Diagram

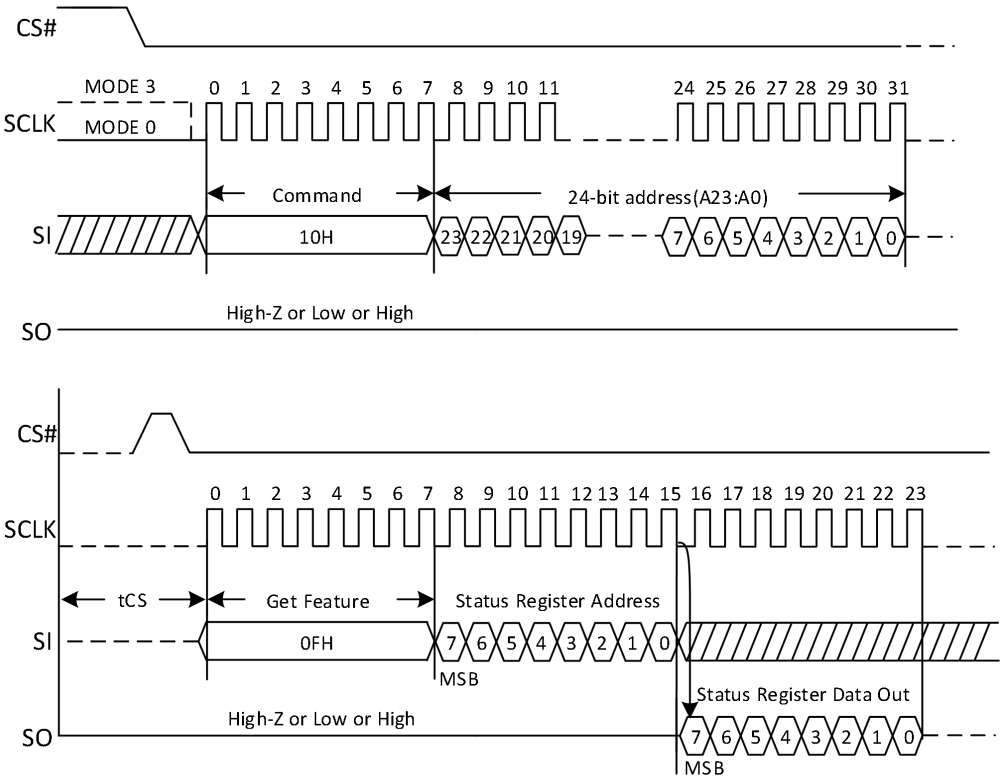


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8.7.4 Program Execute (PE) (10H)

After the data is loaded, a Program Execute (10H) command must be issued to initiate the transfer of data from the cache register to the main array. Program Execute consists of an 8-bit Op code, followed by a 24-bit address (8 dummy bits and a 16-bit page/block address). After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time. During this busy time, the status register can be polled to monitor the status of the operation (refer to Status Register). When the operation completes successfully, the next series of data can be loaded with the Program Load command.

Figure21. Program Execute Sequence Diagram



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8.7.5 Internal Data Move

The Internal Data Move command sequence programs or replaces data in a page with existing data. The Internal Data Move command sequence is as follows:

- 13H (Page Read to Cache)
- 84H/C4H/ 34H/72H (Program Load Random Data : Optional)
- 06H (Write Enable)
- 10H (Program Execute)
- 0FH (Get Features command to read the status)

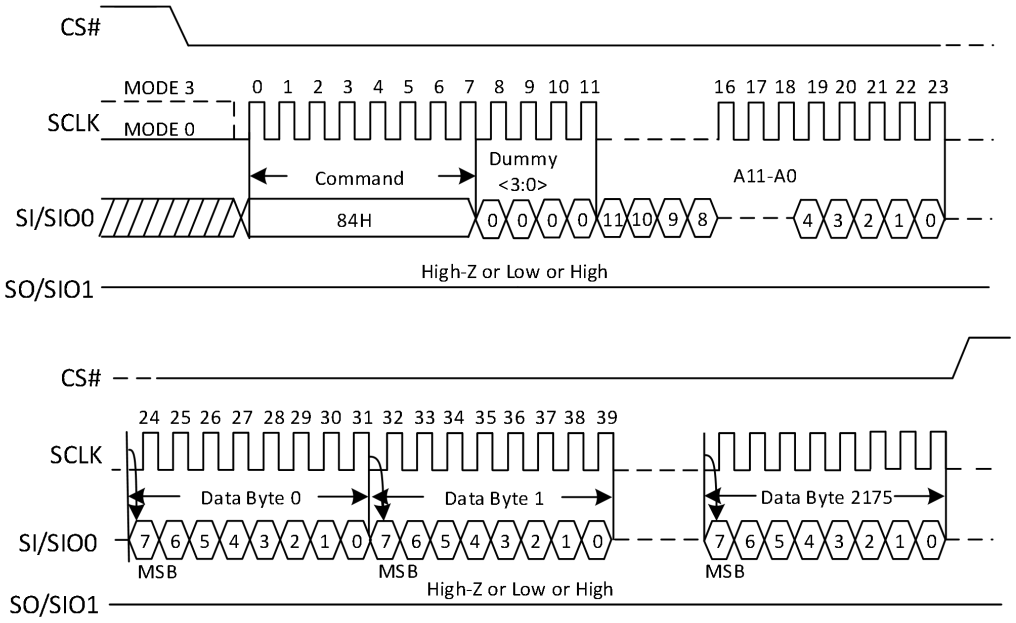
Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a Page Read (13H) command. The Program Load Random Data (84H/C4H/34H/72H) command can be issued, if user wants to update bytes of data in the page.

New data is loaded in the 12-bit column address. If the Random Data is not sequential, another Program Load Random Data (84H/C4H/34H/72H) command must be issued with the new column address. After the data is loaded, the Write Enable command must be issued, and then a Program Execute (10H) command can be issued to start the programming operation.

8.7.6 Program Load Random Data (84H)

This command consists of an 8-bit Op code, followed by 4 dummy bits, and a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another Program Load Random Data (84H) command must be issued with a new column address. After the data is loaded, a Program Execute (10H) command can be issued to start the programming operation.

Figure22. Program Load Random Data Sequence Diagram

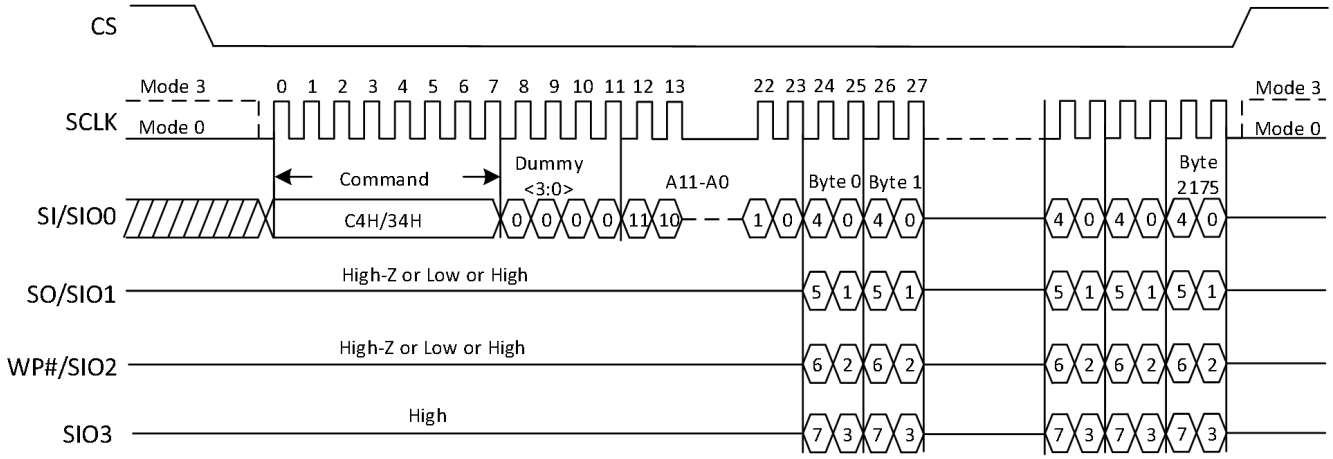


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8.7.7 Program Random Data x4 (C4H/34H)

The Program Load Random Data x4 command (C4H/34H) is similar to the Program Load Random Data command (84H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0 [0]) must be set to enable for the Program Load Random Data x4 command.

Figure23. Program Load Random Data x4 Sequence Diagram

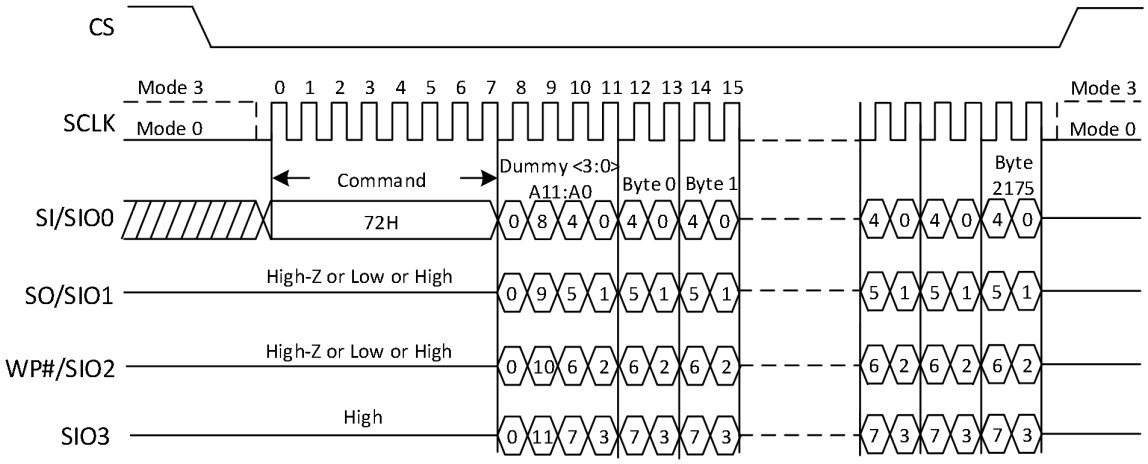


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8.7.8 Program Load Random Data Quad IO (72H)

The Program Load Random Data Quad IO command (72H) is similar to the Program Load Random Data x4 command (C4H/34H) but with the capability to input the 4 dummy bits, and a 12-bit column address by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0 [0]) must be set to enable for the Program Load Random Data Quad IO command.

Figure24. Program Load Random Data Quad IO Sequence Diagram



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8.8 Erase Operations

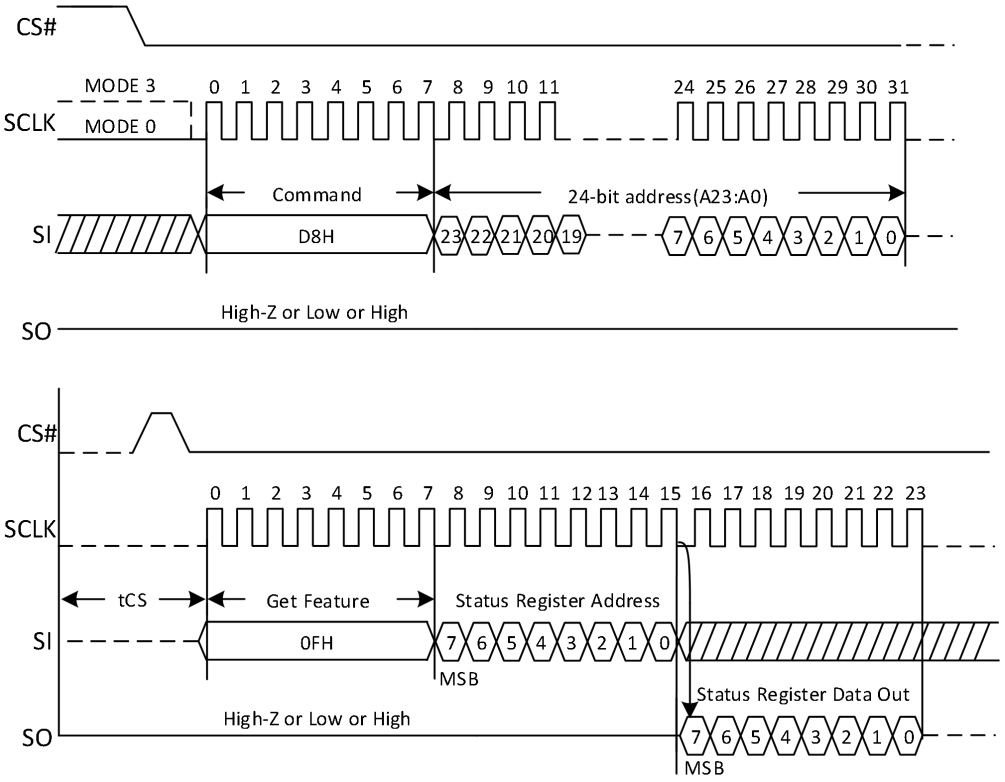
8.8.1 Block Erase (D8H)

The Block Erase (D8H) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2176 bytes per page (2048+128 bytes). Each block is 136Kbytes. The Block Erase command (D8H) operates on one block at a time. The command sequence for the Block Erase operation is as follows:

- 06h (Write Enable command)
- D8h (Block Erase command)
- 0Fh (Get Features command to read the status register)

Prior to performing the Block Erase operation, a Write Enable (06H) command must be issued. As with any command that changes the memory contents, the Write Enable command must be executed in order to set the WEL bit. If the Write Enable command is not issued, then the rest of the erase sequence is ignored. A Write Enable command must be followed by a Block Erase (D8H) command. This command requires a 24-bit address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tERS time during the Block Erase operation. The Get Features (0FH) command can be used to monitor the status of the operation (refer to the Status Register section).

Figure25. Block Erase Sequence Diagram



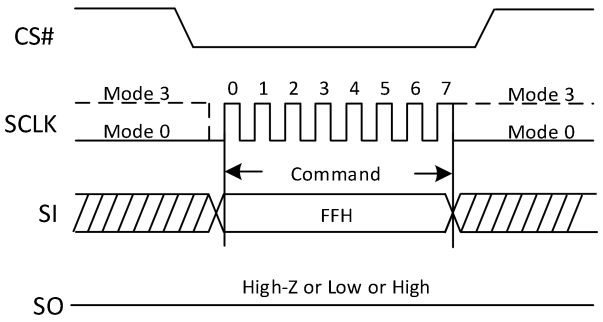
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8.9 Reset Operations

The Reset (FFH) command stops all operations. For example, in case of a program or erase or read operation, the reset command can make the device enter the wait state.

8.9.1 Reset (FFH)

Figure26. Reset (FFH) Sequence Diagram



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8.10 Write Protect

The write protection will be determined by the combination of CMP, INV, BP[2:0] bits in the Block Lock Register (A0).

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the Program and Erase operations. After power-up, the device is in the “locked” state, i.e., feature bits BP0, BP1and BP2are set to 1, INV, CMP and BRWD are set to 0. To unlock all the blocks, or a range of blocks, the Set Features command must be issued to alter the state of protection feature bits. When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set. Also, when a Program/Erase command is issued to a locked block, status bit OIP remains 0.When an Erase command is issued to a locked block, the erase failure, 04H is returned. When a Program command is issued to a locked block, program failure, 08H is returned.

Table8. Block Lock Register Block Protect Bits

CMP	INV	BP2	BP1	BP0	Protected Row Address	Protected Rows
x	x	0	0	0	None	None
0	0	0	0	1	1F800h ～1FFFFh	Upper 1/64
0	0	0	1	0	1F000h ～1FFFFh	Upper 1/32
0	0	0	1	1	1E000h ～1FFFFh	Upper 1/16
0	0	1	0	0	1C000h ～1FFFFh	Upper 1/8
0	0	1	0	1	18000h ～1FFFFh	Upper 1/4
0	0	1	1	0	10000h ～1FFFFh	Upper 1/2
x	x	1	1	1	All (default)	All (default)
0	1	0	0	1	00000h ～007FFh	Lower 1/64
0	1	0	1	0	00000h ～00FFFh	Lower 1/32
0	1	0	1	1	00000h ～01FFFh	Lower 1/16
0	1	1	0	0	00000h ～03FFFh	Lower 1/8
0	1	1	0	1	00000h ～07FFFh	Lower 1/4
0	1	1	1	0	00000h ～0FFFFh	Lower 1/2
1	0	0	0	1	00000h ～1F7FFh	Lower 63/64
1	0	0	1	0	00000h ～1EFFFh	Lower 31/32
1	0	0	1	1	00000h ～1DFFFh	Lower 15/16
1	0	1	0	0	00000h ～1BFFFh	Lower 7/8
1	0	1	0	1	00000h ～17FFFh	Lower 3/4
1	0	1	1	0	00000h ～0003Fh	Block0
1	1	0	0	1	00800h ～1FFFFh	Upper 63/64
1	1	0	1	0	01000h ～1FFFFh	Upper 31/32
1	1	0	1	1	02000h ～1FFFFh	Upper 15/16
1	1	1	0	0	04000h ～1FFFFh	Upper 7/8
1	1	1	0	1	08000h ～1FFFFh	Upper 3/4
1	1	1	1	0	00000h ～0003Fh	Block0

When WP# is not LOW, user can issue bellows commands to alter the protection states as want.

- Issue Set Features register write(1FH)
- Issue the feature bit address(A0H) and the feature bits combination as the table

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9. Status Register

The device has an 8-bit status register that software can read during the device operation for operation state query. The status register can be read by issuing the Get Features (0FH) command, followed by the feature address C0h (see Feature Operation). The Output Driver Register can be set and read by issuing the Set Features (1FH) and Get Features command followed by the feature address D0h (see Feature Operation).

Table9. Status Register Bit Description

Bit	Bit Name	Description
ECCS3,ECCS2, ECCS1,ECCS0	ECC Status	ECCS3/ECCS2/ECCS1/ECCS0 provides ECC Status as follows: XX00b= No bit errors were detected during the previous read algorithm. 0001b= Bit errors(≤4) were detected and corrected. 0101b= Bit errors(=5) were detected and corrected. 1001b= Bit errors(=6) were detected and corrected. 1101b= Bit errors(=7) were detected and corrected. XX10b= Bit errors greater than ECC capability (8 bits) and not corrected XX11b= Bit errors reach ECC capability (8 bits) and corrected Bit errors cannot be detected and corrected if their number exceeds the tolerance. Therefore, block data should be refreshed when ECC status is equal to XX11b. ECCS is set to 0000b either following a Reset, or at the beginning of the Read. It is then updated after the device completes a valid Read operation. After power-on Reset, ECC status is set to reflect the contents of block 0, page 0.
P_FAIL	Program Fail	This bit indicates that a program failure has occurred (P_FAIL set to 1). It will also be set if the user attempts to program an invalid address or a protected region, including the OTP area. This bit is cleared during the Program Execute command sequence or a Reset command (P_FAIL = 0).
E_FAIL	Erase Fail	This bit indicates that an erase failure has occurred (E_FAIL set to 1). It will also be set if the user attempts to erase a locked region. This bit is cleared (E_FAIL = 0) at the start of the Block Erase command sequence or the Reset command.
WEL	WRITE ENABLE Latch	This bit indicates the current status of the Write Enable Latch (WEL) and must be set (WEL=1), prior to issuing a Program Execute or Block Erase command. It is set by issuing the Write Enable command. WEL can also be disabled (WEL= 0), by issuing the Write Disable command.
OIP	Operation In Progress	This bit is set (OIP = 1) when a Program Execute, Page Read, Block Erase, or Reset command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.

ECCS1	ECCS0	ECCS3	ECCS2	Description
0	0	X	X	No bit errors were detected during the previous read algorithm.
0	1	0	0	Bit errors(≤4) were detected and corrected.
0	1	0	1	Bit errors(=5) were detected and corrected.
0	1	1	0	Bit errors(=6) were detected and corrected.
0	1	1	1	Bit errors(=7) were detected and corrected.
1	0	X	X	Bit errors greater than ECC capability (8 bits) and not corrected
1	1	X	X	Bit errors reach ECC capability (8 bits) and corrected

10. OTP Region

The device offers a protected, One-Time Programmable NAND Flash memory area. Four full pages (2176 bytes per page) are available on the device, and the entire range is guaranteed to be good. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0.

To access the OTP feature, the user must issue the Set Features command, followed by feature address B0h. When the OTP is ready for access, pages 02h–05h can be programmed in sequential order. The Program Load (02H) and Program Execute (10H) commands can be used to program the pages. Also, the Page Read (13H) command and Read From Cache (03H/0BH/3BH/6BH/BBH/EBH) commands can be used to read the OTP area. The data bits used in feature address B0h to enable OTP access are shown in the table below.

10.1 OTP Access

To access OTP, perform the following command sequence:

- Issue the Set Features command (1Fh)
- Set feature bit OTP_EN
- Issue the Page Program (if OTP_EN=1) or Page Read command

It is important to note that after bits 6 and 7 of the OTP register are set by the user, the OTP area becomes read-only and no further programming is supported. For OTP states, see the following table.

10.2 OTP Protect

- Issue the Set Features command (1FH)
- Set feature bit OTP_EN and OTP_PRT
- 06H (Write Enable)
- Issue the Program Execute (10H) command.

Table10.OTP States

OTP_PRT	OTP_EN	State
x	0	Normal Operation
0	1	Access OTP region
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue Program Execute (10H) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data.

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11. Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming the Bad Block Mark (00h) to the first spare area location in each bad block. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Table11.Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB)	2008
Total available blocks per die	2048
First spare area location	Byte 2048
Bad-block mark	Non FFh

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12. ECC Protection

The device offers data corruption protection by offering optional internal ECC. ECC is always on after device power up, so the default Read and Program commands operate with internal ECC in the “active” state.

During a Program operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a Read operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:

- Spare area definitions provided in the ECC Protection table below.
- ECC can protect according main and spare areas. WRITEs to the ECC area are ignored.

Table12.ECC Protection and Spare Area

Min Byte Address	Max Byte Address	ECC Protected	Number Of Bytes	Area	Description
000H	1FFH	Yes	512	Main 0	User data 0
200H	3FFH	Yes	512	Main 1	User data 1
400H	5FFH	Yes	512	Main 2	User data 2
600H	7FFH	Yes	512	Main 3	User data 3
800H	80FH	Yes	16	Spare 0	User meta data 0
810H	81FH	Yes	16	Spare 1	User meta data 1
820H	82FH	Yes	16	Spare 2	User meta data 2
830H	83FH	Yes	16	Spare 3	User meta data 3
840H	87FH	Yes	64	Spare area	Internal ECC parity data

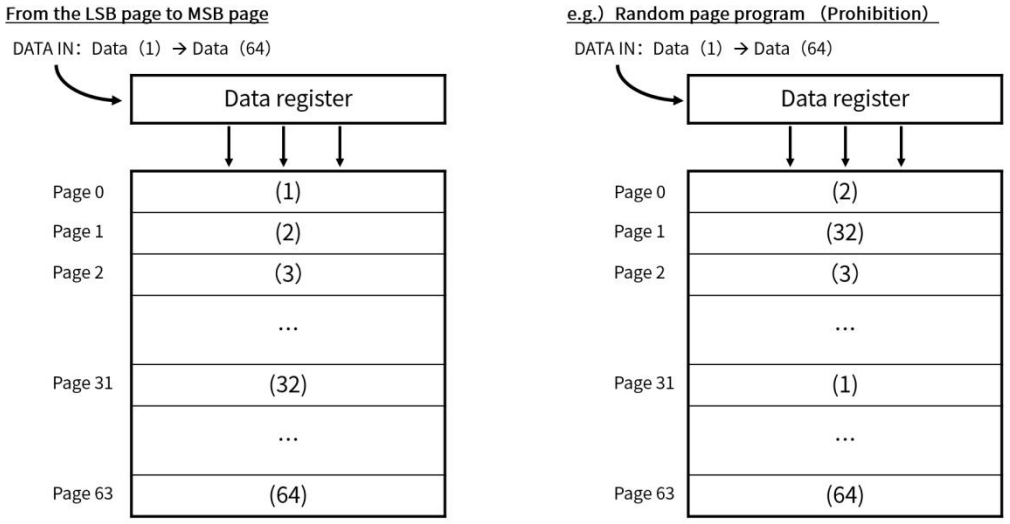
Note:
1. 800H is reserved for initial bad block mark.
2. The Internal ECC parity data (840H~87FH) is prohibited for user, but user can read the Address 840H~87FH.

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13. Application Notes And Comments

13.1 Addressing for program operation

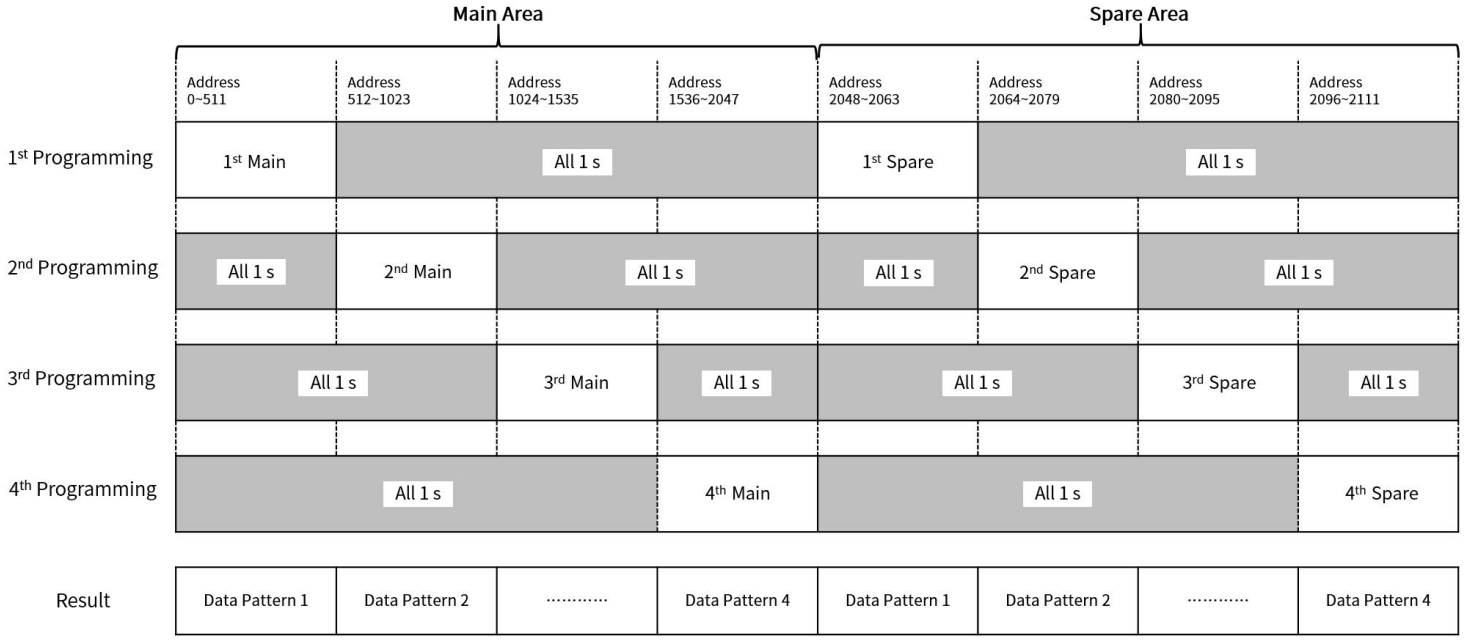
Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to the MSB (most significant bit) page of the block. Random page address programming is prohibited.



13.2 Several programming cycles on the same page (Partial Page Program)

ECC Parity Code is generated during Program operation on Main area (512 byte)+Spare area(16 byte). While using the Partial Page Program, the user must program the data to main field and spare field simultaneously by the definition of sector in section “ECC & Sector definition for ECC”.

For Example, each segment can be programmed individually as follows:



Number of partial program cycles in the same page must not exceed 4.

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13.3 Keep the power stable and sufficient

Do not turn off the power before the Write/Erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before the Write/Erase operation is complete will cause loss of data and/or damage to data.

13.4 Read Disturb

A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Operating Temperature		-40°C to +85°C
Storage Temperature		-65°C to +150°C
Voltage on I/O Pin with Respect to Ground		-0.3V to VCC+0.3V (<= 3.9V)
V_{CC}		-0.3V to 3.9V
Electrostatic Discharge Voltage	Human Body Model(1)	-4000V to +4000V
	Charge Device Model(2)	≥ 1000V

Note:

1. JS-001-2017 (R=1500 ohms, C=100pF).
2. JS-002-2018.

***NOTICE:**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

14.2 Latch-Up Characteristics

	Min.	Max.
Input Voltage with respect to GND on all power pins		1.5 VCCmax
Input Current on all non-power pins	-200mA	+200mA
Test conditions: VCC = VCCmax, one pin at a time (compliant to JEDEC JESD78 standard)		

14.3 Pin Capacitance

Applicable over recommended operating range from: T_A = 25°C, f = 1 MHz.

Symbol	Test Condition	Max.	Units	Conditions
C_{IN}	Input Capacitance	6	pF	VIN = 0V
C_{OUT} (1)	Output Capacitance	8	pF	VOUT = 0V

Note:

Characterized and is not 100% tested.

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14.4 Power-on and Power-off Timing

Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

Figure27. Power-On Timing

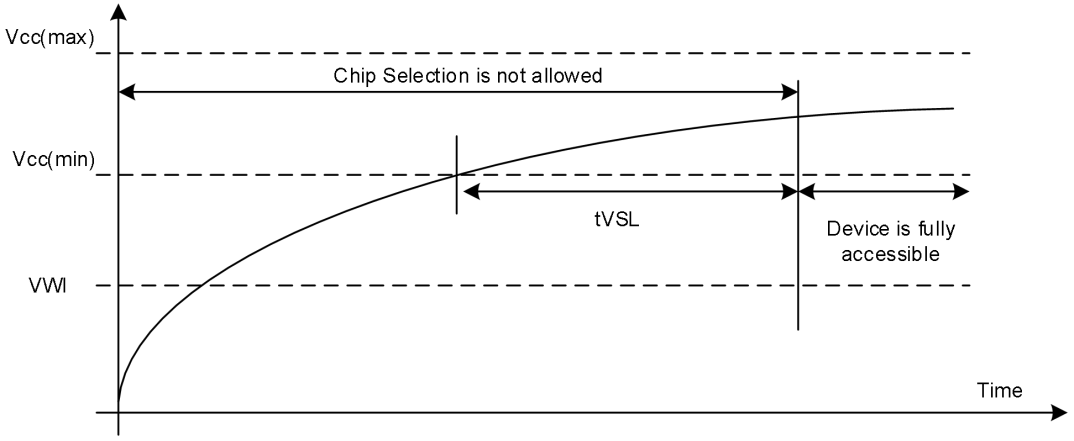


Table13.Power-On Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN.	MAX.	
VCC (min) to CS# Low	tVSL	3		ms
Write Inhibit Voltage	VWI		2.5	V

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14.5 DC Electrical Characteristics

Table14.DC Characteristics

Applicable over recommended operating range from: TA =-40°C to 85°C, VCC = 2.7V to 3.6V, (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN.	TYP.	MAX.	
VCC	Supply Voltage		2.7		3.6	V
ILI	Input Leakage Current Times				±2	µA
ILO	Output Leakage Current				±2	µA
ICC1	Standby Current	CS# = VCC, VIN = VSS or VCC		15	150	µA
ICC2	Read Current	CLK=0.1VCC/0.9VCC fCLK=120MHz		20	40	mA
	Program Current			25	40	mA
	Erase Current			25	40	mA
VIL (1)	Input Low Voltage		-0.3		0.2VCC	V
VIH (1)	Input High Voltage		0.8VCC		VCC+0.3	V
VOL	Output Low Voltage	IOL = 1.6mA			0.4	V
VOH	Output High Voltage	IOH = -100 µA	VCC-0.2			V

Note：

VIL min and VIH max are reference only and are not tested.

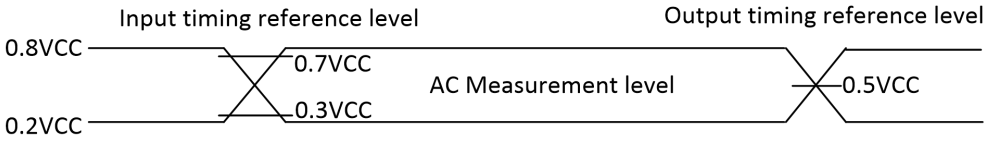
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14.6 AC Measurement Conditions

Table15.AC Measurement Conditions

SYMBOL	PARAMETER	SPEC		UNIT
		MIN.	MAX.	
CL	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2 V_{CC} to 0.8 V_{CC}		V
IN	Input Timing Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}		V
OUT	Output Timing Reference Voltages	0.5V_{CC}		V

Figure28. AC Measurement I/O Waveform



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14.7 AC Electrical Characteristics

Table16.AC Characteristics

Applicable over recommended operating range from: TA = -40°C to 85°C, VCC = 2.7V to 3.6V

SYMBOL	PARAMETER	SPEC			UNIT
		MIN.	TYP.	MAX.	
fC	Serial Clock Frequency for: all command			120	MHz
tCH(1)	Serial Clock High Time	3.75			ns
tCL(1)	Serial Clock Low Time	3.75			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
tSLCH	CS# Active Setup Time	7.5			ns
tCHSH	CS# Active Hold Time	2.5			ns
tSHCH	CS# Not Active Setup Time	2.5			ns
tCHSL	CS# Not Active Hold Time	2.5			ns
tSHSL/tCS	CS# High Time	100			ns
tSHQZ	Output Disable Time			10	ns
tCLQX	Output Hold Time(CL=30pF)	2			ns
tCLQV	Clock Low to Output Valid(CL=30pF)			6	ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	1.75			ns
tWHSL	WP# Setup Time before CS# Low	20			ns
tSHWL	WP# Hold Time after CS# High	100			ns

Note:

1. tCH + tCL >= 1 / fC ; characterized and not 100% tested.
2. Maximum Serial Clock Frequencies are measured results picked at the falling edge.

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Table17.Performance Timing

SYMBOL	PARAMETER	SPEC			UNIT
		MIN.	TYP.	MAX.	
tRST	CS# High to Next Command After Reset(FFh) from Idle/Program/Read			50	µs
tRST	CS# High to Next Command After Reset(FFh) from Erase			550	µs
tRD	Page Read From Array (with ECC) (High speed Mode Disable)		130	185	µs
tRHSA4	Average Read Time for Sequential Read (with ECC) (High Speed Mode Enable, Read buffer x 4)		35		
tPROG	Page Program		360	700	µs
tERS	Block Erase		3.5	10	ms

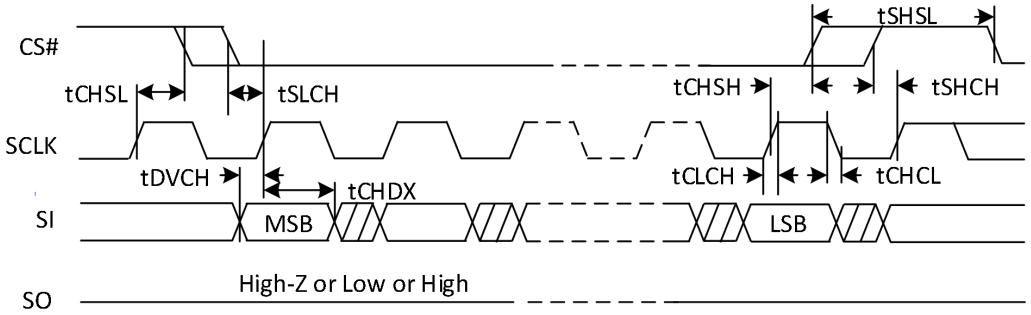
Note:

1. tRD is the average busy time for Page Read operation of 64 page continuously in a block.
2. tRHSA4 is the average busy time for sequential Page Read operation with all data output in each page of 64 pages continuously in a block at 100MHz.

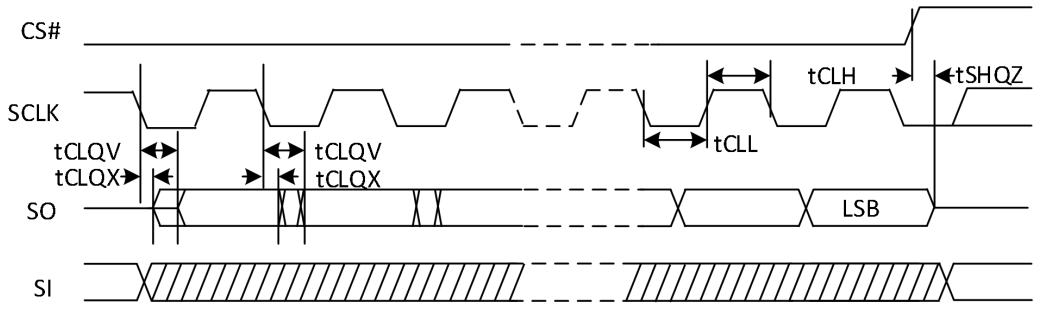
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15. SPI Serial Timing

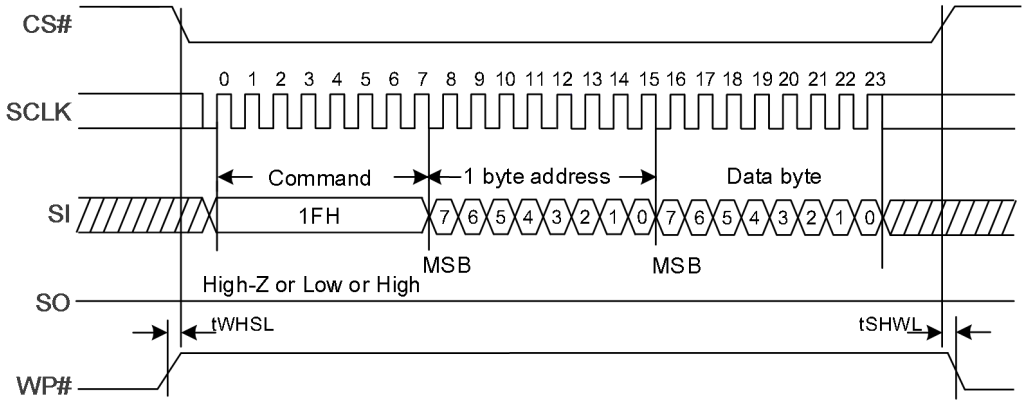
Serial Input Timing



Output Timing

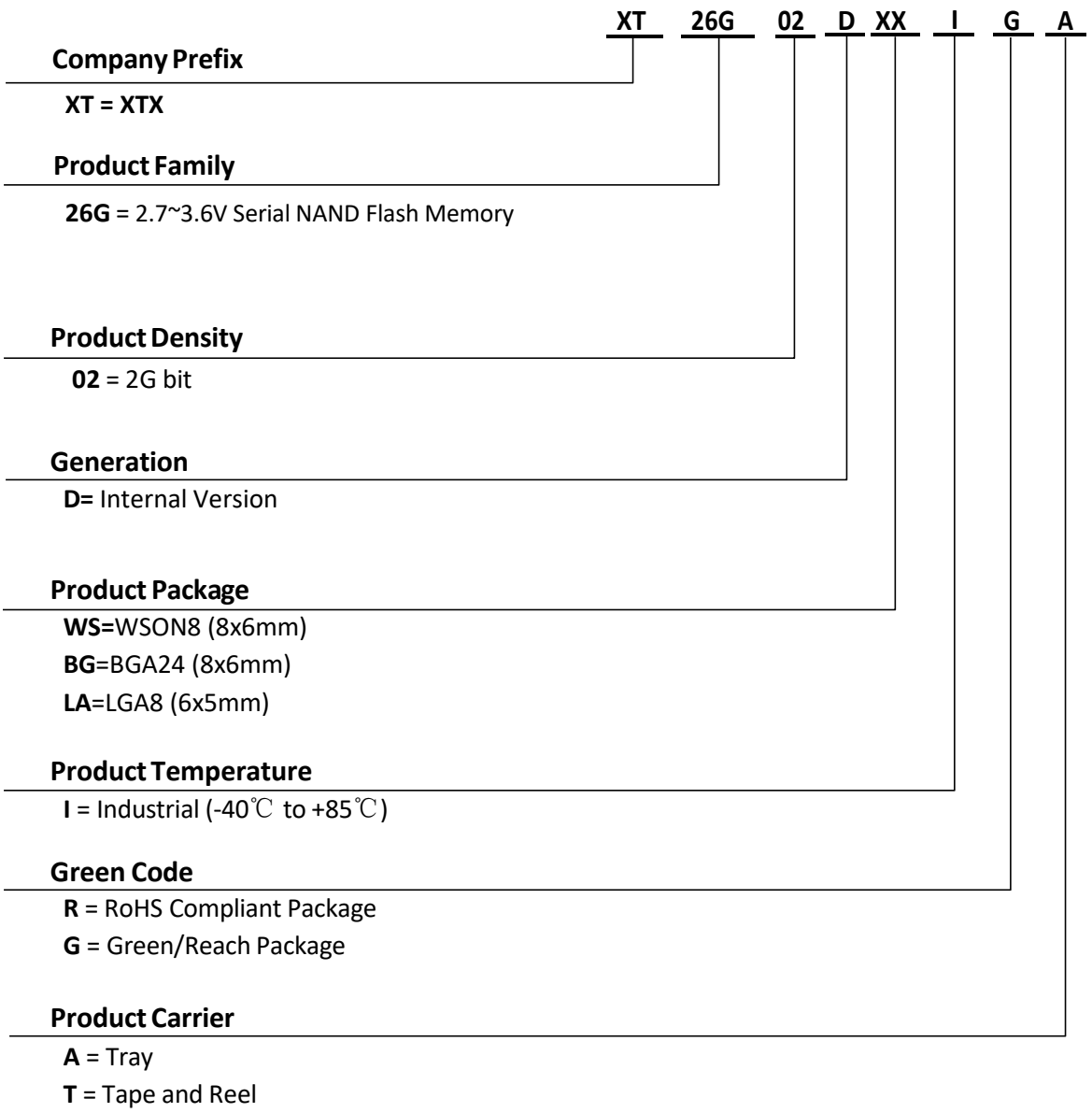


WP Timing



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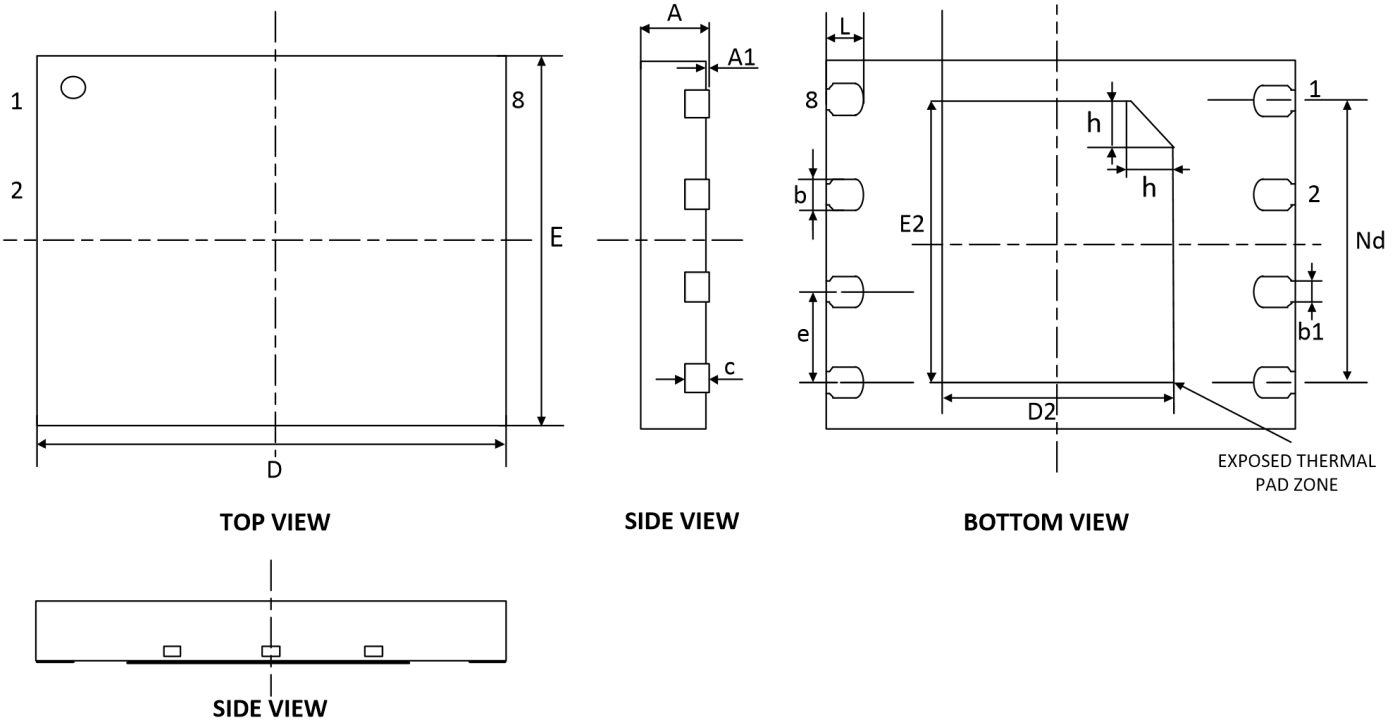
16. Ordering Information



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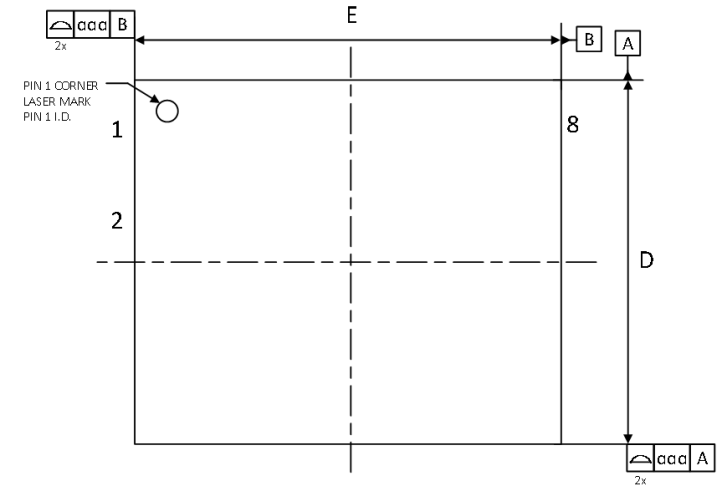
17. Package Information

17.1 8-Pad WSON8 (8x6mm)

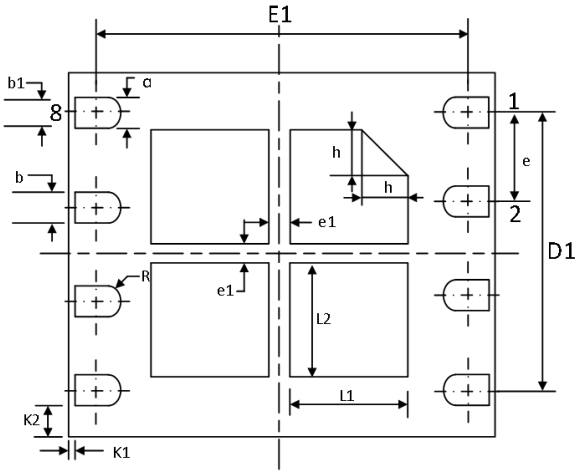


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
b1		0.25REF	
c	0.18	0.20	0.25
D	7.90	8.00	8.10
Nd		3.81BSC	
e		1.27BSC	
E	5.90	6.00	6.10
D2	3.30	3.40	3.50
E2	4.20	4.30	4.40
L	0.45	0.50	0.55
h	0.30	0.35	0.40

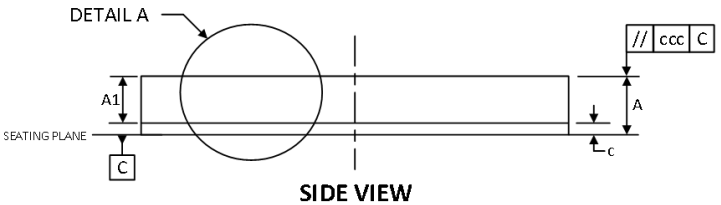
17.2 8-Pad LGA8 (6x5mm)



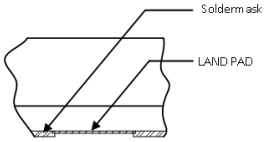
TOP VIEW



BOTTOM VIEW



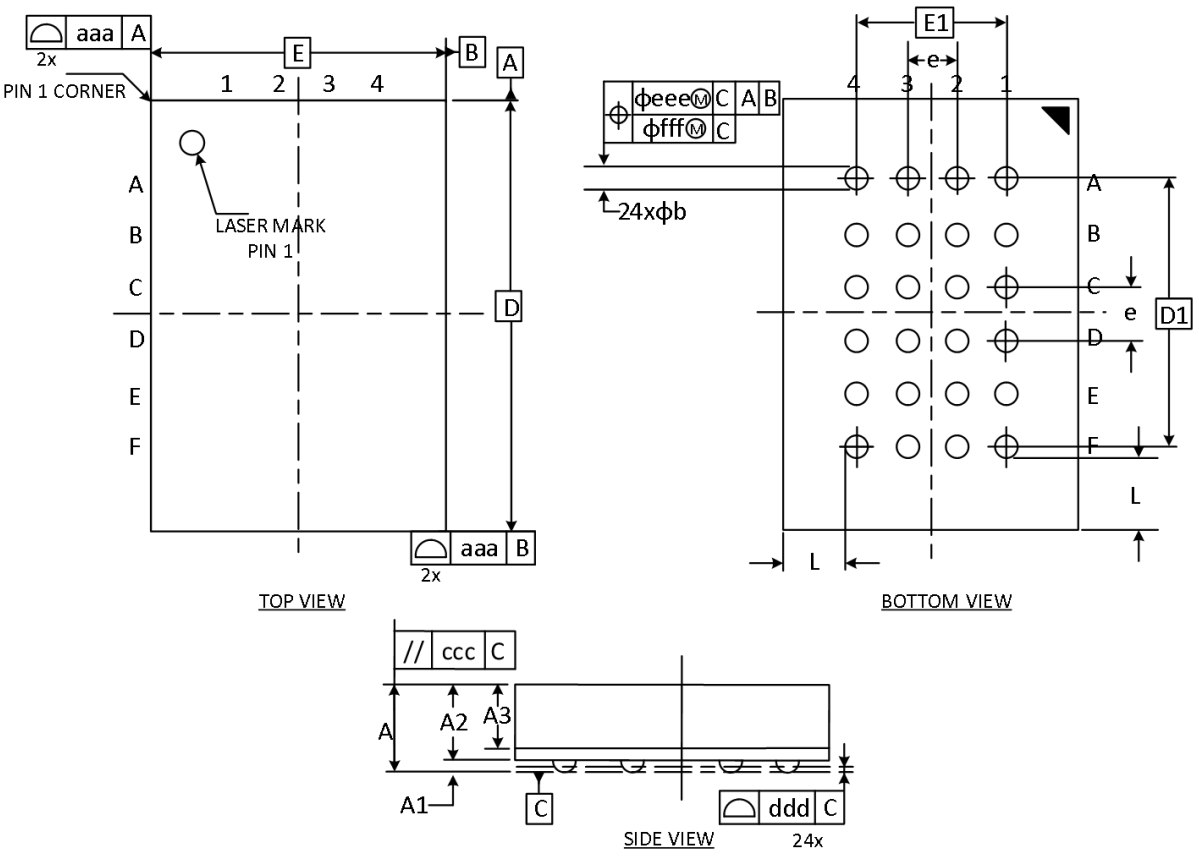
SIDE VIEW



DETAIL A

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1		0.53 BASIC	
c	0.19	0.22	0.25
D	4.90	5.00	5.10
D1		3.81 BASIC	
E	5.90	6.00	6.10
E1		5.40 BASIC	
e		1.27 BASIC	
e1		0.40 BASIC	
a	0.55	0.60	0.65
b	0.35	0.40	0.45
b1		0.25 REF	
L1	1.30	1.80	2.30
L2	1.00	1.50	2.00
h	0.30	0.35	0.40
K1		0.100 REF	
K2		0.395 REF	
aaa		0.10	
ccc		0.20	

17.3 BGA24 (8x6mm) (6x4 Ball Array)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.98	1.06	1.14
A1	0.25	0.30	0.35
A2	0.71	0.76	0.81
A3		0.53 BASIC	
c	0.20	0.23	0.26
D	7.90	8.00	8.10
D1		5.00 BASIC	
E	5.90	6.00	6.10
E1		3.00 BASIC	
e		1.00 BASIC	
b	0.35	0.40	0.45
L		1.30 REF	
aaa		0.10	
ccc		0.15	
ddd		0.10	
eee		0.15	
fff		0.10	

18. Revision History

Version No.	Description	Date
0.0	Initial Release.	Jun-20-2019
0.1	Correct the unclear description.	Nov-30-2019
0.2	Add the note of Table 15 Performance Timing.	Mar-27-2020
0.3	Modify template.	May-04-2023
0.4	Update Power-on and Power-off Timing. Add MSL level description and ESD/Latch UP results. Adjust the typical of Erase Current from 18mA to 28mA.	May-31-2023
0.5	Add BGA24 Package.	Jul-07-2023
0.6	Adjust the value of tCH and tCL from 3ns to 3.75ns Add ESD-CDM Add description of SIO3, and describe SIO pin level state in the waveform Add Order Part No.	Sep-14-2023
0.7	Add Package of LGA8(6x5mm)	Nov-07-2023
1.0	Add Endurance. Add Read Disturb. Adjust the typical value of ICC2(read current) from 26mA to 20mA. Adjust the typical value of ICC2(program current) from 28mA to 25mA. Adjust the typical value of ICC2(erase current) from 28mA to 25mA. Adjust the typical value of tERS from 4ms to 3.5ms.	Dec-03-2023

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