XT25F04D

Dual I/O Serial NOR Flash

Datasheet

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Serial NOR Flash Memory

4M bits 3.3V Dual I/O Serial Flash Memory with 4KB Uniform Sector

- **4M -bit Serial Flash**
  - 512 K-byte
  - 256 bytes per programmable page
- **Standard, Dual SPI**
  - Standard SPI: SCLK, CS#, SI, SO
  - Dual SPI: SCLK, CS#, IO0, IO1
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32k-byte
  - Block of 64k-byte
- **Software Write Protection**
  - Write protect all/portion of memory via software
- **Advanced security Features**
  - 2*256-Byte Security Registers With OTP Lock
- **Package Options**
  - See 1.1 Available Ordering OPN
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- **Temperature Range & Moisture Sensitivity Level**
  - Industrial Level Temperature. (-40°C to +85°C), MSL3
- **Power Consumption**
  - 20mA maximum active current
  - 13μA typical standby current
- **Single Power Supply Voltage**
  - 2.7~3.6V
- **Support SFDP and 128 bits Unique ID**
- **Minimum 100,000 Program/Erase Cycle**
- **High Speed Clock Frequency**
  - 120MHz for fast read with 30pF load
  - Dual I/O Data transfer up to 208Mbit/s
- **Program/Erase Speed**
  - Page Program time: 0.9ms typical
  - Sector Erase time: 55ms typical
  - Block Erase time: 0.3s/ 0.45s typical
  - Chip Erase time: 2.5s typical

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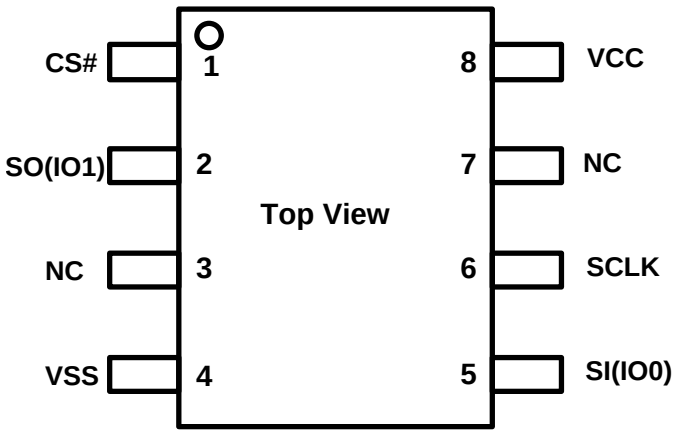
1. GENERAL DESCRIPTION

The XT25F04D Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO). The Dual I/O data is transferred at a speed of 208Mbit/s.

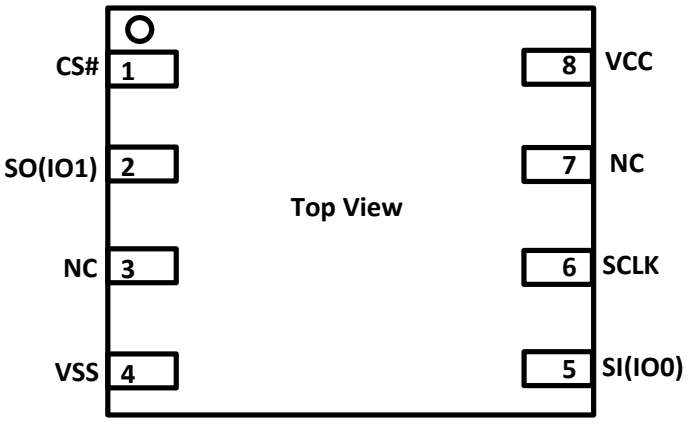
1.1. Available Ordering OPN

OPN	Package Type	Package Carrier
XT25F04DSOIGU	SO8 150mil	Tube
XT25F04DSOIGT	SO8 150mil	Tape & Reel
XT25F04DSOIGA	SO8 150mil	Tray
XT25F04DDTIGT	DFN8 2x3x0.4 mm	Tape & Reel

1.2. Connection Diagram



8-PIN SOP



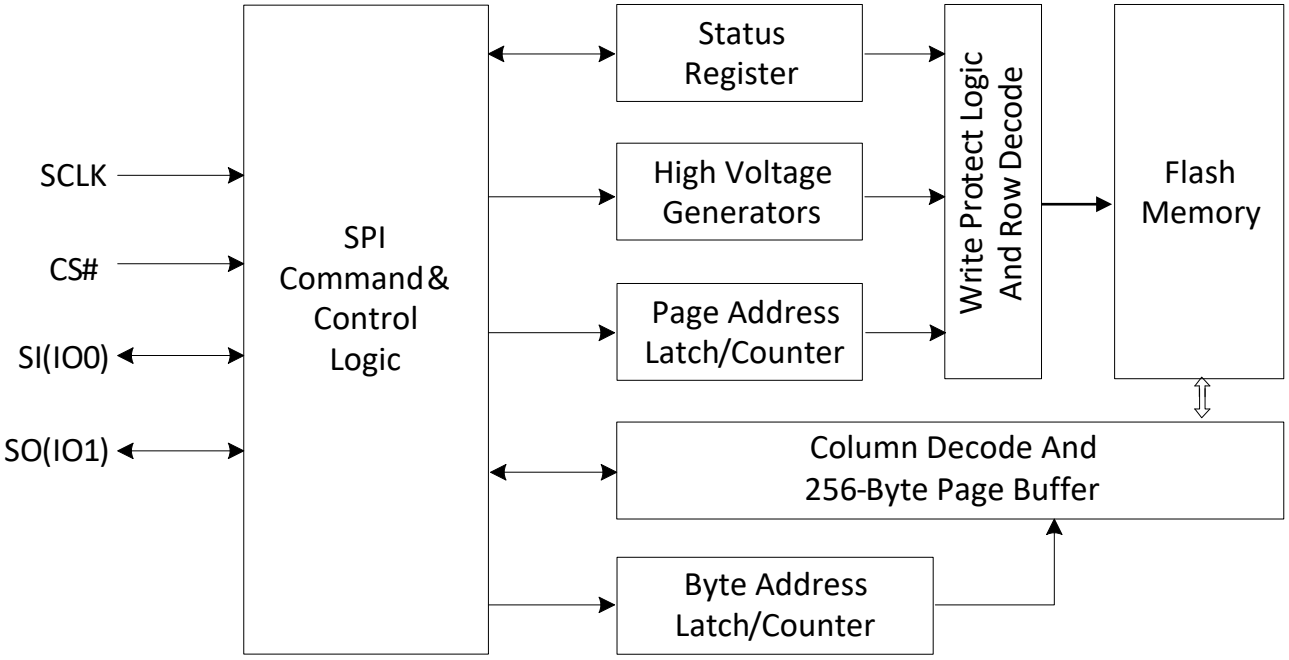
8-PIN DFN

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1.3. Pin Description

Pin Name	I/O	Description
CS#	I	Chip Select Input
SO (IO1)	I/O	Data Output (Data Input Output 1)
VSS		Ground
SI (IO0)	I/O	Data Input (Data Input Output 0)
SCLK	I	Serial Clock Input
VCC		Power Supply
NC		No Connection

1.4. Block Diagram



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2. MEMORY ORGANIZATION

XT25F04D Memory Description

Each Device has	Each Block has	Each Sector has	Each Page has	
512K	32K/64K	4K	256	bytes
2K	128/256	16	-	pages
128	8/16	-	-	sectors
16/8	-	-	-	blocks

XT25F04D 64K Bytes Block Sector Architecture

Block	Sector	Address Range	
7	127	07F000H	07FFFFH
	……	……	……
	112	070000H	070FFFH
6	111	06F000H	06FFFFH
	……	……	……
	96	060000H	060FFFH
……	……	……	……
	……	……	……
	……	……	……
……	……	……	……
	……	……	……
	……	……	……
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

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3. DEVICE OPERATION

Standard SPI

The XT25F04D features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The XT25F04D supports Dual SPI operation when using the "Dual Output Fast Read" and "Dual I/O Fast Read" (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4. STATUS REGISTER

S7	S6	S5	S4	S3	S2	S1	S0
Reserved*	LB	Reserved	BP2	BP1	BP0	WEL	WIP

*Please contact XTX sales or FAE if SRWD bit is needed.

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

LB bit.

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register (S6) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 using the Write Register instruction. LB is One Time Programmable, once it's set to 1, the Security Registers will become read-only permanently.

BP2, BP1, BP0 bits.

The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. Chip Erase command will be ignored if one or more of the Block Protect (BP2, BP1, BP0) bits are 1.

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Table1. the protected memory area of set BP2, BP1, BP0 bits

Status Register Content			Memory Content			
BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	0	0	None	None	None	None
0	0	1	Sector 0 to 125	000000H-07DFFFH	504KB	Lower 126/128
0	1	0	Sector 0 to 123	000000H-07BFFFH	496KB	Lower 124/128
0	1	1	Sector 0 to 119	000000H-077FFFH	480KB	Lower 120/128
1	0	0	Sector 0 to 111	000000H-06FFFFH	448KB	Lower 112/128
1	0	1	Sector 0 to 95	000000H-05FFFFH	384KB	Lower 96/128
1	1	0	Sector 0 to 63	000000H-03FFFFH	256KB	Lower 64/128
1	1	1	All	000000H-07FFFFH	512KB	All

SRWD bit.

The Status Register Write Disable (SRWD) bit is a non-volatile One Time Program(OTP) bit in the status register that provide another software protection. Once it is set to 1, the Write Status Register (WRSR) instruction is not accepted and the Block Protect bits (BP2, BP1, BP0) are read only.

SRWD	Status register
0	Status register can be written in (WEL bit is set to "1") and the SRWD, BP2-BP0 bits can be changed
1	The BP2-BP0 of status register bits cannot be changed

Note: The SRWD bit is reserved by default, please contact XTX sales or FAE if needed.

5. DATA PROTECTION

The XT25F04D provides the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
  - Erase Security Register / Program Security Register
- Software Protection Mode:
  - SRWD=0, the Block Protect (BP2, BP1, BP0) bits define the section of the memory array that can be read and change
  - SRWD=1, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP2, BP1, BP0) are read only.

Note: The Software Protection Mode is reserved by default, please contact XTX sales or FAE if needed.

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6. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table 2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable or Write Disable command, CS# must be driven high exactly at the byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 2. Commands

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	n-Bytes
Write Enable	06H						
Write Enable for Volatile Status Register	50H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Write Status Register	01H	(S7-S0)					
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(continuous)
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)			(continuous)
Continuous read reset	FFH						
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32KB)	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64KB)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Read Manufacturer/Device ID	90H	A23-A16	A15-A8	A7-A0	(MID7-MID0)	(DID7-DID0)	(continuous)
Read Identification	9FH	(MID7-MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)
Read Unique ID	4BH	00H	00H	00H	00H	(D7-D0)	
Read SFDP	5AH						
Erase Security Register	44H	A23-A16	A15-A8	A7-A0			
Program Security Register	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Read Security Register	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	
High Speed Mode	A3H	dummy	dummy	dummy			
Enable Reset	66H						
Reset	99H						

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NOTE:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0

   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

3. Security Registers Address:

   Security Register 0: A23-A16=00H, A15-A8=00H, A7-A0= Byte Address;

   Security Register 1: A23-A16=00H, A15-A8=01H, A7-A0= Byte Address;

Table of ID Device Definitions:

XT25F04D

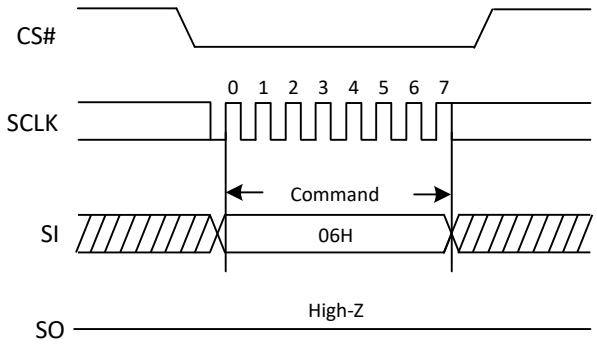
Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	0B	40	13
90H	0B		12
ABH			12

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6.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Program Security Register, Erase Security Register and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low→sending the Write Enable command→CS# goes high.

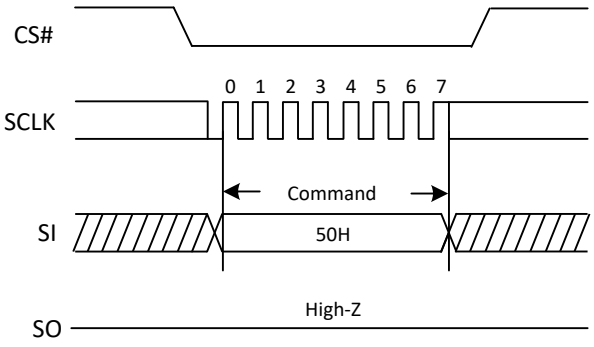
Figure1. Write Enable Sequence Diagram



6.2. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure2. Write Enable for Volatile Status Register Sequence Diagram

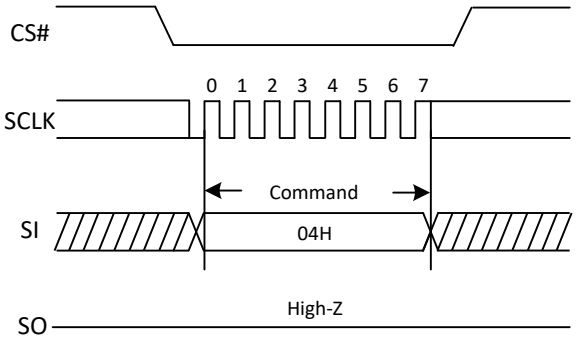


6.3. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low→sending the Write Disable command→CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

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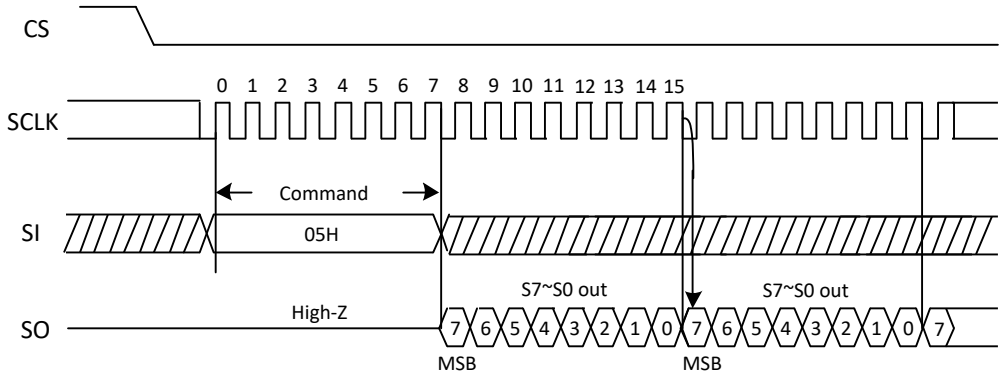
Figure 3. Write Disable Sequence Diagram



6.4. Read Status Register (RDSR) (05H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously.

Figure 4. Read Status Register Sequence Diagram



6.5. Write Status Register (WRSR) (01H)

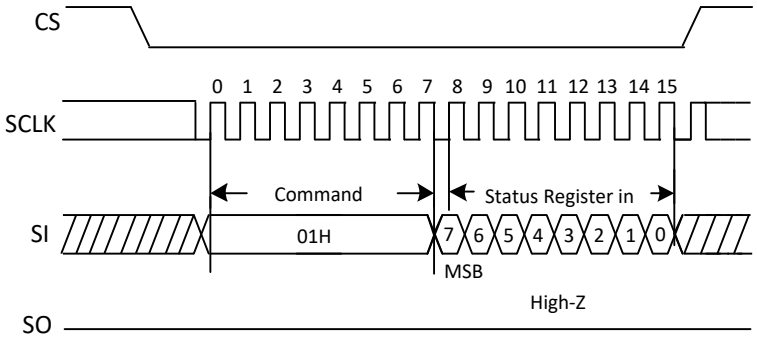
The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S5, S1 and S0 of the Status Register. CS# must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tw) is initiated. While the Write Status Register cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Status Register Write Disable (SRWD) bit is a non-volatile One Time Program(OTP) bit, the Write Status Register (WRSR) command allows the user to set the Status Register Write Disable (SRWD) bit to 1. The Status Register Write Disable (SRWD) bit allow the device to be put in another Software Protected Mode. Once the SRWD bit is set to 1, the Write Status Register (WRSR) command is not executed, and the Block Protect bits (BP2, BP1, BP0) are read only.

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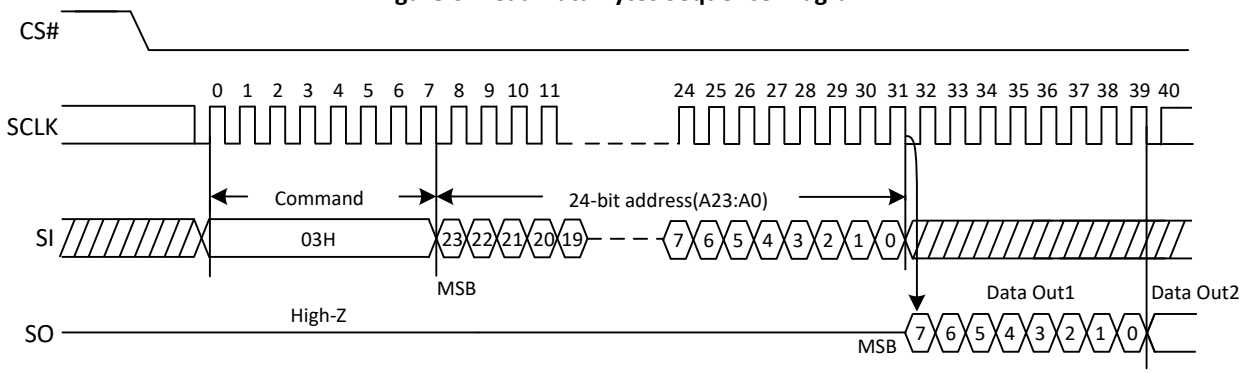
Figure 5. Write Status Register Sequence Diagram



6.6. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 6. Read Data Bytes Sequence Diagram

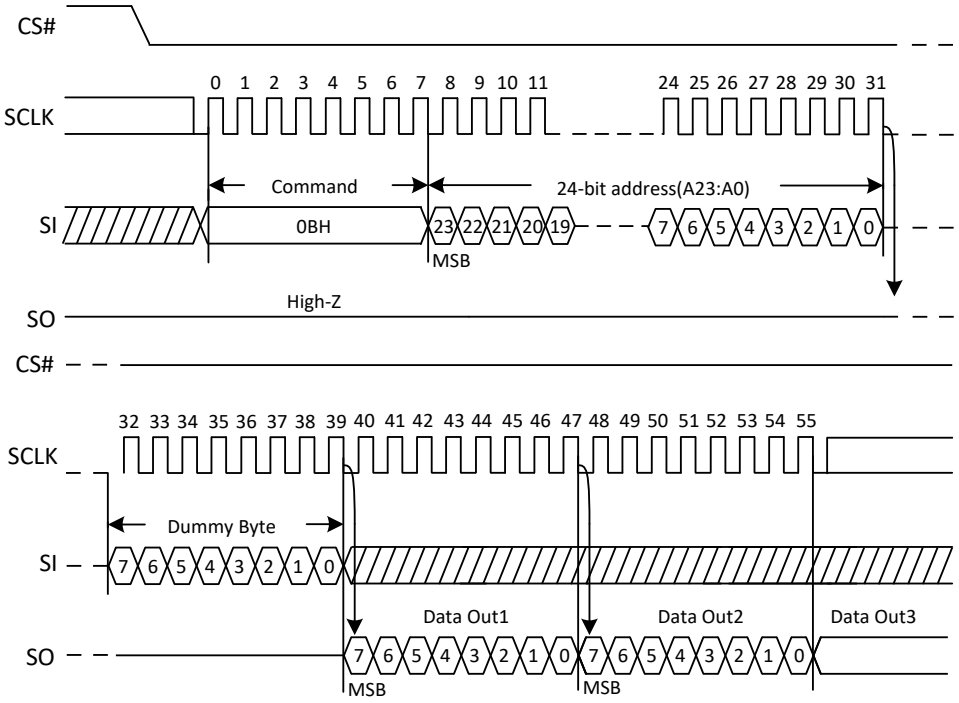


6.7. Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for fast reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

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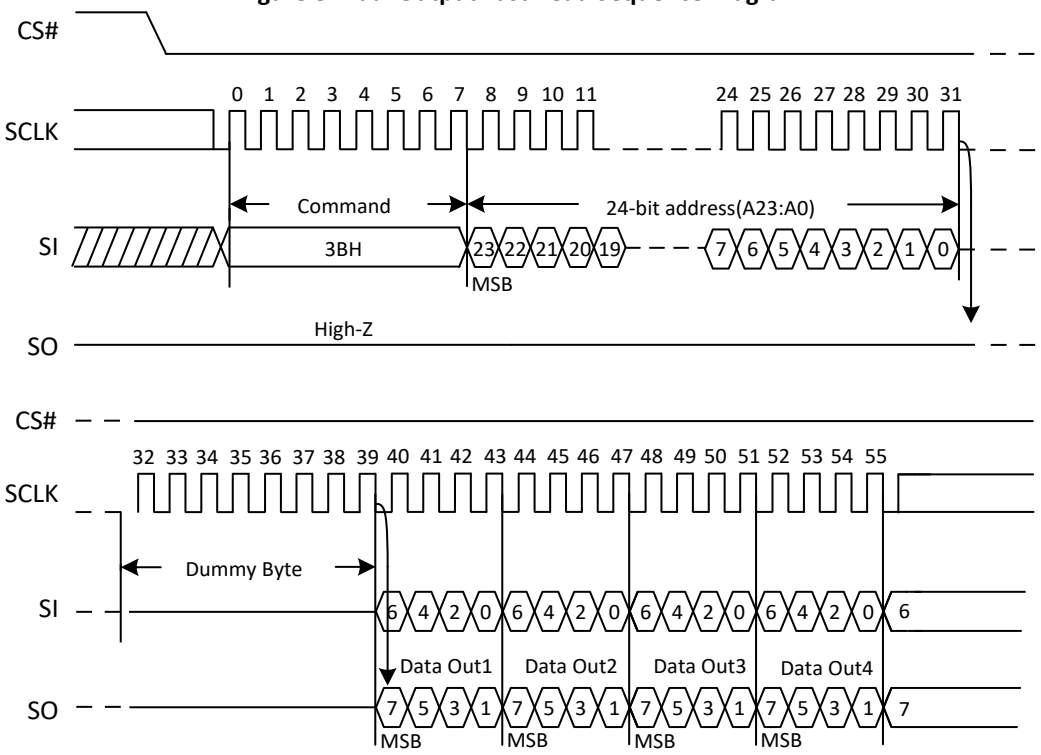
Figure 7. Read Data Bytes at Higher Speed Sequence Diagram



6.8. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 8. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 8. Dual Output Fast Read Sequence Diagram



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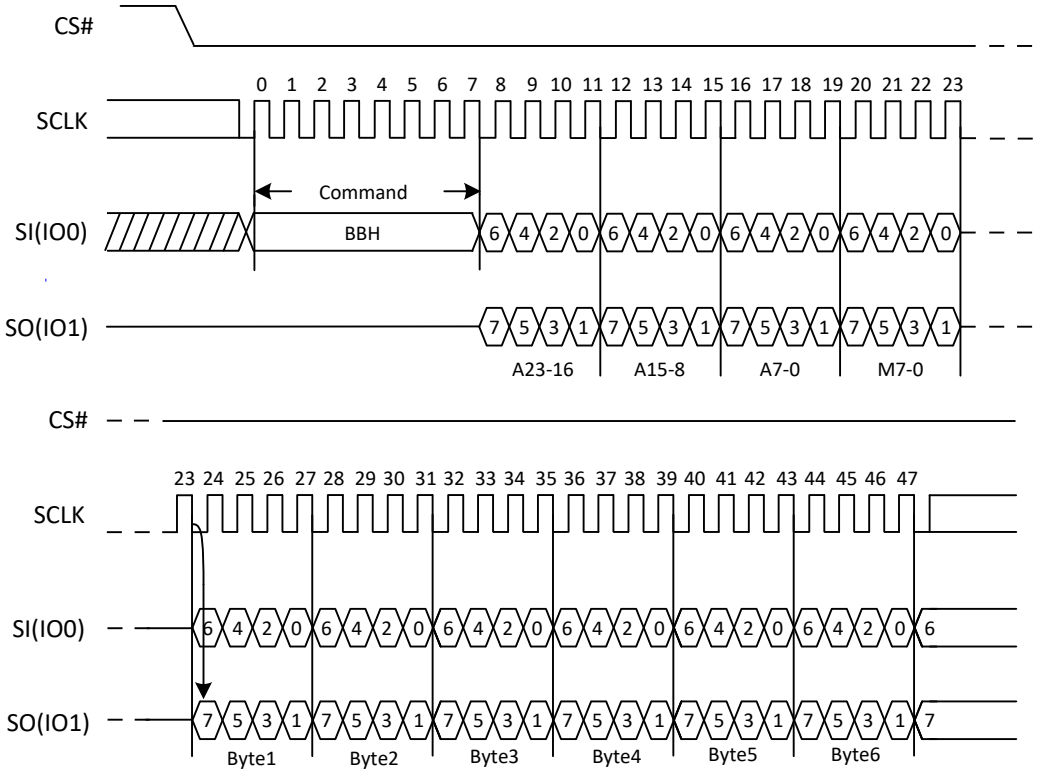
6.9. Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Dual I/O Fast Read with “Continuous Read Mode”

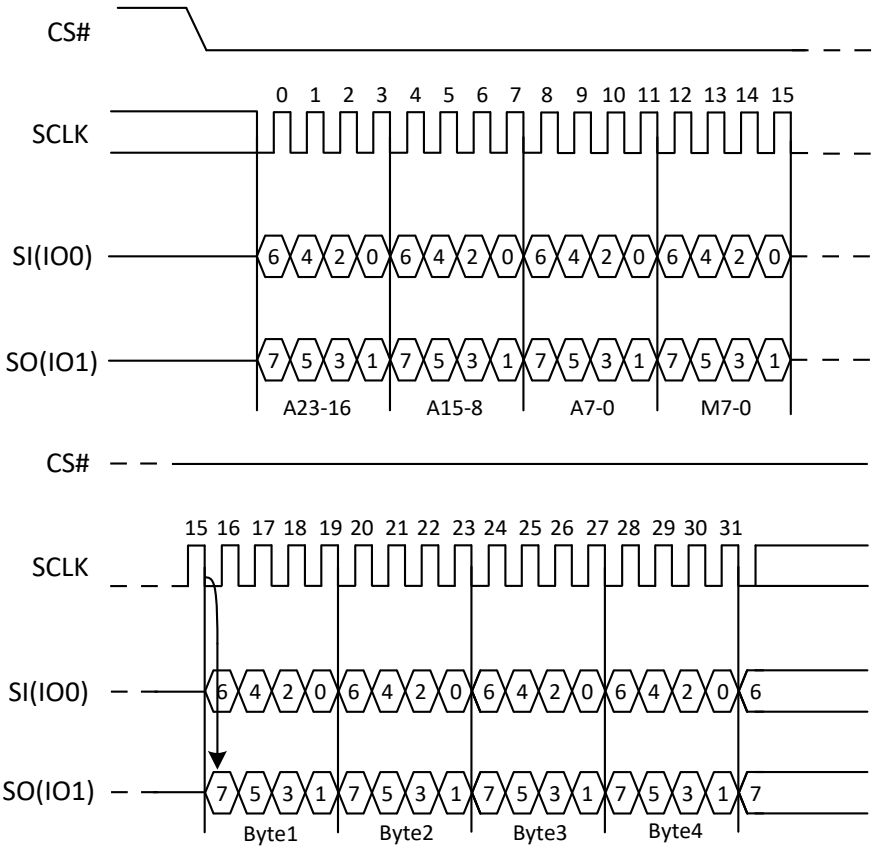
The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7- 0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5- 4) =(1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in figure 9. If the “Continuous Read Mode” bits (M5- 4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5-4) before issuing normal command.

Figure 9. Dual I/O Fast Read Sequence Diagram (M5-4≠(1, 0))



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Figure 9a. Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0))



6.10. Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

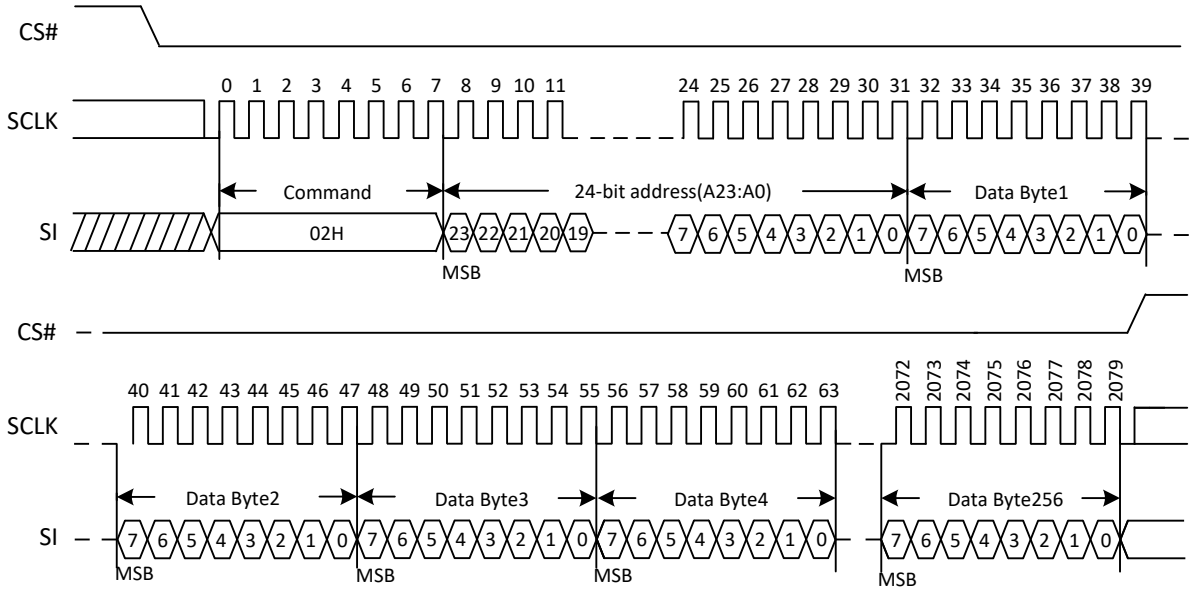
The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in Figure 10. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP2, BP1, BP0) is not executed.

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Figure 10. Page Program Sequence Diagram

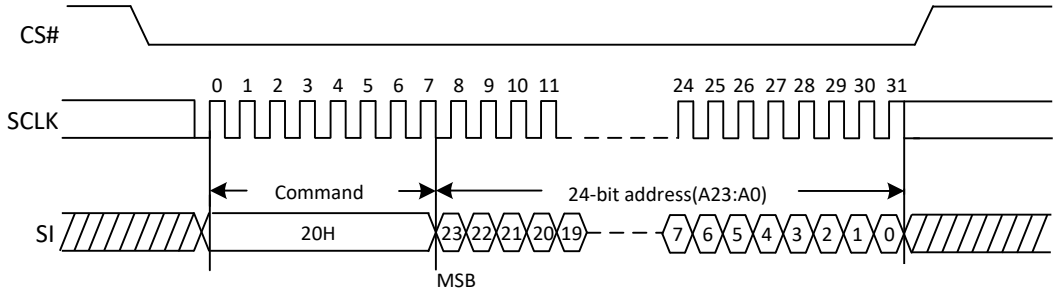


6.11. Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low →sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure 11. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP2, BP1, BP0) bit (see Table1) is not executed. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 11. Sector Erase Sequence Diagram



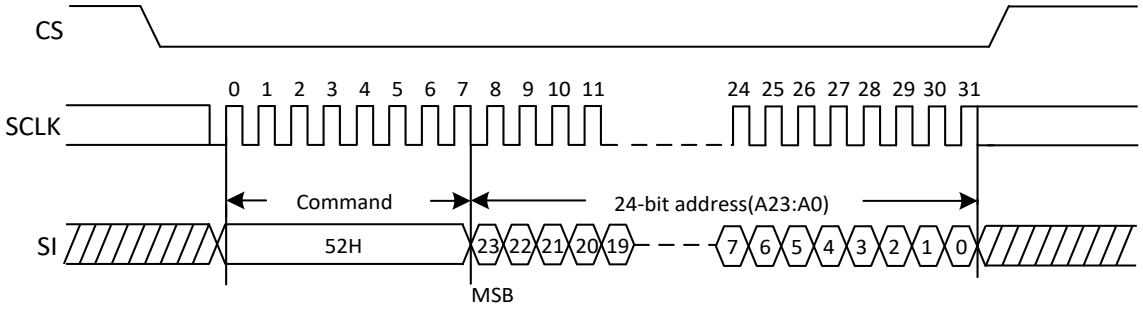
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6.12. 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low→ sending 32KB Block Erase command→ 3-byte address on SI→CS# goes high. The command sequence is shown in Figure12. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table1) will not be executed. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 12. 32KB Block Erase Sequence Diagram

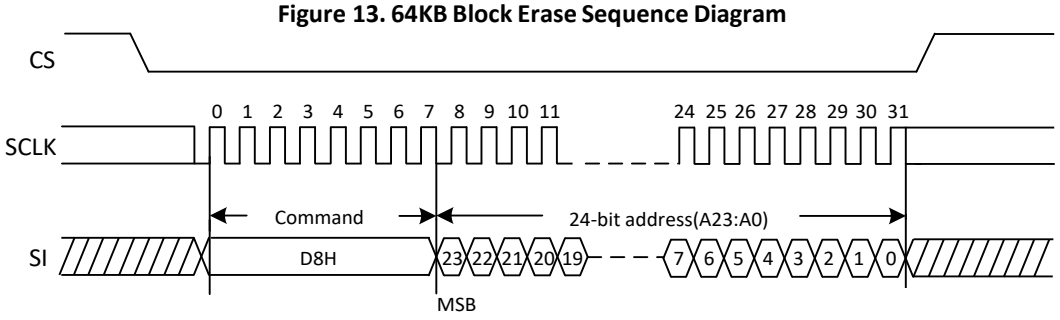


6.13. 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command →3byte address on SI → CS# goes high. The command sequence is shown in Figure 13. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table1) is not executed. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 13. 64KB Block Erase Sequence Diagram



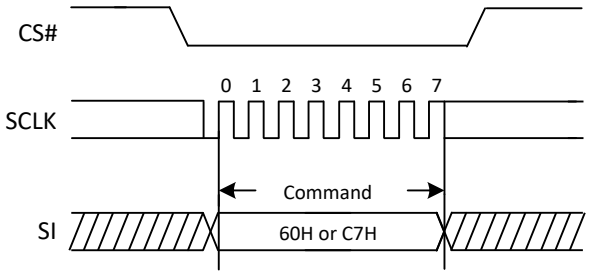
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6.14. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure 14. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are all 0. The Chip Erase (CE) command is ignored if one or more sectors are protected. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 14. Chip Erase Sequence Diagram



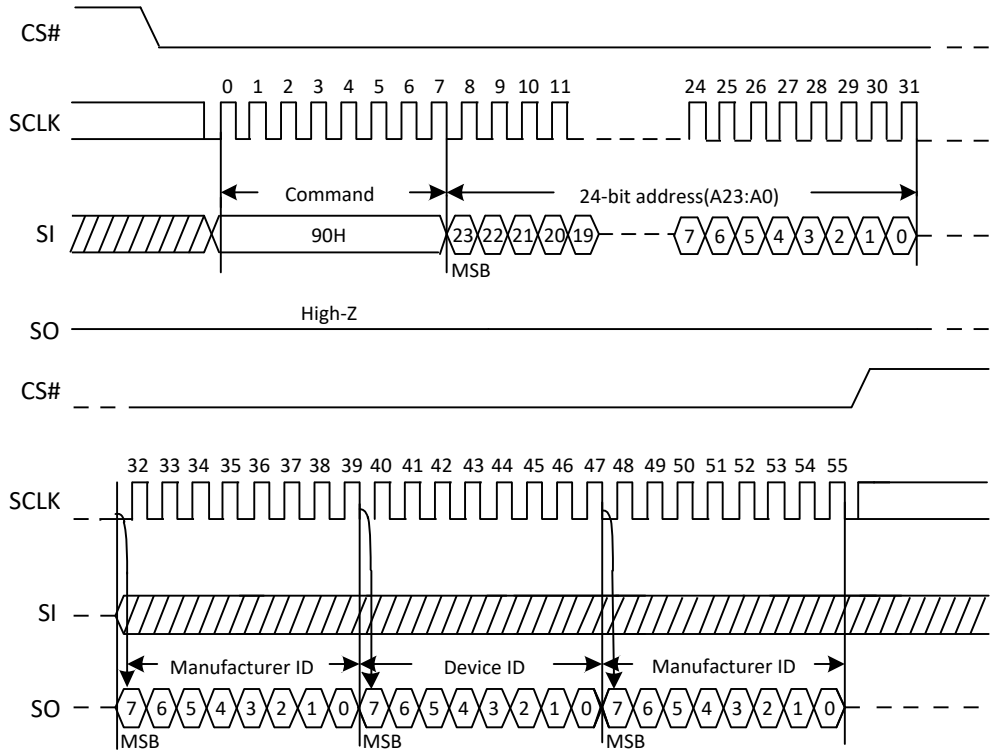
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6.15. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in Figure 15. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 15. Read ID Sequence Diagram



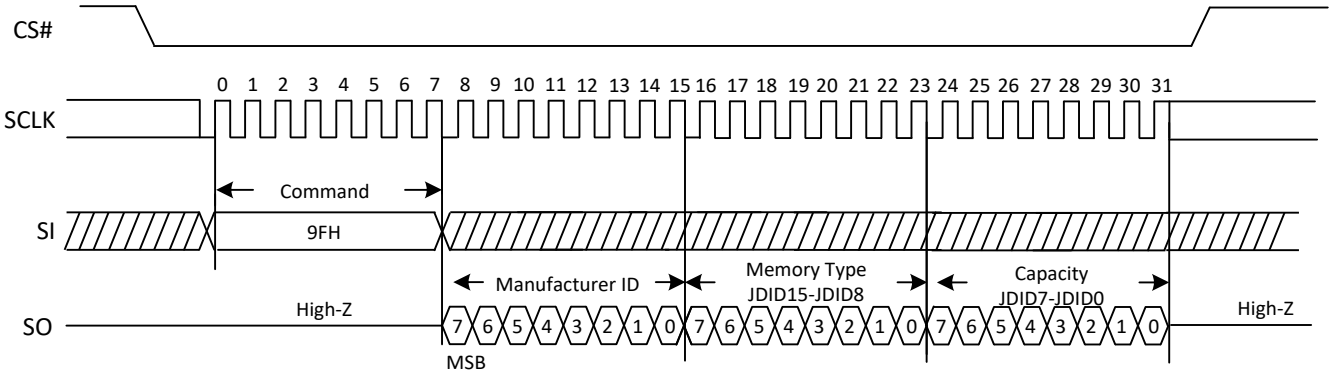
6.16. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure16. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

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Figure 16. Read Identification ID Sequence Diagram



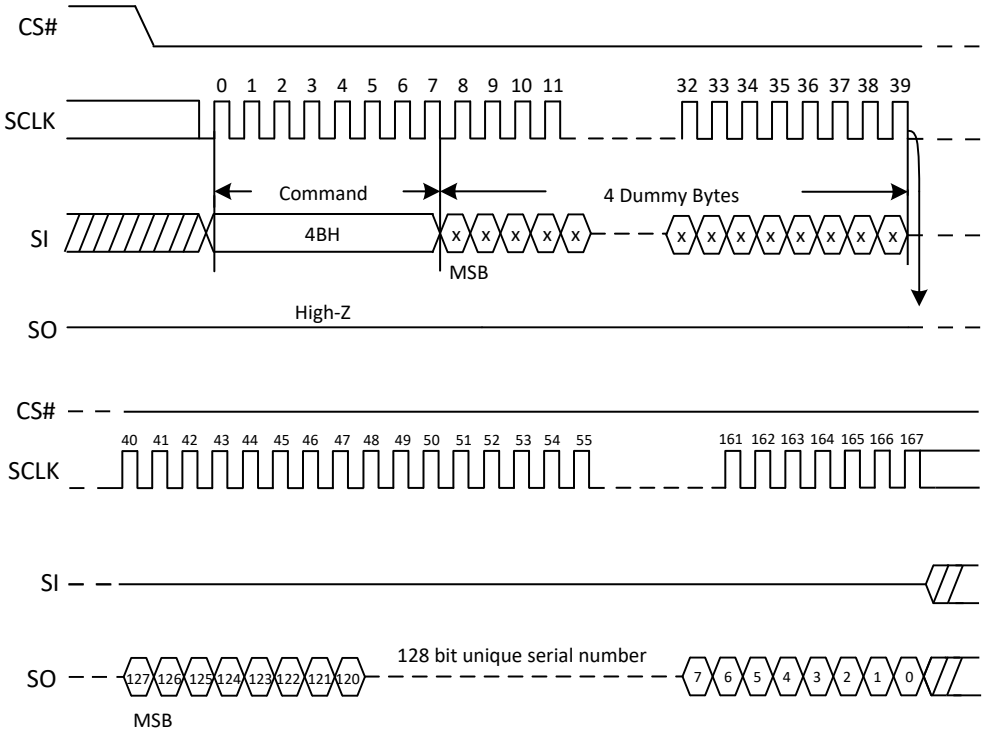
6.17. Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command →4 dummy clocks→ 128bit Unique ID Out → CS# goes high.

The command sequence is shown below.

Figure 17. Read Unique ID (RUID) Sequence (Command 4B)

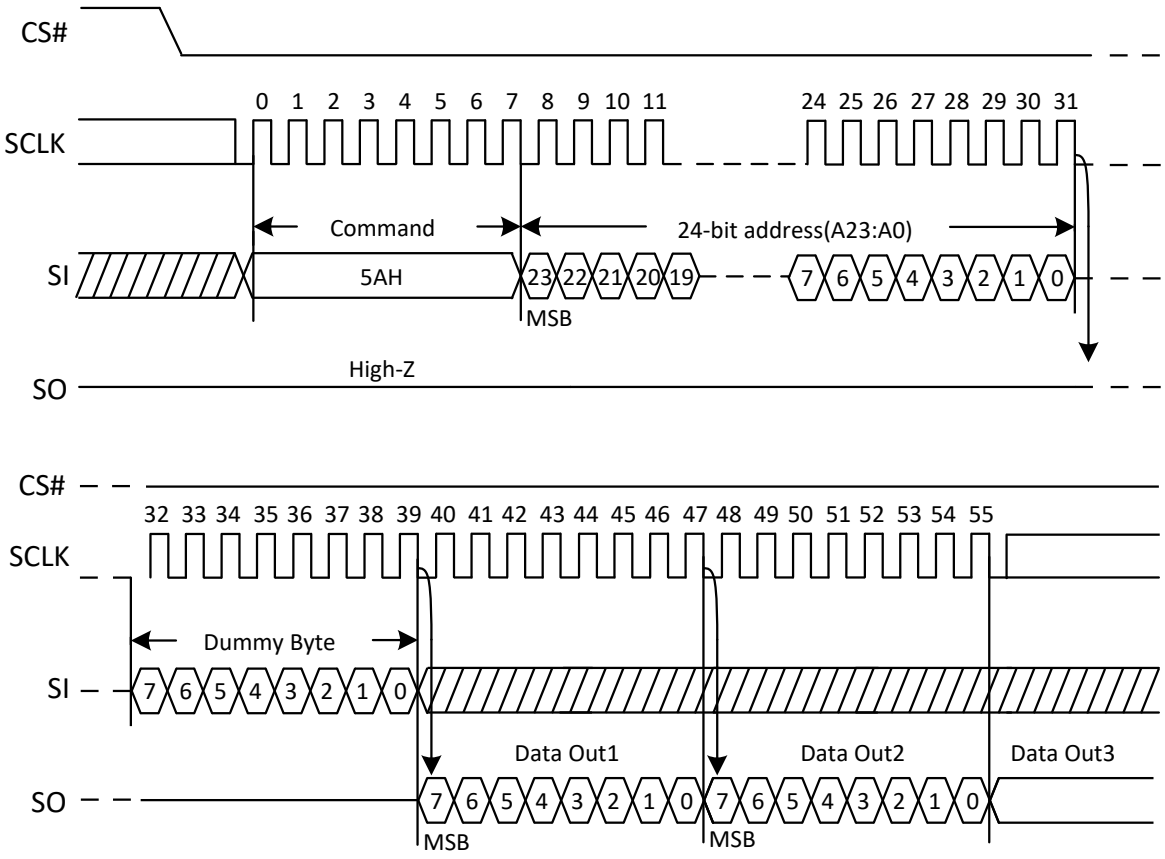


6.18. Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

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Figure 18. Read Serial Flash Discoverable Parameter command Sequence Diagram



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Table 3. Parameter Table (0): Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	02H	02H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	02H	02H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number (XTX Manufacturer ID)	It is indicates XTX manufacturer ID	10H	07:00	0BH	0BH
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	02H	02H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of XTX Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

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Parameter Table (1): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1-2) Fast Read	0=Not support, 1=Support	32H	16	1b	91H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1-2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1-4-4) Fast Read	0=Not support, 1=Support		21	0b	
(1-1-4) Fast Read	0=Not support, 1=Support		22	0b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	003FFFFFH	
(1-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support （M7-M0 excluded）	38H	04:00	00000b	00H
(1-4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	000b	
(1-4-4) Fast Read Opcode		39H	15:08	FFH	FFH
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3AH	20:16	00000b	00H
(1-1-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3BH	31:24	FFH	FFH

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Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support (M7-M0 excluded)	3EH	20:16	000000b	40H
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support 010b: 8bit Mode Bits = 2 dummy clocks （M7-M0）		23:21	010b	
(1-2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFFH	0xFFH
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support (M7-M0 included)	4AH	20:16	00000b	00H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N Bytes 0x00b: this sector type don’t exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N Bytes 0x00b: this sector type don’t exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N Bytes 0x00b: this sector type don’t exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N Bytes 0x00b: this sector type don’t exist	52H	23:16	00H	00H
Sector Type 4 erase Opcode		53H	31:24	FFH	FFH

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Parameter Table (2): XTX Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	91H:90H	15:00	3600H	3600H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2350H=2.350V 2700H=2.700V	93H:92H	31:16	2700H	2700H
HW Reset# pin	0=not support 1=support	95H:94H	00	0b	4998H
HW Hold# pin	0=not support 1=support		01	0b	
Deep Power Down Mode	0=not support 1=support		02	0b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H) before Reset cmd.		11:04	1001 1001b (99H)	
Program Suspend/Resume	0=not support 1=support		12	0b	
Erase Suspend/Resume	0=not support 1=support		13	0b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	0b	
Wrap-Around Read mode Opcode		96H	23:16	FFH	FFH
Wrap-Around Read data length	08H:support 8Byte wrap-around read 16H:8Byte&16Byte 32H:8Byte&16Byte&32Byte 64H:8Byte&16Byte&32Byte&64Byte	97H	31:24	FFH	FFH
Individual block lock	0=not support 1=support	9BH:98H	00	0b	EBFCH
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFH	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	1b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

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6.19. Erase Security Registers (44H)

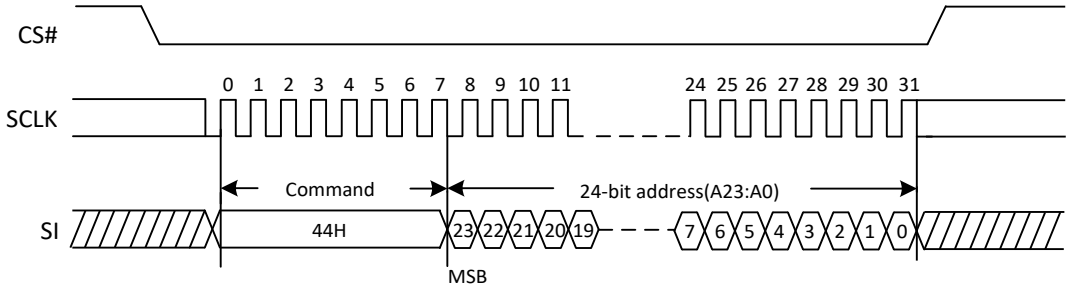
The XT25F04D provides two 256-byte Security Registers which only erased all at once but able to program individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low, sending Erase Security Registers Command, CS# goes high. The command sequence is shown in Figure 19. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-A16	A15-A8	A7-A0
Security Registers 0	00H	00H	Don't Care
Security Registers 1	00H	01H	Don't Care

Figure 19. Erase Security Registers command Sequence Diagram



6.20. Program Security Registers (42H)

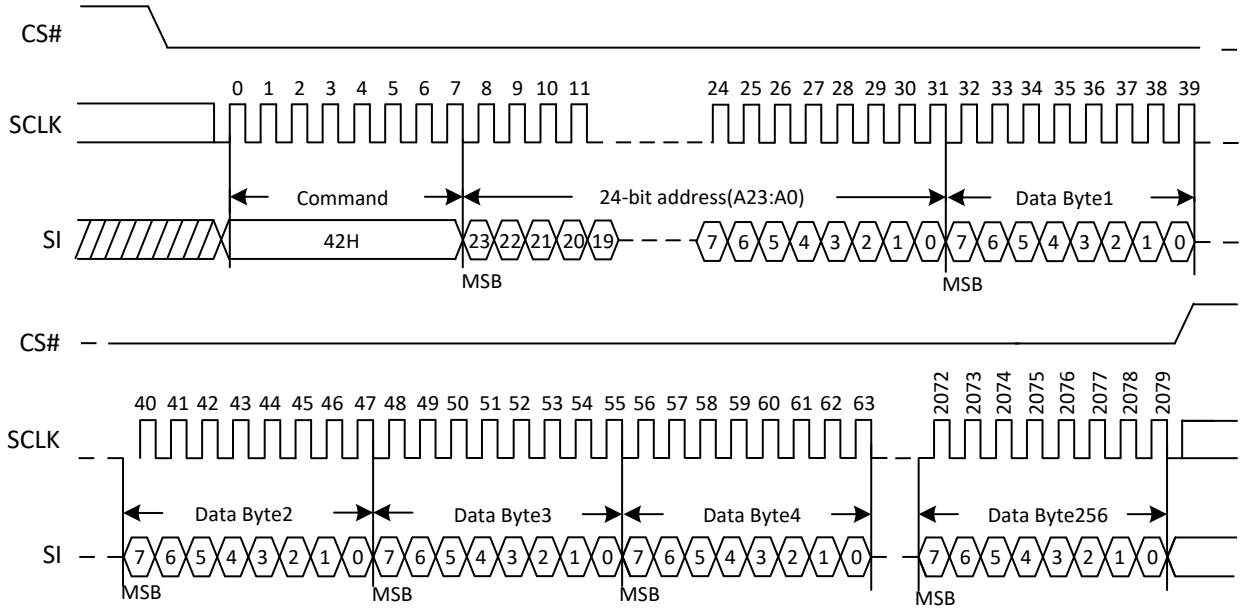
The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-A16	A15-A8	A7-A0
Security Registers 0	00H	00H	Byte Address
Security Registers 1	00H	01H	Byte Address

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Figure 20. Program Security Registers command Sequence Diagram

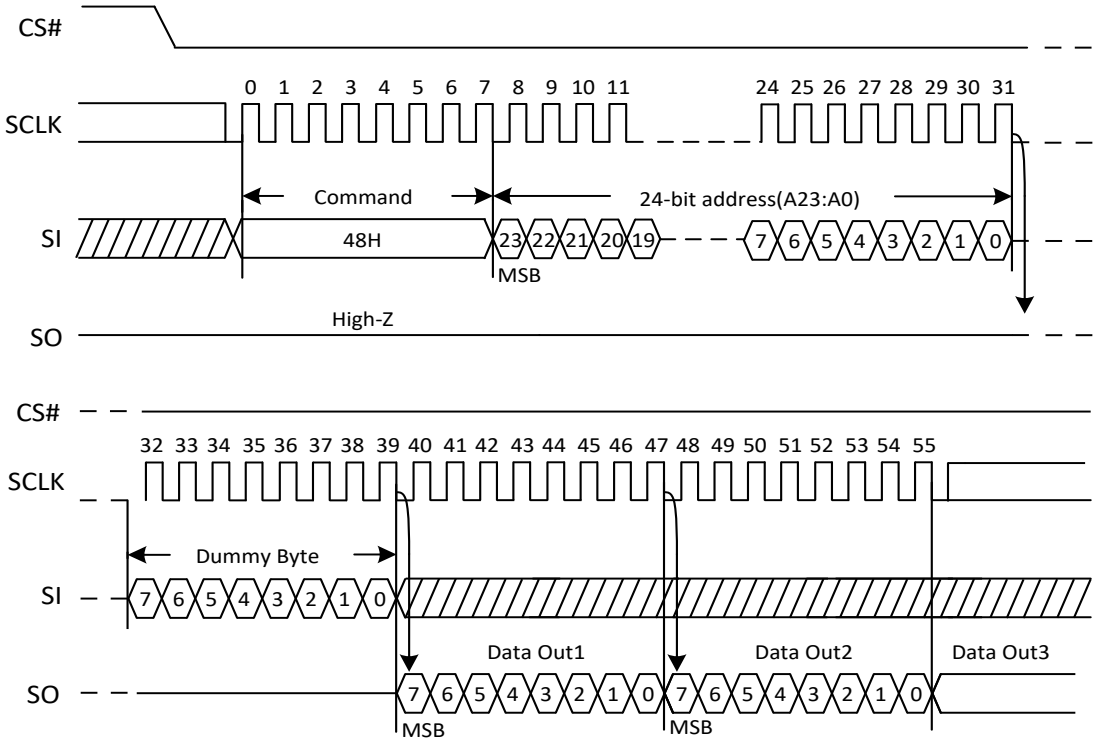


6.21. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-A16	A15-A8	A7-A0
Security Registers 0	00H	00H	Byte Address
Security Registers 1	00H	01H	Byte Address

Figure 21. Read Security Registers command Sequence Diagram

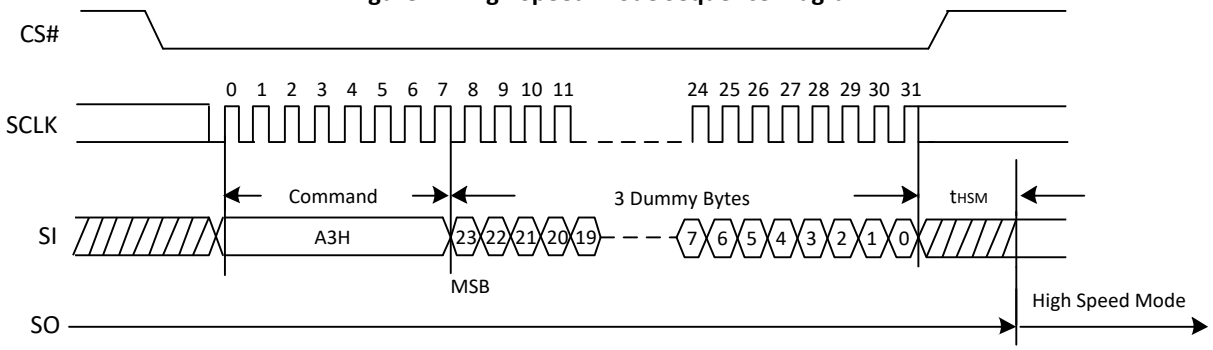


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6.22. High Speed Mode(HSM)(A3H)

The High Speed Mode (HSM) command must be executed prior to Dual I/O commands when operating at high frequencies (see fR and fC1 in AC Electrical Characteristics). This command allows pre-charging of internal charge pumps so the voltages required for accessing the flash memory array are readily available. The command sequence: CS# goes low Sending A3H command Sending 3-dummy byte CS# goes high. See Figure 22. After the HSM command is executed, the device will maintain a slightly higher standby current (ICC8) than standard SPI operation. The Release from Power-Down or HSM command (ABH) can be used to return to standard SPI standby current (ICC1). In addition, Write Enable command (06H) and Power-Down command (B9H) will also release the device from HSM mode back to standard SPI standby state.

Figure 22. High Speed Mode Sequence Diagram

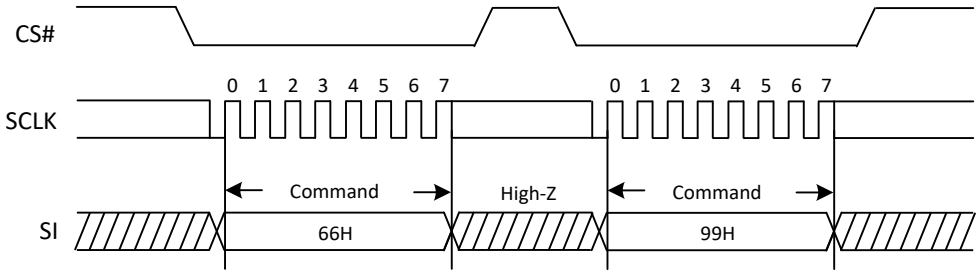


6.23. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL).

The “Reset (99H)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRSTR to reset. During this period, no command will be accepted.

Figure 23. Enable Reset and Reset command Sequence Diagram



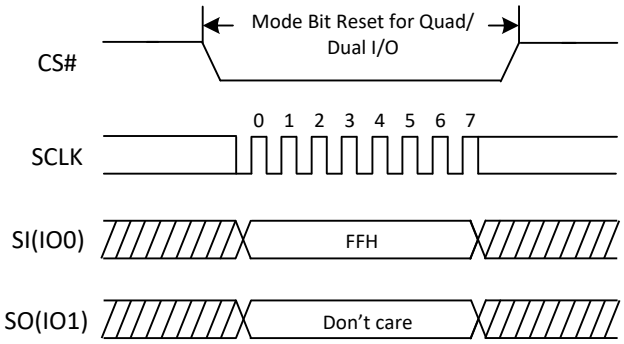
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6.24. Continuous Read Mode Reset (CRMR) (FFH)

The Dual I/O Fast Read operations, “Continuous Read Mode” bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual I/O Fast Read operations do not require the BBH command code.

Because the XT25F04D has no hardware reset pin, so if Continuous Read Mode bits are set to “AXH”, the XT25F04D will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the “AXH” state and allow standard SPI command to be recognized. The command sequence is shown in Figure 24.

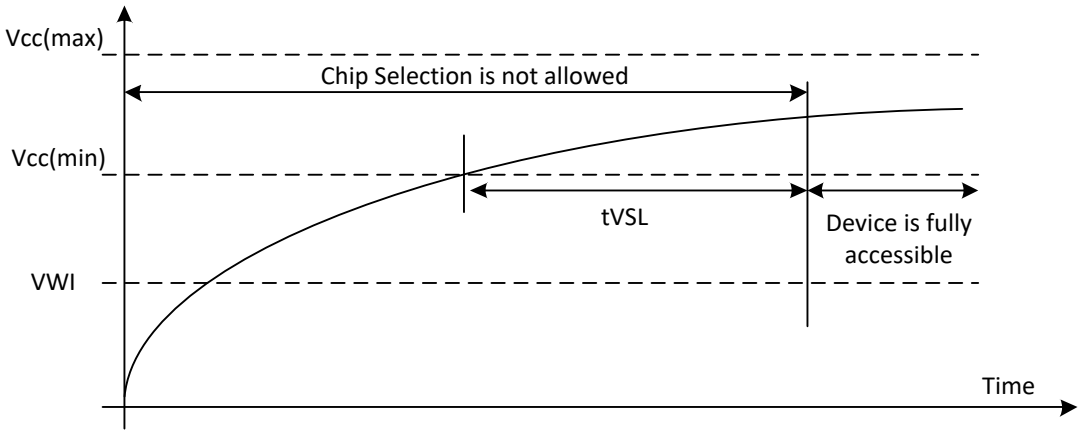
Figure 24. Continuous Read Mode Reset Sequence Diagram



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7. ELECTRICAL CHARACTERISTICS

7.1. Power-on Timing



Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}	VCC(min) To CS# Low	1		ms
V_{WI}	Write Inhibit Voltage	1.5	2.5	V

7.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

7.3. Data Retention and Endurance

Parameter	Typ.	Unit
Data Retention Time	20	Years
Erase/Program Endurance	100K	Cycles

7.4. Latch up Characteristics

Parameter	Min.	Max.
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

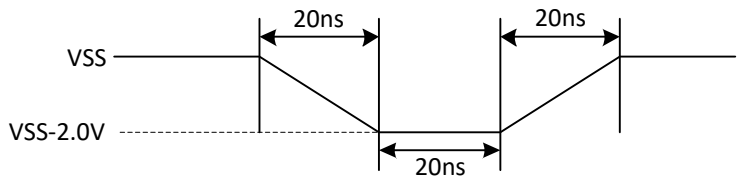
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7.5. Absolute Maximum Ratings

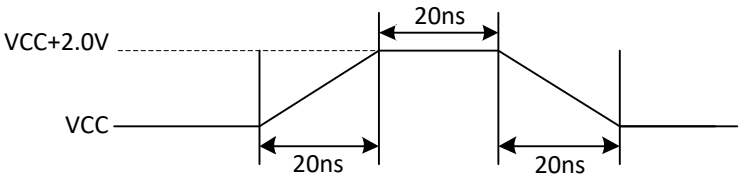
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	°C
Storage Temperature	-65 to 150	°C
Output Short Circuit Current	200	mA
Applied Input / Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

Figure 25. Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



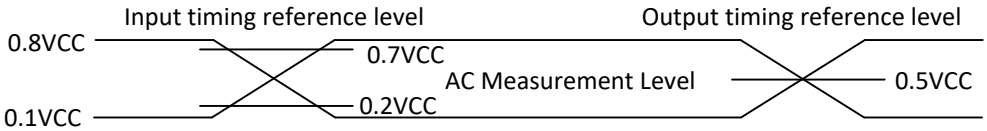
Maximum Positive Overshoot Waveform



7.6. Capacitance Measurement Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure 26. Absolute Maximum Ratings Diagram



Note：Input pulse rise and fall time are <5ns

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7.7. DC Characteristics

(TA=-40°C~85°C, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ. (1)	Max.	Unit
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
I_{CC1}	Standby Current	CS#=VCC VIN=VCC or VSS		13	30	µA
I_{CC3}	Operating Current(Read)	CLK=0.1VCC/0.9VCC at 40MHZ,Q=Open(*1 I/O)		5	7	mA
		CLK=0.1VCC/0.9VCC at 50MHZ,Q=Open(*1 I/O)		6	8	mA
		CLK=0.1VCC/0.9VCC at 120MHZ,Q=Open(*1 I/O)		8	12	mA
		CLK=0.1VCC/0.9VCC at 40MHZ,Q=Open(*2 I/O)		5	8	mA
		CLK=0.1VCC/0.9VCC at 50MHZ,Q=Open(*2 I/O)		6	9	mA
		CLK=0.1VCC/0.9VCC at 120MHZ,Q=Open(*2 I/O)		10	15	mA
I_{CC4}	Operating Current(PP)	CS#=VCC		10	20	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC		10	20	mA
I_{CC6}	Operating Current(SE)	CS#=VCC		10	20	mA
I_{CC7}	Operating Current(BE)	CS#=VCC		10	20	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	IOL=1.6mA			0.4	V
V_{OH}	Output High Voltage	IOH=-100µA	VCC-0.2			V

Note:

1. Typical values given for TA=25°C, VCC=3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

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7.8. AC Characteristics

(TA=-40°C~85°C,VCC=2.7~3.6V， C_L=30pF)

Symbol	Parameter	Min.	Typ.(2)	Max.(7)	Unit
fC	Serial Clock Frequency For: Fast Read(0BH), Dual Output(3BH)	DC		120	MHz
fC1	Serial Clock Frequency For: Dual I/O(BBH)	DC		104	MHz
fR	Serial Clock Frequency For: Read (03H/9FH/90H)	DC		40	MHz
tCLH(1)	Serial Clock High Time	45%PC			ns
tCLL(1)	Serial Clock Low Time	45%PC			ns
tCLCH	Serial Clock Rise Time(Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time(Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL	CS# High Time (read/write)	20			ns
tSHQZ	Output Disable Time			9	ns
tCLQX	Output Hold Time	1			ns
tDVCH	Data In Setup Time	3			ns
tCHDX	Data In Hold Time	3			ns
tCLQV	Clock Low To Output Valid			6.5	ns
tWHSL	Write Protect Setup Time Before CS# Low	20			ns
tSHWL	Write Protect Hold Time After CS# High	100			ns
tDP	CS# High To Deep Power-Down Mode			0.1	µs
tRES1	CS# High To Standby Mode Without Electronic Signature Read			0.5	µs
tRES2	CS# High To Standby Mode With Electronic Signature Read			0.5	µs
tW	Write Status Register Cycle Time		5	600	ms
tPP	Page Programming Time		0.9	3.0	ms
tSE(4) (6)	Sector Erase Time		55	2500	ms
tBE	Block Erase Time(32K Bytes)		0.3	3.0	s
tBE	Block Erase Time(64K Bytes)		0.45	4.0	s
tCE(5)	Chip Erase Time（4M）		2.5	10.0	s

Note:

1. Clock high or Clock low must be more than or equal to 45%PC, PC=1/fC(Max).
2. Typical values given for TA=25°C, VCC=3.3V.
3. Value guaranteed by design and/or characterization, not 100% tested in production.
4. For the first sector of each array at each power on, tSE is 90ms typically; for the rest, tSE is 55ms typically.
5. If pattern=0xFF, tCE = 0.35s.
6. The max value of tSE is 600ms within 20K P/E cycling.
7. Maximum Serial Clock Frequencies are measured results picked at the falling edge.

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Figure 27. Serial Input Timing

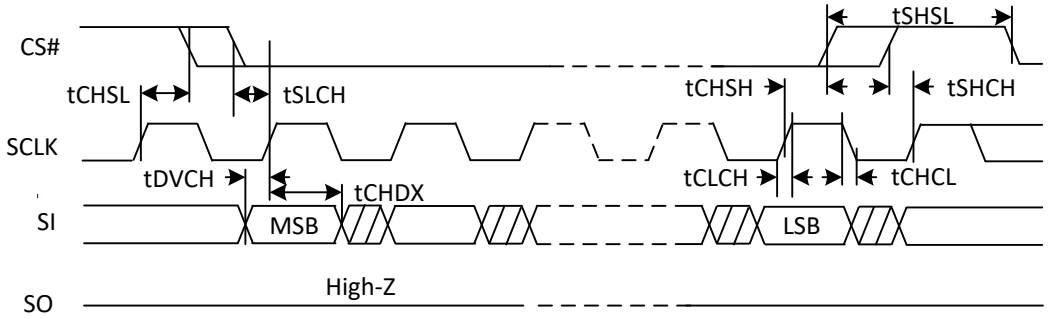
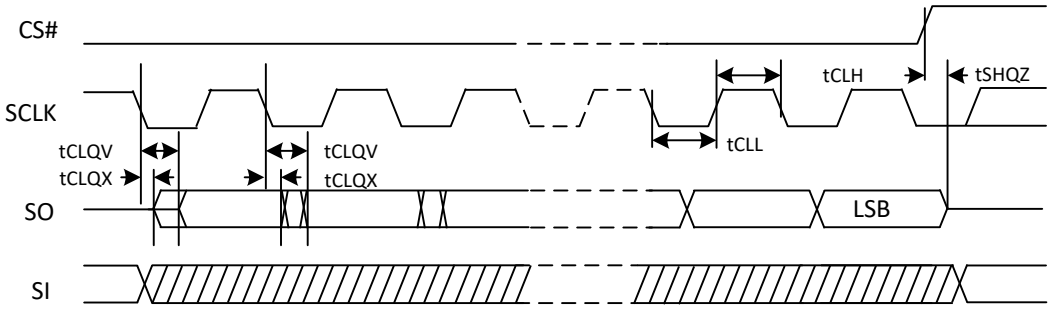


Figure 28. Output Timing



Least significant address bit (LSB) in

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8. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following:

XT 25F 04D SO I G U

Company Prefix

XT = XTX

Product Family

25F = 2.7~3.6V Serial Flash Memory with 4KB Uniform-Sector

Product Density

04D = 4M bit

Product Package

SO = SOP8 (150mil)
DT = DFN8 (2x3x0.4mm)

Temperature & Moisture Sensitivity Level

I = Industrial Level Temp. (-40°C to +85°C), MSL3

Green Code

G = Green/Reach Package

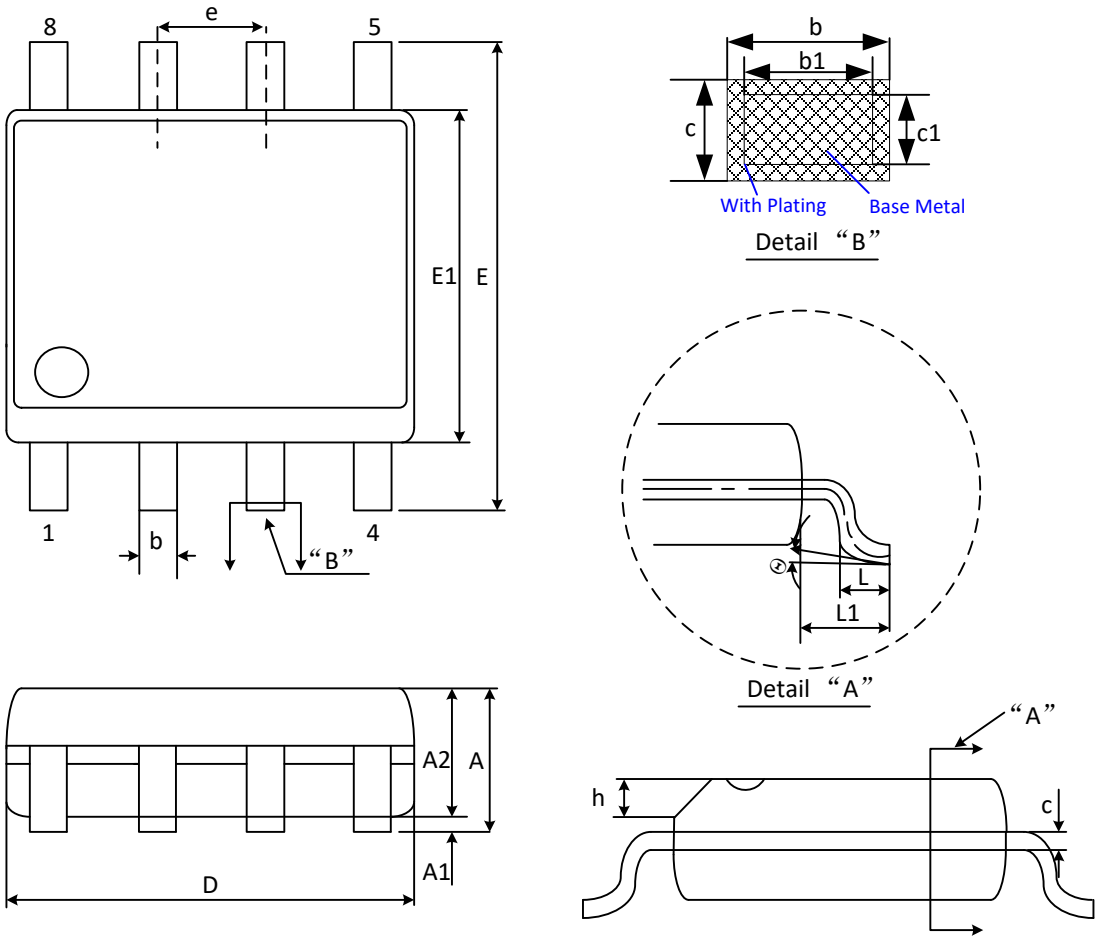
Product Carrier

U = Tube; **T** = Tape & Reel; **A** = Tray

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9. PACKAGE INFORMATION

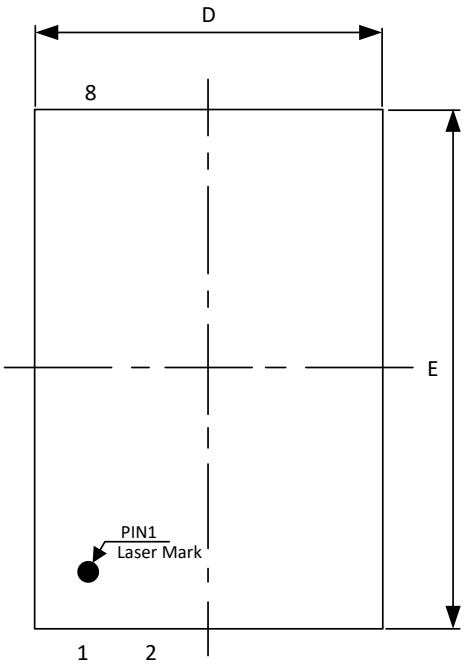
9.1. Package SOP8 150MIL



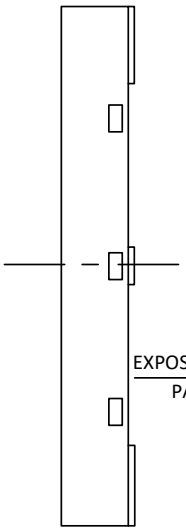
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.25
A2	1.30	1.40	1.50
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0°	—	8°

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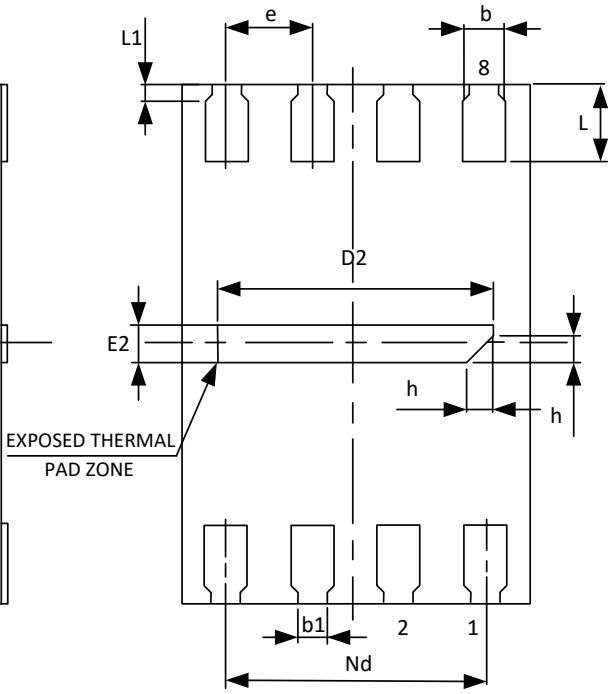
9.2. Package DFN8 (2x3x0.4) mm



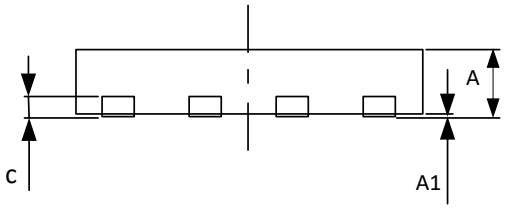
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	—	0.40
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.127REF	
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
e		0.50BSC	
Nd		1.50BSC	
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
L	0.40	0.45	0.50
L1	0.05	0.10	0.15
h	0.10	0.15	0.20

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10. REVISION HISTORY

Revision	Description	Date
1.0	Preliminary version base 2M/4M rev 1.4, 1.3	Jan-14-2019
1.1	Correct typos in SRWD description and add on 6.31. Read Serial Flash Discoverable Parameter tables, modified AC Characteristics according to qualification results	May-13-2019
1.2	Add DFN8 (2x3x0.4) mm package type. Revise AC Characteristics (page #37) TSE max to 200mS.	Jul-12-2019
1.3	Updated Note for power-down requirements at 7.1, deleted package SOP8 208mil, TSSOP8. Reserved SRWD bit and added Note.	Aug-7-2019
1.4	Deleted related contents about deep power down, updated AC Characteristics	Dec-17-2019
1.5	Updated figure of A3H	April 9, 2020
1.6	Updated SFDP Table	Aug 12, 2020
1.7	Deleted DFN 2x3x0.55mm package	Sep 7, 2020
1.8	Add DFN8 connection diagram, updated Pin Description and data protection, change the sequence of status register and data protection.	Sep 24, 2020
1.9	Add OPN XT25F04DSOIGA	Jan 26, 2021
2.0	Update POD of SOP8 150mil, DFN8 (2x3x0.4)mm. Update company name and logo Update the connection diagram of 8-PIN SOP and 8-PIN DFN	Apr 01, 2020
2.1	Adjusted tSHQZ from 6ns to 9ns tDVCH from 2ns to 3ns tCHDX from 2ns to 3ns tSE typical from 90ms to 55ms tSE max from 600ms to 2500ms tBE(32K) max from 1s to 3s tBE(64K) max from 1.5s to 4s tCE typical from 3.2s to 2.5s Added Note 4/5/6/7 after the AC CharacteristicsTable	Aug 04, 2021
2.2	Correct Typo at the front page	Aug 02, 2022

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