128Mb Async./Page,Syn./Burst CellularRAM

1. GENERAL DESCRIPTION

Winbond CellularRAM™ products are high-speed, CMOS pseudo-static random access memories developed for low-power, portable applications. The device has a DRAM core organized. These devices include an industry-standard burst mode Flash interface that dramatically increases read/write bandwidth compared with other low-power SRAM or Pseudo SRAM offerings.

To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device READ/WRITE performance.

Two user-accessible control registers define device operation. The Bus Configuration Register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The Refresh Configuration Register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three mechanisms to minimize standby current. Partial array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) enables the system to halt the refresh operation altogether when no vital information is stored in the device. The system configurable refresh mechanisms are accessed through the RCR.

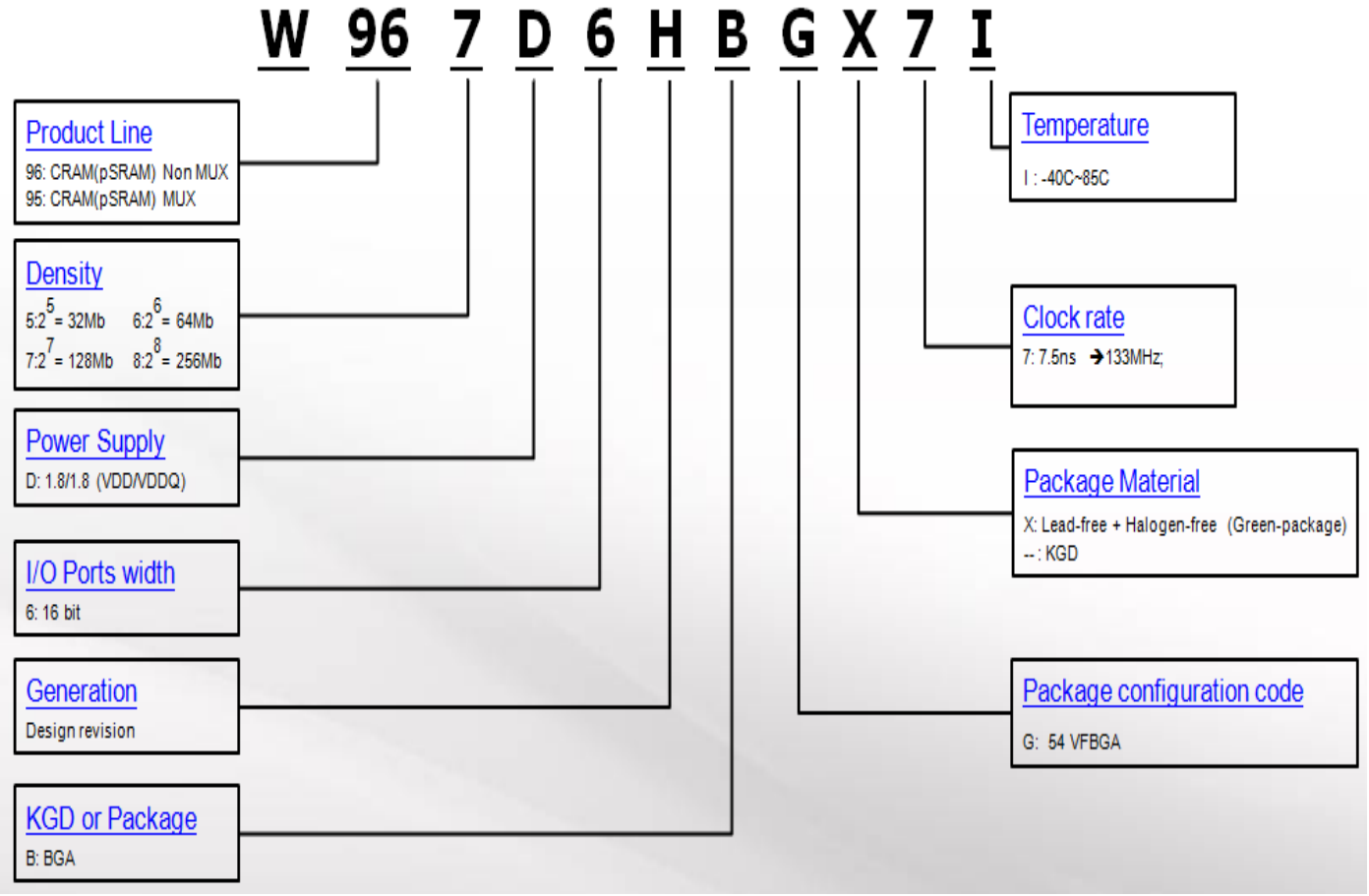
This CellularRAM device is compliant with the industry-standard CellularRAM 1.5 generation feature set established by the CellularRAM Workgroup. It includes support for both variable and fixed latency, with 3 output-device drive-strength settings, additional wrap options, and a device ID register (DIDR).

2. FEATURES

- •Supports asynchronous, page, and burst operations
- • VCC, VCCQ Voltages:
  - 1.7V–1.95V VCC
  - 1.7V–1.95V VCCQ
- • Random access time: 70ns
- • Burst mode READ and WRITE access:
  - 4, 8, 16, or 32 words, or continuous burst
  - Burst wrap or sequential
  - Max clock rate: 133 MHz (tCLK = 7.5ns)
- • Page mode READ access:
  - Sixteen-word page size
  - Interpage READ access: 70ns
  - Intrapage READ access: 20ns
- • Low-power features
  - On-chip temperature compensated refresh (TCR)
  - Partial array refresh (PAR)
  - Deep power-down (DPD) mode
- • Package: 54 Ball VFBGA
- • Active current (ICC1) <35mA at 85°C
- • Standby current 250µA (max) at 85°C
- • Deep power-down: Typical 10µA
- •Operating temperature range : -40°C ~ 85°C

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3. ORDERING INFORMATION



Part Number	VDD/VDDQ	I/O Width	Type	Others
W967D6HBGX7I	1.8/1.8	x16	PKG	CRAM Non-Mux,133MHz, -40°C~85°C

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TABLE OF CONTENTS

1. GENERAL DESCRIPTION 1
2. FEATURES 1
3. ORDERING INFORMATION 2
4. PIN CONFIGURATION 6
4.1 Ball Assignment 6
5. PIN DESCRIPTION 7
5.1 Signal Description 7
6. BLOCK DIAGRAM 8
6.1 Block Diagram 8
6.2 CellularRAM - Interface Configuration Options 9
7. INSTRUCTION SET 10
7.1 Bus Operation 10
8. FUNCTIONAL DESCRIPTION 11
8.1 Power Up Initialization 11
8.1.1 Power-Up Initialization Timing 11
8.2 Bus Operating Modes 11
8.2.1 Asynchronous Modes 11
8.2.1.1 READ Operation(ADV# LOW) 12
8.2.1.2 WRITE Operation (ADV# LOW) 12
8.2.2 Page Mode READ Operation 13
8.2.2.1 Page Mode READ Operation (ADV# LOW) 13
8.2.3 BURST Mode Operation 13
8.2.3.1 Burst Mode READ (4-word burst) 14
8.2.3.2 Burst Mode WRITE (4-word burst) 15
8.2.3.3 Refresh Collision During Variable-Latency READ Operation 16
8.2.4 Mixed-Mode Operation 17
8.2.4.1 WAIT Operation 17
8.2.4.2 Wired-OR WAIT Configuration 17
8.2.5 LB#/ UB# Operation 18
8.3. Low Power Operation 18
8.3.1 Standby Mode Operation 18
8.3.2 Temperature Compensated Refresh 18
8.3.3 Partial Array Refresh 18
8.3.4 Deep Power-Down Operation 18
8.4 Registers 19
8.4.1 Access Using CRE 19
8.4.1.1 Configuration Register WRITE, Asynchronous Mode Followed by READ ARRAY Operation 19
8.4.1.2 Configuration Register WRITE – CE# control 20
8.4.1.3 Configuration Register WRITE, Synchronous Mode Followed by READ ARRAY Operation 21
8.4.1.4 Register READ, Asynchronous Mode Followed by READ ARRAY Operation 22
8.4.1.5 Register READ, Synchronous Mode Followed by READ ARRAY Operation 23
8.4.2 Software Access 24
8.4.2.1 Load Configuration Register 24
8.4.2.2 Read Configuration Register 25
8.4.3 Bus Configuration Register 25
8.4.3.1 Bus Configuration Register Definition 26
8.4.3.2 Burst Length (BCR[2:0]) Default = Continuous Burst 27
8.4.3.3 Burst Wrap (BCR[3]) Default = No Wrap 27
8.4.3.4 Sequence and Burst Length 28
8.4.3.5 Drive Strength (BCR[5:4]) Default = Outputs Use Half-Drive Strength 29
8.4.3.6 Drive Length 29
8.4.3.7 WAIT Signal in Synchronous Burst Mode 29
8.4.3.8 WAIT Config. (BCR[8]) 29

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8.4.3.9 WAIT Polarity (BCR[10]) 29
8.4.3.10 WAIT Configuration During Burst Operation 30
8.4.3.11 WAIT Function by Configuration (WC) – Lat=2, WP=0 30
8.4.3.12 Latency Counter (BCR[13:11]) 31
8.4.3.13 Initial Access Latency (BCR[14]) 31
8.4.3.14 Allowed Latency Counter Settings in Variable Latency Mode 31
8.4.3.15 Latency Counter (Variable Initial Latency, No Refresh Collision) 32
8.4.3.16 Latency Counter (Variable Initial Latency, With Refresh Collision) 32
8.4.3.17 Allowed Latency Counter Settings in Fixed Latency Mode 33
8.4.3.18 Latency Counter (Fixed Latency) 33
8.4.3.19 Burst Write Always Produces Fixed Latency 34
8.4.3.20 Burst Interrupt 34
8.4.3.21 End-of-Row Condition 34
8.4.3.22 Burst Termination or Burst Interrupt At the End of Row 34
8.4.3.23 Operating Mode (BCR[15]) Default = Asynchronous Operation 34
8.4.4 Refresh Configuration Register 35
8.4.4.1 Refresh Configuration Register Mapping 35
8.4.4.2 Partial Array Refresh (RCR[2:0] Default = Full Array Refresh 35
8.4.4.3 Address Patterns for PAR (RCR[4] = 1) 36
8.4.4.4 Deep Power-Down (RCR[4]) 36
8.4.4.5 Page Mode Operation (RCR[7]) 36
8.4.5 Device Identification Register 36
8.4.5.1 Device Identification Register Mapping 36
8.4.6 Virtual Chip Enable Function: 37
9. ELECTRICAL CHARACTERISTIC 37
9.1 Absolute Maximum DC, AC Ratings 37
9.2 Electrical Characteristics and Operating Conditions 38
9.3 Deep Power-Down Specifications 39
9.4 Partial Array Self Refresh Standby Current (Typical Values in µA) 39
9.5 Capacitance 39
9.6 AC Input-Output Reference Waveform 39
9.7 AC Output Load Circuit 39
10. TIMING REQUIRMENTS 40
10.1 Read, Write Timing Requirements 40
10.1.1 Asynchronous READ Cycle Timing Requirements 40
10.1.2 Burst READ Cycle Timing Requirements 41
10.1.3 Asynchronous WRITE Cycle Timing Requirements 42
10.1.4 Burst WRITE Cycle Timing Requirements 43
10.2 TIMING DIAGRAMS 44
10.2.1 Initialization Period 44
10.2.2 DPD Entry and Exit Timing Parameters 44
10.2.3 Initialization and DPD Timing Parameters 44
10.2.4 Asynchronous READ 45
10.2.5 Asynchronous READ Using ADV# 46
10.2.6 Page Mode READ 47
10.2.7 Single-Access Burst READ Operation-Variable Latency 48
10.2.8 4-Word Burst READ Operation-Variable Latency 49
10.2.9 Single-Access Burst READ Operation-Fixed Latency 50
10.2.10 4-Word Burst READ Operation-Fixed Latency 51
10.2.11 READ Burst Suspend 52
10.2.12 Burst READ at End-of-Row (Wrap Off) 53
10.2.13 Burst READ Row Boundary Crossing 54
10.2.14 CE#-Controlled Asynchronous WRITE 55
10.2.15 LB# / UB# Controlled Asynchronous WRITE 56

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10.2.16 WE# - Controlled Asynchronous WRITE 57
10.2.17 Asynchronous WRITE Using ADV# 58
10.2.18 Burst WRITE Operation-Variable Latency Mode 59
10.2.19 Burst WRITE Operation-Fixed Latency Mode 60
10.2.20 Burst WRITE at End of Row (Wrap off) 61
10.2.21 Burst WRITE Row Boundary Crossing 62
10.2.22 Burst WRITE Followed by Burst READ 63
10.2.23 Burst READ Interrupted by Burst READ or WRITE 64
10.2.24 Burst WRITE Interrupted by Burst WRITE or READ–Variable Latency Mode 65
10.2.25 Burst WRITE Interrupted by Burst WRITE or READ-Fixed Latency Mode 66
10.2.26 Asynchronous WRITE Followed by Burst READ 67
10.2.27 Asynchronous WRITE (ADV# LOW) Followed by Burst READ 68
10.2.28 Burst READ Followed By Asynchronous WRITE (WE# - Controlled) 69
10.2.29 Burst READ Followed By Asynchronous WRITE Using ADV# 70
10.2.30 Asynchronous WRITE Followed by Asynchronous READ - ADV# LOW 71
10.2.31 Asynchronous WRITE Followed by Asynchronous READ 72
11. PACKAGE DESCRIPTION 73
11.1 Package Dimension 73
12. REVISION HISTORY 74

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4. PIN CONFIGURATION

4.1 Ball Assignment

	1	2	3	4	5	6
A	LB#	OE#	A0	A1	A2	CRE
B	DQ8	UB#	A3	A4	CE#	DQ0
C	DQ9	DQ10	A5	A6	DQ1	DQ2
D	VSSQ	DQ11	A17	A7	DQ3	VCC
E	VCCQ	DQ12	A21	A16	DQ4	VSS
F	DQ14	DQ13	A14	A15	DQ5	DQ6
G	DQ15	A19	A12	A13	WE#	DQ7
H	A18	A8	A9	A10	A11	A20
J	WAIT	CLK	ADV#	A22	NC	NC

(Top View) Pin Configuration

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5. PIN DESCRIPTION

5.1 Signal Description

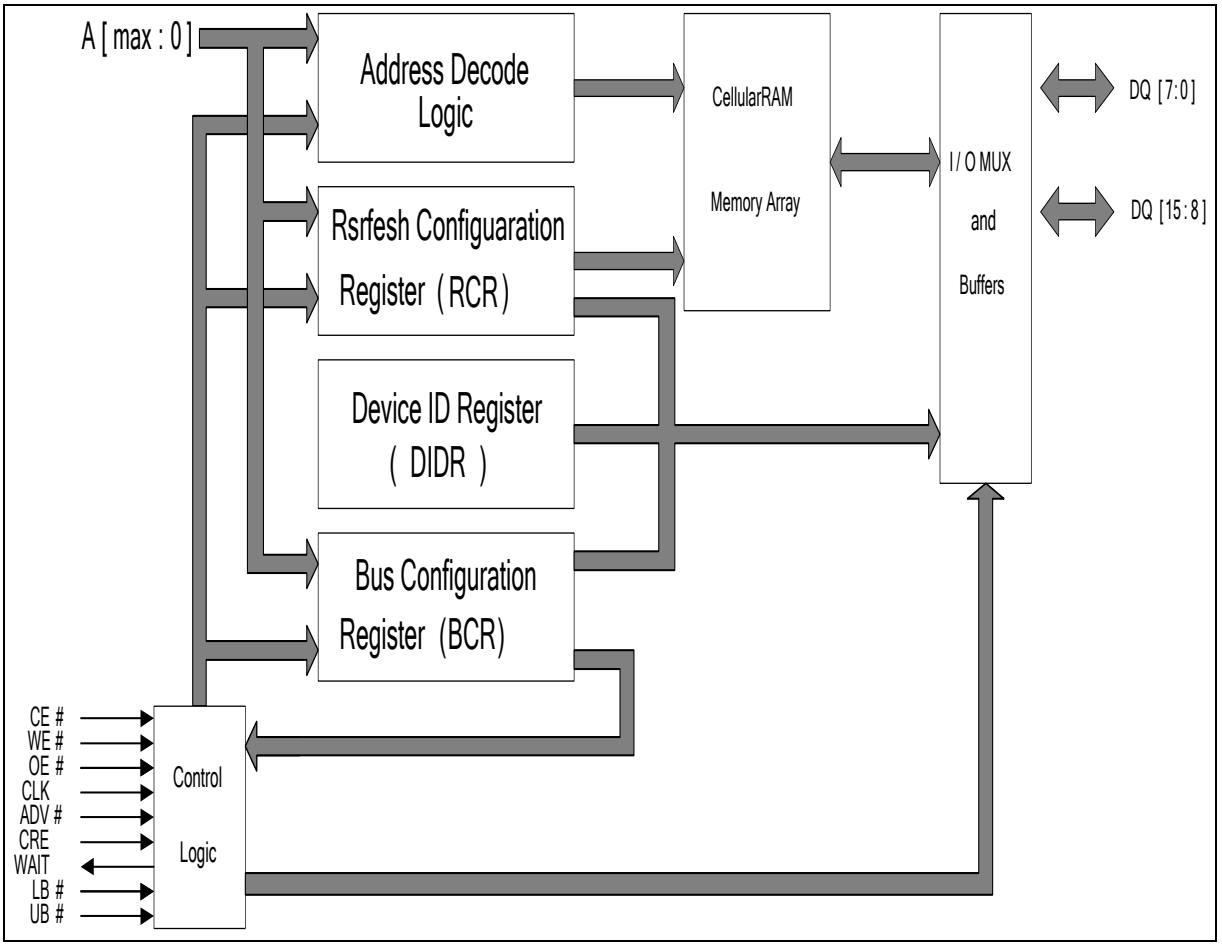
Symbol	Type	Description
A[max:0]	Input	Address inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR. A[max:0] is A[22:0] for 128Mb.
CLK (Note 1)	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static LOW during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations.
ADV# (Note 1)	Input	Address valid: Indicates that a valid address is present on the address inputs. In asynchronous mode, addresses can be latched on the rising edge of ADV# or ADV# can be held LOW. In synchronous mode, addresses are latched on the 1st rising clock edge while ADV# is low. In synchronous mode, the ADV# low pulse width is 1 clock cycle.
CRE	Input	Control register enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations access the RCR, BCR, or DIDR.
CE#	Input	Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode.
OE#	Input	Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
WE#	Input	Write enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array.
LB#	Input	Lower byte enable. DQ[7:0].
UB#	Input	Upper byte enable. DQ[15:8].
DQ[15:0]	Input/Output	Data inputs/outputs.
WAIT (Note 1)	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is also asserted at the end of a row unless wrapping within the burst length. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH.
NC	—	No internal electrical connection is present.
VCC	Supply	Device power supply: power supply for device core operation.
VCCQ	Supply	I/O power supply: power supply for input/output buffers.
VSS	Supply	VSS must be connected to ground.
VSSQ	Supply	VSSQ must be connected to ground.

Note: 1. When using asynchronous mode or page mode exclusively, the CLK and ADV# inputs can be tied to Vss. WAIT will be asserted but should be ignored during asynchronous and page mode operations.

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6. BLOCK DIAGRAM

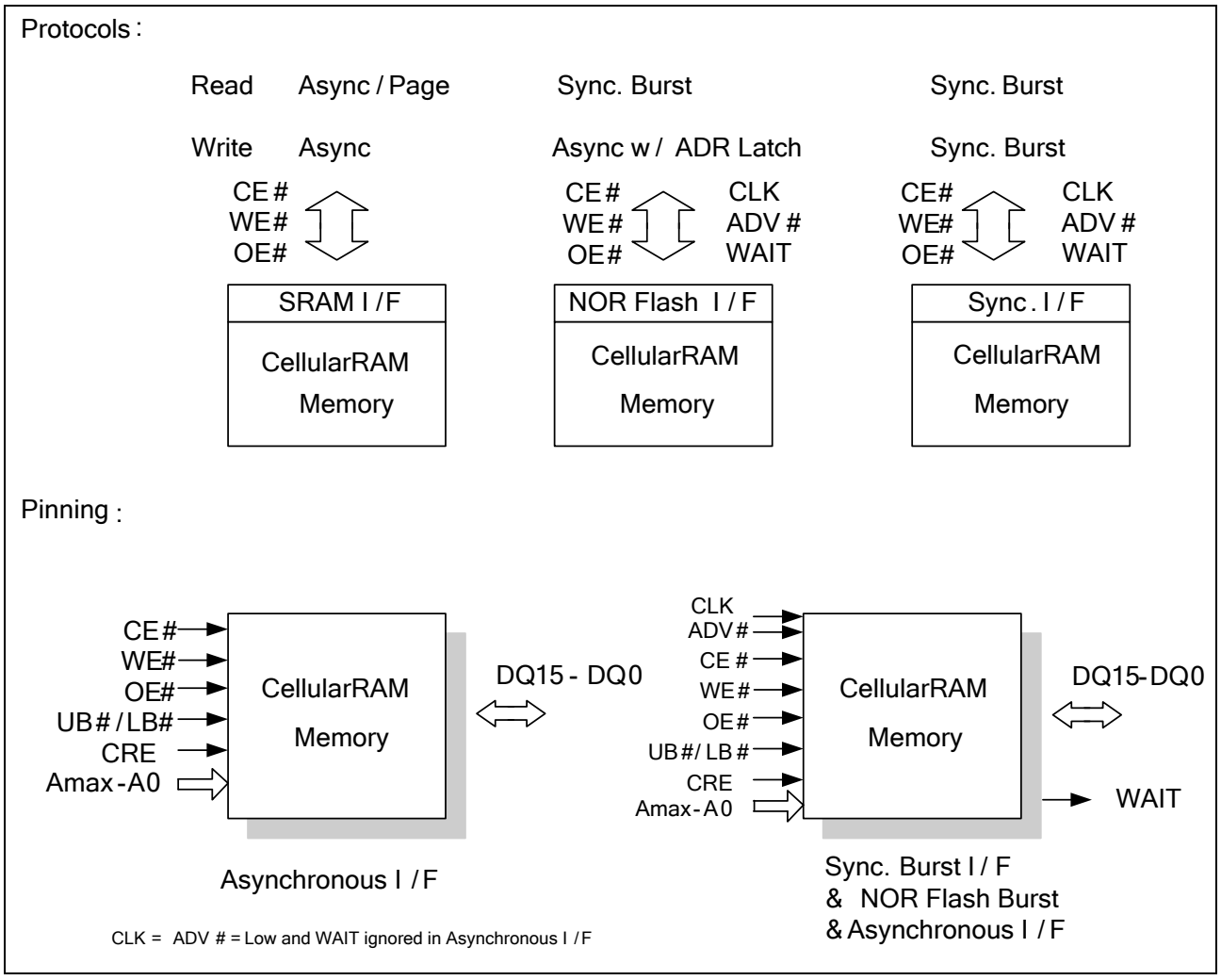
6.1 Block Diagram



Note : Functional block diagrams illustrate simplified device operation. See ball descriptions; bus operations table; and timing diagrams for detailed information.

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6.2 CellularRAM - Interface Configuration Options



7. INSTRUCTION SET

7.1 Bus Operation

Asynchronous Mode BCR [15]=1	Power	CLK*1	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT*2	DQ[15:0]*3	Note
Read	Active	L	L	L	L	H	L	L	Low-Z	Data out	4
Write	Active	L	L	L	X	L	L	L	Low-Z	Data in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5,6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4,6
Configuration register write	Active	L	L	L	H	L	H	X	Low-Z	High-Z	
Configuration register read	Active	L	L	L	L	H	H	L	Low-Z	Config. reg. out	
DPD	Deep power-down	L	X	H	X	X	X	X	High-Z	High-Z	7
Burst Mode BCR [15]=0	**Power**	**CLK*1**	**ADV#**	**CE#**	**OE#**	**WE#**	**CRE**	**LB#/ UB#**	**WAIT*2**	**DQ[15:0]*3**	**Note**
Read	Active	L	L	L	L	H	L	L	Low-Z	Data out	4,8
Write	Active	L	L	L	X	L	L	L	Low-Z	Data in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5,6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4,6
Initial burst read	Active		L	L	X	H	L	L	Low-Z	X	4,9
Initial burst write	Active		L	L	H	L	L	X	Low-Z	X	4,9
Burst continue	Active		H	L	X	X	X	L	Low-Z	Data in or Data out	4,9
Burst suspend	Active	X	X	L	H	X	X	X	Low-Z	High-Z	4,9
Configuration register write	Active		L	L	H	L	H	X	Low-Z	High-Z	9,10
Configuration register read	Active		L	L	L	H	H	L	Low-Z	Config. reg. out	9,10
DPD	Deep power-down	L	X	H	X	X	X	X	High-Z	High-Z	7

Note:
1. CLK must be LOW during asynchronous read and asynchronous write modes; and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. VIN = VCCQ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
7. DPD is initiated when CE# transitions from LOW to HIGH after writing RCR[4] to 0. DPD is maintained until CE# transitions from HIGH to LOW.
8. When the BCR is configured for sync mode, sync READ and WRITE, and async WRITE are supported by all vendors. (Some vendors also support asynchronous READ.)
9. Burst mode operation is initialized through the bus configuration register (BCR[15]).
10. Initial cycle. Following cycles are the same as BURST CONTINUE. CE# must stay LOW for the equivalent of a single-word burst (as indicated by WAIT).

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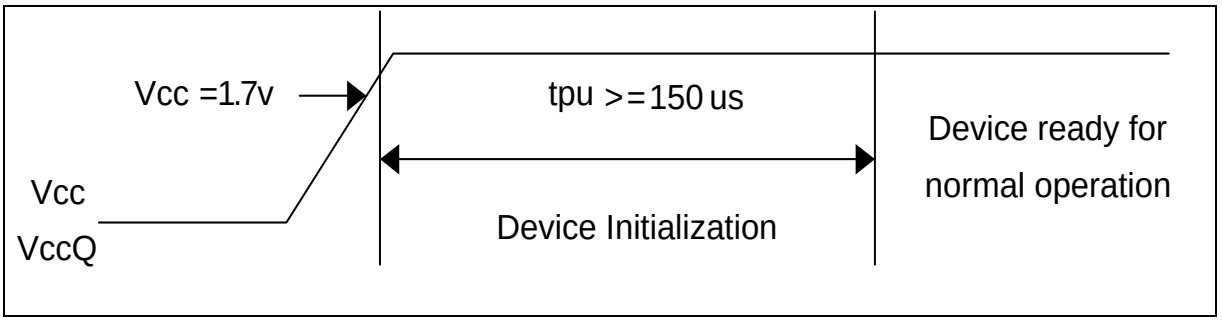
8. FUNCTIONAL DESCRIPTION

In general, CellularRAM devices are high-density alternatives to SRAM and Pseudo SRAM products, popular in low-power, portable applications. The device implements the same high-speed bus interface found on burst mode Flash products. The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

8.1 Power Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings. VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

8.1.1 Power-Up Initialization Timing



8.2 Bus Operating Modes

CellularRAM products incorporate a burst mode interface found on flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR. Page mode is controlled by the refresh configuration register (RCR[7]).

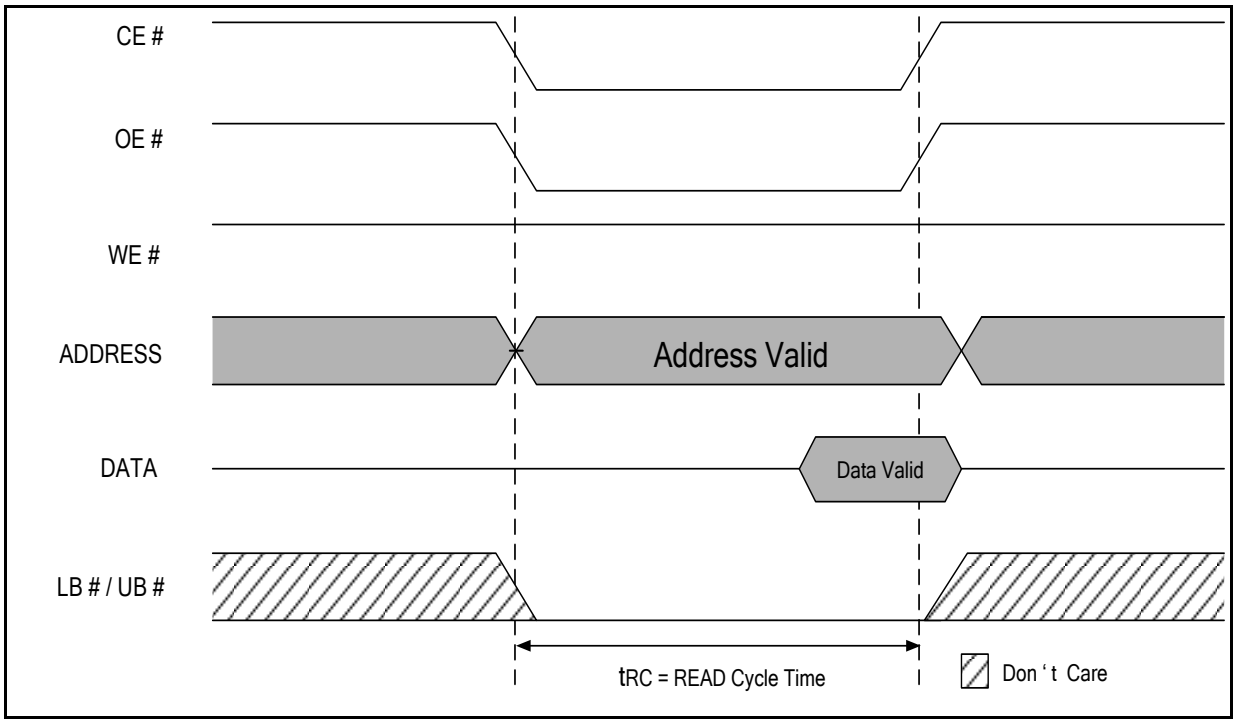
8.2.1 Asynchronous Modes

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry- standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations occur when CE#, WE#, and LB#/UB# are driven LOW. During asynchronous WRITE operations, the OE**#** level is a “don't care,” and WE**#** will override OE**#**. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can either use the ADV input to latch the address, or ADV can be driven LOW during the entire READ/WRITE operation.

During asynchronous operation, the CLK input must be held static LOW. WAIT will be driven while the device is enabled and its state should be ignored. WE# LOW time must be limited to tCEM.

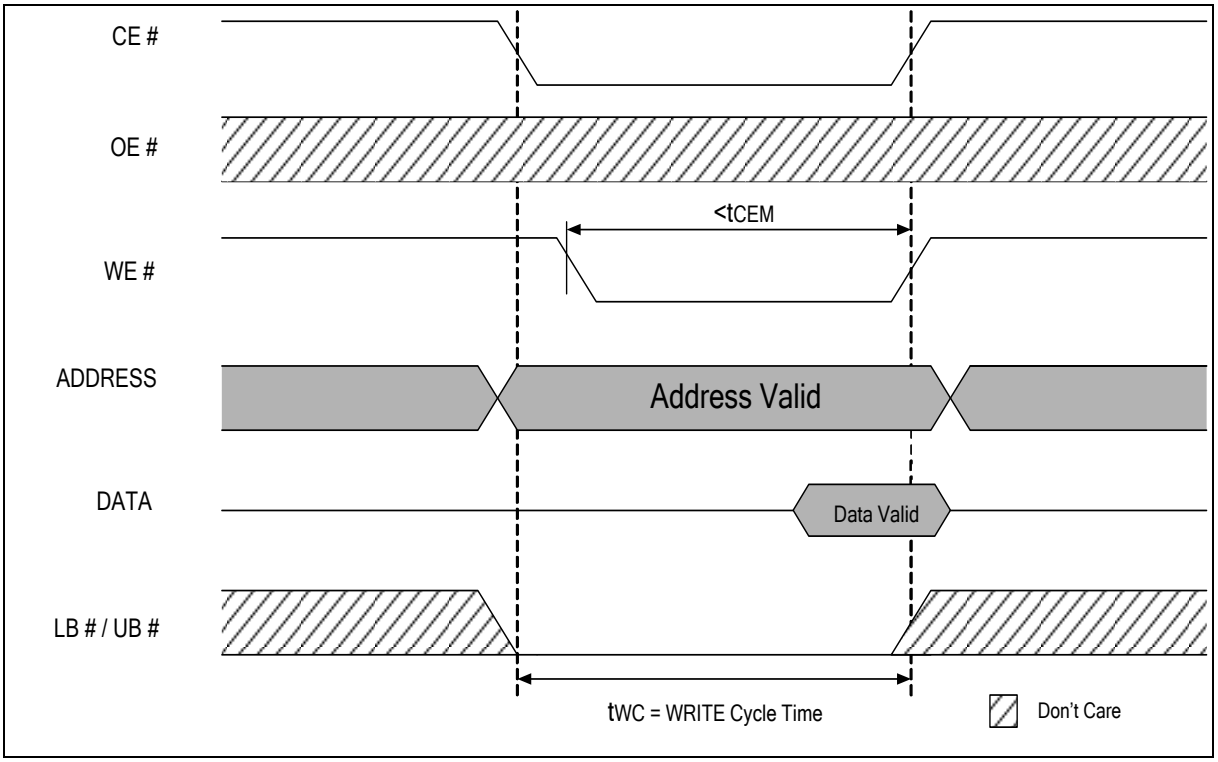
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8.2.1.1 READ Operation(ADV# LOW)



Note : ADV must remain LOW for PAGE MODE operation.

8.2.1.2 WRITE Operation (ADV# LOW)



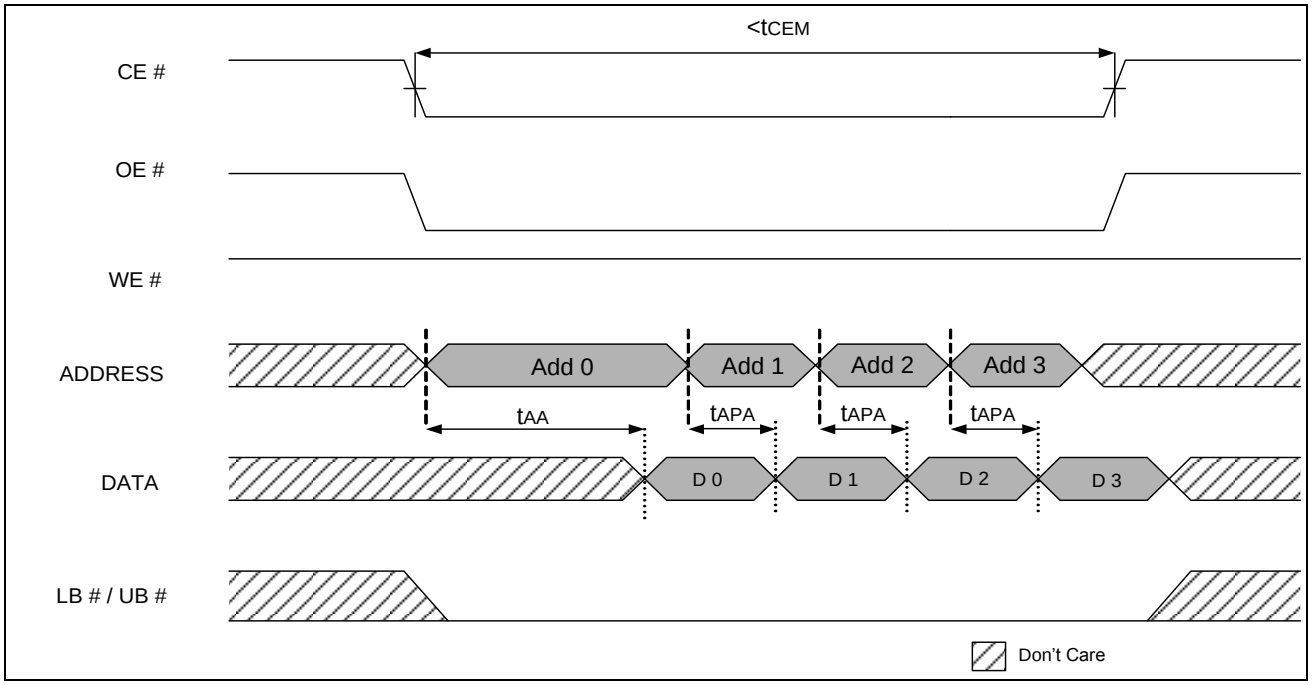
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8.2.2 Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any change in addresses A[4] or higher will initiate a new tAA access time. Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be held LOW. CE# must be driven HIGH upon completion of a page mode access. WAIT will be driven while the device is enabled and its state should be ignored. Page mode is enabled by setting RCR[7] to HIGH. ADV must be driven LOW during all page mode READ accesses. Due to refresh considerations, CE# must not be LOW longer than tCEM.

8.2.2.1 Page Mode READ Operation (ADV# LOW)

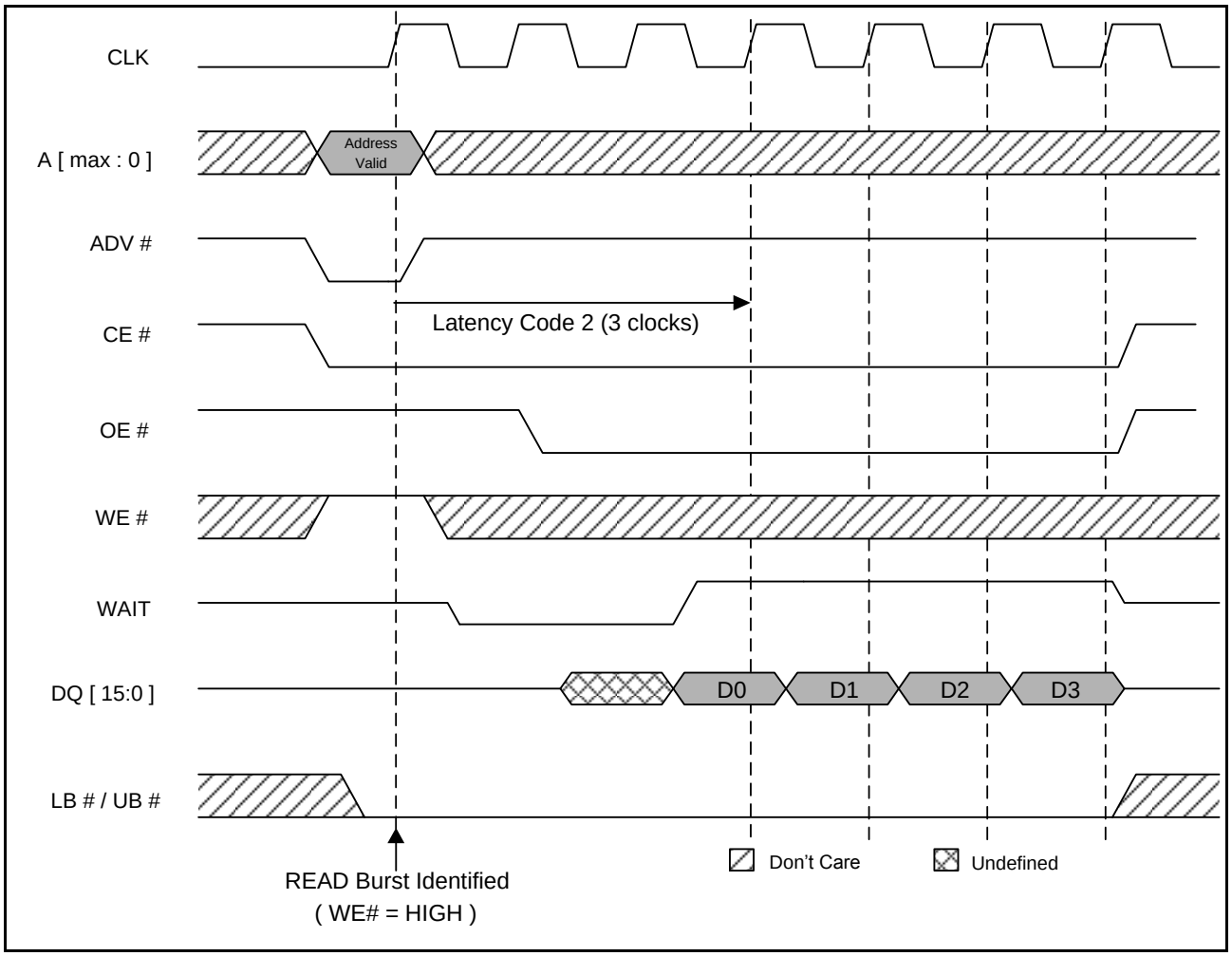


8.2.3 BURST Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the rising edge of the next clock that ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH) or WRITE (WE# =LOW).

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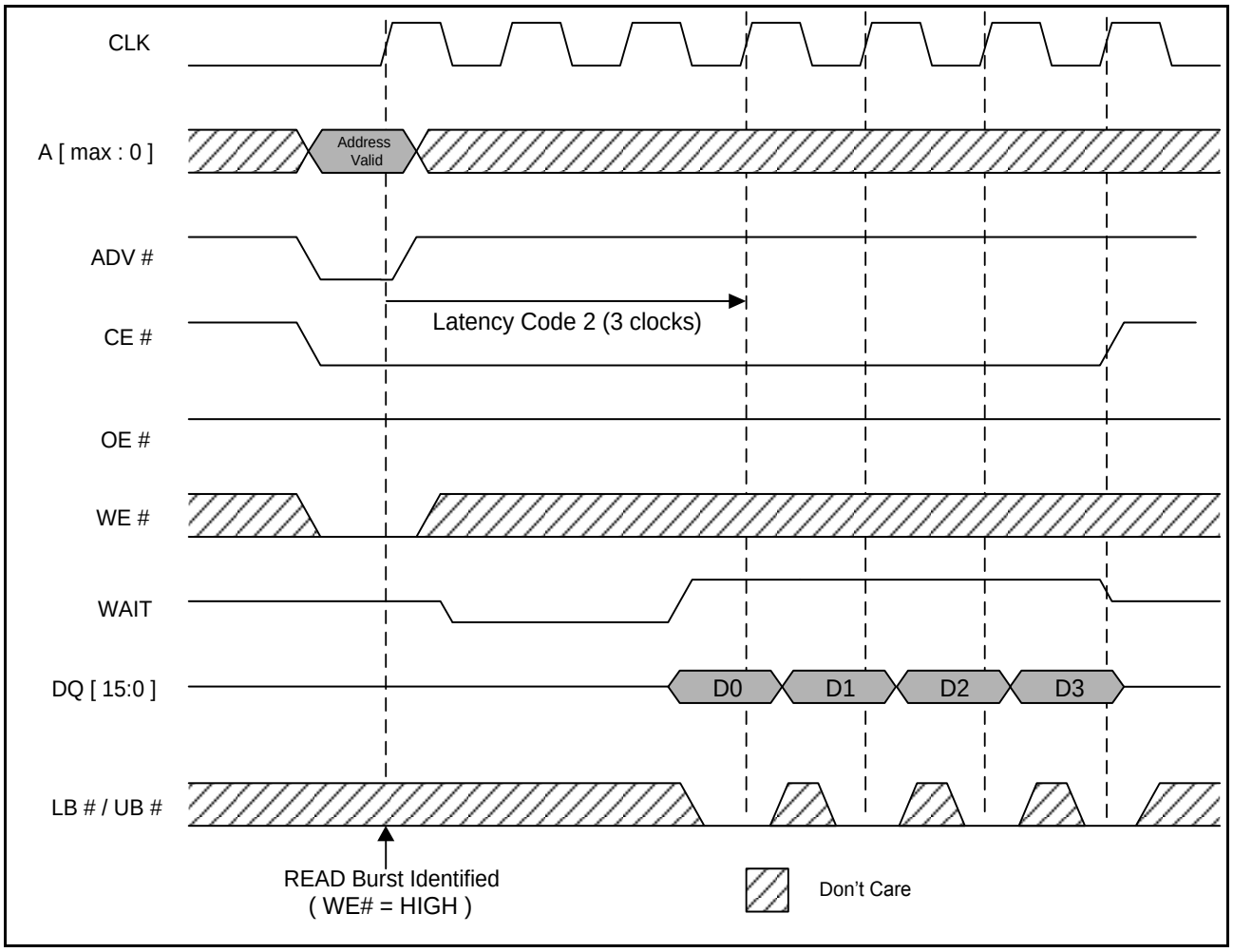
8.2.3.1 Burst Mode READ (4-word burst)



Note : Non-default BCR settings for burst mode READ (4-word burst): Fixed or variable latency; latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay. Diagram is representative of variable latency with no refresh collision or fixed-latency access.

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8.2.3.2 Burst Mode WRITE (4-word burst)



Note : Non-default BCR settings for burst mode WRITE (4-word burst) : Fixed or variable latency; latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

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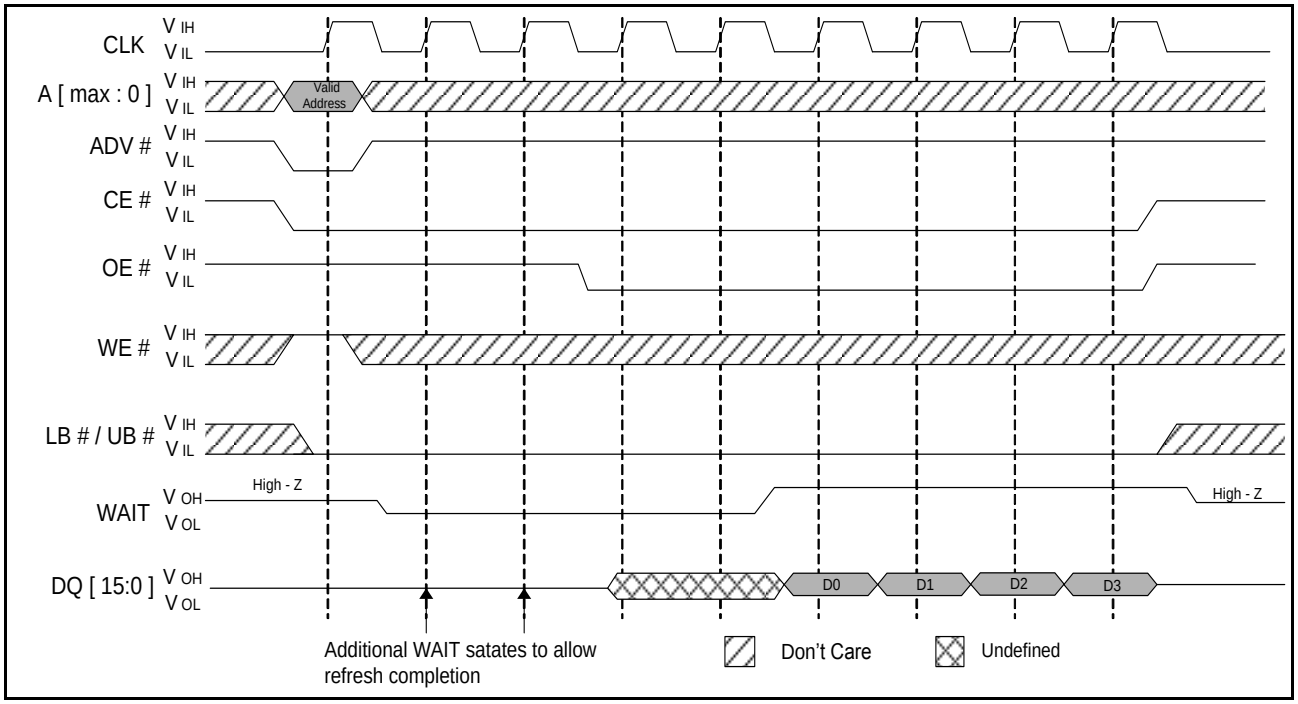
The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of four, eight, sixteen, or thirty-two words. Continuous bursts have the ability to start at a specified address and burst to the end of the row .

The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device. The initial latency for READ operations can be configured as fixed or variable (WRITE operations always use fixed latency). Variable latency allows the CellularRAM to be configured for minimum latency at high clock frequencies, but the controller must monitor WAIT to detect any conflict with refresh cycles. Fixed latency outputs the first data word after the worst-case access delay, including allowance for refresh collisions. The initial latency time and clock speed determine the latency count setting. Fixed latency is used when the controller cannot monitor WAIT. Fixed latency also provides improved performance at lower clock frequencies. The WAIT output asserts when a burst is initiated, and de-asserts to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted at the boundary of the row, unless wrapping within the burst length.

To access other devices on the same bus without the timing penalty of the initial latency for a new burst, burst mode can be suspended. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, OE# should be taken HIGH to disable the CellularRAM outputs; otherwise, OE# can remain LOW. Note that the WAIT output will continue to be active, and as a result no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, OE# is taken LOW, then CLK is restarted after valid data is available on the bus.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than tCEM. If a burst suspension will cause CE# to remain LOW for longer than tCEM, CE# should be taken HIGH and the burst restarted with a new CE# LOW/ADV# LOW cycle.

8.2.3.3 Refresh Collision During Variable-Latency READ Operation



Note : Non-default BCR settings for refresh collision during variable-latency READ operation; latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

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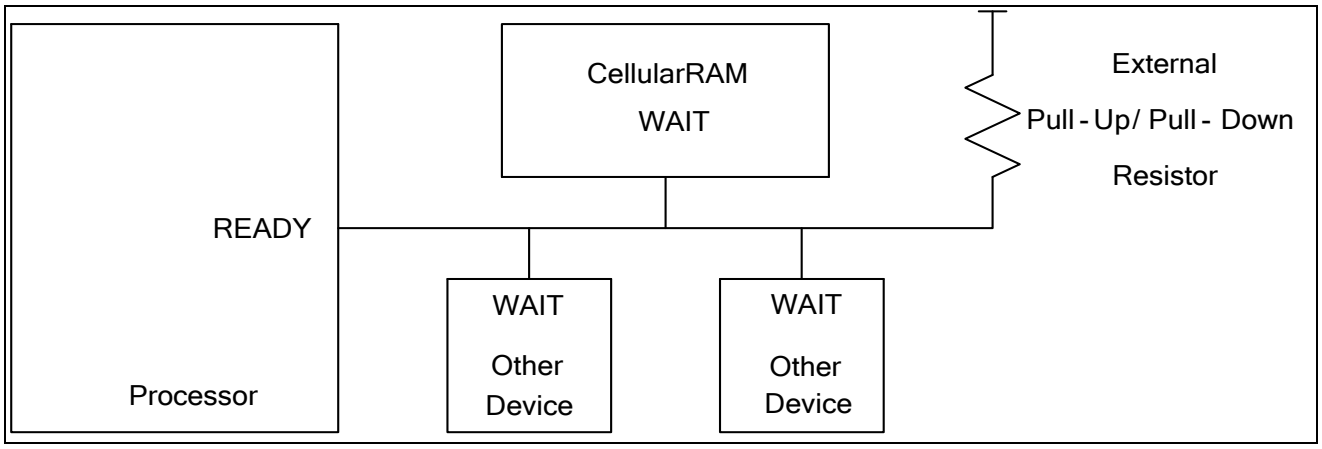
8.2.4 Mixed-Mode Operation

The device supports a combination of synchronous READ and asynchronous READ and asynchronous WRITE operations when the BCR is configured for synchronous operation. The asynchronous READ and asynchronous WRITE operations require that the clock (CLK) remain LOW during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain LOW during the entire asynchronous WRITE operation. CE# can remain LOW when transitioning between mixed-mode operations with fixed latency enabled; however, the CE# LOW time must not exceed tCEM. Mixed-mode operation facilitates a seamless interface to legacy burst mode flash memory controllers.

8.2.4.1 WAIT Operation

The WAIT output on a CellularRAM device is typically connected to a shared, system level WAIT signal. The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

8.2.4.2 Wired-OR WAIT Configuration



Once a READ or WRITE operation has been initiated, WAIT goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the CellularRAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

CE# must remain asserted during WAIT cycles (WAIT asserted and WAIT configuration BCR[8] = 1). Bringing CE# HIGH during WAIT cycles may cause data corruption. (Note that for BCR[8] = 0, the actual WAIT cycles end one cycle after WAIT de-asserts, and at the end of the row the WAIT cycles start one cycle after the WAIT signal asserts.)

When using variable initial access latency (BCR[14] = 0), the WAIT output performs an arbitration role for READ operations launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed. When the refresh operation has completed, the READ operation will continue normally.

WAIT will be asserted but should be ignored during asynchronous READ and WRITE, and page READ operations.

By using fixed initial latency (BCR[14] = 1), this CellularRAM device can be used in burst mode without monitoring the WAIT signal. However, WAIT can still be used to determine when valid data is available at the start of the burst and at the end of the row. If WAIT is not monitored, the controller must stop burst accesses at row boundaries on its own.

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8.2.5 LB#/ UB# Operation

The LB# enable and UB# enable signals support byte-wide data WRITEs. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first. LB# and UB# must be LOW during READ cycles.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

8.3. Low Power Operation

8.3.1 Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is HIGH. The device will enter a reduced power state upon completion of a READ or WRITE operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

8.3.2 Temperature Compensated Refresh

Temperature compensated refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The device continually adjusts the refresh rate to match that temperature.

8.3.3 Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map. READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

8.3.4 Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

DPD can be enabled by writing to the RCR using CRE or the software access sequence; DPD starts when CE# goes HIGH. DPD is disabled the next time CE# goes LOW and stays LOW for at least 10µs.

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8.4 Registers

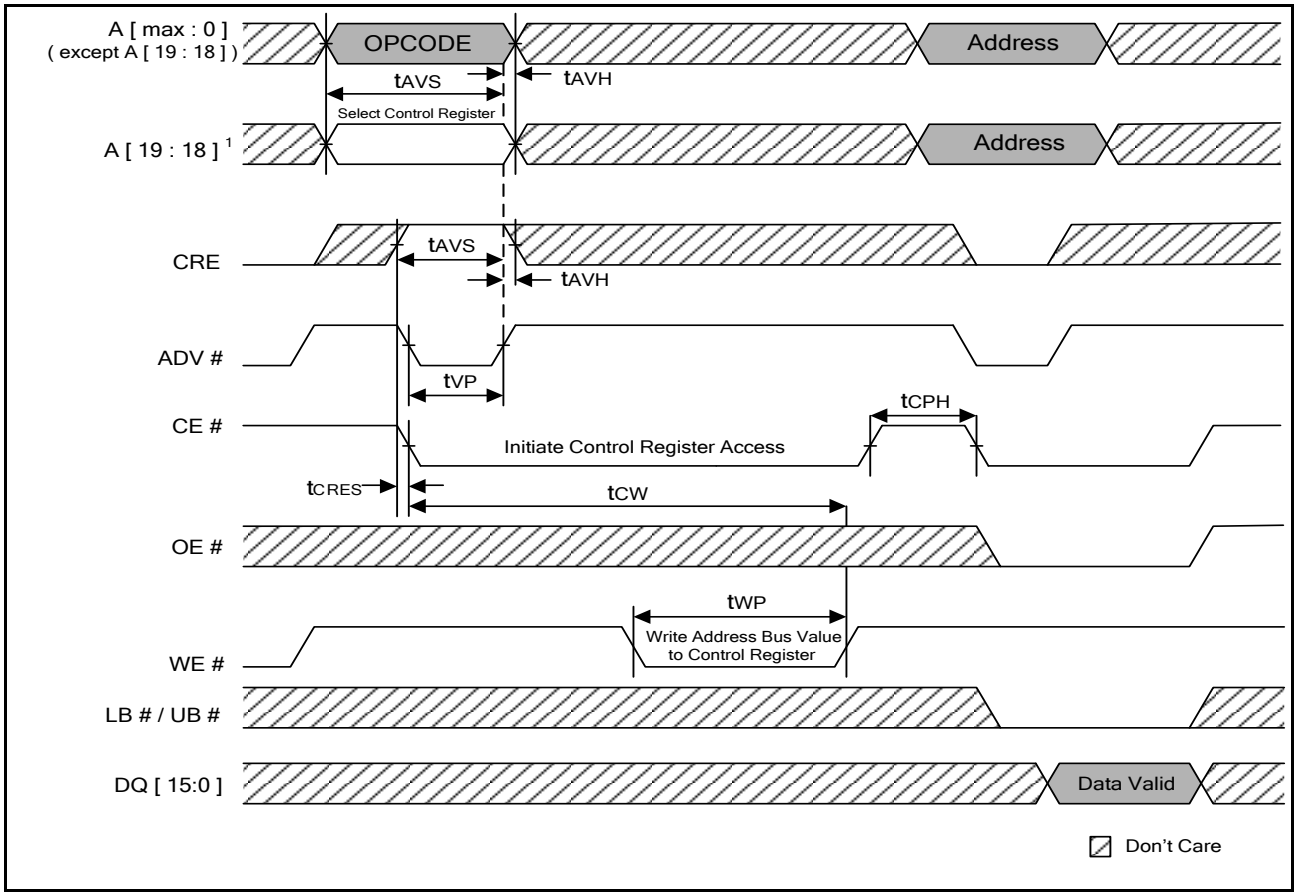
Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state.

A DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. The DIDR is read-only.

8.4.1 Access Using CRE

The registers can be accessed using either a synchronous or an asynchronous operation when the control register enable (CRE) input is HIGH. When CRE is LOW, a READ or WRITE operation will access the memory array. The configuration register values are written via addresses A[max:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are "don't care." The BCR is accessed when A[19:18] are 10b; the RCR is accessed when A[19:18] are 00b. The DIDR is read when A[19:18] are 01b. For reads, address inputs other than A[19:18] are "don't care," and register bits 15:0 are output on DQ[15:0]. Immediately after performing a configuration register READ or WRITE operation, reading the memory array is highly recommended.

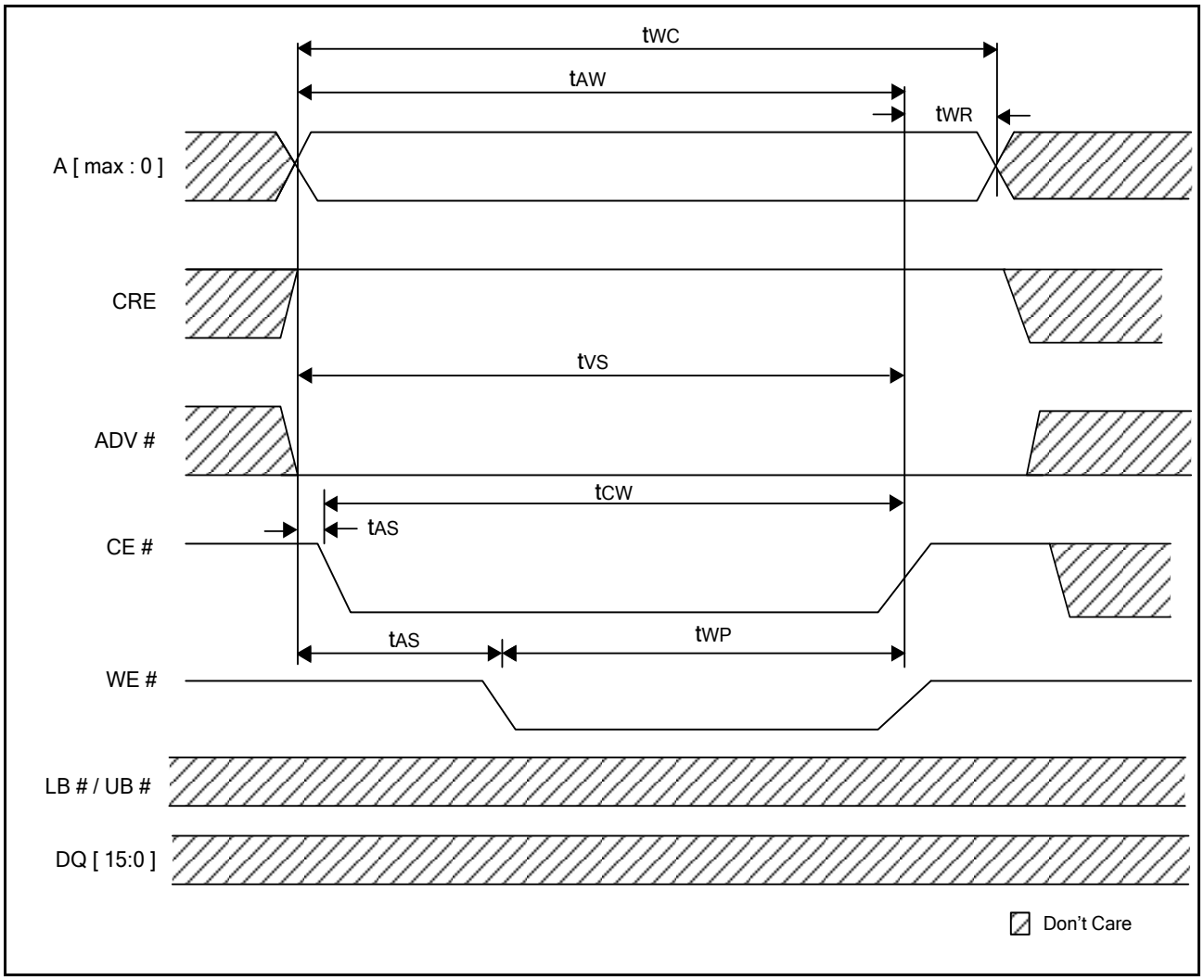
8.4.1.1 Configuration Register WRITE, Asynchronous Mode Followed by READ ARRAY Operation



Note : 1. A[19:18]=00b to load RCR, and 10b to load BCR.

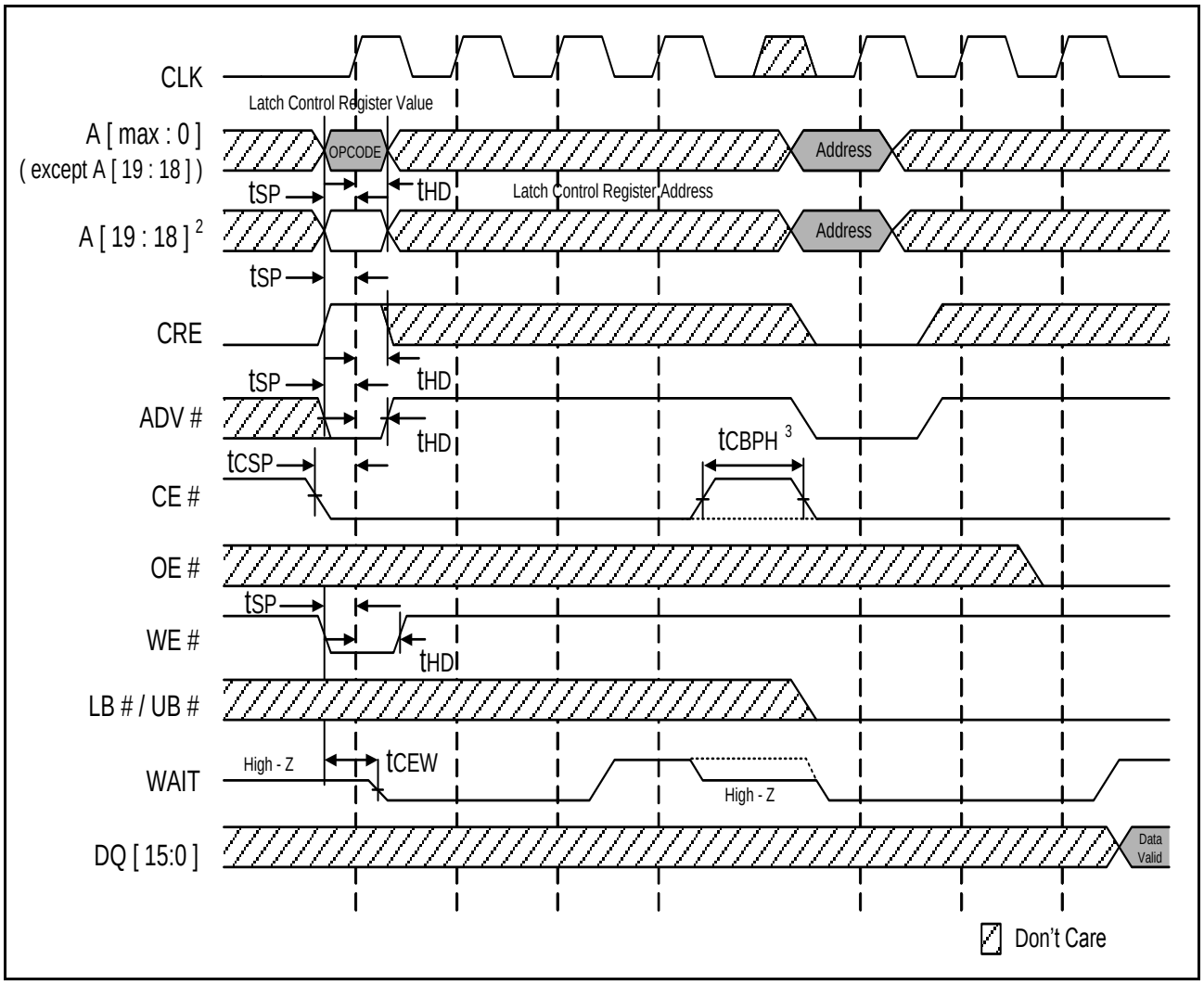
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8.4.1.2 Configuration Register WRITE – CE# control



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8.4.1.3 Configuration Register WRITE, Synchronous Mode Followed by READ ARRAY Operation



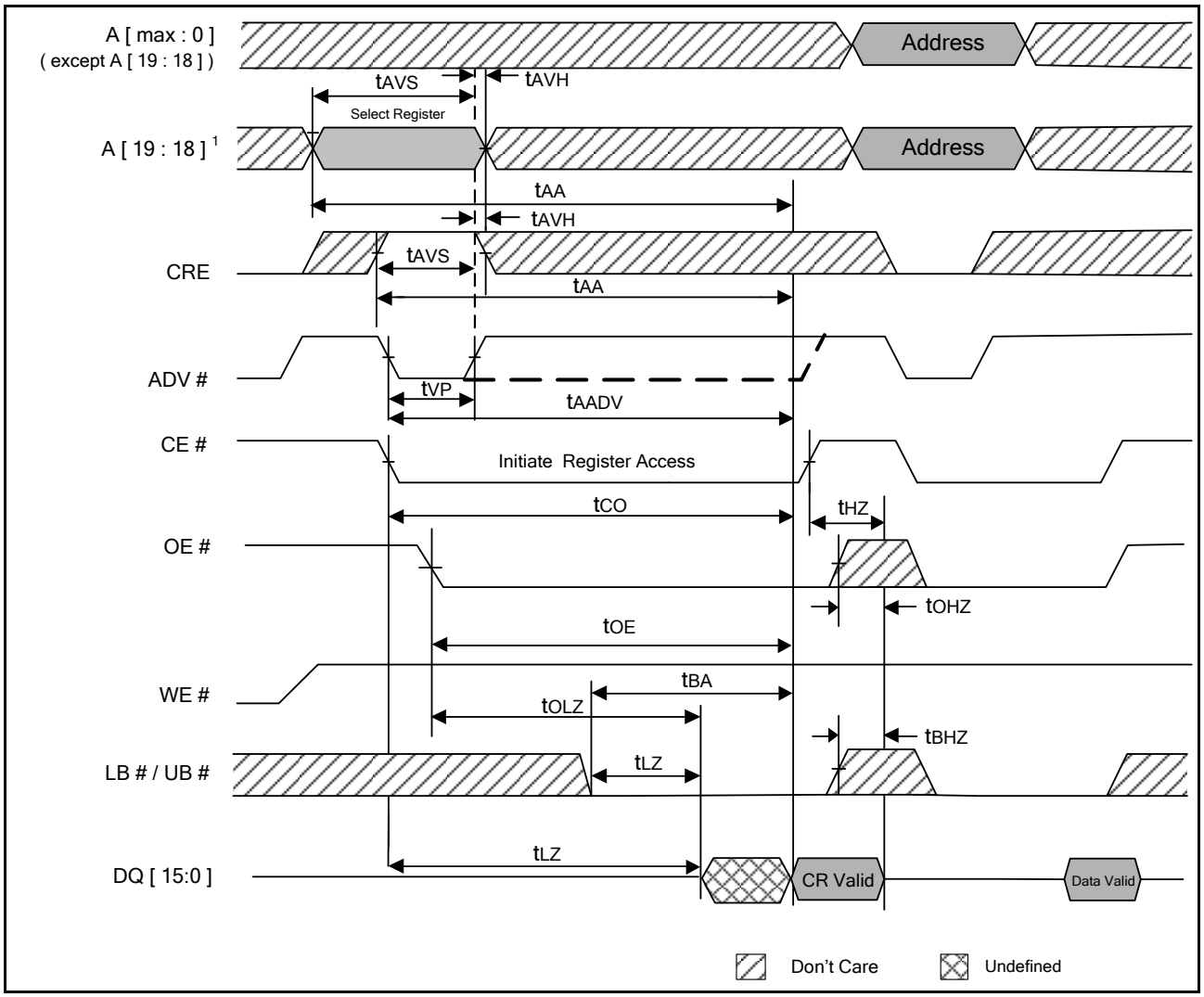
Note : 1. Non-default BCR settings for synchronous mode configuration register WRITE followed by READ ARRAY operation: Latency code 2(3 clocks); WAIT active Low; WAIT asserted during delay.

2. A[19:18] = 00b to load RCR, and 10b to load BCR.

3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored – additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

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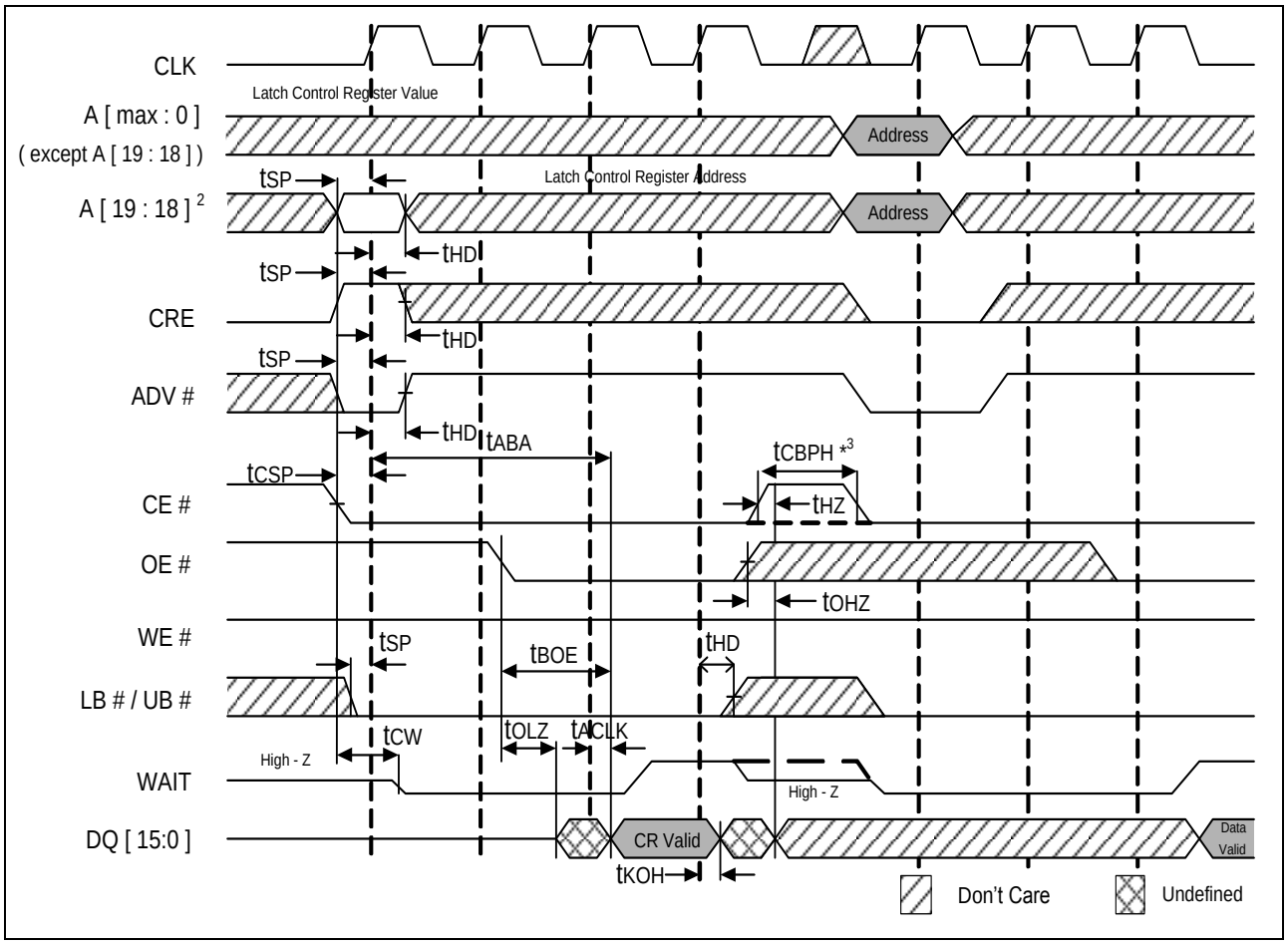
8.4.1.4 Register READ, Asynchronous Mode Followed by READ ARRAY Operation



Note : A[19:18] = 00b to read RCR, 10b to read BCR , and 01b to read DIDR.

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8.4.1.5 Register READ, Synchronous Mode Followed by READ ARRAY Operation



Note : 1. Non-default BCR settings for synchronous mode register READ followed by READ ARRAY operation: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

2. A[19:18] = 00b to read RCR, 10b to read BCR , and 01b to read DIDR.

3. CE# must remain LOW to complete a burst-of-one READ. WAIT must be monitored – additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

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8.4.2 Software Access

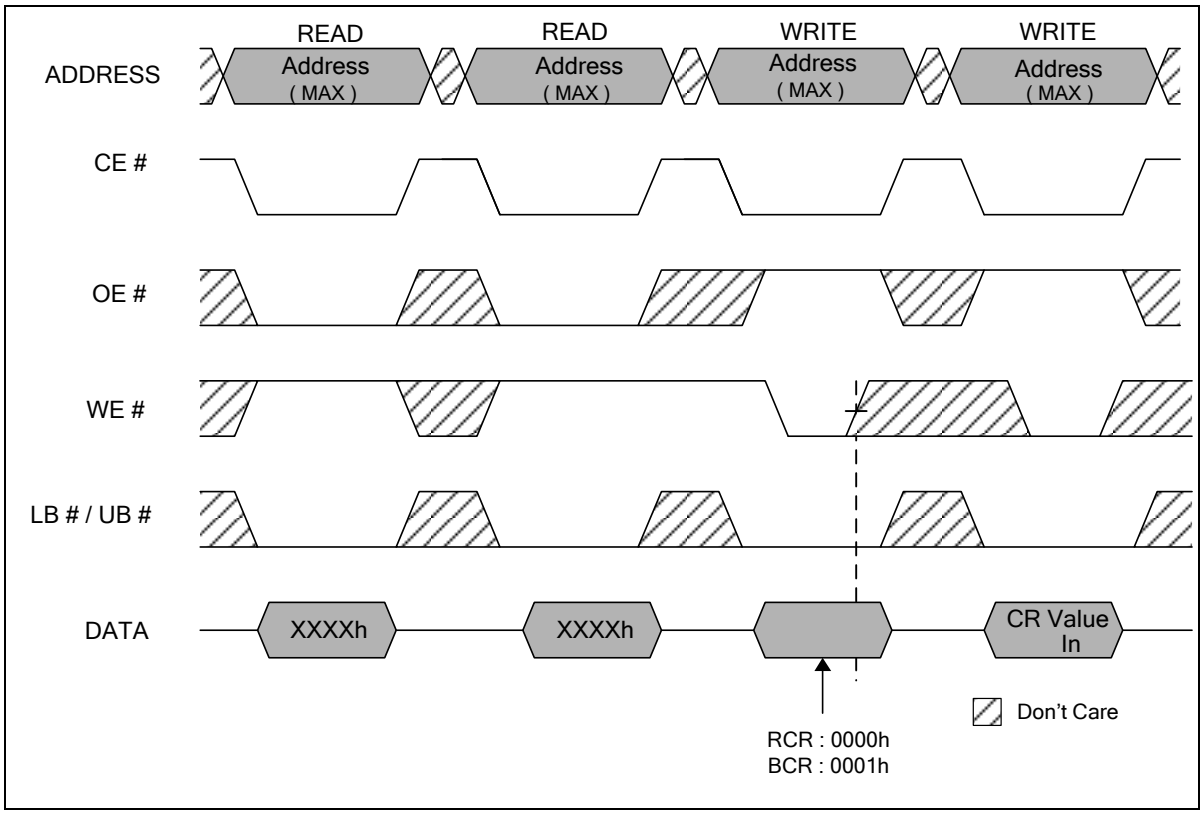
Software access of the registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be modified and all registers can be read using the software sequence.

The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations. The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation. The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed; the contents of this address are not changed by using this sequence.

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR, RCR, or the DIDR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR; if the data is 0002h, the sequence will access the DIDR. During the fourth operation, DQ[15:0] transfer data into or out of bits 15–0 of the registers.

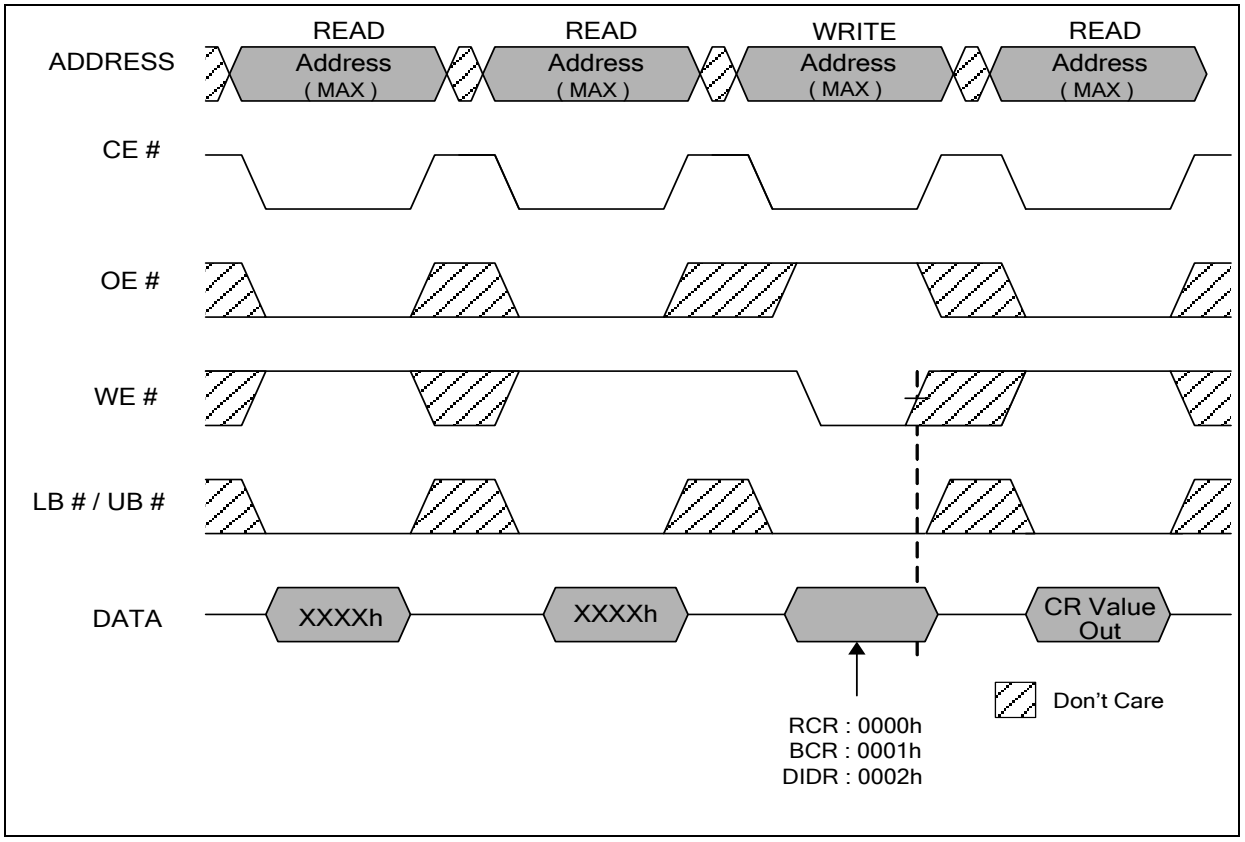
The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for CRE. If the software mechanism is used, CRE can simply be tied to VSS. The port line often used for CRE control purposes is no longer required.

8.4.2.1 Load Configuration Register



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8.4.2.2 Read Configuration Register

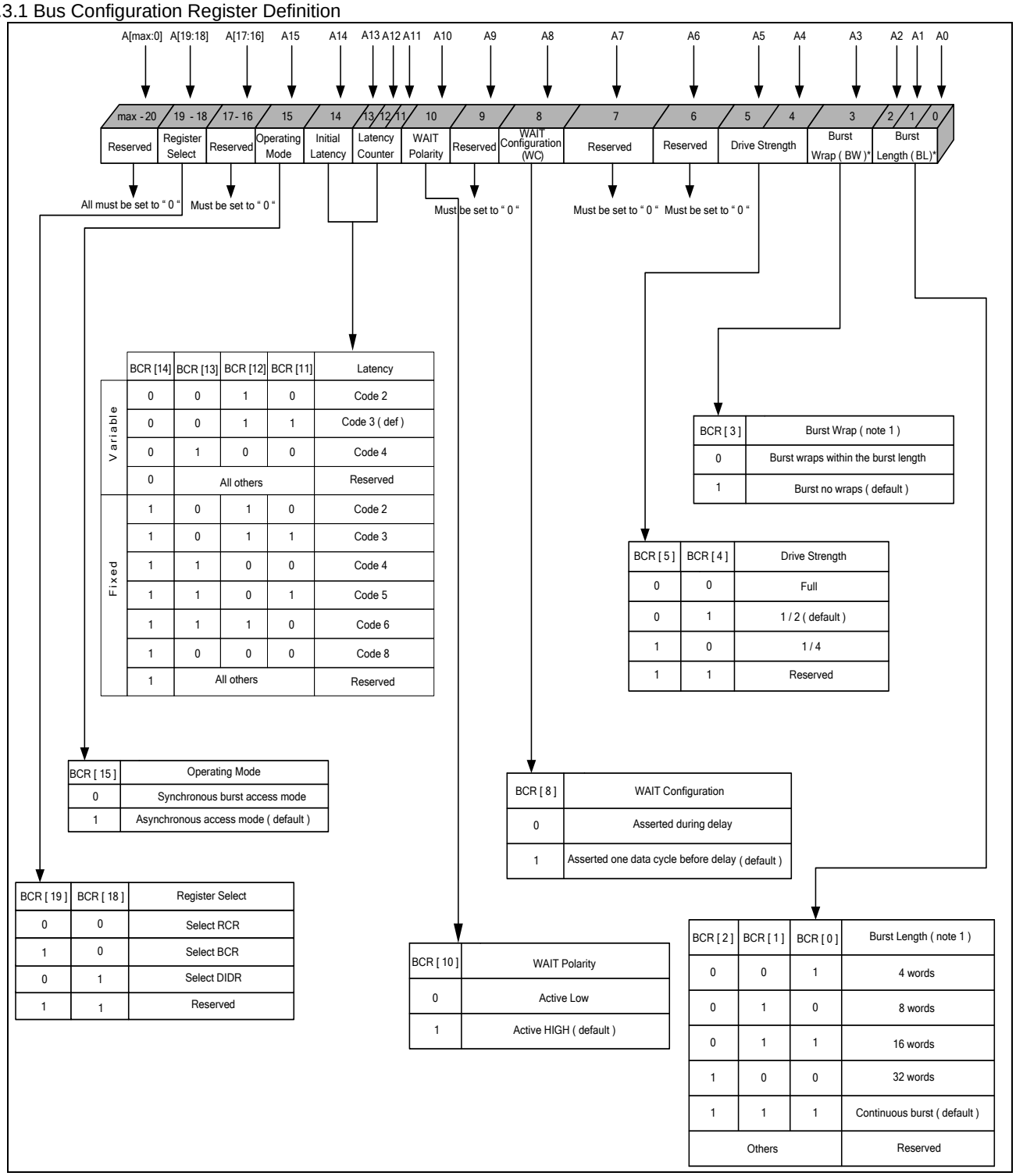


8.4.3 Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. Diagram describes the control bits in the BCR. At power-up, the BCR is set to 9D1Fh. The BCR is accessed with CRE HIGH and A[19:18] = 10b, or through the register access software sequence with DQ = 0001h on the third cycle.

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8.4.3.1 Bus Configuration Register Definition



	BCR [14]	BCR [13]	BCR [12]	BCR [11]	Latency
Variable	0	0	1	0	Code 2
	0	0	1	1	Code 3 (def)
	0	1	0	0	Code 4
	0	All others			Reserved
Fixed	1	0	1	0	Code 2
	1	0	1	1	Code 3
	1	1	0	0	Code 4
	1	1	0	1	Code 5
	1	1	1	0	Code 6
	1	0	0	0	Code 8
	1	All others			Reserved

BCR [3]	Burst Wrap (note 1)
0	Burst wraps within the burst length
1	Burst no wraps (default)

BCR [5]	BCR [4]	Drive Strength
0	0	Full
0	1	1 / 2 (default)
1	0	1 / 4
1	1	Reserved

BCR [15]	Operating Mode
0	Synchronous burst access mode
1	Asynchronous access mode (default)

BCR [8]	WAIT Configuration
0	Asserted during delay
1	Asserted one data cycle before delay (default)

BCR [19]	BCR [18]	Register Select
0	0	Select RCR
1	0	Select BCR
0	1	Select DIDR
1	1	Reserved

BCR [10]	WAIT Polarity
0	Active Low
1	Active HIGH (default)

BCR [2]	BCR [1]	BCR [0]	Burst Length (note 1)
0	0	1	4 words
0	1	0	8 words
0	1	1	16 words
1	0	0	32 words
1	1	1	Continuous burst (default)
Others			Reserved

Note: 1. Burst wrap and length apply to both READ and WRITE operations.

8.4.3.2 Burst Length (BCR[2:0]) Default = Continuous Burst

Burst lengths define the number of words the device outputs during burst READ and WRITE operations. The device supports a burst length of 4, 8, 16, or 32 words. The device can also be set in continuous burst mode where data is accessed sequentially up to the end of the row.

8.4.3.3 Burst Wrap (BCR[3]) Default = No Wrap

The burst-wrap option determines if a 4-, 8-, 16-, or 32-word READ or WRITE burst wraps within the burst length, or steps through sequential addresses. If the wrap option is not enabled, the device accesses data from sequential addresses up to the end of the row.

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8.4.3.4 Sequence and Burst Length

Burst Wrap		Starting Address	4-Word Burst Length	8-Word Burst Length	16-Word Burst Length	32-Word Burst Length	Continuous Burst
BCR[3]	Wrap	(Decimal)	Linear	Linear	Linear	Linear	Linear
0	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-...-29-30-31	0-1-2-3-4-5-6-…
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-...-30-31-0	1-2-3-4-5-6-7-…
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-...-31-0-1	2-3-4-5-6-7-8-…
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-...-0-1-2	3-4-5-6-7-8-9-…
		4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-...-1-2-3	4-5-6-7-8-9-10-…
		5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-...-2-3-4	5-6-7-8-9-10-11-…
		6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-...-3-4-5	6-7-8-9-10-11-12-
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-...-4-5-6	7-8-9-10-11-12-13-…
		...			...	...	...
		14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-...-11-12-13	14-15-16-17-18-19-20-...
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-...-12-13-14	15-16-17-18-19-20-21-...
		...				...	...
		30				30-31-0-...-27-28-29	30-31-32-33-34-...
		31				31-0-1-...-28-29-30	31-32-33-34-35-...
1	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2...--29-30-31	0-1-2-3-4-5-6-…
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-...-30-31-32	1-2-3-4-5-6-7-…
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-...-31-32-33	2-3-4-5-6-7-8-…
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-...-32-33-34	3-4-5-6-7-8-9-…
		4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-...-33-34-35	4-5-6-7-8-9-10-…
		5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-...-15-16-17-18-19-20	5-6-7-...-34-35-36	5-6-7-8-9-10-11…
		6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-...-16-17-18-19-20-21	6-7-8-...-35-36-37	6-7-8-9-10-11-12…
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-...-17-18-19-20-21-22	7-8-9-...-36-37-38	7-8-9-10-11-12-13…
		...			...	...	...
		14			14-15-16-17-18-19-...-23-24-25-26-27-28-29	14-15-16-...-43-44-45	14-15-16-17-18-19-20-…
		15			15-16-17-18-19-20-...-24-25-26-27-28-29-30	15-16-17-...-44-45-46	15-16-17-18-19-20-21-…
		...				...	...
		30				30-31-32-...-59-60-61	30-31-32-33-34-35-36-...
		31				31-32-33-...-60-61-62	31-32-33-34-35-36-37-...

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8.4.3.5 Drive Strength (BCR[5:4]) Default = Outputs Use Half-Drive Strength

The output driver strength can be altered to full, one-half, or one-quarter strength to adjust for different data bus loading scenarios. The reduced-strength options are intended for stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option minimizes the noise generated on the data bus during READ operations. Full output drive strength should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. Outputs are configured at half-drive strength during testing. See the following table for additional information.

8.4.3.6 Drive Length

BCR[5]	BCR[4]	Drive Strength	Impedance Type (Ω)	Use Recommendation
0	0	Full	25–30	CL = 30pF to 50pF
0	1	1/2 (default)	50	CL = 15pF to 30pF
1	0	1/4	100	CL = 15pF or lower
1	1	Reserved		

8.4.3.7 WAIT Signal in Synchronous Burst Mode

The WAIT signal is used in synchronous burst read mode to indicate to the host system when the output data is invalid. Periods of invalid output data within a burst access might be caused either by first access delays, by reaching the end of row, or by self-refresh cycles. To match with the Flash interfaces of different microprocessor types, the polarity and the timing of the WAIT signal can be configured. The polarity can be programmed to either active low or active high logic. The timing of the WAIT signal can be adjusted as well. Depending on the BCR setting, the WAIT signal will be either asserted at the same time the data becomes invalid or it will be set active one clock period in advance. In asynchronous read mode including page mode, the WAIT signal is not used but always stays asserted as BCR bit 10 is specified. In this case, system should ignore WAIT state, since it does not reflect any valid information of data output status.

8.4.3.8 WAIT Config. (BCR[8])

Default = 1 Clk Before Data Valid/Invalid

The WAIT configuration bit is used to determine when WAIT transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the WAIT signal to coordinate data transfer during synchronous READ and WRITE operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after WAIT transitions to the de-asserted or asserted state, respectively. When A8 = 1(default), the WAIT signal transitions one clock period prior to the data bus going valid or invalid.

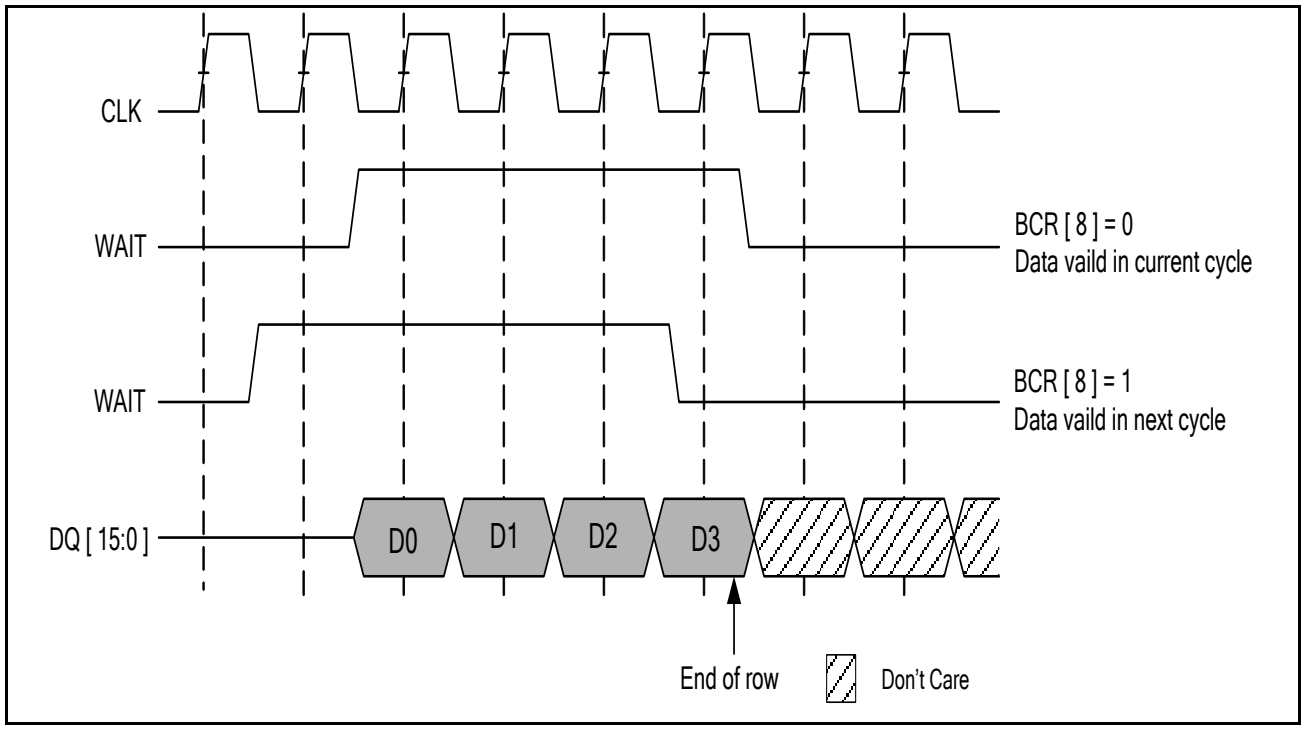
8.4.3.9 WAIT Polarity (BCR[10])

Default = WAIT Active HIGH

The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state. The default value is BCR[10]=1, indicating WAIT active HIGH.

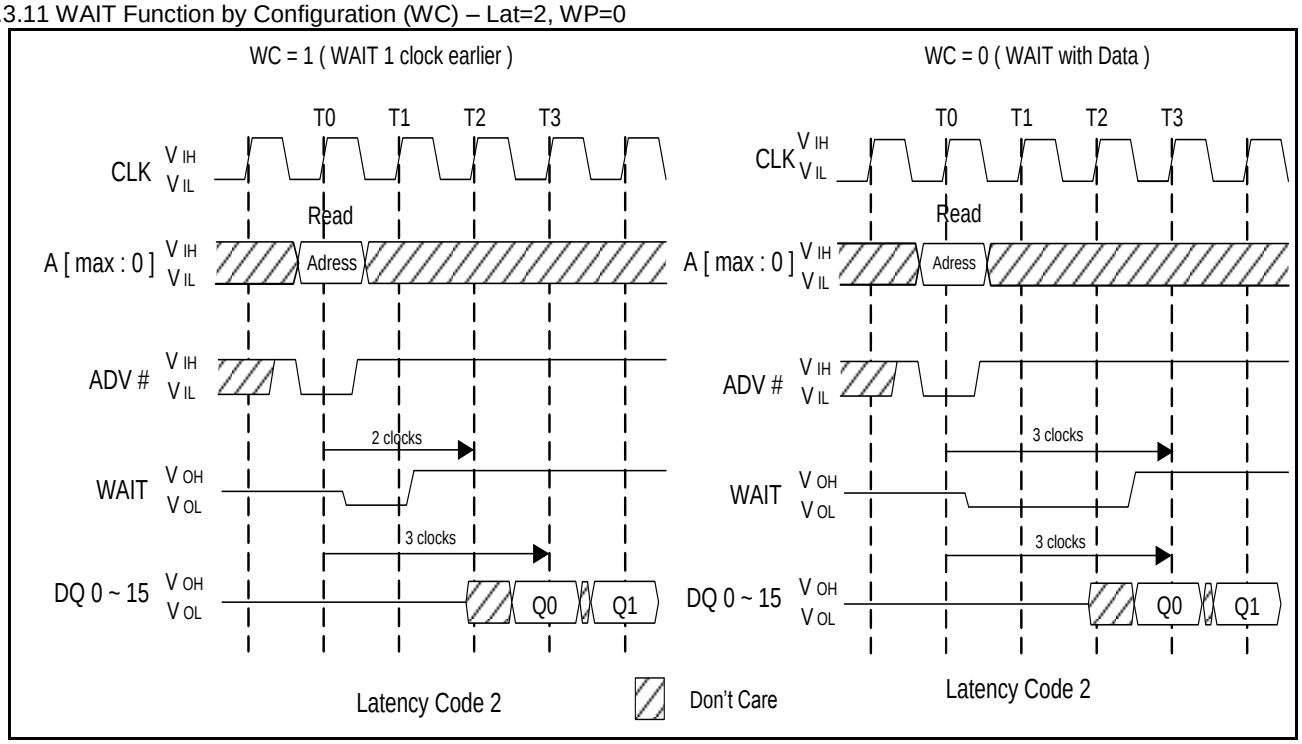
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8.4.3.10 WAIT Configuration During Burst Operation



Note : Non-default BCR setting; WAIT active LOW.

8.4.3.11 WAIT Function by Configuration (WC) – Lat=2, WP=0



8.4.3.12 Latency Counter (BCR[13:11])

Default = Three Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. For allowable latency codes, see the following tables and figures.

8.4.3.13 Initial Access Latency (BCR[14])

Default = Variable

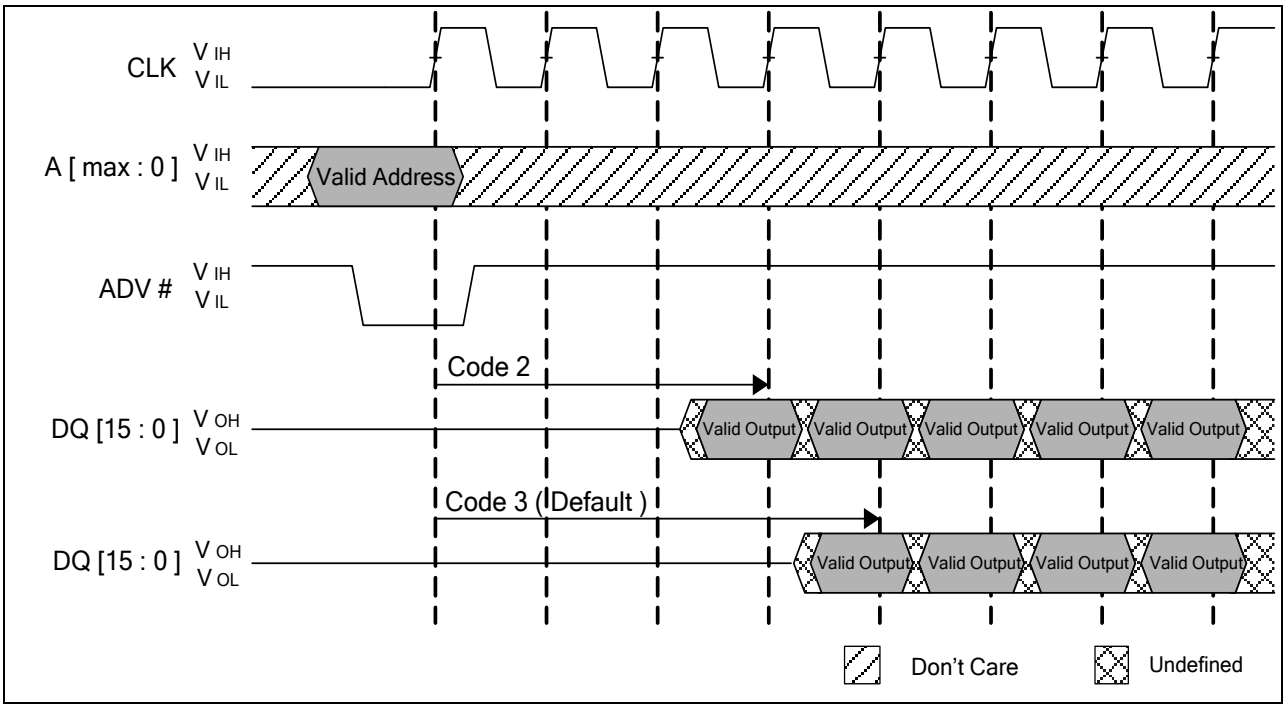
Variable initial access latency outputs data after the number of clocks set by the latency counter. However, WAIT must be monitored to detect delays caused by collisions with refresh operations.
Fixed initial access latency outputs the first data at a consistent time that allows for worst-case refresh collisions. The latency counter must be configured to match the initial latency and the clock frequency. It is not necessary to monitor WAIT with fixed initial latency. The burst begins after the number of clock cycles configured by the latency counter.

8.4.3.14 Allowed Latency Counter Settings in Variable Latency Mode

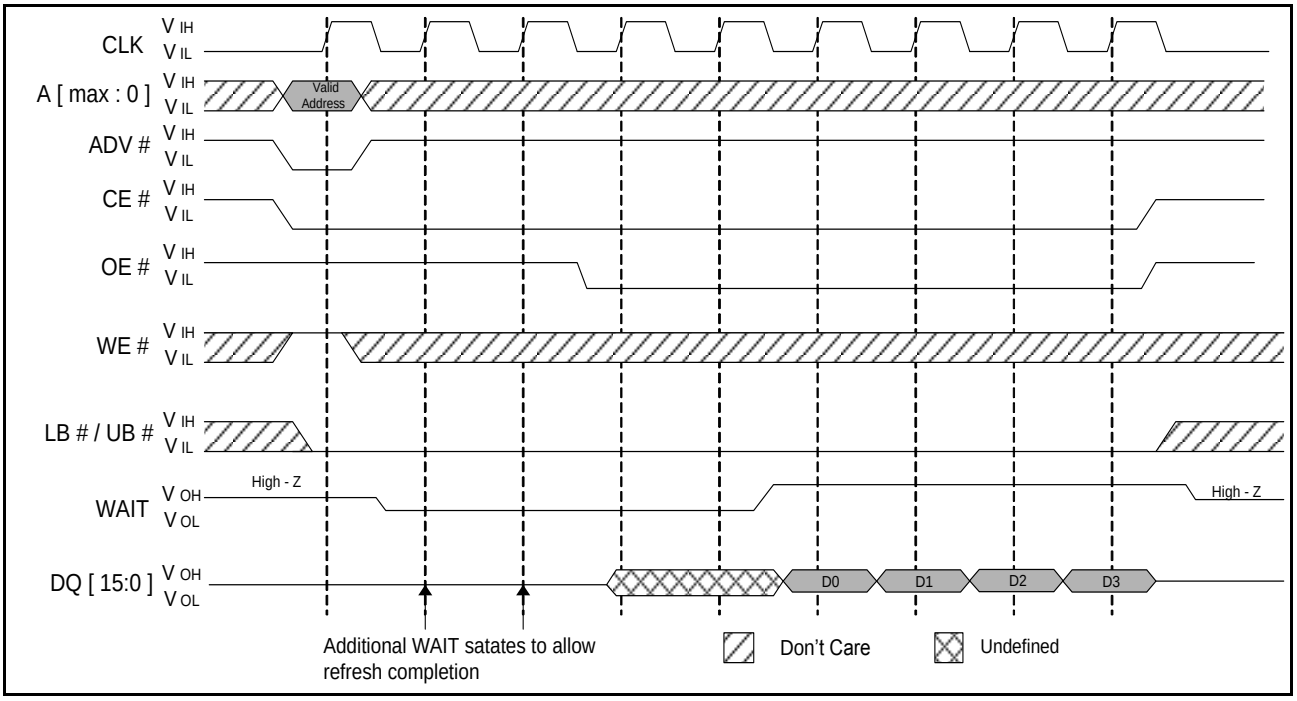
BCR[13:11]	133 MHz Rated CRAM	104MHz Rated CRAM
010	Code 2: Max 66 MHz	Code 2: Max 66 MHz
011	Code 3: Max 104 MHz	Code 3: Max 104 MHz
100	Code 4: Max 133 MHz	Reserved
Others	Reserved	Reserved

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8.4.3.15 Latency Counter (Variable Initial Latency, No Refresh Collision)



8.4.3.16 Latency Counter (Variable Initial Latency, With Refresh Collision)

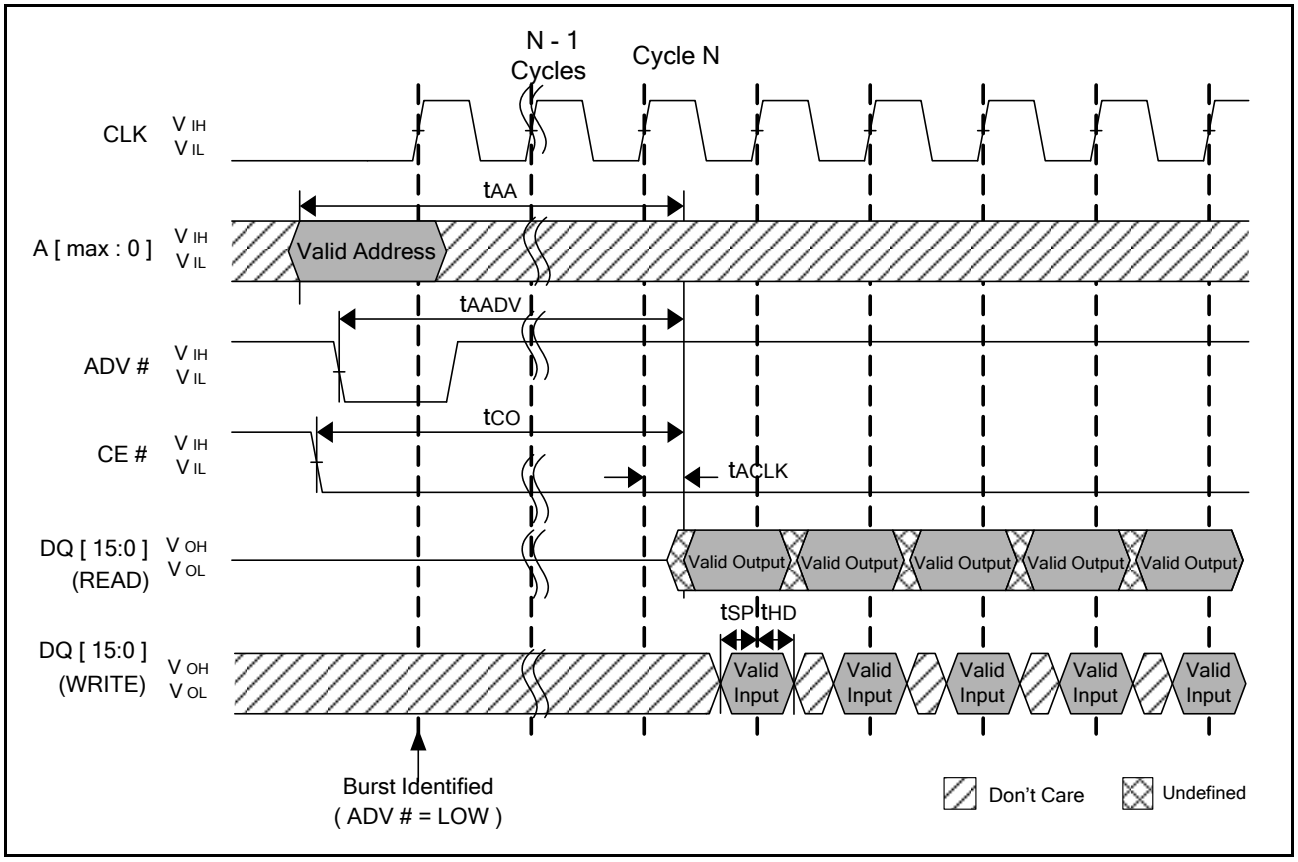


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8.4.3.17 Allowed Latency Counter Settings in Fixed Latency Mode

BCR[13:11]	133MHz Rated CRAM	104MHz Rated CRAM
010	Code 2: Max 33 MHz	Code 2: Max 33 MHz
011	Code 3: Max 52 MHz	Code 3: Max 52 MHz
100	Code 4: Max 66 MHz	Code 4: Max 66 MHz
101	Code 5: Max 75 MHz	Code 5: Max 75 MHz
110	Code 6: Max 104 MHz	Code 6: Max 104 MHz
000	Code 8: Max 133 MHz	Reserved
Others	Reserved	Reserved

8.4.3.18 Latency Counter (Fixed Latency)



8.4.3.19 Burst Write Always Produces Fixed Latency

For burst read, either variable or fixed latency mode is performed depending on BCR.bit14 value. For burst write, only fixed latency mode is performed even if latency mode bit is configured in variable latency (BCR.bit14=0). The fixed latency behavior of a write burst applies to burst initial access.

The controller has to observe maximum *t*CEM (= 4 µs) in case a write burst continues over long bursts. When CE# being held low, no refresh operation can be scheduled properly, so that *t*CEM (= 4 µs) limitation applies.

8.4.3.20 Burst Interrupt

When any burst is complete or needs to be terminated to start new burst, bringing CE# high and back to low in next clock cycle is highly recommended. Burst interrupt means an on-going burst is terminated by newly issued burst initial command without toggling CE#. In this case, special care has to be taken to avoid any malfunction of CellularRAM.

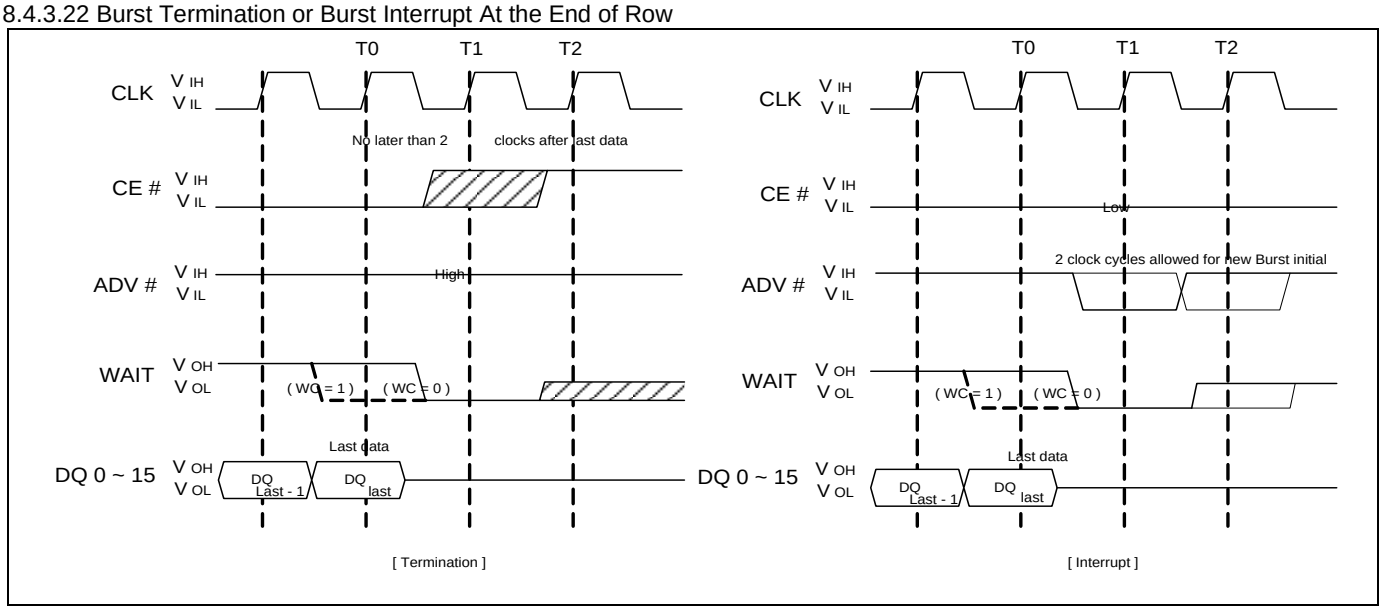
In any case, the burst interrupt is prohibited until the current burst initial command completes the first valid data cycle (first data output or first data input cycle). At new burst initial command, DQ pins go into high-Z if ongoing burst is a read. In case of write burst being interrupted, the data input is masked and will not be updated to the memory location.

8.4.3.21 End-of-Row Condition

The CellularRAM in this design has the row size of 256-word , therefore the end of row condition takes place at every address. In continuous burst mode or wrap-off burst mode, if the burst operation continues over the row boundary, the controller may not to terminate it by bringing CE high or interrupt it by starting a new burst. To indicate the end of row condition, WAIT is asserted from the last data of previous row.

The end of row condition can also be detected (by controller) by tracking the address of ongoing burst, it is available to read out the row size through accessing device ID register (DIDR).

8.4.3.22 Burst Termination or Burst Interrupt At the End of Row



8.4.3.23 Operating Mode (BCR[15]) Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation. Note that when synchronous burst operation is programmed (BCR[15]=1), in addition to synchronous read/write, asynchronous read/write operation is also allowed.

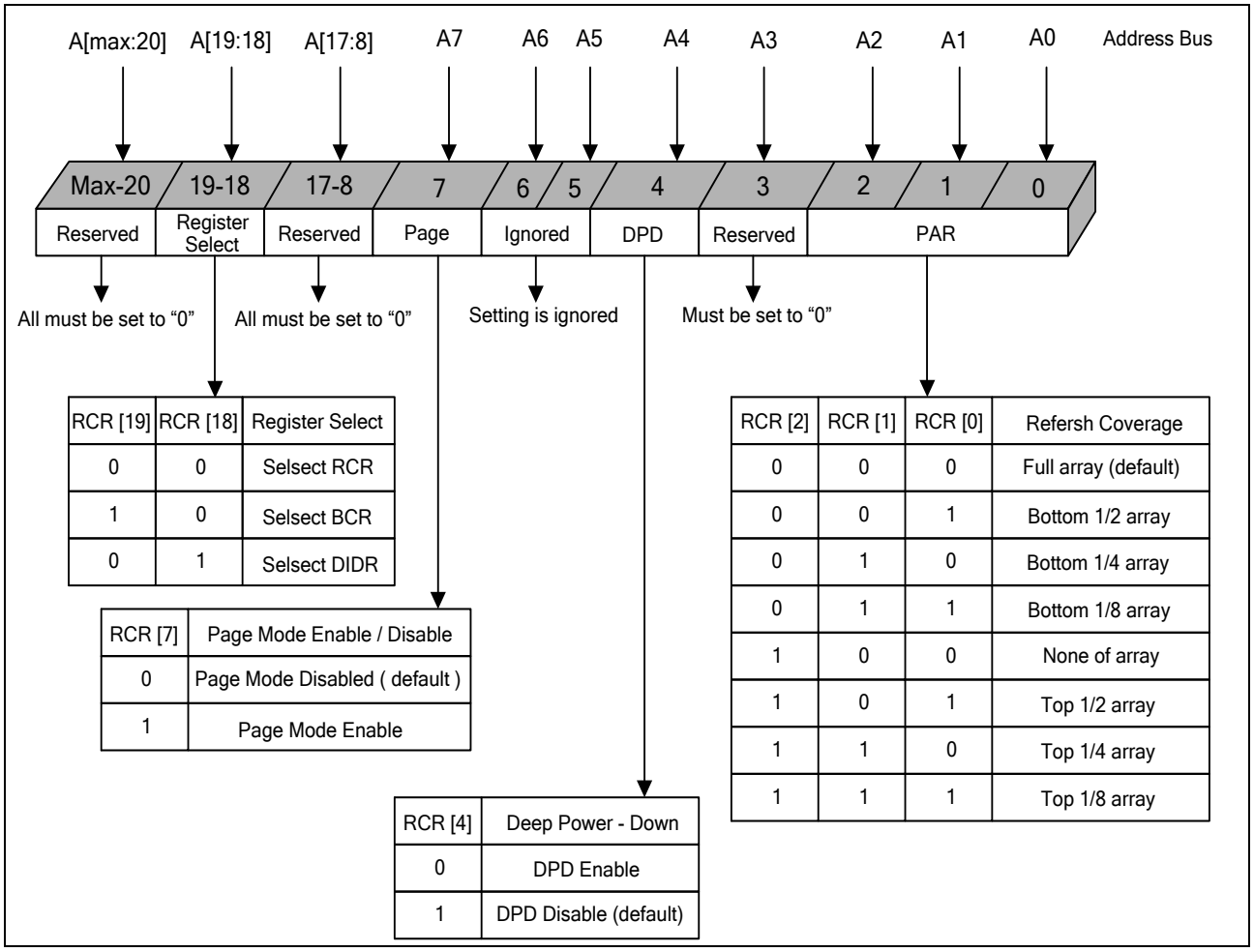
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8.4.4 Refresh Configuration Register

The refresh configuration register (RCR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the RCR.

The RCR is accessed with CRE HIGH and A[19:18] = 00b; or through the register access software sequence with DQ = 0000h on the third cycle.

8.4.4.1 Refresh Configuration Register Mapping



RCR [19]	RCR [18]	Register Select
0	0	Selsect RCR
1	0	Selsect BCR
0	1	Selsect DIDR

RCR [7]	Page Mode Enable / Disable
0	Page Mode Disabled (default)
1	Page Mode Enable

RCR [4]	Deep Power - Down
0	DPD Enable
1	DPD Disable (default)

RCR [2]	RCR [1]	RCR [0]	Refersh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 1/2 array
0	1	0	Bottom 1/4 array
0	1	1	Bottom 1/8 array
1	0	0	None of array
1	0	1	Top 1/2 array
1	1	0	Top 1/4 array
1	1	1	Top 1/8 array

8.4.4.2 Partial Array Refresh (RCR[2:0] Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

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8.4.4.3 Address Patterns for PAR (RCR[4] = 1)

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	000000h–7FFFFFh	8 Meg x 16	128Mb
0	0	1	One-half of die	000000h–3FFFFFh	4 Meg x 16	64Mb
0	1	0	One-quarter of die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	1	1	One-eighth of die	000000h–0FFFFFh	1 Meg x 16	16Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	400000h–7FFFFFh	4 Meg x 16	64Mb
1	1	0	One-quarter of die	600000h–7FFFFFh	2 Meg x 16	32Mb
1	1	1	One-eighth of die	700000h–7FFFFFh	1 Meg x 16	16Mb

8.4.4.4 Deep Power-Down (RCR[4])

Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume.

Deep power-down is enabled by setting RCR[4] = 0 and taking CE# HIGH. DPD can be enabled using CRE or the software sequence to access the RCR. Taking CE# LOW for at least 10µs disables DPD and sets RCR[4] = 1; it is not necessary to write to the RCR to disable DPD. BCR and RCR values (other than BCR[4]) are preserved during DPD.

8.4.4.5 Page Mode Operation (RCR[7])

Default = Disabled

The page mode operation bit determines whether page mode is enabled for asynchronous READ operations. In the power-up default state, page mode is disabled.

8.4.5 Device Identification Register

The DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. This register is read-only.

The DIDR is accessed with CRE HIGH and A[19:18] = 01b, or through the register access software sequence with DQ = 0002h on the third cycle.

8.4.5.1 Device Identification Register Mapping

Bit Field	DIDR[15]		DIDR[14:11]		DIDR[10:8]		DIDR[7:5]		DIDR[4:0]	
Field name	Row length		Device version		Device density		CellularRAM generation		Vendor ID	
Options	Length	Bit Setting	Version	Bit Setting	Density	Bit Setting	Generation	Bit Setting	Vendor	Bit Setting
	Reserved	0b	1st	0000b	16Mb	000b	CR1.5	010b	Winbond	00110b
	256words	1b	2nd	0001b	32Mb	001b	CR2.0	011b		
			...	...	64Mb	010b				
					128Mb	011b				
					256Mb	100b				

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8.4.6 Virtual Chip Enable Function:

A 256Mb device can be implemented by a MCP consisting of two stacked 128Mb devices with Virtual Chip Enable function. By proper configuration, one 128Mb device of the MCP is mapped to the lower 128Mb memory space of the 256Mb device and the another one 128Mb device is mapped to the upper 128Mb memory space of the 256Mb device. The 128Mb device with Virtual Chip Enable function provides a VCE input pin which is controlled by the A23 (the MSB of address bus of 256Mb memory space). When the 128Mb device is mapped to the lower 128Mb memory space, the device will be active if A23 is low. When the 128Mb device is mapped to the upper 128Mb memory space, the device will be active if A23 is high.

9. ELECTRICAL CHARACTERISTIC

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

9.1 Absolute Maximum DC, AC Ratings

Parameter	Min	Max	Unit	Note
Absolute Maximum DC Ratings				
Operating temperature (case) Wireless	-40	85	ºC	
Storage temperature (plastic)	-55	+150	ºC	
Soldering temperature and time 10s (solder ball only)	-	+260	ºC	
Voltage to any ball except VCC, VCCQ relative to VSS	-0.20	+2.3	V	
Voltage on VCC supply relative to VSS	-0.20	+2.3	V	
Voltage on VCCQ supply relative to VSS	-0.20	+2.3	V	
ISH output short circuit current	-	50	mA	1
Absolute Maximum AC Ratings				
Input voltage	-1.0	+2.45	V	2
VCC voltage	-1.0	+2.3	V	3
VCCQ voltage	-1.0	+2.3	V	3

Notes: 1. Input Output shorted for no more than one second. No more than one output shorted at a time. I/O = 1.8V.
2. Assumes absence of clamping diodes. Input voltage overshoot above VCCQ and undershoot below VSSQ should be less than 2V-nS.
3. Condition should be less than 2 nS.

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9.2 Electrical Characteristics and Operating Conditions

Description	Conditions	Symbol	Typical	Min	Max	Unit	Notes
Supply voltage		VCC		1.7	1.95	V	
I/O supply voltage		VCCQ		1.7	1.95	V	
Input high voltage		VIH		VCCQ–0.4	VCCQ+0.2	V	1
Input low voltage		VIL		–0.20	0.4	V	2
Output high voltage	IOH=–0.2mA	VOH		0.8xVCCQ		V	3
Output low voltage	IOL=+0.2mA	VOL			0.2xVCCQ	V	3
Input leakage current	VIN=0toVCCQ	ILI			1	µA	
Output leakage current	OE#=VIH or chip disabled	ILO			1	µA	
Operating Current							
Asynchronous random READ/WRITE	VIN = VCCQ or 0V chip enabled, IOUT=0	ICC1	tRC/tWC=70ns	-	35	mA	4
Asynchronous PAGE READ		ICC1P	tRC=70ns		25	mA	4
Initial access, burst READ/WRITE		ICC2	133MHz	-	45	mA	4
			104MHz	-	40		
Continuous burst READ		ICC3R	133MHz	-	40	mA	4
			104MHz	-	35		
Continuous burst WRITE		ICC3W	133MHz	-	40	mA	4
			104MHz	-	40		
Standby Current	VIN = VCCQ or 0V, CE# = VCCQ	ISB	Standard	-	250	uA	5,6

Note: 1. Input signals may overshoot to VCCQ + 1.0V for periods less than 2ns during transitions.
2. Input signals may undershoot to VSS – 1.0V for periods less than 2ns during transitions.
3. BCR[5:4] = 01b (default setting of one-half drive strength).
4. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
5. ISB (max) values measured with PAR set to FULL ARRAY and at +85°C. In order to achieve low standby current, all inputs must be driven to either VCCQ or VSS. ISB might be slightly higher for up to 500ms after power-up, or when entering standby mode.
6. ISB (typ) is the average ISB at 25°C and VCC = VCCQ = 1.8V. This parameter is verified during characterization, and is not 100% tested.

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9.3 Deep Power-Down Specifications

Description	Conditions	Symbol	Typical	Unit
Deep Power-Down	VIN = VCCQ or 0V; VCC, VCCQ = 1.95V; +85°C	IZZ	10	µA

Note: Typical (TYP) Izz value applies across all operating temperatures and voltages.

9.4 Partial Array Self Refresh Standby Current (Typical Values in µA)

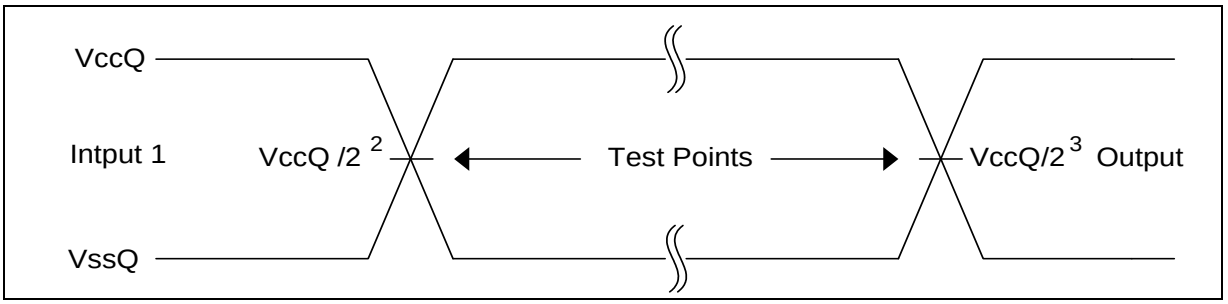
Description	Conditions	Symbol		Array Partition	Max	Unit
Partial-array refresh Standby current	VIN = VCCQ or 0V, CE# = VCCQ	IPAR	Standard power (no designation)	Full	250	uA
				1 / 2	TBD	
				1 / 4	TBD	
				1 / 8	TBD	
				0	TBD	

9.5 Capacitance

Description	Conditions	Symbol	Min	Max	Unit	Note
Input Capacitance	TC = +25ºC; f = 1 MHz; VIN = 0V	CIN	2.0	6	pF	1
Input/Output Capacitance (DQ)		CIO	3.5	6	pF	1

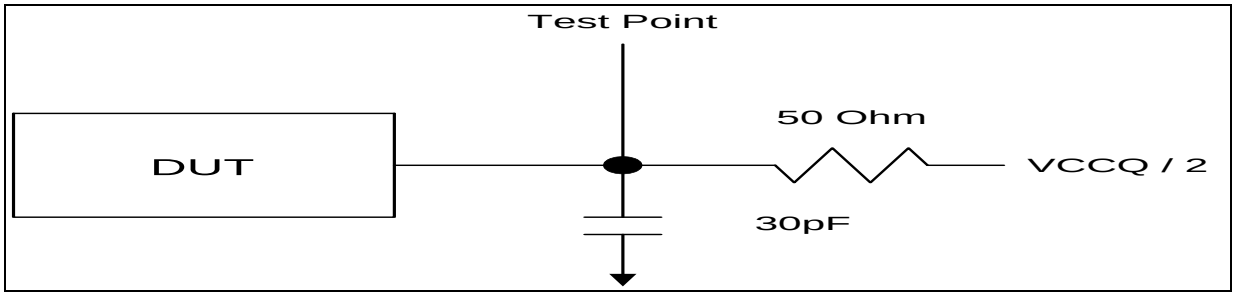
Note: These parameters are verified in device characterization and are not 100% tested.

9.6 AC Input-Output Reference Waveform



Note: 1. AC test inputs are driven at VccQ for a logic 1 and VssQ for a logic 0. Input rise and fall times (10% to 90%) <1.6ns.
2. Input timing begins at VccQ/2.
3. Output timing ends at VccQ/2.

9.7 AC Output Load Circuit



Note: All tests are performed with the outputs configured for default setting of half drive strength (BCR[5:4] = 01b).

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10. TIMING REQUIRMENTS

10.1 Read, Write Timing Requirements

10.1.1 Asynchronous READ Cycle Timing Requirements

All tests performed with outputs configured for default setting of half drive strength, (BCR[5:4] = 01b).

Parameter	Symbol	Min	Max	Unit	Note
Address access time	tAA	-	70	ns	
ADV# access time	tAADV	-	70	ns	
Page access time	tAPA	-	20	ns	
Address hold from ADV# HIGH	tAVH	2	-	ns	
Address setup to ADV# HIGH	tAVS	5	-	ns	
LB#/UB# access time	tBA	-	70	ns	
LB#/UB# disable to DQ High-Z Output	tBHZ	-	8	ns	1
LB#/UB# enable to Low-Z output	tBLZ	6	-	ns	2
Maximum CE# pulse width	tCEM	-	4	µs	3
CE# LOW to WAIT valid	tCEW	1	7.5	ns	
Chip select access time	tCO	-	70	ns	
CE# LOW to ADV# HIGH	tCVS	7	-	ns	
Chip disable to DQ and WAIT High-Z output	tHZ	-	8	ns	1
Chip enable to Low-Z output	tLZ	6	-	ns	2
Output enable to valid output	tOE	-	20	ns	
Output hold from address change	tOH	5	-	ns	
Output disable to DQ High-Z output	tOHZ	-	8	ns	1
Output enable to Low-Z output	tOLZ	3	-	ns	2
Page READ cycle time	tPC	20	-	ns	
READ cycle time	tRC	70	-	ns	
ADV# pulse width LOW	tVP	5	-	ns	

Note: 1.Low-Z to High-Z timings are tested with AC Output Load Circuit. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CCQ}/2$.
2. High-Z to Low-Z timings are tested with AC Output Load Circuit. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CCQ}/2$) level toward either V_{OH} or V_{OL}.
3. Applies to all modes.

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10.1.2 Burst READ Cycle Timing Requirements

All tests performed with outputs configured for default setting of half drive strength, (BCR[5:4] = 01b).

Parameter	Symbol	133MHz		104MHz		Unit	Note
		Min	Max	Min	Max		
Address access time (fixed latency)	tAA		70		70	ns	
ADV# access time (fixed latency)	tAADV		70		70	ns	
Burst to READ access time (variable latency)	tABA		34.75		34.75	ns	
CLK to output delay	tACLK		5.5		7	ns	
Address hold from ADV# HIGH (fixed latency)	tAVH	2		2		ns	
Burst OE# LOW to output delay	tBOE		20		20	ns	
CE# HIGH between subsequent burst or mixed-mode operations	tCBPH	5		5		ns	1
Maximum CE# pulse width	tCEM		4		4	µs	1
CE# or ADV# LOW to WAIT valid	tCEW	1	7.5	1	7.5	ns	
CLK period	tCLK	7.5		9.62		ns	
Chip select access time (fixed latency)	tCO		70		70	ns	
CE# setup time to active CLK edge	tCSP	2.5		3		ns	
Hold time from active CLK edge	tHD	1.5		2		ns	
Chip disable to DQ and WAIT High-Z output	tHZ		7		8	ns	2
CLK rise or fall time	tKHKL		1.2		1.6	ns	
CLK to WAIT valid	tKHTL		5.5		7	ns	
Output HOLD from CLK	tKOH	2		2		ns	
CLK HIGH or LOW time	tKP	3		3		ns	
Output disable to DQ High-Z output	tOHZ		7		8	ns	2
Output enable to Low-Z output	tOLZ	3		3		ns	3
Setup time to active CLK edge	tSP	2		3		ns	

Note: 1. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
2. Low-Z to High-Z timings are tested with the AC Output Load Circuit. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.
3. High-Z to Low-Z timings are tested with the AC Output Load Circuit. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.

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10.1.3 Asynchronous WRITE Cycle Timing Requirements

Parameter	Symbol	Min	Max	Unit	Note
Address and ADV# LOW setup time	tAS	0	-	ns	
Address HOLD from ADV# going HIGH	tAVH	2	-	ns	
Address setup to ADV# going HIGH	tAVS	5	-	ns	
Address valid to end of WRITE	tAW	70	-	ns	
LB#/UB# select to end of WRITE	tBW	70	-	ns	
CE# LOW to WAIT valid	tCEW	1	7.5	ns	
CE# HIGH between subsequent asynchronous operations	tCPH	5	-	ns	
CE# LOW to ADV# HIGH	tCVS	7	-	ns	
Chip enable to end of WRITE	tCW	70	-	ns	
Data HOLD from WRITE time	tDH	0	-	ns	
Data WRITE setup time	tDW	20	-	ns	
Chip disable to WAIT High-Z output	tHZ	-	8	ns	1
Chip enable to Low-Z output	tLZ	10	-	ns	2
End WRITE to Low-Z output	tOW	5	-	ns	2
ADV# pulse width	tVP	5	-	ns	
ADV# setup to end of WRITE	tVS	70	-	ns	
WRITE cycle time	tWC	70	-	ns	
WRITE to DQ High-Z output	tWHZ	-	8	ns	1
WRITE pulse width	tWP	45	-	ns	3
WRITE pulse width HIGH	tWPH	10	-	ns	
WRITE recovery time	tWR	0	-	ns	

Note: 1. Low-Z to High-Z timings are tested with AC Output Load Circuit. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.
2. High-Z to Low-Z timings are tested with AC Output Load Circuit. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.
3. WE# LOW time must be limited to tCEM (4µs).

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10.1.4 Burst WRITE Cycle Timing Requirements

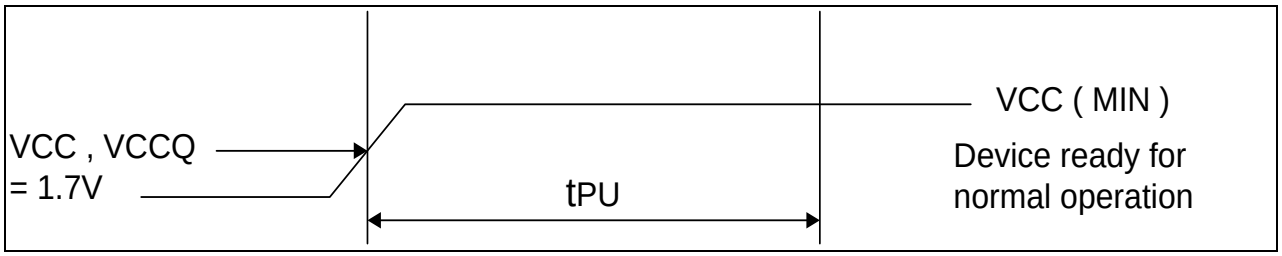
Parameter	Symbol	133MHz		104MHz		Unit	Notes
		Min	Man	Min	Max		
Address and ADV# LOW setup time	tAS	0		0		ns	1
Address HOLD from ADV# HIGH (fixed latency)	tAVH	2		2		ns	
CE# HIGH between subsequent burst or mixed-mode operations	tCBPH	5		5		ns	2
Maximum CE# pulse width	tCEM		4		4	µs	2
CE# LOW to WAIT valid	tCEW	1	7.5	1	7.5	ns	
Clock period	tCLK	7.5		9.62		ns	
CE# setup to CLK active edge	tCSP	2.5		3		ns	
Hold time from active CLK edge	tHD	1.5		2		ns	
Chip disable to WAIT High-Z output	tHZ		7		8	ns	3
CLK rise or fall time	tKHKL		1.2		1.6	ns	
Clock to WAIT valid	tKHTL		5.5		7	ns	
CLK HIGH or LOW time	tKP	3		3		ns	
Setup time to activate CLK edge	tSP	2		3		ns	

Note: 1. tAS required if tCSP > 20ns.
2. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
3. Low-Z to High-Z timings are tested with the AC Output Load circuit. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.

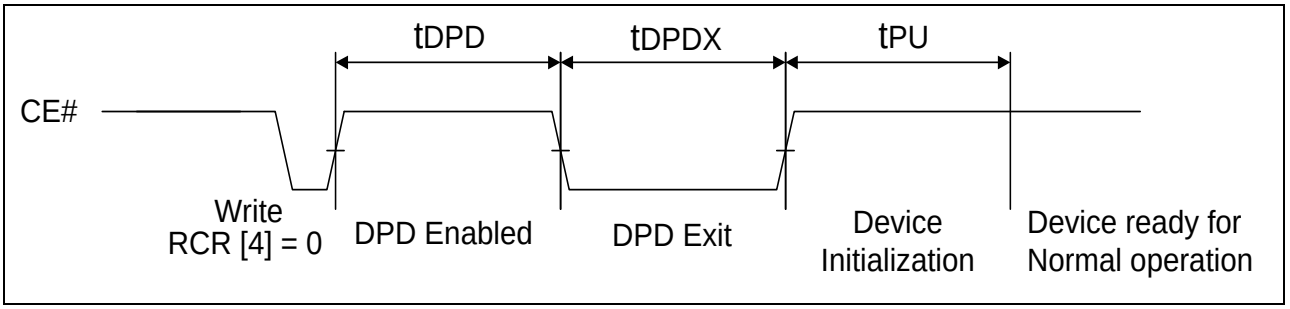
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10.2 TIMING DIAGRAMS

10.2.1 Initialization Period



10.2.2 DPD Entry and Exit Timing Parameters

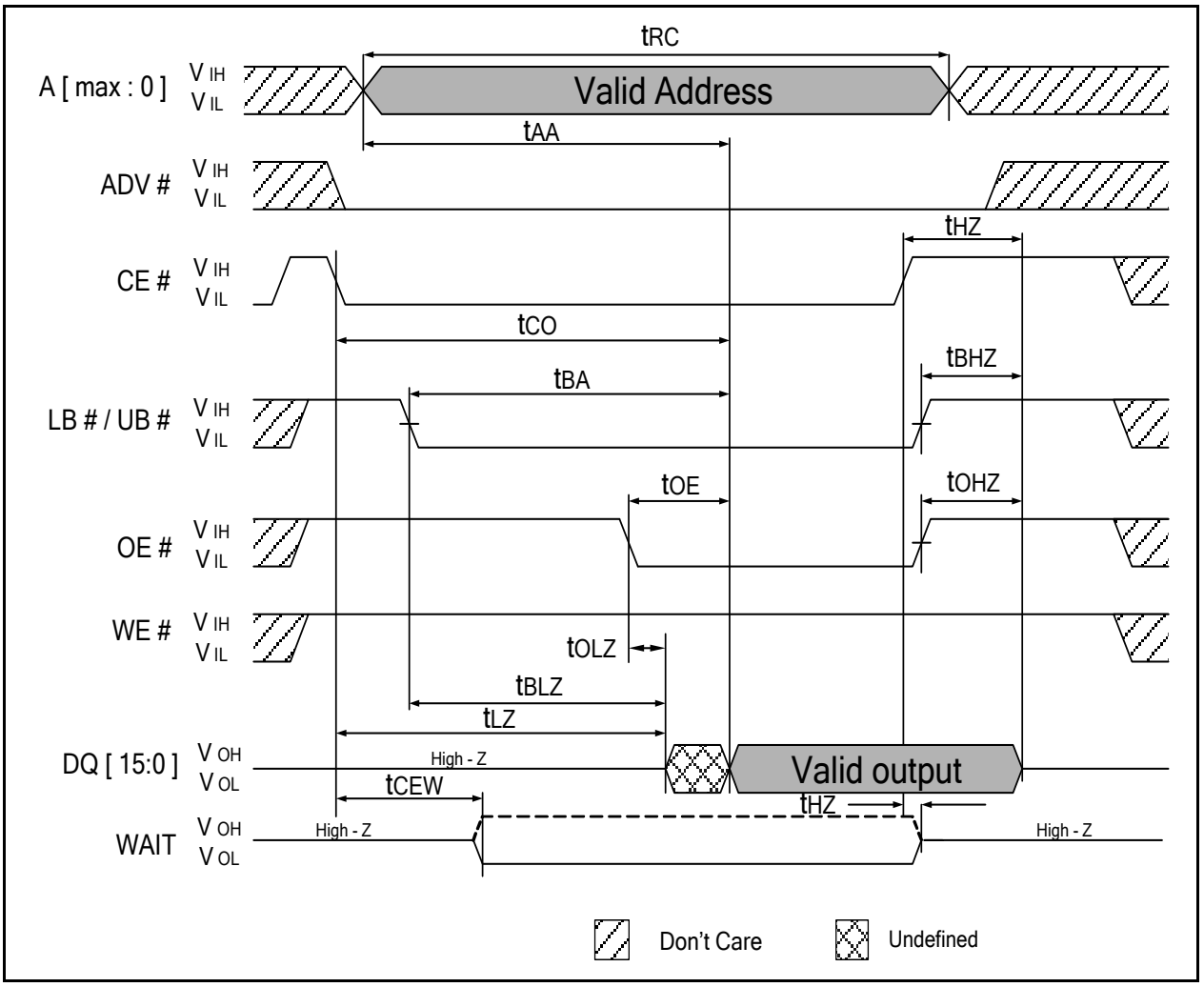


10.2.3 Initialization and DPD Timing Parameters

Description	Symbol	Min	Max	Unit
CE# HIGH after Write BCR[4]=0	tDPD	150	-	µs
CE# LOW between DPD Enable and Device Initialization	tDPDX	10	-	µs
DPD Exit to next Operation Command	tPU	-	150	µs

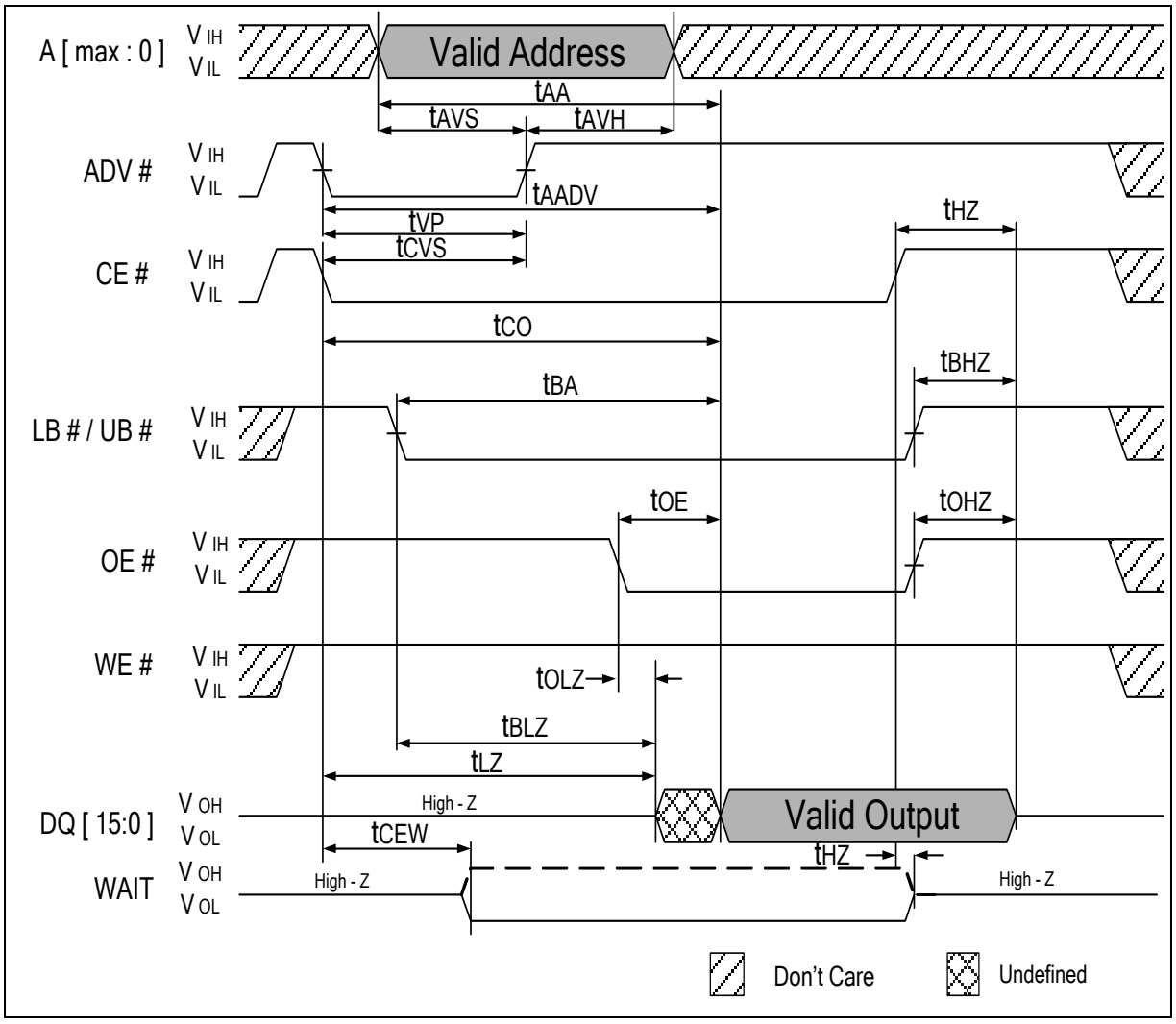
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10.2.4 Asynchronous READ

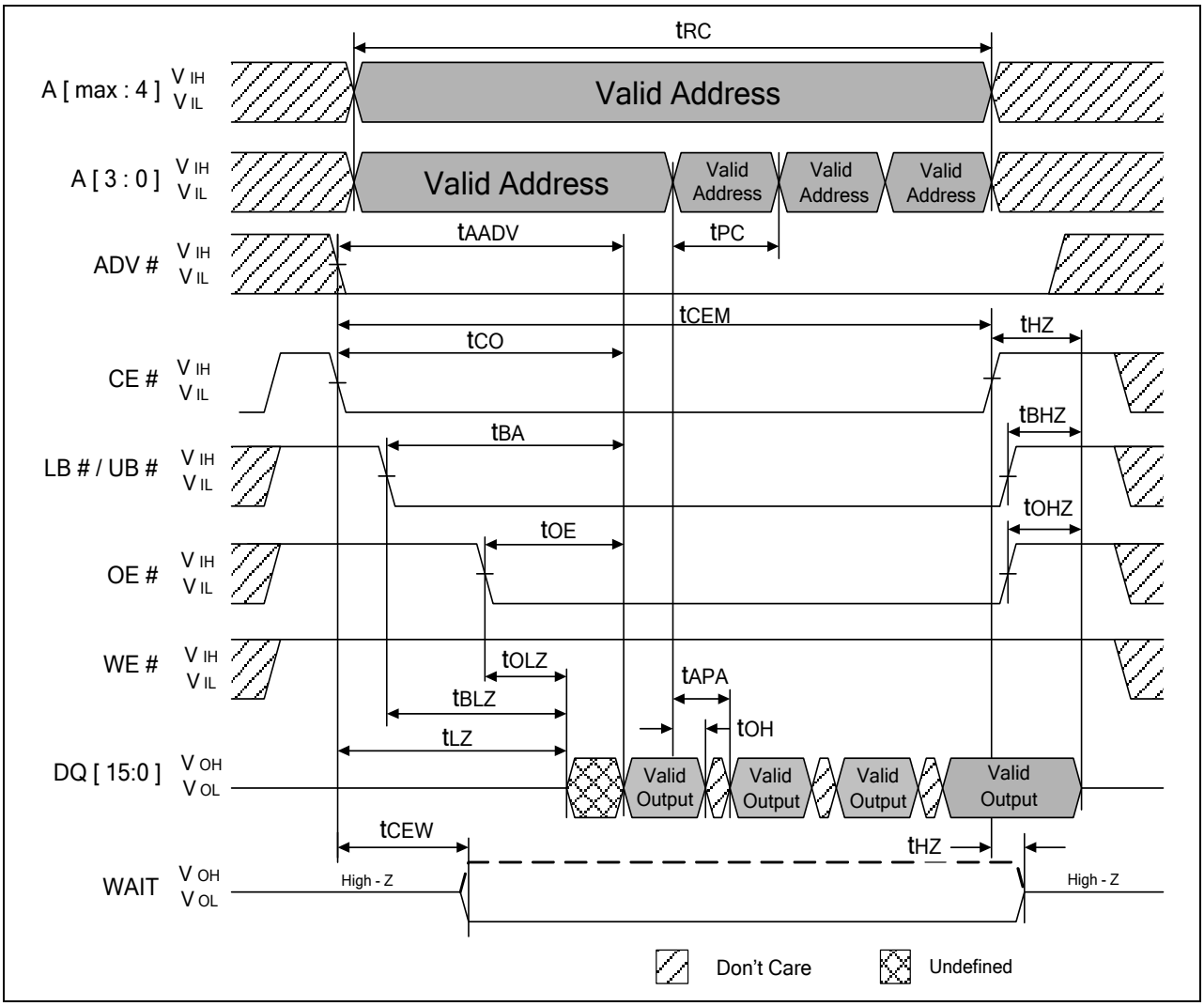


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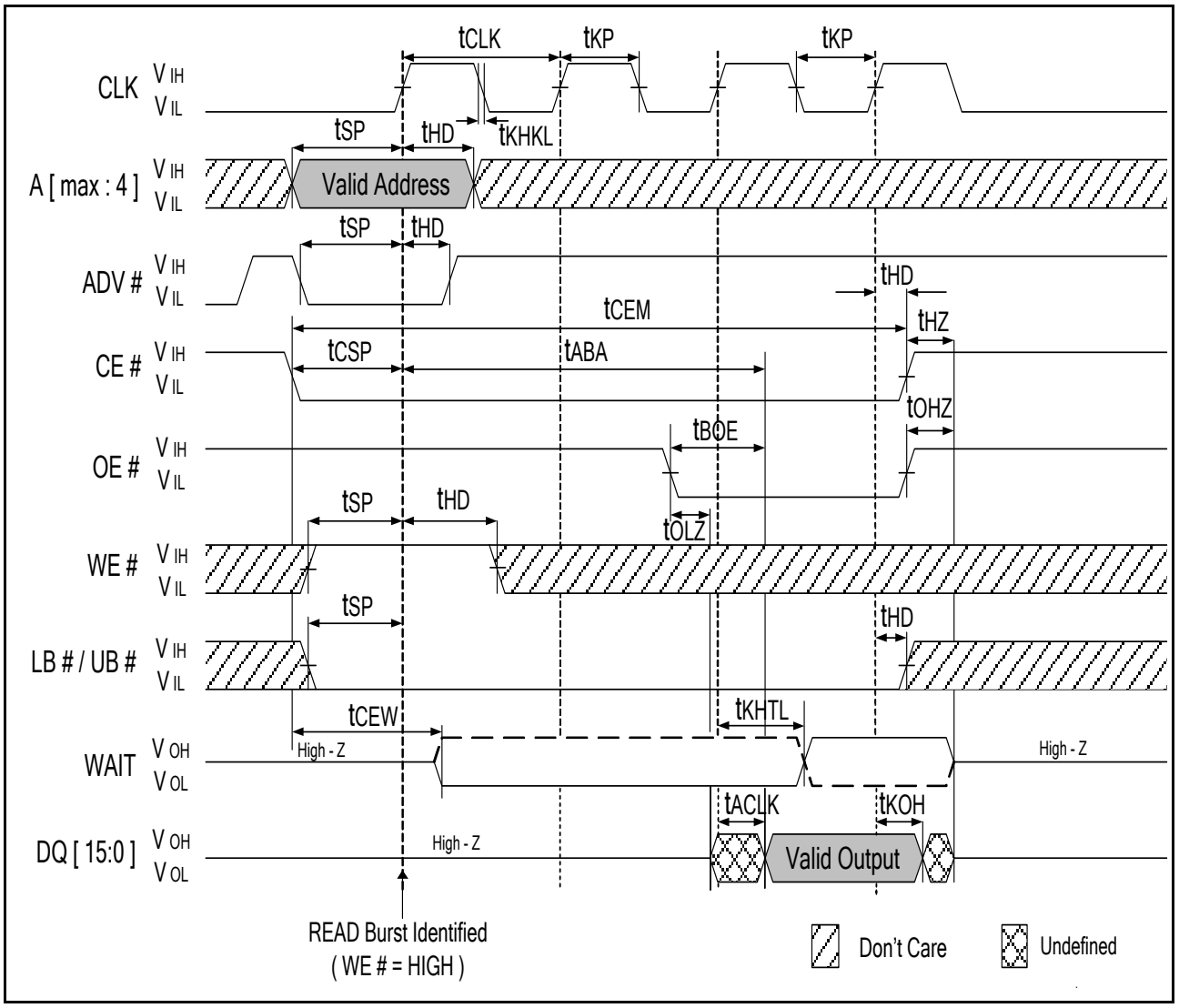
10.2.5 Asynchronous READ Using ADV#



10.2.6 Page Mode READ



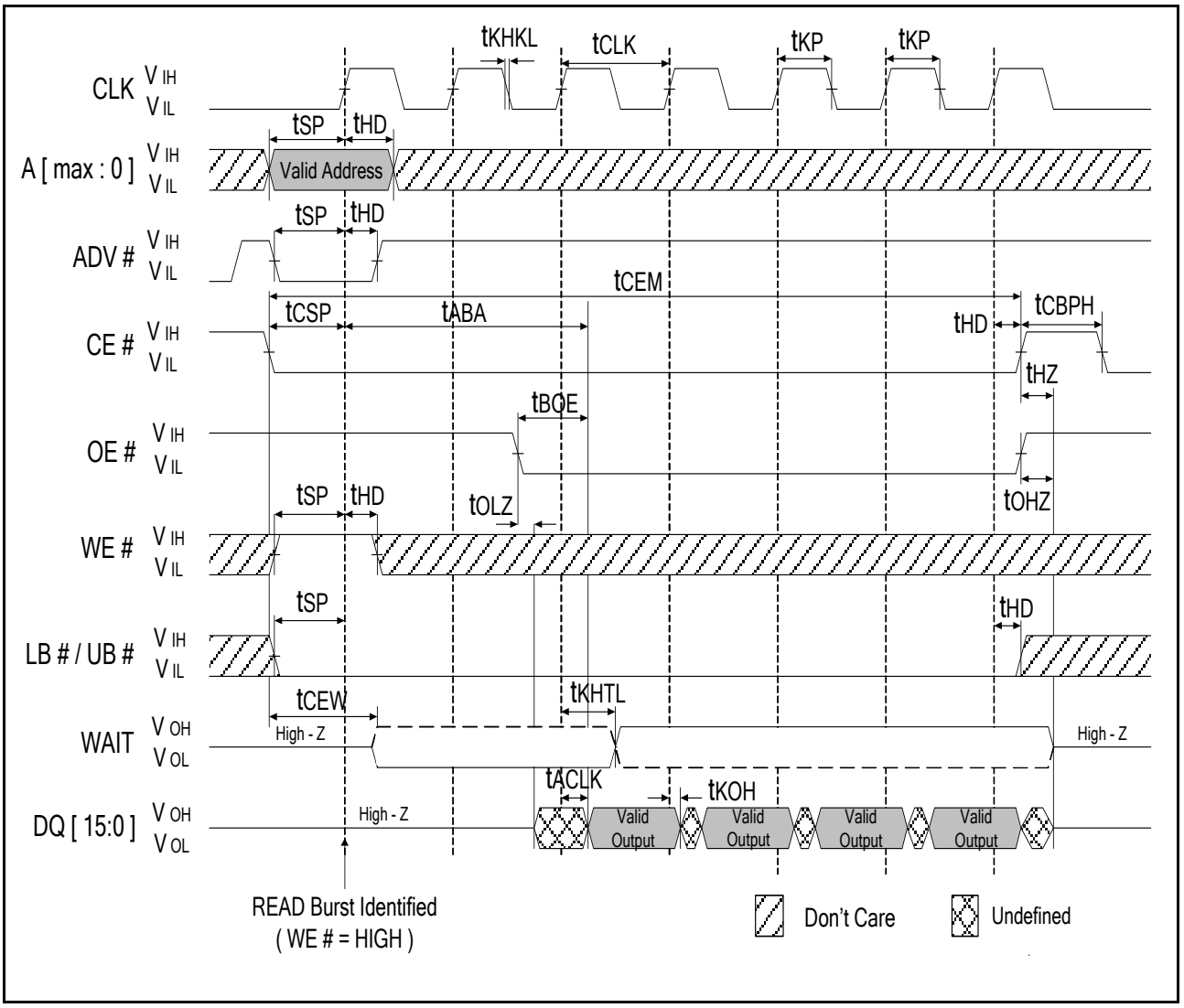
10.2.7 Single-Access Burst READ Operation-Variable Latency



Note : Non-default BCR settings : Latency code 2(3 clocks); WAIT active LOW; WAIT asserted during delay.

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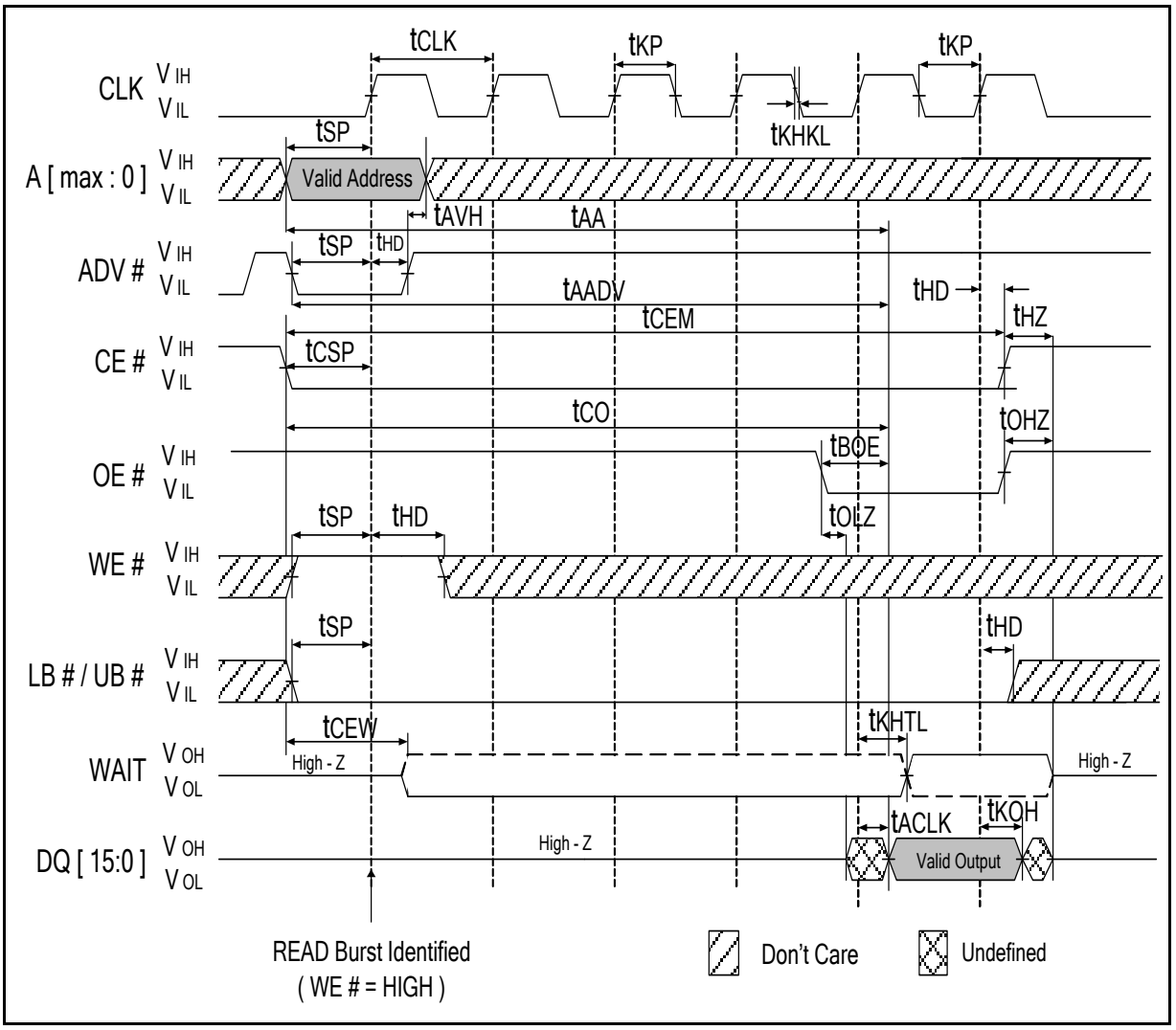
10.2.8 4-Word Burst READ Operation-Variable Latency



Note : Non-default BCR settings : Latency code 2(3 clocks); WAIT active LOW; WAIT asserted during delay.

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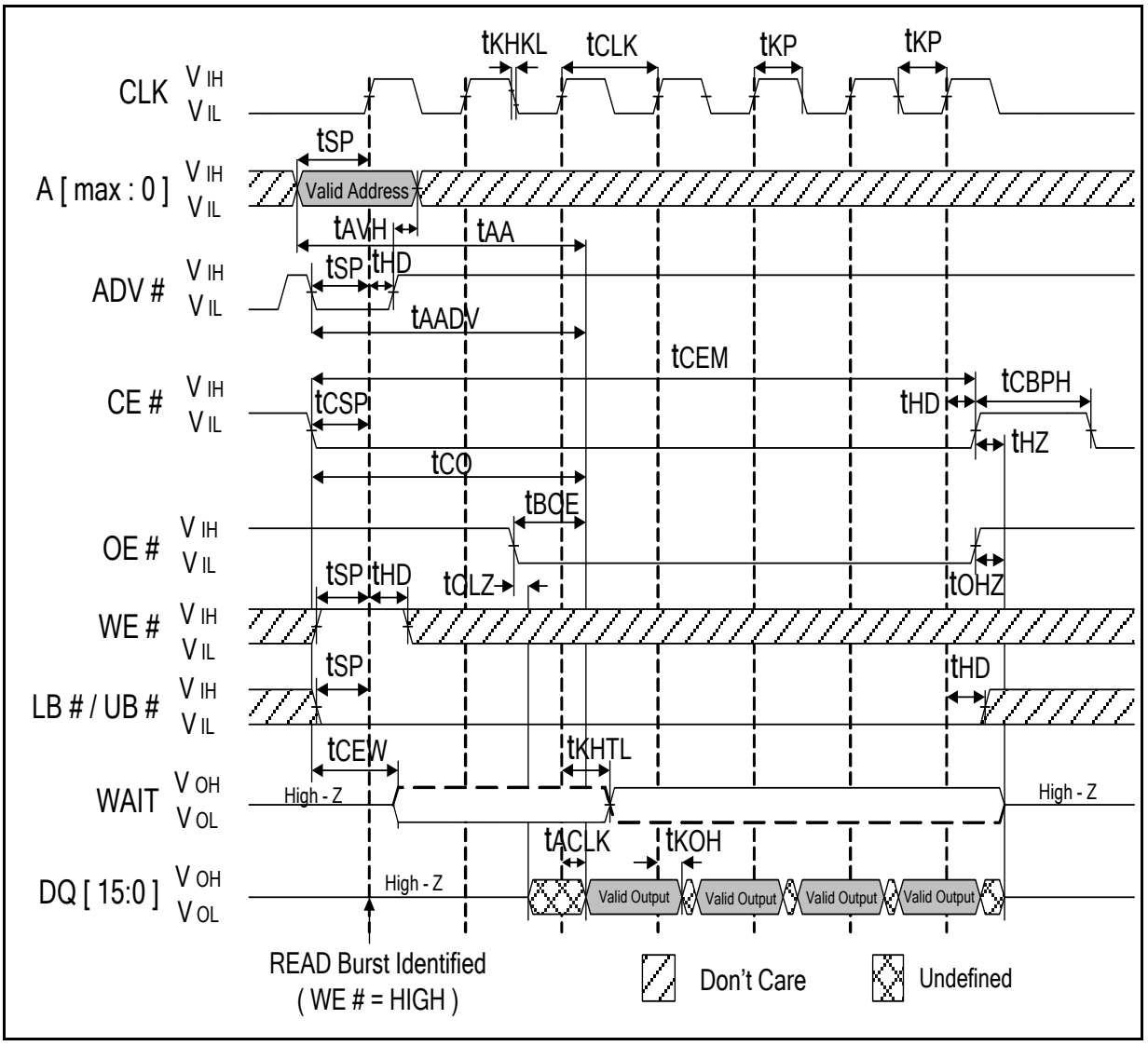
10.2.9 Single-Access Burst READ Operation-Fixed Latency



Note : Non-default BCR settings : Fixed latency; Latency code 4(5 clocks); WAIT active LOW; WAIT asserted during delay.

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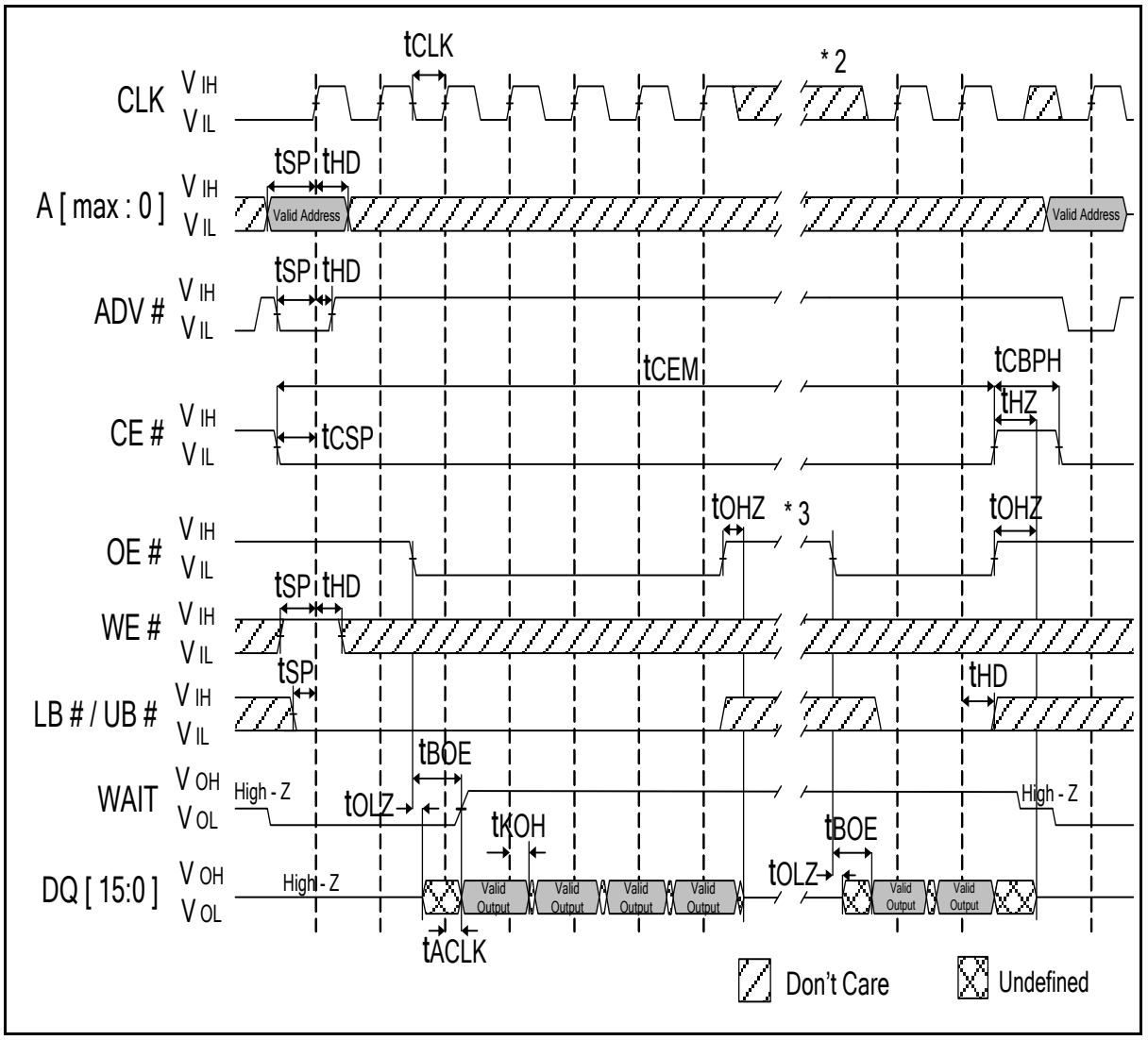
10.2.10 4-Word Burst READ Operation-Fixed Latency



Note : Non-default BCR settings : Fixed latency; Latency code 2(3 clocks); WAIT active LOW; WAIT asserted during delay.

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10.2.11 READ Burst Suspend



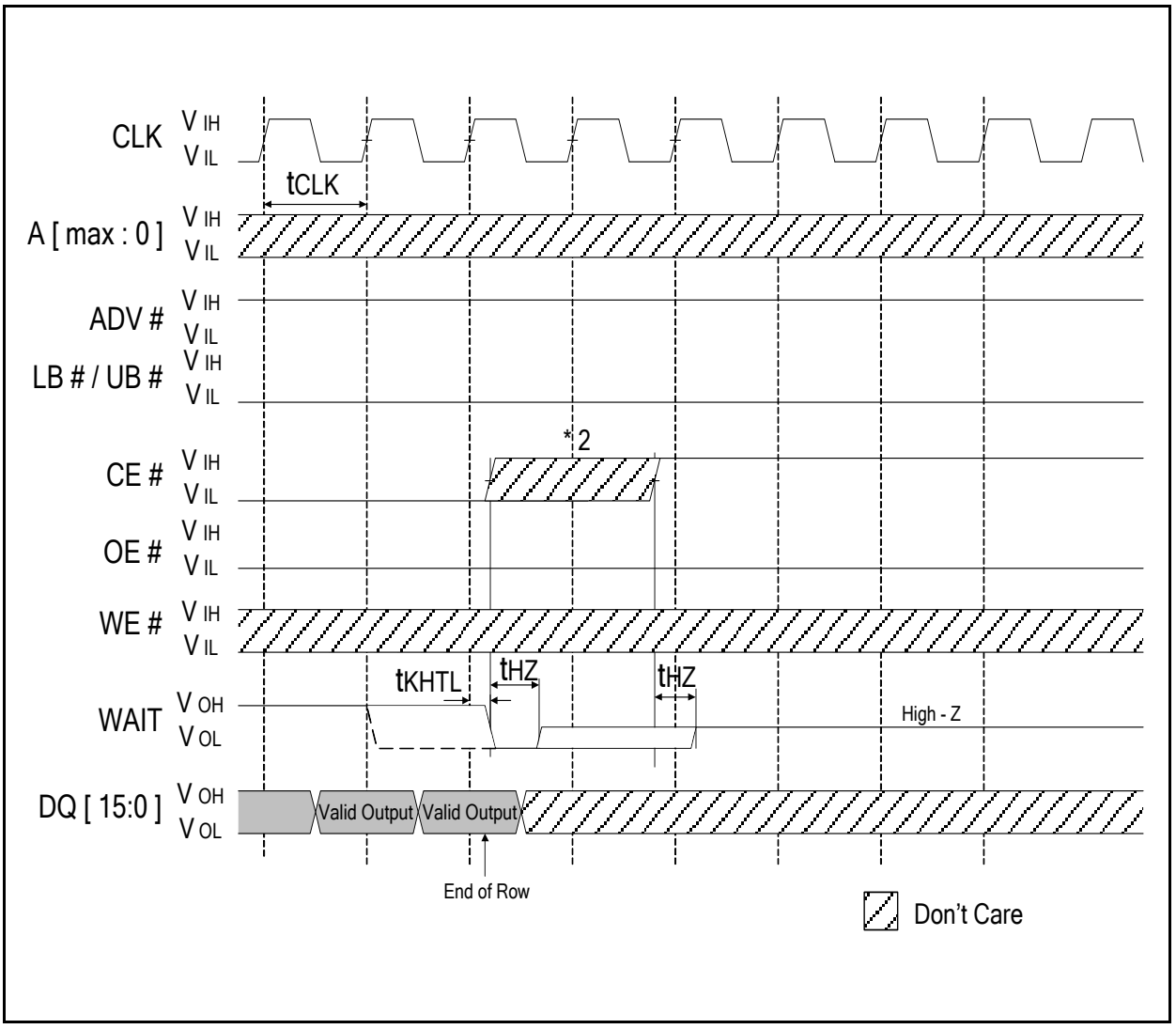
Note : 1. Non-default BCR settings for READ burst suspend; Fixed or variable latency code 2(3 clocks); WAIT asserted during delay.

2. CLK can be stopped LOW or HIGH, but must be static, with no LOW-to HIGH transitions during burst suspend.

3. OE# can stay LOW during burst suspend, if OE# is LOW, DQ[15:0] will continue to output valid data.

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10.2.12 Burst READ at End-of-Row (Wrap Off)

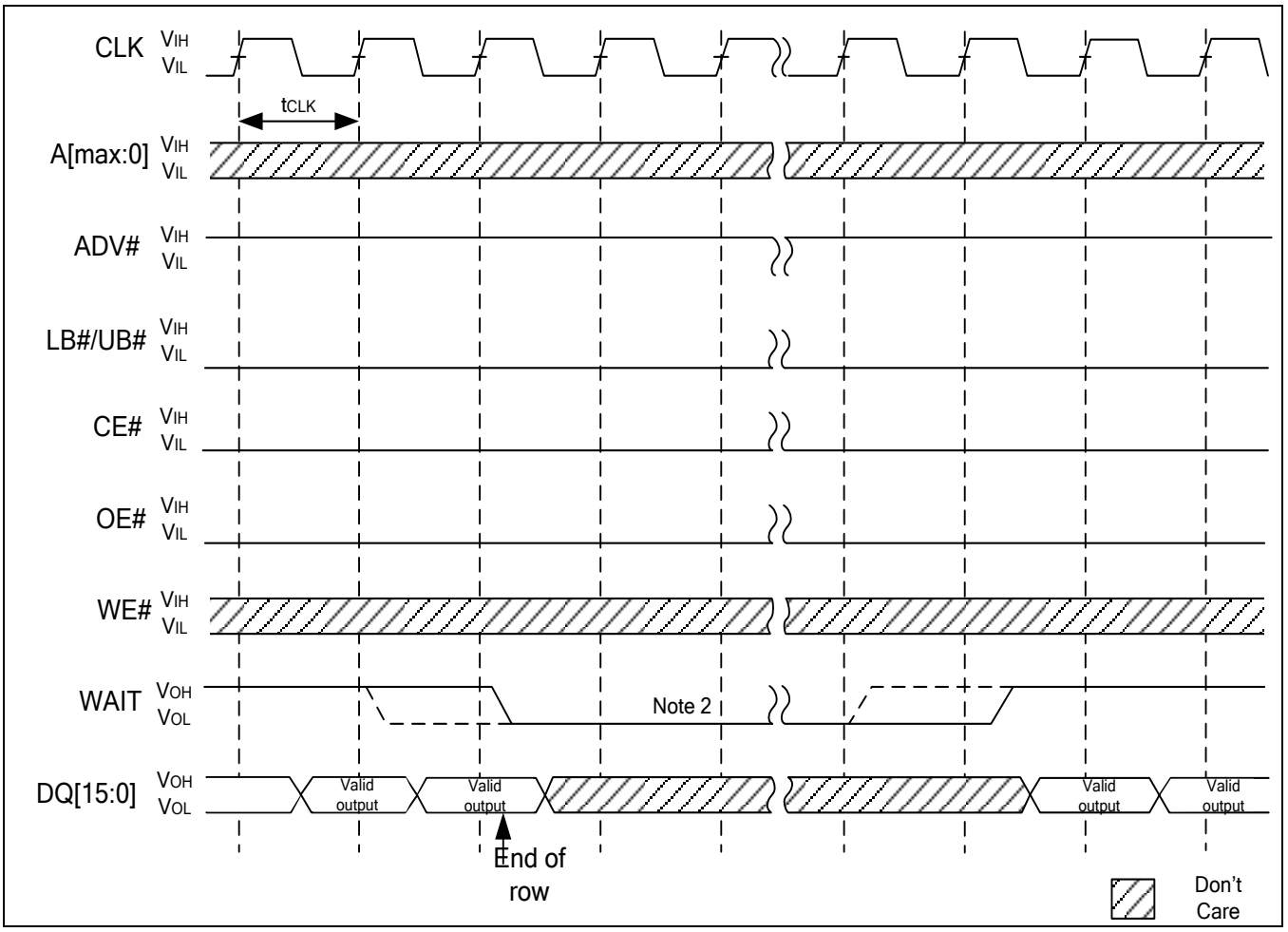


Note : 1. Non-default BCR settings for burst READ at end of row; fixed or variable latency; WAIT active LOW; WAIT asserted during delay.

2. For burst READs. CE# must go HIGH before the second CLK after the WAIT period begins (before the second CLK after WAIT asserts with BCR[8] = 0, or before the third CLK after WAIT asserts with BCR[8] = 1).

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10.2.13 Burst READ Row Boundary Crossing

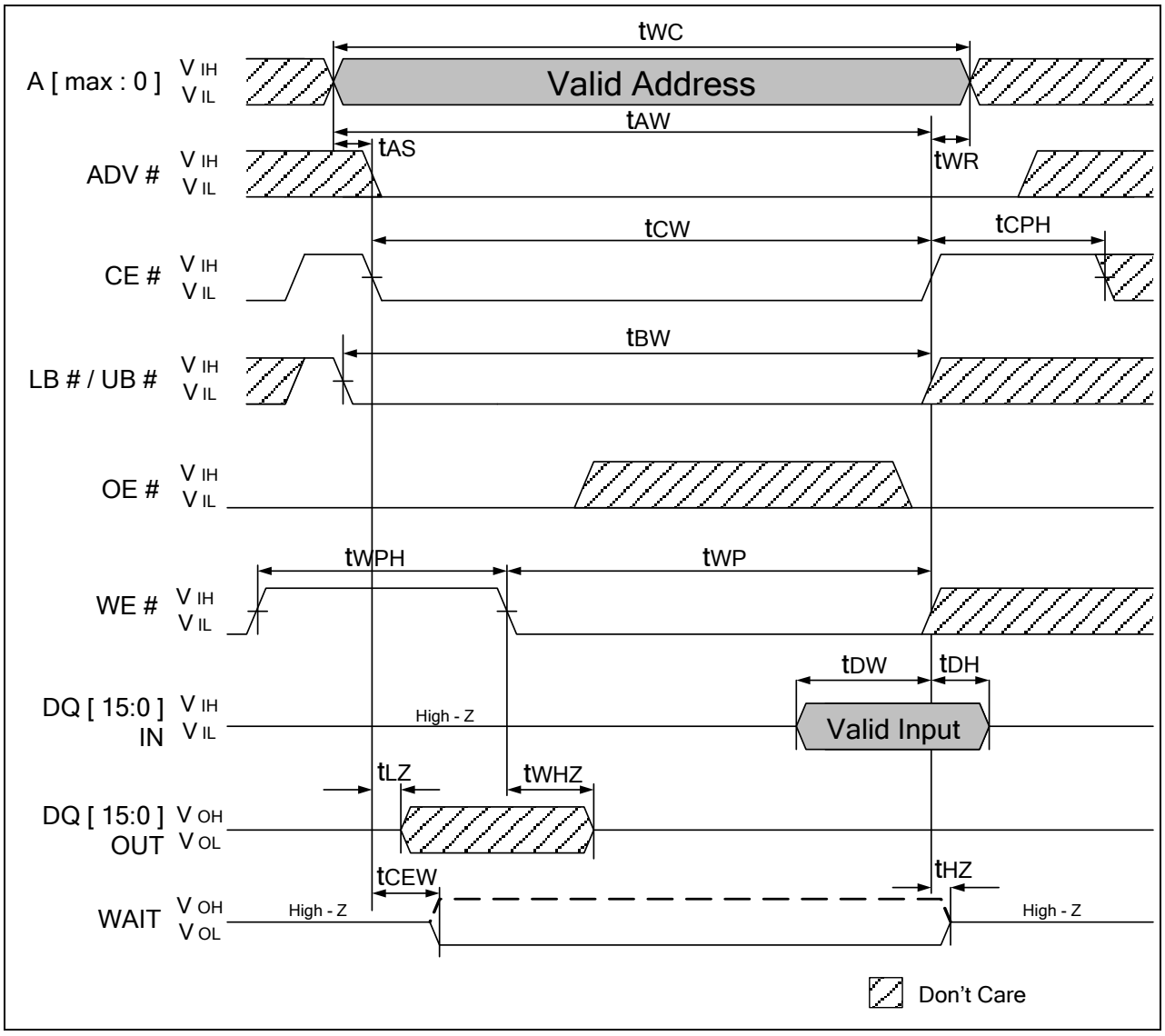


Note : 1. Non-default BCR settings for burst READ at end of row fixed or variable latency, WAIT active LOW, WAIT asserted during delay (shown as solid line).

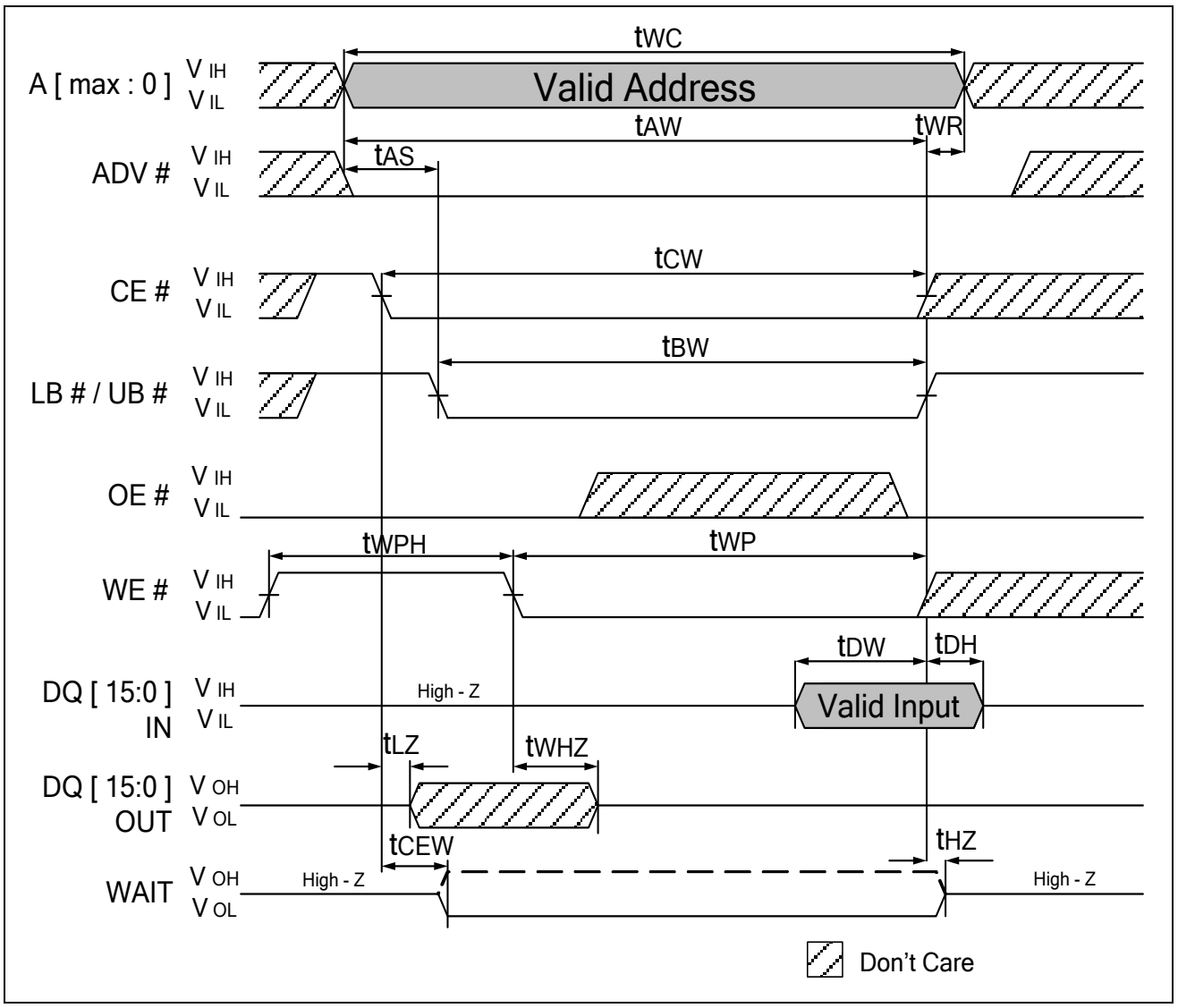
2. WAIT will be asserted for LC cycles for variable latency, or LC cycles for fixed latency.

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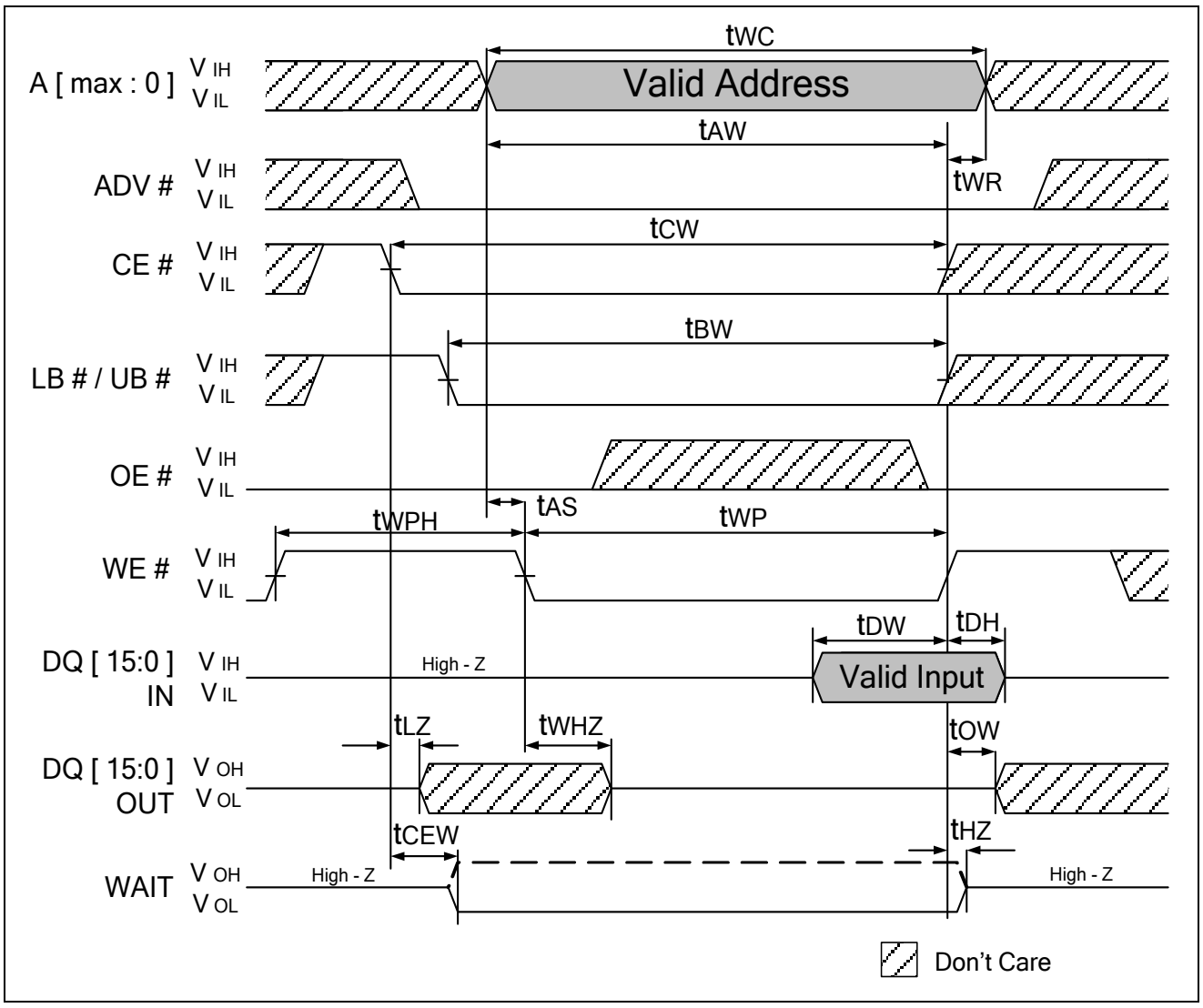
10.2.14 CE#-Controlled Asynchronous WRITE



10.2.15 LB# / UB# Controlled Asynchronous WRITE

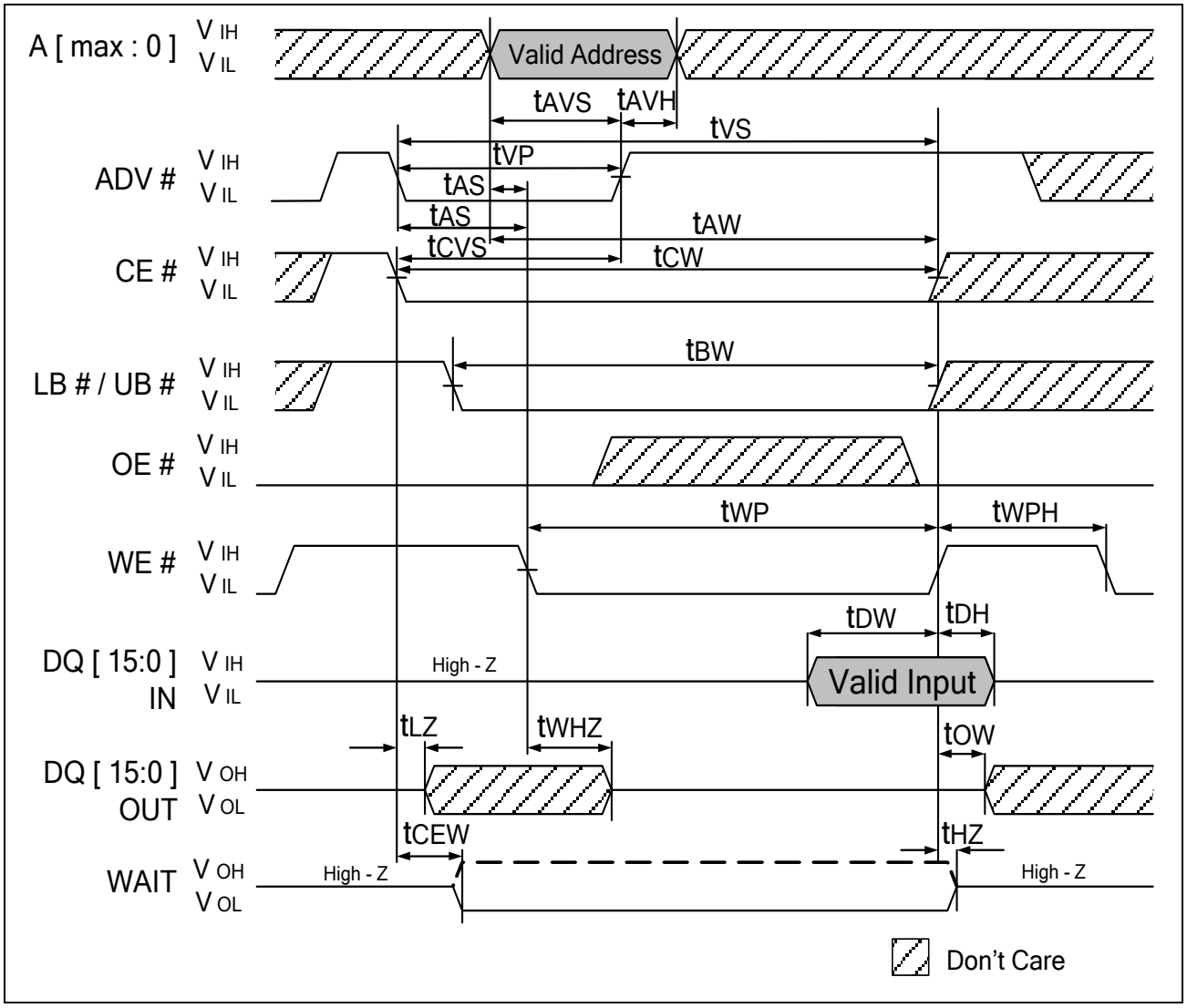


10.2.16 WE# - Controlled Asynchronous WRITE

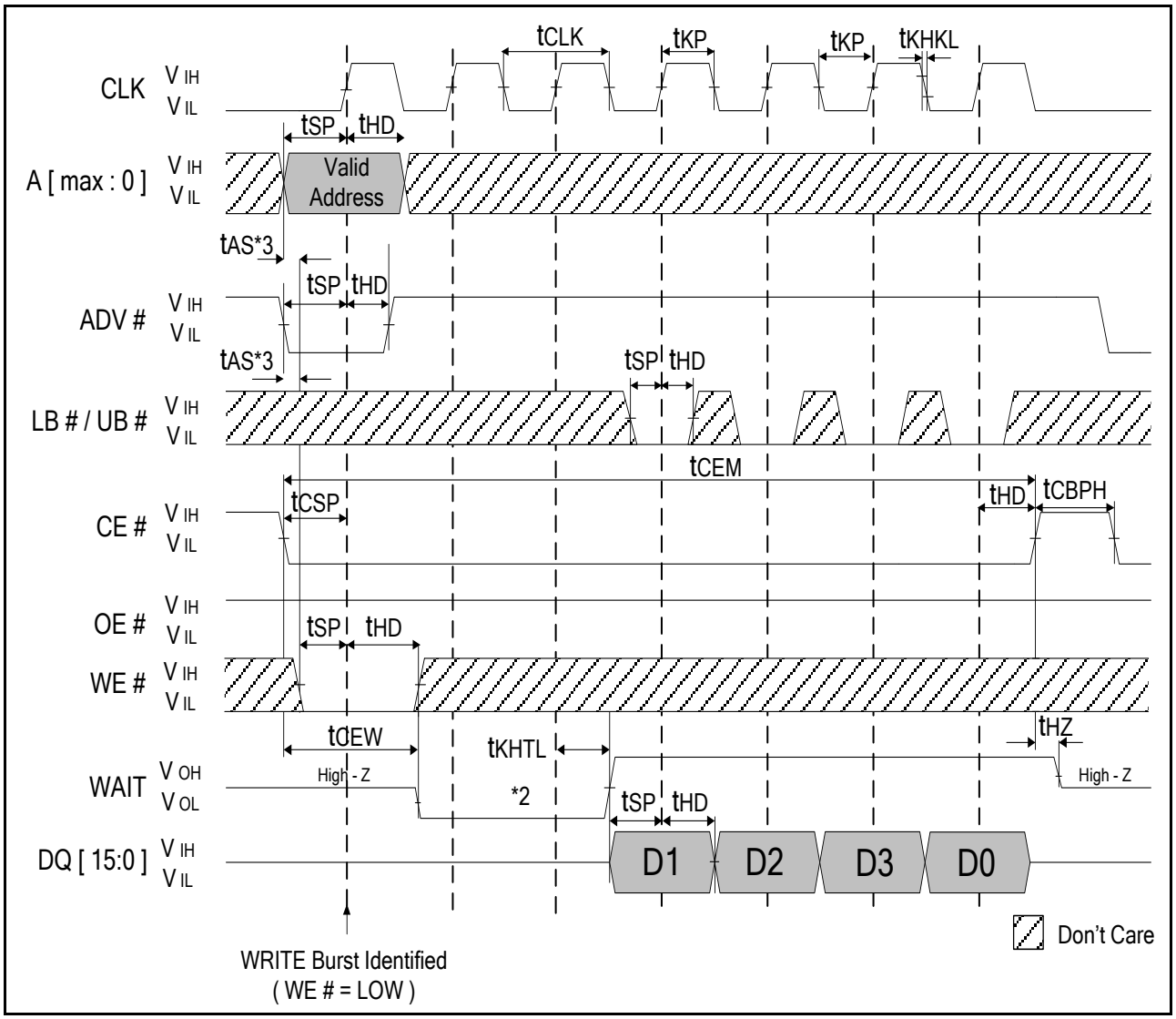


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10.2.17 Asynchronous WRITE Using ADV#



10.2.18 Burst WRITE Operation-Variable Latency Mode



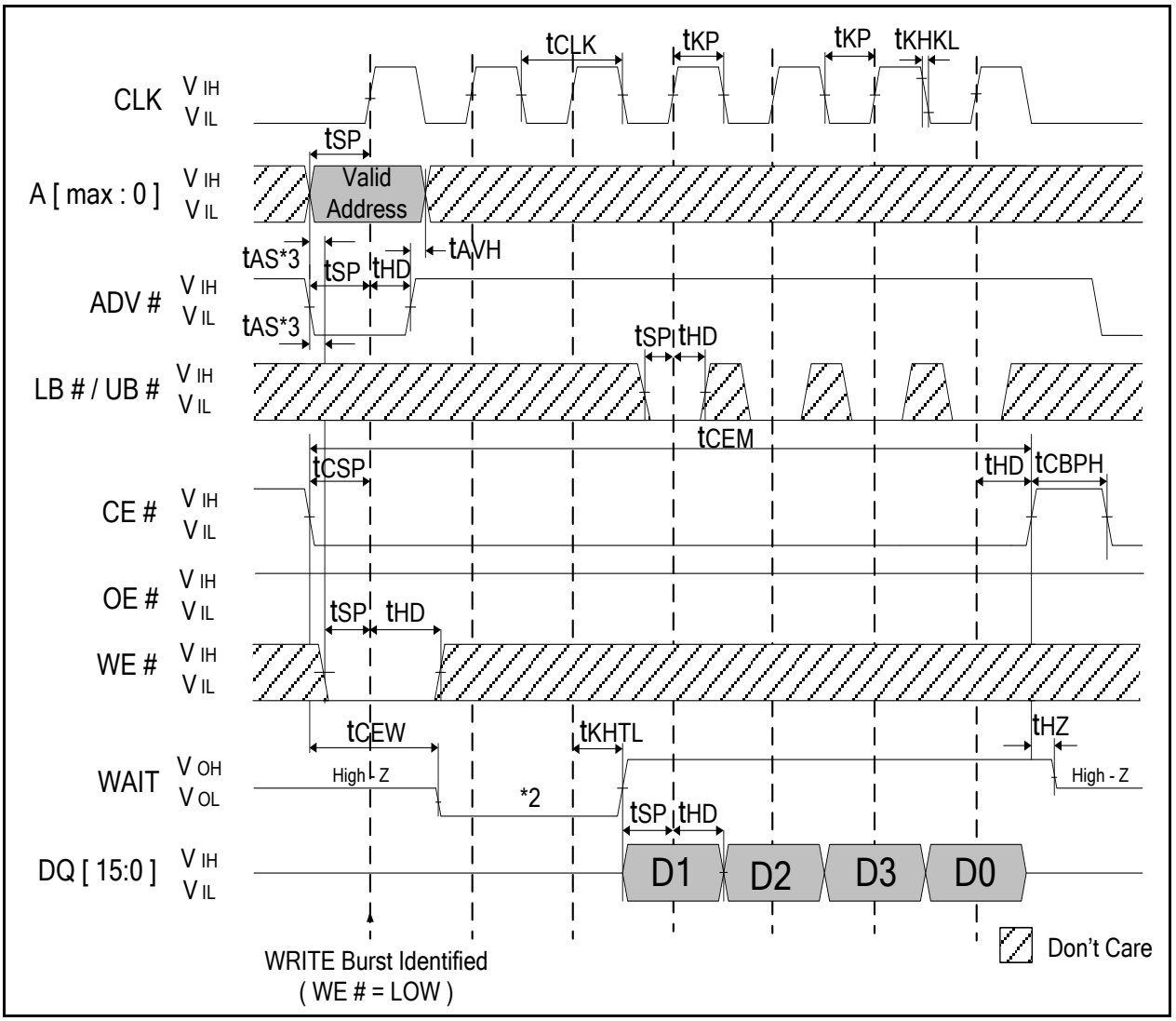
Note : 1. Non-default BCR settings for burst WRITE operation in variable latency mode; Latency code 2)3 clocks); WAIT active LOW; WAIT a asserted during delay; burst length 4; burst wrap enabled.

2. WAIT asserts for LC cycles for both fixed and variable latency, LC = Latency code (BCR[13:11]).

3. tAS required if tCSP > 20ns.

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10.2.19 Burst WRITE Operation-Fixed Latency Mode



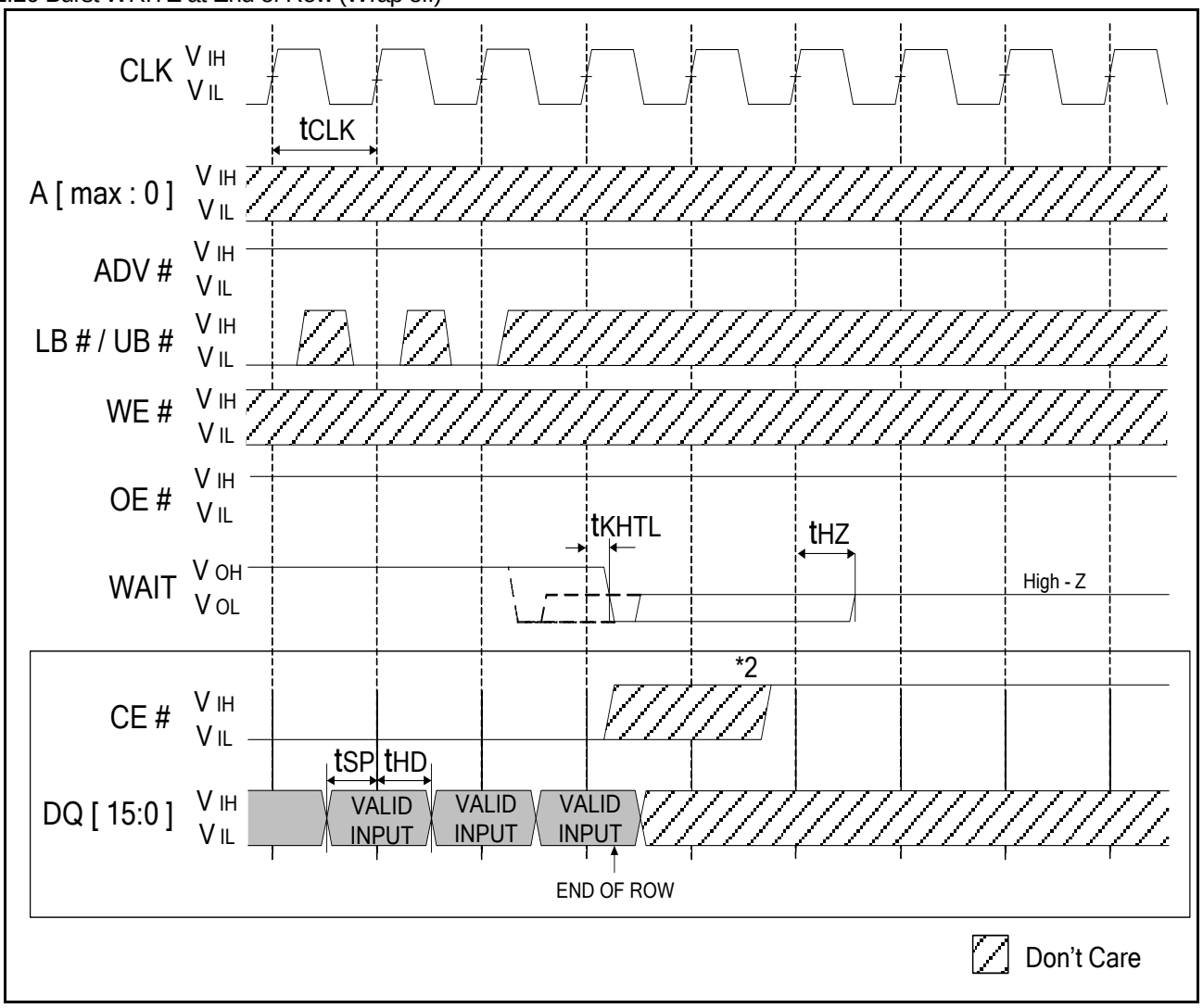
Note : 1. Non-default BCR settings for burst WRITE operation in fixed latency mode; Fixed latency, latency code 2)3 clocks); WAIT active LOW; WAIT a asserted during delay; burst length 4; burst wrap enabled.

2. WAIT asserts for LC cycles for both fixed and variable latency, LC = Latency code (BCR[13:11]).

3. tAS required if tCSP > 20ns.

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10.2.20 Burst WRITE at End of Row (Wrap off)

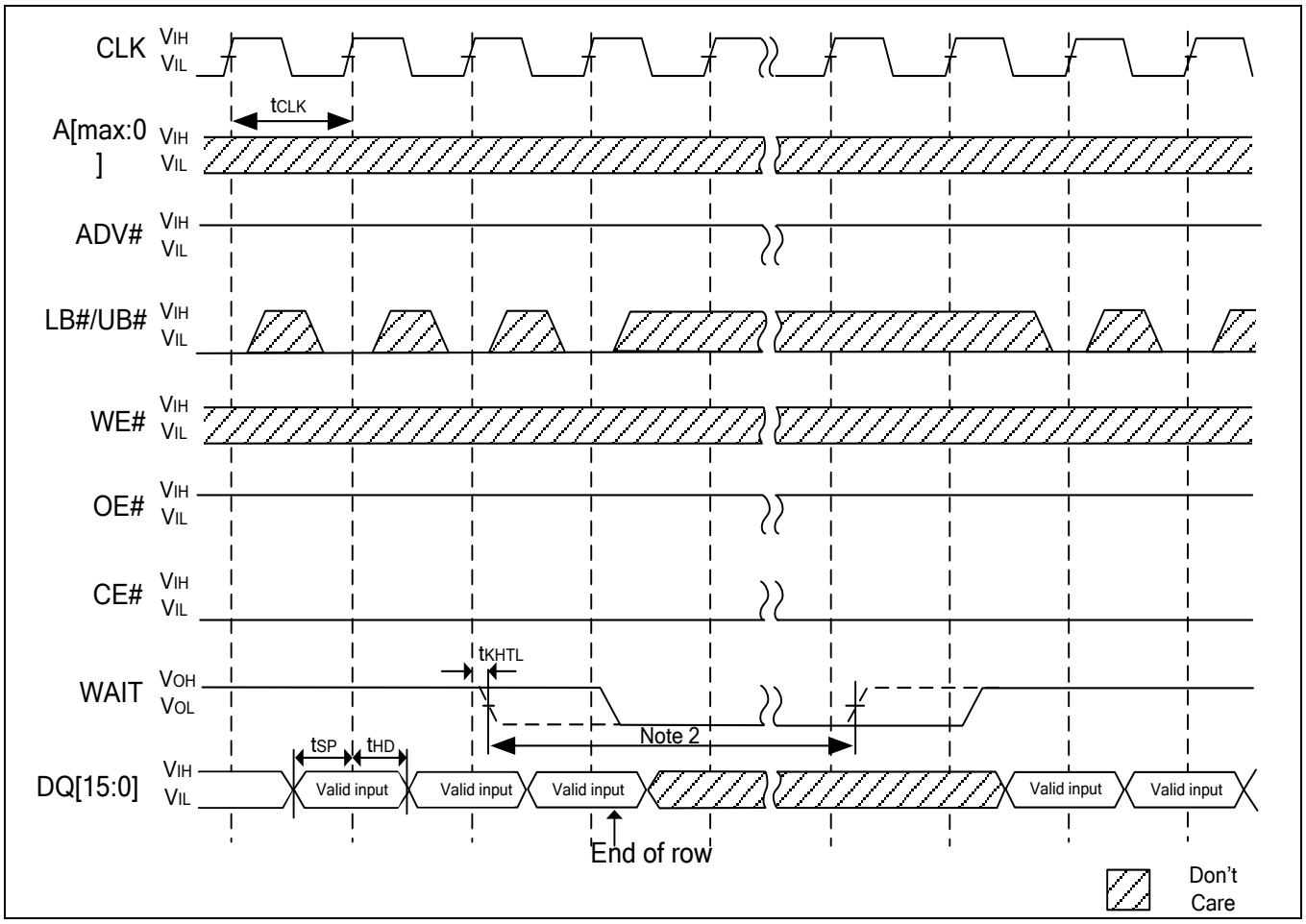


Note : 1. Non-default BCR settings for burst WRITE at end row; fixed or variable latency ; WAIT active LOW; WAIT asserted during delay.

2. For burst WRITEs, CE# must go HIGH before the second CLK after the WAIT period begins (before the 2nd CLK after WAIT asserts with BCR[8] = 0, or before the third CLK after WAIT asserts with BCR[8] = 1.

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10.2.21 Burst WRITE Row Boundary Crossing

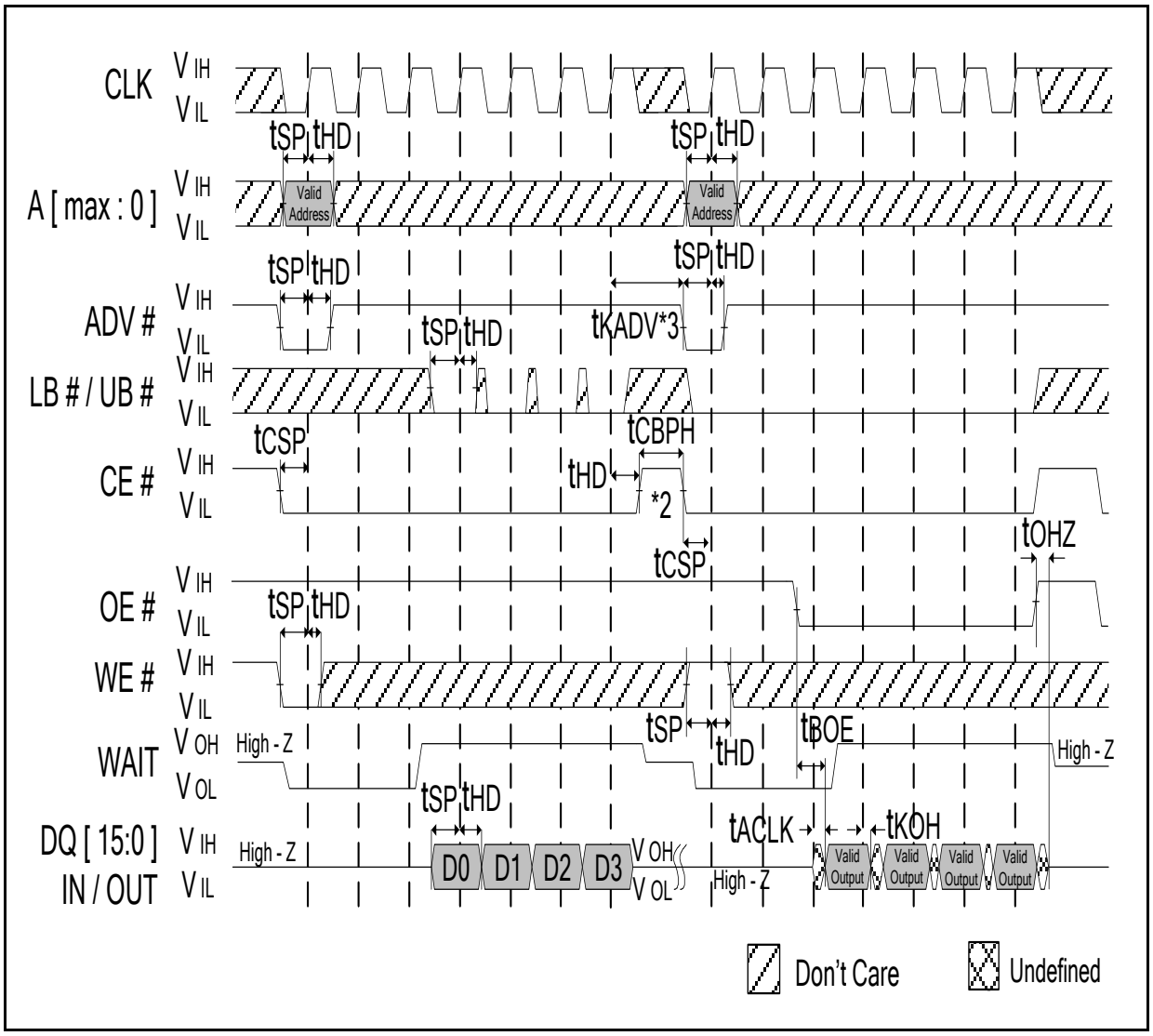


Notes : 1. Non-default BCR settings for burst WRITE at end of row : foxed or variable latency, WAIT active LOW, WAIT asserted during delay (shown as solid line).

2. WAIT will be asserted for LC cycles for variable latency, or LC cycles for fixed latency.

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10.2.22 Burst WRITE Followed by Burst READ

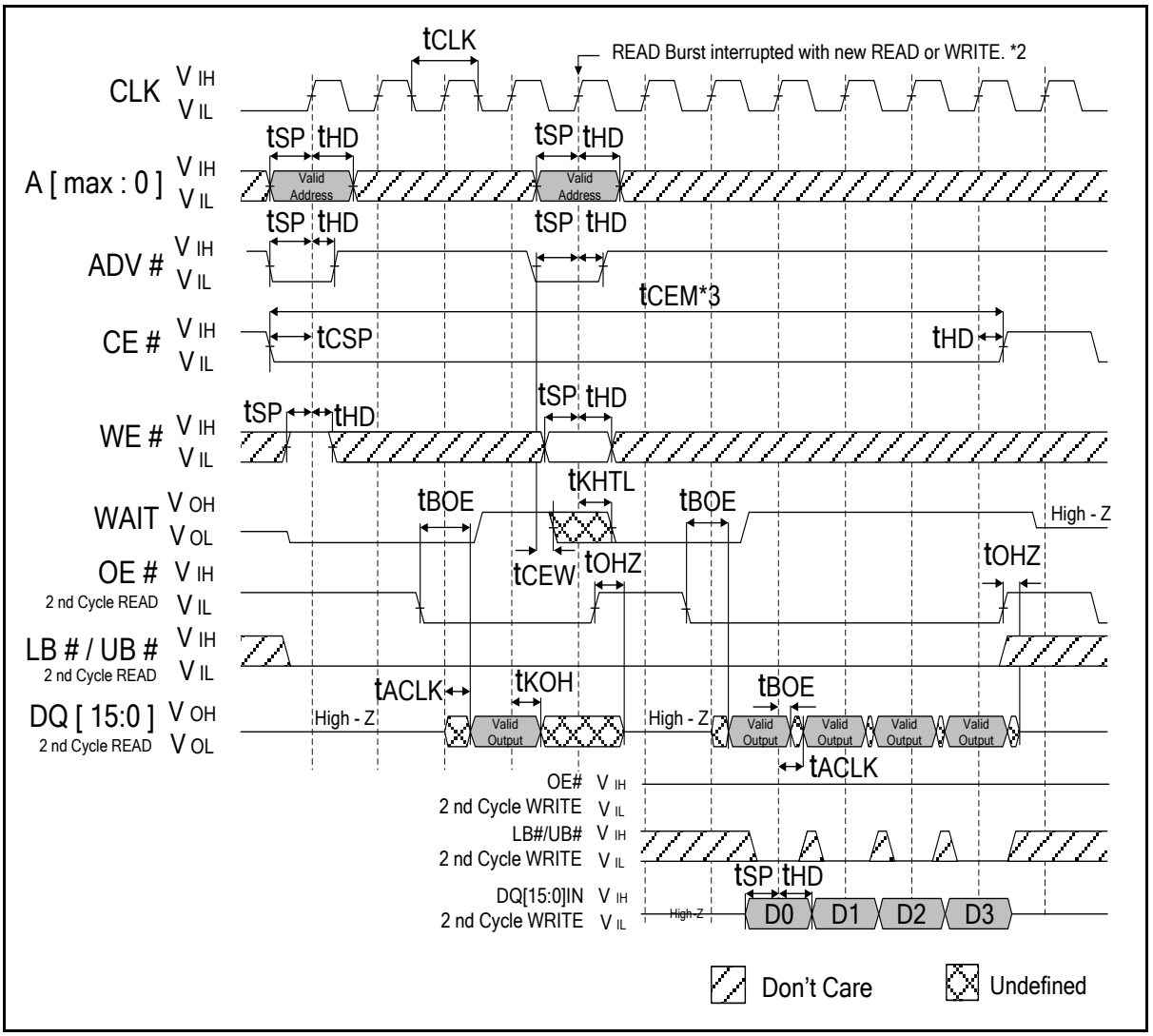


Note：1. Non-default BCR settings for burst WRITE followed by burst READ: Fixed or variable latency; latency code 2(3clocks); WAIT active LOW; WAIT asserted during delay.

2. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns. CE# can stay LOW between burst READ and burst WRITE operations, but CE# must not remain LOW longer than tCEM. See burst interrupt diagrams for cases where CE# stays LOW between bursts.

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10.2.23 Burst READ Interrupted by Burst READ or WRITE



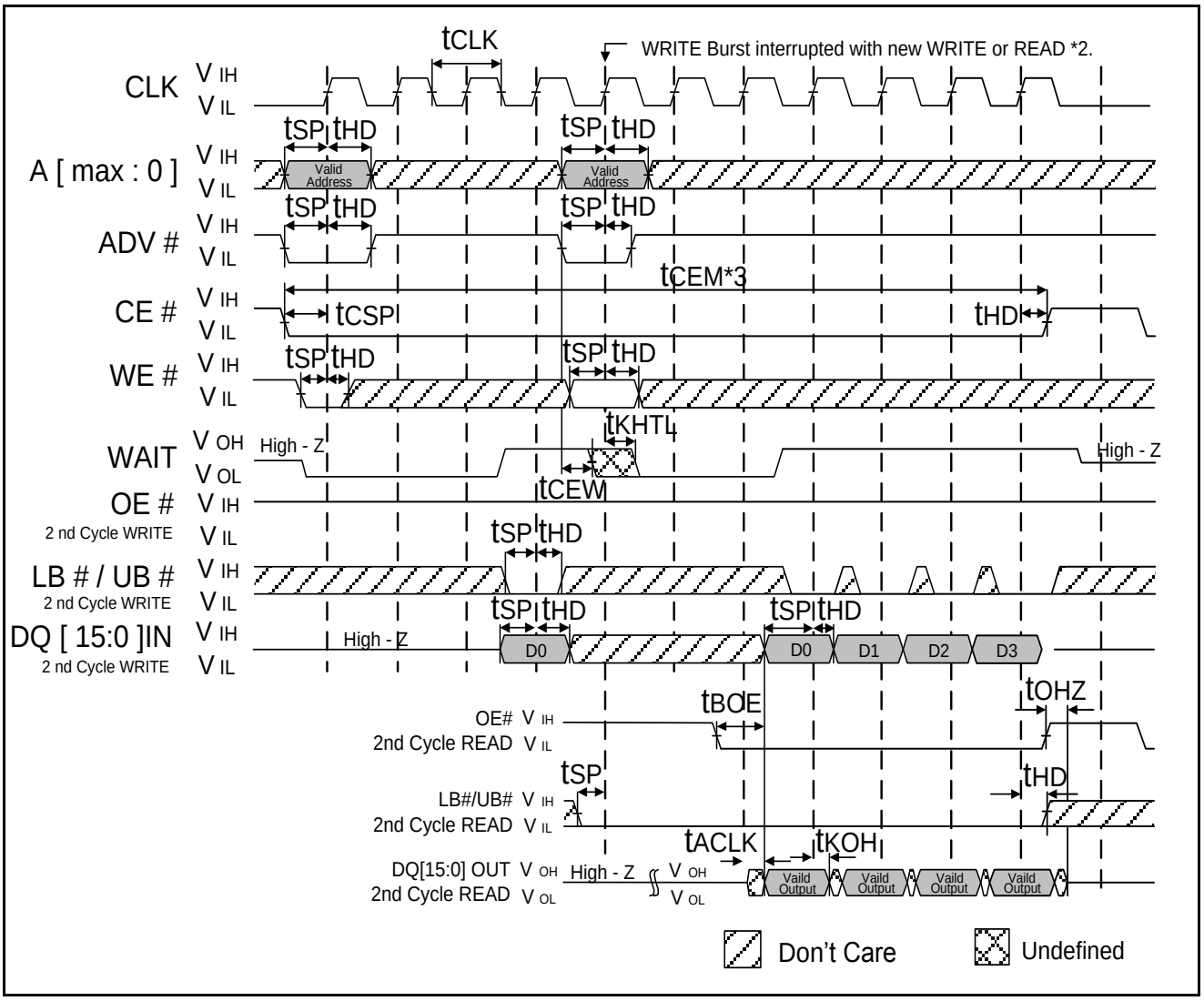
Note : 1. Non-default BCR settings for burst READ interrupted by burst READ or WRITE: Fixed or variable latency code 2(3 clocks); WAIT active LOW; WAIT asserted during delay. All bursts shown for variable latency; no refresh collision.

2. Burst interrupt shown on first allowable clock (i.e., after the first data received by the controller).

3. CE# can stay LOW between burst operations, but CE# must not remain LOW longer than tCEM.

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10.2.24 Burst WRITE Interrupted by Burst WRITE or READ–Variable Latency Mode



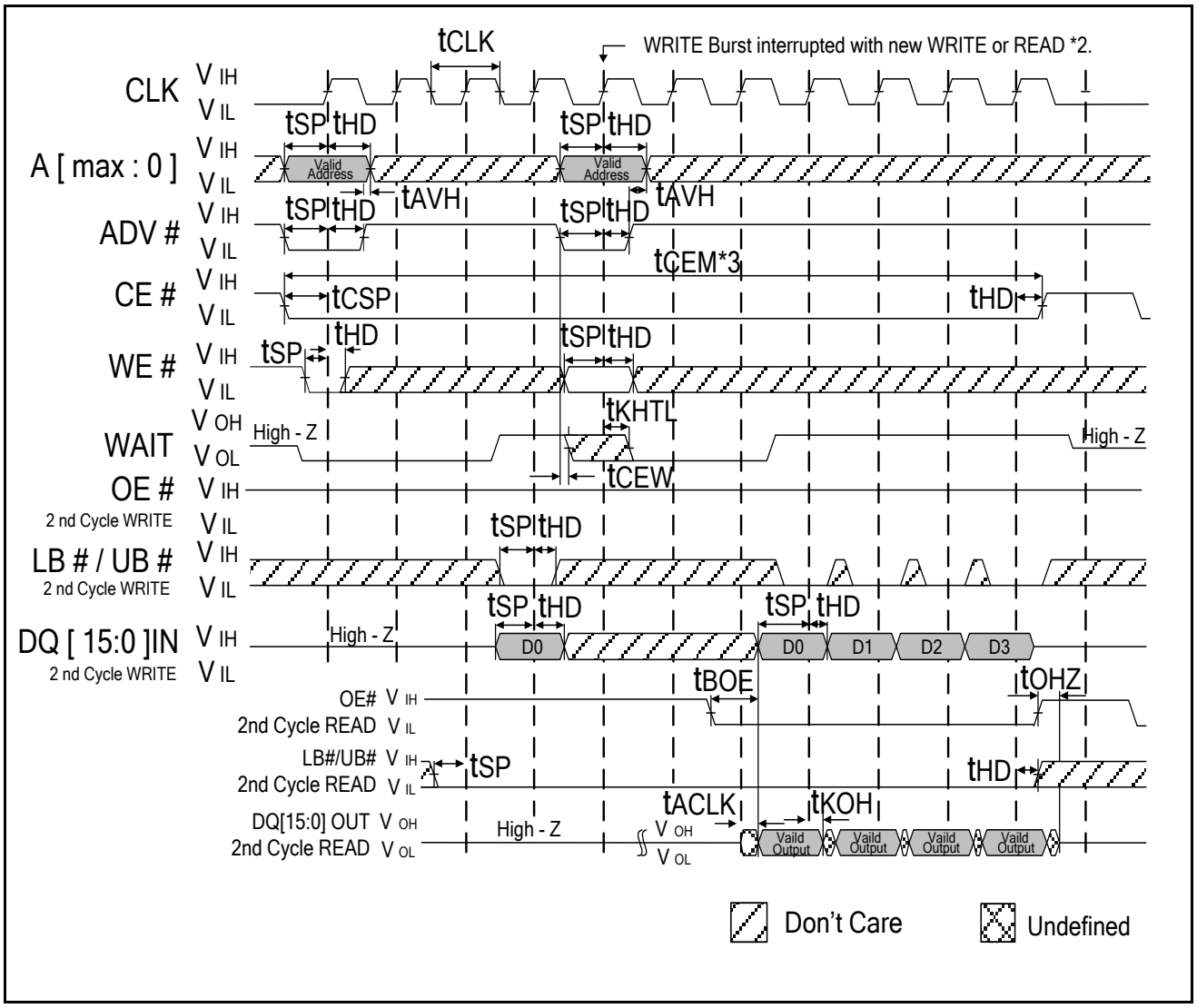
Note : 1. Non-default BCR settings for burst WRITE interrupted by burst WRITE or READ in variable latency mode: Variable latency; latency code 2(3 clocks); WAIT active LOW; WAIT asserted during delay. All bursts shown for variable latency; no refresh collision.

2. Burst interrupt shown on first allowable clock (i.e., after first data word written).

3. CE# can stay LOW between burst operations, but CE# must not remain LOW longer than tCEM.

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10.2.25 Burst WRITE Interrupted by Burst WRITE or READ-Fixed Latency Mode



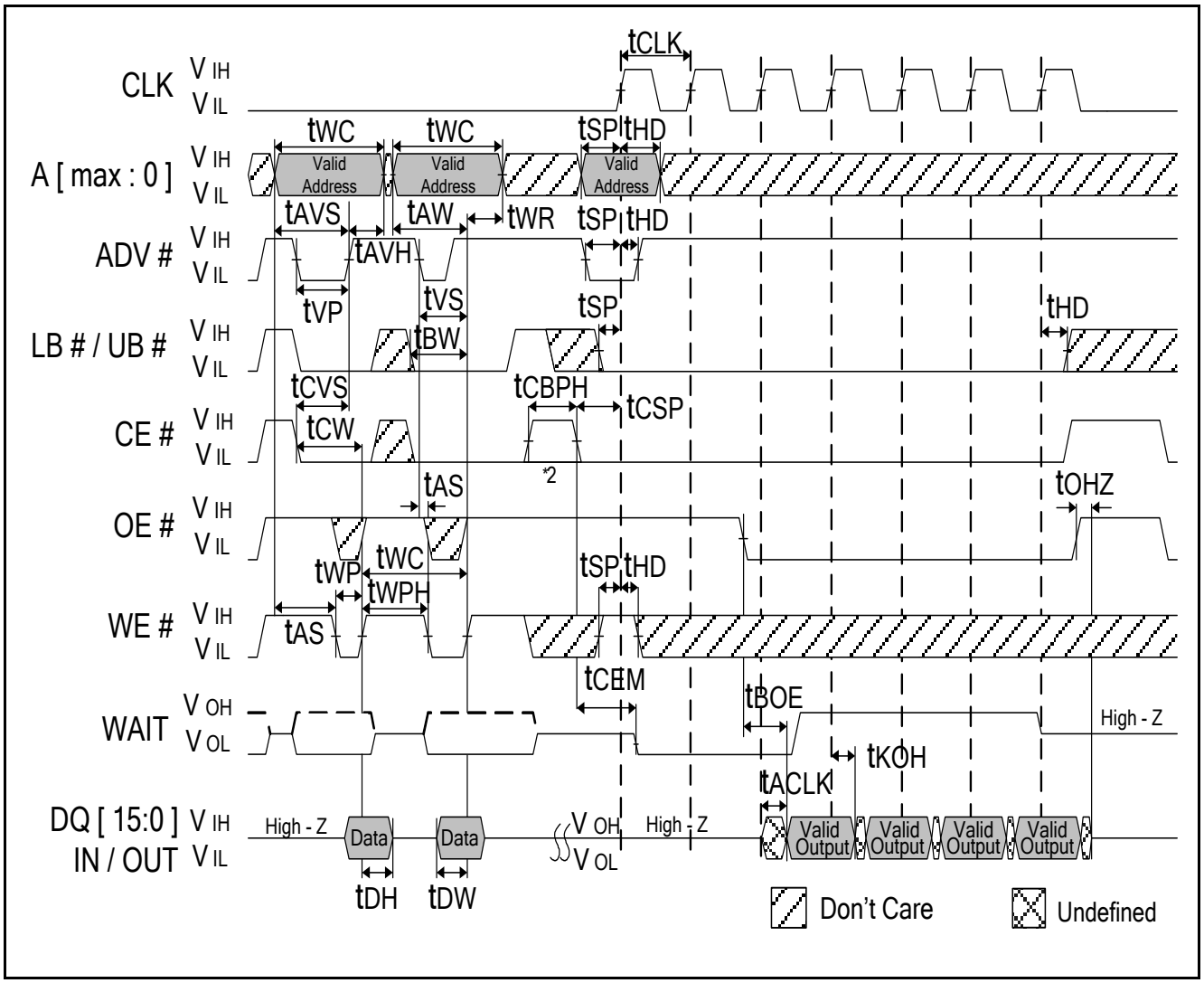
Note : 1. Non-default BCR settings for burst WRITE interrupted by burst WRITE or READ in fixed latency mode: Fixed latency; latency code 2(3 clocks); WAIT active LOW; WAIT asserted during delay.

2. Burst interrupt shown on first allowable clock(i, e., after first data word written).

3. CE# can stay LOW between burst operations, but CE# must not remain LOW longer than tCEM.

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10.2.26 Asynchronous WRITE Followed by Burst READ

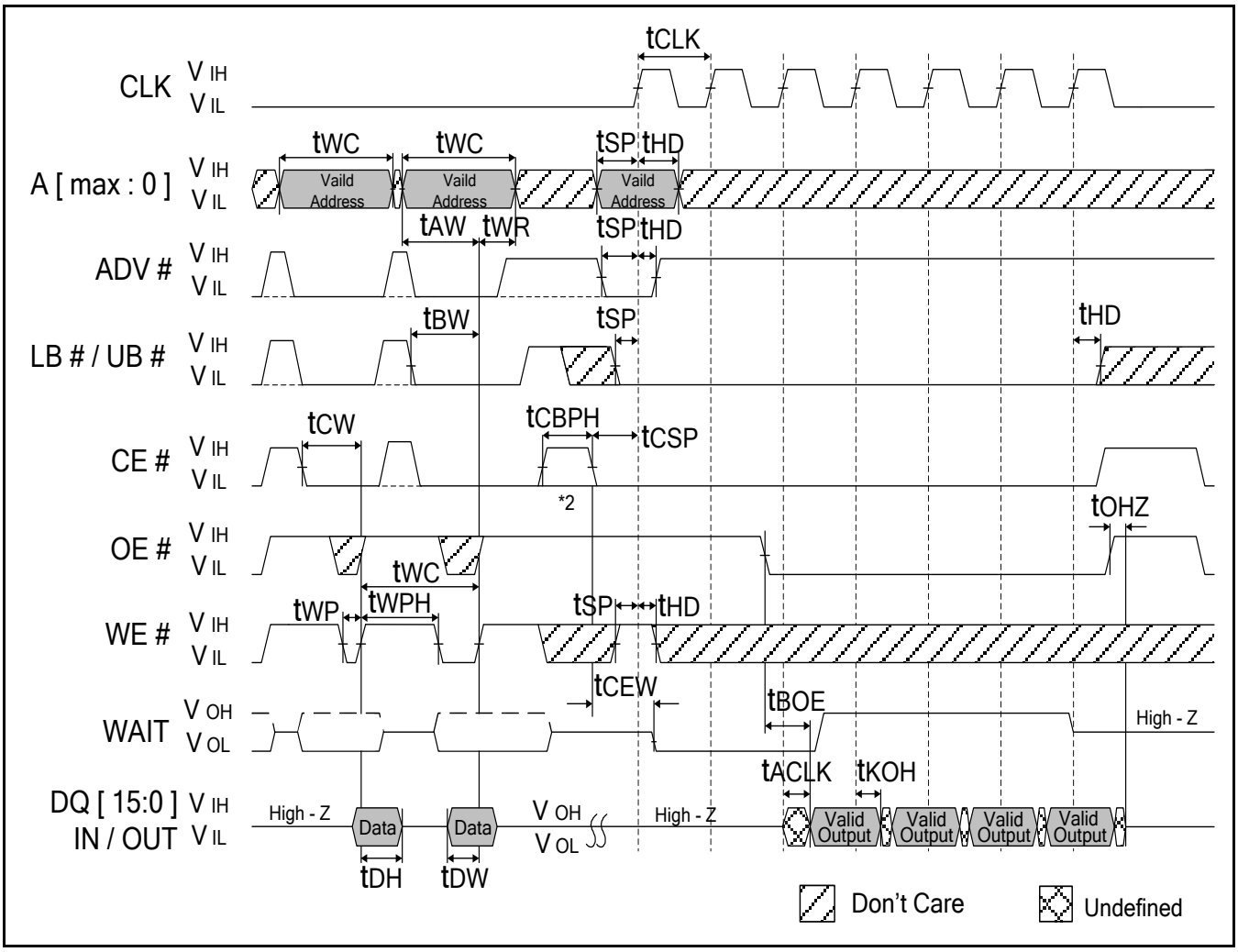


Note : 1. Non-default BCR settings for asynchronous WRITE followed by burst READ: Fixed or variable latency; latency code 2(3 clocks); WAIT active LOW; WAIT asserted during delay.

2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning to fixed-latency burst READs. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

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10.2.27 Asynchronous WRITE (ADV# LOW) Followed by Burst READ

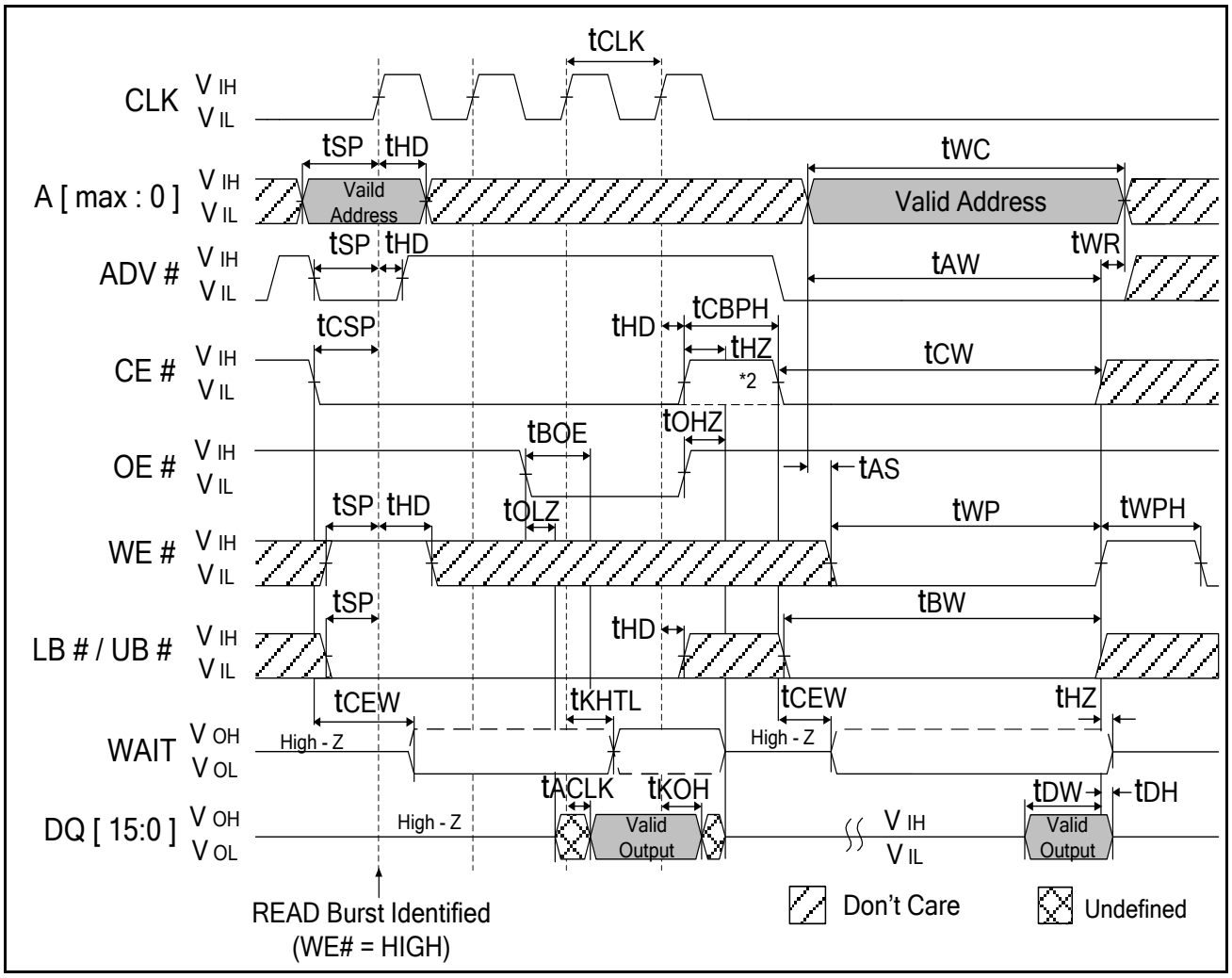


Note : 1. Non-default BCR settings for asynchronous WRITE ,with ADV# LOW, followed by burst READ: Fixed or variable latency; latency code 2(3 clocks); WAIT active LOW; WAIT asserted during delay.

2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning to fixed-latency burst READs. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

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10.2.28 Burst READ Followed By Asynchronous WRITE (WE# - Controlled)

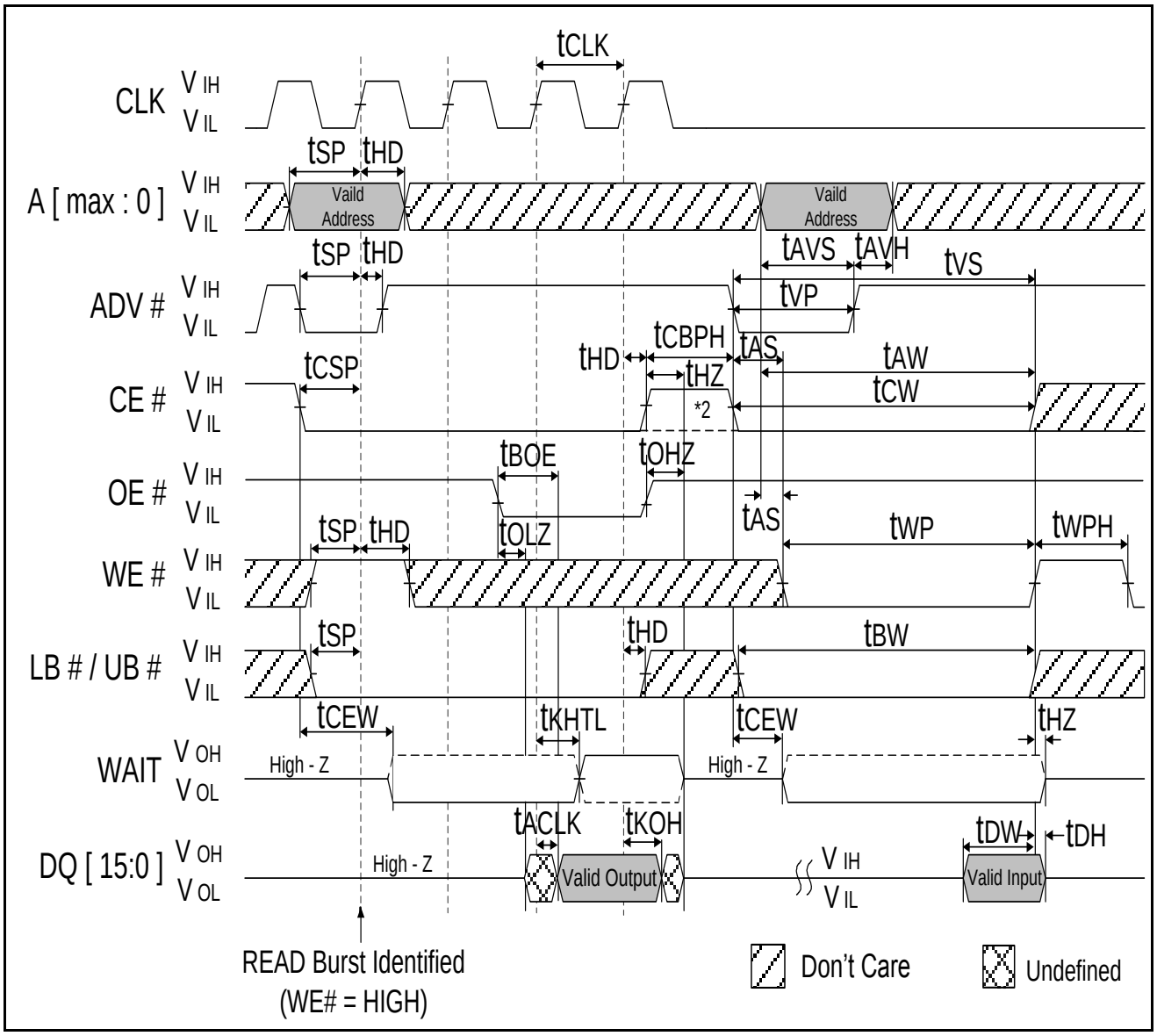


Note : 1. Non-default BCR settings for burst READ followed by asynchronous WE#-controlled WRITE : Fixed or variable latency; latency code 2(3 clocks); WAIT active LOW; WAIT asserted during delay.

2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning from fixed-latency burst READs. Asynchronous operation begins at the falling edge of ADV#.A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

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10.2.29 Burst READ Followed By Asynchronous WRITE Using ADV#

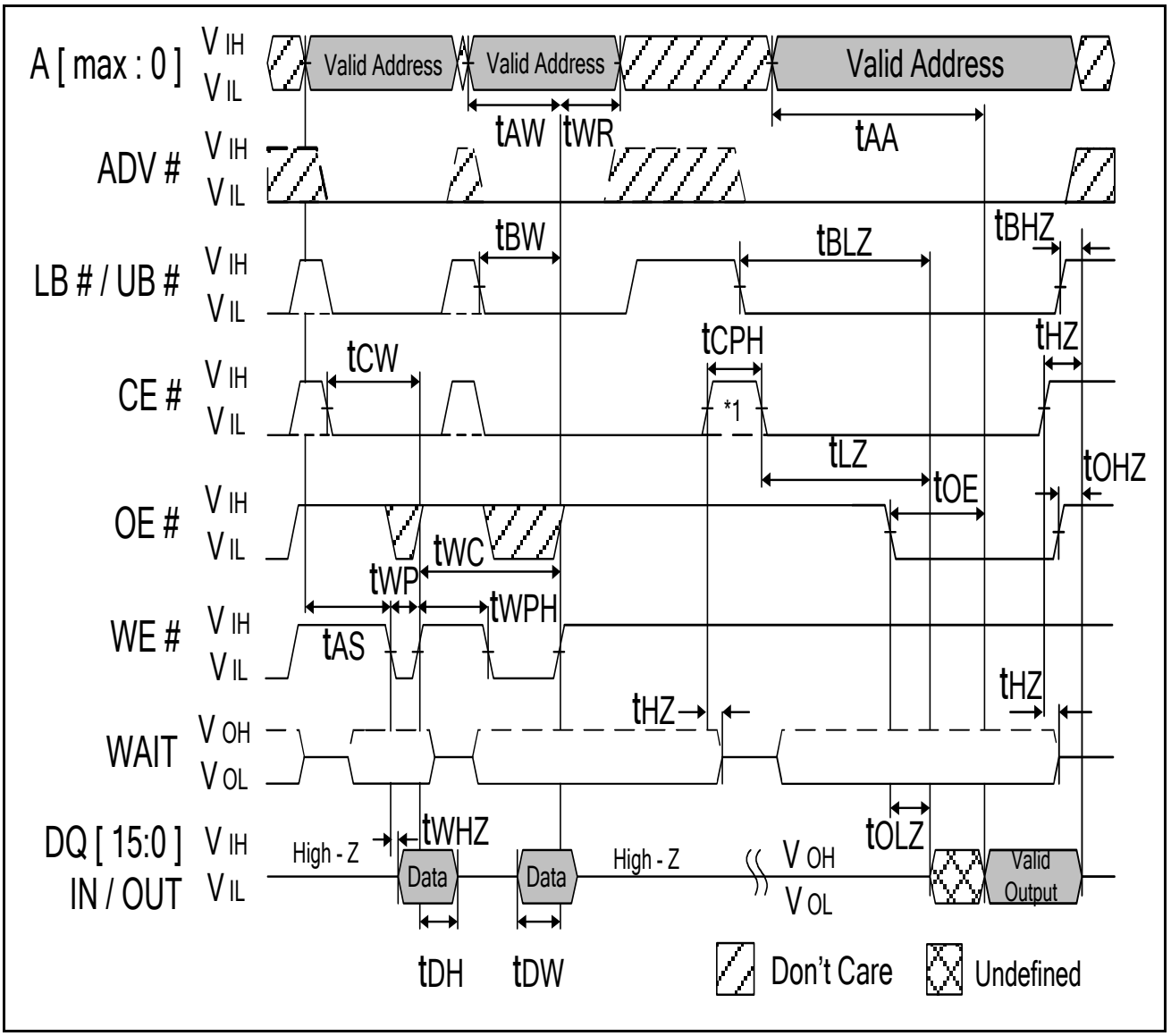


Note : 1. Non-default BCR settings for burst READ followed by asynchronous WRITE using ADV#: Fixed or variable latency; latency code 2(3 clocks); WAIT active LOW; WAIT asserted during delay.

2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning from fixed-latency burst READs. Asynchronous operation begins at the falling edge of ADV#.A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

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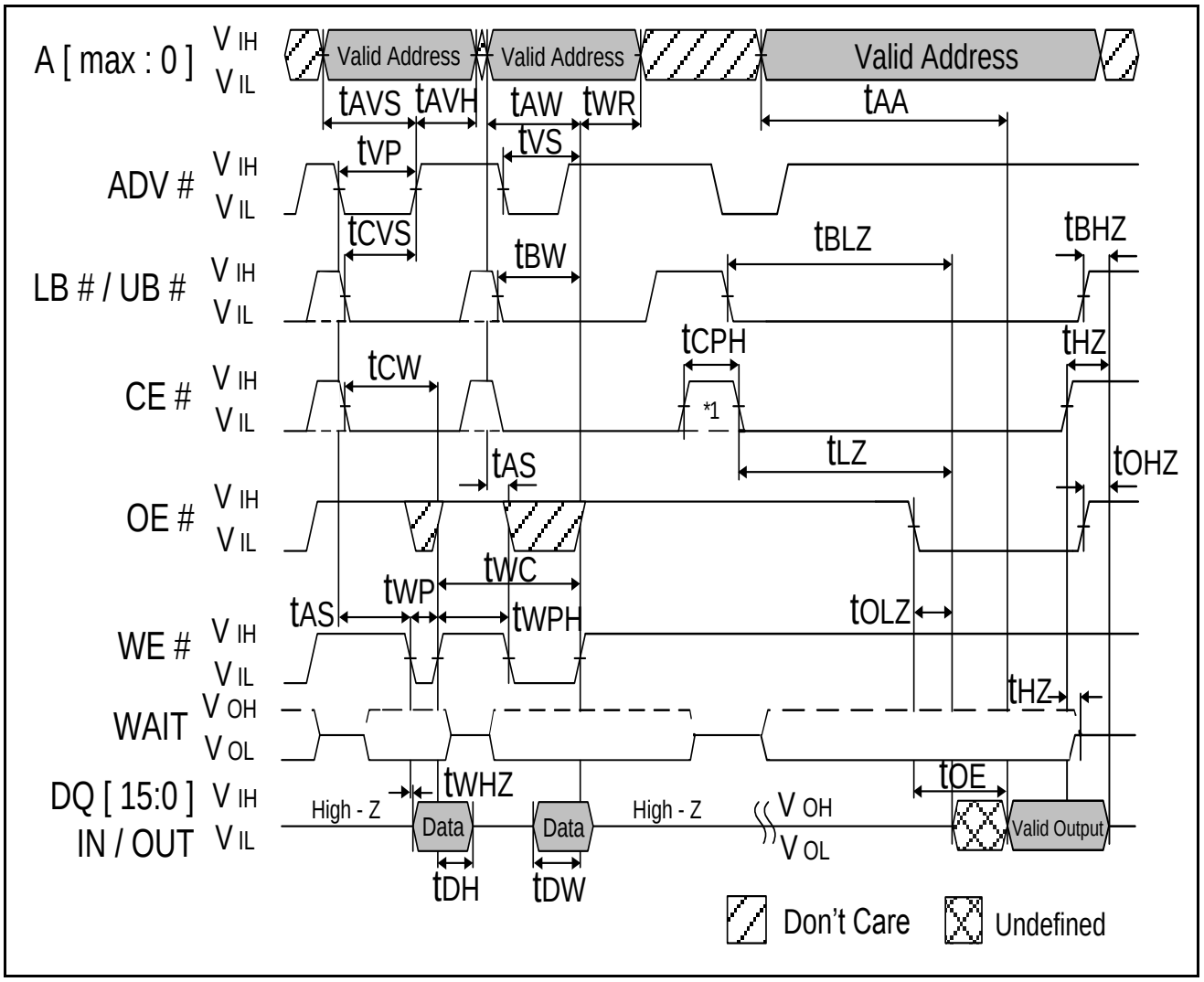
10.2.30 Asynchronous WRITE Followed by Asynchronous READ - ADV# LOW



Note : 1. When configured for synchronous mode (BCR[15] = 0), CE# must remain HIGH for at least 5ns (tCPH) to schedule the appropriate refresh interval, Otherwise, tCPH is only required after CE#-controlled WRITEs.

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10.2.31 Asynchronous WRITE Followed by Asynchronous READ



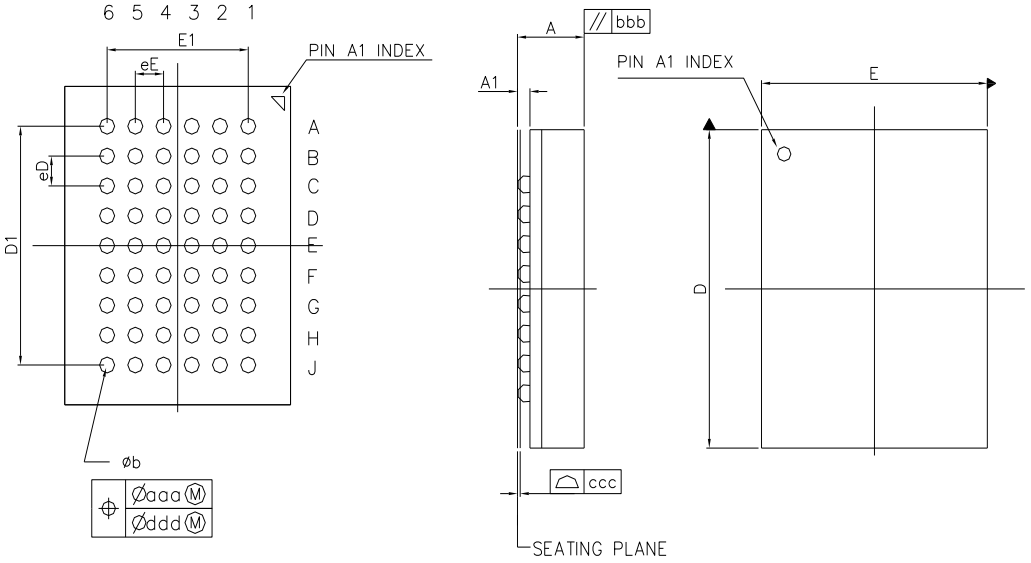
Note : 1. When configured for synchronous mode (BCR[15] = 0), CE# must remain HIGH for at least 5ns (tCPH) to schedule the appropriate refresh interval, Otherwise, tCPH is only required after CE#-controlled WRITEs.

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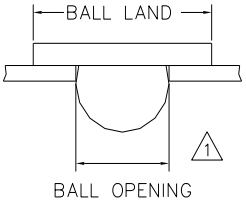
11. PACKAGE DESCRIPTION

11.1 Package Dimension

54 Ball VFBGA (6X8 mm^2,Ball pitch:0.75mm, Ø=0.4mm)



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	---	---	1.0
A1	0.24	0.29	0.34
D	7.90	8.00	8.10
D1		6.00 BSC.	
E	5.90	6.00	6.10
E1		3.75 BSC.	
b	0.35	0.40	0.45
aaa		0.15	
bbb		0.20	
ccc	--	--	0.10
ddd		0.15	
eee		0.08	
e		0.75	



Note:
1. Ball land:0.45mm. Ball opening:0.35mm.
   PCB ball land suggested <=0. 35 mm

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12. REVISION HISTORY

Version	Date	Page	Description
A01-001	02/27/2013	All	Create new document.
A01-002	05/09/2013	All,2	Update part #.
A01-003	05/29/2013	All,2	Update naming typo.

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