64Mb HyperRAM 2.1 x8 pSRAM

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1. FEATURES

- Interface:
  - HyperBus (HyperRAM 2.1)
  - I/O Electrical:
    - LVCMOS_18
    - LVCMOS_15
    - LVCMOS_135
    - LVCMOS_12
- Power supply (VCC):
  - LVCMOS_18: 1.7~2.0V; 1.8V typical
  - LVCMOS_15: 1.425~1.575V; 1.5V typical
  - LVCMOS_135: 1.3~1.45V; 1.35V typical
  - LVCMOS_12: 1.16~1.3V; 1.2V typical
- Maximum clock rate: 250MHz
- Double-Data Rate (DDR)
- Single-ended clock (CK)
- Chip Select (CS#)
- 8-bit data bus (DQ[7:0])
- Hardware reset (RESET#)
- Software Reset
- Read-Write Data Strobe (RWDS)
- Power Saving Modes
  - Hybrid Sleep Mode
  - Deep Power Down Mode
- Configurable output drive strength
  - 25/50/100/200/300 ohm
- Configurable Burst Characteristics
  - Linear burst
  - Wrapped burst lengths:
    - 16 (8 clocks)
    - 32 (16 clocks)
    - 64 (32 clocks)
    - 128 (64 clocks)
    - 1024 (512 clocks)
- Row boundary crossing supported for Read
- Partial Array Refresh Modes
  - Full Array Refresh
  - Partial Array Refresh
- Refresh Feature:
  - Refresh Rate set by CR1 [7]
    - 0b Auto Refresh Rate (default, 1μS/4μS)
    - 1b Fast Refresh Rate (1μS)
- Support package:
  24 balls TFBGA

Operating Temperature

-40°C ≤ TCASE ≤ 85°C

2. ORDER INFORMATION

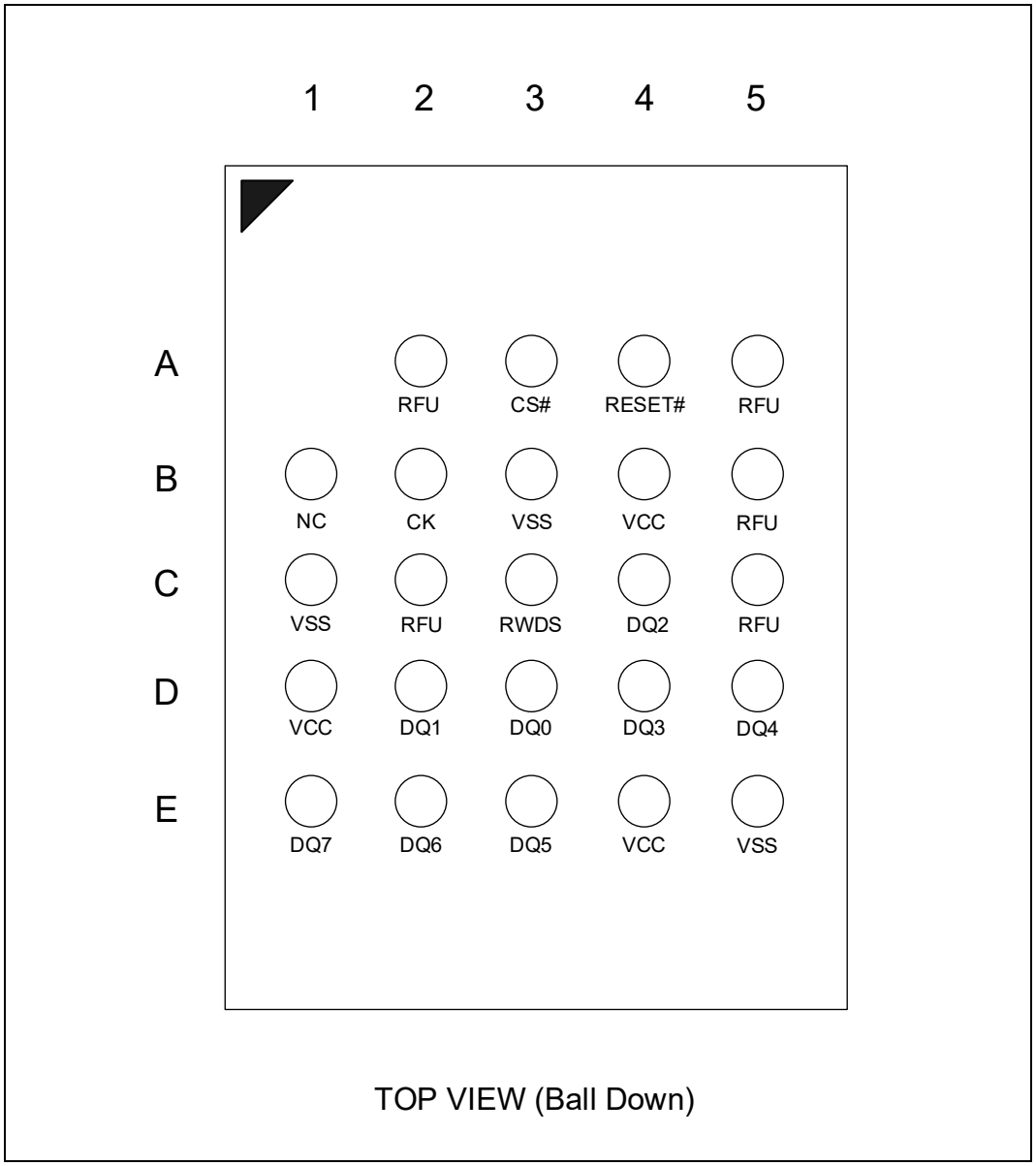
Part Number	VCC	I/O Width	Interface	Others
W956D8NBRA4I	1.8V, 1.5V, 1.35V, 1.2V	8	HyperBus (HyperRAM 2.1)	TFBGA24, 250MHz, -40°C~85°C
W956D8NBRA5I	1.8V, 1.5V, 1.35V, 1.2V	8	HyperBus (HyperRAM 2.1)	TFBGA24, 200MHz, -40°C~85°C

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3. BALL ASSIGNMENT



24 Balls TFBGA, 5x5-1 Ball Footprint, Top View

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4. BALL DESCRIPTIONS

Signal Name	Type	Description
CS#	Input	**Chip Select:** Bus transactions are initiated with a High to Low transition. Bus transactions are terminated with a Low to High transition. The master device has a separate CS# for each slave. When CS# is HIGH, all inputs and outputs other than CS# and RESET# are not monitored.
CK	Input	**Clock:** Single ended clock input. The clock (CK) is used for information capture by a HyperRAM slave device when receiving command, address, or data on the DQ signals. (See Note)
DQ[7:0]	Input / Output	**Data Input / Output:** DQ[7:0] for Command, Address, and Data information are transferred on these signals during Read and Write transactions.
RWDS	Input / Output	**Read Write Data Strobe:** During the Command/Address portion of all bus transactions RWDS is an output and indicates whether additional initial latency is required. High indicates additional latency required, Low indicates no additional latency required. During read data transfer, DQ data output is edge aligned with RWDS. During data transfer in write transactions, RWDS function as a data mask. RWDS corresponds to the data on DQ[7:0]
RESET#	Input, Internal Pull-up	**Hardware Reset:** When Low the slave device will do self-initialization. RWDS and DQ[7:0] are placed into the High-Z state when RESET# is Low. The RESET# input includes a weak pull-up inside the HyperRAM device. If RESET# is left unconnected, it will be pulled up to the High state.
VCC	Power Supply	**Power Supply:** Supplying power for input buffer of CK, CS#, RESET#, DQ[7:0], RWDS, internal circuitry and memory array.
VSS	Power Supply	**Ground:** Ground of VCC.
NC	--	**No Connection**
RFU	No Connect	**Reserved for Future Use**: The ball may be used by a signal in the future. The ball location should be left unconnected and unused by PCB routing channel for future compatibility.

Note:

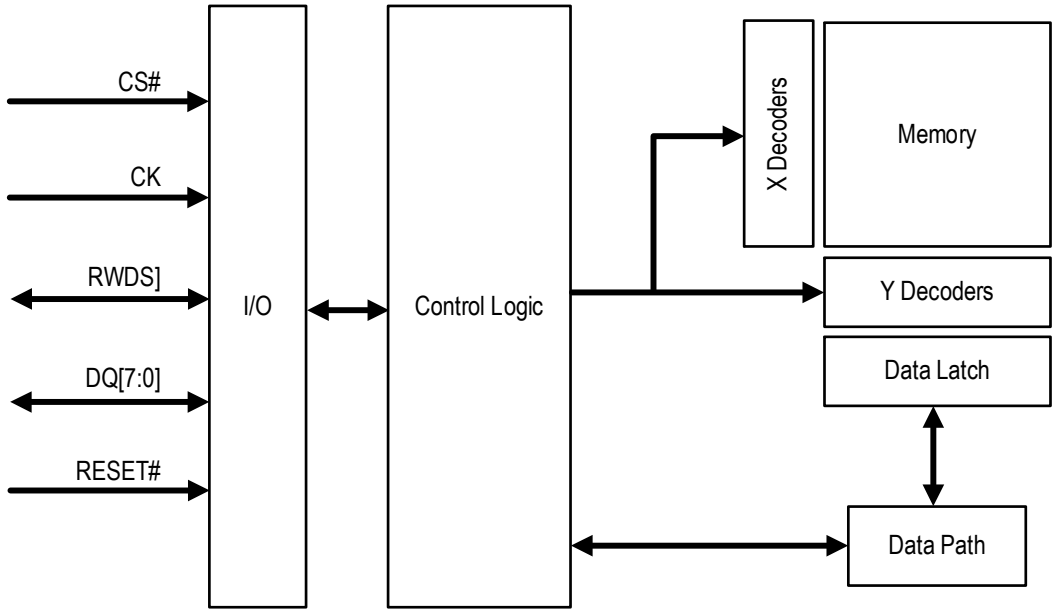
For data read/write and register read operation, the clock input must keep toggling during the period from the start of command-address portion to the end of latency. For register write operation, the clock input must keep toggling at least for 4 cycles.

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5. BLOCK DIAGRAM



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6. FUNCTIONAL DESCRIPTION

6.1 General Description

HyperRAM is a pSRAM device with HyperBus low signal count, Double Data Rate (DDR) interfaces. The DDR protocol transfers two 8-bit data per clock cycle on the DQ input/output pads. HyperBus consists 8-bit wide DQ signals, a 16-bit wide data can be transferred in one clock cycle. All inputs and outputs are LV-CMOS compatible.

6.2 HyperBus

The DDR protocol transfers two data bytes per clock cycle on the DQ input/output signals. A read or write transaction on HyperRAM consists of a series of 16-bit wide, one clock cycle data transfers at the internal HyperRAM array with two corresponding 8-bit wide, one-half-clock-cycle data transfers on the DQ signals.

Command, address, and data information is transferred over the eight HyperBus DQ[7:0] signals. The clock (CK) is used for information capture by a HyperRAM device when receiving command, address, or data on the DQ signals. Command or Address values are center aligned with clock transitions.

Every transaction begins with the assertion of CS# and Command-Address (CA) signals, followed by the start of clock transitions to transfer six CA bytes, followed by initial access latency and either read or write data transfers, until CS# is de-asserted.

Read and write transactions require two clock cycles to define the target row address and burst type, then an initial access latency of t_{ACC}. During the CA part of a transaction, the memory will indicate whether an additional latency for a required refresh time is added to the initial latency by driving the RWDS signal to the High state. During the CA period the third clock cycle will specify the target word address within the target row. During a read (or write) transaction, after the initial data value has been output (or input), additional data can be read from (or written to) the row on subsequent clock cycles in either a wrapped or linear sequence. When the HyperRAM configured in linear burst mode, during read transaction, the device will automatically fetch the next sequential row from the memory array to support a linear burst. When outputting the data crossing the row boundary, the HyperRAM will hold DQ delivery with a wait time for changing active row, accessing the next row in the array while the read data transfer is in progress, to allow a linear sequential burst operation.

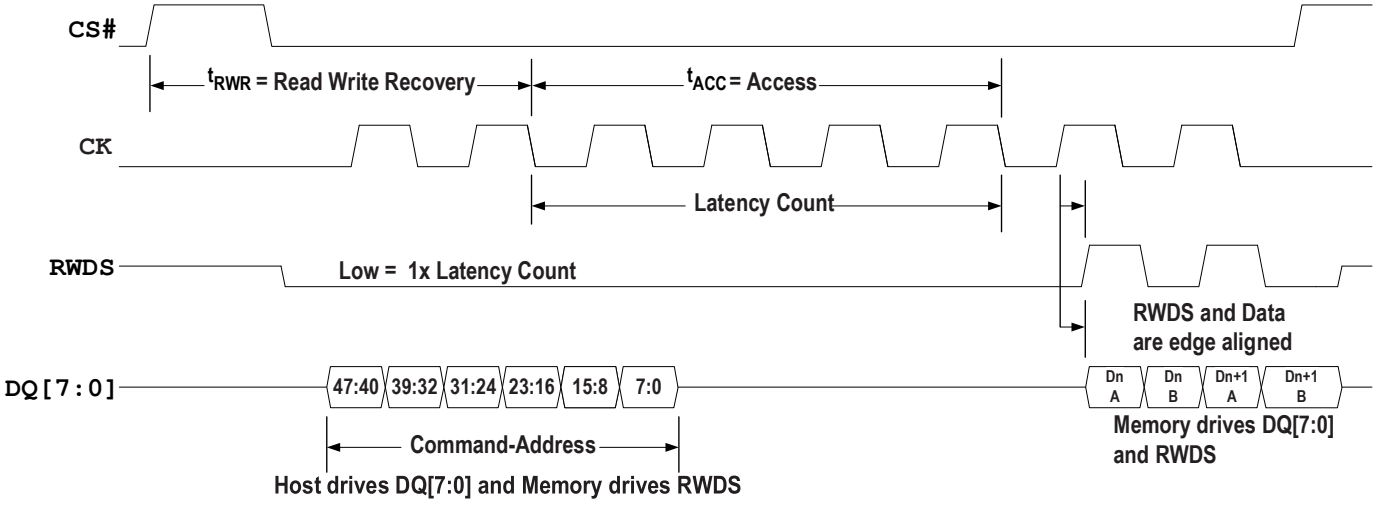


Figure 1 - Read Transaction, Single Initial Latency Count

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The Read/Write Data Strobe (RWDS) are bidirectional signals that indicates:

- When data will start to transfer from a HyperRAM device to the master device in read transactions (initial read latency)
- When data is being transferred from a HyperRAM device to the master device during read transactions (as a source synchronous read data strobe)
- When data may start to transfer from the master device to a HyperRAM device in write transactions (initial write latency)
- Data masking during write data transfers

During the CA transfer portion of a read or write transaction, RWDS acts as an output from a HyperRAM device to indicate whether additional initial access latency is needed in the transaction.
During read data transfers, RWDS is a read data strobe with data values edge aligned with the transitions of RWDS.

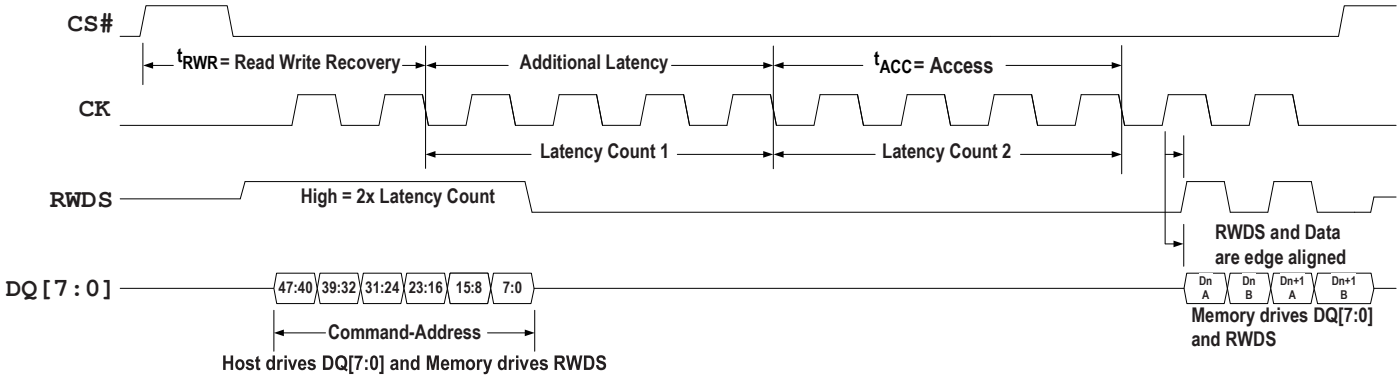


Figure 2 - Read Transaction, Additional Latency Count

During write data transfers, RWDS indicates whether each data byte transfer is masked with RWDS High (invalid and prevented from changing the byte location in a memory) or not masked with RWDS Low (valid and written to a memory). Data masking may be used by the host to byte align write data within a memory or to enable merging of multiple non-word aligned writes in a single burst write. During write transactions, data is center aligned with clock transitions.

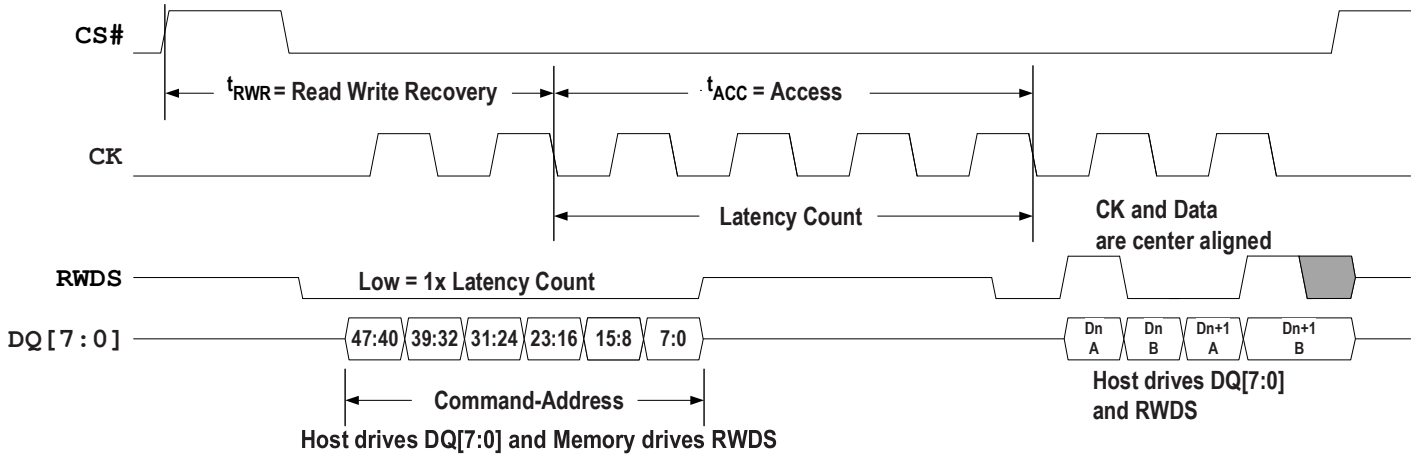


Figure3 - Write Transaction, Single Initial Latency Count

Note: The last write data can be masked or not masked.

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Read and write transactions are burst oriented, transferring the next sequential word during each clock cycle. Each individual read or write transaction can use either a wrapped or linear burst sequence.

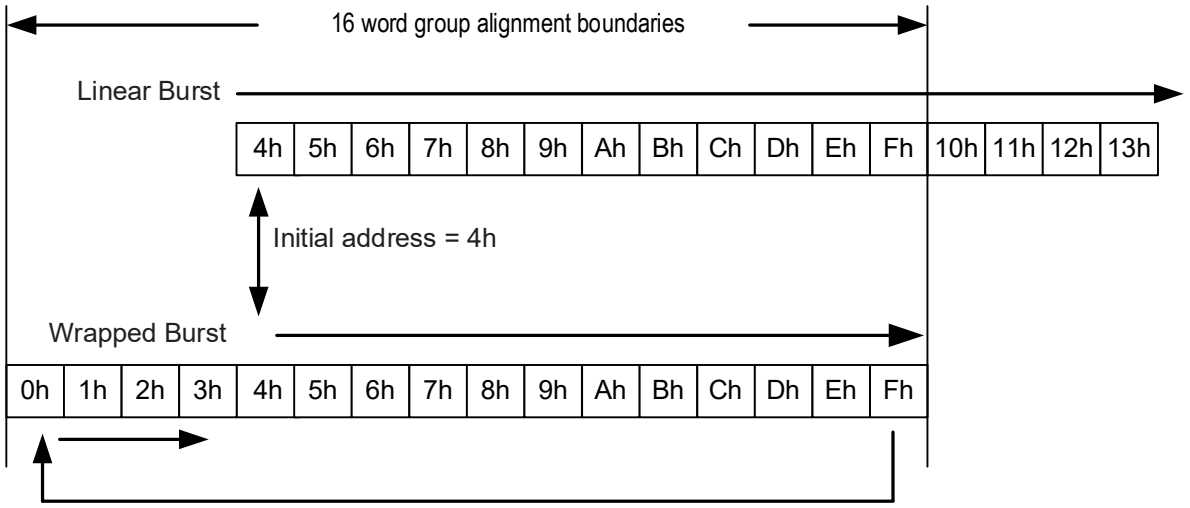


Figure 4 - Linear Versus Wrapped Burst Sequence

During wrapped transactions, accesses start at a selected location and continue to the end of a configured word group aligned boundary, then wrap to the beginning location in the group, then continue back to the starting location. Wrapped bursts are generally used for critical word first cache line fill read transactions.

During linear transactions, accesses start at a selected location and continue in a sequential manner until the transaction is terminated when CS# returns High. Linear transactions are generally used for large contiguous data transfers such as graphic images.

Since each transaction command selects the type of burst sequence for that transaction, wrapped and linear bursts transactions can be dynamically intermixed as needed.

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7. BUS TRANSACTION DETAILS

7.1 Command/Address Bit Assignments

All HyperBus transactions can be classified as either read or write. A bus transaction is started with CS# going Low with clock in idle state. The first three clock cycles transfer three words of Command/Address (CA0, CA1, CA2) information to define the transaction characteristics. The Command/Address words are presented with DDR timing, using the first six clock edges. The following characteristics are defined by the Command/Address information:

- Read or Write transaction
- Address Space: memory array space or register space
  - Register space is used to access Device Identification (ID) registers and Configuration Registers (CR) that identify the device characteristics and determine the slave specific behavior of read and write transfers on the HyperBus.
- Whether a transaction will use a linear or wrapped burst sequence
- The target row (and half-page) address (upper order address)
- The target column (word within half-page) address (lower order address)



Figure 5 - Command-Address (CA) Sequence

Notes:
1. Figure shows the initial three clock cycles of all transactions on the HyperBus.
2. CA information is “center aligned” with the clock during both Read and Write transactions.
3. Data bits in each byte are always in high to low order with bit 7 on DQ7 and bit 0 on DQ0.

Table 1 - CA Bit Assignment to DQ Signals

Signal	CA0[47:40]	CA0[39:32]	CA1[31:24]	CA1[23:16]	CA2[15:8]	CA2[7:0]
DQ[7]	CA[47]	CA[39]	CA[31]	CA[23]	CA[15]	CA[7]
DQ[6]	CA[46]	CA[38]	CA[30]	CA[22]	CA[14]	CA[6]
DQ[5]	CA[45]	CA[37]	CA[29]	CA[21]	CA[13]	CA[5]
DQ[4]	CA[44]	CA[36]	CA[28]	CA[20]	CA[12]	CA[4]
DQ[3]	CA[43]	CA[35]	CA[27]	CA[19]	CA[11]	CA[3]
DQ[2]	CA[42]	CA[34]	CA[26]	CA[18]	CA[10]	CA[2]
DQ[1]	CA[41]	CA[33]	CA[25]	CA[17]	CA[9]	CA[1]
DQ[0]	CA[40]	CA[32]	CA[24]	CA[16]	CA[8]	CA[0]

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Table 2 - Command/Address Bit Assignments

CA Bit#	Bit Name	Bit Function
47	R/W#	Identifies the transaction as a read or write. R/W#=1 indicates a Read transaction R/W#=0 indicates a Write transaction
46	Address Space (AS)	Indicates whether the read or write transaction accesses the memory or register space. AS=0 indicates memory space AS=1 indicates the register space The register space is used to access device ID and Configuration registers.
45	Burst Type	Indicates whether the burst will be linear or wrapped. Burst Type=0 indicates wrapped burst Burst Type=1 indicates linear burst
44-16	Row & Upper Column Address	Row & Upper Column component of the target address: System word address bits A31-A3 Any upper Row address bits not used by a particular device density should be set to 0 by the host controller master interface. The size of Rows and therefore the address bit boundary between Row and Column address is slave device dependent.
15-3	Reserved	Reserved for future column address expansion. Reserved bits are don't care in current HyperRAM devices but should be set to 0 by the host controller master interface for future compatibility.
2-0	Lower Column Address	Lower Column component of the target address: System word address bits A2-A0 selecting the starting data within a half-page.

Notes:

1. The Column address selects the burst transaction starting word location within a Row. The Column address is split into an upper and lower portion. The upper portion selects an 8-word (16-byte) Half-page and the lower portion selects the word within a Half-page where a read or write transaction burst starts.
2. The initial read access time starts when the Row and Upper Column (Half-page) address bits are captured by a slave interface. Continuous linear read burst is enabled by memory devices internally interleaving access to 16 bytes half-pages.

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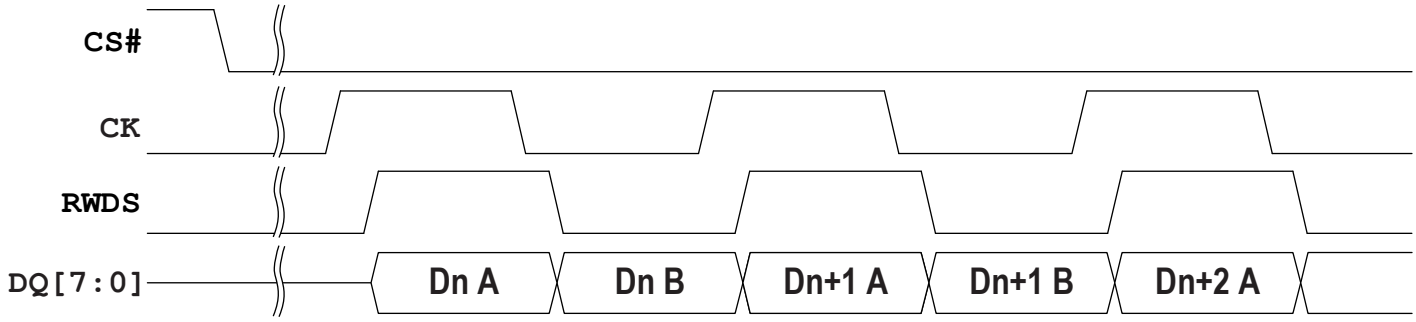


Figure 6 - Data Placement during a Read Transaction

Notes:

1. Figure shows a portion of a Read transaction on the HyperBus.
2. Data is “edge aligned” with the RWDS serving as a read data strobe during read transactions.
3. Data is always transferred in full word increments (word granularity transfers).
4. Word address increments in each clock cycle. Byte A is between RWDS rising and falling edges and is followed by byte B between RWDS falling and rising edges, of each word.
5. Data bits in each byte are always in high to low order with bit 7 on DQ7 and bit 0 on DQ0.

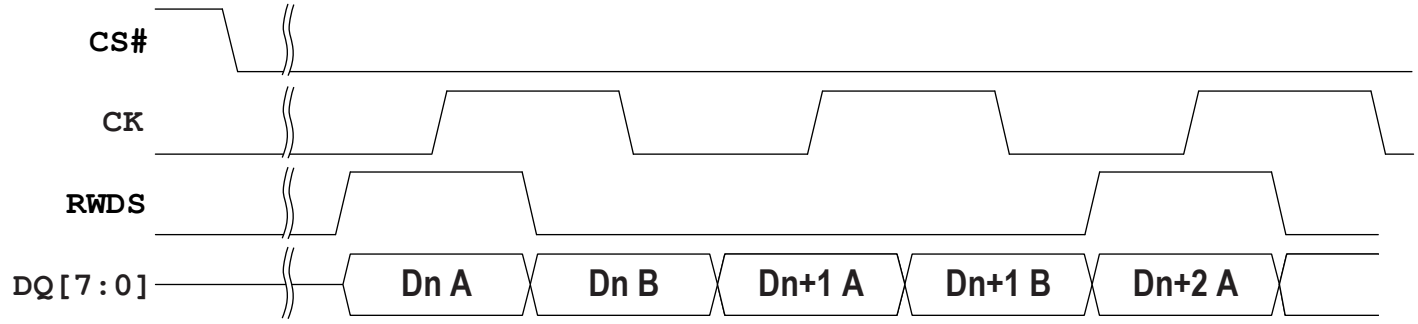


Figure 7 - Data Placement during a Write Transaction

Notes:

1. Figure shows a portion of a Write transaction on the HyperBus.
2. Data is “center aligned” with the clock during a Write transaction.
3. RWDS functions as a data mask during write data transfers with initial latency. Masking of the first and last byte is shown to illustrate an unaligned 3 byte write of data.
4. RWDS is not driven by the master during write data transfers with zero initial latency. Full data words are always written in this case. RWDS may be driven Low or left High-Z by the slave in this case.

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7.2 Read Transactions

The HyperRAM master begins a transaction by driving CS# Low while clock is idle. The clock then begins toggling while CA words are transferred.

In CA0 word, CA[47] = 1 indicates that a Read transaction is to be performed. CA[46] = 0 indicates the memory space is being read or CA[46] = 1 indicates the register space is being read. CA[45] indicates the burst type (wrapped or linear). Read transactions can begin the internal array access as soon as the row and upper column address has been presented in CA0 word and CA1 word (CA[47:16]). CA2 word (CA[15:0]) identifies the target word address within the chosen row.

The HyperRAM master then must continue clocking for a number of cycles defined by the latency count setting in Configuration Register 0. The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is Low during the CA cycles, one latency count is inserted. If RWDS is High during the CA cycles, an additional latency count is inserted. Once these latency clocks have been completed, the HyperRAM device starts to simultaneously transition the Read-Write Data Strobe (RWDS) and output the target data.

New data is output edge aligned with every transition of RWDS. Data will continue to be output as long as the host continues to transition the clock while CS# is Low.

Wrapped bursts will continue to wrap within the burst length and linear burst will output data in a sequential manner across row boundaries. When a linear burst read reaches the last address in the array, continuing the burst beyond the last address will provide data from the beginning of the address range. Meanwhile, when a linear burst read crossing row boundaries of memory array, the HyperRAM device will stop RWDS transitions with keeping RWDS Low, between the deliveries of words, in order to insert latency between words.

Read transfers can be ended at any time by bringing CS# High when the clock is idle. The clock is not required to be free-running while CS# is High. The clock may remain idle while CS# is High.

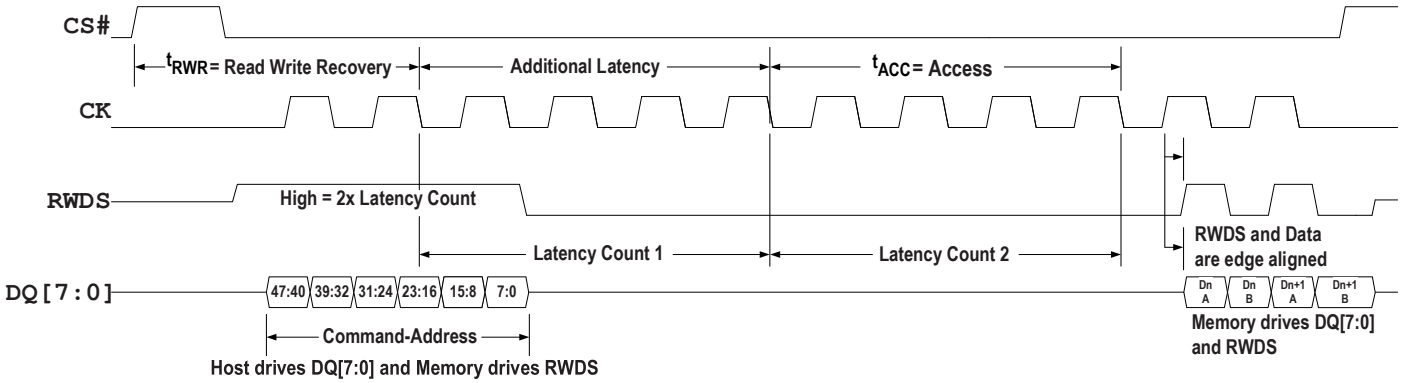


Figure 8 - Read Transaction with Additional Initial Latency

Notes:

1. Transactions are initiated with CS# falling while CK=Low.
2. CS# must return High before a new transaction is initiated.
3. Read access array starts once CA[23:16] is captured.
4. The read latency is defined by the initial latency value in a configuration register.
5. In this read transaction example the initial latency count was set to four clocks.
6. In this read transaction RWDS High indication during CA delays output of target data by an additional four clocks.
7. The memory device drives RWDS during read transactions.
8. For register read, the output data Dn A[7:0] is RG[15:8], Dn B[7:0] is RG[7:0], Dn+1 A[7:0] is RG[15:8], Dn+1 B[7:0] is RG[7:0].

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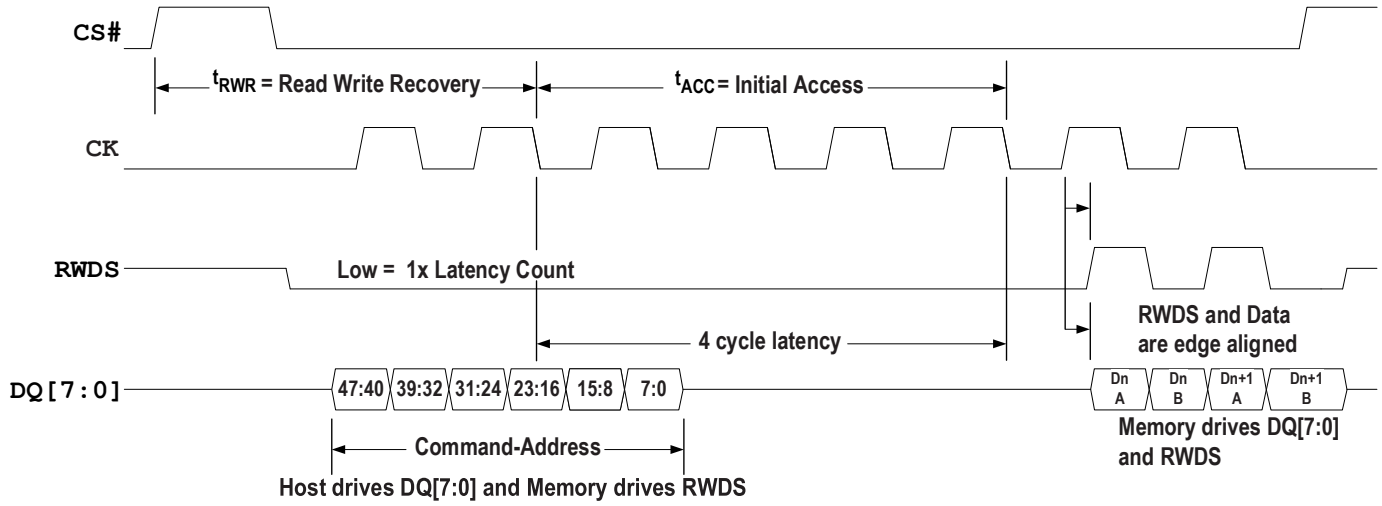


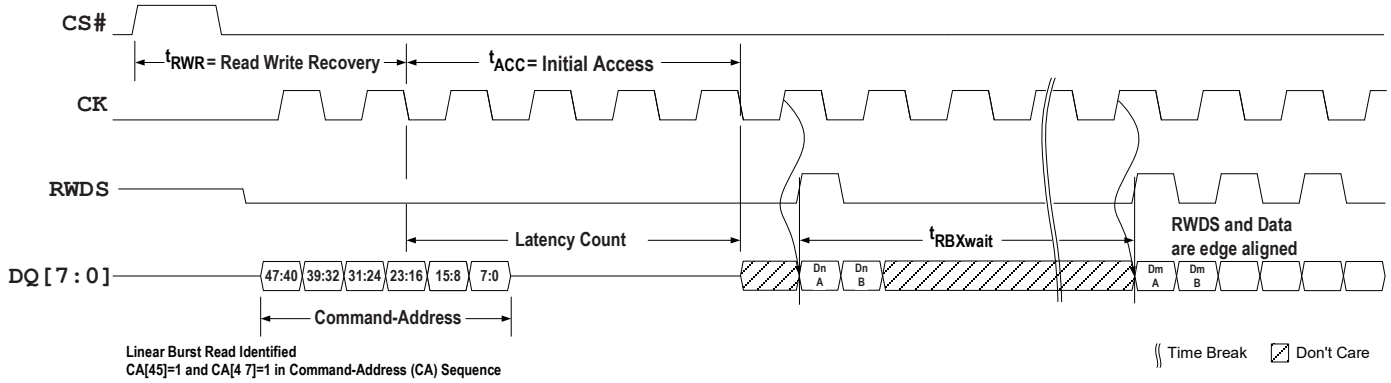
Figure 9 - Read Transaction without Additional Initial Latency

Note:

1. RWDS is Low during the CA cycles. In this Read Transaction there is a single initial latency count for read data access because, this read transaction does not begin at a time when additional latency is required by the slave.

7.2.1 Linear Burst Read with Row Boundary Crossing

A Linear Burst Read command is initiated when first clock cycle of Command-Address (CA) sequence phase, CA[45]=1 and CA[47]=1. The Linear Burst Read operation may cross row boundaries as shown in below figure.



Notes:

1. When the chip is crossing the row boundary, the clock input must keep toggling and is not allowed to be stop.
2. The system address bits of A8~A0 for the data word (Dn) of the end of row is 1FFh.

Figure 10: Linear Burst Read with Row Boundary Crossing

As the Figure 10 showing, for normally perform the read transaction with row boundary crossing, during the whole period of read transaction, the CS# input must keep LOW and the CK input must keep toggling. Meanwhile, the RWDS will keep LOW and DQ[7:0] will be invalid after the end of row data out for a time period of tRBXwait. On the other hand, it is not recommended to terminate the read transaction by pull CS# HIGH or holding the read transaction by stopping CK input during the time period of tRBXwait because that might cause uncertain operation regarding internal refresh and data accessing.

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7.3 Write Transactions (Memory Array Write)

The HyperRAM master begins a transaction by driving CS# Low while clock is idle. Then the clock begins toggling while CA words are transferred.

In CA0 word, CA[47] = 0 indicates that a Write transaction is to be performed. CA[46] = 0 indicates the memory space is being written. CA[45] indicates the burst type (wrapped or linear). Write transactions can begin the internal array access as soon as the row and upper column address has been presented in CA0 word and CA1 word (CA[47:16]). CA2 word (CA[15:0]) identifies the target word address within the chosen row.

The HyperRAM master then must continue clocking for a number of cycles defined by the latency count setting in configuration register 0. The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is Low during the CA cycles, one latency count is inserted. If RWDS is High during the CA cycles, an additional latency count is inserted.

Once these latency clocks have been completed the HyperRAM master starts to output the target data. Write data is center aligned with the clock edges. The first byte of data in each word is captured by the memory on the rising edge of CK and the second byte is captured on the falling edge of CK.

During the CA clock cycles, RWDS is driven by the memory.

During the write data transfers, RWDS is driven by the host master interface as a data mask. When data is being written and RWDS is High the data will be masked and the array will not be altered. When data is being written and RWDS is Low the data will be placed into the array. Because the master is driving RWDS during write data transfers, neither the master nor the HyperRAM device are able to indicate a need for latency within the data transfer portion of a write transaction. The acceptable write data burst length setting is also shown in configuration register 0.

Data will continue to be transferred as long as the HyperRAM master continues to transition the clock while CS# is Low. Legacy format wrapped bursts will continue to wrap within the burst length. Linear burst accepts data in a sequential manner, but it is not allowed across row boundary.

Write transfers can be ended at any time by bringing CS# HIGH when the clock is idle. The clock is not required to be free-running while CS# is High. The clock may remain idle while CS# is High.

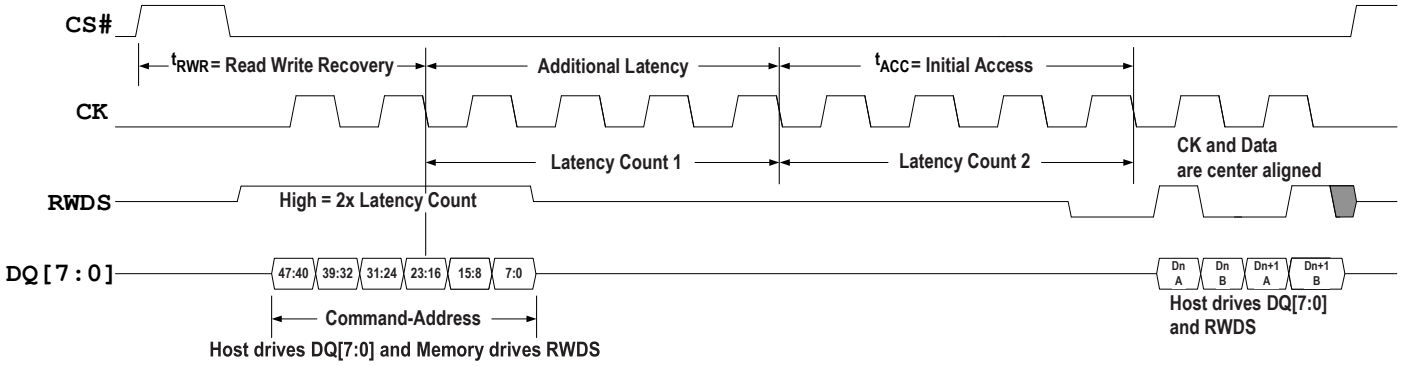


Figure 11 - Write Transaction with Additional Initial Latency

Notes:

1. Transactions are initiated with CS# falling while CK=Low.
2. CS# must return High before a new transaction is initiated.
3. During CA, RWDS is driven by the memory and indicates whether additional latency cycles are required.
4. In this example, RWDS indicates that additional initial latency cycles are required.
5. At the end of CA cycles the memory stops driving RWDS to allow the host HyperRAM master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave.
6. During data transfer, RWDS is driven by the host to indicate which bytes of data should be either masked or loaded into the array.
7. The figure shows RWDS masking byte Dn A and byte Dn+1 B to perform an unaligned word write to bytes Dn B and Dn+1 A.

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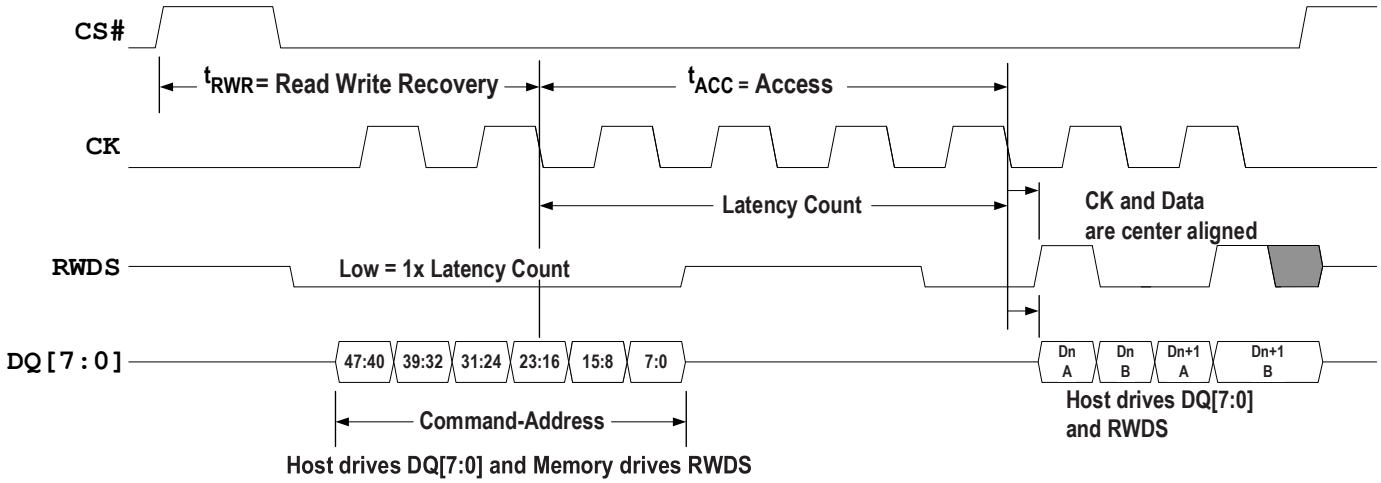


Figure 12 - Write Transaction without Additional Initial Latency

Notes:

1. During CA, RWDS is driven by the memory and indicates whether additional latency cycles are required.
2. In this example, RWDS indicates that there is no additional latency required.
3. At the end of CA cycles the memory stops driving RWDS to allow the host HyperRAM master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave.
4. During data transfer, RWDS is driven by the host to indicate which bytes of data should be either masked or loaded into the array.
5. The figure shows RWDS masking byte Dn A and byte Dn+1 B to perform an unaligned word write to bytes Dn B and Dn+1 A.

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7.4 Write Transactions without Initial Latency (Register Write)

A Write transaction starts with the first three clock cycles providing the Command/Address information indicating the transaction characteristics. CA0 word may indicate that a Write transaction is to be performed and also indicates the address space and burst type (wrapped or linear).

Writes without initial latency are used for register space writes. HyperRAM device write transactions with zero latency mean that the CA cycles are followed by write data transfers. Writes with zero initial latency, do not have a turnaround period for RWDS. The HyperRAM device will always drive RWDS during the CA period to indicate whether extended latency is required for a transaction that has initial latency. However, the RWDS is driven before the HyperRAM device has received the first byte of CA i.e. before the HyperRAM device knows whether the transaction is a read or write to register space. In the case of a write with zero latency, the RWDS state during the CA period does not affect the initial latency of zero. Since master write data immediately follows the CA period in this case, the HyperRAM device may continue to drive RWDS Low or may take RWDS to High-Z during write data transfer. The master must not drive RWDS during Writes with zero latency. Writes with zero latency do not use RWDS as a data mask function. All bytes of write data are written (full word writes).

The first byte of data in each word is presented on the rising edge of CK and the second byte is presented on the falling edge of CK. Write data is center aligned with the clock inputs. Write transfers can be ended at any time by bringing CS# High when clock is idle. The clock is not required to be free-running.

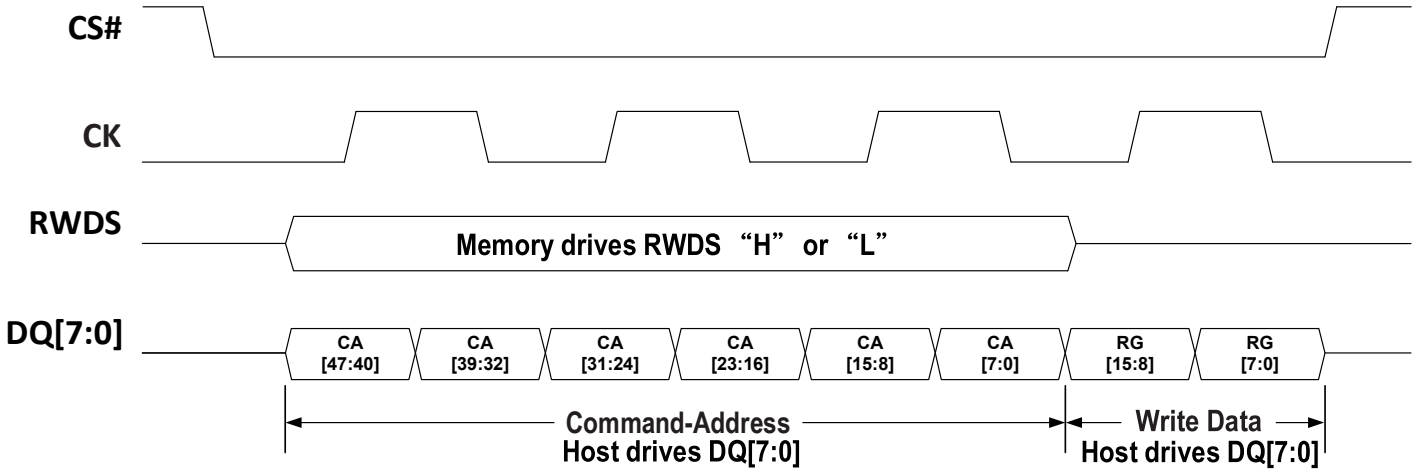


Figure 13 - Write Operation without Initial Latency (Register Write)

Note:

1. RWDS not driven by the master during write data transfers with zero initial latency. Full data are always written in this case. RWDS may be driven Low or left High-Z by the HyperRAM during write data transfer.

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8. MEMORY SPACE

8.1 HyperRAM Memory Space addressing

Table 3 - Memory Space Address Map (word based – 16-bits)

Unit Type	Count	System Word Address Bits	CA Bits	Notes
Rows within 64 Mb device	8192 (Rows)	A21~A9	34~22	
Row	1 (row)	A8~A3	21~16	512 (word addresses) 1K bytes
Half-Page	8 (word addresses)	A2~A0	2~0	8 (word addresses) (16 bytes)

Table 4 - Memory Space Address Map

		64Mb
Row Address	System Data Address Bits	A21~A9
	CA Bits	34~22
Column Address	System Data Address Bits	A8~A0
	CA Bits	21~16; 2~0
Half-Page (HP) Address	System Data Address Bits	A8~A3
	CA Bits	21~16
Word of Half-Page Address	System Data Address Bits	A2~A0
	CA Bits	2~0

Notes:

1. Each row has 64 Half-pages. Each Half-page has 8 words. Each column has 512 words (1K bytes).
2. Half-Page address is also named as upper column address. Word of Half-page address is also named as lower column address.

8.2 Density and Row Boundaries

The memory array size (density) of the device can be determined from the total number of system address bits used for the row and column addresses as indicated by the Row Address Bit Count and Column Address Bit Count fields in the ID0 register.

A 64-Mbit HyperRAM device has 9 column address bits and 13 row address bits. There are 22 address bits for addressing a memory space of 4M (= 2^{22}) words which is equal to 8M bytes (=64M bits).

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9. REGISTER SPACE

9.1 HyperRAM Register Addressing

Table 5 - Register Space Address Map

Register	System Address	—	—	—	31~27	26~19	18~11	10~3	—	2~0
	CA Bits	47	46	45	44~40	39~32	31~24	23~16	15~8	7~0
Identification Register 0 (read only)		C0h or E0h				00h	00h	00h	00h	00h
Identification Register 1 (read only)		C0h or E0h				00h	00h	00h	00h	01h
Configuration Register 0 Read		C0h or E0h				00h	01h	00h	00h	00h
Configuration Register 0 Write		60h				00h	01h	00h	00h	00h
Configuration Register 1 Read		C0h or E0h				00h	01h	00h	00h	01h
Configuration Register 1 Write		60h				00h	01h	00h	00h	01h

Notes:
1. When CA[46] is 1, a read or write transaction accesses the Register Space.
2. For register space read, CA[45] may be either 0 or 1 for either wrapped or linear read.
3. For linear single word register writes, CA[45] must be 1.

9.2 Register Space Access

Register default values are loaded upon power-up or hardware reset. The registers can be altered at any time while the device is in the standby state.

Loading a register is accomplished with write transaction without initial latency using a single 16-bit word write transaction.

Each register is written with a separate single word write transaction. Register write transactions have zero latency, the single word of data immediately follows the CA. RWDS is not driven by the host during the write because RWDS is always driven by the memory during the CA cycles to indicate whether a memory array refresh is in progress. Because a register space write goes directly to a register, rather than the memory array, there is no initial write latency, related to an array refresh that may be in progress. In a register write, RWDS is also not used as a data mask because both bytes of a register are always written and never masked.

Reserved register fields must be written with their default value. Writing reserved fields with other than default values may produce undefined results.

Note: The host must not drive RWDS during a write to register space.

Note: The RWDS signal is driven by the memory during the CA period based on whether the memory array is being refreshed. This refresh indication does not affect the writing of register data.

Note: The RWDS signal returns to high impedance after the CA period. Register data is never masked. Both data bytes of the register data are loaded into the selected register.

Reading of a register is accomplished with read transaction with single or double initial latency using a single 16 bit read transaction. If more than one word is read, the same register value is repeated in each word read. The contents of the register are returned in the same manner as reading array data, with one or two latency counts, based on the state of RWDS during the CA period. The latency count is defined in the Configuration Register 0 Read Latency field (CR0[7:4]).

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9.3 Device Identification Registers

There are two read only, non-volatile, word registers, that provide information on the device selected when CS# is low. The device information fields identify:

- Manufacture
- Type
- Density
  - Row address bit count
  - Column address bit count

Table 6 - ID Register 0 Bit Assignments

Bits	Function	Settings (Binary)
[15:13]	Reserved	000b - (default)
[12:8]	Row Address Bit Count	01100b - Thirteen Row address bits (64 Mbit)
[7:4]	Column Address Bit Count	1000b - Nine column address bits
[3:0]	Manufacturer	0110b - Winbond Others - Reserved

Table 7 - ID Register 1 Bit Assignments

Bits	Function	Settings (Binary)
[15:8]	Reserved	0000_0000b (default)
[7]	Die Status	0b - Good die (default) 1b - Fail die
[6:4]	Reserved	000b (default)
[3:0]	Device Type	0010b – x8, HyperRAM 2.1 Others - Reserved

9.4 Configuration Register 0

Configuration Register 0 (CR0) is used to define the power state and access protocol operating conditions for the HyperRAM device. Configurable characteristics include:

- Wrapped Burst Length (16, 32, 64, 128 or 1024 data aligned and length data group)
- Wrapped Burst Type
  - Legacy wrapped burst (sequential access with wrap around within a selected length and aligned group)
- Initial Latency
- Variable Latency
  - Whether an array read or write transaction will use fixed or variable latency. If fixed latency is selected the memory will always indicate a refresh latency and delay the read data transfer accordingly. If variable latency is selected, latency for a refresh is only added when a refresh is required at the same time a new transaction is starting.
- Output Drive Strength
- Deep Power Down Mode

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Table 8 - Configuration Register 0 Bit Assignments

CR0 Bit	Function	Settings (Binary)
[15]	Deep Power Down Enable	1b - Normal operation (default) 0b - Writing 0 to CR0[15] causes the device to enter Deep Power Down (DPD) Note: 1: HyperRAM will automatically set the value of CR0[15] to “1” after exit DPD.
[14:12]	Drive Strength*2	000b - 25 ohms (default) 001b - 50 ohms 010b - 100 ohms 011b - 200 ohms 100b - 300 ohms
[11:9]	Reserved	111b - Reserved (default) Reserved for Future Use. When writing this register, these bits should be set to 1 for future compatibility.
[8]	Burst Length	Burst Length select bits with CR0[1:0]
[7:4]	Initial Latency	0000b - 5 Clock Latency for clock rate ≤ 133MHz 0001b - 6 Clock Latency for clock rate ≤ 166MHz 0010b - 7 Clock Latency for clock rate ≤ 200MHz (default) 0101b - 10 Clock Latency for clock rate ≤ 250MHz 1110b - 3 Clock Latency for clock rate ≤ 85MHz 1111b - 4 Clock Latency for clock rate ≤ 104MHz Others - Reserved
[3]	Fixed Latency Enable	0b - Variable Latency. 1 or 2 times Initial Latency depending on RWDS during CA cycles. 1b - Fixed Latency. Fixed 2 times Initial Latency (default)
[2]	Wrapped Burst*1	1b: Wrapped burst sequences in legacy wrapped burst manner (default) 0b: Reserved
[1:0]	Burst Length	**CR0[8,1,0]** 011b - 1024 100b - 128 101b - 64 110b - 16 111b - 32 (default) Others - Reserved

Notes:

1. If CA[45]=1 Linear burst is set, CR0[2] setting is don’t care.
2. The drive strength value is determined under a 1.8V condition and is dependent on the power supply voltage. In general, as the power supply voltage decreases, the drive strength also decreases.

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9.4.1 CR0[15] Deep Power Down

When the HyperRAM device is not needed for system operation, it may be placed in a very low power consuming state called Deep Power Down (DPD), by writing 0 to CR0[15]. When CR0[15] is cleared to 0, the device enters the DPD state within t_{DPDIN} time and all refresh operations stop. The data in memory cell would be lost, (becomes invalid without refresh) during DPD state. Exiting DPD requires driving CS# Low then High, POR, or a reset. Only CS# and RESET# signals are monitored during DPD mode. All register content might be lost in Deep Power Down State.

9.4.2 CR0[14:12] Drive Strength

DQ and RWDS signal line loading, length, and impedance vary depending on each system design. Configuration register bits CR0[14:12] provide a means to adjust the output impedance of DQ[7:0] and RWDS signal to customize the DQ and RWDS signal impedance to the system conditions to minimize high speed signal behaviors such as overshoot, undershoot, and ringing. The default POR or reset configuration value is 000b to select the lowest value of the available output impedance options.

The impedance values shown are typical for both pull-up and pull-down drivers at typical silicon process conditions, nominal operating voltage and temperature. The impedance values may vary from the typical values depending on the Process, Voltage, and Temperature (PVT) conditions.

Each system design should evaluate the data signal integrity across the operating voltage and temperature ranges to select the best drive strength settings for the operating conditions.

9.4.3 CR0[7:4] Initial Latency

Memory Space read and write transactions or Register Space read transactions require some initial latency to open the row selected by the CA. This initial latency is t_{ACC}. The number of latency clocks needed to satisfy t_{ACC} depends on the HyperRAM clock input frequency. The value in CR0[7:4] selects the number of clocks for initial latency. The host system may set a proper initial latency value that may be more optimal for the system.

In the event a distributed refresh is required at the time a Memory Space read or write transaction or Register Space read transaction begins, the RWDS signal goes High during the CA period to indicate that an additional initial latency is being inserted to allow a refresh operation to complete before opening the selected row.

Register Space write transactions always have zero initial latency. RWDS may be High or Low during the CA period. The level of RWDS during the CA period does not affect the placement of register data immediately after the CA, as there is no initial latency needed to capture the register data. A refresh operation may be performed in the memory array in parallel with the capture of register data.

9.4.4 CR0[3] Fixed Latency

A configuration register option bit CR0[3] is provided to make all Memory Space read and write transactions or Register Space read transactions require the same initial latency by always driving RWDS High during the CA to indicate that two initial latency periods are required. This fixed initial latency is independent of any need for a distributed refresh, it simply provides a fixed (deterministic) initial latency for all of these transaction types. The fixed latency option may simplify the design of some HyperRAM memory controllers or ensure deterministic transaction performance. Fixed latency is the default POR or reset configuration. The system may clear this configuration bit to disable fixed latency and allow variable initial latency with RWDS driven High only when additional latency for a refresh is required.

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9.4.5 CR0[2] Wrapped Burst

Legacy Wrap Burst

Set CR0[2]=1 will enable the HyperRAM perform legacy wrapped operation. A legacy wrapped burst transaction accesses memory within a group of words aligned on data boundary matching the length of the configured group. Wrapped access groups can be configured as 16, 32, 64, 128, or 1024 data alignment and length. During wrapped transactions, access starts at the CA selected location within the group, continues to the end of the configured data group aligned boundary, then wraps around to the beginning location in the group, then continues back to the starting location. Wrapped bursts are generally used for critical word first instruction or data cache line fill read accesses.

Table 9 - Example Wrapped Burst Sequences (HyperRAM Addressing)

Burst Type	Wrap Boundary (bytes)	Start Address (Hex)	Sequence of Word Addresses (Hex)
Wrap 16	16	XXXXXX02	02, 03, 04, 05, 06, 07, 00, 01, ...
Wrap 16	16	XXXXXX0C	0C, 0D, 0E, 0F, 08, 09, 0A, 0B, ...
Wrap 32	32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, ...
Wrap 64	64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, ...
Wrap 64	64	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, ...
Wrap 1024	1024	XXXXX003	003, 004, 005, 006, 007, 008, ..., 07E, 07F, 080, ..., 0FE, 0FF, 100, 101, 102, 103, 104, 105, 106, ..., 17E, 17F, 180, ..., 1FE, 1FF, 000, 001, 002, ...
Linear	Linear Burst	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, ...

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9.5 Configuration Register 1

Configuration Register 1 (CR1) is used to define the refresh array size, refresh rate, Hybrid Sleep and Software Reset for the HyperRAM device. Configurable characteristics include:

- Software Reset
- Set Refresh Rate
- Hybrid Sleep State
- Partial Array Refresh
- Refresh Rate

Table 10 - Configuration Register 1 Bit Assignments

CR1 Bit	Function	Settings (Binary)
[15:12]	Software Reset	1010b - Software Reset 1111b - No execute Software Reset. (default) For additional information see11.3.7 **"Software Reset"** section.
[11-8]	Reserved	1111b - Reserved (default) When writing this register, these bits should keep 1111b for future compatibility.
[7]	Set Refresh Rate	0b - Auto Refresh Rate (temperature dependence) 1b - Set to Fast Refresh Rate
[6]	Master Clock Type	1b - Single Ended - CK (default)
[5]	Hybrid Sleep	0b - Normal operation (default) 1b - Writing 1 to CR1[5] causes the device to enter Hybrid Sleep (HS) State
[4:2]	Partial Array Refresh	000b - Full Array (default) 001b - Bottom 1/2 Array 010b - Bottom 1/4 Array 011b - Bottom 1/8 Array 100b - Reserved 101b - Top 1/2 Array 110b - Top 1/4 Array 111b - Top 1/8 Array
[1:0]*[1]	Distributed Refresh Interval	00b - Reserved 01b - 4μS (t_{CSM}) 10b - 1μS (t_{CSM}) 11b - Reserved

Note:
1. CR1[1:0] is read only.

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9.5.1 CR1[5] Hybrid Sleep

When the HyperRAM device is not needed for system operation, it may be placed in Hybrid Sleep state if data in the device needs to be retained. Enter Hybrid Sleep state by writing 1 to CR1[5]. Bringing CS# Low will cause the HyperRAM device to exit HS state and set CR1[5] to 0. Also, POR, or a hardware reset will cause the device to exit Hybrid Sleep state. Note that a POR or a hardware reset disables refresh where the data stored in memory array would be potentially lost.

9.5.2 CR1[4:2] Partial Array Refresh

The partial array refresh configuration restricts the refresh operation in HyperRAM device to a portion of the memory array specified by CR1[4:2]. This reduces the standby current. The default configuration refreshes the whole array.

9.5.3 CR1[7] Set Refresh Rate

When the device set to Fast Refresh Rate by set the value of CR1[7] to “1”, the t_{CSM} =1μS will be request that equal to the high temperature maximum distributed refresh interval. The host system is required to respect the t_{CSM} value by ending each transaction before violating t_{CSM} and will no need to monitor the state of CR1[1:0].

9.5.4 CR1[1:0] Distributed Refresh Interval

The HyperRAM device is built with volatile memory array which requires periodic refresh of all bits in the array. The refresh operation can be done by an internal self-refresh logic that will evenly refresh the memory array automatically.

The automatic refresh operation can only be done when the memory array is not being actively read or written by the host system. The refresh logic waits for the end of any active read or write before doing a refresh, if a refresh is needed at that time. If a new read or write begins before the refresh is completed, the memory will drive RWDS high during the CA period to indicate that an additional initial latency time is required at the start of the new access in order to allow the refresh operation to complete before starting the new access.

The evenly distributed refresh operations require a maximum refresh interval between two adjacent refresh operations. The maximum distributed refresh interval will vary with temperature as shown in Table 11 - Distributed Refresh Interval per Temperature.

Table 11 - Distributed Refresh Interval per Temperature

Device Temperature (T_{CASE} ˚C)	Maximum Distributed Refresh Interval (μs)	CR1[1:0]
T_{CASE} < 85	4	01b

The distributed refresh operation requires that the host does not do burst transactions longer than the distributed refresh interval to prevent the memory from unable doing the distributed refreshes operation when it is needed.

This sets an upper limit on the length of read and write transactions so that the automatic distributed refresh operation can be done between transactions. This limit is called the CS# low maximum time (t_{CSM}) and the t_{CSM} will be equal to the maximum distributed refresh interval.

The host system is required to respect the t_{CSM} value by ending each transaction before violating t_{CSM}. This can be done by host memory controller logic splitting long transactions when reaching the t_{CSM} limit, or by host system hardware or software not performing a single read or write transaction that would be longer than t_{CSM}.

As noted in Table of distributed refresh interval, the maximum refresh interval is longer at lower temperatures such that t_{CSM} could be increased to allow longer transactions. The host system can either use the CR1[1:0] value for determining the maximum operating temperature or, may determine the current operating temperature from a temperature sensor in the system in order to set a longer distributed refresh interval.

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10. INTERFACE STATES

10.1 IO condition of interface states

Below Interface States table describes the required value of each signal for each interface state.

Table 12 - Interface States

Interface State	Vcc	CS#	CK	DQ7-DQ0	RWDS	RESET#
Power-Off	< V_{LKO}	X	X	High-Z	High-Z	X
Power-On (Cold) Reset	≥ Vcc min	X	X	High-Z	High-Z	X
Hardware (Warm) Reset	≥ Vcc min	X	X	High-Z	High-Z	L
Interface Standby	≥ Vcc min	H	X	High-Z	High-Z	H
CA	≥ Vcc min	L	T	Master Output Valid	X	H
Read Initial Access Latency (data bus turn around period)	≥ Vcc min	L	T	High-Z	L	H
Write Initial Access Latency (RWDS turn around period)	≥ Vcc min	L	T	High-Z	High-Z	H
Read data transfer	≥ Vcc min	L	T	Slave Output Valid	Slave Output Valid X or T	H
Write data transfer with Initial Latency	≥ Vcc min	L	T	Master Output Valid	Master Output Valid X or T	H
Write data transfer without Initial Latency	≥ Vcc min	L	T	Master Output Valid	Slave Output L or High-Z	H
Active Clock Stop	≥ Vcc min	L	Idle	Master or Slave Output Valid or High-Z	X	H
Deep Power Down	≥ Vcc min	H	X or T	High-Z	High-Z	H
Hybrid Sleep	≥ Vcc min	H	X or T	High-Z	High-Z	H
Software Reset	≥ Vcc min	H	X or T	High-Z	High-Z	H

Legend

L = $V_{IL(DC)}$

H = $V_{IH(DC)}$

X = Either $V_{IL(DC)}$, $V_{IH(DC)}$, V_{OL} or V_{OH}

L/H = Rising edge

H/L = Falling edge

T = Toggling during information transfer

Idle = CK is Low

Valid = All bus signals have stable L or H level

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10.2 Power Conservation Modes

10.2.1 Interface Standby

Standby is the default, low power, state for the interface while the device is not selected by the host for data transfer by keeping CS#= High. The HyperRAM device will stay at interface standby state when CS# = High, CK = 0 or 1, and RESET# = High. When the HyperRAM device staying at interface standby state, it will not drive the DQs pad and RWDS pad and only monitor the status of CS# and RESET# input pads.

10.2.2 Active Clock Stop

The Active Clock Stop state reduces device interface energy consumption to the I_{CC6} level during the data transfer portion of a read or write operation. The device automatically enables this state when clock remains stable for t_{ACC} + 30 nS. While in Active Clock Stop state, read data is latched and always driven onto the data bus. Active Clock Stop state helps reduce current consumption when the host system clock has stopped to pause the data transfer. Even though CS# may be Low throughout these extended data transfer cycles, the memory device host interface will go into the Active Clock Stop current level at t_{ACC} + 30 nS. This allows the device to transition into a lower current state if the data transfer is stalled. Active read or write current will resume once the data transfer is restarted with a toggling clock. The Active Clock Stop state must not be used in violation of the t_{CSM} limit. CS# must go High before t_{CSM} is violated.

Note that it is recommended not to stop the clock during register access.

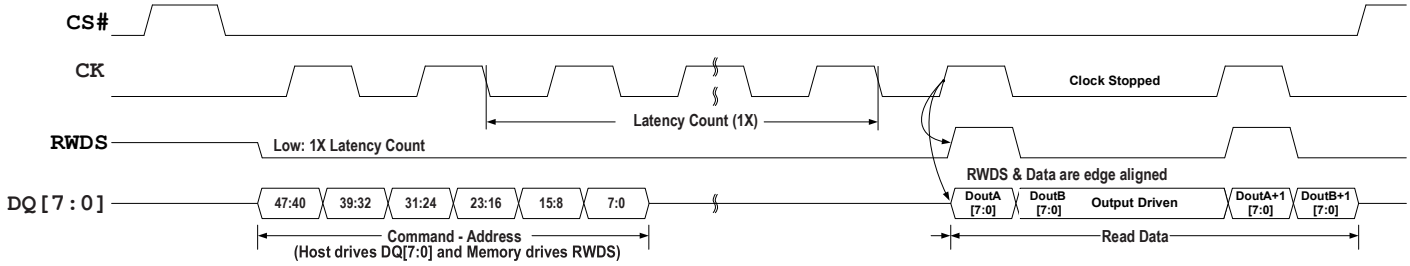


Figure 14 - Active Clock Stop during Read Transaction

10.2.3 Hybrid Sleep

In the Hybrid Sleep (HS) state, the current consumption is reduced (I_{HS}). HS state is entered by writing a 1 to CR1[5]. The device reduces power within t_{HSIN} time. The data in Memory Space and Register Space is retained during HS state. Bringing CS# Low will cause the device to exit HS state and set CR1[5] to 0. Also, POR, or a hardware reset will cause the device to exit HS state. The HyperRAM device returning to Standby state from HS state requires t_{EXTHS} time. Following the exit from HS due to any of these events, the device is in the same state as entering HS. Prior to the t_{EXTHS} expired, the CS# is not allowed to go LOW for the next valid command input.

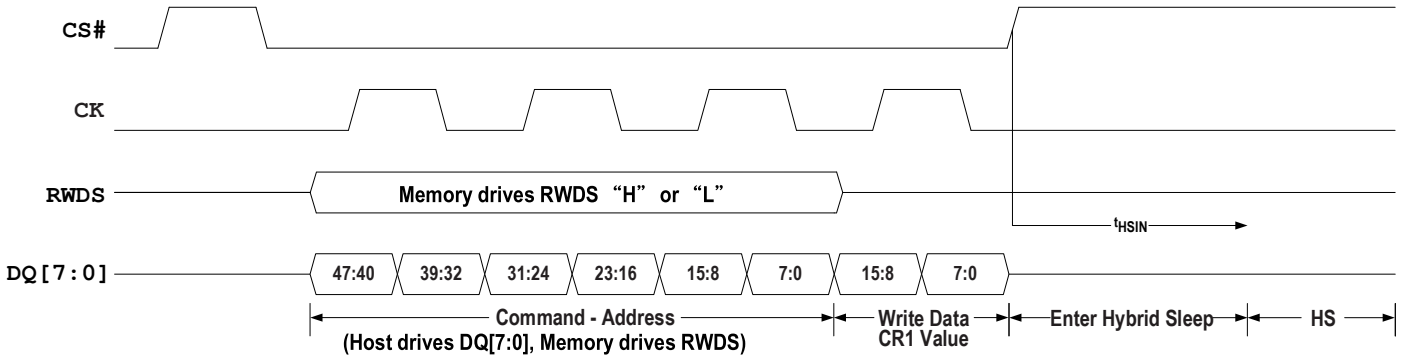


Figure 15 - Enter Hybrid Sleep Transaction

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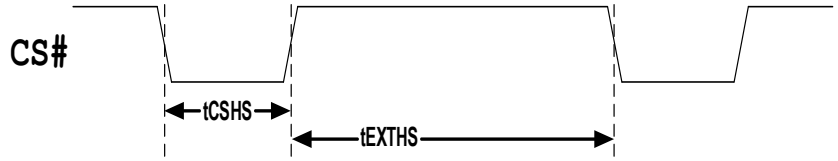


Figure 16 - Exit Hybrid Sleep Transaction

10.2.4 Deep Power Down

In the Deep Power Down (DPD) state, current consumption is driven to the lowest possible level (I_{DPD}). DPD state is entered by writing a 0 to CR0[15]. The device reduces power within t_{DPDIN} time and all refresh operations stop. The data in memory array would be lost, (becomes invalid without refresh) during DPD state. Driving CS# Low then High will cause the device to exit DPD state. Also, POR, or a hardware reset will cause the device to exit DPD state. The HyperRAM device returning to Standby state by driving CS# Low then High requires t_{EXTDPD} time. The HyperRAM device returning to Standby state following a POR requires t_{VCS} time, as with any other POR.

Following the exit from DPD due to any of these events, the device is in the same state as following POR.

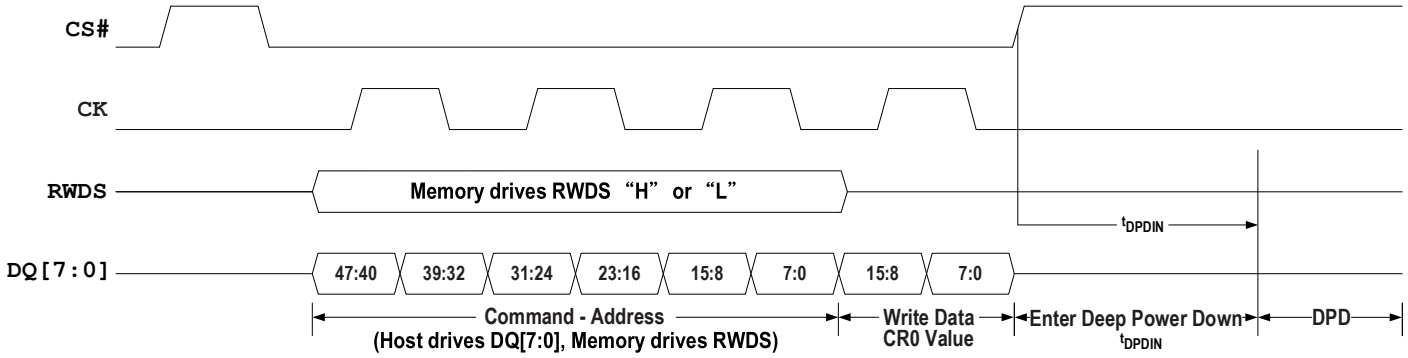


Figure 17 - Enter DPD Transaction

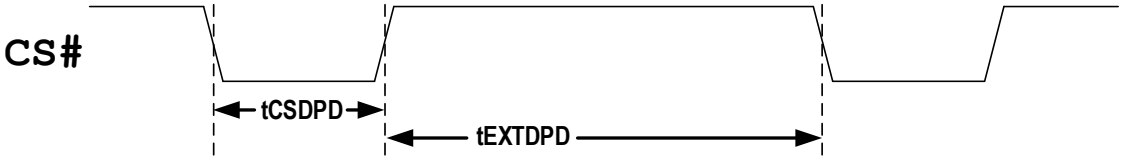


Figure 18 - Exit DPD Transaction

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11. ELECTRICAL SPECIFICATIONS

11.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Voltage on VCC supply relative to VSS	-0.5	VCC +0.5	V	1
Soldering temperature and time 10s (solder ball only)	+260		°C	1
Storage temperature (plastic)	-65	+150	°C	1
Output Short Circuit Current		100	mA	1, 2

Notes:

1. Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect devicereliability.
2. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

11.2 Latch up Characteristics

Table 13 - Latch up Specification

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	-1.0	V_{CC} + 1.0	V
Input voltage with respect to V_{SS} on all I/O connections	-1.0	V_{CC} + 1.0	V
VCC Current	-100	+100	mA

Note:

1. Excludes power supplies VCC. Test conditions: VCC = 1.8V or 1.5V or 1.35V or 1.2V, one connection at a time tested, connections not being tested are at VSS.

11.3 Operating Ranges

11.3.1 Electrical Characteristics and DC/AC Operating Conditions

Parameter	Description	Test Conditions	Min	Max	Unit
VCC	Power Supply (typical 1.8V)		1.7	2.0	V
VCC	Power Supply (typical 1.5V)		1.425	1.575	V
VCC	Power Supply (typical 1.35V)		1.3	1.45	V
VCC	Power Supply (typical 1.2V)		1.16	1.3	V
VIH(DC)	DC Input High Voltage		0.7 x VCC	1.15 x VCC	V
VIL(DC)	DC Input Low Voltage		-0.15 x VCC	0.3 x VCC	V
VIH(AC)	AC Input High Voltage		0.8 x VCC	1.15 x VCC	V
VIL(AC)	AC Input Low Voltage		-0.15 x VCC	0.2 x VCC	V
VOH	Output High Voltage	IOH = 100 µA	VCC - 0.2	–	V
VOL	Output Low Voltage	IOL = 100 µA	–	0.2	V

Note:

1. All parts list in order information table (section 2) will not guarantee to meet functional and AC specification if the VCC operation condition out of range mentioned in above table.

11.3.2 Operating Temperature

Parameter	Symbol	Range	Unit	Notes
Operating Temperature	TCASE	-40~85	°C	1

Note:

1. All parts list in order information table (section 2) will not guarantee to meet functional and AC specification if the operation temperature range out of range mentioned in above table.

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11.3.3 ICC Characteristics

Parameter	Description	Test Conditions	Min	Typ*1	Max	Unit
I_{LI2}	Input Leakage Current (85°C) Reset Signal High Only	V_{IN} = Vss to Vcc; Vcc = Vcc max	–	–	2	µA
I_{LI4}	Input Leakage Current (85°C) Reset Signal Low Only*2	V_{IN} = Vss to Vcc; Vcc = Vcc max	–	–	15	µA
I_{CC1}	Vcc Active Read Current*3 (85°C)	CS# = Vss, @250 MHz; Vcc = Vcc max	–	9.5	9.7	mA
		CS# = Vss, @200 MHz; Vcc = Vcc max	–	8.6	8.8	mA
I_{CC2}	Vcc Active Write Current (85°C)	CS# = Vss, @250 MHz; Vcc = Vcc max	–	9.4	9.8	mA
		CS# = Vss, @200 MHz; Vcc = Vcc max	–	7.9	8.2	mA
I_{CC5}	Reset Current (85°C)	CS# = Vcc, RESET# = Vss; Vcc = Vcc max	–	0.06	0.09	mA
I_{CC6}	Active Clock Stop Current (85°C)	CS# = Vss, RESET# = Vcc; Vcc = Vcc max	–	3.2	3.5	mA
I_{CC7}	Vcc Current during power up*1 (85°C)	CS# = Vcc; Vcc = Vcc max	–	–	35	mA
I_{DPD}	Deep Power Down Current (85°C)	CS# = Vcc; Vcc = Vcc max	–	0.5	2	µA
I_{CC8}	Software Reset Current (85°C)	CS# = Vcc; Vcc = Vcc max	–	0.04	0.22	mA

Parameter	Description	Test Conditions		Min	Typ*1	Max	Unit
I_{CC4}	V_{CC} Standby Current (85°C)	CS# = Vcc; Vcc = Vcc max	Full Array	–	56	155	µA
			Bottom 1/2 Array	–	52	121	
			Bottom 1/4 Array	–	50	105	
			Bottom 1/8 Array	–	50	95	
			Top 1/2 Array	–	52	121	
			Top 1/4 Array	–	50	105	
			Top 1/8 Array	–	50	95	
I_{HS}	Hybrid Sleep Current (85°C)	CS# = Vcc; Vcc = Vcc max	Full Array	–	20	111	µA
			Bottom 1/2 Array	–	19	95	
			Bottom 1/4 Array	–	18	86	
			Bottom 1/8 Array	–	17	82	
			Top 1/2 Array	–	19	95	
			Top 1/4 Array	–	18	86	
			Top 1/8 Array	–	17	82	

Notes:
1. Typical values is the median average value measured @ T_{CASE} =25°C and not tested in mass production process.
2. RESET# Low initiates exits from DPD state and initiates the draw of I_{CC5} reset current, making I_{LI} during Reset# Low insignificant.
3. I_{CC1} is measured under a condition with data output buffer is disabled.

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11.3.4 Power-Up Initialization

The HyperRAM device include an on-chip voltage sensor used to launch the power-up initialization process. When the power supply reaches a stable level at or above V_{CC} (min), the device will require t_{VCS} time to complete its self-initialization process.

The device must not be selected during power-up. CS# must follow the voltage applied on V_{CC} until V_{CC} (min) is reached during power-up, and then CS# must remain high for a further delay of t_{VCS}. A simple pull-up resistor from V_{CC} to Chip Select (CS#) can be used to insure safe and proper power-up.

If RESET# is Low during power up, the device delays start of the t_{VCS} period until RESET# is High. The t_{VCS} period is used primarily to perform refresh operations on the DRAM array to initialize it.

When initialization is complete, the device is ready for normal operation.

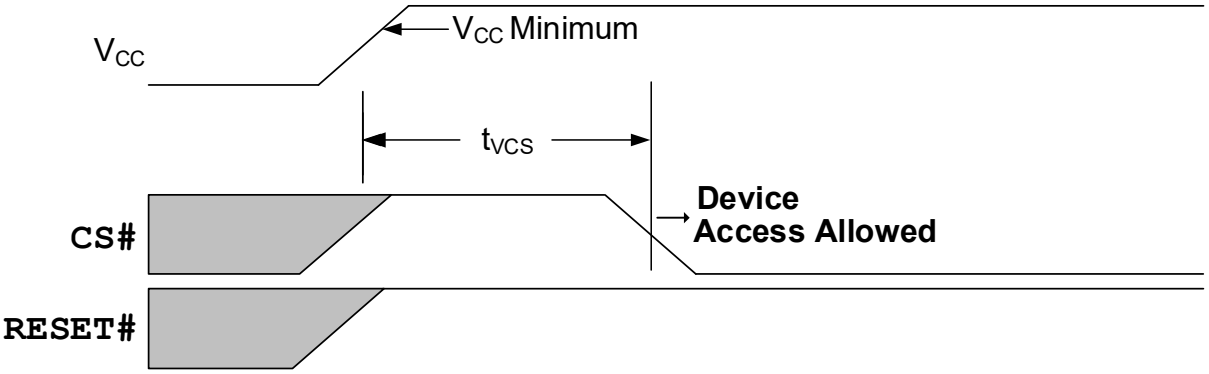


Figure 19 - Power-up with RESET# High

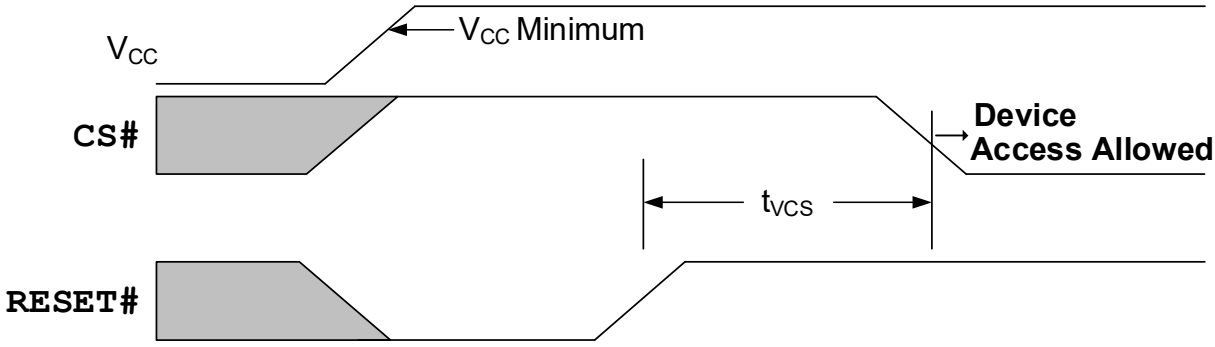


Figure 20 - Power-up with RESET# Low

Table 14 - Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
VCC	VCC Power Supply (typical 1.8V)	1.7	2.0	V
VCC	VCC Power Supply (typical 1.5V)	1.425	1.575	V
VCC	VCC Power Supply (typical 1.35V)	1.3	1.45	V
VCC	VCC Power Supply (typical 1.2V)	1.16	1.3	V
t_{VCS}	VCC ≥ minimum and RESET# High to first access	–	150	µS

Notes:

1. Bus transactions (read and write) are not allowed during the power-up reset time (t_{VCS}).
2. VCC ramp rate may be non-linear.

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11.3.5 Power-Down

The HyperRAM devices are considered to be powered-off when the array power supply (VCC) drops below the VCC Lock-Out voltage (VLKO). At the VLKO level, the HyperRAM device will have lost configuration or array data. However, if during a voltage drop the VCC stays above VLKO the part will stay initialized and will work correctly when VCC is again above VCC minimum.

During Power-Down or voltage drops below VLKO, the array power supply voltages must also drop below VCC Reset (VRST) for a Power Down period (t_{PD}) for the part to initialize correctly when the power supply again rises to VCC minimum. See Figure 21 - Power Down or Voltage Drop.

If during a voltage drop the VCC stays above VLKO the part will stay initialized and will work correctly when VCC is again above VCC minimum. If VCC does not go below and remain below VRST for greater than t_{PD}, then there is no assurance that the POR process will be performed. In this case, a hardware reset will be required ensure the HyperRAM device is properly initialized.

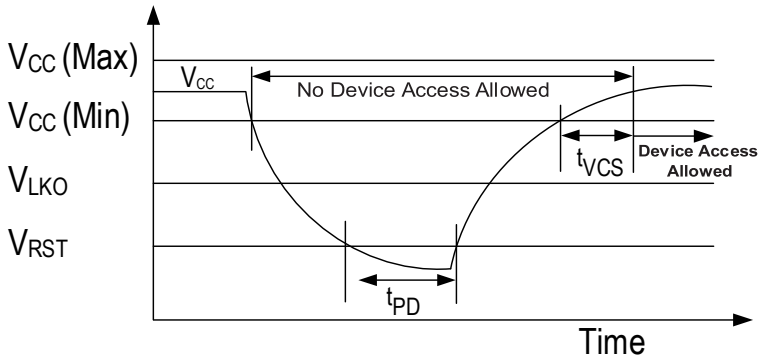


Figure 21 - Power Down or Voltage Drop

The following section describes HyperRAM device dependent aspects of power down specifications.

Table 15 - Power-Down Voltage and Timing

Parameter	Description	Min	Max	Unit
VCC	VCC Power Supply (typical 1.8V)	1.7	2.0	V
VCC	VCC Power Supply (typical 1.5V)	1.425	1.575	V
VCC	VCC Power Supply (typical 1.35V)	1.3	1.45	V
VCC	VCC Power Supply (typical 1.2V)	1.16	1.3	V
VLKO	VCC Lock-out below which re-initialization is required	1.13	–	V
VRST	VCC Low Voltage needed to ensure initialization will occur	0.5	–	V
t_{PD}	Duration of VCC ≤ VRST	50	–	µS

Note: VCC ramp rate can be non-linear.

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11.3.6 Hardware Reset

The RESET# input provides a hardware method of returning the device to the standby state.

During t_{RPH} the device will draw I_{CC5} current. If RESET# continues to be held Low beyond t_{RPH}, the device draws CMOS standby current (I_{CC4}). While RESET# is Low (during t_{RP}), and during t_{RPH}, bus transactions are not allowed.

A Hardware Reset will:

- Cause the configuration registers to return to their default values
- Halt self-refresh operation while RESET# is low - memory array data is considered as invalid
- Force the device to exit the Hybrid Sleep state
- Force the device to exit the Deep Power Down state

After RESET# returns High, the self-refresh operation will resume. Because self-refresh operation is stopped during RESET# Low, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh interval per Table 11 - Distributed Refresh Interval per Temperature on page 25. This may result in the loss of DRAM array data during or immediately following a hardware reset. The host system should assume memory array data is lost after a hardware reset and reload any required data.

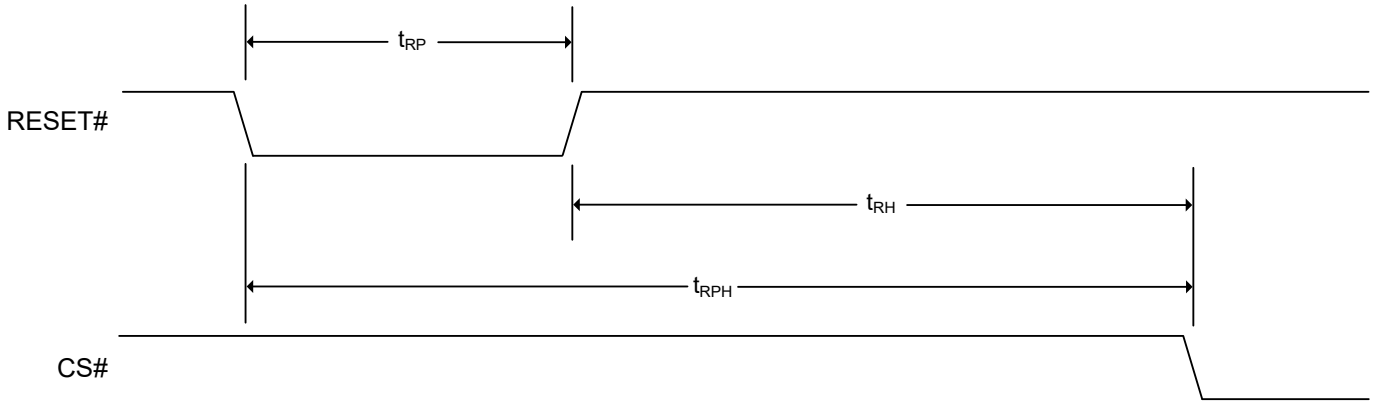


Figure 22 - Hardware Reset Timing Diagram

Table 16 - Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
t_{RP}	RESET# Pulse Width	200	–	nS
t_{RH}	Time between RESET# (High) and CS# (Low)	200	–	nS
t_{RPH}	RESET# Low to CS# Low	400	–	nS

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11.3.7 Software Reset

The Software Reset provides a software method of returning the device to the standby state.

During tRPH the device will draw ICC8 current. While Software Reset time (tRPH), bus transactions are not allowed.

A Software Reset will:

- Cause the configuration registers to return to their default values
- Halt self-refresh operation while Software Reset time - memory array data is considered as invalid

After Software Reset exit, the self-refresh operation will resume. Because self-refresh operation is stopped during Software Reset time, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh interval per Table 11 - Distributed Refresh Interval per Temperature on page 25. This may result in the loss of DRAM array data during or immediately following a Software reset. The host system should assume memory array data is lost after Software Reset and reload any required data.

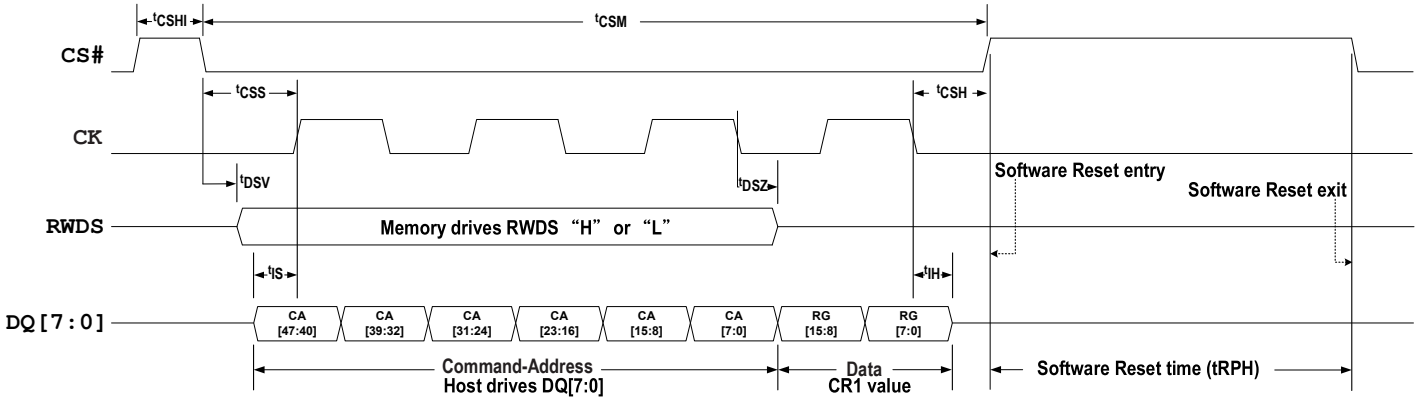


Figure 23 - Software Reset Timing Diagram

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11.4 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between VSS and VCC.

During voltage transitions, inputs or I/Os may negative overshoot VSS to -1.0V or positive overshoot to VCC +1.0V, for periods up to 20 nS.

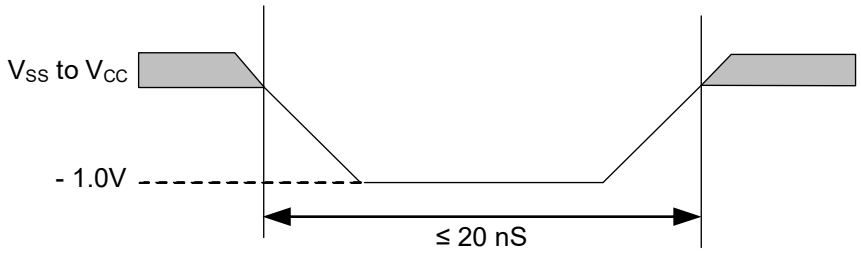


Figure 24 - Maximum Negative Overshoot Waveform

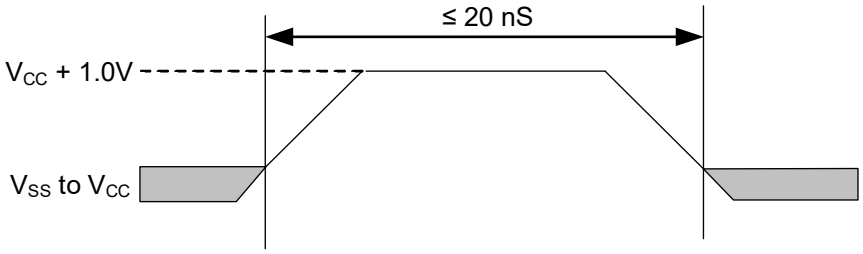


Figure 25 - Maximum Positive Overshoot Waveform

11.5 Capacitance Characteristics

Parameter	Description	Min	Max	Unit
CI	Input capacitance (CK, CS#)		3.0	pF
CIO	Input/output capacitance (DQx, RWDS)		3.5	pF
CIOD	Input/output capacitance delta (DQx)		0.8	pF

Note: The capacitance is applied to the ball of package. The capacitance values are guaranteed by design.

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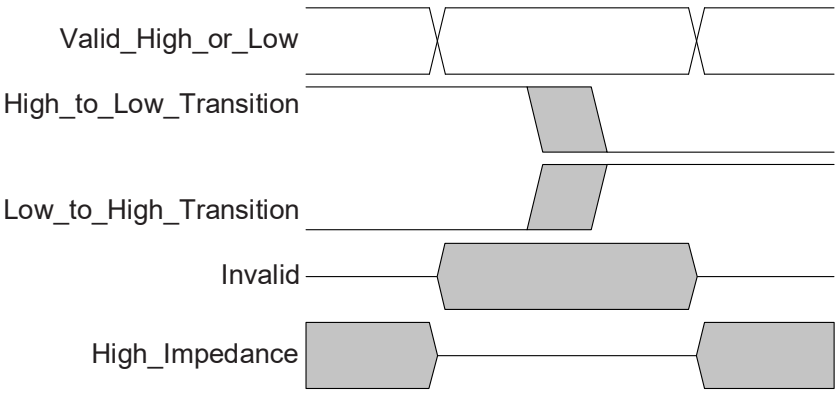
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12. TIMING SPECIFICATIONS

The following section describes HyperRAM device dependent aspects of timing specifications.

12.1 Key to Switching Waveforms



12.2 AC Test Conditions

12.2.1 HyperRAM Driver Output Timing Reference Load

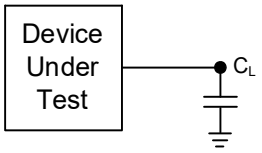


Figure 26 - Test Setup

Table 17 - Test Specification

Description	All	Unit	Notes
Output Load Capacitance, C_L	5	pF	
Minimum Input Rise and Fall Slew Rates	1.13	V/nS	1
Input Pulse Levels	0-V_{CC}	V	
Input / Output timing measurement reference levels	V_{CC}/2	V	2

Notes:

1. All AC timings assume this input slew rate.
2. Input and output timing is referenced to V_{CC}/2 for single ended clock.

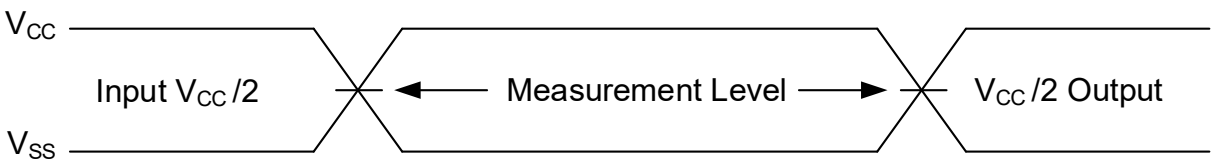


Figure 27 - Input Waveforms and Measurement Levels

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12.3 AC Characteristics

12.3.1 Read Transactions

Table 18 - HyperRAM Specific Read Timing Parameters

Description	Parameter	250 MHz		200 MHz		166 MHz		133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Chip Select High Between Transactions	t_{CSHI}	6	–	6	–	6	–	7.5	–	nS	
HyperRAM Read-Write Recovery Time	t_{RWR}	35	–	35	–	36	–	37.5	–	nS	
Chip Select Setup to next CK Rising Edge	t_{CSS}	5	–	5	–	5	–	5	–	nS	
Data Strobe Valid	t_{DSV}	–	5	–	5	–	12	–	12	nS	
Input Setup Time	t_{IS}	0.46	–	0.5	–	0.6	–	0.8	–	nS	
Input Hold Time	t_{IH}	0.46	–	0.5	–	0.6	–	0.8	–	nS	
HyperRAM Read Initial Access Time	t_{ACC}	40	–	35	–	36	–	37.5	–	nS	
Clock to DQs Low Z	t_{DQLZ}	0	–	0	–	0	–	0	–	nS	
CK transition to DQ Valid	t_{CKD}	1	5.3	1	5.3	1	5.5	1	5.5	nS	
CK transition to DQ Invalid	t_{CKDI}	0	4.2	0	4.2	0	4.6	0	4.5	nS	
Data Valid (t_{DV} min = t_{CKHP} min - t_{CKD} max + t_{CKDI} max)	t_{DV}	0.7	–	1.15	–	1.8	–	2.375	–	nS	
CK transition to RWDS Low @CA phase @Read	t_{CKDSR}	1	5.5	1	5.5	1	5.5	1	5.5	nS	
CK transition to RWDS Valid	t_{CKDS}	1	5.3	1	5.3	1	5.5	1	5.5	nS	
RWDS transition to DQ Valid	t_{DSS}	-0.4	+0.4	-0.4	+0.4	-0.45	+0.45	-0.6	+0.6	nS	
RWDS transition to DQ Invalid	t_{DSH}	-0.4	+0.4	-0.4	+0.4	-0.45	+0.45	-0.6	+0.6	nS	
Chip Select Hold After CK Falling Edge	t_{CSH}	0	–	0	–	0	–	0	–	nS	2, 3
Chip Select Inactive to RWDS High-Z	t_{DSZ}	–	5	–	5	–	6	–	6	nS	
Chip Select Inactive to DQ High-Z	t_{OZ}	–	5	–	5	–	6	–	6	nS	
HyperRAM Chip Select Maximum Low Time (TCASE < 85°C)	t_{CSM}	–	4	–	4	–	4	–	4	µS	
Row Boundary Crossing Wait Time	$t_{RBXwait}$	–	65	–	65	–	65	–	65	nS	1

Notes:

1. When crossing row boundary, the host must wait for at least 65nS for doing data read from next row.
2. The last falling edge of CK input can be recognized when t_{CSH}=0.
3. The read data will become High-Z after t_{OZ} when CS#=H.

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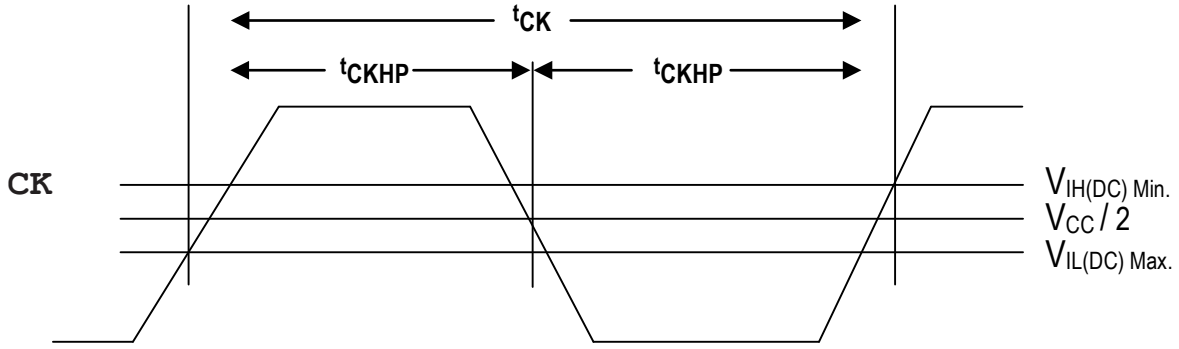


Figure 28 - Clock Characteristics

Table 19 - Clock Timings

Description	Parameter	250 MHz		200 MHz		166 MHz		133 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
CK Period	t_{CK}	4	100	5	100	6	100	7.5	100	nS
CK Half Period - Duty Cycle	t_{CKHP}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
CK Half Period at Frequency Min = 0.45 t_{CK} Min Max = 0.55 t_{CK} Min	t_{CKHP}	1.8	2.2	2.25	2.75	2.7	3.3	3.375	4.125	nS

Note: All parts list in order information table (section 2) will not guarantee to meet functional and AC specification if the t_{CK} and t_{CKHP} out of range mentioned in above table.

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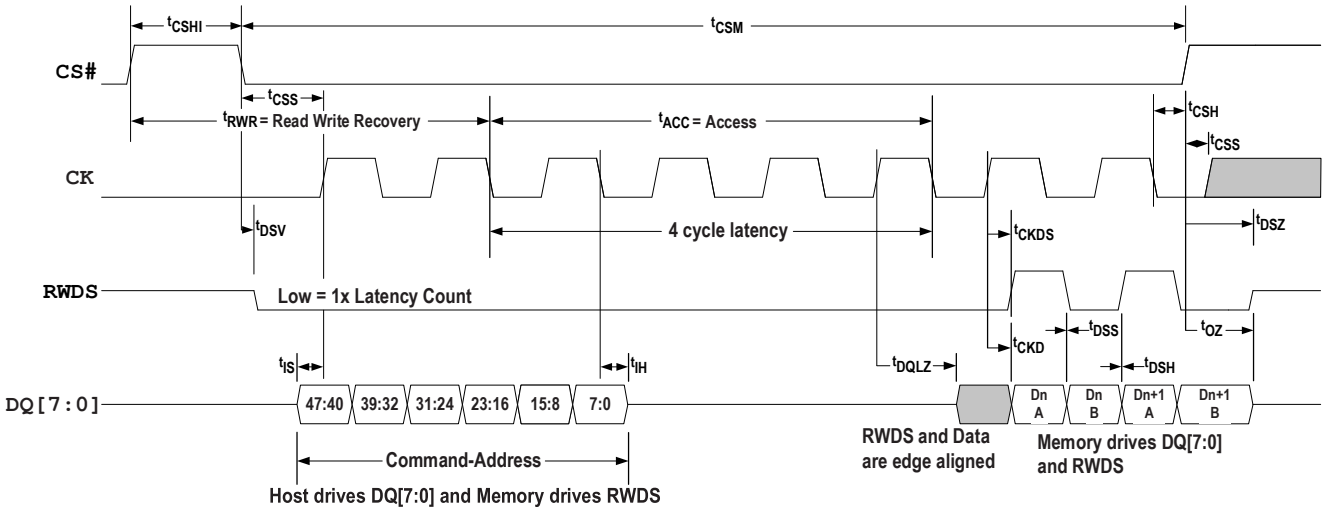


Figure 29 - Read Timing Diagram — No Additional Latency Required

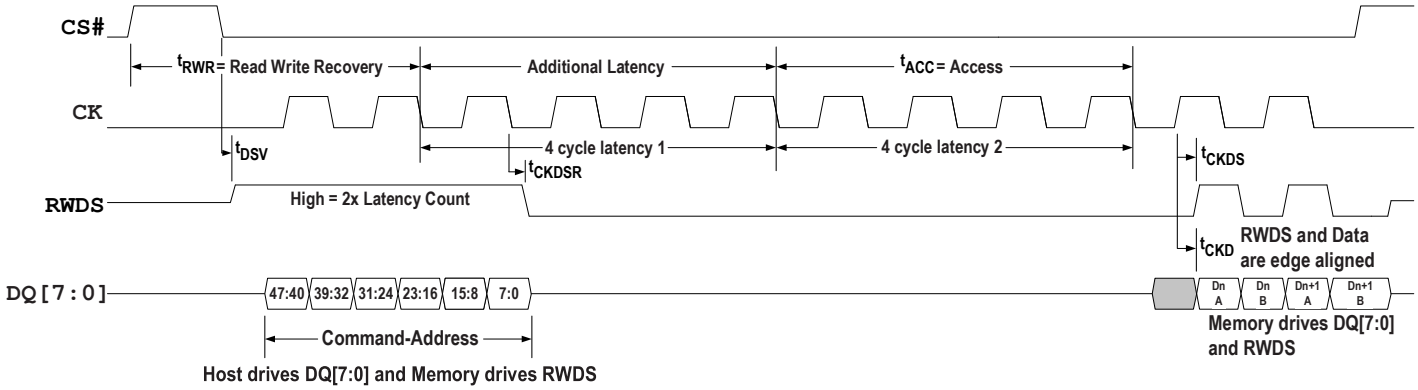


Figure 30 - Read Timing Diagram — With Additional Latency

Notes:

1. Transactions are initiated with CS# falling while CK=Low.
2. CS# must return High before a new transaction is initiated.
3. The memory drives RWDS during the entire Read transaction.
4. Transactions without additional latency count have RWDS Low during CA cycles. Transactions with additional latency count have RWDS High during CA cycles and RWDS returns low at t_{CKDSR}. All other timing relationships are the same for both figures although they are not shown in the second figure. A four cycles latency is used for illustration purposes only. The required latency count is device and clock frequency dependent.

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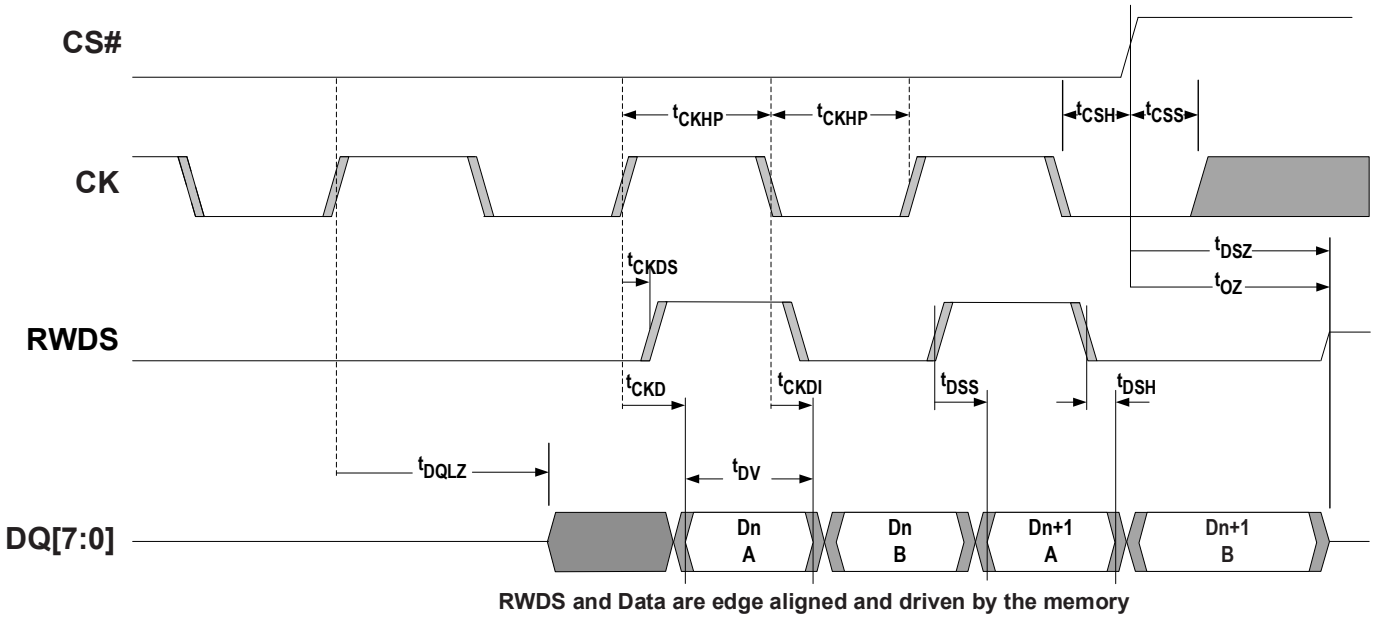


Figure 31 - Data Valid Timing

Notes:

1. This figure shows a closer view of the data transfer portion of read transaction diagrams to more clearly show the Data Valid period as affected by clock duty and clock to output delay uncertainty.
2. The t_{CKD} and t_{CKDI} timing parameters define the beginning and end position of the data valid period.
3. The t_{DSS} and t_{DSH} timing parameters define how early or late RWDS may transition relative to the transition of data. This is the potential skew between the clock to data delay t_{CKD}, and clock to data strobe delay t_{CKDS}. Aside from this skew, the t_{CKD}, t_{CKDI}, and t_{CKDS} values track together (vary by the same ratio) because RWDS and Data are outputs from the same device under the same voltage and temperature conditions.

12.3.2 Write Transactions

Table 20 - Write Timing Parameters

Description	Parameter	250 MHz		200 MHz		166 MHz		133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
HyperRAM Read-Write Recovery Time	t_{RWR}	35	–	35	–	36	–	37.5	–	nS	
HyperRAM Read Initial Access Time	t_{ACC}	40	–	35	–	36	–	37.5	–	nS	
HyperRAM Chip Select Maximum Low Time (TCASE < 85°C)	t_{CSM}	–	4	–	4	–	4	–	4	µS	
RWDS Data Mask Valid	t_{DMV}	0	–	0	–	0	–	0	–	nS	
Chip Select Hold After CK Falling Edge	t_{CSH}	0	–	0	–	0	–	0	–	nS	1

Note:

1. The last falling edge of CK input can be recognized when t_{CSH}=0.

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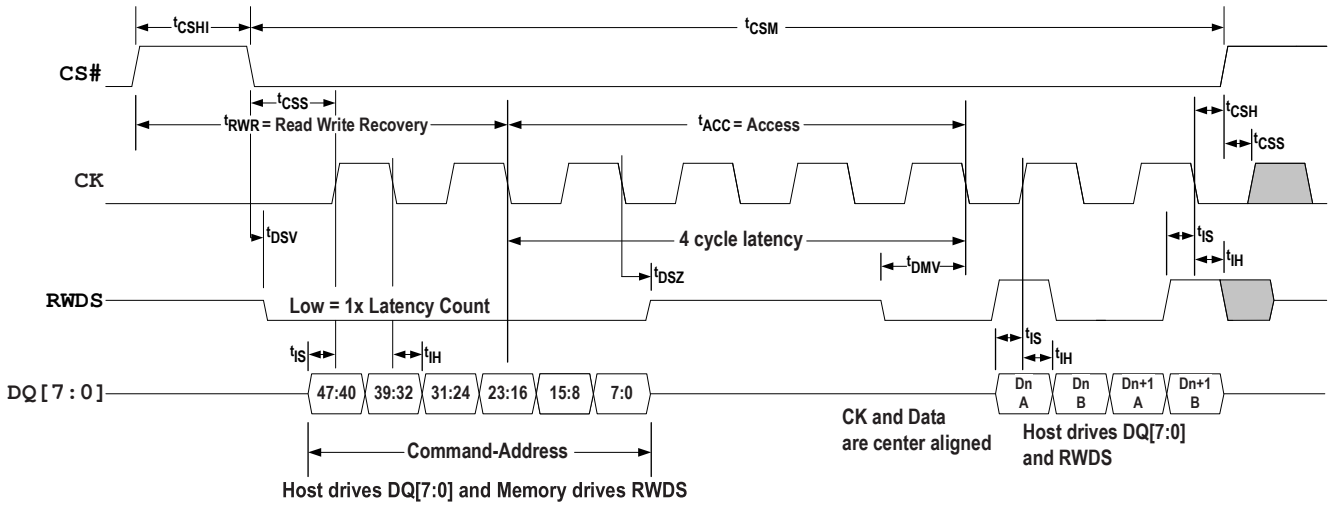


Figure 32 - Write Timing Diagram — No Additional Latency

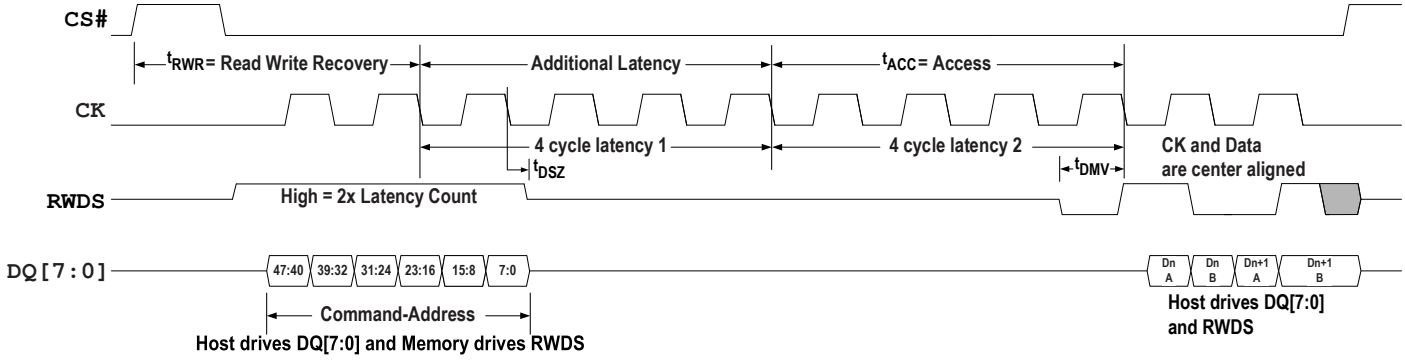


Figure 33 - Write Timing Diagram — With Additional Latency

Notes:

1. Transactions are initiated with CS# falling while CK=Low. CS# must return High before a new transaction is initiated.
2. During write transactions with latency, RWDS is used as an additional latency indicator initially and is then used as a data mask during data transfer.
3. Transactions without additional latency count have RWDS Low during CA cycles and RWDS returns Hi-Z at t_{DSZ}. Transactions with additional latency count have RWDS High during CA cycles and RWDS returns Hi-Z at t_{DSZ}. All other timing relationships are the same for both figures although they are not shown in the second figure. A four cycles latency is used for illustration purposes only. The required latency count is device and clock frequency dependent.
4. At the end of Command-Address cycles the memory stops driving RWDS to allow the host HyperRAM master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave. This can be done during the last cycle of the initial latency.
5. The write transaction shown demonstrates the Dn A byte and the Dn+1 B byte being masked. Only Dn B byte and Dn+1 A byte are wrote into memory the array. Dn A byte and Dn+1 B byte are not wrote into memory array.

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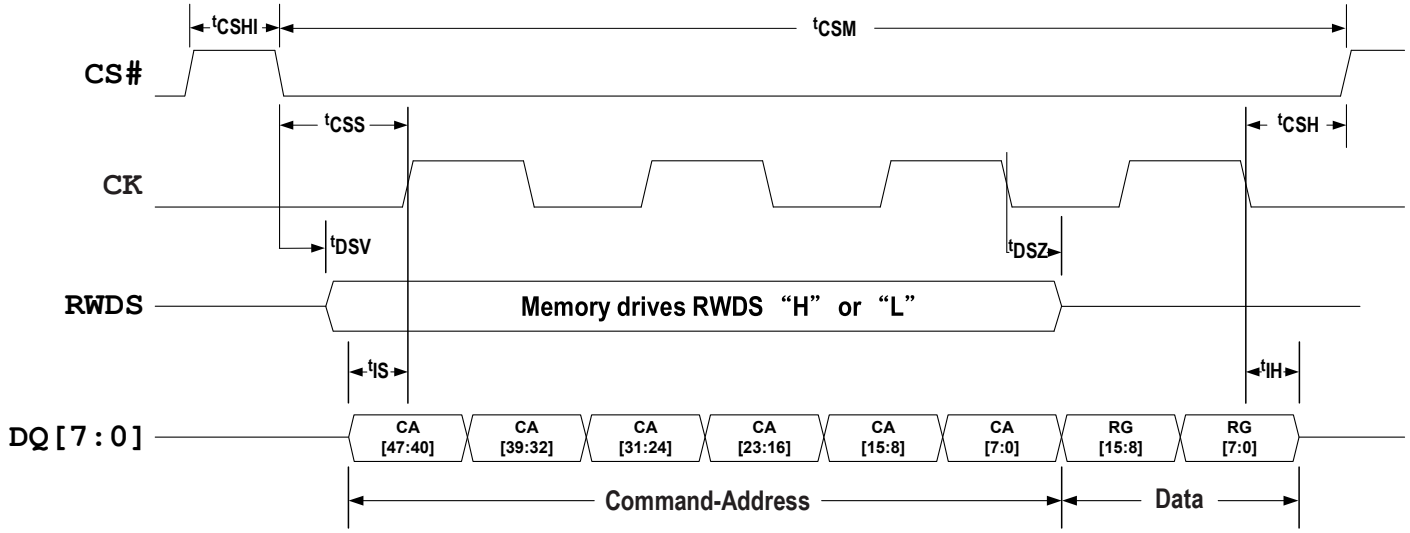


Figure 34 - Write Operation without Initial Latency (Register Write)

Notes:

1. Transactions are initiated with CS# falling while CK=Low. CS# must return High before a new transaction is initiated.
2. Writes with zero initial latency, do not have a turnaround period for RWDS. The slave device will always drive RWDS during the Command-Address period to indicate whether extended latency is required for a transaction that has initial latency. However, the RWDS is driven before the slave device has received the first byte of CA, that is, before the slave knows whether the transaction is a read or write, to memory space or register space. In the case of a write with zero latency, the RWDS state during the CA period does not affect the initial latency of zero. Since master write data immediately follows the Command-Address period in this case, the slave may continue to drive RWDS Low or may take RWDS to High-Z during write data transfer. The master must not drive RWDS during Writes with zero latency. Writes with zero latency do not use RWDS as a data mask function. All bytes of write data are written (full word writes).

12.3.3 Hybrid Sleep Timings

Table 21 - Hybrid Sleep Timing Parameters

Description	Parameter	Min	Max	Unit	Note
Hybrid Sleep CR1[5]=1 register write to HS power level	t_{HSIN}	–	3	µS	
CS# Pulse Width to Exit Hybrid Sleep	t_{CSHS}	60	3000	nS	
CS# Exit Hybrid Sleep to Standby wakeup time	t_{EXTHS}	–	100	µS	1

Note:

1. After exit Hybrid Sleep command effective. the host must wait for at least 100µS to do the next valid command to the HyperRAM device.

12.3.4 Deep Power down Timings

Table 22 - Deep Power Down Timing Parameters

Description	Parameter	Min	Max	Unit	Note
Deep Power Down CR0[15]=0 register write to DPD power level	t_{DPDIN}	–	3	µS	
CS# Pulse Width to Exit DPD	t_{CSDPD}	200	3000	nS	
CS# Exit Deep Power Down to Standby wakeup time	t_{EXTDPD}	–	150	µS	1

Note:

1. After exit DPD command effective. the host must wait for at least 150µS to do the next valid command to the HyperRAM device.

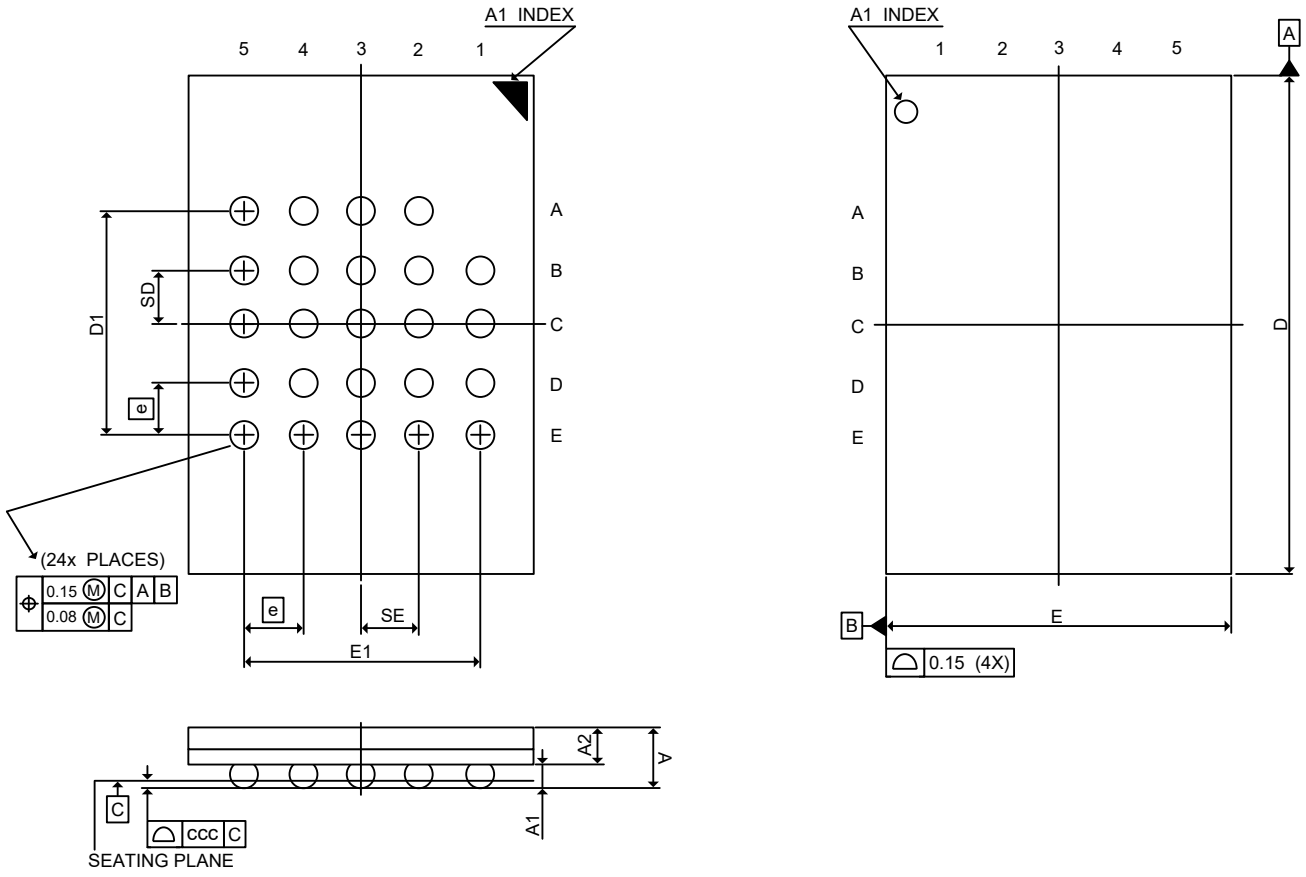
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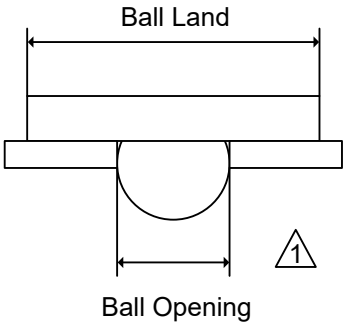
13. PACKAGE SPECIFICATION

Package Outline TFBGA24 Ball (6x8 mm² (5x5-1 ball arrays), Ball pitch: 1.00mm, Ø=0.40mm)



Controlling Dimensions are in milmeters

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	0.047
A1	0.26	0.31	0.36	0.010	0.012	0.014
A2	---	0.85	---	---	0.033	---
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	4.00 BSC			0.157 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.00 BSC			0.157 BSC		
SE	1.00 TYP			0.039 TYP		
SD	1.00 TYP			0.039 TYP		
e	1.00 BSC			0.039 TBSC		
ccc	---	---	0.10	---	---	0.0039



Note:
1. Ball land: 0.45mm. Ball opening: 0.35mm
   PCB Ball land suggested ≤ 0.35mm

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14. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01-001	Jan. 24, 2025	All	Initial formal datasheet

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