winbond

# 1M × 4 BANKS × 16 BITS DDR SDRAM

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## 1. GENERAL DESCRIPTION

W9464G6JH is a CMOS Double Data Rate synchronous dynamic random access memory (DDR SDRAM); organized as 1M words × 4 banks × 16 bits. W9464G6JH delivers a data bandwidth of up to 500M words per second (-4). To fully comply with the personal computer industrial standard, W9464G6JH is sorted into the following speed grades: -4, -5 and -5I. The -4 is compliant to the DDR500/CL3 and CL4 specification. The -5/-5I is compliant to the DDR400/CL3 specification (the -5I grade which is guaranteed to support -40°C ~ 85°C).

All Inputs reference to the positive edge of CLK (except for DQ, DM and CKE). The timing reference point for the differential clock is when the CLK and $\overline{CLK}$ signals cross during a transition. Write and Read data are synchronized with the both edges of DQS (Data Strobe).

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. W9464G6JH is ideal for any high performance applications.

## 2. FEATURES

- 2.5V ±0.2V Power Supply for DDR400
- 2.4V~2.7V Power Supply for DDR500
- Up to 250 MHz Clock Frequency
- Double Data Rate architecture; two data transfers per clock cycle
- Differential clock inputs (CLK and $\overline{CLK}$ )
- DQS is edge-aligned with data for Read; center-aligned with data for Write
- CAS Latency: 2, 2.5, 3 and 4
- Burst Length: 2, 4 and 8
- Auto Refresh and Self Refresh
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = 1
- 15.6µS Refresh interval (4K/64 mS Refresh)
- Maximum burst refresh cycle: 8
- Interface: SSTL_2
- Packaged in TSOP II 66-pin, using Lead free materials with RoHS compliant



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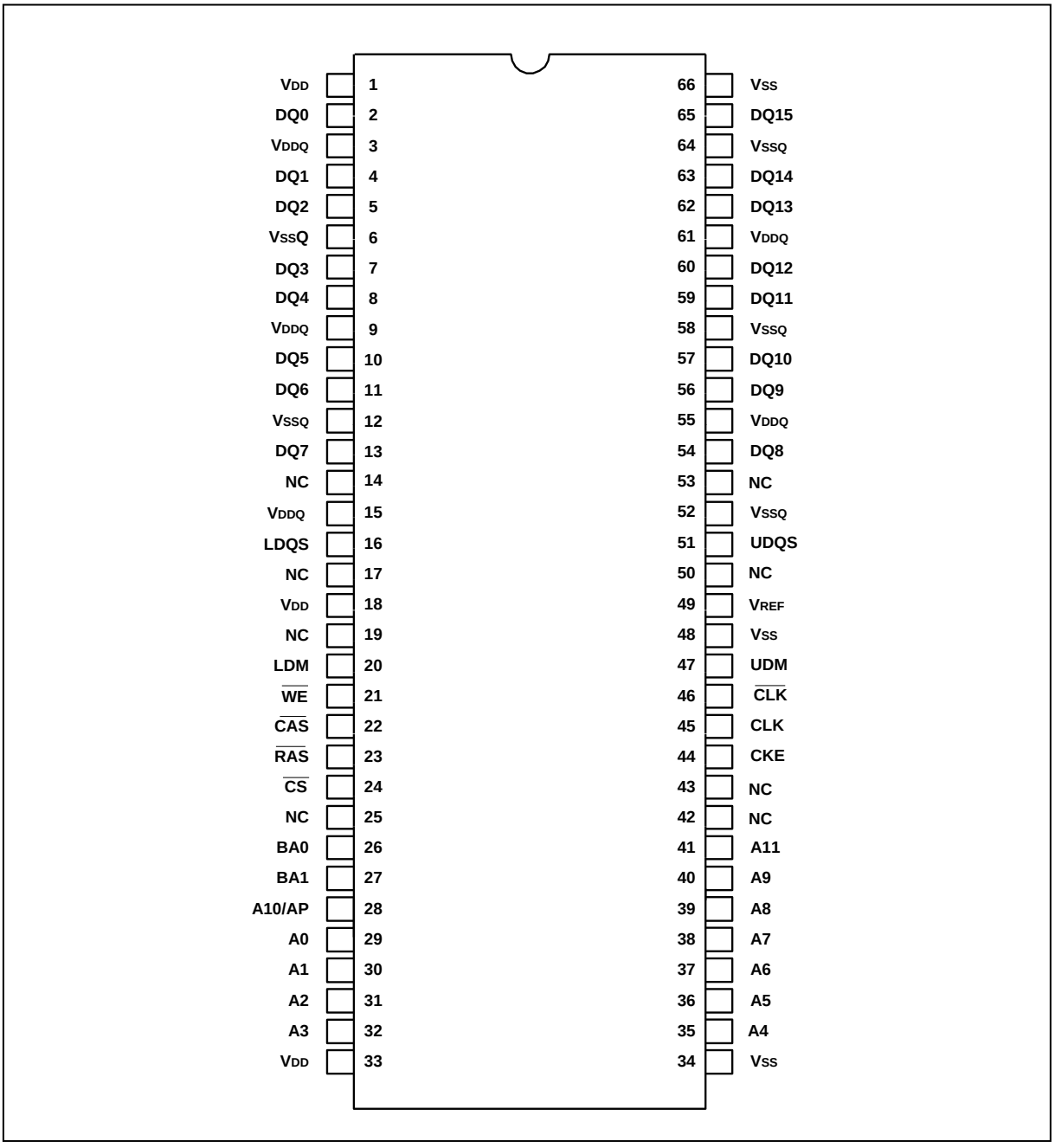
## 3. KEY PARAMETERS

| SYMBOL | DESCRIPTION | | MIN/MAX. | -4 | -5/-5I |
|---|---|---|---|---|---|
| tCK | Clock Cycle Time | CL = 2 | Min. | - | 7.5 nS |
| | | | Max. | - | 10 nS |
| | | CL = 2.5 | Min. | - | 6 nS |
| | | | Max. | - | 10 nS |
| | | CL = 3 | Min. | 4 nS | 5 nS |
| | | | Max. | 10 nS | 10 nS |
| | | CL = 4 | Min. | 4 nS | - |
| | | | Max. | 10 nS | - |
| tRAS | Active to Precharge Command Period | | Min. | 40 nS | 40 nS |
| tRC | Active to Ref/Active Command Period | | Min. | 55 nS | 55 nS |
| IDD0 | Operating current | | Max. | 50 mA | 45 mA |
| IDD1 | Operation Current (Single bank) | | Max. | 60 mA | 55 mA |
| IDD2F | Precharge floating standby current | | Max. | 25 mA | 25 mA |
| IDD2Q | Precharge quiet standby current | | Max. | 25 mA | 25 mA |
| IDD4R | Burst Operation Current | | Max. | 110 mA | 100 mA |
| IDD4W | Burst Operation Current | | Max. | 105 mA | 95 mA |
| IDD5 | Auto Refresh Burst current | | Max. | 60 mA | 60 mA |
| IDD6 | Self-Refresh Current | | Max. | 2 mA | 2 mA |



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## 4. PIN CONFIGURATION






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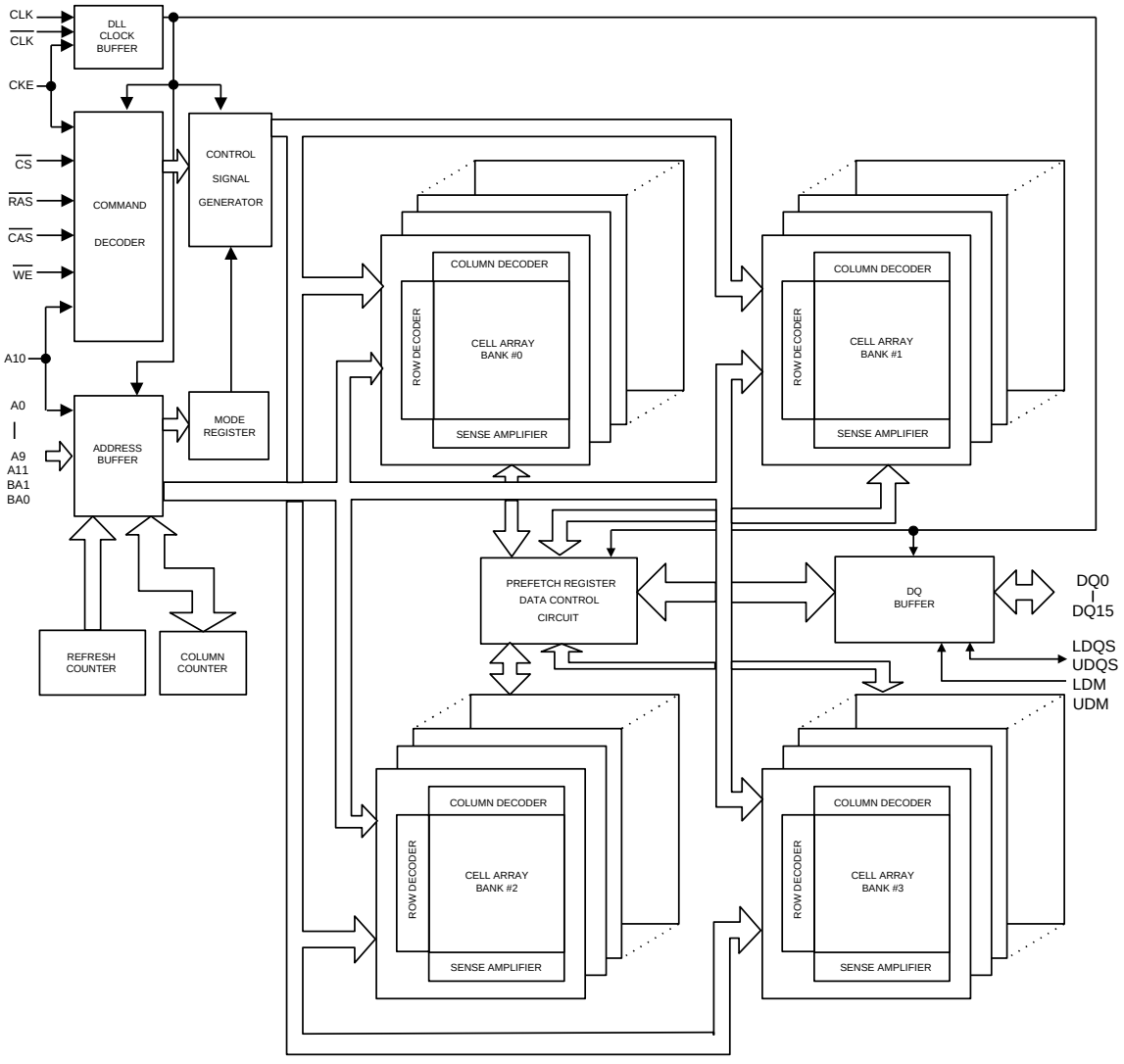
## 5. PIN DESCRIPTION

| PIN NUMBER | PIN NAME | FUNCTION | DESCRIPTION |
|---|---|---|---|
| 28 – 32, 35 – 41 | A0 – A11 | Address | Multiplexed pins for row and column address.<br>Row address: A0 – A11.<br>Column address: A0 – A7. (A10 is used for Auto-precharge) |
| 26, 27 | BA0, BA1 | Bank Select | Select bank to activate during row address latch time, or bank to read/write during column address latch time. |
| 2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65 | DQ0 – DQ15 | Data Input/ Output | The DQ0 – DQ15 input and output data are synchronized with both edges of DQS. |
| 16,51 | LDQS, UDQS | Data Strobe | DQS is Bi-directional signal. DQS is input signal during write operation and output signal during read operation. It is Edge-aligned with read data, Center-aligned with write data. |
| 24 | $\overline{CS}$ | Chip Select | Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues. |
| 23, 22, 21 | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Command Inputs | Command inputs (along with $\overline{CS}$) define the command being entered. |
| 20, 47 | LDM, UDM | Write Mask | When DM is asserted “high” in burst write, the input data is masked. DM is synchronized with both edges of DQS. |
| 45, 46 | CLK, $\overline{CLK}$ | Differential Clock Inputs | All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of $\overline{CLK}$. |
| 44 | CKE | Clock Enable | CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered. |
| 49 | $V_{REF}$ | Reference Voltage | $V_{REF}$ is reference voltage for inputs. |
| 1, 18, 33 | $V_{DD}$ | Power | Power for logic circuit inside DDR SDRAM. |
| 34, 48, 66 | $V_{SS}$ | Ground | Ground for logic circuit inside DDR SDRAM. |
| 3, 9, 15, 55, 61 | $V_{DDQ}$ | Power for I/O Buffer | Separated power from $V_{DD}$, used for output buffer, to improve noise. |
| 6, 12, 52, 58, 64 | $V_{SSQ}$ | Ground for I/O Buffer | Separated ground from $V_{SS}$, used for output buffer, to improve noise. |
| 14, 17, 19, 25, 42, 43, 50, 53 | NC | No Connection | No connection |



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## 6. BLOCK DIAGRAM




NOTE : The cell array configuration is 4096 * 256 * 16



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# 7. FUNCTIONAL DESCRIPTION

## 7.1 Power Up Sequence

(1) Apply power and attempt to CKE at a low state (≤ 0.2V), all other inputs may be undefined
   1) Apply $V_{DD}$ before or at the same time as $V_{DDQ}$.
   2) Apply $V_{DDQ}$ before or at the same time as $V_{TT}$ and $V_{REF}$.

(2) Start Clock and maintain stable condition for 200 µS (min.).

(3) After stable power and clock, apply NOP and take CKE high.

(4) Issue precharge command for all banks of the device.

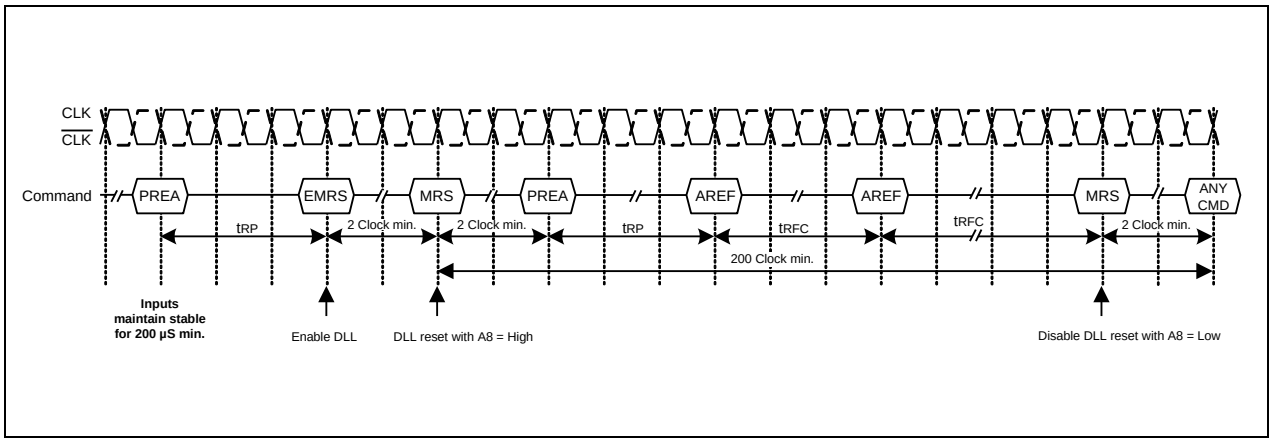
(5) Issue EMRS (Extended Mode Register Set) to enable DLL and establish Output Driver Type.

(6) Issue MRS (Mode Register Set) to reset DLL and set device to idle with bit A8.
(An additional 200 cycles(min) of clock are required for DLL Lock before any executable command applied.)

(7) Issue precharge command for all banks of the device.

(8) Issue two or more Auto Refresh commands.

(9) Issue MRS-Initialize device operation with the reset DLL bit deactivated A8 to low.




**Initialization sequence after power-up**



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## 7.2 Command Function

### 7.2.1 Bank Activate Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "H", BA0, BA1 = Bank, A0 to A11 = Row Address)

The Bank Activate command activates the bank designated by the BA (Bank address) signal. Row addresses are latched on A0 to A11 when this command is issued and the cell data is read out of the sense amplifiers. The maximum time that each bank can be held in the active state is specified as $t_{RAS\ (max)}$. After this command is issued, Read or Write operation can be executed.

### 7.2.2 Bank Precharge Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "L", BA0, BA1 = Bank, A10 = "L", A0 to A9, A11 = Don't Care)

The Bank Precharge command percharges the bank designated by BA. The precharged bank is switched from the active state to the idle state.

### 7.2.3 Precharge All Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "L", BA0, BA1 = Don't Care, A10 = "H", A0 to A9, A11 = Don't Care)

The Precharge All command precharges all banks simultaneously. Then all banks are switched to the idle state.

### 7.2.4 Write Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0, BA1 = Bank, A10 = "L", A0 to A7 = Column Address)

The write command performs a Write operation to the bank designated by BA. The write data are latched at both edges of DQS. The length of the write data (Burst Length) and column access sequence (Addressing Mode) must be in the Mode Register at power-up prior to the Write operation.

### 7.2.5 Write with Auto-precharge Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0, BA1 = Bank, A10 = "H", A0 to A7 = Column Address)

The Write with Auto-precharge command performs the Precharge operation automatically after the Write operation. This command must not be interrupted by any other commands.

### 7.2.6 Read Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", BA0, BA1 = Bank, A10 = "L", A0 to A7 = Column Address)

The Read command performs a Read operation to the bank designated by BA. The read data are synchronized with both edges of DQS. The length of read data (Burst Length), Addressing Mode and CAS Latency (access time from $\overline{CAS}$ command in a clock cycle) must be programmed in the Mode Register at power-up prior to the Read operation.

### 7.2.7 Read with Auto-precharge Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", BA0, BA1 = Bank, A10 = "H", A0 to A7 = Column Address)

The Read with Auto-precharge command automatically performs the Precharge operation after the Read operation.



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1. READA ≥ $t_{RAS\ (min)}$ – (BL/2) x $t_{CK}$

Internal precharge operation begins after BL/2 cycle from Read with Auto-precharge command.

2. $t_{RCD(min)}$ ≤ READA < $t_{RAS(min)}$ – (BL/2) x $t_{CK}$

Data can be read with shortest latency, but the internal Precharge operation does not begin until after $t_{RAS\ (min)}$ has completed.

This command must not be interrupted by any other command.

### 7.2.8 Mode Register Set Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "L", BA1 = "L", A0 to A11 = Register Data)

The Mode Register Set command programs the values of CAS Latency, Addressing Mode, Burst Length and DLL reset in the Mode Register. The default values in the Mode Register after power-up are undefined, therefore this command must be issued during the power-up sequence. Also, this command can be issued while all banks are in the idle state. Refer to the table for specific codes.

### 7.2.9 Extended Mode Register Set Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "H", BA1 = "L", A0 to A11 = Register data)

The Extended Mode Register Set command can be implemented as needed for function extensions to the standard (SDR-SDRAM). Currently the only available mode in EMRS is DLL enable/disable, decoded by A0. The default value of the extended mode register is not defined; therefore this command must be issued during the power-up sequence for enabling DLL. Refer to the table for specific codes.

### 7.2.10 No-Operation Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "H", $\overline{WE}$ = "H")

The No-Operation command simply performs no operation (same command as Device Deselect).

### 7.2.11 Burst Read Stop Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "H", $\overline{WE}$ = "L")

The Burst stop command is used to stop the burst operation. This command is only valid during a Burst Read operation.

### 7.2.12 Device Deselect Command

($\overline{CS}$ = "H")

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

### 7.2.13 Auto Refresh Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", CKE = "H", BA0, BA1, A0 to A11 = Don't Care)

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS–BEFORE–RAS (CBR) refresh in previous DRAM types. This command is non persistent, so it must be issued each time a refresh is required.
The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The DDR SDRAM requires AUTO



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REFRESH cycles at an average periodic interval of $t_{REFI}$ (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 * $t_{REFI}$.

### 7.2.14 Self Refresh Entry Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", CKE = "L", BA0, BA1, A0 to A11 = Don't Care)

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH. Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles should occur before a READ command can be issued. Input signals except CKE are "Don't Care" during SELF REFRESH. Since CKE is an SSTL_2 input, $V_{REF}$ must be maintained during SELF REFRESH.

### 7.2.15 Self Refresh Exit Command

(CKE = "H", $\overline{CS}$ = "H" or CKE = "H", $\overline{RAS}$ = "H", $\overline{CAS}$ = "H")

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for $t_{XSNR}$ because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

The use of SELF REFREH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra auto refresh command is recommended.

### 7.2.16 Data Write Enable /Disable Command

(DM = "L/H" or LDM, UDM = "L/H")

During a Write cycle, the DM or LDM, UDM signal functions as Data Mask and can control every word of the input data. The LDM signal controls DQ0 to DQ7 and UDM signal controls DQ8 to DQ15.

## 7.3 Read Operation

Issuing the Bank Activate command to the idle bank puts it into the active state. When the Read command is issued after $t_{RCD}$ from the Bank Activate command, the data is read out sequentially, synchronized with both edges of DQS (Burst Read operation). The initial read data becomes available after CAS Latency from the issuing of the Read command. The CAS Latency must be set in the Mode Register at power-up.

When the Precharge Operation is performed on a bank during a Burst Read and operation, the Burst operation is terminated.

When the Read with Auto-precharge command is issued, the Precharge operation is performed automatically after the Read cycle then the bank is switched to the idle state. This command cannot be interrupted by any other commands. Refer to the diagrams for Read operation.



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## 7.4 Write Operation

Issuing the Write command after $t_{RCD}$ from the bank activate command. The input data is latched sequentially, synchronizing with both edges(rising & falling) of DQS after the Write command (Burst write operation). The burst length of the Write data (Burst Length) and Addressing Mode must be set in the Mode Register at power-up.

When the Precharge operation is performed in a bank during a Burst Write operation, the Burst operation is terminated.

When the Write with Auto-precharge command is issued, the Precharge operation is performed automatically after the Write cycle, then the bank is switched to the idle state, The Write with Auto-precharge command cannot be interrupted by any other command for the entire burst data duration.

Refer to the diagrams for Write operation.

## 7.5 Precharge

There are two Commands, which perform the precharge operation (Bank Precharge and Precharge All). When the Bank Precharge command is issued to the active bank, the bank is precharged and then switched to the idle state. The Bank Precharge command can precharge one bank independently of the other bank and hold the unprecharged bank in the active state. The maximum time each bank can be held in the active state is specified as $t_{RAS\ (max)}$. Therefore, each bank must be precharged within $t_{RAS(max)}$ from the bank activate command.

The Precharge All command can be used to precharge all banks simultaneously. Even if banks are not in the active state, the Precharge All command can still be issued. In this case, the Precharge operation is performed only for the active bank and the precharge bank is then switched to the idle state.

## 7.6 Burst Termination

When the Precharge command is used for a bank in a Burst cycle, the Burst operation is terminated. When Burst Read cycle is interrupted by the Precharge command, read operation is disabled after clock cycle of (CAS Latency) from the Precharge command. When the Burst Write cycle is interrupted by the Precharge command, the input circuit is reset at the same clock cycle at which the precharge command is issued. In this case, the DM signal must be asserted “high” during $t_{WR}$ to prevent writing the invalided data to the cell array.

When the Burst Read Stop command is issued for the bank in a Burst Read cycle, the Burst Read operation is terminated. The Burst read Stop command is not supported during a write burst operation. Refer to the diagrams for Burst termination.

## 7.7 Refresh Operation

Two types of Refresh operation can be performed on the device: Auto Refresh and Self Refresh. By repeating the Auto Refresh cycle, each bank in turn refreshed automatically. The Refresh operation must be performed 4096 times (rows) within 64mS. The period between the Auto Refresh command and the next command is specified by $t_{RFC}$.

Self Refresh mode enters issuing the Self Refresh command (CKE asserted “low”) while all banks are in the idle state. The device is in Self Refresh mode for as long as CKE held “low”. In the case of distributed Auto Refresh commands, distributed auto refresh commands must be issued every 15.6 µS and the last distributed Auto Refresh commands must be performed within 15.6 µS before entering the self refresh mode. After exiting from the Self Refresh mode, the refresh operation must be performed within 15.6 µS. In Self Refresh mode, all input/output buffers are disabled,



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resulting in lower power dissipation (except CKE buffer). Refer to the diagrams for Refresh operation.

## 7.8 Power Down Mode

Two types of Power Down Mode can be performed on the device: Active Standby Power Down Mode and Precharge Standby Power Down Mode.

When the device enters the Power Down Mode, all input/output buffers are disabled resulting in low power dissipation (except CKE buffer).

Power Down Mode enter asserting CKE “low” while the device is not running a burst cycle. Taking CKE “high” can exit this mode. When CKE goes high, a No operation command must be input at next CLK rising edge. Refer to the diagrams for Power Down Mode.

## 7.9 Input Clock Frequency Change during Precharge Power Down Mode

DDR SDRAM input clock frequency can be changed under following condition:

DDR SDRAM must be in precharged power down mode with CKE at logic LOW level. After a minimum of 2 clocks after CKE goes LOW, the clock frequency may change to any frequency between minimum and maximum operating frequency specified for the particular speed grade. During an input clock frequency change, CKE must be held LOW. Once the input clock frequency is changed, a stable clock must be provided to DRAM before precharge power down mode may be exited. The DLL must be RESET via EMRS after precharge power down exit. An additional MRS command may need to be issued to appropriately set CL etc. After the DLL relock time, the DRAM is ready to operate with new clock frequency.

## 7.10 Mode Register Operation

The mode register is programmed by the Mode Register Set command (MRS/EMRS) when all banks are in the idle state. The data to be set in the Mode Register is transferred using the A0 to A11 and BA0, BA1 address inputs.

The Mode Register designates the operation mode for the read or write cycle. The register is divided into five filed: (1) Burst Length field to set the length of burst data (2) Addressing Mode selected bit to designate the column access sequence in a Burst cycle (3) CAS Latency field to set the assess time in clock cycle (4) DLL reset field to reset the DLL (5) Regular/Extended Mode Register filed to select a type of MRS (Regular/Extended MRS). EMRS cycle can be implemented the extended function (DLL enable/Disable mode).

The initial value of the Mode Register (including EMRS) after power up is undefined; therefore the Mode Register Set command must be issued before power operation.

### 7.10.1 Burst Length field (A2 to A0)

This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 2, 4 and 8 words.

| A2 | A1 | A0 | BURST LENGTH |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | 2 words |
| 0 | 1 | 0 | 4 words |
| 0 | 1 | 1 | 8 words |
| 1 | x | x | Reserved |



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### 7.10.2 Addressing Mode Select (A3)

The Addressing Mode can be one of two modes; Interleave mode or Sequential Mode, When the A3 bit is “0”, Sequential mode is selected. When the A3 bit is “1”, Interleave mode is selected. Both addressing Mode support burst length 2, 4 and 8 words.

| A3 | ADDRESSING MODE |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

#### 7.10.2.1. Addressing Sequence of Sequential Mode

A column access is performed by incrementing the column address input to the device. The address is varied by the Burst Length as the following.

**Addressing Sequence of Sequential Mode**

| DATA | ACCESS ADDRESS | BURST LENGTH |
|---|---|---|
| Data 0 | n | 2 words (address bits is A0) |
| Data 1 | n + 1 | not carried from A0 to A1 |
| Data 2 | n + 2 | 4 words (address bit A0, A1) |
| Data 3 | n + 3 | Not carried from A1 to A2 |
| Data 4 | n + 4 | |
| Data 5 | n + 5 | 8 words (address bits A2, A1 and A0) |
| Data 6 | n + 6 | Not carried from A2 to A3 |
| Data 7 | n + 7 | |

#### 7.10.2.2. Addressing Sequence for Interleave Mode

A Column access is started from the inputted column address and is performed by interleaving the address bits in the sequence shown as the following.

**Addressing Sequence of Interleave Mode**

| DATA | ACCESS ADDRESS | BURST LENGTH |
|---|---|---|
| Data 0 | A8 A7 A6 A5 A4 A3 A2 A1 A0 | 2 words |
| Data 1 | A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$ | |
| Data 2 | A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0 | 4 words |
| Data 3 | A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$ | |
| Data 4 | A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0 | 8 words |
| Data 5 | A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$ | |
| Data 6 | A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0 | |
| Data 7 | A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$ | |



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### 7.10.3 CAS Latency field (A6 to A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first data read. The minimum values of CAS Latency depend on the frequency of CLK.

| A6 | A5 | A4 | CAS LATENCY |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | 2.5 |
| 1 | 1 | 1 | Reserved |

### 7.10.4 DLL Reset bit (A8)

This bit is used to reset DLL. When the A8 bit is "1", DLL is reset.

### 7.10.5 Mode Register /Extended Mode register change bits (BA0, BA1)

These bits are used to select MRS/EMRS.

| BA1 | BA0 | A11-A0 |
|---|---|---|
| 0 | 0 | Regular MRS Cycle |
| 0 | 1 | Extended MRS Cycle |
| 1 | x | Reserved |

### 7.10.6 Extended Mode Register field

1) DLL Switch field (A0)

This bit is used to select DLL enable or disable

| A0 | DLL |
|---|---|
| 0 | Enable |
| 1 | Disable |

2) Output Driver Strength Control field (A6, A1)

The 100%, 60% and 30% or matched impedance driver strength are required Extended Mode Register Set (EMRS) as the following:

| A6 | A1 | BUFFER STRENGTH |
|---|---|---|
| 0 | 0 | 100% Strength |
| 0 | 1 | 60% Strength |
| 1 | 0 | Reserved |
| 1 | 1 | 30% Strength |

### 7.10.7 Reserved field

- Test mode entry bit (A7)
  This bit is used to enter Test mode and must be set to "0" for normal operation.
- Reserved bits (A9, A10, A11)
  These bits are reserved for future operations. They must be set to "0" for normal operation.



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## 8. OPERATION MODE

The following table shows the operation commands.

### 8.1 Simplified Truth Table

| SYM. | COMMAND | DEVICE STATE | CKEn-1 | CKEn | DM[4] | BA0, BA1 | A10 | A0-A9 ,A11 | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ACT | Bank Active | Idle[3] | H | X | X | V | V | V | L | L | H | H |
| PRE | Bank Precharge | Any[3] | H | X | X | V | L | X | L | L | H | L |
| PREA | Precharge All | Any | H | X | X | X | H | X | L | L | H | L |
| WRIT | Write | Active[3] | H | X | X | V | L | V | L | H | L | L |
| WRITA | Write with Auto-precharge | Active[3] | H | X | X | V | H | V | L | H | L | L |
| READ | Read | Active[3] | H | X | X | V | L | V | L | H | L | H |
| READA | Read with Auto-precharge | Active[3] | H | X | X | V | H | V | L | H | L | H |
| MRS | Mode Register Set | Idle | H | X | X | L, L | C | C | L | L | L | L |
| EMRS | Extended Mode Register Set | Idle | H | X | X | H, L | V | V | L | L | L | L |
| NOP | No Operation | Any | H | X | X | X | X | X | L | H | H | H |
| BST | Burst Read Stop | Active | H | X | X | X | X | X | L | H | H | L |
| DSL | Device Deselect | Any | H | X | X | X | X | X | H | X | X | X |
| AREF | Auto Refresh | Idle | H | H | X | X | X | X | L | L | L | H |
| SELF | Self Refresh Entry | Idle | H | L | X | X | X | X | L | L | L | H |
| SELEX | Self Refresh Exit | Idle (Self Refresh) | L | H | X | X | X | X | H | X | X | X |
| | | | | | | | | | L | H | H | X |
| PD | Power Down Mode Entry | Idle/ Active[5] | H | L | X | X | X | X | H | X | X | X |
| | | | | | | | | | L | H | H | X |
| PDEX | Power Down Mode Exit | Any (Power Down) | L | H | X | X | X | X | H | X | X | X |
| | | | | | | | | | L | H | H | X |
| WDE | Data Write Enable | Active | H | X | L | X | X | X | X | X | X | X |
| WDD | Data Write Disable | Active | H | X | H | X | X | X | X | X | X | X |

**Notes:**

1. V = Valid X = Don't Care L = Low level H = High level
2. CKEn signal is input level when commands are issued.
   CKEn-1 signal is input level one clock cycle before the commands are issued.
3. These are state designated by the BA0, BA1 signals.
4. LDM, UDM (W9464G6JH).
5. Power Down Mode can not entry in the burst cycle.



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## 8.2 Function Truth Table

(Note 1)

| CURRENT STATE | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ADDRESS | COMMAND | ACTION | NOTES |
|---|---|---|---|---|---|---|---|---|
| Idle | H | X | X | X | X | DSL | NOP | |
| | L | H | H | X | X | NOP/BST | NOP | |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA, RA | ACT | Row activating | |
| | L | L | H | L | BA, A10 | PRE/PREA | NOP | |
| | L | L | L | H | X | AREF/SELF | Refresh or Self refresh | 2 |
| | L | L | L | L | Op-Code | MRS/EMRS | Mode register accessing | 2 |
| Row Active | H | X | X | X | X | DSL | NOP | |
| | L | H | H | X | X | NOP/BST | NOP | |
| | L | H | L | H | BA, CA, A10 | READ/READA | Begin read: Determine AP | 4 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | Begin write: Determine AP | 4 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PREA | Precharge | 5 |
| | L | L | L | H | X | AREF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL | |
| Read | H | X | X | X | X | DSL | Continue burst to end | |
| | L | H | H | H | X | NOP | Continue burst to end | |
| | L | H | H | L | X | BST | Burst stop | |
| | L | H | L | H | BA, CA, A10 | READ/READA | Term burst, new read: Determine AP | 6 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL | |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PREA | Term burst, Precharging | |
| | L | L | L | H | X | AREF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL | |
| Write | H | X | X | X | X | DSL | Continue burst to end | |
| | L | H | H | H | X | NOP | Continue burst to end | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA, CA, A10 | READ/READA | Term burst, start read: Determine AP | 6, 7 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | Term burst, start read: Determine AP | 6 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PREA | Term burst, Precharging | 8 |
| | L | L | L | H | X | AREF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL | |



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Function Truth Table, continued

| CURRENT STATE | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ADDRESS | COMMAND | ACTION | NOTES |
|---|---|---|---|---|---|---|---|---|
| Read with Auto-precharge | H | X | X | X | X | DSL | Continue burst to end | |
| | L | H | H | H | X | NOP | Continue burst to end | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL | |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PREA | ILLEGAL | |
| | L | L | L | H | X | AREF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL | |
| Write with Auto-precharge | H | X | X | X | X | DSL | Continue burst to end | |
| | L | H | H | H | X | NOP | Continue burst to end | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL | |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL | |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PREA | ILLEGAL | 3 |
| | L | L | L | H | X | AREF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL | |
| Precharging | H | X | X | X | X | DSL | NOP-> Idle after $t_{RP}$ | |
| | L | H | H | H | X | NOP | NOP-> Idle after $t_{RP}$ | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PREA | Idle after $t_{RP}$ | |
| | L | L | L | H | X | AREF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL | |
| Row Activating | H | X | X | X | X | DSL | NOP-> Row active after $t_{RCD}$ | |
| | L | H | H | H | X | NOP | NOP-> Row active after $t_{RCD}$ | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PREA | ILLEGAL | 3 |
| | L | L | L | H | X | AREF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL | |



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Function Truth Table, continued

| CURRENT STATE | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ADDRESS | COMMAND | ACTION | NOTES |
|---|---|---|---|---|---|---|---|---|
| Write Recovering | H | X | X | X | X | DSL | NOP->Row active after $t_{WR}$ | |
| | L | H | H | H | X | NOP | NOP->Row active after $t_{WR}$ | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PREA | ILLEGAL | 3 |
| | L | L | L | H | X | AREF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL | |
| Write Recovering with Auto-precharge | H | X | X | X | X | DSL | NOP->Enter precharge after $t_{WR}$ | |
| | L | H | H | H | X | NOP | NOP->Enter precharge after $t_{WR}$ | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PREA | ILLEGAL | 3 |
| | L | L | L | H | X | AREF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS/EMRS | ILLEGAL | |
| Refreshing | H | X | X | X | X | DSL | NOP->Idle after $t_{RC}$ | |
| | L | H | H | H | X | NOP | NOP->Idle after $t_{RC}$ | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | X | READ/WRIT | ILLEGAL | |
| | L | L | H | X | X | ACT/PRE/PREA | ILLEGAL | |
| | L | L | L | X | X | AREF/SELF/MRS/EMRS | ILLEGAL | |
| Mode Register Accessing | H | X | X | X | X | DSL | NOP->Row after $t_{MRD}$ | |
| | L | H | H | H | X | NOP | NOP->Row after $t_{MRD}$ | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | X | X | READ/WRIT | ILLEGAL | |
| | L | L | X | X | X | ACT/PRE/PREA/AREF/SELF/MRS/EMRS | ILLEGAL | |

**Notes:**

1. All entries assume that CKE was active (High level) during the preceding clock cycle and the current clock cycle.
2. Illegal if any bank is not idle.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. Illegal if $t_{RCD}$ is not satisfied.
5. Illegal if $t_{RAS}$ is not satisfied.
6. Must satisfy burst interrupt condition.
7. Must avoid bus contention, bus turn around, and/or satisfy write recovery requirements.
8. Must mask preceding data which don't satisfy $t_{WR}$

Remark: H = High level, L = Low level, X = High or Low level (Don't Care), V = Valid data



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## 8.3 Function Truth Table for CKE

| CURRENT STATE | CKE | | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ADDRESS | ACTION | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | n-1 | n | | | | | | | |
| Self Refresh | H | X | X | X | X | X | X | INVALID | |
| | L | H | H | X | X | X | X | Exit Self Refresh->Idle after $t_{XSNR}$ | |
| | L | H | L | H | H | X | X | Exit Self Refresh->Idle after $t_{XSNR}$ | |
| | L | H | L | H | L | X | X | ILLEGAL | |
| | L | H | L | L | X | X | X | ILLEGAL | |
| | L | L | X | X | X | X | X | Maintain Self Refresh | |
| Power Down | H | X | X | X | X | X | X | INVALID | |
| | L | H | X | X | X | X | X | Exit Power down->Idle after $t_{IS}$ | |
| | L | L | X | X | X | X | X | Maintain power down mode | |
| All banks Idle | H | H | X | X | X | X | X | Refer to Function Truth Table | |
| | H | L | H | X | X | X | X | Enter Power down | 2 |
| | H | L | L | H | H | X | X | Enter Power down | 2 |
| | H | L | L | L | L | H | X | Self Refresh | 1 |
| | H | L | L | H | L | X | X | ILLEGAL | |
| | H | L | L | L | X | X | X | ILLEGAL | |
| | L | X | X | X | X | X | X | Power down | |
| Row Active | H | H | X | X | X | X | X | Refer to Function Truth Table | |
| | H | L | H | X | X | X | X | Enter Power down | 3 |
| | H | L | L | H | H | X | X | Enter Power down | 3 |
| | H | L | L | L | L | H | X | ILLEGAL | |
| | H | L | L | H | L | X | X | ILLEGAL | |
| | H | L | L | L | X | X | X | ILLEGAL | |
| | L | X | X | X | X | X | X | Power down | |
| Any State Other Than Listed Above | H | H | X | X | X | X | X | Refer to Function Truth Table | |

**Notes:**

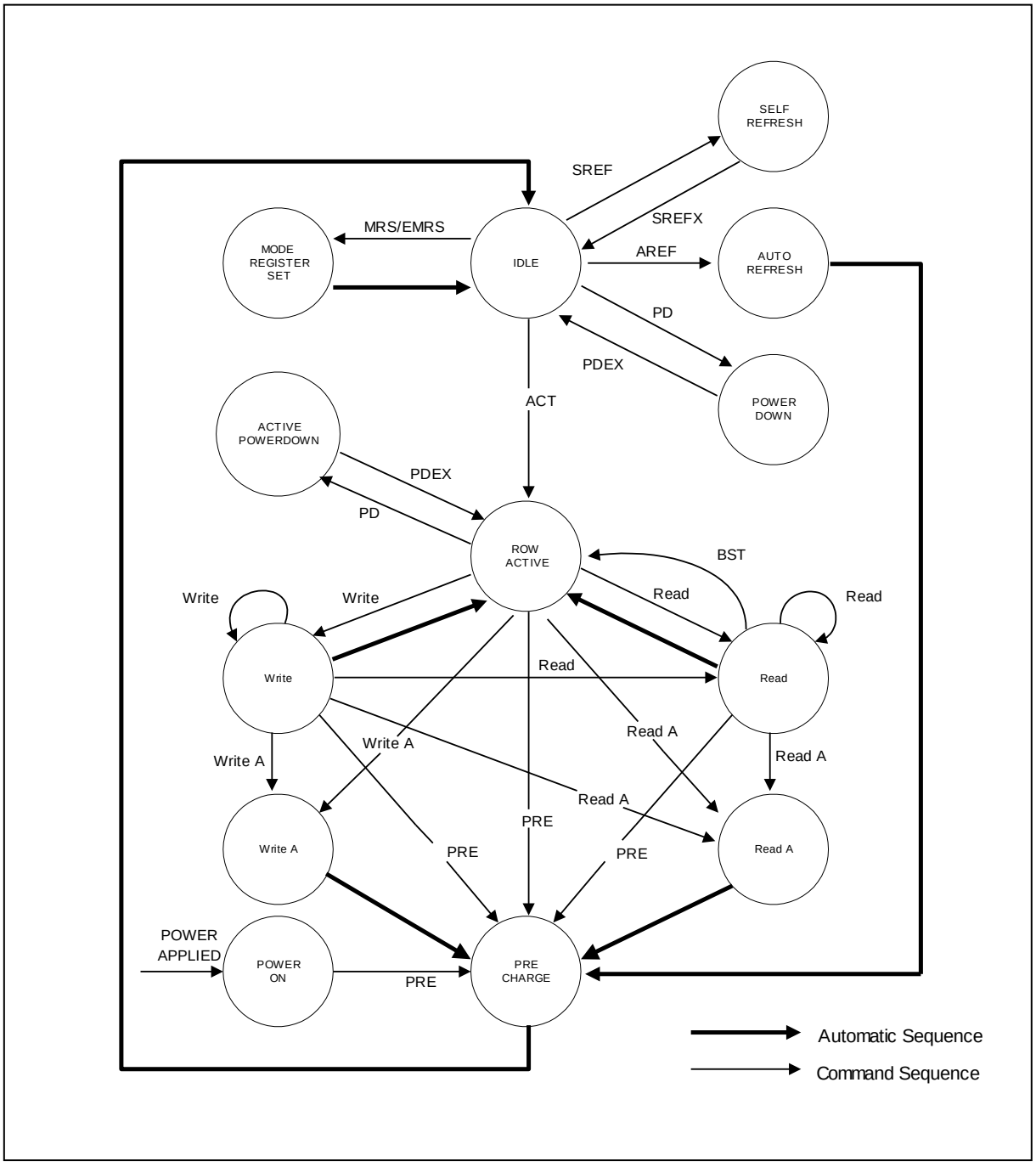
1. Self refresh can enter only from the all banks idle state.
2. Power Down occurs when all banks are idle; this mode is referred to as precharge power down.
3. Power Down occurs when there is a row active in any bank; this mode is referred to as active power down.

Remark: H = High level, L = Low level, X = High or Low level (Don't Care), V = Valid data



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## 8.4 Simplified Stated Diagram






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# 9. ELECTRICAL CHARACTERISTICS

## 9.1 Absolute Maximum Ratings

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Voltage on I/O Pins Relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -0.5 ~ $V_{DDQ}$ +0.5 | V |
| Voltage on Input Pins Relative to $V_{SS}$ | $V_{IN}$ | -1 ~ 3.6 | V |
| Voltage on $V_{DD}$ Supply Relative to $V_{SS}$ | $V_{DD}$ | -1 ~ 3.6 | V |
| Voltage on $V_{DDQ}$ Supply Relative to $V_{SS}$ | $V_{DDQ}$ | -1 ~ 3.6 | V |
| Operating Temperature (-4/-5) | $T_{OPR}$ | 0 ~ 70 | °C |
| Operating Temperature (-5I) | $T_{OPR}$ | -40 ~ 85 | °C |
| Storage Temperature | $T_{STG}$ | -55 ~ 150 | °C |
| Soldering Temperature (10s) | $T_{SOLDER}$ | 260 | °C |
| Power Dissipation | $P_D$ | 1 | W |
| Short Circuit Output Current | $I_{OUT}$ | 50 | mA |

**Note:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 9.2 Recommended DC Operating Conditions

($T_A$ = 0 to 70°C for -4/-5, $T_A$ = -40 to 85°C for -5I)

| SYM. | PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTES |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage (for -5/-5I) | 2.3 | 2.5 | 2.7 | V | 2 |
| $V_{DD}$ | Power Supply Voltage (for -4) | 2.4 | - | 2.7 | V | 2 |
| $V_{DDQ}$ | I/O Buffer Supply Voltage (for -5/-5I) | 2.3 | 2.5 | 2.7 | V | 2 |
| $V_{DDQ}$ | I/O Buffer Supply Voltage (for -4) | 2.4 | - | 2.7 | V | 2 |
| $V_{REF}$ | Input reference Voltage | 0.49 x $V_{DDQ}$ | 0.50 x $V_{DDQ}$ | 0.51 x $V_{DDQ}$ | V | 2, 3 |
| $V_{TT}$ | Termination Voltage (System) | $V_{REF}$ - 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V | 2, 8 |
| $V_{IH\ (DC)}$ | Input High Voltage (DC) | $V_{REF}$ + 0.15 | - | $V_{DDQ}$ + 0.3 | V | 2 |
| $V_{IL\ (DC)}$ | Input Low Voltage (DC) | -0.3 | - | $V_{REF}$ - 0.15 | V | 2 |
| $V_{ICK\ (DC)}$ | Differential Clock DC Input Voltage | -0.3 | - | $V_{DDQ}$ + 0.3 | V | 15 |
| $V_{ID\ (DC)}$ | Input Differential Voltage. CLK and $\overline{CLK}$ inputs (DC) | 0.36 | - | $V_{DDQ}$ + 0.6 | V | 13, 15 |
| $V_{IH\ (AC)}$ | Input High Voltage (AC) | $V_{REF}$ + 0.31 | - | - | V | 2 |
| $V_{IL\ (AC)}$ | Input Low Voltage (AC) | - | - | $V_{REF}$ - 0.31 | V | 2 |
| $V_{ID\ (AC)}$ | Input Differential Voltage. CLK and $\overline{CLK}$ inputs (AC) | 0.7 | - | $V_{DDQ}$ + 0.6 | V | 13, 15 |
| $V_{X\ (AC)}$ | Differential AC input Cross Point Voltage | $V_{DDQ}$/2 - 0.2 | - | $V_{DDQ}$/2 + 0.2 | V | 12, 15 |
| $V_{ISO\ (AC)}$ | Differential Clock AC Middle Point | $V_{DDQ}$/2 - 0.2 | - | $V_{DDQ}$/2 + 0.2 | V | 14, 15 |

**Notes:** $V_{IH\ (DC)}$ and $V_{IL\ (DC)}$ are levels to maintain the current logic state.
$V_{IH\ (AC)}$ and $V_{IL\ (AC)}$ are levels to change to the new logic state.



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## 9.3 Capacitance

($V_{DD}$ = $V_{DDQ}$ = 2.5V ±0.2V, f = 1 MHz, $T_A$ = 25°C, $V_{OUT\ (DC)}$ = $V_{DDQ}$/2, $V_{OUT}$ (Peak to Peak) = 0.2V)

| SYMBOL | PARAMETER | MIN. | MAX. | DELTA (MAX.) | UNIT |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance (except for CLK pins) | 2.0 | 3.0 | 0.5 | pF |
| $C_{CLK}$ | Input Capacitance (CLK pins) | 2.0 | 3.0 | 0.25 | pF |
| $C_{I/O}$ | DQ, DQS, DM Capacitance | 4.0 | 5.0 | 0.5 | pF |
| $C_{NC}$ | NC Pin Capacitance | - | 1.5 | - | pF |

**Notes:** These parameters are periodically sampled and not 100% tested.

The NC pins have additional capacitance for adjustment of the adjacent pin capacitance.

## 9.4 Leakage and Output Buffer Characteristics

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | NOTES |
|---|---|---|---|---|---|
| $I_{I\ (L)}$ | Input Leakage Current<br>Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$, $V_{REF}$ Pin 0V ≤ $V_{IN}$ ≤ 1.35V<br>(All other pins not under test = 0V) | -2 | 2 | µA | |
| $I_{O\ (L)}$ | Output Leakage Current<br>(Output disabled, 0V ≤ $V_{OUT}$ ≤ $V_{DDQ}$) | -5 | 5 | µA | |
| $V_{OH}$ | Output High Voltage<br>(under AC test load condition) | $V_{TT}$ +0.76 | - | V | |
| $V_{OL}$ | Output Low Voltage<br>(under AC test load condition) | - | $V_{TT}$ -0.76 | V | |
| $I_{OH}$ | Output Levels: Full drive option<br>High Current<br>($V_{OUT}$ = $V_{DDQ}$ - 0.373V, min. $V_{REF}$, min. $V_{TT}$ | -15 | - | mA | 4, 6 |
| $I_{OL}$ | Low Current<br>($V_{OUT}$ = 0.373V, max. $V_{REF}$, max. $V_{TT}$) | 15 | - | mA | 4, 6 |
| $I_{OHR}$ | Output Levels: Reduced drive option - 60%<br>High Current<br>($V_{OUT}$ = $V_{DDQ}$ - 0.763V, min. $V_{REF}$, min. $V_{TT}$ | -9 | - | mA | 5 |
| $I_{OLR}$ | Low Current<br>($V_{OUT}$ = 0.763V, max. VREF, max. $V_{TT}$) | 9 | - | mA | 5 |
| $I_{OHR(30)}$ | Output Levels: Reduced drive option - 30%<br>High Current<br>($V_{OUT}$ = $V_{DDQ}$ – 1.056V, min. $V_{REF}$, min. $V_{TT}$ | -4.5 | - | mA | 5 |
| $I_{OLR(30)}$ | Low Current<br>($V_{OUT}$ = 1.056V, max. $V_{REF}$, max. $V_{TT}$) | 4.5 | - | mA | 5 |



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## 9.5 DC Characteristics

| SYM. | PARAMETER | MAX. | | UNIT | NOTES |
|---|---|---|---|---|---|
| | | -4 | -5/-5I | | |
| $I_{DD0}$ | Operating current: One Bank Active-Precharge;<br>$t_{RC}$ = $t_{RC}$ min; $t_{CK}$ = $t_{CK}$ min;<br>DQ, DM and DQS inputs changing once per clock cycle;<br>Address and control inputs changing once every two clock cycles | 50 | 45 | mA | 7 |
| $I_{DD1}$ | Operating current: One Bank Active-Read-Precharge;<br>Burst = 4; $t_{RC}$ = $t_{RC}$ min; CL = 3; $t_{CK}$ = $t_{CK}$ min; $I_{OUT}$ = 0 mA; Address and control inputs changing once per clock cycle. | 60 | 55 | | 7, 9 |
| $I_{DD2P}$ | Precharge Power Down standby current:<br>All Banks Idle; Power down mode;<br>CKE ≤ $V_{IL}$ max; $t_{CK}$ = $t_{CK}$ min; Vin = $V_{REF}$ for DQ, DQS and DM | 5 | 5 | | |
| $I_{DD2N}$ | Idle standby current:<br>$\overline{CS}$ ≥ $V_{IH}$ min; All Banks Idle; CKE ≥ $V_{IH}$ min; $t_{CK}$ = $t_{CK}$ min;<br>Address and other control inputs changing once per clock cycle;<br>Vin ≥ $V_{IH}$ min or Vin ≤ $V_{IL}$ max for DQ, DQS and DM | 25 | 25 | | 7 |
| $I_{DD2F}$ | Precharge floating standby current:<br>$\overline{CS}$ ≥ $V_{IH}$ min; all banks idle; CKE ≥ $V_{IH}$ min;<br>Address and other control inputs changing once per clock cycle;<br>$V_{IN}$ = $V_{REF}$ for DQ, DQS and DM. | 25 | 25 | | |
| $I_{DD2Q}$ | Precharge quiet standby current:<br>$\overline{CS}$ ≥ $V_{IH}$ min; all banks idle; CKE > $V_{IH}$ min;<br>Address and other control inputs stable at > $V_{IH}$ min or ≤ $V_{IL}$ max;<br>Vin = $V_{REF}$ for DQ, DQS and DM. | 25 | 25 | | |
| $I_{DD3P}$ | Active Power Down standby current:<br>One Bank Active; Power down mode;<br>CKE ≤ $V_{IL}$ max; $t_{CK}$ = $t_{CK}$ min;<br>Vin = $V_{REF}$ for DQ, DQS and DM | 15 | 15 | | |
| $I_{DD3N}$ | Active standby current:<br>$\overline{CS}$ ≥ $V_{IH}$ min; CKE ≥ $V_{IH}$ min; One Bank Active-Precharge;<br>$t_{RC}$ = $t_{RAS}$ max; $t_{CK}$ = $t_{CK}$ min;<br>DQ, DM and DQS inputs changing twice per clock cycle;<br>Address and other control inputs changing once per clock cycle | 30 | 30 | | 7 |
| $I_{DD4R}$ | Operating current:<br>Burst = 2; Reads; Continuous burst; One Bank Active;<br>Address and control inputs changing once per clock cycle;<br>CL=2; $t_{CK}$ = $t_{CK}$ min; $I_{OUT}$ = 0mA | 110 | 100 | | 7, 9 |
| $I_{DD4W}$ | Operating current:<br>Burst = 2; Write; Continuous burst; One Bank Active;<br>Address and control inputs changing once per clock cycle;<br>CL = 2; $t_{CK}$ = $t_{CK}$ min;<br>DQ, DM and DQS inputs changing twice per clock cycle | 105 | 95 | | 7 |
| $I_{DD5}$ | Auto Refresh current: $t_{RC}$ = $t_{RFC}$ min | 60 | 60 | | 7 |
| $I_{DD6}$ | Self Refresh current: CKE ≤ 0.2V; external clock on; $t_{CK}$ = $t_{CK}$ min | 2 | 2 | | |
| $I_{DD7}$ | Random Read current: 4 Banks Active Read with activate every 20nS, Auto-Precharge Read every 20 nS;<br>Burst = 4; $t_{RCD}$ = 3; $I_{OUT}$ = 0mA;<br>DQ, DM and DQS inputs changing twice per clock cycle;<br>Address changing once per clock cycle | 120 | 110 | | |



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## 9.6 AC Characteristics and Operating Condition

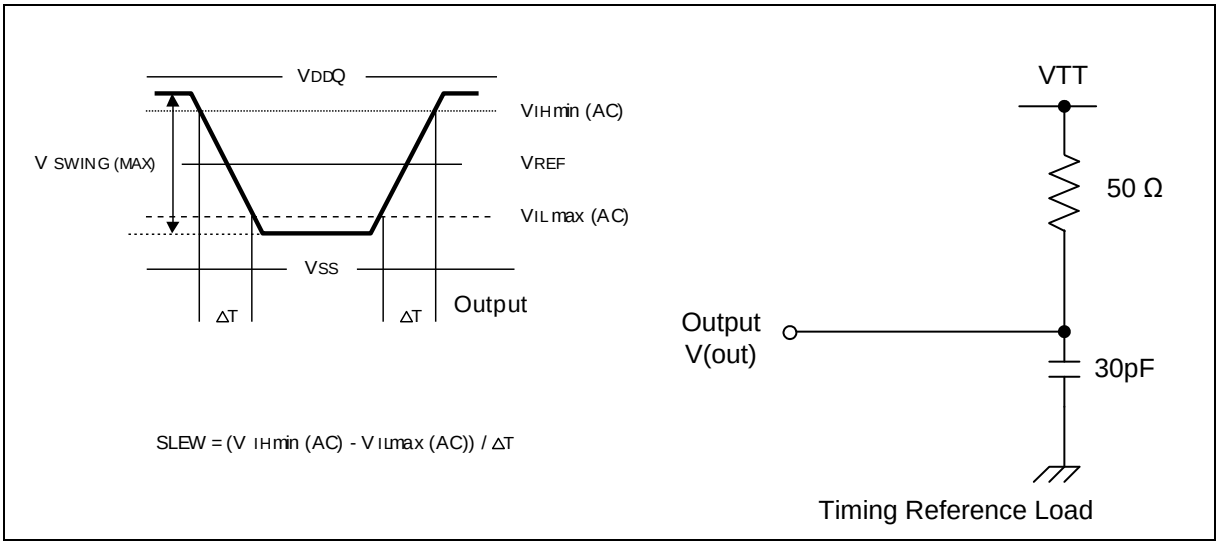
| SYM. | PARAMETER | | -4 | | -5/-5I | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | | |
| $t_{RC}$ | Active to Ref/Active Command Period | | 55 | | 55 | | nS | |
| $t_{RFC}$ | Ref to Ref/Active Command Period | | 60 | | 70 | | | |
| $t_{RAS}$ | Active to Precharge Command Period | | 40 | 70000 | 40 | 100000 | | |
| $t_{RCD}$ | Active to Read/Write Command Delay Time | | 16 | | 15 | | | |
| $t_{RAP}$ | Active to Read with Auto-precharge Enable | | 16 | | 15 | | | |
| $t_{CCD}$ | Read/Write(a) to Read/Write(b) Command Period | | 1 | | 1 | | $t_{CK}$ | |
| $t_{RP}$ | Precharge to Active Command Period | | 16 | | 15 | | nS | |
| $t_{RRD}$ | Active(a) to Active(b) Command Period | | 12 | | 10 | | | |
| $t_{WR}$ | Write Recovery Time | | 15 | | 15 | | | |
| $t_{DAL}$ | Auto-precharge Write Recovery + Precharge Time | | ($t_{WR}/t_{CK}$) + ($t_{RP}/t_{CK}$) | | ($t_{WR}/t_{CK}$) + ($t_{RP}/t_{CK}$) | | $t_{CK}$ | 18 |
| $t_{CK}$ | CLK Cycle Time | CL = 2 | - | - | 7.5 | 10 | nS | |
| | | CL = 2.5 | - | - | 6 | 10 | | |
| | | CL = 3 | 4 | 10 | 5 | 10 | | |
| | | CL = 4 | 4 | 10 | - | - | | |
| $t_{AC}$ | Data Access Time from CLK, $\overline{CLK}$ | | -0.65 | 0.65 | -0.7 | 0.7 | | 16 |
| $t_{DQSCK}$ | DQS Output Access Time from CLK, $\overline{CLK}$ | | -0.55 | 0.55 | -0.6 | 0.6 | | 16 |
| $t_{DQSQ}$ | Data Strobe Edge to Output Data Edge Skew | | | 0.4 | | 0.4 | | |
| $t_{CH}$ | CLk High Level Width | | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | 11 |
| $t_{CL}$ | CLK Low Level Width | | 0.45 | 0.55 | 0.45 | 0.55 | | |
| $t_{HP}$ | CLK Half Period (minimum of actual $t_{CH}$, $t_{CL}$) | | min ($t_{CL}$,$t_{CH}$) | | Min, ($t_{CL}$,$t_{CH}$) | | nS | |
| $t_{QH}$ | DQ Output Data Hold Time from DQS | | $t_{HP}$-0.5 | | $t_{HP}$-0.5 | | | |
| $t_{RPRE}$ | DQS Read Preamble Time | | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ | 11 |
| $t_{RPST}$ | DQS Read Postamble Time | | 0.4 | 0.6 | 0.4 | 0.6 | | |
| $t_{DS}$ | DQ and DM Setup Time to DQS, slew rate 0.5V/nS | | 0.4 | | 0.4 | | nS | |
| $t_{DH}$ | DQ and DM Hold Time to DQS, slew rate 0.5V/nS | | 0.4 | | 0.4 | | | |
| $t_{DIPW}$ | DQ and DM Input Pulse Width (for each input) | | 1.75 | | 1.75 | | | |
| $t_{DQSH}$ | DQS Input High Pulse Width | | 0.35 | | 0.35 | | $t_{CK}$ | 11 |
| $t_{DQSL}$ | DQS Input Low Pulse Width | | 0.35 | | 0.35 | | | |
| $t_{DSS}$ | DQS Falling Edge to CLK Setup Time | | 0.2 | | 0.2 | | | |
| $t_{DSH}$ | DQS Falling Edge Hold Time from CLK | | 0.2 | | 0.2 | | | |
| $t_{WPRES}$ | Clock to DQS Write Preamble Set-up Time | | 0 | | 0 | | nS | |
| $t_{WPRE}$ | DQS Write Preamble Time | | 0.25 | | 0.25 | | $t_{CK}$ | 11 |
| $t_{WPST}$ | DQS Write Postamble Time | | 0.4 | 0.6 | 0.4 | 0.6 | | |
| $t_{DQSS}$ | Write Command to First DQS Latching Transition | | 0.85 | 1.15 | 0.72 | 1.25 | | |
| $t_{IS}$ | Input Setup Time (fast slew rate) | | 0.6 | | 0.6 | | nS | 19, 21-23 |
| $t_{IH}$ | Input Hold Time (fast slew rate) | | 0.6 | | 0.6 | | | 19, 21-23 |
| $t_{IS}$ | Input Setup Time (slow slew rate) | | 0.7 | | 0.7 | | | 20-23 |
| $t_{IH}$ | Input Hold Time (slow slew rate) | | 0.7 | | 0.7 | | | 20-23 |
| $t_{IPW}$ | Control & Address Input Pulse Width (for each input) | | 2.2 | | 2.2 | | | |
| $t_{HZ}$ | Data-out High-impedance Time from CLK, $\overline{CLK}$ | | | 0.7 | | 0.7 | | |
| $t_{LZ}$ | Data-out Low-impedance Time from CLK, $\overline{CLK}$ | | -0.7 | 0.7 | -0.7 | 0.7 | | |
| $t_{T(SS)}$ | SSTL Input Transition | | 0.5 | 1.5 | 0.5 | 1.5 | | |
| $t_{WTR}$ | Internal Write to Read Command Delay | | 2 | | 2 | | $t_{CK}$ | |
| $t_{XSNR}$ | Exit Self Refresh to non-Read Command | | 75 | | 75 | | nS | |
| $t_{XSRD}$ | Exit Self Refresh to Read Command | | 200 | | 200 | | $t_{CK}$ | |
| $t_{REFI}$ | Refresh Interval Time (4K/ 64mS) | | | 15.6 | | 15.6 | µS | 17 |
| $t_{MRD}$ | Mode Register Set Cycle Time | | 8 | | 10 | | nS | |



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## 9.7 AC Test Conditions

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Input High Voltage (AC) | $V_{IH}$ | $V_{REF}$ + 0.31 | V |
| Input Low Voltage (AC) | $V_{IL}$ | $V_{REF}$ - 0.31 | V |
| Input Reference Voltage | $V_{REF}$ | 0.5 x $V_{DDQ}$ | V |
| Termination Voltage | $V_{TT}$ | 0.5 x $V_{DDQ}$ | V |
| Differential Clock Input Reference Voltage | $V_R$ | $V_x$ (AC) | V |
| Input Difference Voltage. CLK and $\overline{CLK}$ Inputs (AC) | $V_{ID}$ (AC) | 1.5 | V |
| Output Timing Measurement Reference Voltage | $V_{OTR}$ | 0.5 x $V_{DDQ}$ | V |




**Notes:**

(1) Conditions outside the limits listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

(2) All voltages are referenced to $V_{DD}$, $V_{DDQ}$.

(3) Peak to peak AC noise on $V_{REF}$ may not exceed ±2% $V_{REF(DC)}$.

(4) $V_{OH}$ = 1.95V, $V_{OL}$ = 0.35V

(5) $V_{OH}$ = 1.9V, $V_{OL}$ = 0.4V

(6) The values of $I_{OH(DC)}$ is based on $V_{DDQ}$ = 2.3V and $V_{TT}$ = 1.19V.
The values of $I_{OL(DC)}$ is based on $V_{DDQ}$ = 2.3V and $V_{TT}$ = 1.11V.

(7) These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of $t_{CK}$ and $t_{RC}$.

(8) $V_{TT}$ is not applied directly to the device. $V_{TT}$ is a system supply for signal termination resistors is expected to be set equal to $V_{REF}$ and must track variations in the DC level of $V_{REF}$.

(9) These parameters depend on the output loading. Specified values are obtained with the output open.

(10) Transition times are measured between $V_{IH\ min(AC)}$ and $V_{IL\ max(AC)}$.Transition (rise and fall) of input signals have a fixed slope.

(11) IF the result of nominal calculation with regard to $t_{CK}$ contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., $t_{DQSS}$ = 1.25 × $t_{CK}$, $t_{CK}$ = 5 nS, 1.25 × 5 nS = 6.25 nS is rounded up to 6.2 nS.)



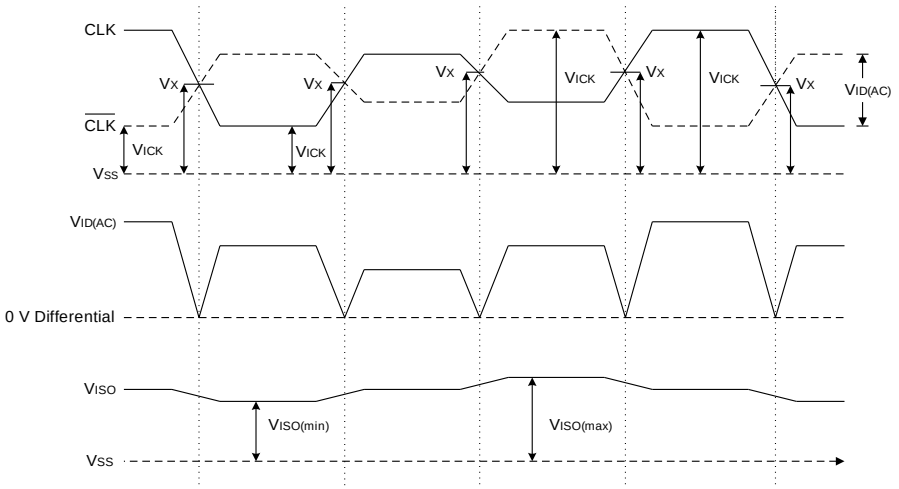
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(12) $V_X$ is the differential clock cross point voltage where input timing measurement is referenced.

(13) $V_{ID}$ is magnitude of the difference between CLK input level and $\overline{CLK}$ input level.

(14) $V_{ISO}$ means {$V_{ICK}$(CLK)+$V_{ICK}$($\overline{CLK}$)}/2.

(15) Refer to the figure below.




(16) $t_{AC}$ and $t_{DQSCK}$ depend on the clock jitter. These timing are measured at stable clock.

(17) A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.

(18) $t_{DAL}$ = ($t_{WR}$/$t_{CK}$) + ($t_{RP}$/$t_{CK}$)

For each of the terms above, if not already an integer, round to the next highest integer.

Example: For -5 speed grade at CL=2.5 and tCK=6 nS

$t_{DAL}$ = ((15 nS / 6 nS) + (15 nS / 6 nS)) clocks = ((3) + (3)) clocks = 6 clocks

(19) For command/address input slew rate ≥1.0 V/nS.

(20) For command/address input slew rate ≥0.5 V/nS and <1.0 V/nS.

(21) For CLK & $\overline{CLK}$ slew rate ≥1.0 V/nS (single-ended).

(22) These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

(23) Slew Rate is measured between VOH(ac) and VOL(ac).



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## 10. SYSTEM CHARACTERISTICS FOR DDR SDRAM

The following specification parameters are required in systems using DDR500 & DDR400 devices to ensure proper system performance. These characteristics are for system simulation purposes and are guaranteed by design.

### 10.1 Table 1: Input Slew Rate for DQ, DQS, and DM

| AC CHARACTERISTICS | SYM. | DDR500 | | DDR400 | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|
| PARAMETER | | MIN. | MAX. | MIN. | MAX. | | |
| DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC) | DCSLEW | 0.5 | 4.0 | 0.5 | 4.0 | V/nS | a, m |

### 10.2 Table 2: Input Setup & Hold Time Derating for Slew Rate

| INPUT SLEW RATE | ΔtIS | ΔtIH | UNIT | NOTES |
|---|---|---|---|---|
| 0.5 V/nS | 0 | 0 | pS | i |
| 0.4 V/nS | +50 | 0 | pS | i |
| 0.3 V/nS | +100 | 0 | pS | i |

### 10.3 Table 3: Input/Output Setup & Hold Time Derating for Slew Rate

| INPUT SLEW RATE | ΔtDS | ΔtDH | UNIT | NOTES |
|---|---|---|---|---|
| 0.5 V/nS | 0 | 0 | pS | k |
| 0.4 V/nS | +75 | 0 | pS | k |
| 0.3 V/nS | +150 | 0 | pS | k |

### 10.4 Table 4: Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

| INPUT SLEW RATE | ΔtDS | ΔtDH | UNIT | NOTES |
|---|---|---|---|---|
| ±0.0 nS/V | 0 | 0 | pS | j |
| ±0.25 nS/V | +50 | 0 | pS | j |
| ±0.5 nS/V | +100 | 0 | pS | j |

### 10.5 Table 5: Output Slew Rate Characteristics (X16 Devices only)

| SLEW RATE CHARACTERISTIC | TYPICAL RANGE (V/NS) | MINIMUM (V/NS) | MAXIMUM (V/NS) | NOTES |
|---|---|---|---|---|
| Pullup Slew Rate | 1.2 ~ 2.5 | 0.7 | 5.0 | a, c, d, f, g, h |
| Pulldown Slew Rate | 1.2 ~ 2.5 | 0.7 | 5.0 | b, c, d, f, g, h |



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## 10.6 Table 6: Output Slew Rate Matching Ratio Characteristics

| SLEW RATE CHARACTERISTIC | DDR500 | | DDR400 | | NOTES |
|---|---|---|---|---|---|
| PARAMETER | MIN. | MAX. | MIN. | MAX. | |
| Output Slew Rate Matching Ratio (Pullup to Pulldown) | 0.67 | 1.5 | 0.67 | 1.5 | e, m |

## 10.7 Table 7: AC Overshoot/Undershoot Specification for Address and Control Pins

| PARAMETER | SPECIFICATION | |
|---|---|---|
| | DDR500 | DDR400 |
| Maximum peak amplitude allowed for overshoot | 1.5 V | 1.5 V |
| Maximum peak amplitude allowed for undershoot | 1.5 V | 1.5 V |
| The area between the overshoot signal and VDD must be less than or equal to Max. area in Figure 3 | 4.5 V-nS | 4.5 V-nS |
| The area between the undershoot signal and GND must be less than or equal to Max. area in Figure 3 | 4.5 V-nS | 4.5 V-nS |

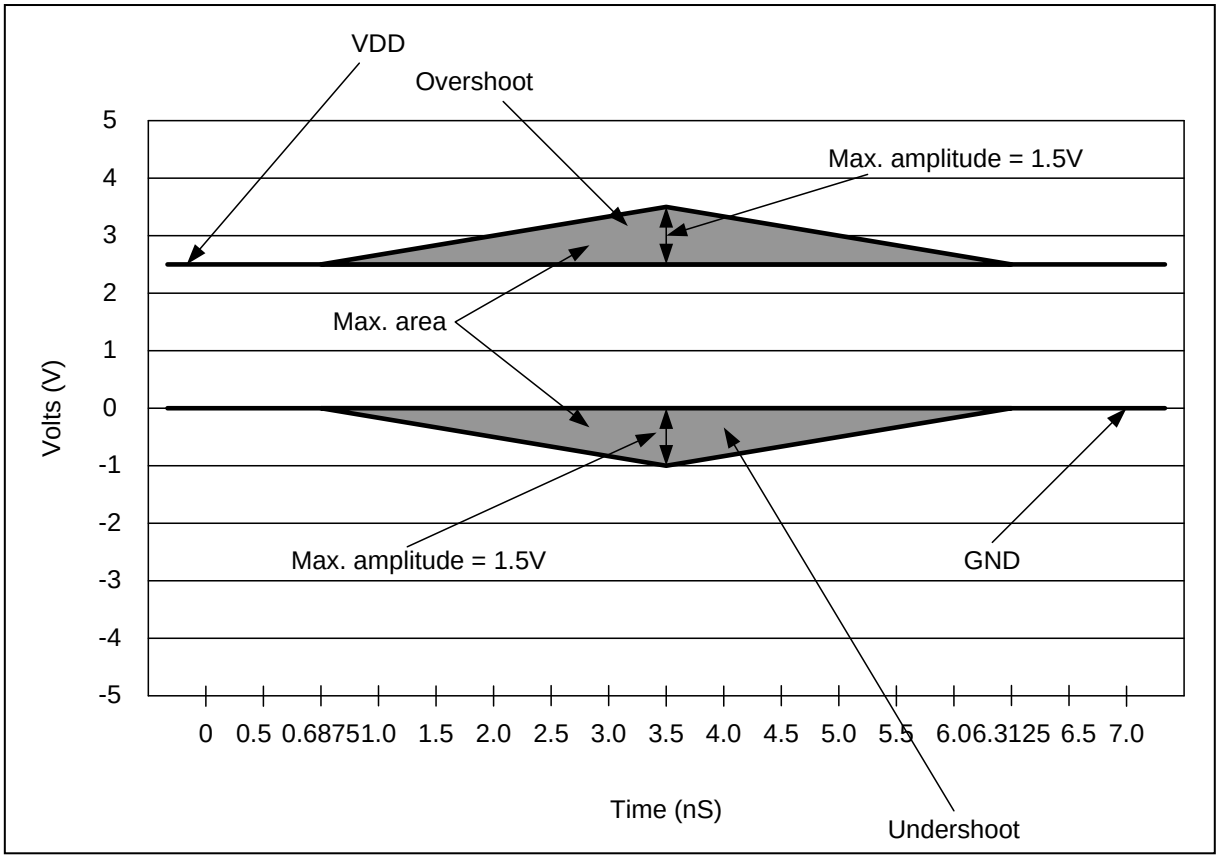



**Figure 3: Address and Control AC Overshoot and Undershoot Definition**



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## 10.8 Table 8: Overshoot/Undershoot Specification for Data, Strobe, and Mask Pins

| PARAMETER | SPECIFICATION | |
|---|---|---|
| | DDR500 | DDR400 |
| Maximum peak amplitude allowed for overshoot | 1.2 V | 1.2 V |
| Maximum peak amplitude allowed for undershoot | 1.2 V | 1.2 V |
| The area between the overshoot signal and VDD must be less than or equal to Max. area in Figure 4 | 2.4 V-nS | 2.4 V-nS |
| The area between the undershoot signal and GND must be less than or equal to Max. area in Figure 4 | 2.4 V-nS | 2.4 V-nS |

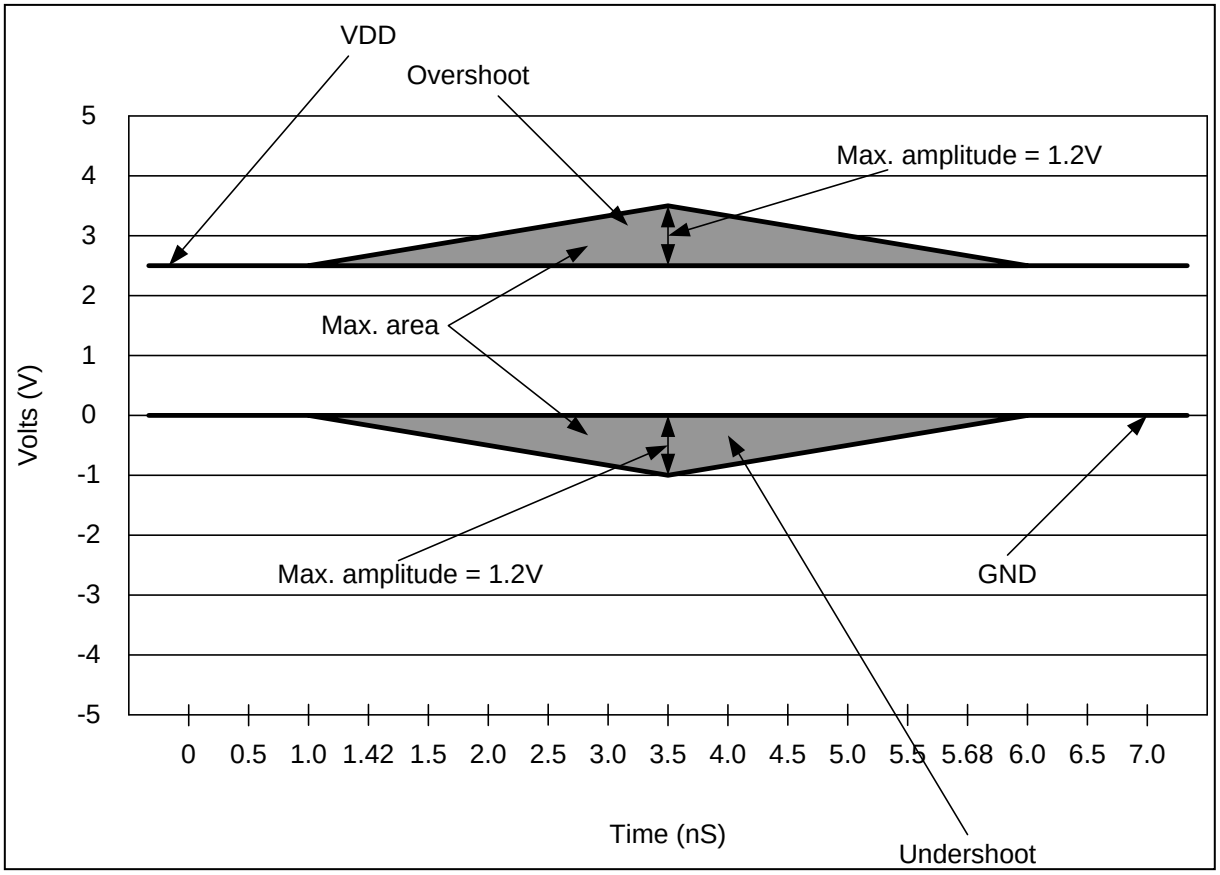



**Figure 4: DQ/DM/DQS AC Overshoot and Undershoot Definition**



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## 10.9 System Notes:

a. Pullup slew rate is characterized under the test conditions as shown in Figure 1.

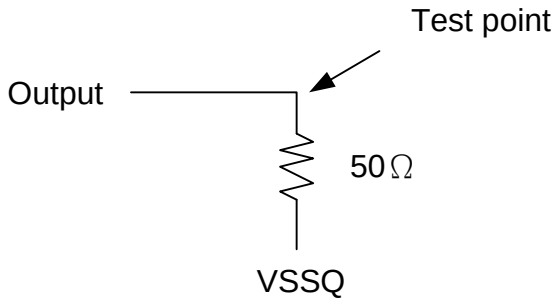



Figure 1: Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 2.

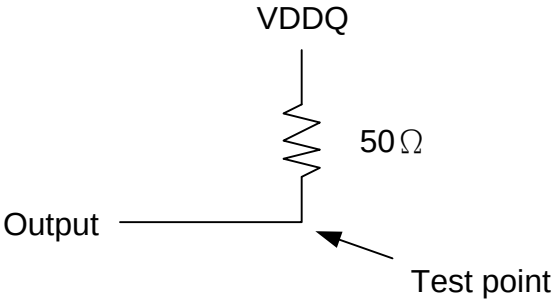



Figure 2: Pulldown slew rate test load

c. Pullup slew rate is measured between ($V_{DDQ}$/2 - 320 mV ± 250 mV)

Pulldown slew rate is measured between ($V_{DDQ}$/2 + 320 mV ± 250 mV)

Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example: For typical slew rate, DQ0 is switching

For minimum slew rate, all DQ bits are switching worst case pattern

For maximum slew rate, only one DQ is switching from either high to low, or low to high

The remaining DQ bits remain the same as for previous state

d. Evaluation conditions

| | |
|---|---|
| Typical: | 25°C (T Ambient), $V_{DDQ}$ = nominal, typical process |
| Minimum: | 70°C (T Ambient), $V_{DDQ}$ = minimum, slow-slow process |
| Maximum: | 0°C (T Ambient), $V_{DDQ}$ = maximum, fast-fast process |



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e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOP II package devices only.

h. Only intended for operation up to 266 Mbps per pin.

i. A derating factor will be used to increase $t_{IS}$ and $t_{IH}$ in the case where the input slew rate is below 0.5 V/nS as shown in Table 2. The Input slew rate is based on the lesser of the slew rates determined by either $V_{IH(AC)}$ to $V_{IL(AC)}$ or $V_{IH(DC)}$ to $V_{IL(DC)}$, similarly for rising transitions.

j. A derating factor will be used to increase $t_{DS}$ and $t_{DH}$ in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH(AC)}$ to $V_{IL(AC)}$ or $V_{IH(DC)}$ to $V_{IL(DC)}$, similarly for rising transitions.

The delta rise/fall rate is calculated as:

{1/(Slew Rate1)}-{1/(slew Rate2)}

For example: If Slew Rate 1 is 0.5 V/nS and Slew Rate 2 is 0.4 V/nS, then the delta rise, fall rate is

-0.5 nS/V. Using the table given, this would result in the need for an increase in $t_{DS}$ and $t_{DH}$ of 100 pS.

k. Table 3 is used to increase $t_{DS}$ and $t_{DH}$ in the case where the I/O slew rate is below 0.5 V/nS. The I/O slew rate is based on the lesser of the AC-AC slew rate and the DC-DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either $V_{IH(AC)}$ to $V_{IL(AC)}$ or $V_{IH(DC)}$ to $V_{IL(DC)}$, and similarly for rising transitions.

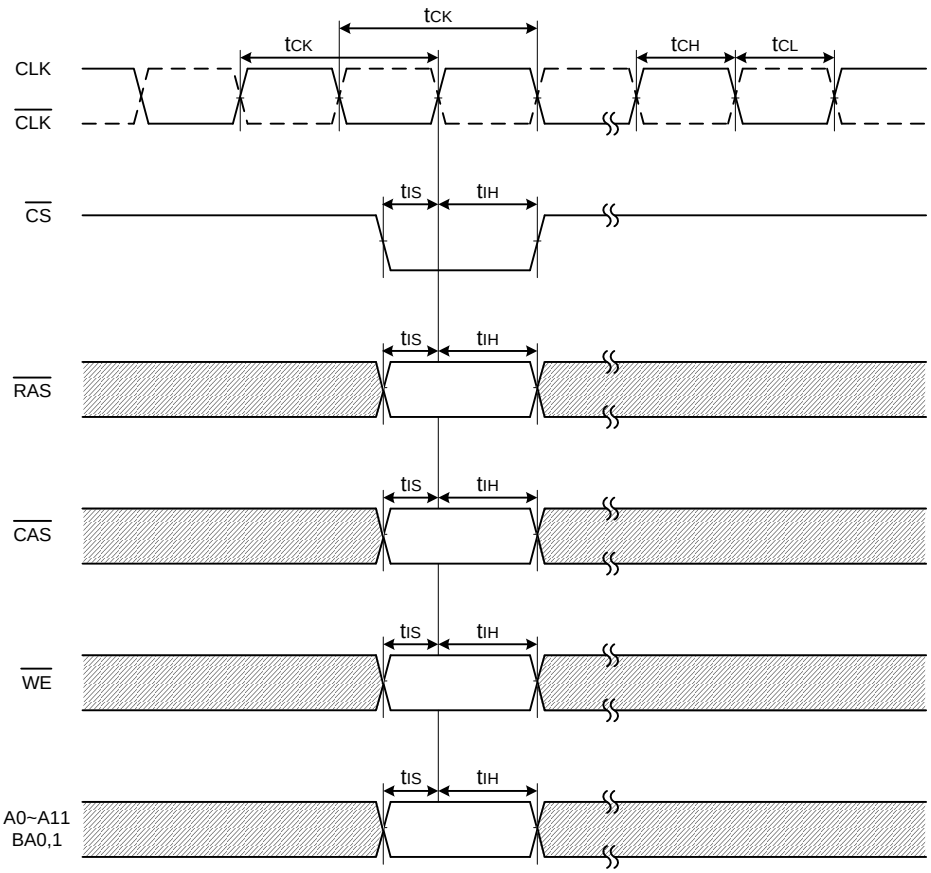
m. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.



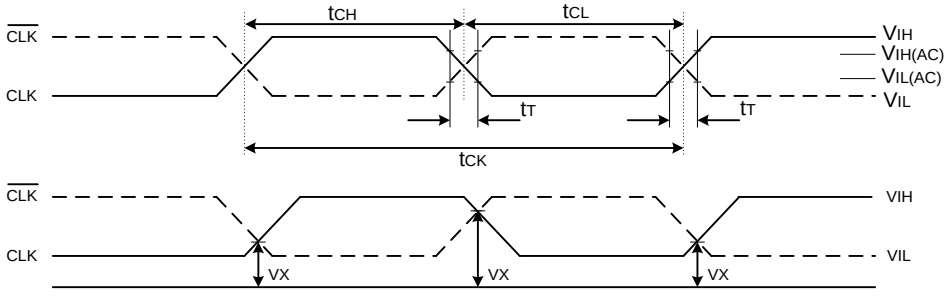
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# 11. TIMING WAVEFORMS

## 11.1 Command Input Timing



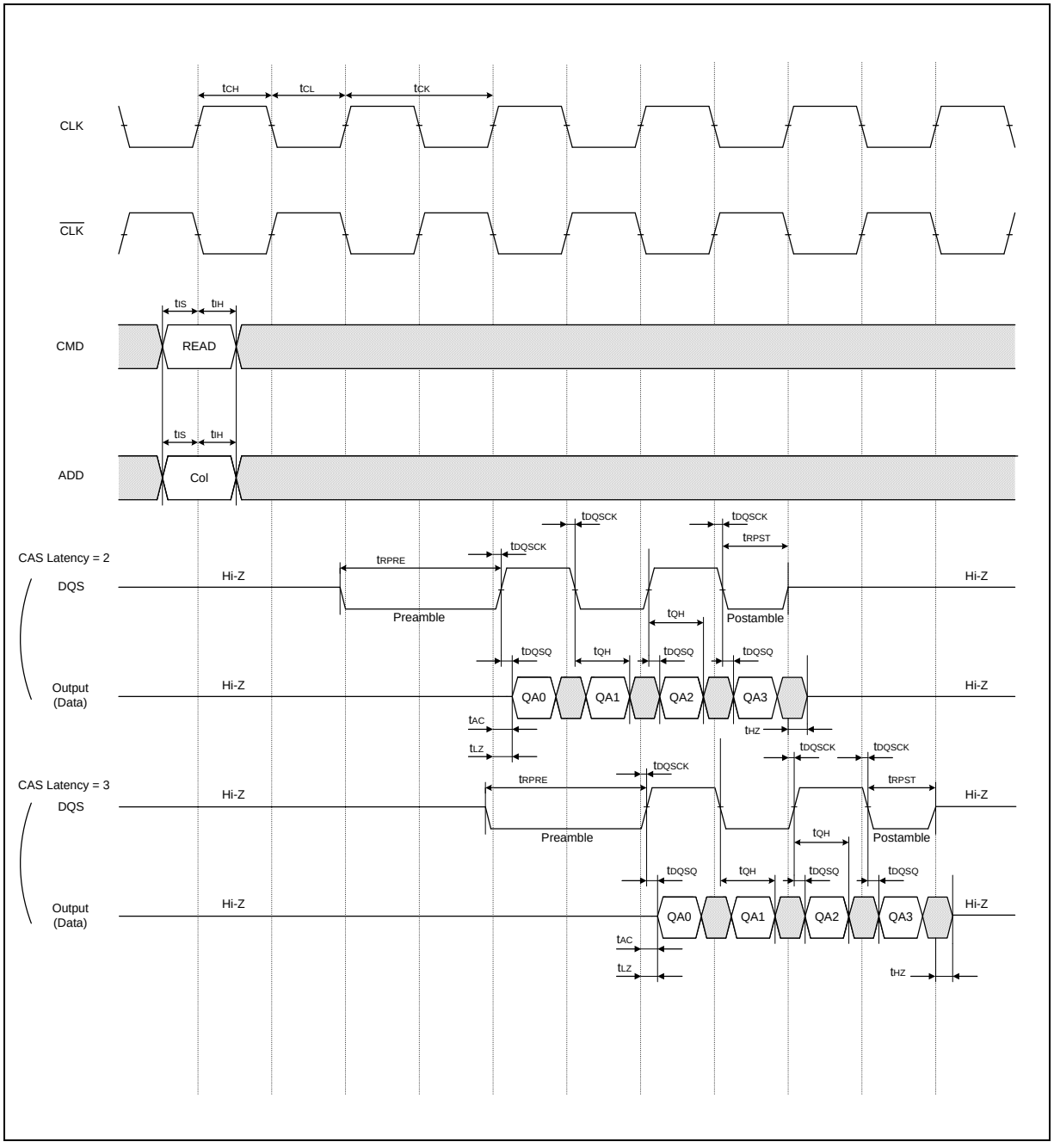

## 11.2 Timing of the CLK Signals






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## 11.3 Read Timing (Burst Length = 4)



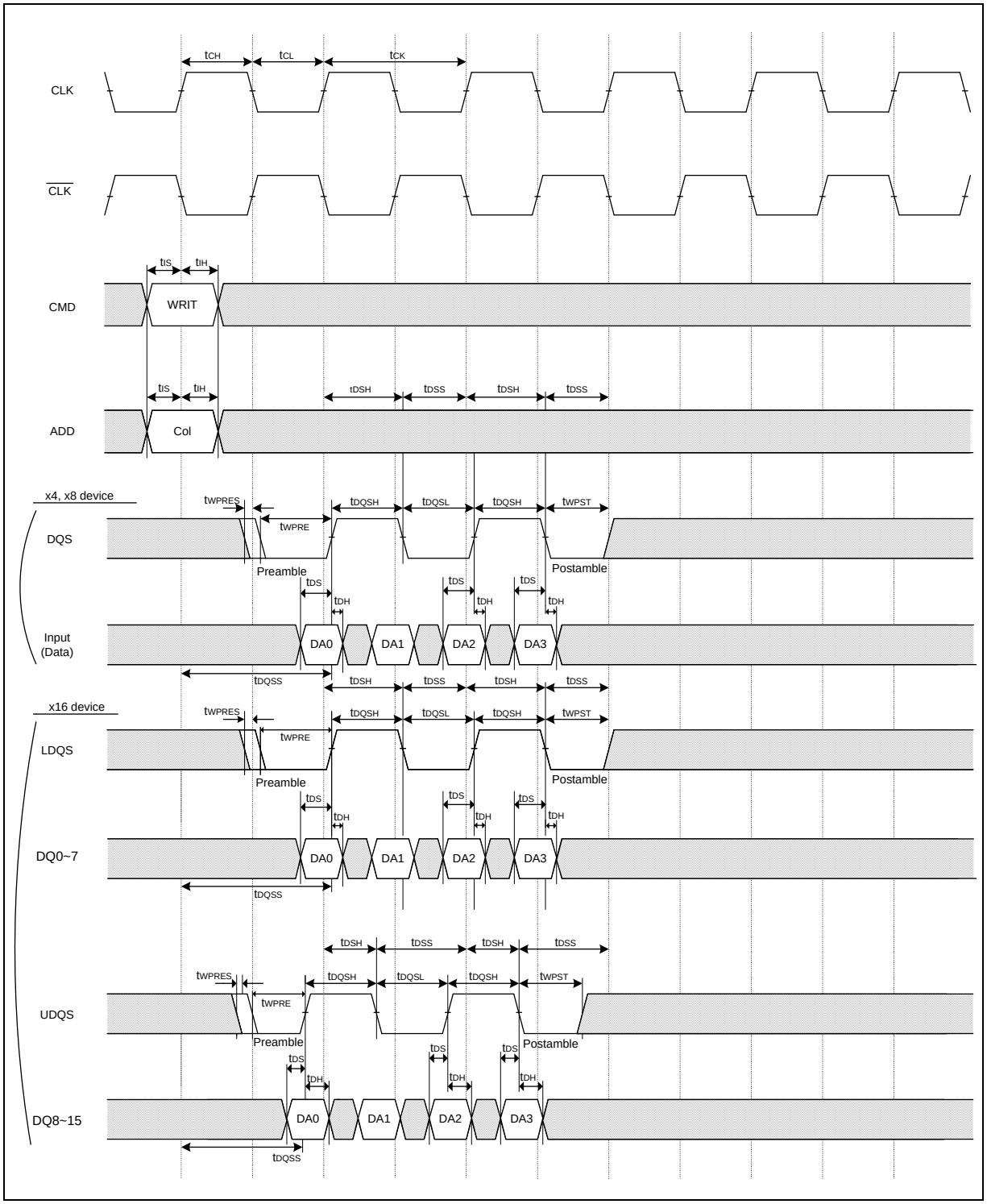

**Notes**: The correspondence of LDQS, UDQS to DQ. (W9464G6JH)

| | |
|---|---|
| LDQS | DQ0~7 |
| UDQS | DQ8~15 |



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## 11.4 Write Timing (Burst Length = 4)

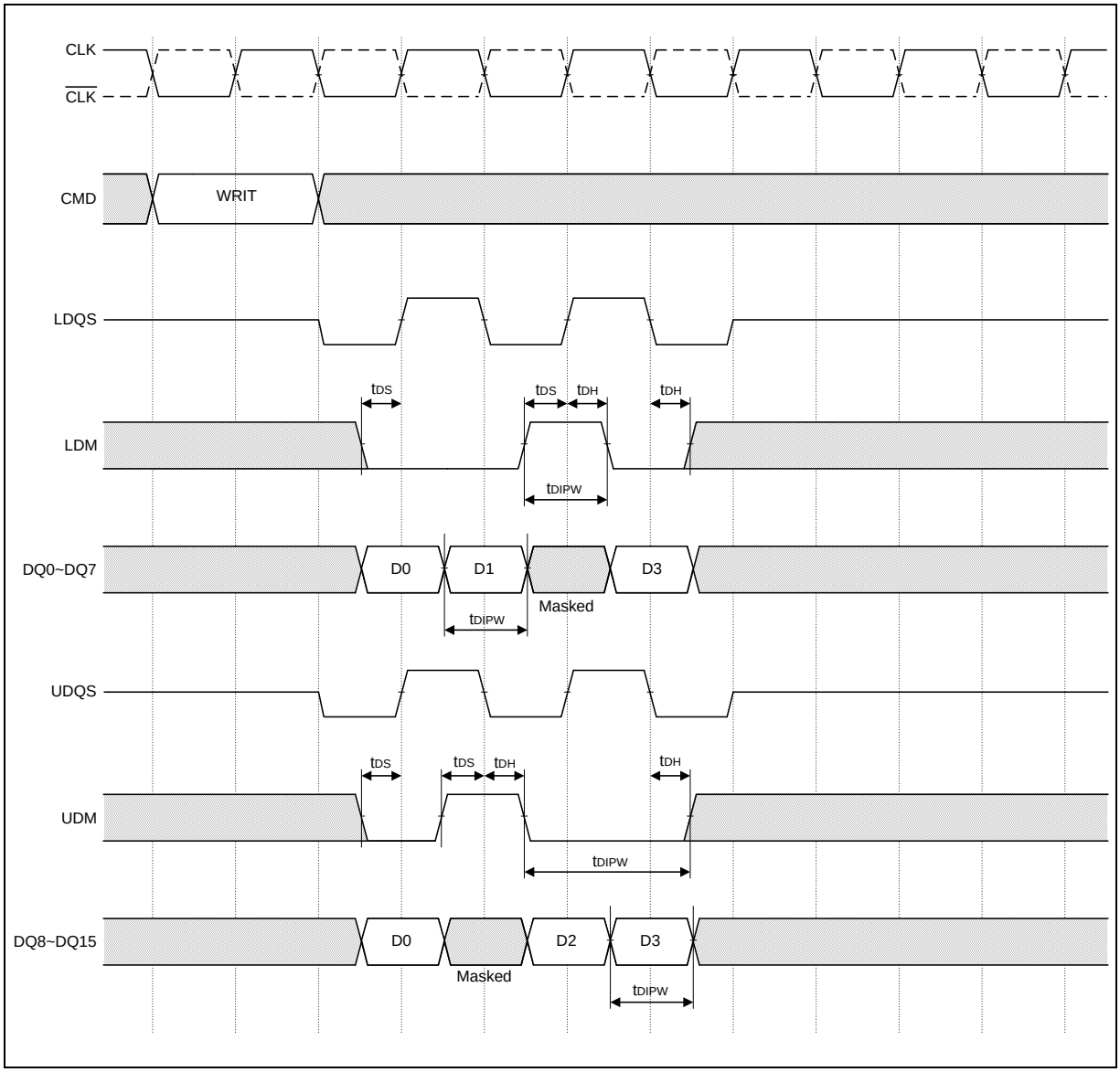



**Note:** x16 has two DQSs (UDQS for upper byte and LDQS for lower byte). Even if one of the 2 bytes is not used, both UDQS and LDQS must be toggled.



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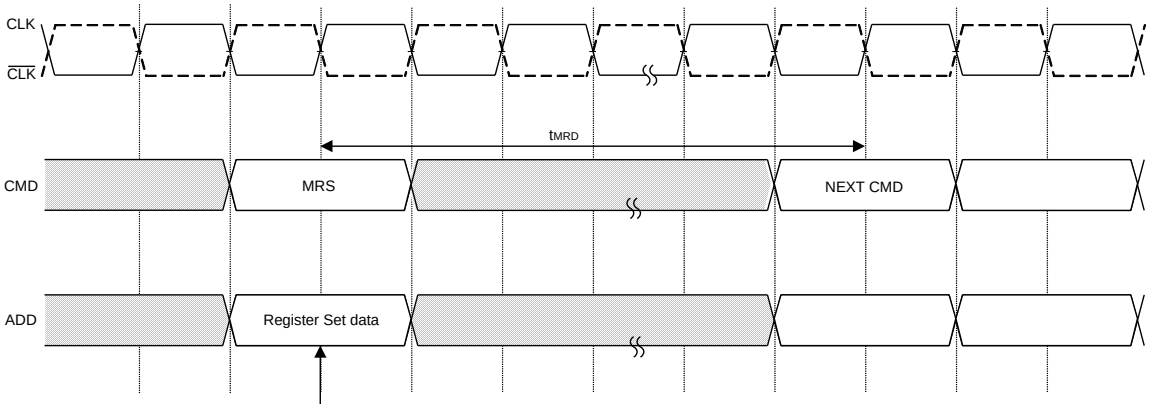
## 11.5 DM, DATA MASK (W9464G6JH)






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## 11.6 Mode Register Set (MRS) Timing




| | | |
|---|---|---|
| A0 | Burst Length | |
| A1 | | |
| A2 | | |
| A3 | Addressing Mode | |
| A4 | CAS Latency | |
| A5 | | |
| A6 | | |
| A7 | "0" | Reserved |
| A8 | DLL Reset | |
| A9 | "0" | Reserved |
| A10 | "0" | |
| A11 | "0" | |
| BA0 | "0" | Mode Register Set or Extended Mode Register Set |
| BA1 | "0" | |

* "Reserved" should stay "0" during MRS cycle.

| | | | Burst Length | |
|---|---|---|---|---|
| A2 | A1 | A0 | Sequential | Interleaved |
| 0 | 0 | 0 | Reserved | Reserved |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

| A3 | Addressing Mode |
|---|---|
| 0 | Sequential |
| 1 | Interleaved |

| A6 | A5 | A4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | 2.5 |
| 1 | 1 | 1 | Reserved |

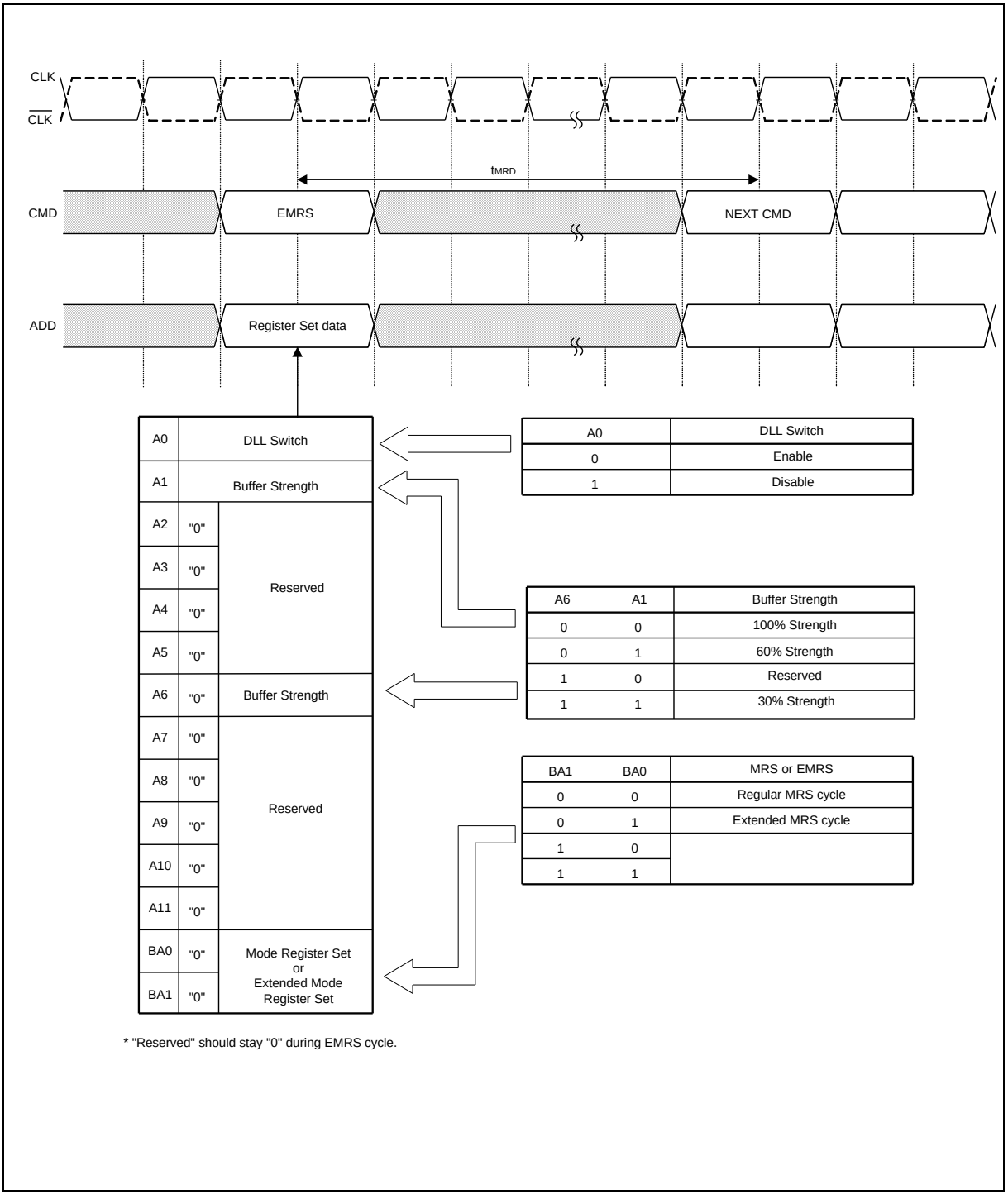
| A8 | DLL Reset |
|---|---|
| 0 | No |
| 1 | Yes |

| BA1 | BA0 | MRS or EMRS |
|---|---|---|
| 0 | 0 | Regular MRS cycle |
| 0 | 1 | Extended MRS cycle |
| 1 | 0 | Reserved |
| 1 | 1 | |



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## 11.7 Extend Mode Register Set (EMRS) Timing



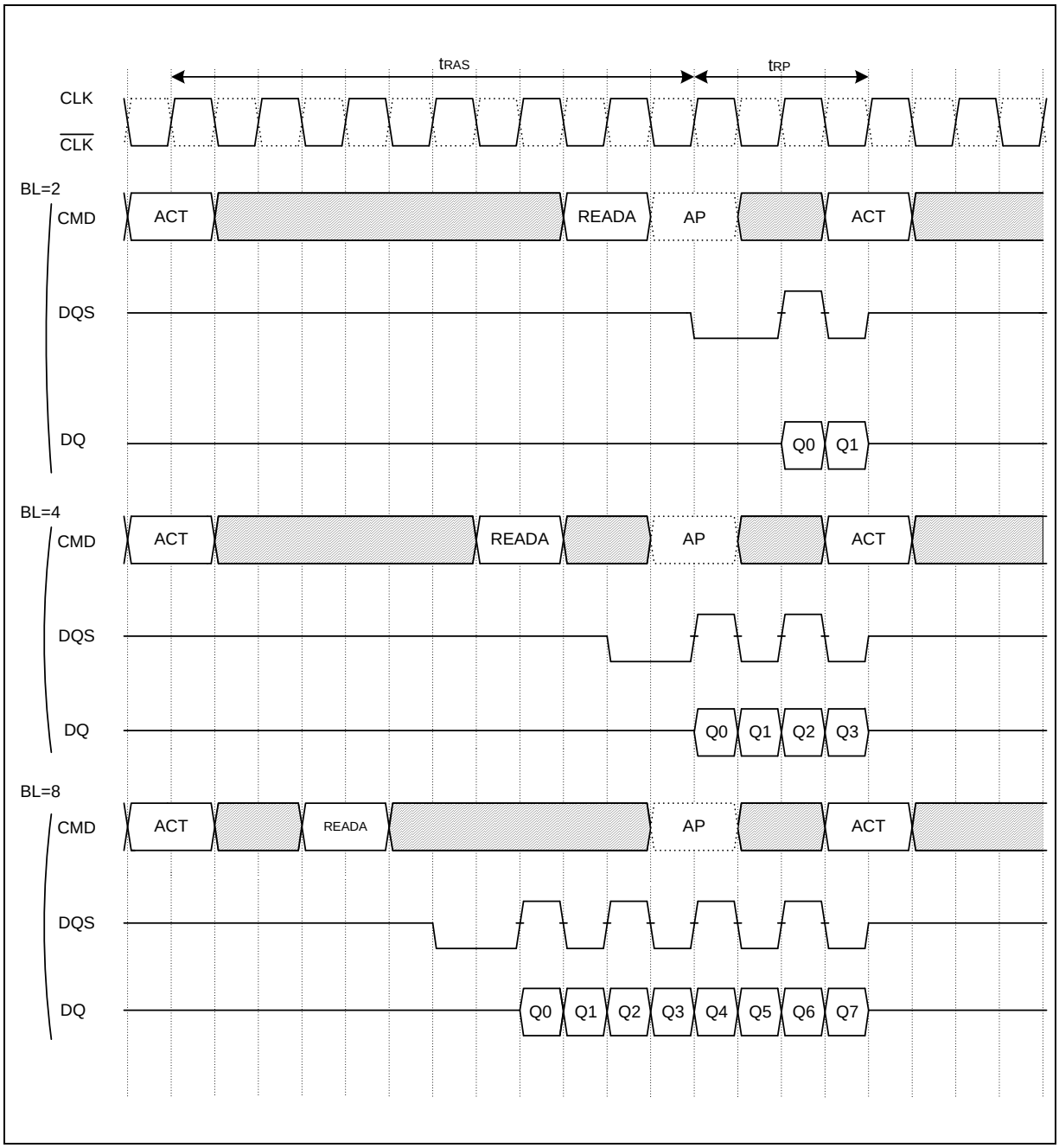

* "Reserved" should stay "0" during EMRS cycle.



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## 11.8 Auto-precharge Timing (Read Cycle, CL = 2)

1. $t_{RCD}$ (READA) ≥ $t_{RAS}$ (min) – (BL/2) × $t_{CK}$




**Notes:** CL=2 shown; same command operation timing with CL = 2,5 and CL=3

In this case, the internal precharge operation begin after BL/2 cycle from READA command.

AP Represents the start of internal precharging.

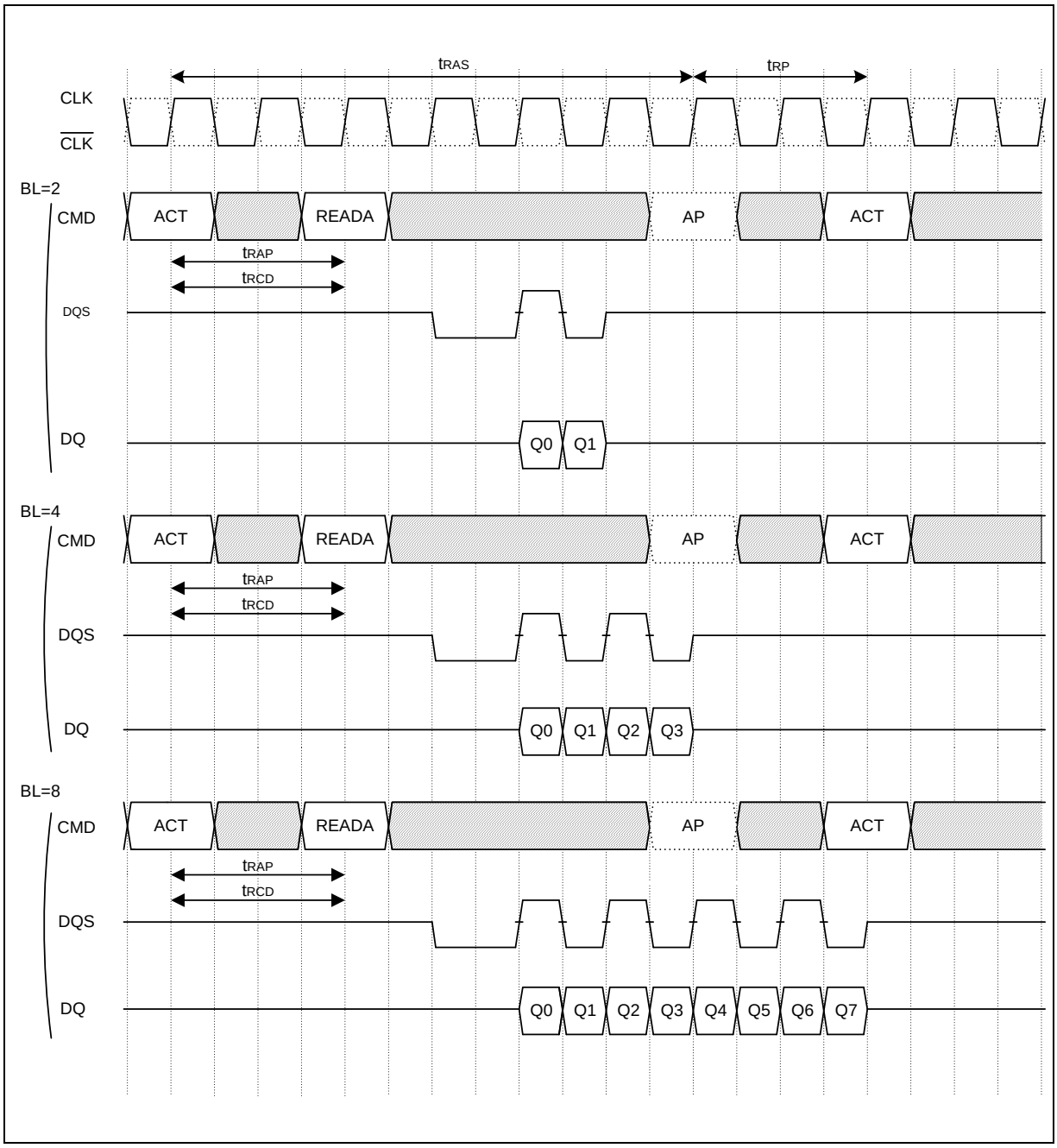
The Read with Auto-precharge command cannot be interrupted by any other command.



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## 11.9 Auto-precharge Timing (Read cycle, CL = 2), continued

2. $t_{RCD/RAP(min)} \leq t_{RCD}$ (READA) $< t_{RAS\ (min)} - (BL/2) \times t_{CK}$




**Notes:** CL2 shown; same command operation timing with CL = 2.5, CL=3.

In this case, the internal precharge operation does not begin until after $t_{RAS}$(min) has command.

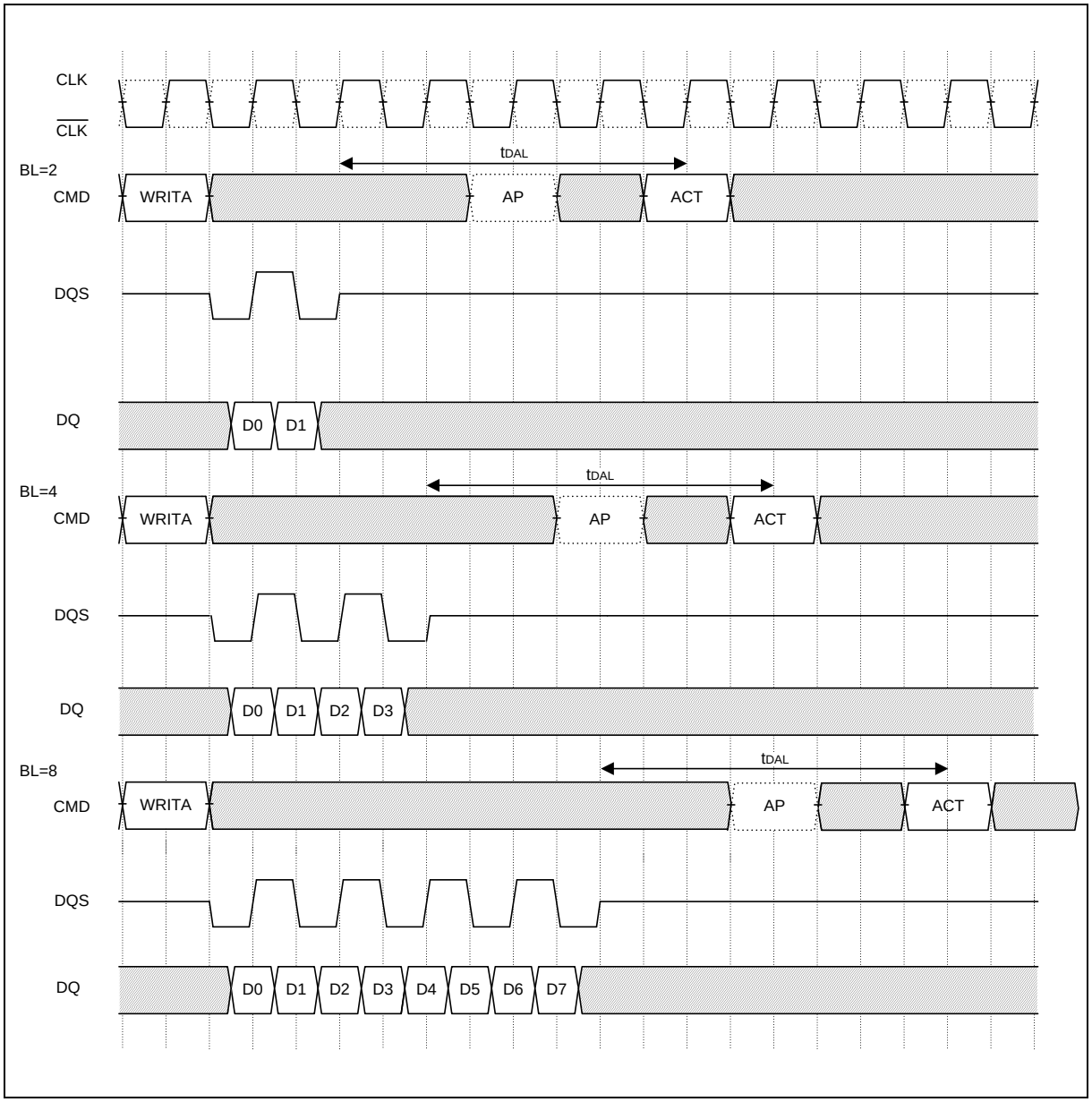
AP Represents the start of internal precharging.

The Read with Auto-precharge command cannot be interrupted by any other command.



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## 11.10 Auto-precharge Timing (Write Cycle)



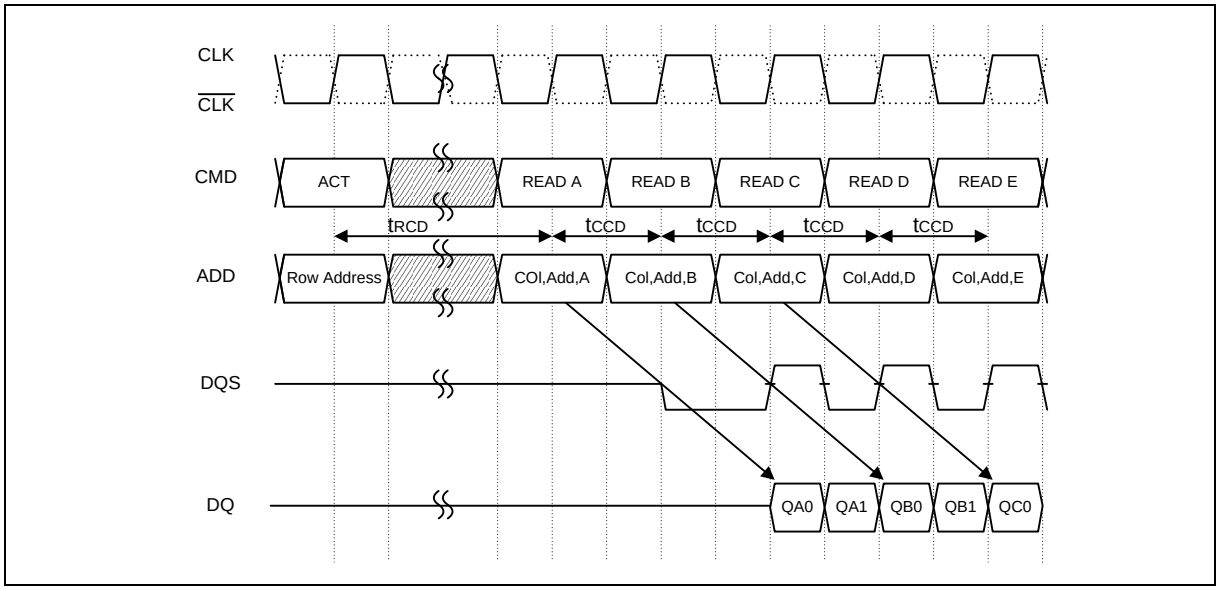

The Write with Auto-precharge command cannot be interrupted by any other command.

AP Represents the start of internal precharging.

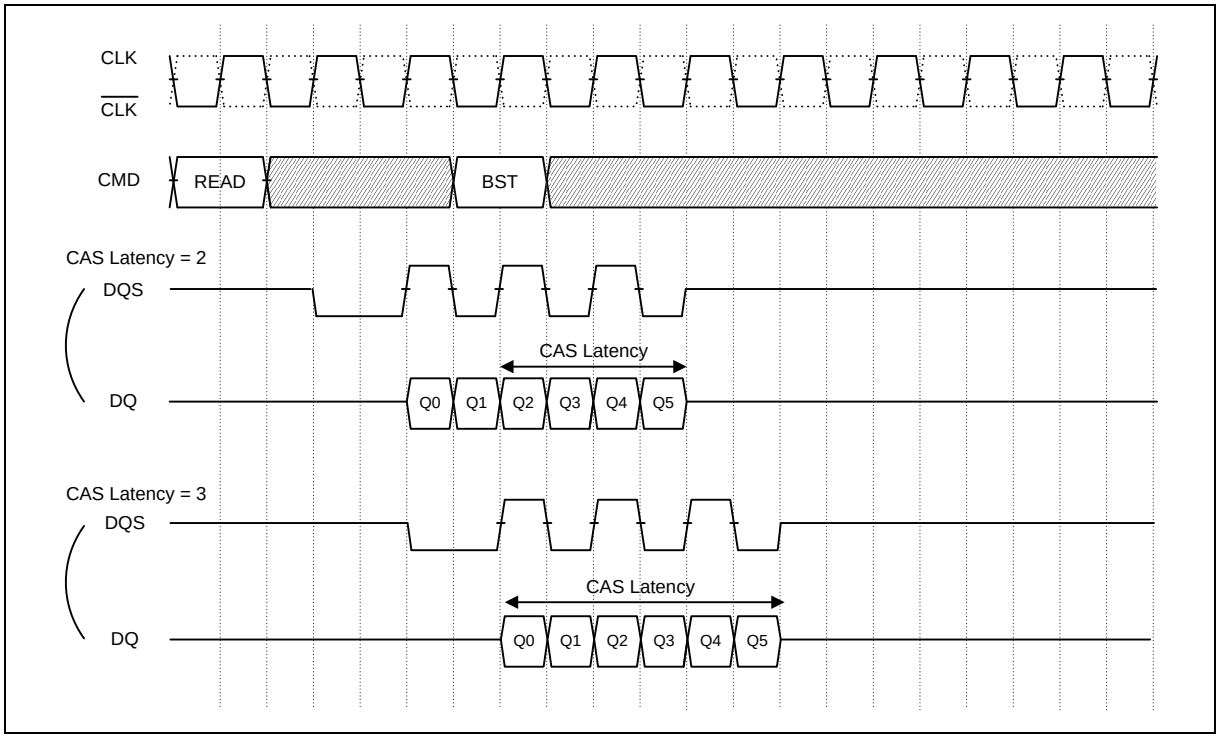


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## 11.11 Read Interrupted by Read (CL = 2, BL = 2, 4, 8)



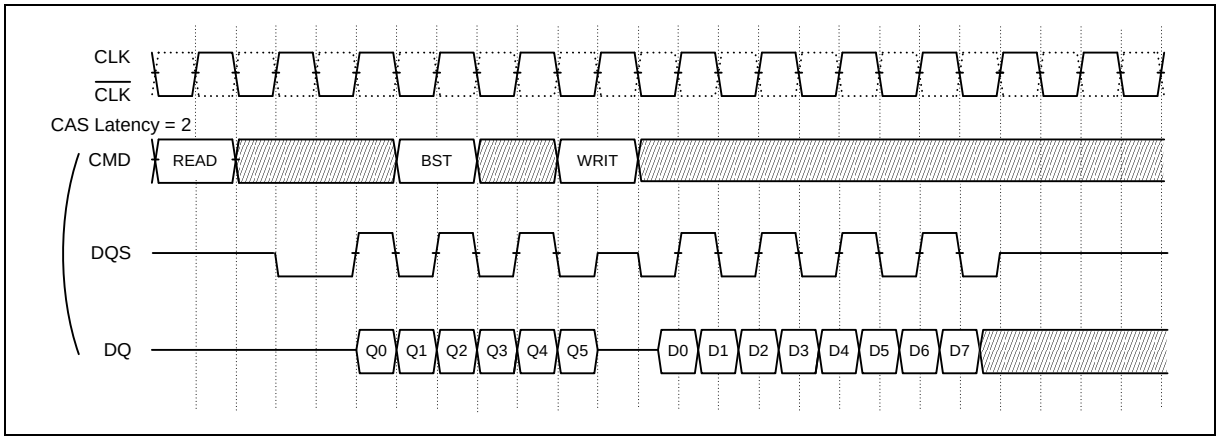

## 11.12 Burst Read Stop (BL = 8)





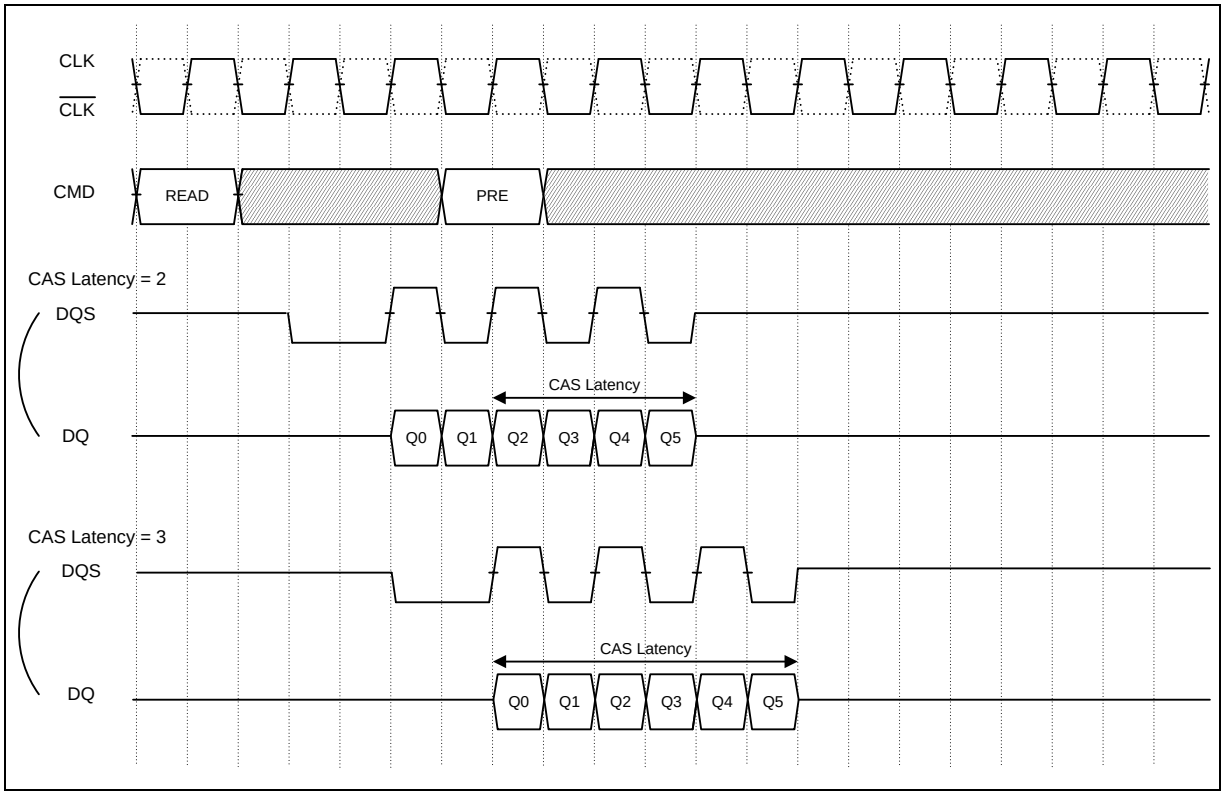

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## 11.13 Read Interrupted by Write & BST (BL = 8)




Burst Read cycle must be terminated by BST Command to avoid I/O conflict.

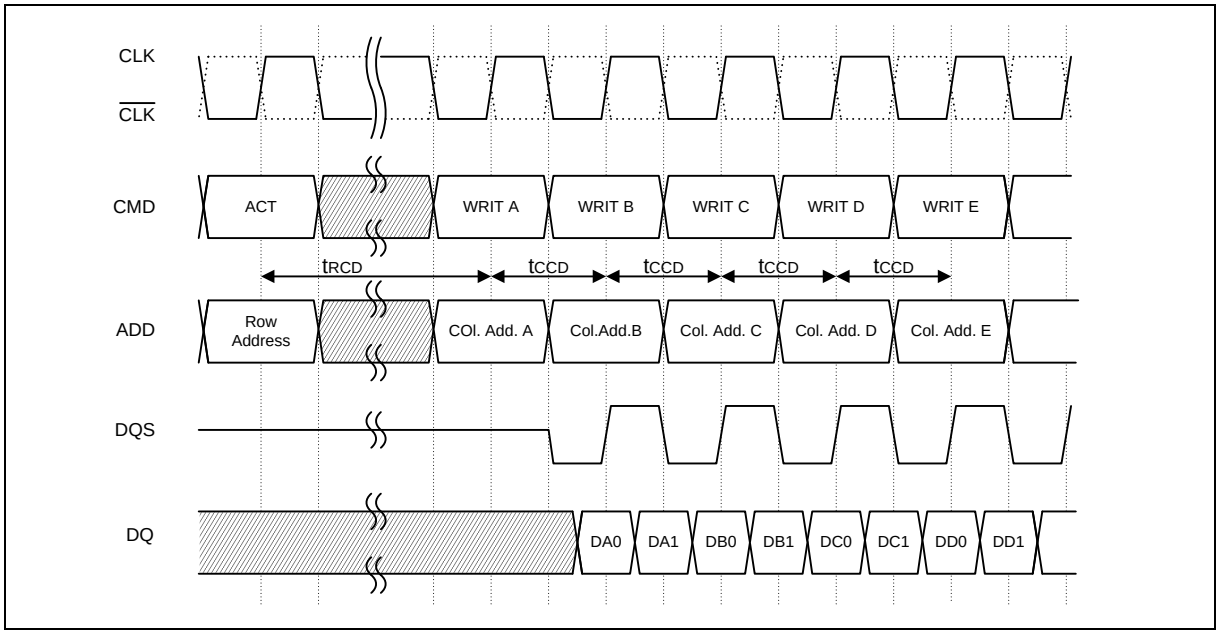
## 11.14 Read Interrupted by Precharge (BL = 8)



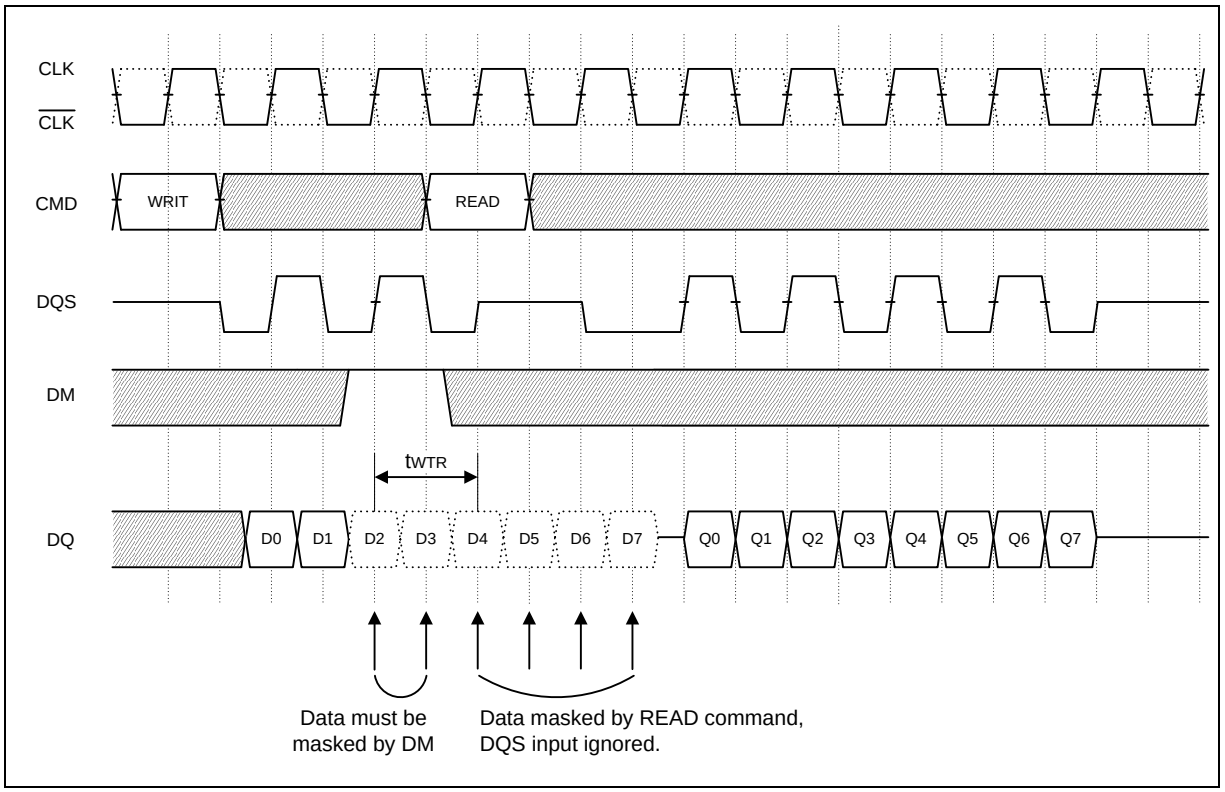



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## 11.15 Write Interrupted by Write (BL = 2, 4, 8)



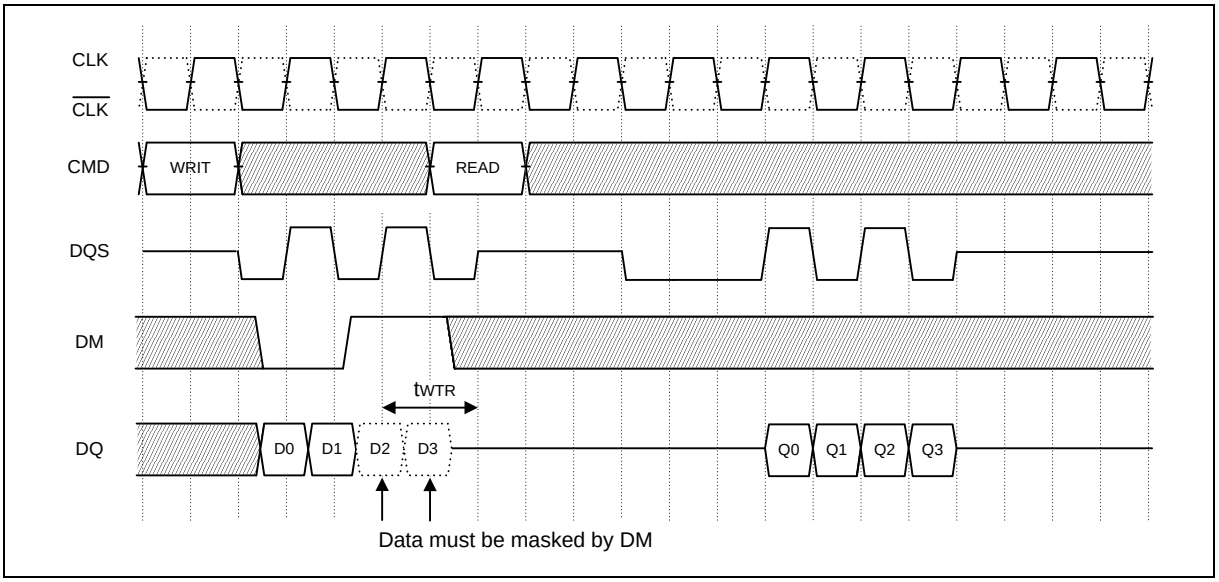

## 11.16 Write Interrupted by Read (CL = 2, BL = 8)



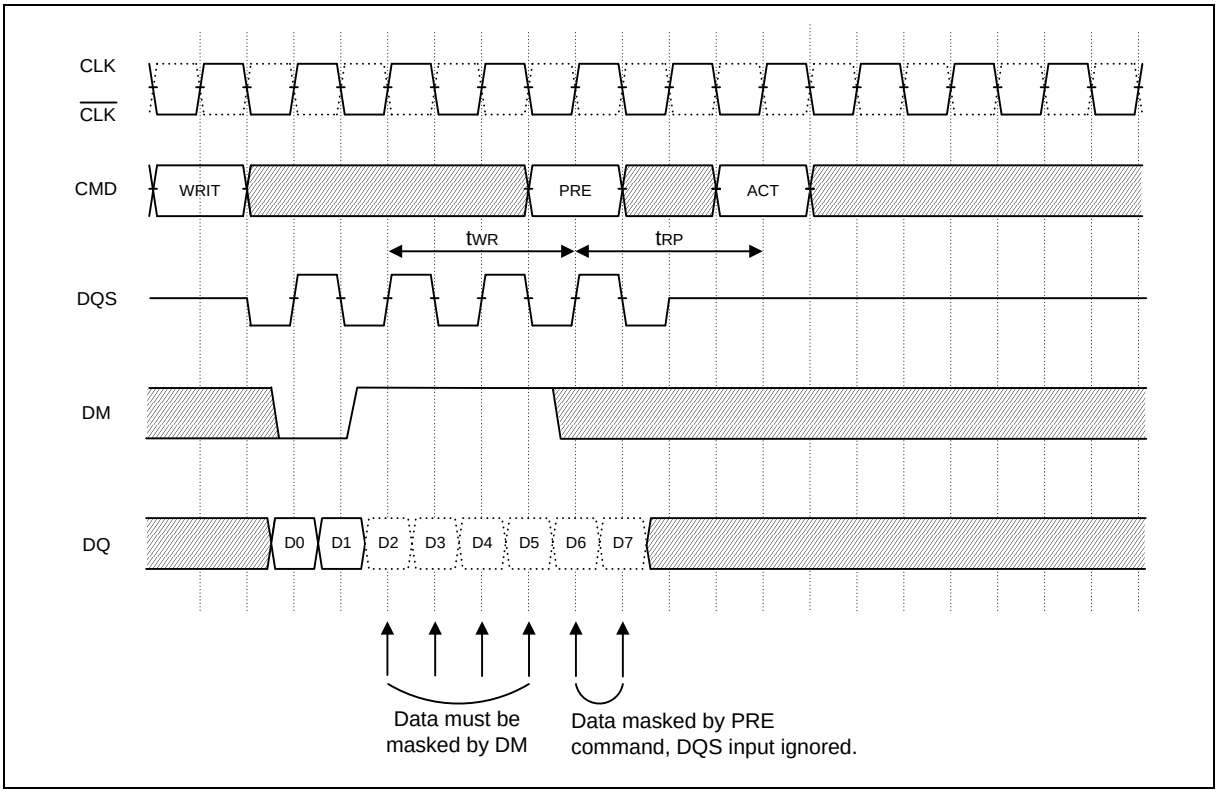



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## 11.17 Write Interrupted by Read (CL = 3, BL = 4)



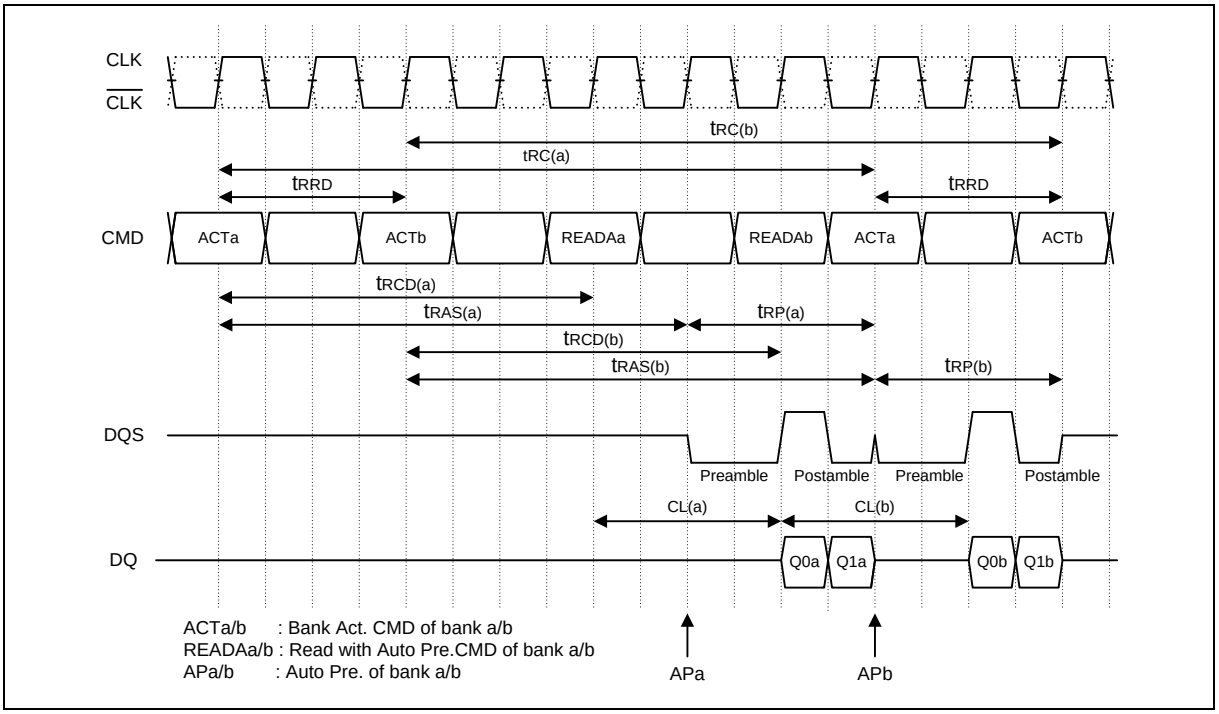

## 11.18 Write Interrupted by Precharge (BL = 8)



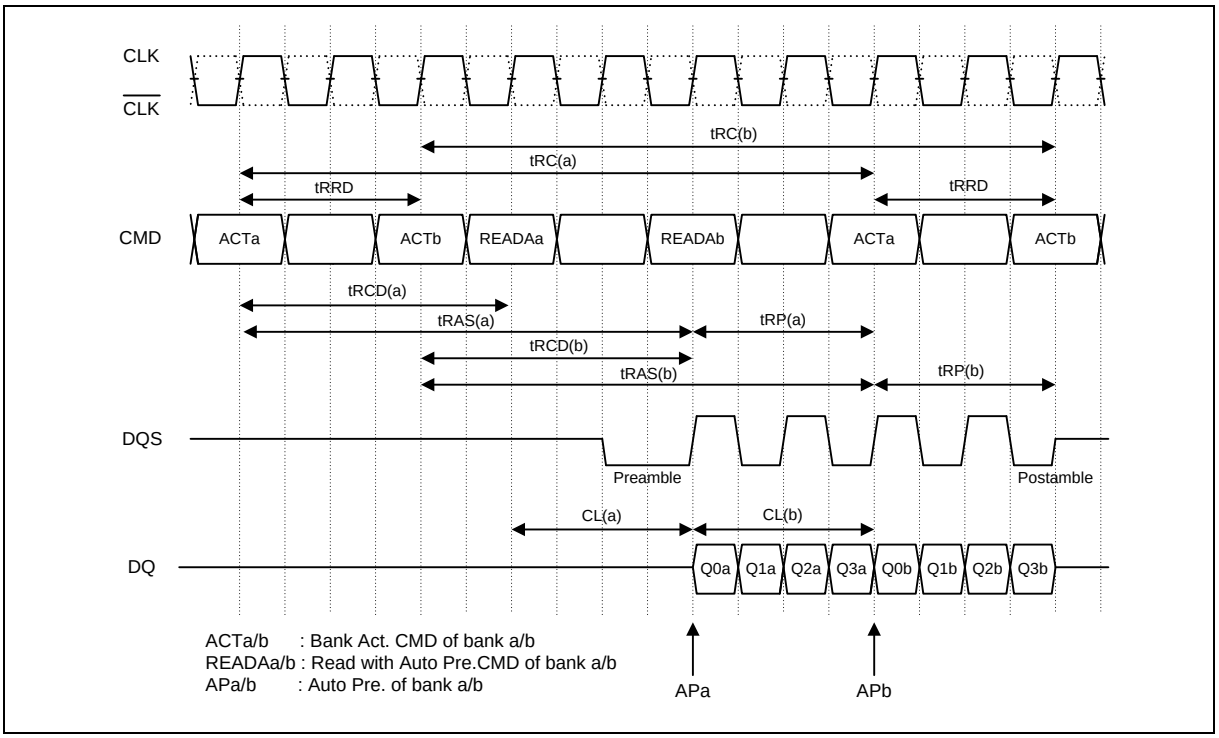



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## 11.19 2 Bank Interleave Read Operation (CL = 2, BL = 2)



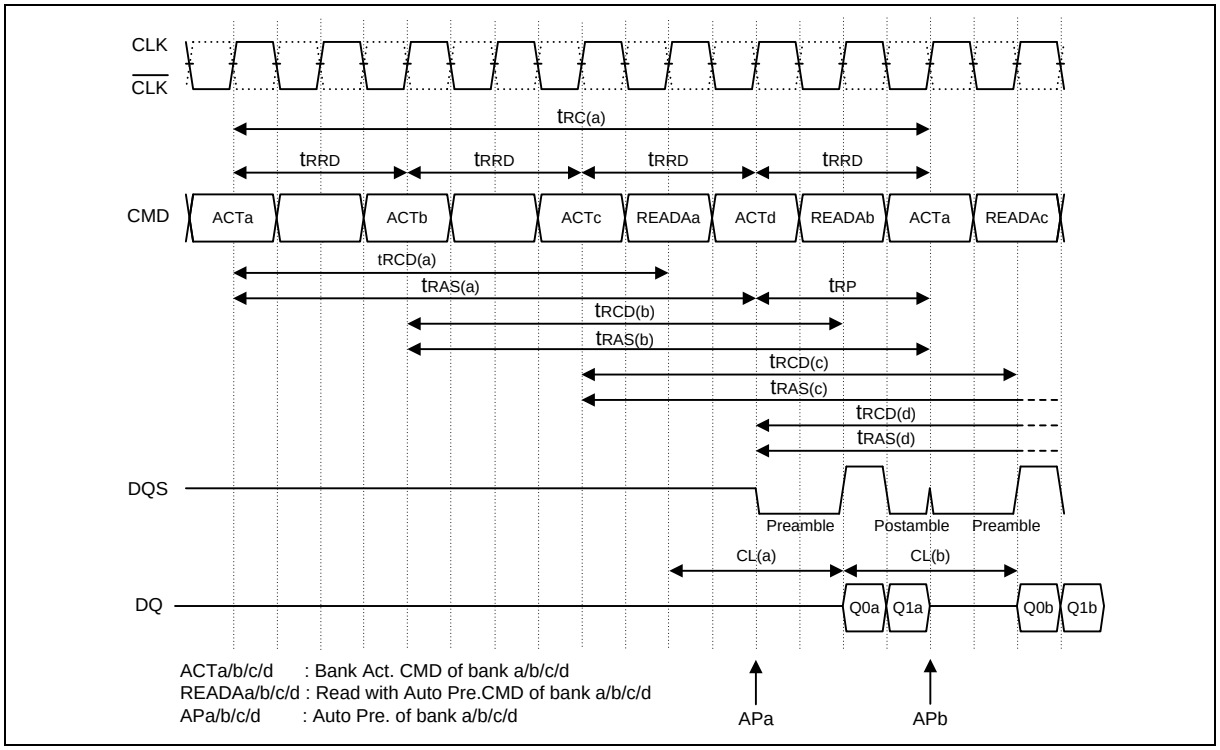

## 11.20 2 Bank Interleave Read Operation (CL = 2, BL = 4)



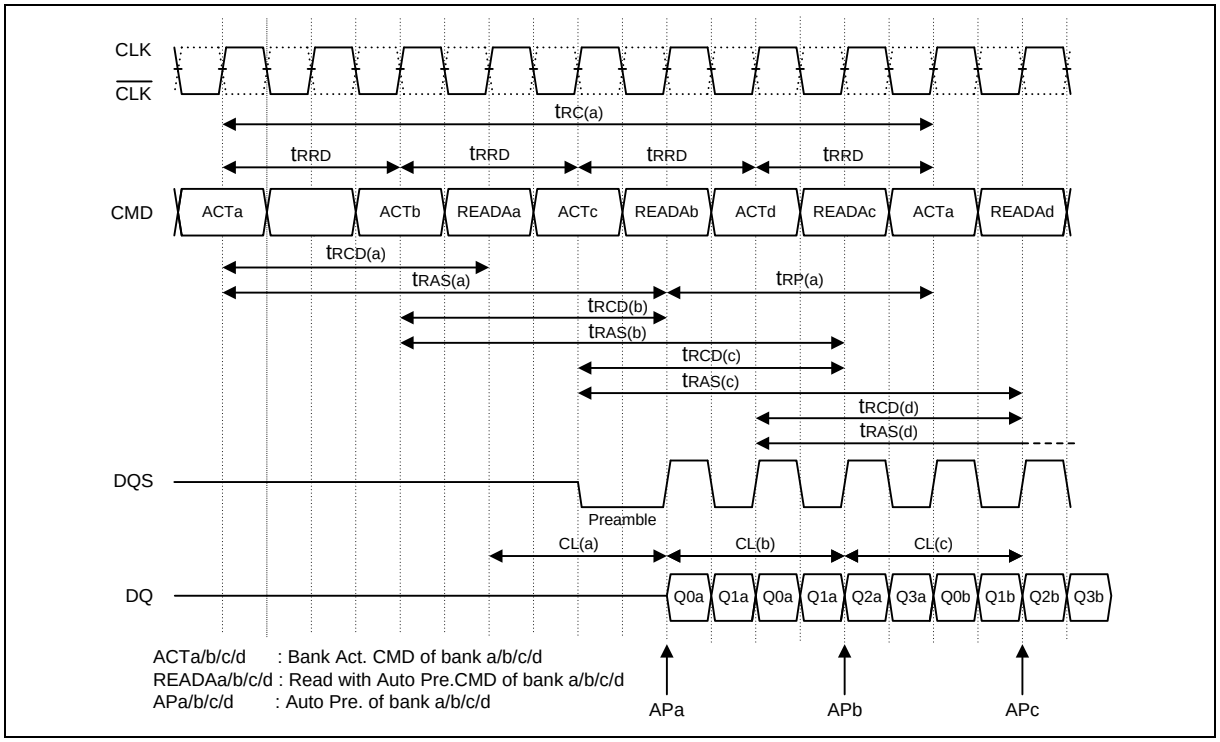



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## 11.21 4 Bank Interleave Read Operation (CL = 2, BL = 2)



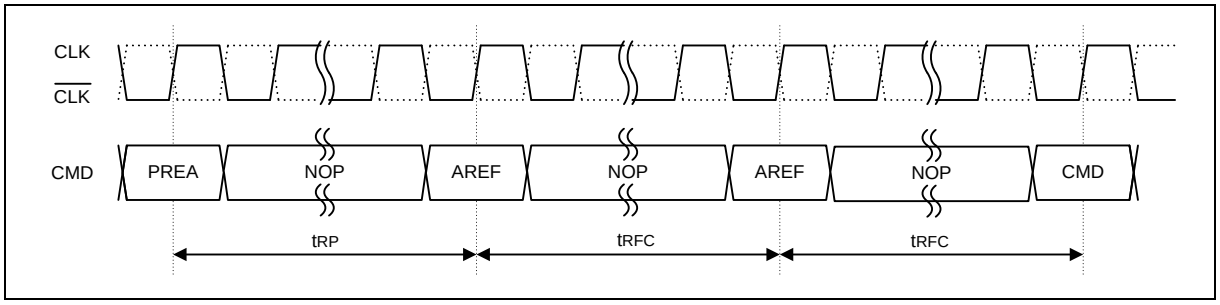

## 11.22 4 Bank Interleave Read Operation (CL = 2, BL = 4)





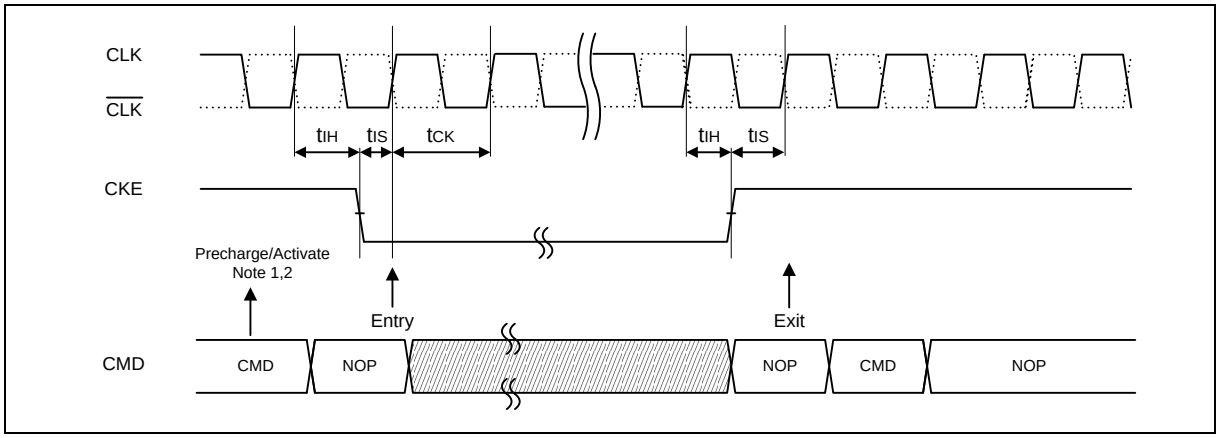

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## 11.23 Auto Refresh Cycle




**Note:** CKE has to be kept "High" level for Auto-Refresh cycle.

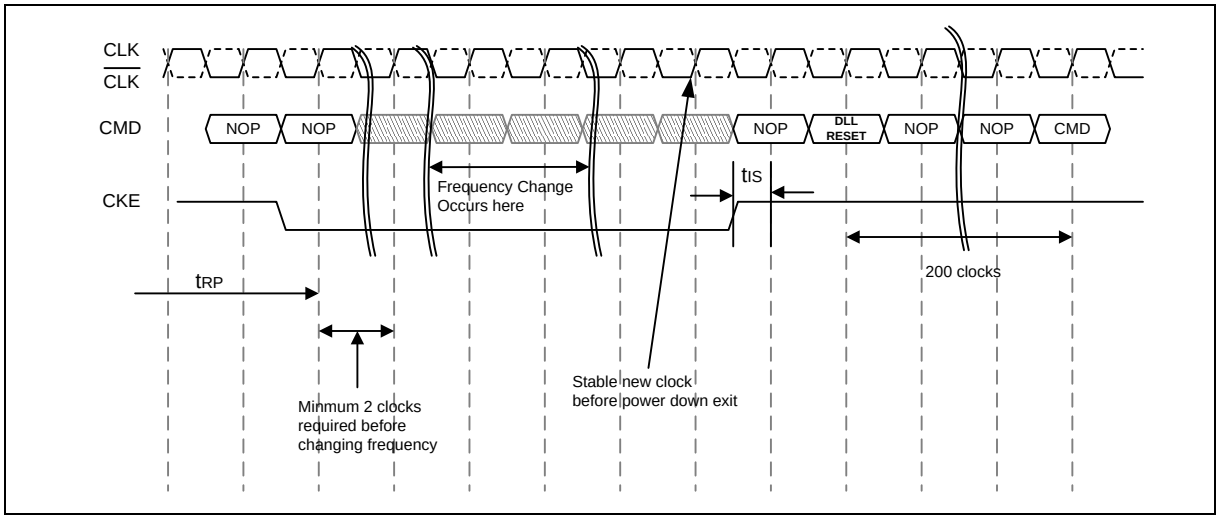
## 11.24 Precharge/Activate Power Down Mode Entry and Exit Timing




**Note:**

1. If power down occurs when all banks are idle, this mode is referred to as precharge power down.
2. If power down occurs when there is a row active in any bank, this mode is referred to as active power down.

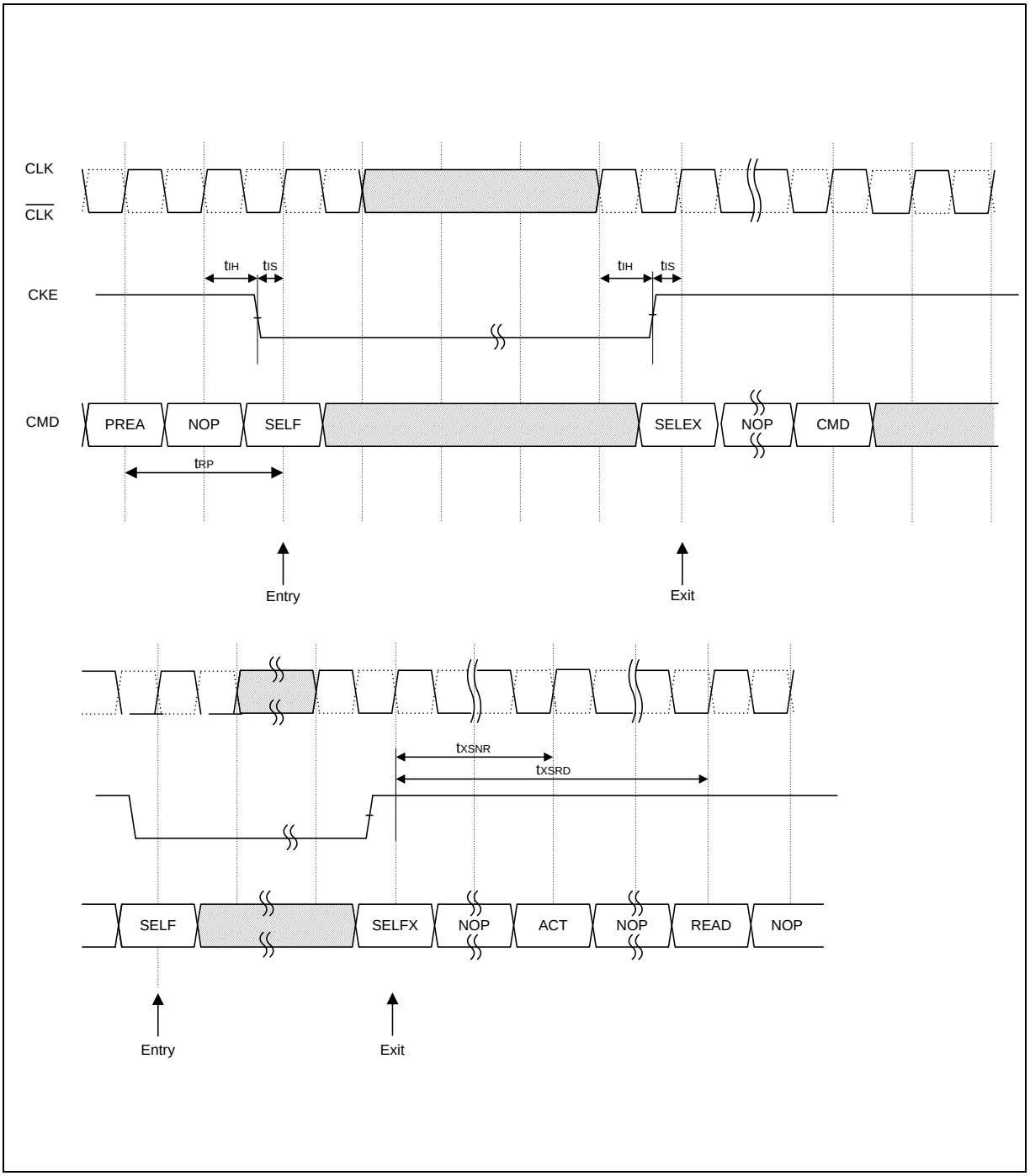
## 11.25 Input Clock Frequency Change during Precharge Power Down Mode Timing






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## 11.26 Self Refresh Entry and Exit Timing




**Note:**

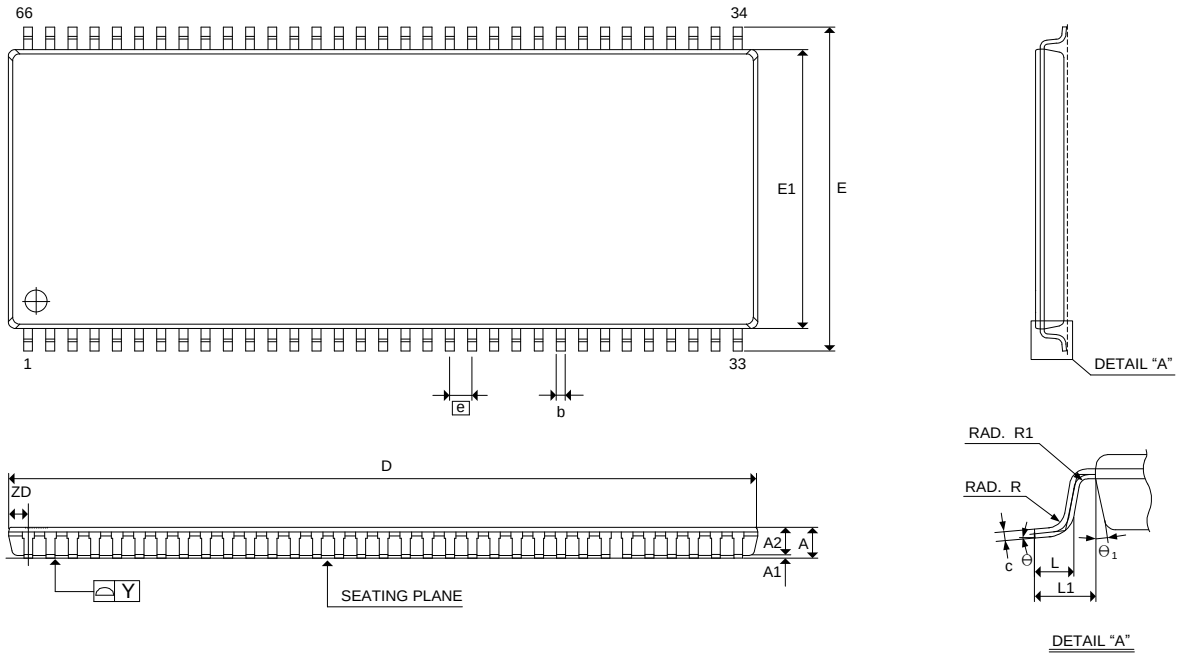
If the clock frequency is changed during self refresh mode, a DLL reset is required upon exit.



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## 12. PACKAGE SPECIFICATION

### 12.1 66L TSOP – 400 mil




Controlling Dimension : Millimeters

| SYMBOL | DIMENSION (mm) | | | DIMENSION (inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | --- | --- | 1.20 | --- | --- | 0.047 |
| A1 | 0.05 | --- | 0.15 | 0.002 | --- | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.22 | --- | 0.38 | 0.009 | --- | 0.015 |
| c | 0.12 | --- | 0.21 | 0.005 | --- | 0.008 |
| D | 22.09 | 22.22 | 22.35 | 0.870 | 0.875 | 0.880 |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| e | 0.65 BASIC | | | 0.026 BASIC | | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | 0.80 BASIC | | | 0.031 BASIC | | |
| R | 0.12 | --- | 0.25 | 0.005 | --- | 0.010 |
| R1 | 0.12 | --- | --- | 0.005 | --- | --- |
| ZD | 0.71 REF | | | 0.028 REF | | |
| Θ | 0° | --- | 8° | 0° | --- | 8° |
| $\Theta_1$ | 10° | --- | 20° | 10° | --- | 20° |
| Y | --- | --- | 0.10 | --- | --- | 0.004 |



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## 13. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A01 | Apr. 02, 2010 | All | Initial formally data sheet |
| A02 | Oct. 20, 2011 | 4, 5, 23, 25, 26 | Add -5I industrial grade parts |

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