winbond

spiflash®

TrustME®

W77Q32JW/W77Q16JW 1.8V 32M-BIT/16M-BIT Secure Serial NOR Flash Memory with Dual/Quad SPI, QPI & DTR

Datasheet

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1 ABOUT THIS DOCUMENT

1.1 Executive summary

This document describes Winbond's **TrustME®** ***W77Q32JW/W77Q16JW Secure Flash Memory***.

- Section 4 - Device Features
- Section 6 - Overview of device Security Functions and main concepts
- Section 7 - Standard Flash Instructions
- Section 8 - Standard Flash Registers
- Section 9 - Electrical Characteristics
- Section 10 - Pin Configurations
- Section 11 - Package Specifications

For further information regarding the device Security Functions, related Commands and Registers, refer to the [SA] document.

1.2 References Documents

A reference is made to the following related documents:

REFERENCE	DESCRIPTION
[SA]	W77Q32JW/W77Q16JW Secure Serial NOR Flash Memory Security Manual, Winbond

1.3 Notation

Throughout this document, two notations are used to describe numbers: Hexadecimal numbers and Byte Streams.

- **Hexadecimal numbers** are represented as Little Endians (LS-Byte is first):
  - 0x44332211 is a 32-bit number, with the LS-Byte (11h) being the first byte.
  - The Verilog notation {0x44, 0x33, 0x22, 0x11} is used to represent the same value.
- **Byte Streams** are read from left to right:
  - "11 22 33 44" is a stream of 4 Bytes, where the left-most byte (11h) is the first byte of the message.
  - Therefore: "0x665544332211" is equivalent to "11 22 33 44 55 66", with 11h being the first byte of the message.

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2 GENERAL DESCRIPTION

The W77Q32JW/W77Q16JW **TrustME®** Secure Serial Flash memory provides a secure storage solution for systems with limited space, pins, and power. The W77Q32JW/W77Q16JW is certified for **Common Criteria EAL2** and meets SESIP L2 security certification requirements. The W77Q32JW/W77Q16JW is **ASIL-C ready** for automotive applications.

The W77Q32JW/W77Q16JW is a **drop-in replacement** for standard Serial NOR Flash Memory devices, offering security, flexibility, and performance well beyond ordinary NOR Flash Memory devices. It is ideal for secure code storage with support for execute in place (XIP), cryptographic key distribution, management and storage, secure data storage, and general data storage.

The W77Q32JW/W77Q16JW features sophisticated cryptographic encryption of the communication channel, personalization of each device with unique keys, cryptographic read and write locks, protection of data integrity, secure firmware update, Root of Trust (RoT) functions, secure read, write and erase operations.

The W77Q32JW/W77Q16JW series supports Single, Dual, and Quad SPI as well as QPI modes of operation, running at up to 133 MHz. Dual Transfer Rate (DTR) is supported at rates of up to 66 MHz.

3 OUTSTANDING FEATURES

Single die secure solution

- ISO 15408 CC EAL2 certified
- Meets SESIP L2 security certification requirements with compliance to IEC62443-4-2 and NIST 8259A
- ISO 21434 automotive cybersecurity certification ready
- FIPS PUB 180-4 CAVP certified
- JEDEC JESD254 compliant
- Secure code and data storage
- Secure code update with rollback protection
- Ultra fast Secure Boot
- Firmware Integrity Protection
- Authenticated Watchdog Timer
- Secure & Unique Device ID
- Cryptographically-secured write-protection
- Local and remote secure channel, encrypted, authenticated, replay-protected
- Replay Protection Monotonic counter
- Platform Firmware Resiliency assurance (NIST SP 800-193)
- Secure Root of Trust (RoT) for IoT devices

Automotive Safety

- Meets ISO 26262 ASIL-C automotive safety requirements

Standard SPI-Flash drop-in replacement

- Highest Performance Secure Serial Flash
  - Execute in place (XIP)
  - 133 MHz SPI Single/Dual/Quad/QPI
  - 66 MHz Dual Transfer Rate (DTR) mode
- Flexible Architecture with 4kB Blocks
  - Uniform 4K-bytes granularity for Block Erase
  - Page Program up to 256 bytes per command
  - Erase/Program Suspend & Resume
- Low Power, single 1.8V power supply
- Wide Temperature Range
  - -40°C to +85°C (Industrial)
- Space efficient packaging
  - 8-pin SOIC 208-mil
  - 16-pin SOIC 300-mil
  - WSON8 6x5mm
  - 8-pad XSON 4x4mm
  - Contact Winbond for KGD and other options

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4 FEATURES

Single die secure solution

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- Meets SESIP L2 security certification requirements with compliance to IEC62443-4-2 and NIST 8259A
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- Secure & Unique Device ID
- Cryptographically-secured write-protection
- Local and remote secure channel, encrypted, authenticated, replay-protected
- Replay Protection Monotonic counter
- Platform Firmware Resiliency assurance (NIST SP 800-193)
- Secure Root of Trust (RoT) for IoT devices
- Secure provisioning, management and storage of keys
- Unique device Master Key
- Remote Key Provisioning
- On-chip data hash for fast code authentication
- DICE-like device attestation
- In-system and mass programming options

Automotive Safety

- Meets ISO 26262 ASIL-C automotive safety requirements

Standard SPI-Flash drop-in replacement

- Highest Performance Secure Serial Flash
  - 133 MHz SPI Single/Dual/Quad/QPI
  - 66 MHz Dual Transfer Rate (DTR) mode
  - More than 100,000 erase/program cycles per block
  - More than 20-year data retention
- Efficient Host Interface
  - Execution in place (XIP)
  - Continuous read and burst read
  - 32-Byte Secure burst read
- Flexible Architecture with 4kB Blocks
  - Uniform 4K-bytes granularity for Block Erase
  - Page Program up to 256 bytes per command
  - Secure Program 32 bytes in a single command
  - Automatic write verification
  - Erase/Program Suspend & Resume
- Low Power, single 1.8V power supply
- Wide Temperature Range
  - -40°C to +85°C (Industrial)
- Space efficient packaging
  - 8-pin SOIC 208-mil
  - 16-pin SOIC 300-mil
  - WSON8 6x5mm
  - 8-pad XSON 4x4mm
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5 BLOCK DIAGRAM

The W77Q32JW/W77Q16JW can be connected to a host device as shown in Figure 1.

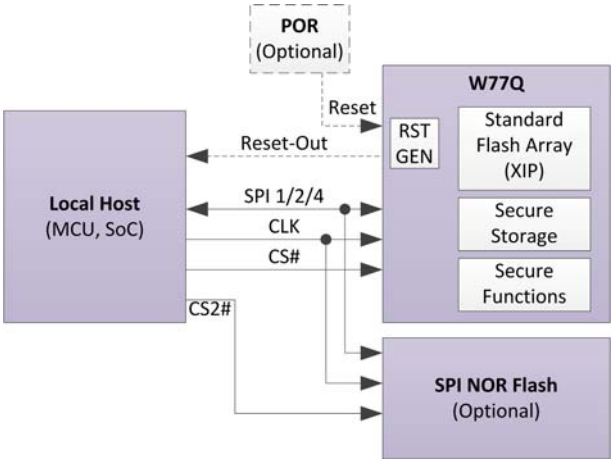
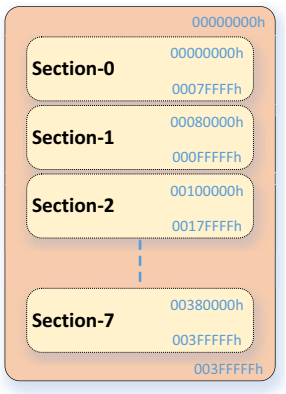


Figure 1: System Overview

The W77Q32JW/W77Q16JW memory is partitioned into 8 logical Sections, mapped from *logical address space* to *physical address space* by its security functions. The logical address space refers to the User address space as used in the plain-access SPI instructions. The physical address space refers to addresses of physical memory.

For example, the logical address space may be partitioned into 8 Sections, as illustrated in the following diagram:



Refer to Section 7.2 for further information regarding memory mapping and the Logical Address Space.

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6 OVERVIEW

The W77Q32JW/W77Q16JW device is composed of a single contiguous Flash Memory Array, logically divided into 8 Logical Sections. Each section can be individually configured with a Security Policy that enables advanced security functions. When none of these functions are enabled, the device operates as a standard SPI NOR Flash Memory device with no additional restrictions on read and write access.

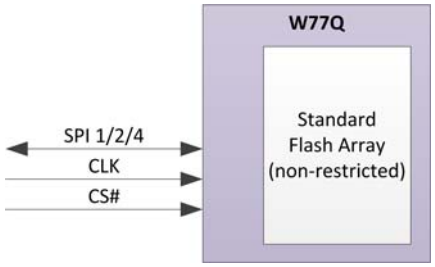


Figure 2: W77Q32JW/W77Q16JW with Security Functions Disabled (default configuration)

By setting up different sections, the array can be logically partitioned into separate areas. An individually configured Security Policy can then be applied to each section, enabling Encryption, Authentication, Write Protection, Rollback Protection, Integrity Protection and other security functions. Figure 3 shows an example of a W77Q32JW/ W77Q16JW device with a few enabled security functions.

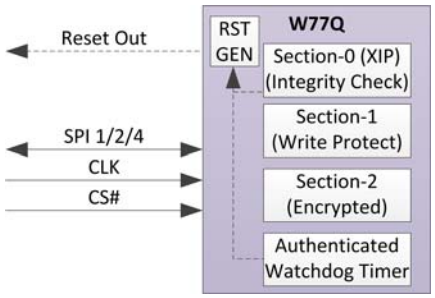


Figure 3: W77Q32JW/W77Q16JW With Enabled Security Functions (Example)

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6.1 Introduction

The W77Q32JW/W77Q16JW TrustME® Secure Serial Flash memory combines general purpose code and data storage, as well as secure storage and advanced security functions, all within a single Flash Memory device.

The W77Q32JW/W77Q16JW Secure Flash Memory device has full functional and pin-to-pin compatibility with standard Flash Memory devices, yet it offers security well beyond ordinary Flash devices. The internal cryptographic hardware engines handle all aspects of secure key provisioning, management and storage, as well as secure storage and general purpose storage solution.

The Secure Flash Memory device offers advanced security functions to ensure:

- Data confidentiality
- Data and command authentication
- Replay protection
- Platform firmware resiliency (with respect to *Protection, Detection* and *Recovery* of firmware state changes)
- Cryptographically secured write protection
- Secure code update with Rollback Protection
- Root of Trust management
- Authenticated Watchdog Timer with an optional hardware reset output

These functions are managed by privileged users, defined and assigned by the Device and Section Controllers, as explained in the following chapters.

6.2 Device Controller

Each Secure Flash Memory device is managed by a **Device Controller**, which is the authorized user or process that can configure the device and issue keys that grant access to its security functions.

Controlling the device requires knowing the **Device Master Key (K_D)**, which is used to set the device **Global Memory Configurations**. These partition the device into Memory Sections, as explained in the following chapters.

The device is fabricated with default Device Master Key (K_D). This Key may be updated later by the Device Controller.

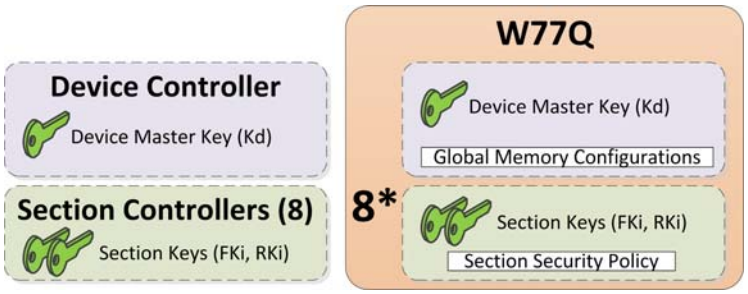


Figure 4: Device and Section Controllers

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6.3 Memory Sections

Access to the W77Q32JW/W77Q16JW Flash memory is managed on the basis of **Memory Sections**.

The device implements up to 8 logical Memory Sections. Each section is mapped to a region of physical memory, and each has a **Section Security Policy** that controls access to the memory mapped to the Section and the associated security functions.

Each Memory Section is independently managed by a **Section Controller**, which is the authorized user or process that can configure the Section and its security functions.

Secure access to a Section's memory and security functions requires using a **Secure Channel**.

6.4 Secure Channel

The **Secure Channel** is a Logical Communication Channel used to access the secure data and security functions associated with each Memory Section. These cannot be accessed without establishing a Secure Channel.

The Secure Channel handles data encryption and authentication for all secure transactions between the W77Q32JW/W77Q16JW device and a privileged user (e.g., a local MCU or remote server).

Note: Standard (non-secure, plain text) read and write access to a section (e.g., FAST_READ instructions) does not require a Secure Channel, if permitted by the Section Security Policy.

A Secure Channel is associated with a specific Memory Section or Secure Function. Only one Secure Channel may be established at any point of time, thus only one Memory Section may be securely accessed at any time. Switching to a different Memory Section requires establishing a new Secure Channel.

Plain Read/Write access to one Memory Section (including XIP), may be interleaved with secure access (through a Secure Channel) to another section.

Establishing a Secure Channel is done by opening a **Session**. Each Session defines a secret, one-time-use **Session Key** that is shared between the W77Q32JW/W77Q16JW device and the privileged user. This key is used to access the Section data and security functions.

A Secure Channel can be established between the W77Q32JW/W77Q16JW and a software process running on the local MCU as shown in Figure 5, or between the W77Q32JW/W77Q16JW and a Remote User or Process as shown in Figure 6.

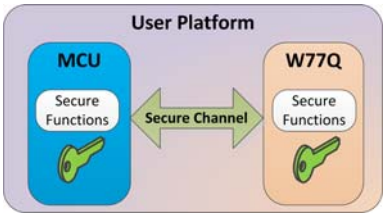


Figure 5: Secure Channel (Local)

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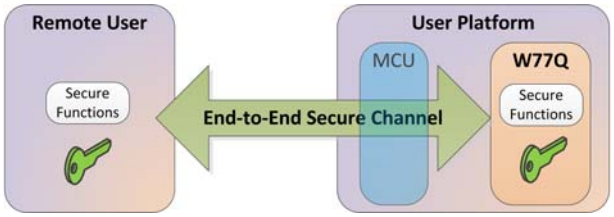


Figure 6: End-To-End Secure Channel (Remote)

6.4.1 Authentication

Secure transactions over the Secure Channel are authenticated by using the Session Key:

- Configuration commands must be properly signed by the user
- A Section may be configured as Cryptographically Write Protected, requiring all write and erase commands to be properly signed by the user
- Read data, status registers and configuration registers may be signed by the W77Q32JW/W77Q16JW device

6.4.2 Encryption

Payload of secure transactions over the Secure Channel is encrypted, using a secret, single-use **Cipher Key** (derived from the Session Key):

- Read, write and erase commands
- Configuration registers and status registers

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6.5 Platform Firmware Resiliency

The W77Q32JW/W77Q16JW device supports **Platform Firmware Resiliency** by providing mechanisms to ensure:

- **Protection**: Mechanisms for ensuring integrity of firmware code and critical data, including protection against corruption and unauthorized update.
- **Detection:** Mechanisms for detecting when firmware code and critical data have been corrupted or changed from an authorized state.
- **Recovery:** Mechanisms for restoring firmware code and critical data to a state of integrity in the event it have been corrupted or changed from an authorized state.

Protection is ensured by the Cryptographic Write Protection function, which requires authentication of each write access. Secure Firmware update is further protected by the Secure Firmware Update with Rollback Protection function.

Detection is ensured by the Integrity Protection function that performs integrity checks of the section memory contents.

Recovery is ensured by the Safe Fallback function that remaps the Boot Section (section 0) to an alternative Fallback Section in the case of a failed integrity check.

6.6 Cryptographic Write Protection

A section may be configured to require authenticated write and erase commands. These commands must be properly signed with the active Session Key.

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6.7 Secure Firmware Update with Rollback Protection

A rollback attack is a known method used to exploit vulnerabilities found in older code versions. The attack is carried out by replacing existing code with an older version. The older version may be properly signed and authenticated, making it hard to defend against this form of attack.

The Secure Flash Memory device implements a Hardware Rollback Protection function that can authenticate memory content and its version, and securely update existing memory.

This function allows Secure Firmware Update using *a single atomic operation*. A failed update operation reverts the code to the last known authentic state.

The Rollback Protection function enables the user/host to execute (XIP) from existing code stored in Flash memory, while a newer version of this code is being updated. After the new code version is written to the Flash memory, it is authenticated and its version is verified. When authentication is complete, the device hardware seamlessly swaps the two versions.

The authentication process verifies that the version of the new code is equal to or greater than the version of the existing memory content. This prevents older versions from replacing newer versions, even if they are properly signed.

This function partitions a memory section into two partitions of equal size. One partition holds the existing memory content while a newer version of the memory content can be written to the other partition. The partitions are mapped from logical address space into physical memory by a hardware mapping function that can swap between the two physical partitions. Swapping is done only after the new content is programmed and authenticated.

6.8 Integrity Protection

The Integrity Protection function performs integrity checks of the section memory contents. These checks may be scheduled automatically after reset, when a session is opened or when the section is updated.

6.8.1 Safe Fallback

The Safe Fallback function provides mechanisms for restoring firmware code and critical data to a state of integrity in the event they have been corrupted or changed from an authorized state.

This is ensured by remapping the Boot Section (section 0) to an alternative Fallback Section in the case of a failed integrity check. The boot code should provide means to handle failed integrity checks of other sections.

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6.9 Authenticated Watchdog Timer (AWDT)

The Secure Flash Memory device maintains a secure watchdog timer. The timer is reset by an authenticated command, signed by a designated key.

The device reaction to an expired timer is configurable and may include:

- Status indication
- Setting the reset-output pin

6.10 Root Of Trust Management

Root-of-Trust (RoT) is the foundation for the secure operation of a system, ensuring it is executing authentic code as intended by the system designer.

The W77Q32JW/W77Q16JW implements advanced security functions to ensuring code authenticity throughout the entire device life-time, i.e. when code is stored or updated and when the system performs its reset (boot) sequence.

The W77Q32JW/W77Q16JW also supports advance Security Functions for **remote device attestation**. These are used to establish Root Of Trust between the device and a remote User, by authenticating the device hardware and firmware identities.

The W77Q32JW/W77Q16JW offers an advanced approach for Remote Attestation that does not require the participation of the local MCU in the cryptographic operation. This approach is based on the ability of the W77Q32JW/W77Q16JW to establish an End-to-End Secure Channel to a remote User and directly measure the stored code and securely report and authenticate the measurement to the remote User.

6.11 Secure Reset Sequence

A device reset sequence may take a considerable amount of time to complete (up to a few milliseconds), due to enforcement of security policies and integrity checks for some of the sections memory contents.

The device implements a reset output pin to keep the Host in reset while the Secure Flash Memory completes its reset sequence.

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6.12 SPI Bus

6.12.1 Standard SPI Instructions

The W77Q32JW/W77Q16JW is accessed through an SPI-compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI), and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses. or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operations Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.12.2 Dual SPI Instructions

The W77Q32JW/W77Q16JW supports Dual SPI operation when using instructions such as Fast Read Dual Output (3Bh) and Fast Read Dual I/O (BBh). These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash Memory devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.12.3 Quad SPI Instructions

The W77Q32JW/W77Q16JW supports Quad SPI operation when using instructions such as Fast Read Quad Output (6Bh), and Fast Read Quad I/O (EBh). These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.12.4 QPI Instructions

The W77Q32JW/W77Q16JW supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the Enter QPI Mode (38h) instruction. The typical SPI protocol requires that the byte-long instruction code be shifted into the device only via the DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment.

Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. Enter QPI Mode (38h) and Exit QPI Mode (FFh) instructions are used to switch between these two modes.

Upon power-up or after a software reset using the Reset (99h) instruction (see Section 7.8.14), the default state of the device is Standard/Dual/Quad SPI mode. To

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enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 must be set. See Figure 7.When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See Figure 7 for the device operation modes.

6.12.5 SPI/QPI Operations

Figure 7 is a schematic diagram that shows the SPI and QPI operations of the W77Q32JW/W77Q16JW Serial Flash Memory

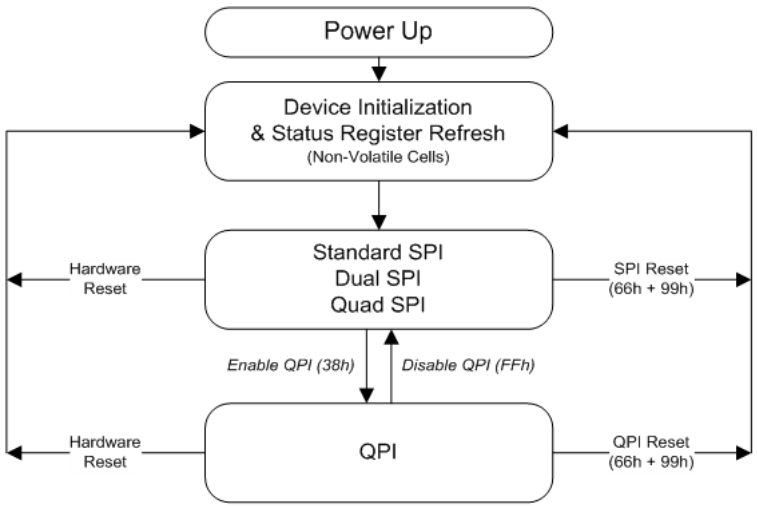


Figure 7: SPI Mode Operation Diagram

6.12.6 SPI/QPI DTR Read Instructions

To effectively improve the read operation throughput without increasing the serial clock frequency, W77Q32JW/W77Q16JW introduces multiple Double Transfer Rate (DTR) Read instructions that support Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output are latched on both rising and falling edges of the serial clock.

6.12.7 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W77Q32JW/ W77Q16JW operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI or QPI operation. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as /HOLD pin or data I/O pin. When QE = 0 (factory default), the pin is /HOLD; when QE = 1, the pin becomes an I/O pin, and the /HOLD function is no longer available.

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To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low, the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK.

During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal must be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.12.8 Software Reset and Hardware Reset Pin

The W77Q32JW/W77Q16JW can be reset to the initial power-on state by a software Reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) and Reset Device (99h). If the command sequence is successfully accepted, the device will take approximately 35uS (t_{RST}) to reset. No command will be accepted during the reset period.

For 8-pin package types, W77Q32JW/W77Q16JW can be configured to utilize a hardware reset pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for a HOLD pin function or a RESET pin function. If the QE bit is set to 1, the HOLD or RESET function are disabled and the pin becomes one of the four data I/O pins.

- When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above.
- When HOLD/RST=1, the pin acts as RSTI# pin.

Driving the RSTI# pin low for a minimum period of ~1 us (tRESET*) resets the device to its initial power-on state. Any ongoing Program/Erase operation is interrupted and data corruption may happen. While RSTI# is low, the device does not accept any command input.

For larger packages (more than 8-pins), the W77Q32JW/W77Q16JW provides a dedicated RSTIN# pin in addition to the shared HOLD/RESET (IO_3) pin as illustrated in Figure 1. Driving the dedicated RSTIN# pin low for a minimum period of ~1us (tRESET*) resets the device to its initial power-on state. The HOLD/RST bit or the QE bit in the Status Register does not affect the function of this dedicated RSTIN# pin.

The Hardware Reset pin has the highest priority among all the input signals. Driving this pin low for a minimum period of ~1 us (tRESET*) interrupts any ongoing external/ internal operation, regardless of the status of other SPI signals (/CS, CLK, IOs, /WP and/or /HOLD).

Note:

1. Whereas a faster reset pulse (as short as a few hundred nanoseconds) will often reset the device, a 1 us minimum is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated RSTIN# pin. If the reset function is not needed, this pin can be left floating in the system.

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6.13 Standard-Flash Write Protection

Applications that use non-volatile memory must take into consideration the possibility that noise and other adverse system conditions may compromise data integrity. To address this concern, the W77Q32JW/W77Q16JW provides several means to protect data from inadvertent writes.

6.13.1 Write Protection Features

- Device resets when VCC is below threshold
- Time-delay write disable after Power-Up
- Write-enable/disable instructions and automatic write-disable after erase or program
- Software and hardware (/WP pin) write-protection using status registers
- Additional individual block/sector locks for array protection
- Write-protection using Power-Down instruction
- Lock Down write-protection for Status Register until the next Power-Up
- One Time Program (OTP) write-protection for array and security registers using Status Register*

NOTE: The OTP feature is available upon special flow. Please contact Winbond for details.

6.13.2 Write Protection After Power-Up

Upon Power-Up or at Power-Down, the W77Q32JW/W77Q16JW maintains a reset condition while VCC is below the threshold value of V_{WI}, (See Power-Up Timing and Voltage Levels and Figure 86. While reset, all operations are disabled and instructions are not recognized. During Power-Up and after the VCC voltage exceeds V_{WI}, all program and erase-related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable (06h), Page Program (02h), Quad Input Page Program Instruction (SPI Mode only)), Sector Erase Instruction (QPI Mode), 64KB Block Erase (D8h), Chip Erase (C7h/60h), and the Write Status Register (see Section 12) instructions. Note that the chip select pin (/CS) must track the VCC supply level at Power-Up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at Power-Down to prevent adverse command sequence. If needed, a pull-up resistor on /CS can be used to accomplish this.

6.13.3 Write Enable / Disable State

After Power-Up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to 0. A Write Enable (06h) instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase, or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Additionally, the Power-Down (B9h) instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-Down instruction.

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6.13.4 Memory Range Protection

Software-controlled write-protection (WPS=0) is facilitated using the Write Status Register instruction and by setting the Status Register Protect/Lock (SRP, SRL) and Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits. These settings allow a continuous portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See the Status Register section (Section 8.2) for further information.

6.13.5 Individual Block/Sector Locks

The W77Q32JW/W77Q16JW also provides another Write Protect method (WPS=1) using the Individual Block Locks. Each 64 KB block (except the top and bottom blocks, total of 62 blocks) and each 4 KB sector within the top/bottom blocks (total of 32 sectors) are equipped with an Individual Block Lock bit. When the lock bit is 0, the corresponding sector or block can be erased or programmed; when the lock bit is set to 1, Erase or Program commands issued to the corresponding sector or block are ignored. When the device is powered on, all Individual Block Lock bits are 1, so the entire memory array is protected from Erase/Program. An Individual Block Unlock (39h) instruction (see Section 16) must be issued to unlock any specific sector or block.

6.13.6 Write Protection Mode Select

The WPS bit in Status Register-3 is used to decide which Write Protect scheme is used.

- When WPS = 0 (factory default), the device utilizes the Memory Range Protection function (CMP, SEC, TB, BP[2:0] bits) to protect specific areas of the array.
- When WPS = 1, the device utilizes the Individual Block/Sector Locks for write protection.

6.13.7 Standard Write Protection and Secure Features

Standard-Flash Write Protection features described in Section 6.13 may be affected by the logical-to-physical memory mapping, whereas the Secure Write Protection features (see [SA]) are always mapped to ***logical*** memory. It is therefore recommended not to use Standard-Flash Write Protection features in a security-aware application.

To prevent unexpected behavior, Standard-Flash Write Protection features should be used under the following restrictions (refer to [SA] for further details):

- Standard Write Protection features should be used only when the device is in its Factory-default configuration, i.e. Section-0 mapped to entire physical memory.
- Logical memory partitions (“Sections”) must not overlap, i.e., must not point to same physical memory.
- Memory Range Protection (WPS=0) affects the first/last portion of the ***logical*** memory, while considering only address bits [23:0] (ignoring the extended address register).
- Individual Block/Sector Locks (WPS=1) is mapped to ***physical*** memory.

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- Individual Sector Lock is allowed only within the first/last ***physical*** memory block.

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7 INSTRUCTIONS

The W77Q32JW/W77Q16JW device supports standard Serial Flash instructions, as well as proprietary instructions to operate its advanced security functions.

Standard Flash instructions include:

- Standard Configuration Instructions
- Standard Read Instructions
- Standard Write Instructions
- Standard Auxiliary Instructions

These instructions are supported in different formats, including Standard / Dual / Quad SPI, as well as QPI mode, and Single or Double Transfer Rates (STR / DTR).

Instructions to operate the advanced security functions are described in the [SA].

7.1 Standard Serial Flash Instruction Formats

The Standard/Dual/Quad SPI instruction set of the W77Q32JW/W77Q16JW consists of 48 basic instructions that are fully controlled through the SPI bus (see Section 7.4.1 and Section 7.4.2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of the clock with the most significant bit (MSB) first.

The QPI instruction set of the W77Q32JW/W77Q16JW consists of 35 basic instructions that are fully controlled through the SPI bus (see Section 7.4.3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked through IO[3:0] pins provides the instruction code. Data on all four IO pins is sampled on the rising edge of clock with Most Significant Bit (MSB) first. All QPI instructions, addresses, data, and dummy bytes use all four IO pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination of bytes. Instructions are completed with the rising edge of edge /CS. Clock-relative timing diagrams for each instruction are included in Figure 7 through Figure 24. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program, or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked), otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

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7.2 Plain Access Memory Addressing

Plain access instructions (e.g. Fast-Read, Page-Program, etc) use the ***logical address*** to directly access any address in memory.

The 3 MS-bits of the *logical address* are used as the Section Index (SID) to select one of the Sections. The exact location of the SID bits is defined by the SECT_SEL register, as defined in [SA].

The remaining address bits are used as offset within the Section memory.

Refer to [SA] for further information on Section Address Modes.

7.3 Manufacturer ID and Device ID

Manufacturer ID and Device ID parameters can be read using different SPI instructions (e.g. Read Manufacturer/Device ID (90h), Read JEDEC ID (9Fh)). The response value for these instructions is defined as follows:

FIELD	DESIGNATION	VALUE	NOTES
Manufacturer ID	MF7-MF0	EFh	Winbond Serial Flash
Device ID	ID7-ID0	15h	Instructions: ABh, 90h, 92h, 94h
	ID15-ID0	8A16h	Instruction 9Fh (W77Q32JW/ W77Q16JW Single-Die)

Note: Device ID is stated in the table above, for both 16Mbit and 32Mbit devices. To differentiate between 16Mbit and 32Mbit devices, read SFDP byte at address C6h.

7.4 Standard Serial Flash Instruction Set Tables

The following Instruction Set tables show standard Flash instructions:

- Instruction Set Table 1 (Standard SPI Instructions)
- Instruction Set Table 2 (Dual/Quad SPI Instructions)
- Instruction Set Table 3 (QPI Instructions)
- Instruction Set Table 4 (DTR with SPI Instructions)
- Instruction Set Table 5 (DTR with QPI Instructions)

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7.4.1 Instruction Set Table 1 (Standard SPI Instructions)

Table 1: Standard SPI Instruction Set (1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	8	8	8	8	8	8	8
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Release Power-down	ABh						
Device ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	90h	00	00	00	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read Unique ID	4Bh	Dummy	Dummy	Dummy	Dummy	(UID63-0)	
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)		
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Read Status Register-1	05h	(S7-S0)(2)					
Write Status Register-1	01h	(S7-S0)(4)					
Read Status Register-2	35h	(S15-S8)(2)					
Write Status Register-2	31h	(S15-S8)					
Read Status Register-3	15h	(S23-S16)(2)					
Write Status Register-3	11h	(S23-S16)					
Write Extended Addr Register	C5h	EA7-EA0					
Read SFDP Register	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase Security Register(5)	44h	A23-A16	A15-A8	A7-A0			
Program Security Register(5)	42h	A23-A16	A15-A8	A7-A0	D7-D0(3)		
Read Security Register(5)	48h	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Global Block Lock	7Eh						
Global Block Unlock	98h						
Read Block Lock	3Dh	A23-A16	A15-A8	A7-A0	(L7-L0)		
Individual Block Lock	36h	A23-A16	A15-A8	A7-A0			
Individual Block Unlock	39h	A23-A16	A15-A8	A7-A0			
Erase/Program Suspend	75h						
Erase/Program Resume	7Ah						
Power-down	B9h						
Enter QPI Mode	38h						
Enable Reset	66h						
Reset Device	99h						

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7.4.2 Instruction Set Table 2 (Dual/Quad SPI Instructions)

Table 2: Dual/Quad SPI Instruction Table(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Number of Clock(1-1-2)	**8**	**8**	**8**	**8**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(7)	…	
Number of Clock(1-2-2)	**8**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual I/O	**BBh**	A23-A16(6)	A15-A8(6)	A7-A0(6)	M7-M0	(D7-D0)(7)	…		
Mftr./Device ID Dual I/O	**92h**	A23-A16(6)	A15-A8(6)	00(6)	Dummy(14)	(MF7-MF0)	(ID7-ID0)(7)		
Number of Clock(1-1-4)	**8**	**8**	**8**	**8**	**2**	**2**	**2**	**2**	**2**
Quad Input Page Program	**32h**	A23-A16	A15-A8	A7-A0	(D7-D0)(9)	(D7-D0)(3)	…		
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)(10)
Number of Clock(1-4-4)	**8**	**2**(8)	**2**(8)	**2**(8)	**2**	**2**	**2**	**2**	**2**
Mftr./Device ID Quad I/O	**94h**	A23-A16	A15-A8	00	Dummy(14)	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)	…
Set Burst with Wrap	**77h**	Dummy	Dummy	Dummy	W7-W0				

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7.4.3 Instruction Set Table 3 (QPI Instructions)

Table 3: QPI Instruction Table(12)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (4-4-4)	2	2	2	2	2	2	2
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Release Power-down	ABh						
Device ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Set Read Parameters	C0h	P7-P0					
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy(13)	(D7-D0)	…
Burst Read with Wrap	0Ch	A23-A16	A15-A8	A7-A0	Dummy(13)	(D7-D0)	…
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0(13)	(D7-D0)	…
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0(9)	D7-D0(3)	…
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Read Status Register-1	05h	(S7-S0)(2)					
Write Status Register-1	01h	(S7-S0)(4)					
Read Status Register-2	35h	(S15-S8)(2)					
Write Status Register-2	31h	(S15-S8)					
Read Status Register-3	15h	(S23-S16)(2)					
Write Status Register-3	11h	(S23-S16)					
Write Extended Addr Register	C5h	EA7-EA0					
Global Block Lock	7Eh						
Global Block Unlock	98h						
Read Block Lock	3Dh	A23-A16	A15-A8	A7-A0	(L7-L0)		
Individual Block Lock	36h	A23-A16	A15-A8	A7-A0			
Individual Block Unlock	39h	A23-A16	A15-A8	A7-A0			
Erase/Program Suspend	75h						
Erase/Program Resume	7Ah						
Power-down	B9h						
Enable Reset	66h						
Reset Device	99h						
Exit QPI Mode	FFh						

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7.4.4 Instruction Set Table 4 (DTR with SPI Instructions)

Table 4: DTR with SPI Instructions Table

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	8	4	4	4	6	4	4
DTR Fast Read	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Number of Clock(1-2-2)	8	2	2	2	6	2	2
DTR Fast Read Dual I/O	**BDh**	A23-A16	A15-A8	A7-A0	Dummy(14)	(D7-D0)	….
Number of Clock(1-4-4)	8	1	1	1	8	1	1
DTR Fast Read Quad	**EDh**	A23-A16	A15-A8	A7-A0	Dummy(14)	(D7-D0)	(D7-D0)

7.4.5 Instruction Set Table 5 (DTR with QPI Instructions)

Table 5: DTR with QPI Instructions Table

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (4-4-4)	2	1	1	1	8	1	1
DTR Read with Wrap(13)	**0Eh**	A23-A16	A15-A8	A7-0	Dummy	(D7-D0)	…
DTR Fast Read	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
DTR Fast Read	**EDh**	A23-A16	A15-A8	A7-A0	Dummy(14)	(D7-D0)	

Notes:

1.Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1, 2 or 4 IO pins.

2.The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.

3.At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.

4.Write Status Register-1 (01h) can also be used to program Status Register-1&2. See section 8.2.5.

5.Security Register Address:

Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address

6.Dual SPI address input format:

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

7.Dual SPI data output format:

IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

8.Quad SPI address input format:

IO0 = A20, A16, A12, A8, A4, A0, M4, M0
IO1 = A21, A17, A13, A9, A5, A1, M5, M1
IO2 = A22, A18, A14, A10, A6, A2, M6, M2
IO3 = A23, A19, A15, A11, A7, A3, M7, M3

Set Burst with Wrap input format:

IO0 = x, x, x, x, x, x, W4, x
IO1 = x, x, x, x, x, x, W5, x
IO2 = x, x, x, x, x, x, W6, x
IO3 = x, x, x, x, x, x, x, x

9.Quad SPI data input/output format:

IO0 = (D4, D0, …..)
IO1 = (D5, D1, …..)
IO2 = (D6, D2, …..)
IO3 = (D7, D3, …..)

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10.Fast Read Quad I/O data output format:

IO0 = (x, x, x, x, D4, D0, D4, D0)
IO1 = (x, x, x, x, D5, D1, D5, D1)
IO2 = (x, x, x, x, D6, D2, D6, D2)
IO3 = (x, x, x, x, D7, D3, D7, D3)

11.QPI Command, Address, Data input/output format:

CLK #	0	1	2	3	4	5	6	7	8	9	10	11
IO0 =	C4,	C0,	A20,	A16,	A12,	A8,	A4,	A0,	D4,	D0,	D4,	D0
IO1 =	C5,	C1,	A21,	A17,	A13,	A9,	A5,	A1,	D5,	D1,	D5,	D1
IO2 =	C6,	C2,	A22,	A18,	A14,	A10,	A6,	A2,	D6,	D2,	D6,	D2
IO3 =	C7,	C3,	A23,	A19,	A15,	A11,	A7,	A3,	D7,	D3,	D7,	D3

12.The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.

13.The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.

14.The first dummy is M7-M0 should be set to Fxh; if not use continuous mode.

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7.5 Standard Configuration Instructions

This section describes standard Flash instructions to configure and operate the device:

- Write Enable (06h)
- Write Enable for Volatile Status Register (50h)
- Write Disable (04h)
- Read Status Registers: SR-1 (05h), SR-2 (35h) & SR-3 (15h)
- Write Status Registers: SR-1 (01h), SR-2 (31h) & SR-3 (11h)
- Individual Block/Sector Lock (36h)
- Individual Block/Sector Unlock (39h)
- Read Block/Sector Lock (3Dh)
- Global Block/Sector Lock (7Eh)
- Global Block/Sector Unlock (98h)
- Set Burst with Wrap (77h)
- Set Read Parameters (C0h)

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7.5.1 Write Enable (06h)

This instruction (Figure 8) sets the Write Enable Latch (WEL) bit in the Status Register to 1.

The WEL bit must be set prior to every Page Program, Sector/Block/Chip Erase, Write Status Register and Erase/Program Security Register operation.

The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

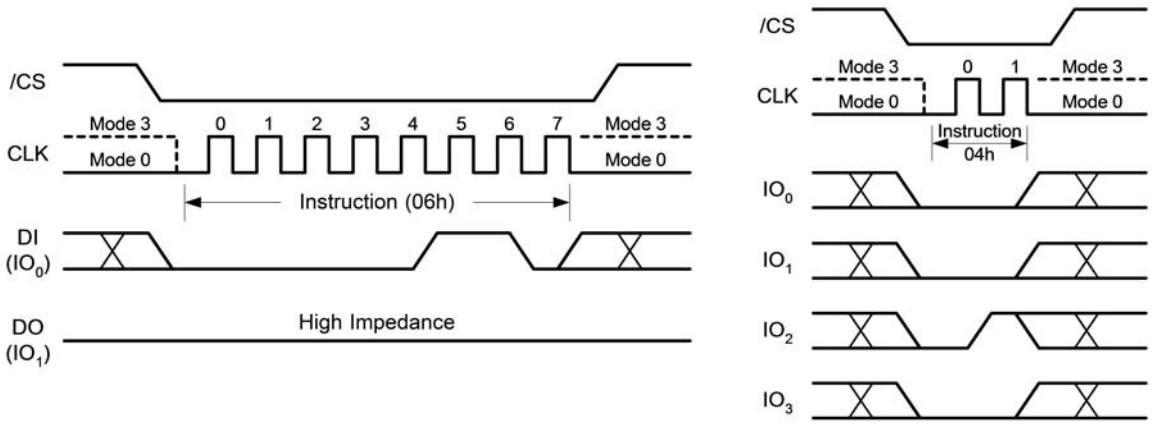


Figure 8: Write Enable Instruction for SPI Mode (left) or QPI Mode (right)

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7.5.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in Section 8.2 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits.

To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h, 31h or 11h) instruction (see Section 7.5.5).

A Write Enable for Volatile Status Register instruction (Figure 9) will not set the Write Enable Latch (WEL) bit; it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

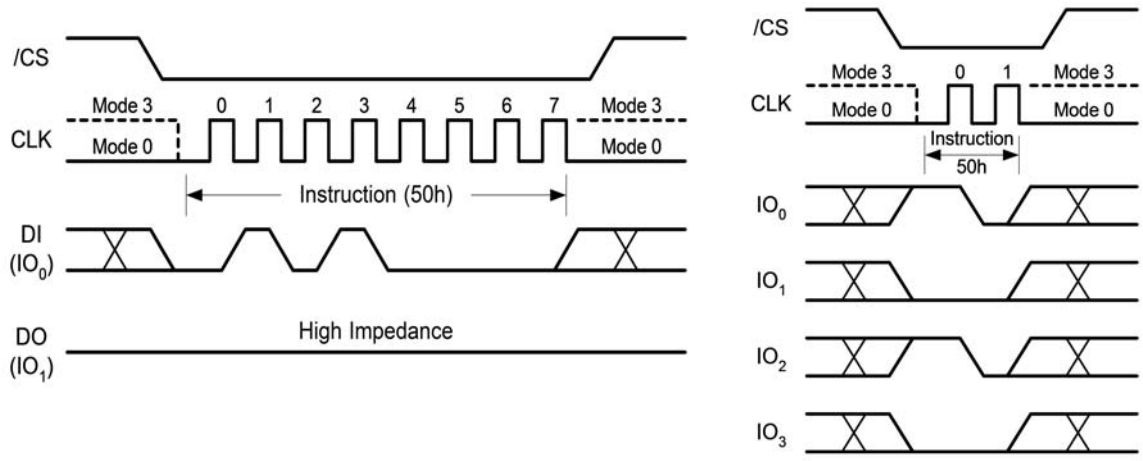


Figure 9: Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)

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7.5.3 Write Disable (04h)

The Write Disable instruction (Figure 10) resets the Write Enable Latch (WEL) bit in the Status Register to 0.

The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high.

Note that the WEL bit is automatically reset after Power-Up and upon completion of every Page Program, Sector/Block/Chip Erase, Write Status Register and Erase/ Program Security Register, Write Status Register, Reset operations and Secure Operations.

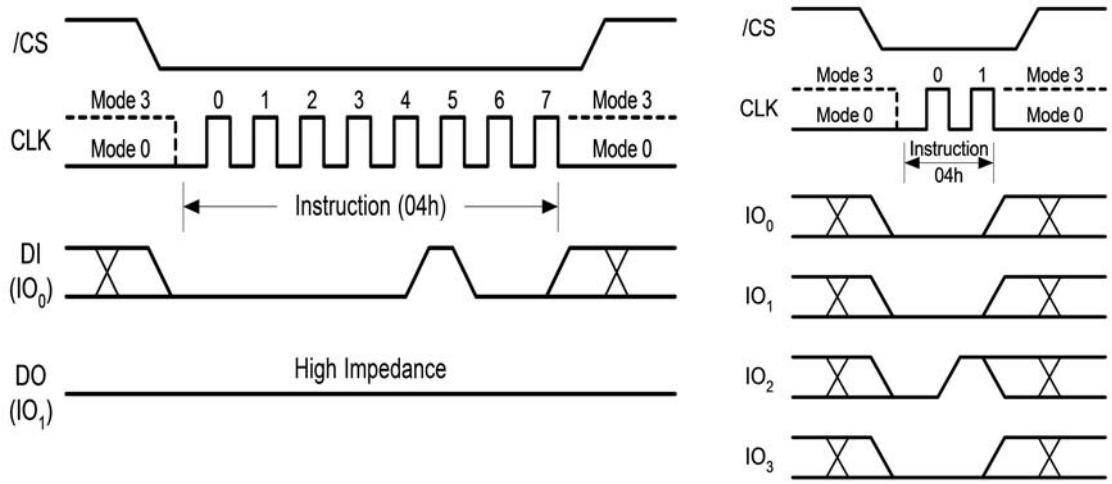


Figure 10: Write Disable Instruction for SPI Mode (left) or QPI Mode (right)

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7.5.4 Read Status Registers: SR-1 (05h), SR-2 (35h) & SR-3 (15h)

These instructions allow the 8-bit Status Registers (SR1, SR2 and SR3) to be read. Refer to Section 8.2 for Status Register descriptions.

The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register 1 (SR1), “35h” for Status Register 2 (SR2) or “15h” for Status Register 3 (SR3) into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 11.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 11 and Figure 12. The instruction is completed by driving /CS high.

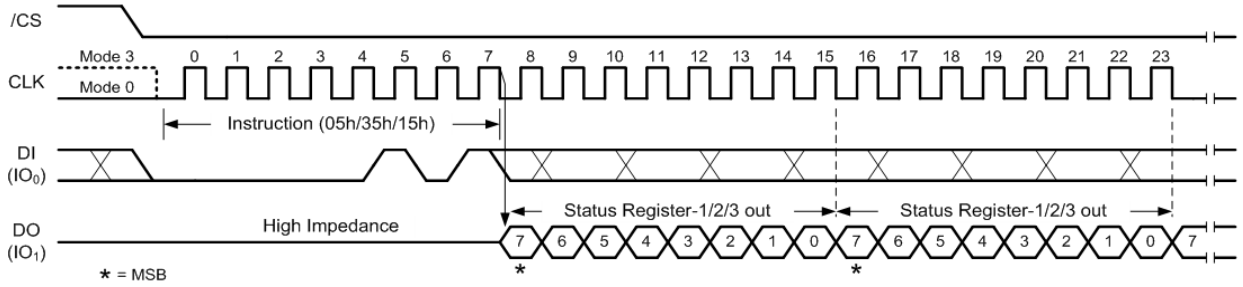


Figure 11: Read Status Register Instruction (SPI Mode)

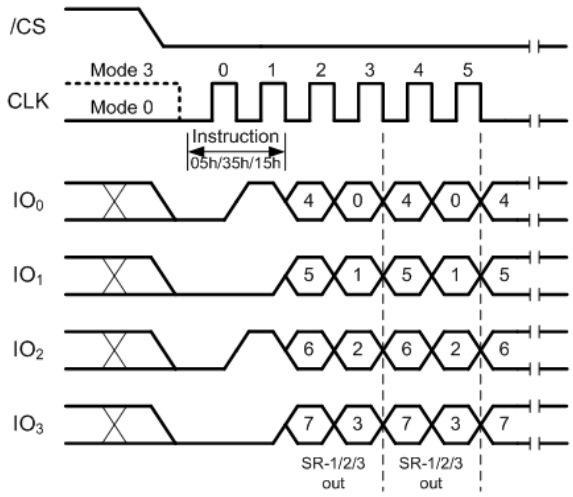


Figure 12: Read Status Register Instruction (QPI Mode)

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7.5.5 Write Status Registers: SR-1 (01h), SR-2 (31h) & SR-3 (11h)

The Write Status Register instruction allows the Status Registers (SR1, SR2 and SR3) to be written.

To write **volatile** Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). The SRL and LB3-LB1 cannot be changed from "1" to "0" because of the OTP protection for these bits.

Upon power off or the execution of a Software/Hardware Reset or Power-Down instruction, the volatile Status Register bit values revert to their default values loaded from the non-volatile Status Registers.

To write **non-volatile** Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write- enabled, the instruction is entered by driving /CS low, sending the instruction code "01h/31h/11h", and then writing the status register data byte as illustrated in Figure 13 and Figure 14.

During a non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle commences for a time duration of t_W (see AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (see AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE = 1 is required for the device to enter and operate in the QPI mode.

Refer to Section 8.2 for Status Register descriptions.

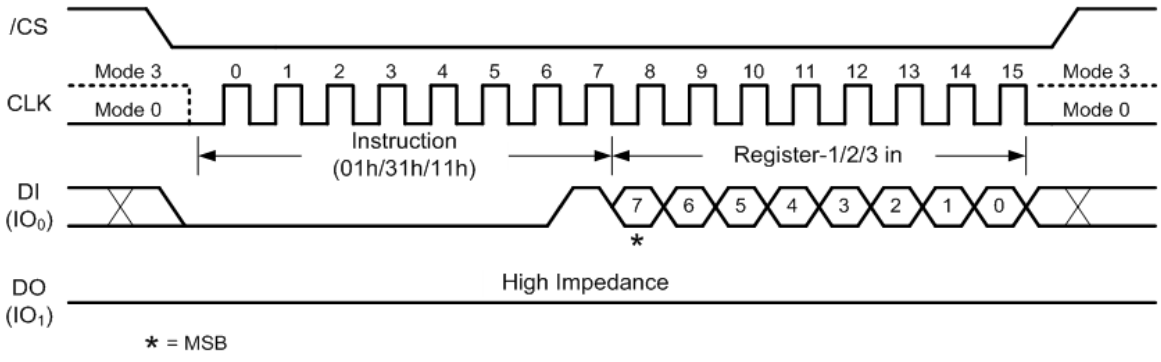


Figure 13: Write Status Register-1/2/3 Instruction (SPI Mode)

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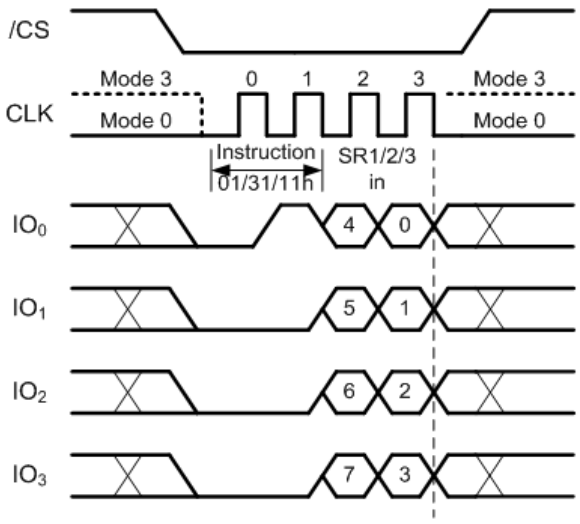


Figure 14: Write Status Register-1/2/3 Instruction (QPI Mode)

The W77Q32JW/W77Q16JW is also backward compatible to Winbond's previous generations of serial flash memories, in which Status Register 1 (SR1) and Status Register 2 (SR2) can be written using a single "Write Status Register-1 (01h)" command. To complete the Write Status Register-1 and 2 instruction, the /CS pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 15 and Figure 16. If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction only programs the Status Register 1 (SR1); the Status Register 2 (SR2) is not affected. (Previous generations will clear CMP and QE bits.)

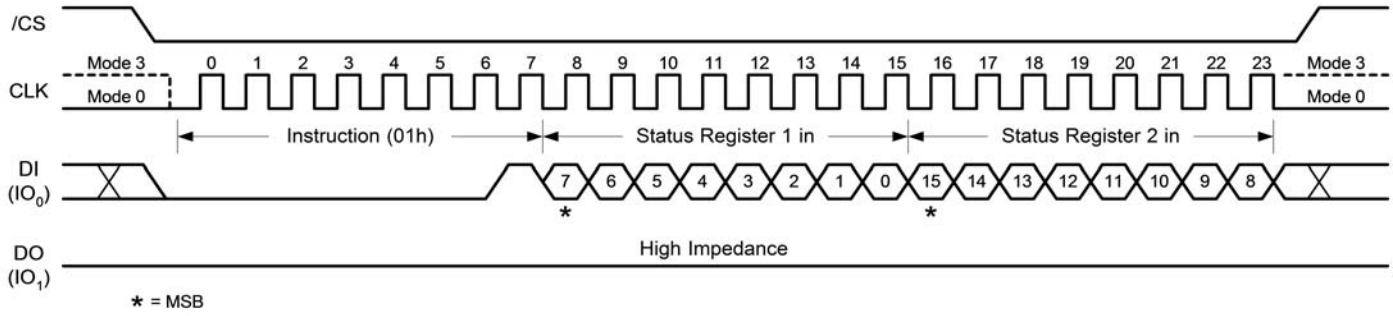


Figure 15: Write Status Register-1/2 Instruction (SPI Mode)

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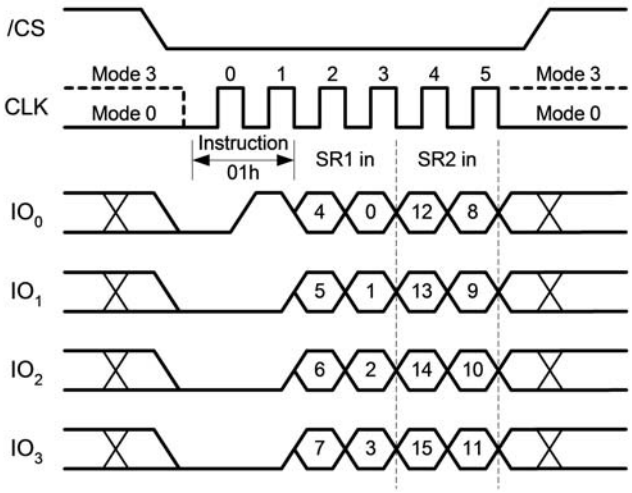


Figure 16: Write Status Register-1/2 Instruction (QPI Mode)

7.5.6 Individual Block/Sector Lock (36h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from an adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register 3 (SR3) must be set to 1. If WPS = 0, the write protection will be determined by the combination of CMP, SEC, TB, BP2, BP1, and BP0 in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

To lock a specific block or sector as illustrated in Figure 17 and Figure 18, an Individual Block/Sector Lock command must be issued by driving /CS low, shifting the instruction code “36h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving /CS high.

A Write Enable (06h) instruction must be executed before the device will accept the Individual Block/Sector Lock Instruction (Status Register bit WEL = 1).

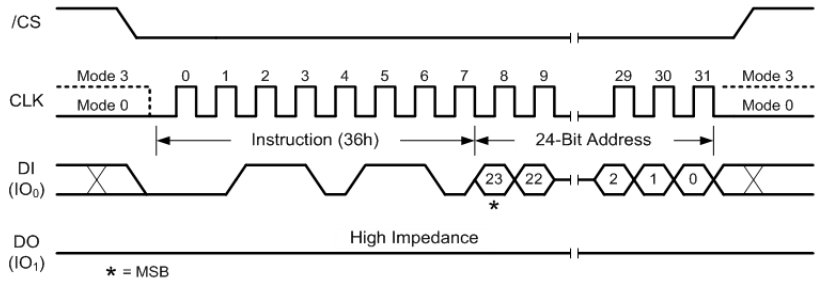


Figure 17: Individual Block/Sector Lock Instruction (SPI Mode)

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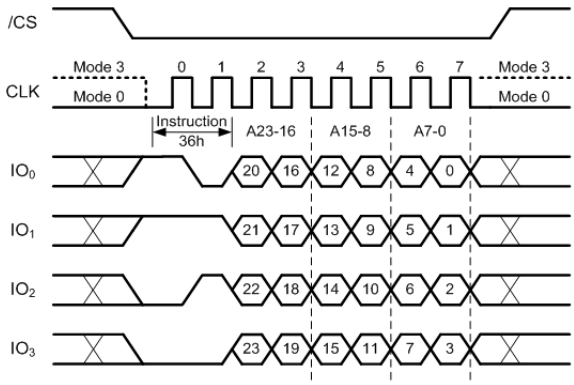


Figure 18: Individual Block/Sector Lock Instruction (QPI Mode)

7.5.7 Individual Block/Sector Unlock (39h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from an adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register 3 (SR3) must be set to 1. If WPS = 0, the write protection is determined by the combination of CMP, SEC, TB, BP2, BP1, and BP0 bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is protected.

To unlock a specific block or sector as illustrated in Figure 19 and Figure 20, an Individual Block/Sector Unlock command must be issued by driving /CS low, shifting the instruction code “39h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving /CS high. A Write Enable instruction must be executed before the device accepts the Individual Block/Sector Unlock Instruction (Status Register bit WEL = 1).

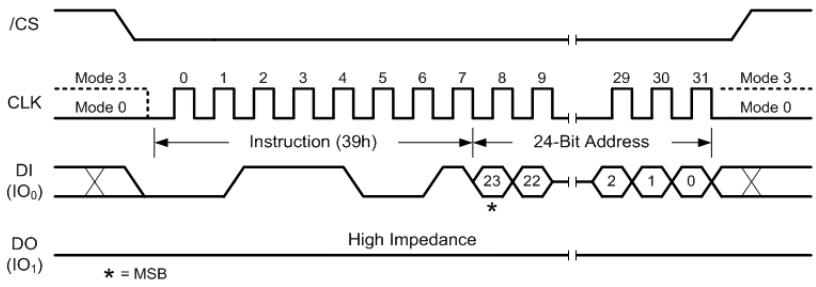


Figure 19: Individual Block/Sector Unlock Instruction (SPI Mode)

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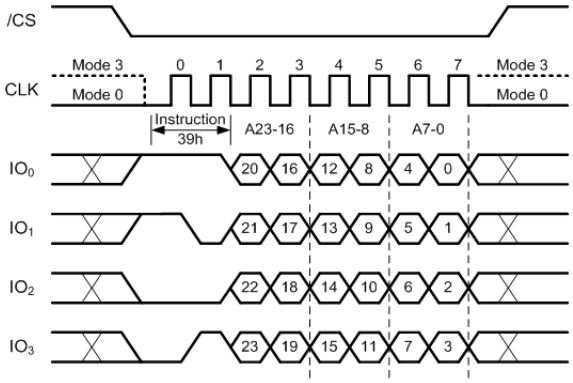


Figure 20: Individual Block/Sector Unlock Instruction (QPI Mode)

7.5.8 Read Block/Sector Lock (3Dh)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from an adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register 3 (SR3) must be set to 1. If WPS = 0, the write protection is determined by the combination of CMP, SEC, TB, BP2, BP1 and BP0 bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is protected.

To read out the lock bit value of a specific block or sector, a Read Block/Sector Lock command must be issued by driving /CS low, shifting the instruction code “3Dh” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address. The Block/Sector Lock bit value is shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 21 and Figure 22. If the least significant bit (LSB) is 1, the corresponding block/sector is locked; if LSB = 0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.

Note: Block and Sector Lock does not affect Secure operations.

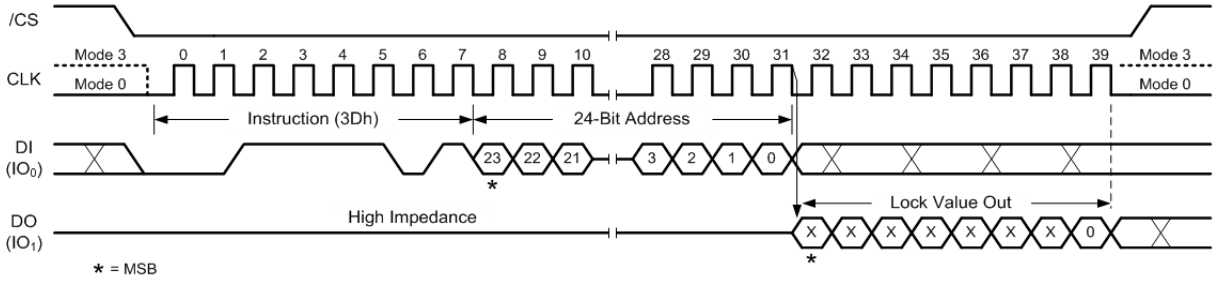


Figure 21: Read Block Lock Instruction (SPI Mode))

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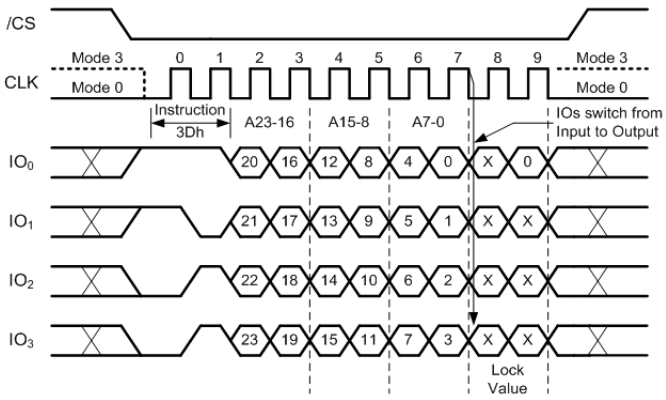


Figure 22: Read Block Lock Instruction (QPI Mode)

7.5.9 Global Block/Sector Lock (7Eh)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock instruction. The command must be issued by driving /CS low, shifting the instruction code "7Eh" into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high. A Write Enable (06h) instruction must be executed before the device will accept the Global Block/Sector Lock Instruction (Status Register bit WEL = 1).

Note: Block and Sector Lock does not affect Secure operations.)

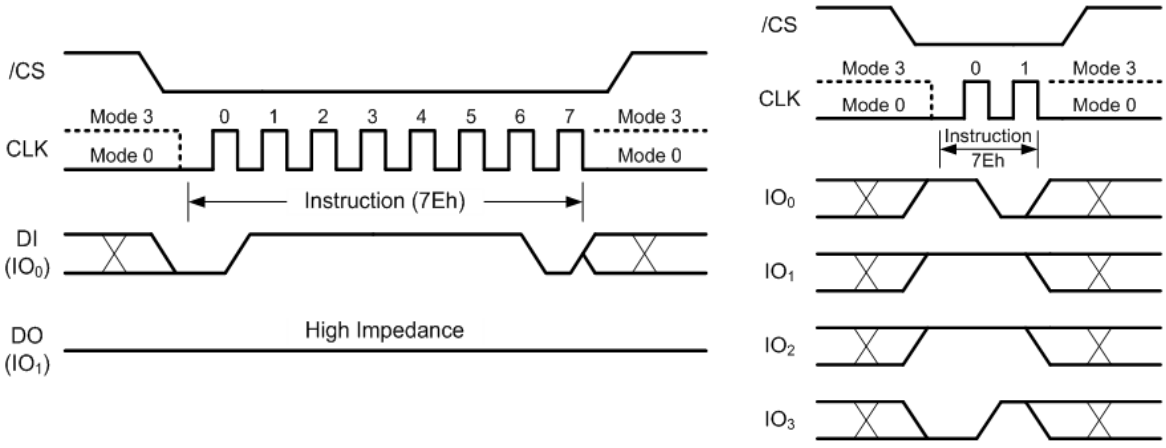


Figure 23: Global Block Lock Instruction for SPI Mode (left) or QPI Mode (right)

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7.5.10 Global Block/Sector Unlock (98h)

All Block/Sector Lock bits can be set to 0 by the Global Block/Sector Unlock instruction. The command must be issued by driving /CS low, shifting the instruction code “98h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high. A Write Enable (06h) instruction must be executed before the device will accept the Global Block/Sector Unlock Instruction (Status Register bit WEL = 1).

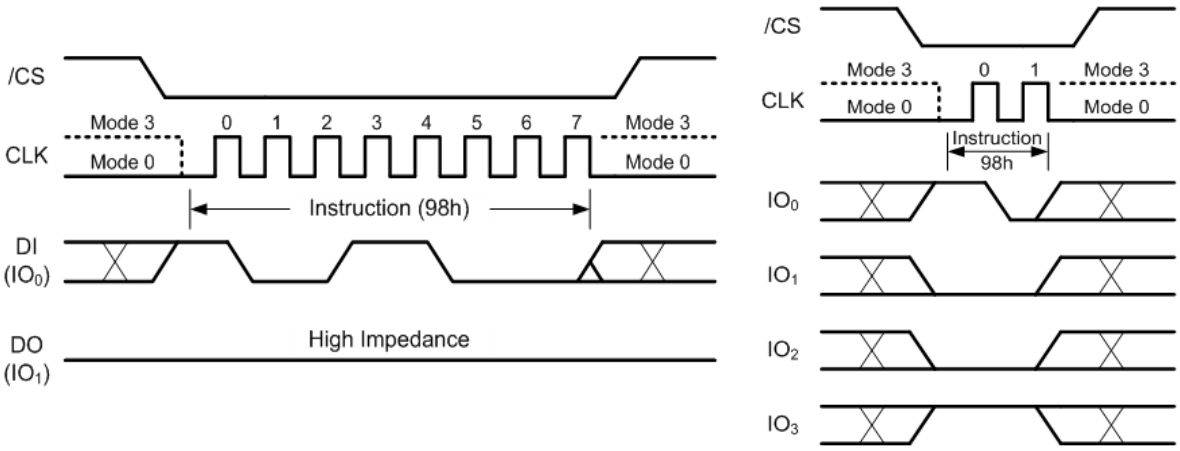


Figure 24: Global Block Unlock Instruction for SPI Mode (left) or QPI Mode (right)

7.5.11 Set Burst with Wrap (77h)

This instruction is used in conjunction with Fast Read Quad I/O (EBh), DTR Fast Read Quad I/O (EDh) instruction (SPI mode only) to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 25. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	WRAP AROUND	WRAP LENGTH	WRAP AROUND	WRAP LENGTH
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, the following “Fast Read Quad I/O” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

In QPI mode, the Burst Read with Wrap (0Ch) instruction should be used to perform the Read operation with “Wrap Around” feature. The Wrap Length set by W5-4 in

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Standard SPI mode is still valid in QPI mode and can also be reconfigured by the Set Read Parameters (C0h) instruction.

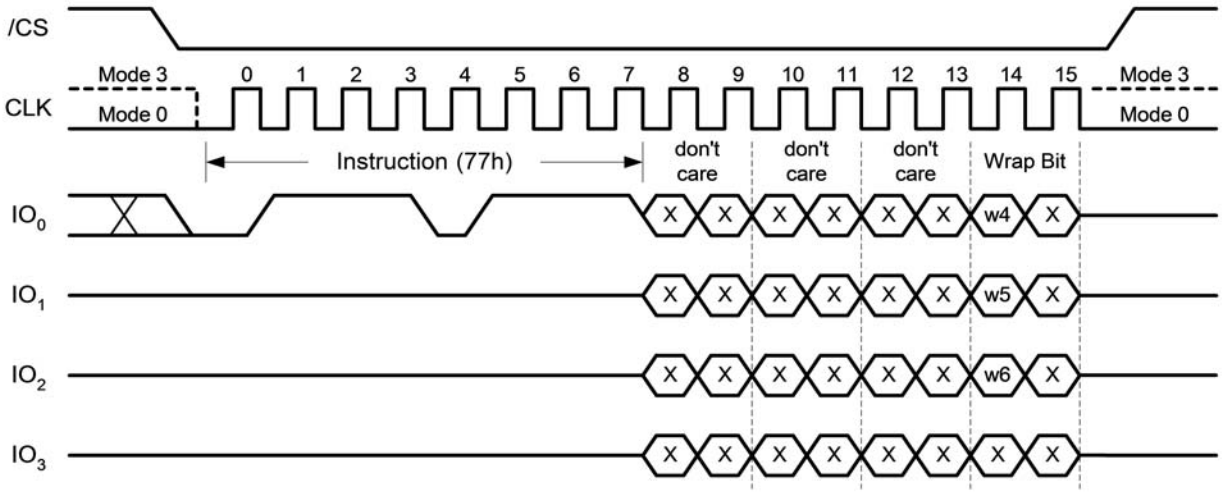


Figure 25: Set Burst With Wrap Instruction (SPI mode only)

7.5.12 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, the Set Read Parameters (C0h) instruction can be used to configure the number of dummy clocks for Fast Read (0Bh), Fast Read Quad I/O (EBh) and Burst Read with Wrap (0Ch) instructions, and to configure the number of bytes of "Wrap Length" for the Burst Read with Wrap (0Ch) instruction.

In Standard SPI mode, the Set Read Parameters (C0h) instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed. Refer to the Instruction Table 1-2 for details. The "Wrap Length" is set by W5-4 bit in the Set Burst with Wrap (77h) instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default "Wrap Length" after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 2. The number of dummy clocks is only programmable for the Fast Read (0Bh), Fast Read Quad I/O (EBh) and Burst Read with Wrap (0Ch) instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again, prior to any 0Bh, EBh or 0Ch instructions.

P5 – P4	DUMMY CLOCKS	MAXIMUM READ FREQUENCY
0 0	Not supported	
0 1	4	50 MHz
1 0	6	80 MHz
1 1	8	104 MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

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Note: 4-bytes address alignment for QPI Read: read address start from A1,A0=0,0

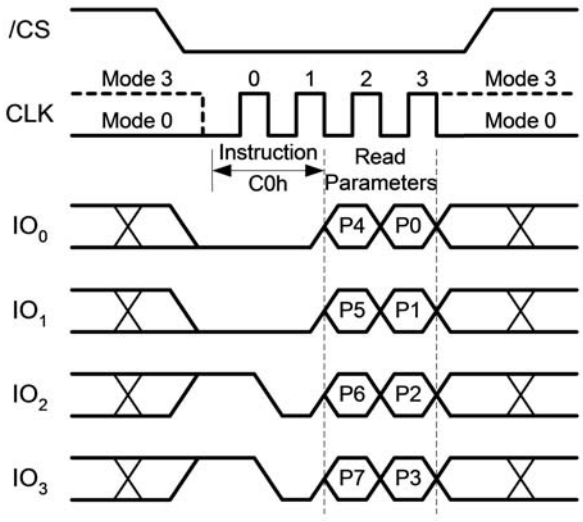


Figure 26: Set Read Parameters Instruction (QPI Mode only)

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7.6 Standard Read Instructions

This section describes standard Flash instructions to read Flash contents:

- Read Data (03h)
- Fast Read (0Bh)
- Fast Read (0Bh) in QPI Mode
- DTR Fast Read (0Dh)
- DTR Fast Read (0Dh) in QPI Mode
- Fast Read Dual Output (3Bh)
- Fast Read Quad Output (6Bh)
- Fast Read Dual I/O (BBh)
- DTR Fast Read Dual I/O (BDh)
- Fast Read Quad I/O (EBh)
- Fast Read Quad I/O (EBh) in QPI Mode
- DTR Fast Read Quad I/O (EDh)
- DTR Fast Read Quad I/O (EDh) in QPI Mode
- Burst Read with Wrap (0Ch)
- DTR Burst Read with Wrap (0Eh)

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7.6.1 Read Data (03h)

This instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin.

The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 27. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY = 1) the instruction is ignored and will not have any effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics Section 9.5).

The Read Data (03h) instruction is supported only in Standard SPI mode.

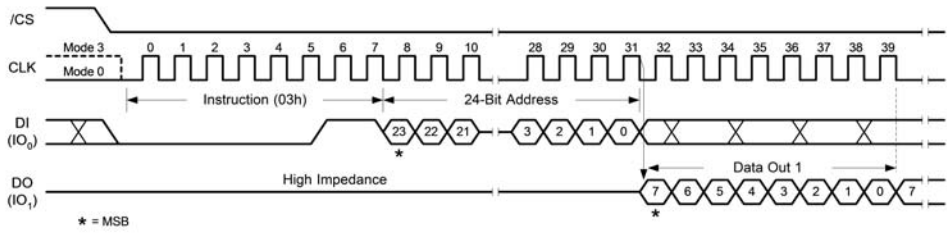


Figure 27: Read Data Instruction (SPI Mode only

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7.6.2 Fast Read (0Bh)

This instruction is similar to the Read Data (03h) instruction except that Fast Read can operate at the highest possible frequency of FR (see AC Electrical Characteristics Section 9.5). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 28. The dummy clocks allow the device’s internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care.”

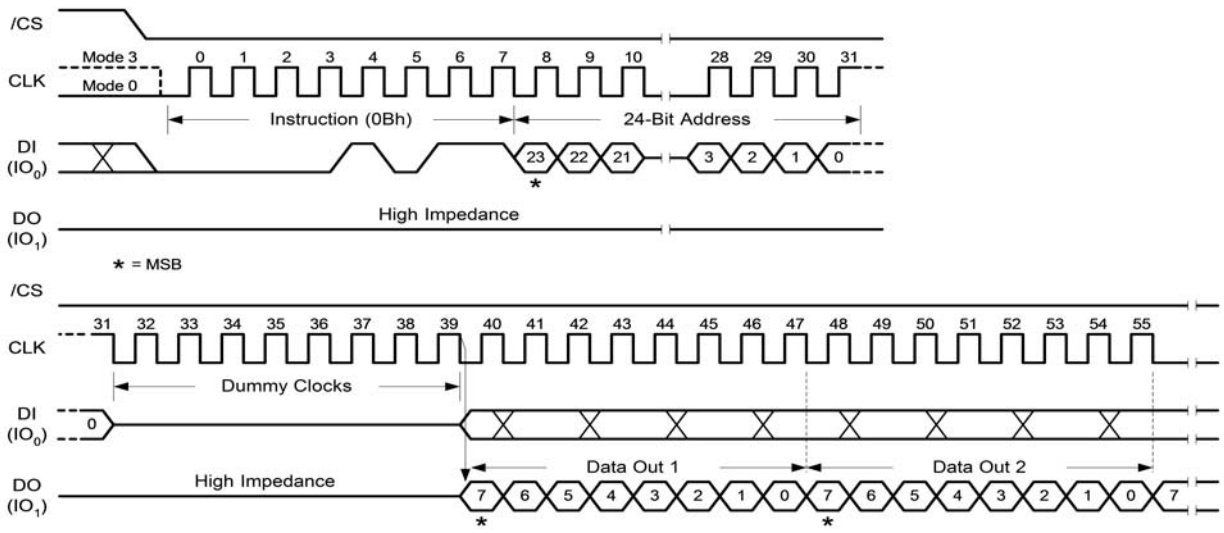


Figure 28: Fast Read Instruction (SPI Mode)

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7.6.3 Fast Read (0Bh) in QPI Mode

This instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6, or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2.

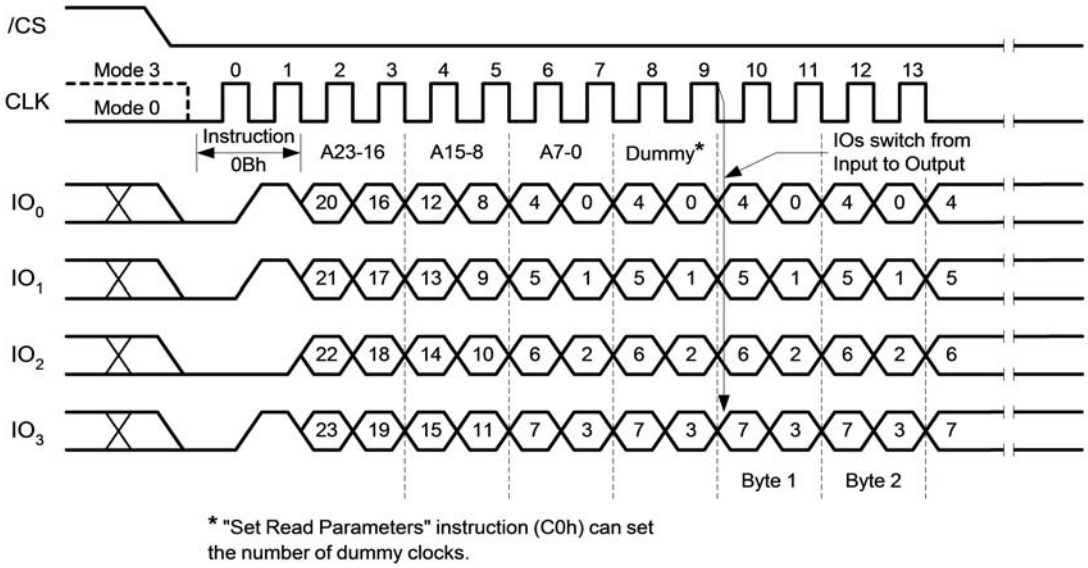


Figure 29: Fast Read Instruction (QPI Mode)

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7.6.4 DTR Fast Read (0Dh)

The DTR Fast Read instruction is similar to the Fast Read (0Bh) instruction except that the 24-bit address input and the data output require Double Transfer Rate (DTR) operation. This is accomplished by adding six/eight “dummy” clocks after the address as shown in Figure 30. The dummy clocks allow the device’s internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

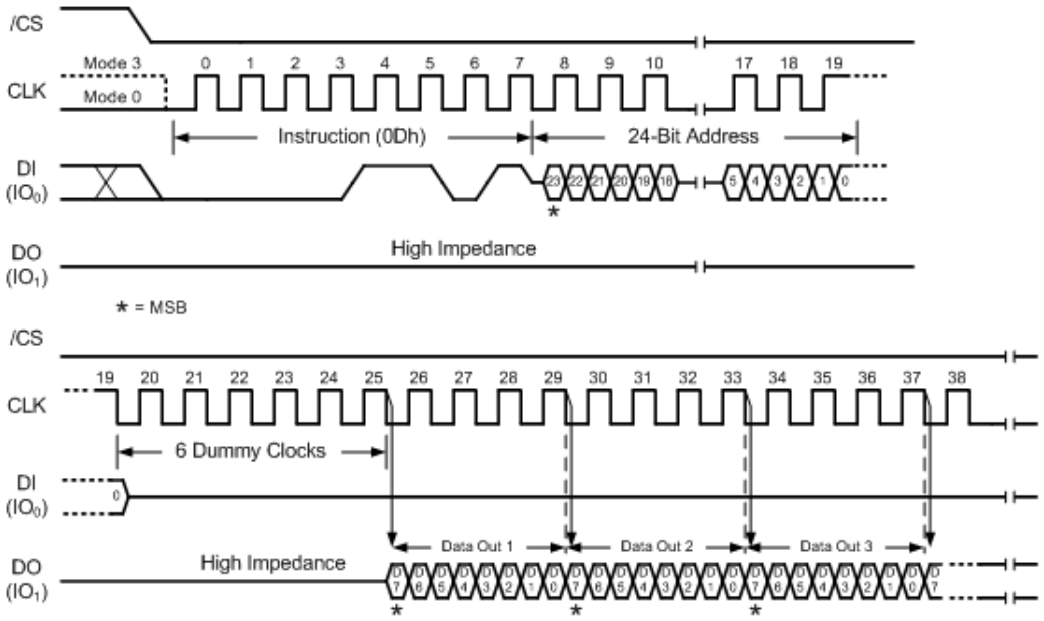


Figure 30: DTR Fast Read Instruction (SPI Mode

7.6.5 DTR Fast Read (0Dh) in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode.

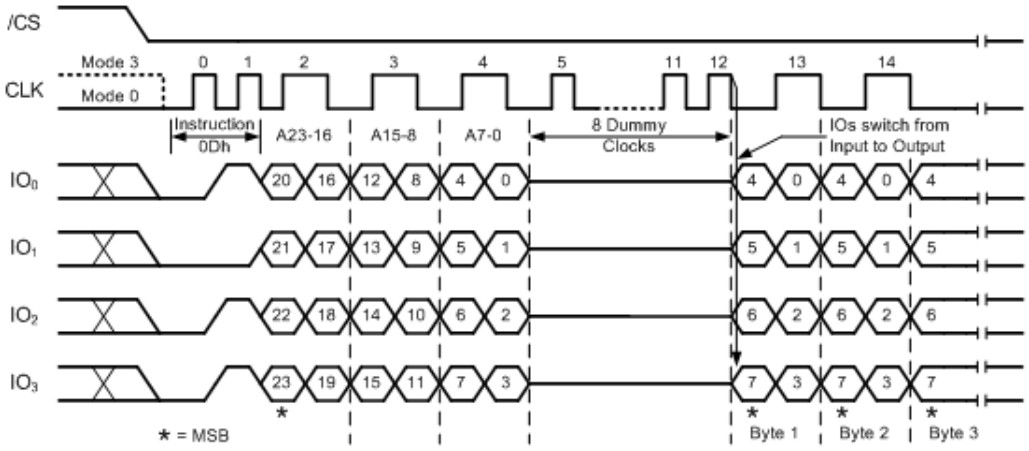


Figure 31: DTR Fast Read Instruction (QPI Mode)

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7.6.6 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output (3Bh) instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics Section 9.5). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 32. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

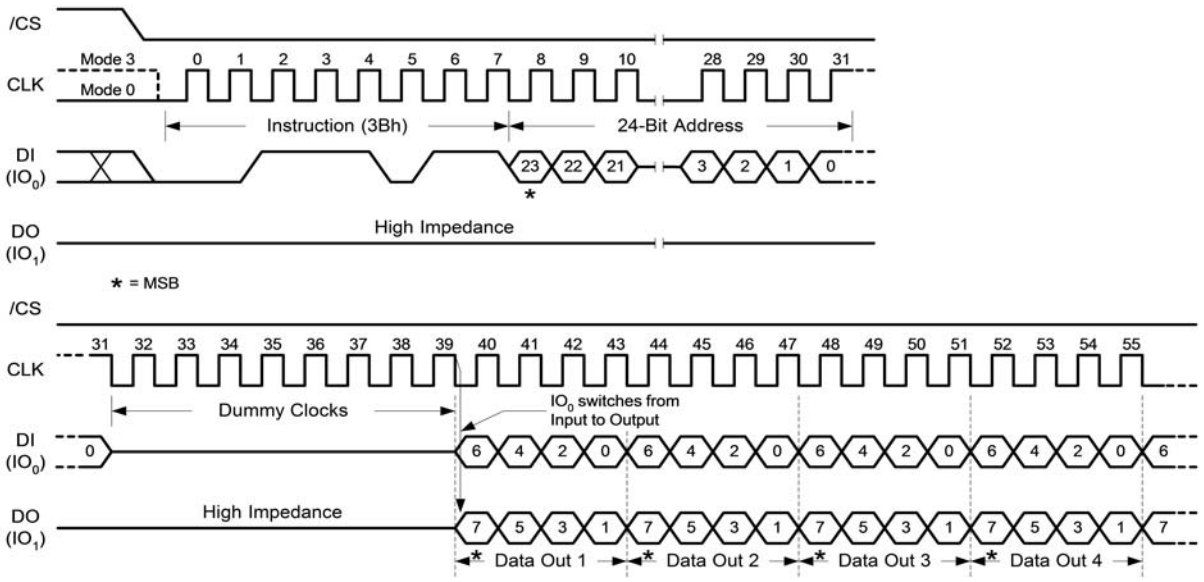


Figure 32: Fast Read Dual Output Instruction (SPI Mode only)

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7.6.7 Fast Read Quad Output (6Bh)

This instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Quad Enable (QE) bit in Status Register 2 (SR2) must be set to 1 before the device will accept this instruction.

The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics Section Section 9.5). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 33. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

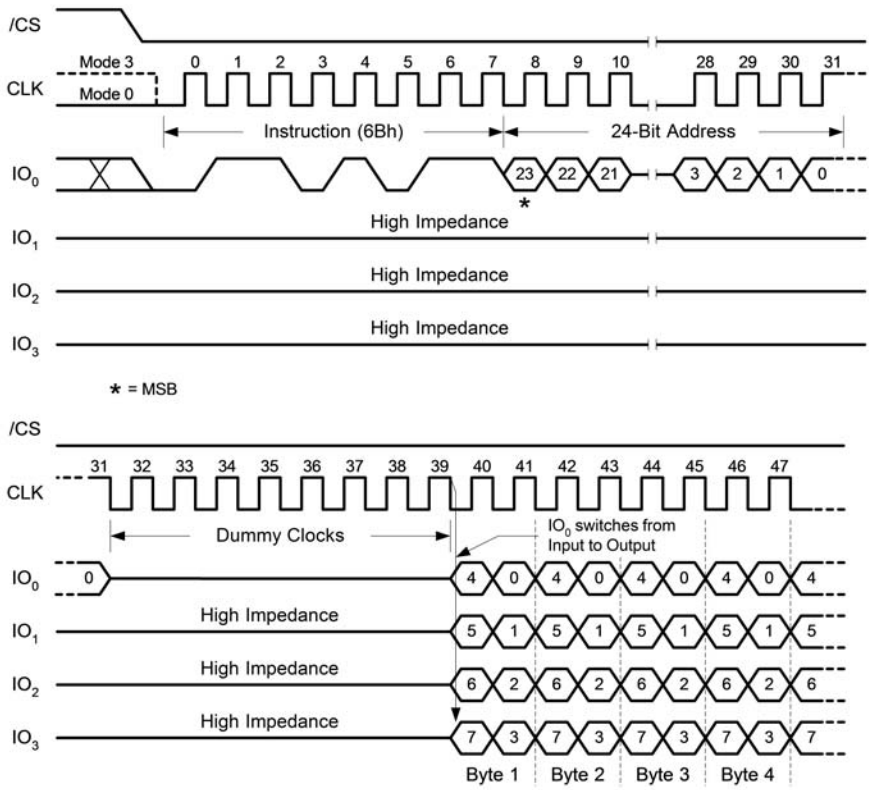


Figure 33: Fast Read Quad Output Instruction (SPI Mode Only))

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7.6.8 Fast Read Dual I/O (BBh)

This instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Similar to the Fast Read Dual Output (3Bh) instruction, the Fast Read Dual I/O instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics Section 9.5). This is accomplished by adding four “dummy” clocks after the 24-bit address as shown in Figure 34 and Figure 35. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO0 pin should be high-impedance prior to the falling edge of the first data out clock.

Fast Read Dual I/O with “Read Command Bypass Mode”

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the “Read Command Bypass Mode” bits (M7-0) after the input Address bits (A23-0), as shown in Figure 34. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don’t care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the “Read Command Bypass Mode” bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 34 and Figure 35. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the “Read Command Bypass Mode” bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

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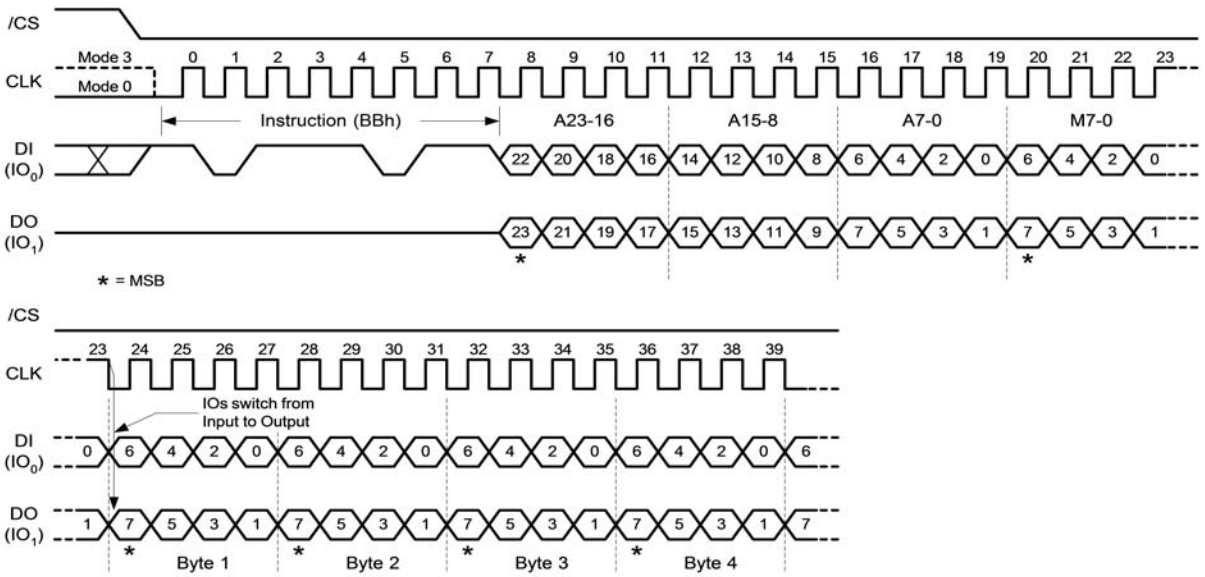


Figure 34: Fast Read Dual I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode Only)

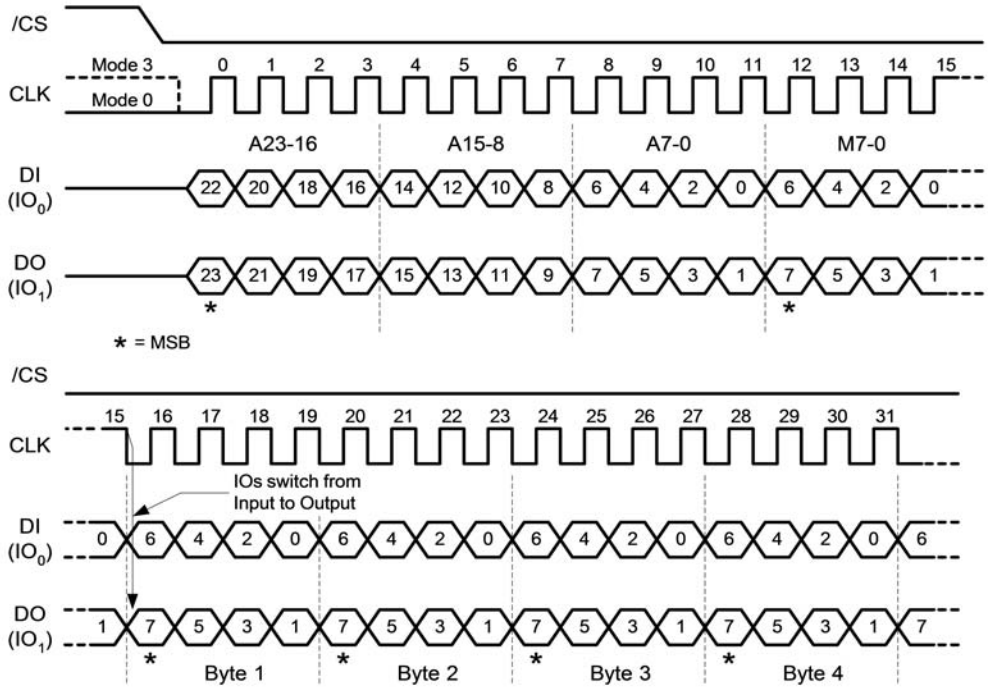


Figure 35: Fast Read Dual I/O Instruction
(Previous instruction set M5-4=10, SPI Mode only, DTR Fast Read Dual I/O (BDh))

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7.6.9 DTR Fast Read Dual I/O (BDh)

This instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

DTR Fast Read Dual I/O with "Read Command Bypass Mode"

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Read Command Bypass Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 36. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Read Command Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 37. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Command Bypass Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh/FFFFFh on IO0 for the next instruction (16/20 clocks), to ensure M4 = 1 and return the device to normal operation.

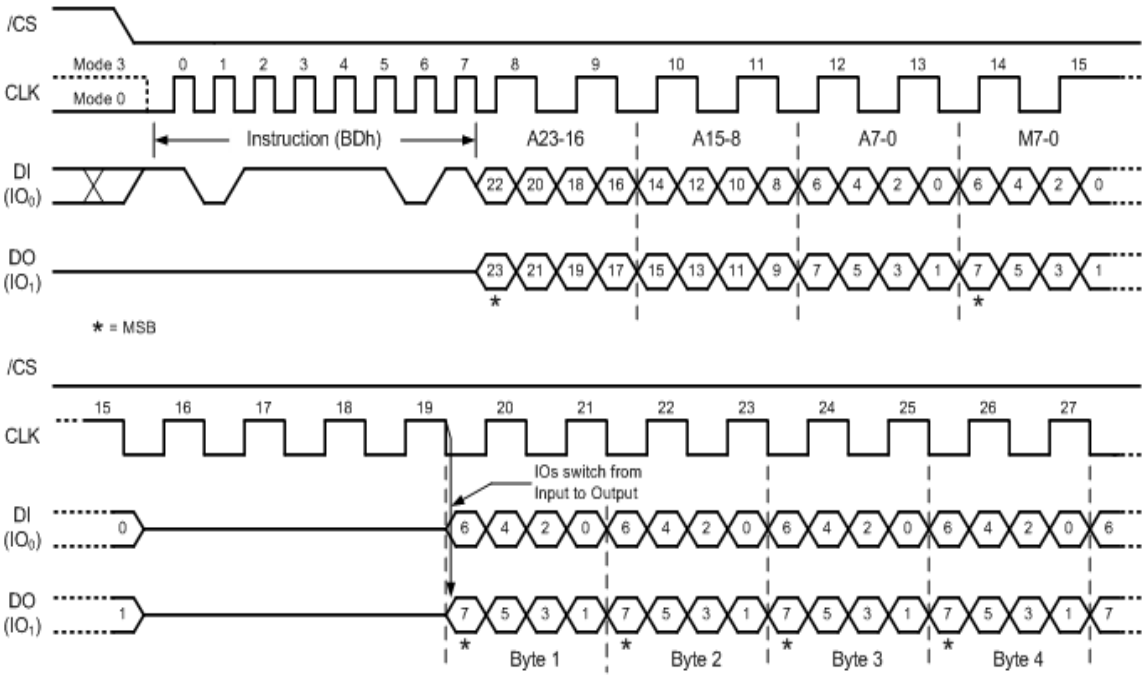


Figure 36: DTR Fast Read Dual I/O (Initial instruction or previous M5-4≠10, SPI Mode Only)

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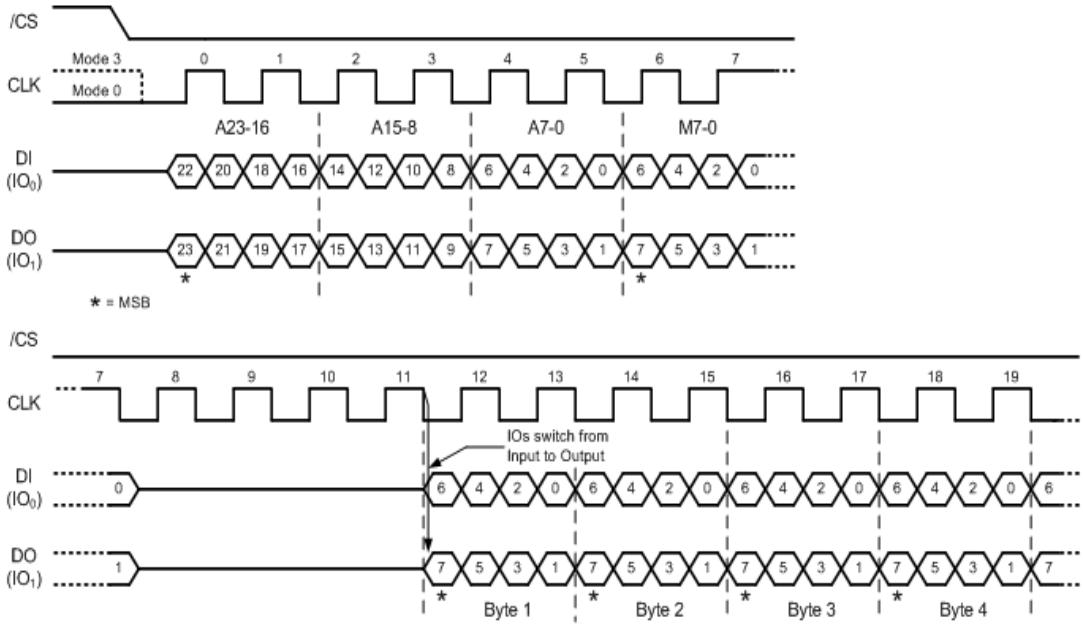


Figure 37: DTR Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode Only)

7.6.10 Fast Read Quad I/O (EBh)

This instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Fast Read Quad I/O with "Read Command Bypass Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Read Command Bypass Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 38. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Read Command Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 39. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Command Bypass Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

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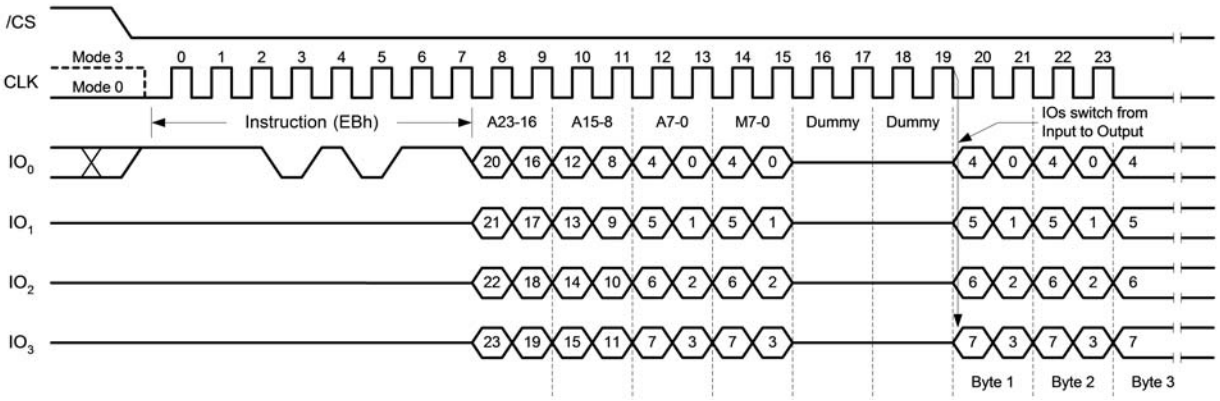


Figure 38: Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

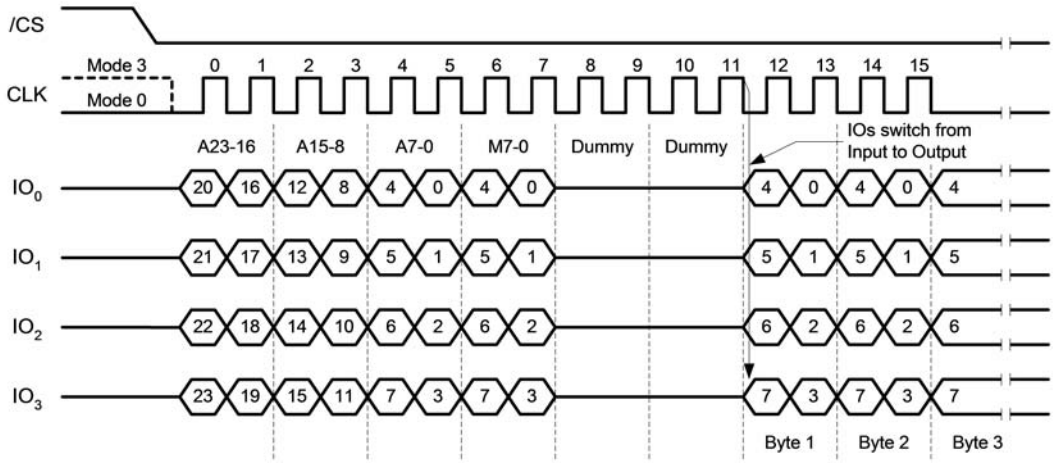


Figure 39: Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI Mode

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-bytes) of data without issuing multiple read commands.

When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32, or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction. Once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Set Burst with Wrap (77h) instruction is used to enable or disable the Wrap function for the following EBh instructions. It configures three "Wrap Bits" (W6-4). The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to Section 7.5.11 for a detailed description.

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7.6.11 Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O (EBh) instruction is also supported in QPI mode, as shown in Figure 40.

When QPI mode is enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6, or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2.

"Read Command Bypass Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Refer to the description on previous pages. In QPI mode, the "Read Command Bypass Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Read Command Bypass Mode bits immediately.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, the dedicated Burst Read with Wrap (0Ch) instruction must be used.

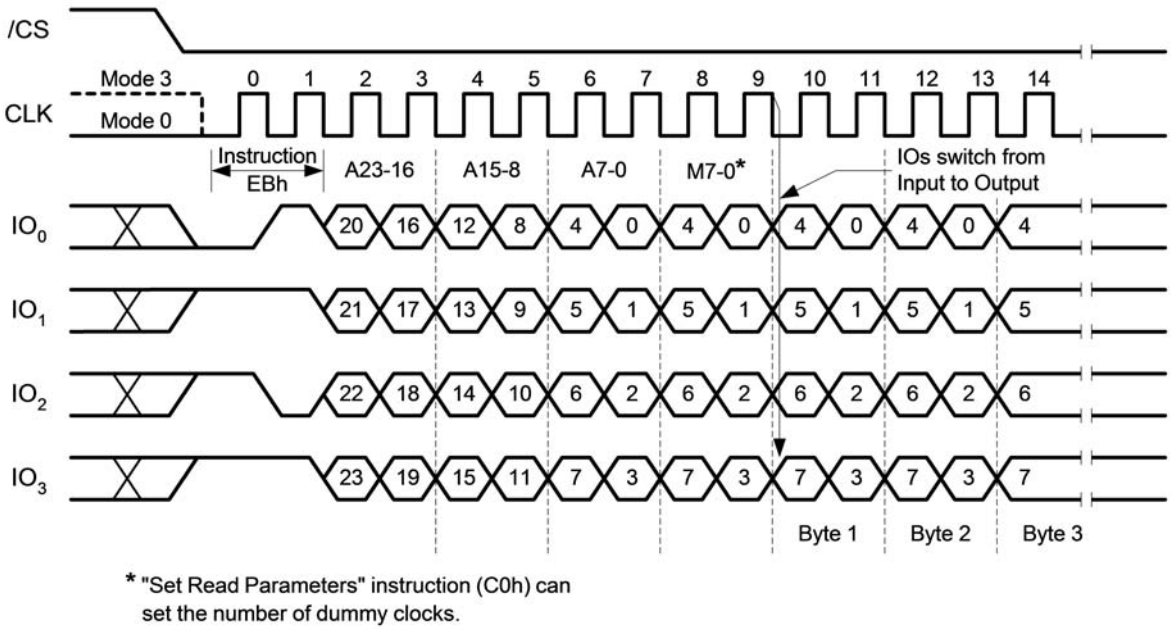


Figure 40: Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, QPI Mode)

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7.6.12 DTR Fast Read Quad I/O (EDh)

This instruction is similar to the Fast Read Quad I/O (EBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable this instruction.

DTR Fast Read Quad I/O with "Read Command Bypass Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Read Command Bypass Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 41. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Read Command Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 42. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Command Bypass Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh/3FFh on IO0 for the next instruction (8/10 clocks), to ensure M4 = 1 and return the device to normal operation.

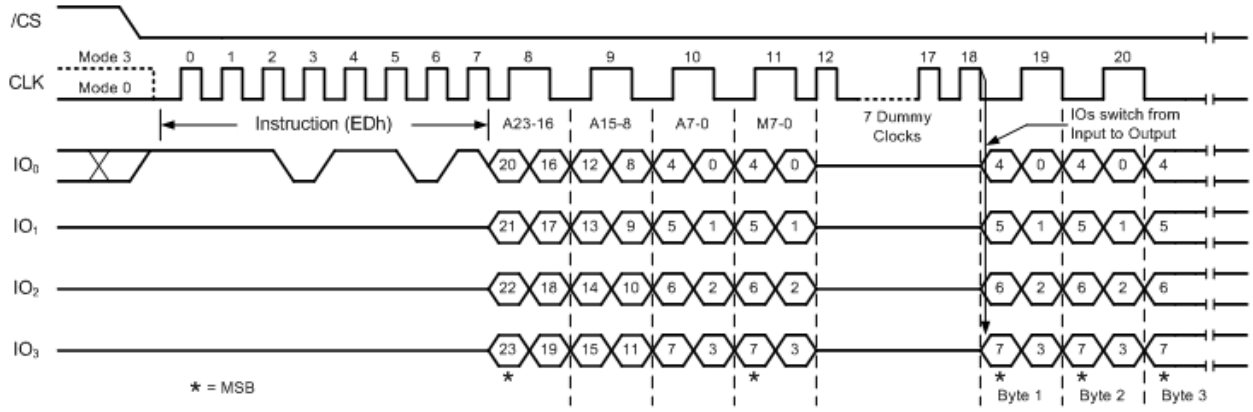


Figure 41: DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, SPI Mode)

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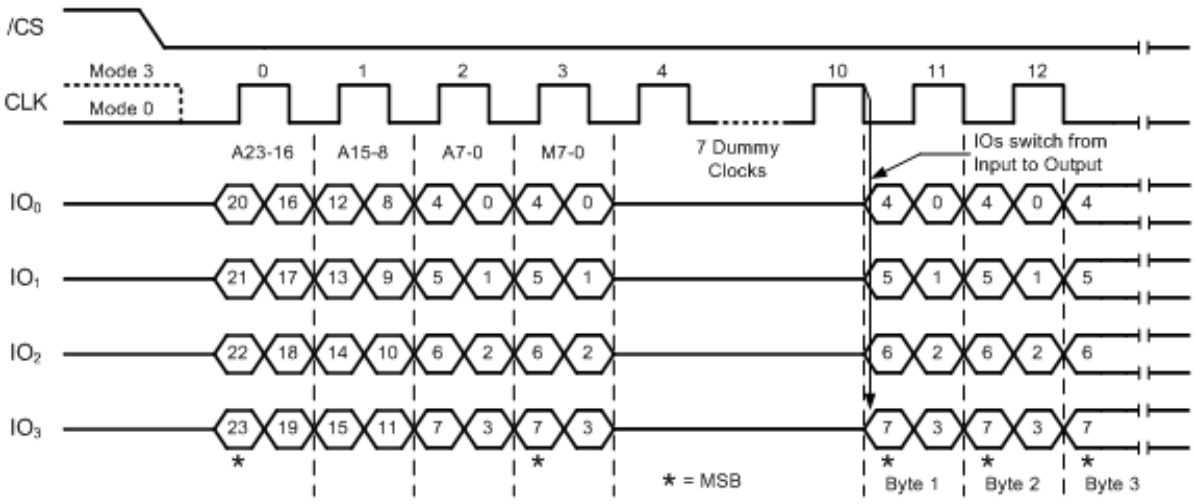


Figure 42: Fast Read Quad I/O (Previous instruction set M5-4=10, SPI Mode)

DTR Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI Mode

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32, or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The "Set Burst with Wrap (77h) instruction is used to enable or disable the Wrap function for the following EBh instructions. It configures three "Wrap Bits" (W6-4). The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to Section 7.5.11 for a detailed description.

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7.6.13 DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O (EDh) instruction is also supported in QPI mode, as shown in Figure 43.

"Read Command Bypass Mode" feature is also available in QPI mode for DTR Fast Read Quad I/O instruction. Refer to the description on previous pages. In QPI mode, the "Read Command Bypass Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Read Command Bypass Mode bits immediately.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, the dedicated DTR Burst Read with Wrap (0Eh) instruction must be used.

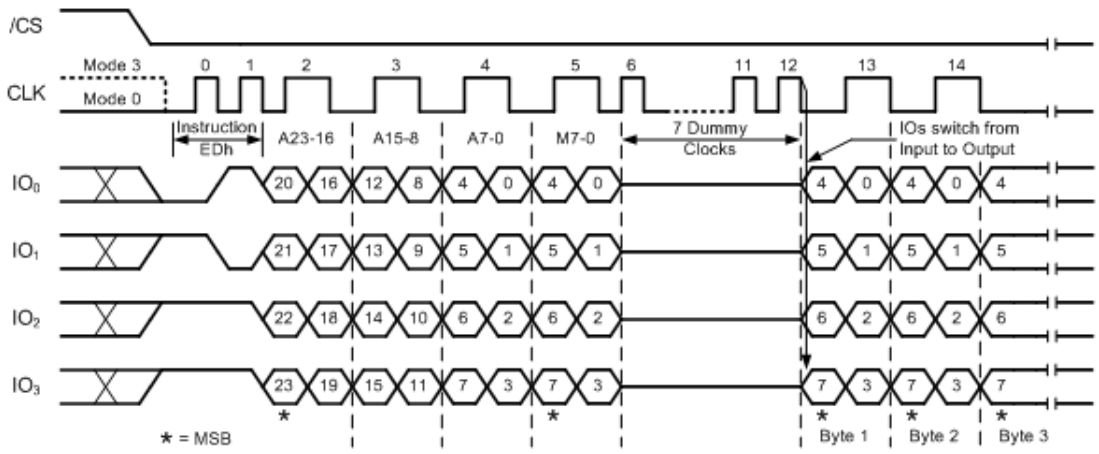


Figure 43: DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)

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7.6.14 Burst Read with Wrap (0Ch)

This instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode.

The instruction is similar to the Fast Read (0Bh) in QPI Mode instruction, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the Set Read Parameters (C0h) instruction.

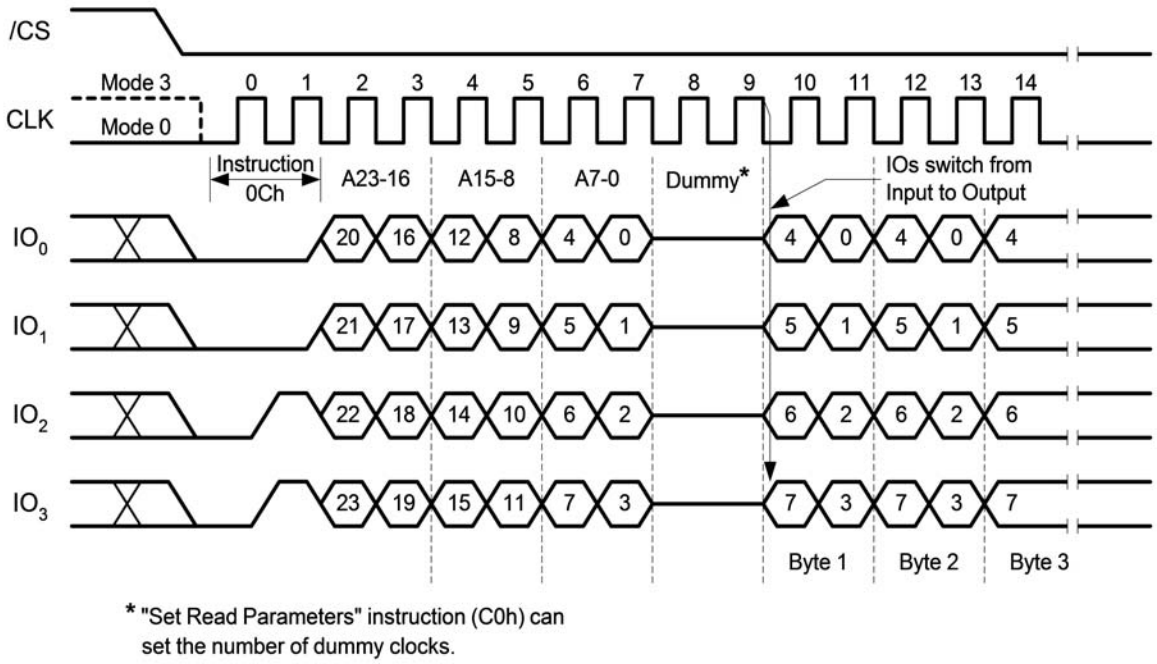


Figure 44: Burst Read with Wrap Instruction (QPI Mode Only)

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7.6.15 DTR Burst Read with Wrap (0Eh)

This instruction is similar to the Burst Read with Wrap (0Ch) instruction, except for the instruction format which is in DTR mode as describe in Figure 45.

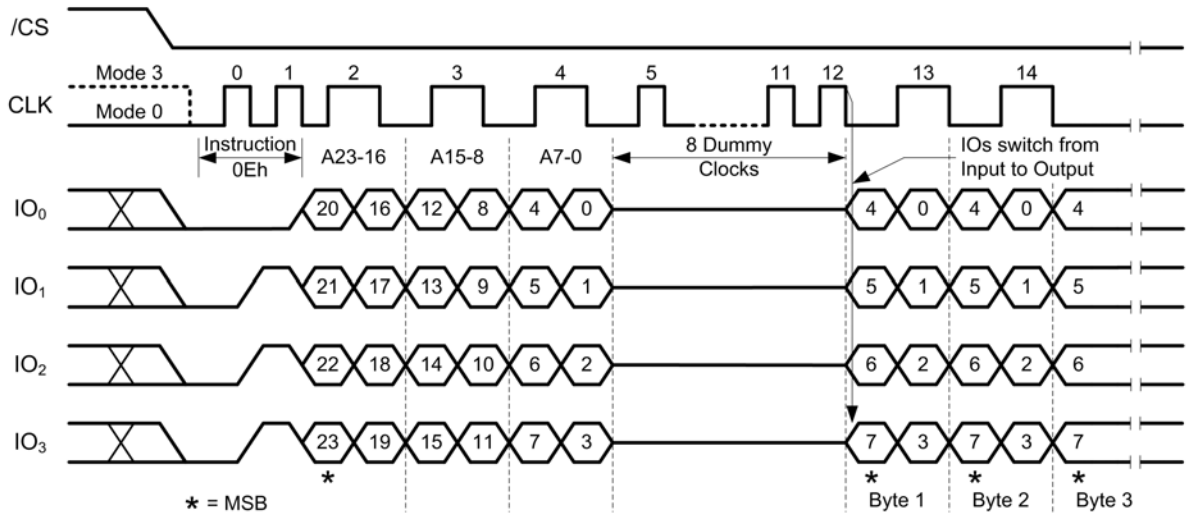


Figure 45: DTR Burst Read with Wrap Instruction (QPI Mode only)

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7.7 Standard Write Instructions

This section describes standard Flash instructions to modify Flash contents (program and erase):

- Page Program (02h)
- Quad Input Page Program (32h)
- Sector Erase (20h)
- 32KB Block Erase (52h)
- 64KB Block Erase (D8h)
- Chip Erase (C7h/60h)
- Erase/Program Suspend (75h)
- Erase/Program Resume (7Ah)

Refer also to these instructions:

- Write Enable (06h)
- Write Disable (04h)
- Individual Block/Sector Lock (36h)
- Individual Block/Sector Unlock (39h)
- Global Block/Sector Lock (7Eh)
- Global Block/Sector Unlock (98h)

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7.7.1 Page Program (02h)

This instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations.

A Write Enable (06h) instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL = 1).

The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24/32-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 46 and Figure 47.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Page Program instruction will not be executed.

After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (see AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction (see Section 7.5.4) may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

The Page Program instruction is not executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/ Sector Locks.

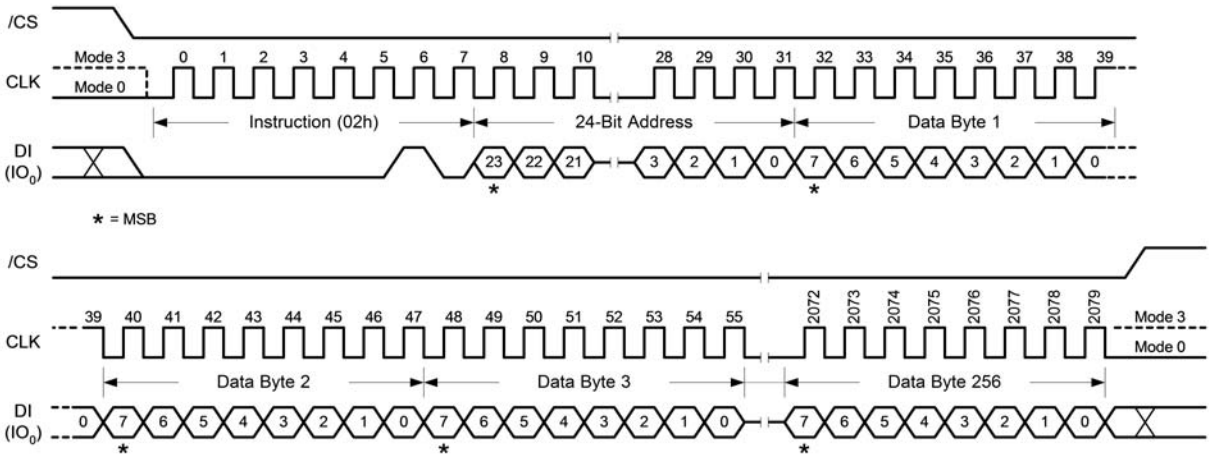


Figure 46: Page Program Instruction (SPI Mode))

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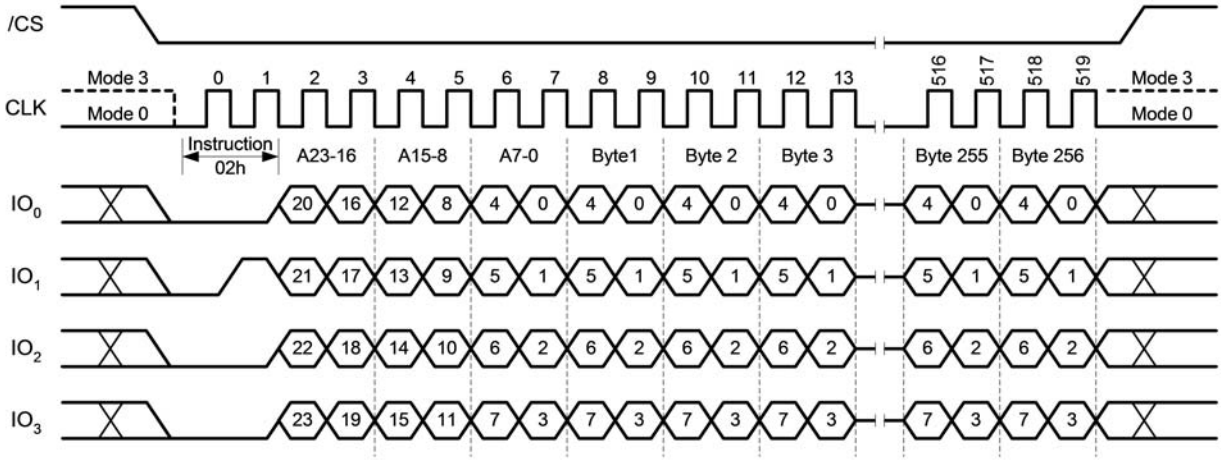


Figure 47: Page Program Instruction (QPI Mode))

7.7.2 Quad Input Page Program (32h)

This instruction is similar to the Page Program (02h) instruction, except that address and data are input using four pins: IO_0, IO_1, IO_2, and IO_3. It allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations.

The Quad Input Page Program improves programming performance for applications that have slow SPI clock speeds (<5MHz), where the SPI transaction takes a significant amount of time. Systems with faster clock speed will see only a small benefit for the Quad Input Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Input Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable (06h) instruction must be executed before the device will accept the Quad Input Page Program instruction (Status Register-1, WEL=1).

The instruction is initiated by driving the /CS pin low then shifting the instruction code “32h” followed by a 24/32-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

The Quad Input Page Program instruction is not executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

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The Quad Page Input Program instruction sequence is shown in Figure 48.

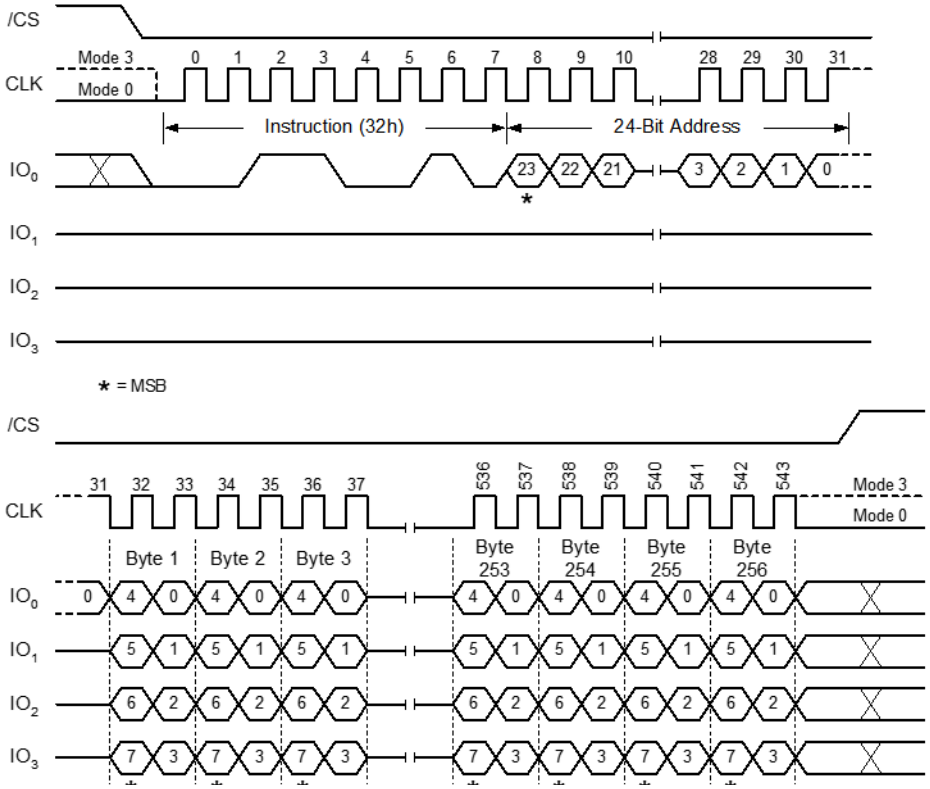


Figure 48: Quad Input Page Program Instruction (SPI Mode only))

7.7.3 Sector Erase (20h)

This instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable (06h) instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24/32-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in Figure 49 and Figure 50.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (see AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction (see Section 7.5.4) may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

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The Sector Erase instruction is not executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.)

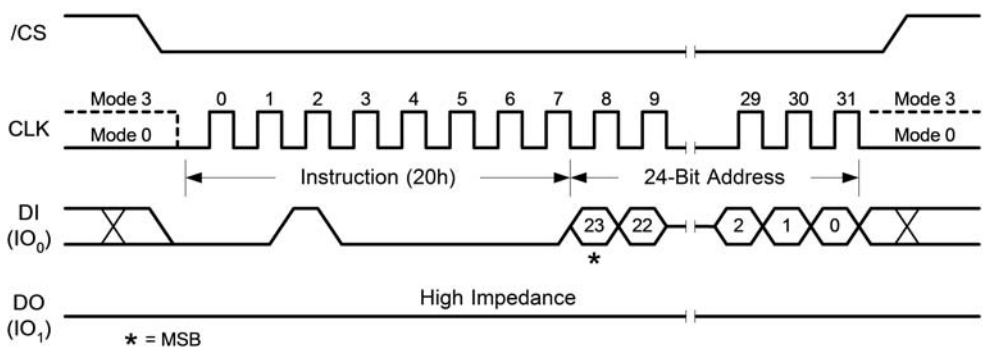


Figure 49: Sector Erase Instruction (SPI Mode)

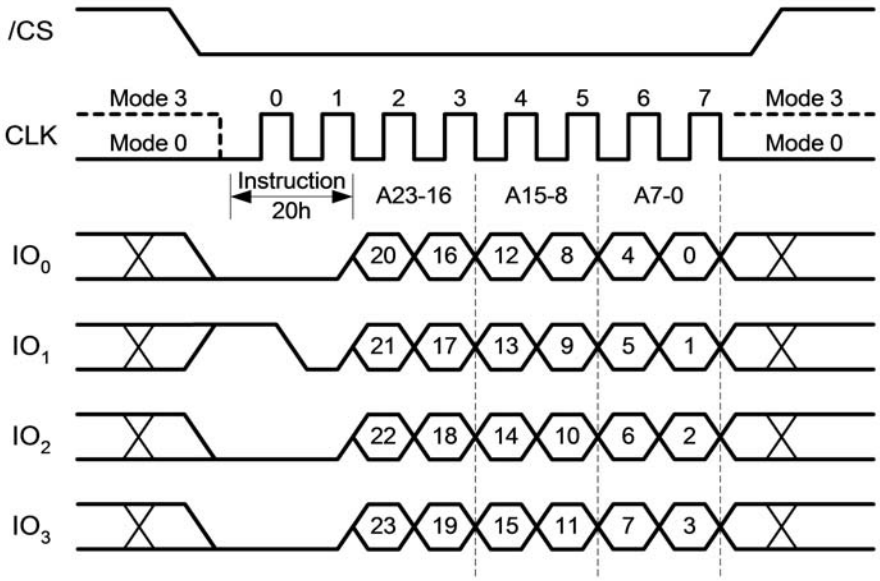


Figure 50: Sector Erase Instruction (QPI Mode)

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7.7.4 32KB Block Erase (52h)

This instruction sets all memory within a specified block (32 Kb) to the erased state of all 1s (FFh). A Write Enable (06h) instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1).

The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed by a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 51 and Figure 52.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Block Erase instruction is not executed. After /CS is driven high, the self-timed Block Erase instruction commences for a time duration of t_{BE1} (see AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction (see Section 7.5.4) may still be accessed for checking the status of the BUSY bit. The BUSY bit is 1 during the Block Erase cycle and becomes 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

The Block Erase instruction is not executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

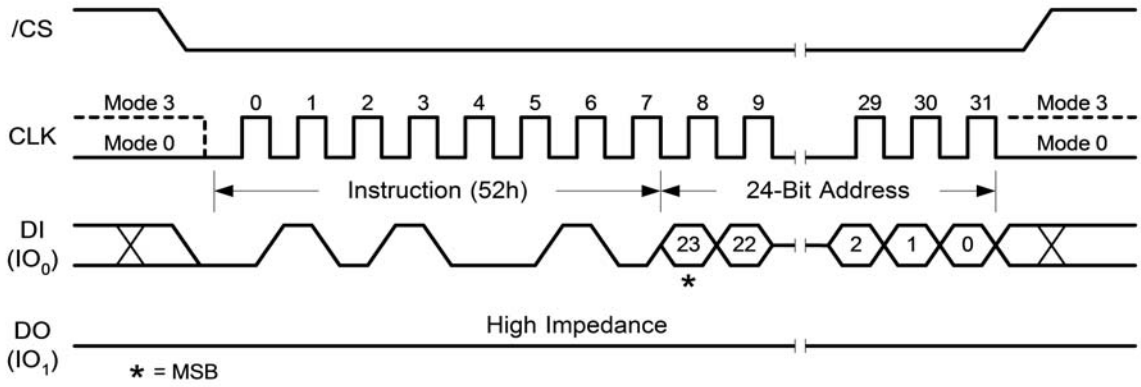


Figure 51: 32KB Block Erase Instruction (SPI Mode))

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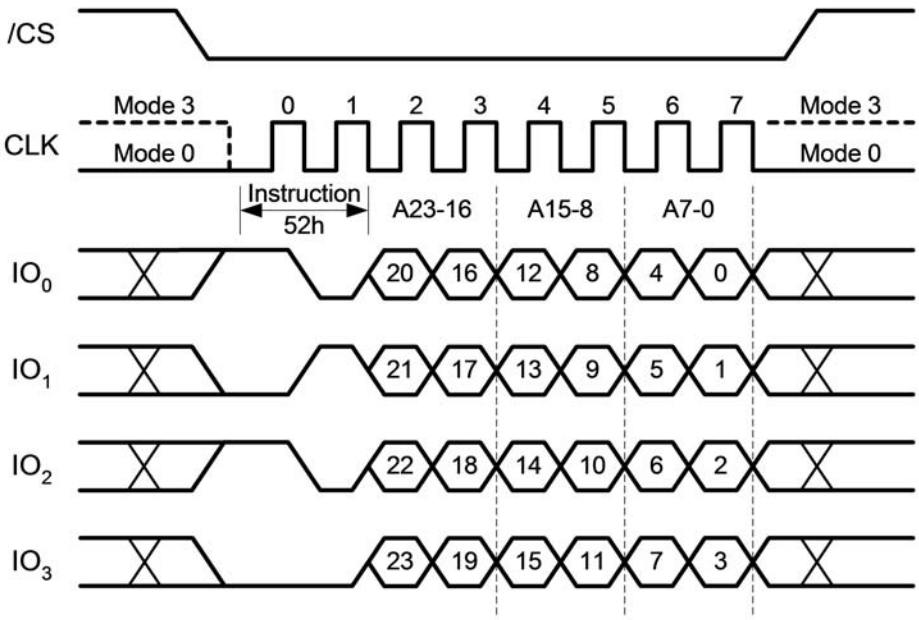


Figure 52: 32KB Block Erase Instruction (QPI Mode))

7.7.5 64KB Block Erase (D8h)

This instruction sets all memory within a specified block (64 Kbytes) to the erased state of all 1s (FFh). A Write Enable (06h) instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1).

The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed by a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 53 and Figure 54.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (see AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction (see Section 7.5.4) may still be accessed for checking the status of the BUSY bit. The BUSY bit is 1 during the Block Erase cycle and becomes 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or by the Individual Block/ Sector Locks.

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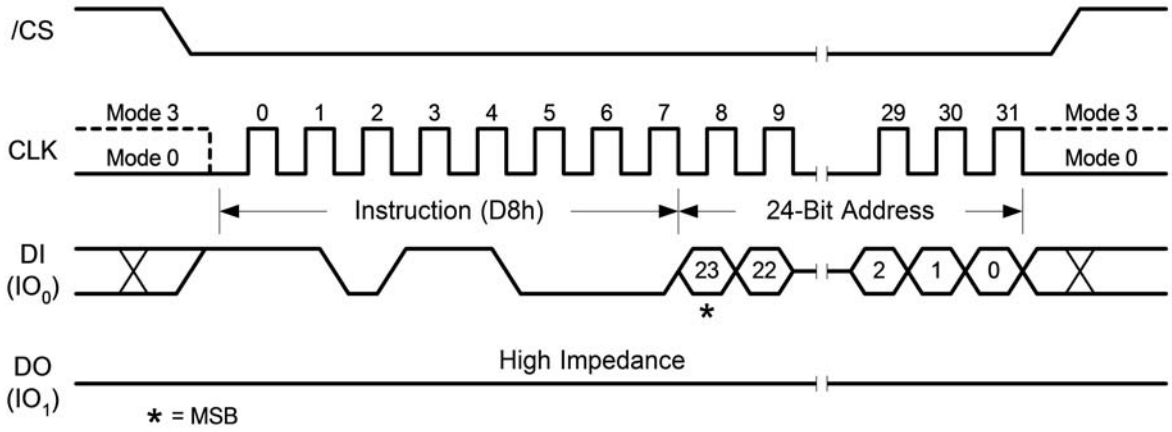


Figure 53: 64KB Block Erase Instruction (SPI Mode))

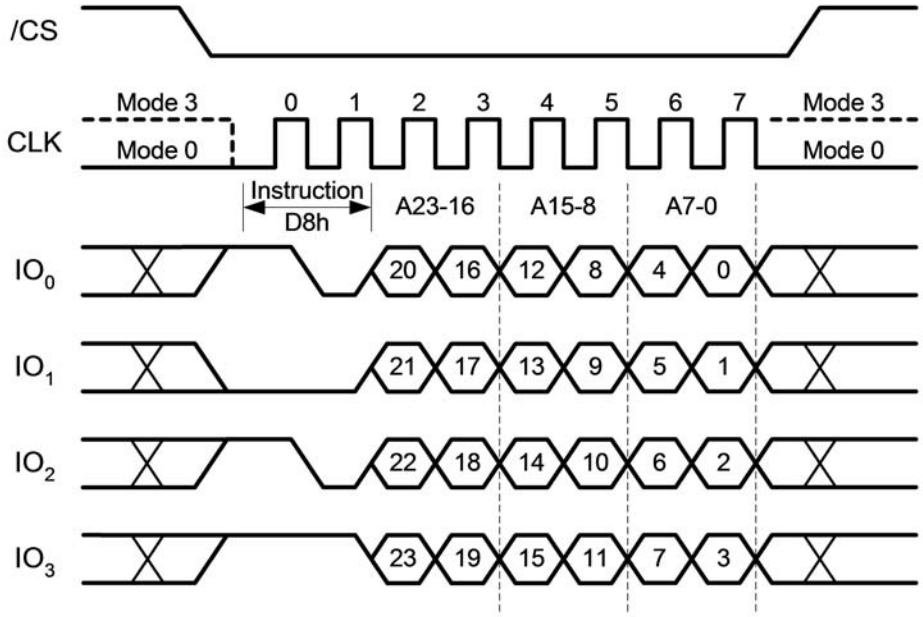


Figure 54: 64KB Block Erase Instruction (QPI Mode))

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7.7.6 Chip Erase (C7h/60h)

This instruction sets all memory within the device to the erased state of all 1s (FFh). The command is mapped to Erase Section-0 (regardless of the Fallback function), and is subject to legacy write protection mechanisms as well as to security policies affecting Section-0.

Note: This legacy instruction is deprecated and replaced by the Secure FORMAT and SFORMAT commands, and should not be used in new applications.

A Write Enable (06h) instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1).

The instruction is initiated by driving the /CS pin low and shifting the instruction code "C7h" or "60h". The Chip Erase instruction sequence is shown in Figure 55.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done, the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (see AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register (see Section 7.5.4) instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is 1 during the Chip Erase cycle and becomes 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/ Sector Locks.

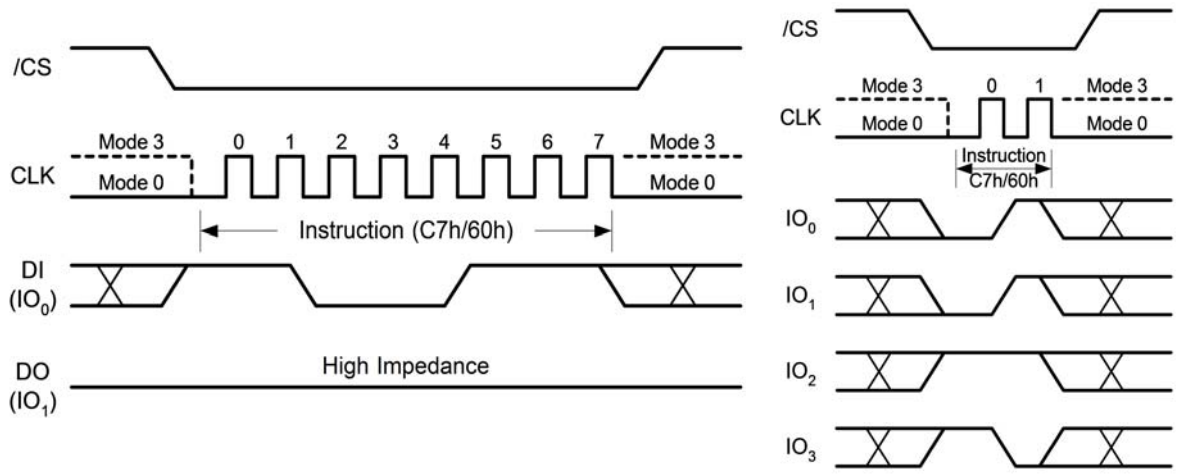


Figure 55: Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)

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7.7.7 Erase/Program Suspend (75h)

This instruction allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 56 and Figure 57.

- Program Suspend is valid only during the Page Program or Quad Page Program operation.
- Write Status Register and Page Program instructions are not allowed during Program Suspend.
- Erase Suspend is valid only during the Sector or Block erase operation. If received during the Chip Erase (C7h/60h) operation, the Erase Suspend instruction is ignored.
- The Write Status Register instructions (Section 7.5.5) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend.

The Erase/Program Suspend instruction (75h) will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device.

A maximum of time of "t_{SUS}" (see AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within "t_{SUS}" and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction "75h" is not issued earlier than a minimum of time of "t_{SUS}" following the preceding Resume instruction "7Ah".

An unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. The SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state. Note that once the Suspend instruction (75h) is accepted, the following Power-Down (B9h) is ignored.

Note: Secure operations are atomic and cannot be suspended. Secure operations are not allowed when another operation is suspended.

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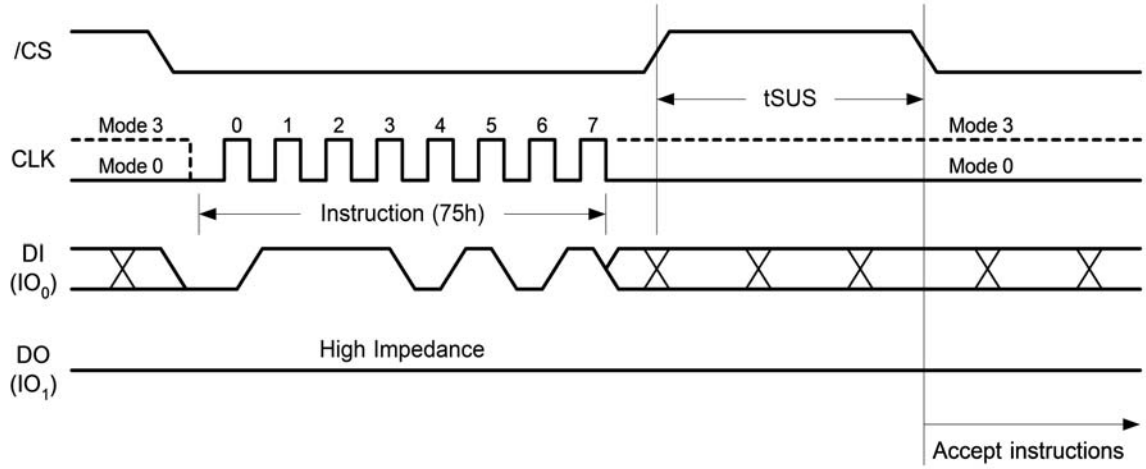


Figure 56: Erase/Program Suspend Instruction (SPI Mode)

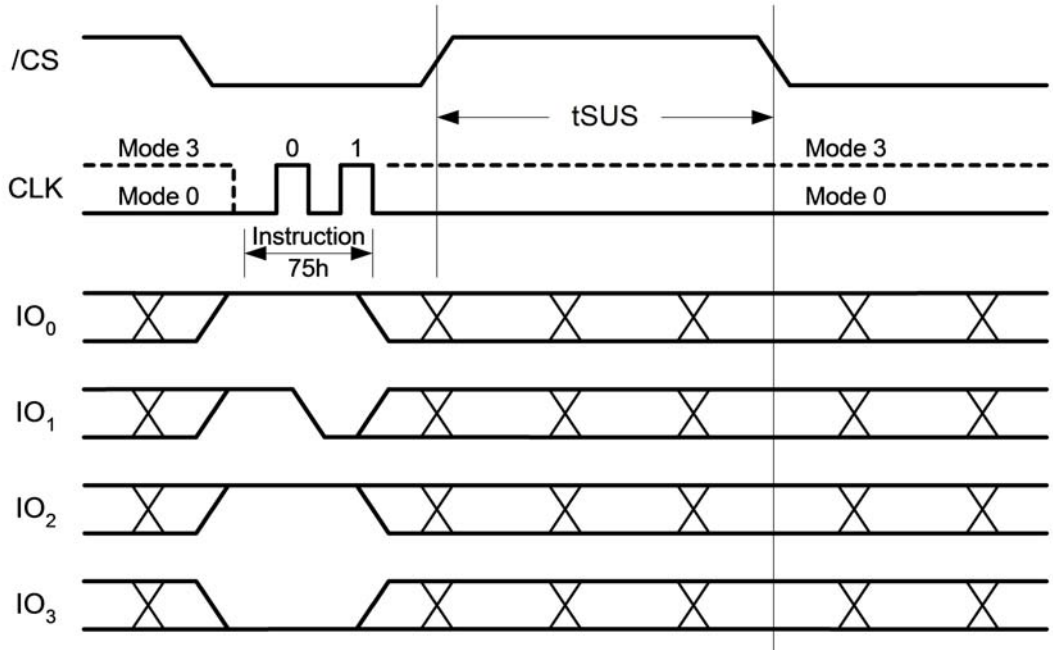


Figure 57: Erase/Program Suspend Instruction (QPI Mode)

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7.7.8 Erase/Program Resume (7Ah)

This instruction must be written to resume a Sector or Block Erase operation, or a Page Program operation after an Erase/Program Suspend (75h).

The Resume instruction is accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0.

After the Resume instruction has been issued the SUS bit is cleared from 1 to 0 immediately, the BUSY bit is set from 0 to 1 within 200 ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 58 and Figure 59.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/ Program Suspend instruction not to be issued within a minimum of time of “t_{SUS}” following a previous Resume instruction.

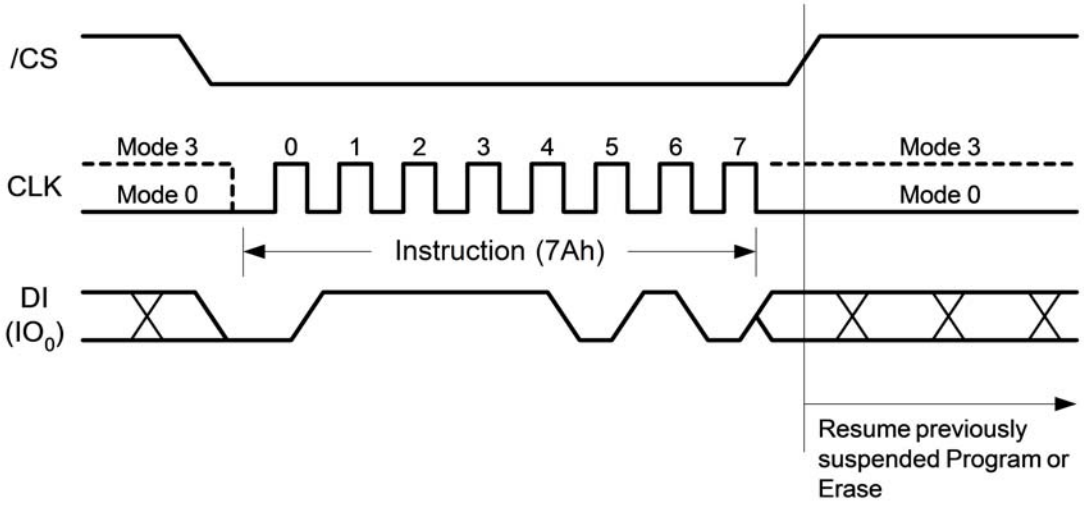


Figure 58: Erase/Program Resume Instruction (SPI Mode)

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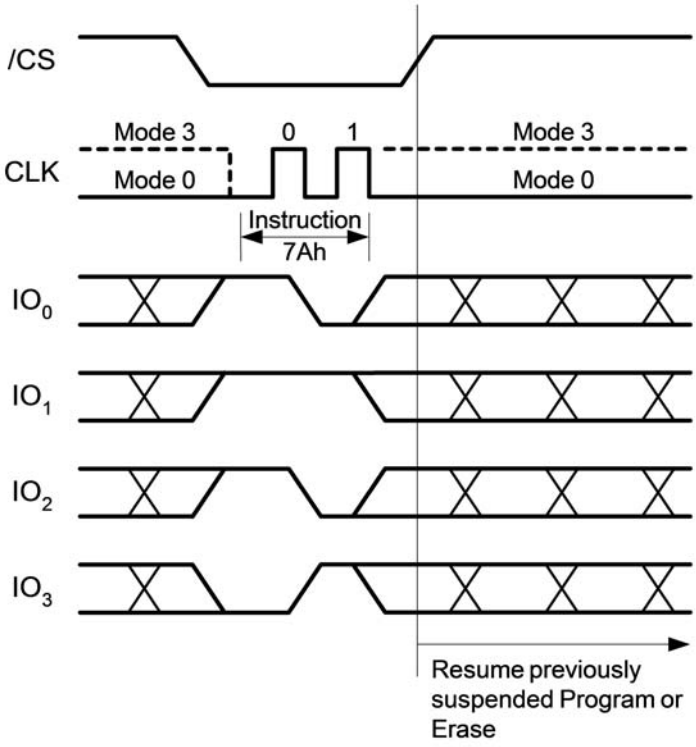


Figure 59: Erase/Program Resume Instruction (QPI Mode)

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7.8 Standard Auxiliary Instructions

This section describes standard Flash instructions to perform auxiliary device functions:

- Power-Down (B9h)
- Release Power-Down/Device ID (ABh)
- Read Manufacturer/Device ID (90h)
- Read Manufacturer/Device ID Dual I/O (92h)
- Read Manufacturer/Device ID Quad I/O (94h)
- Read Unique ID Number (4Bh)
- Read JEDEC ID (9Fh)
- Read SFDP Register (5Ah)
- Erase Security Register (44h)
- Program Security Register (42h)
- Read Security Register (48h)
- Enter QPI Mode (38h)
- Exit QPI Mode (FFh)
- Enable Reset (66h) and Reset Device (99h)
- Write Extended Address Register (C5h)

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7.8.1 Power-Down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-Down instruction. The lower power consumption makes the Power-Down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics).

The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in Figure 60 and Figure 61.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done, the Power-Down instruction will not be executed. After /CS is driven high, the power-down state will be entered within the time duration of t_{DP} (See AC Characteristics).

While in the power-down state, only the Release Power-Down/Device ID (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction (see Section 7.5.4), which is always available during normal operation. Ignoring all but one instruction makes the power-down state a useful condition for securing maximum write protection.

The device always powers-up in the normal operation with the standby current of ICC1. After the Power-Down instruction is accepted, the device will lose all the current volatile Status Register bits. Refer to Section 8.2.

Notes:

- When entering power-down state, the active Session is terminated and all access privileges are revoked. After returning to power-up state, you must use SESSION_OPEN or INIT_SECTION_PA instructions to regain access privileges to required Sections.
- Integrity verification status of each Section is maintained through the power-down state (no need to verify Section integrity again after power-down).
- Once the Erase/Program Suspend (75h) instruction, is accepted, the following Power-Down instruction (B9h) will be ignored.

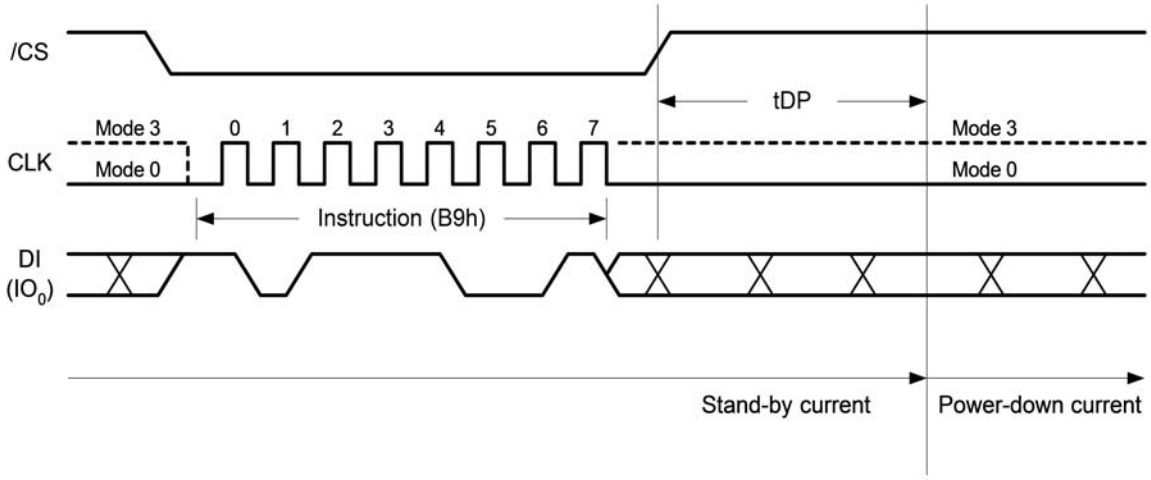


Figure 60: Deep Power-Down Instruction (SPI Mode)

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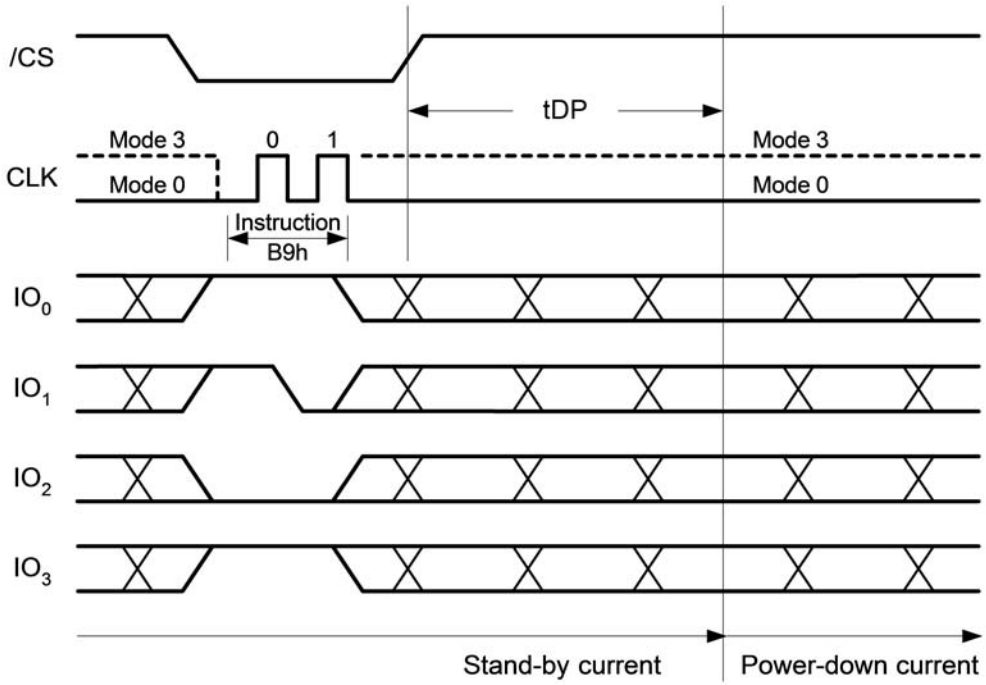


Figure 61: Deep Power-Down Instruction (QPI Mode)

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7.8.2 Release Power-Down/Device ID (ABh)

This instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or to obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in Figure 62, Figure 63, Figure 64, and Figure 65. Release of power-down takes the time duration of t_{RES1} (See AC Characteristics) before the device resumes normal operation and other instructions are accepted. The /CS pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID value for the W77Q32JW/W77Q16JW is listed in the Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

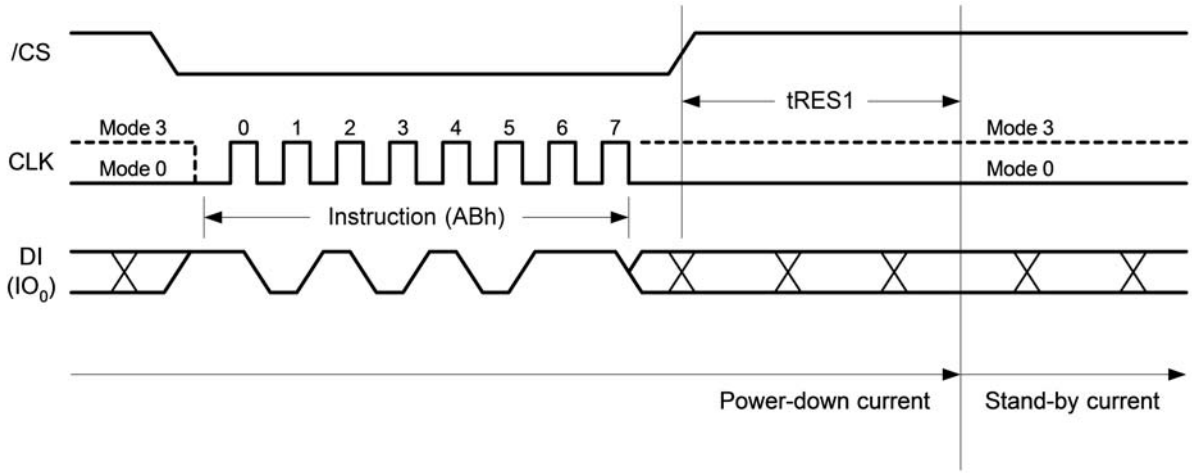


Figure 62: Release Power-Down Instruction (SPI Mode)

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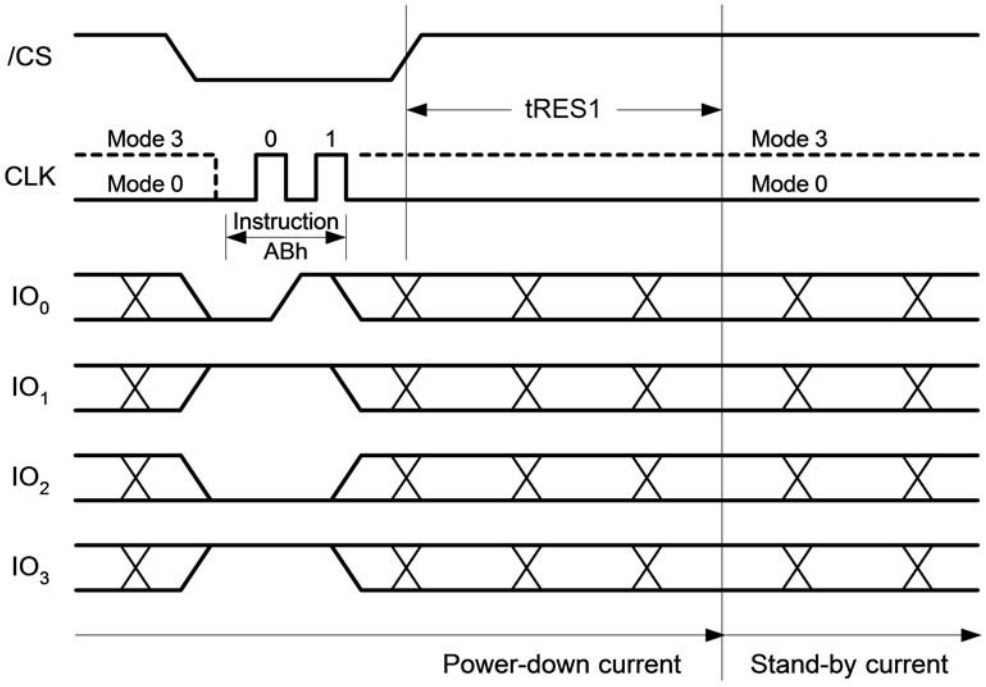


Figure 63: Release Power-Down Instruction (QPI Mode)

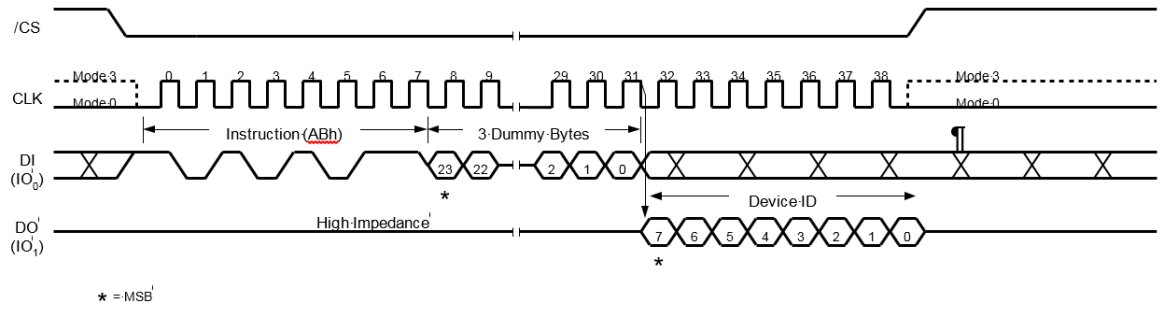


Figure 64: Device ID Instruction (SPI Mode)

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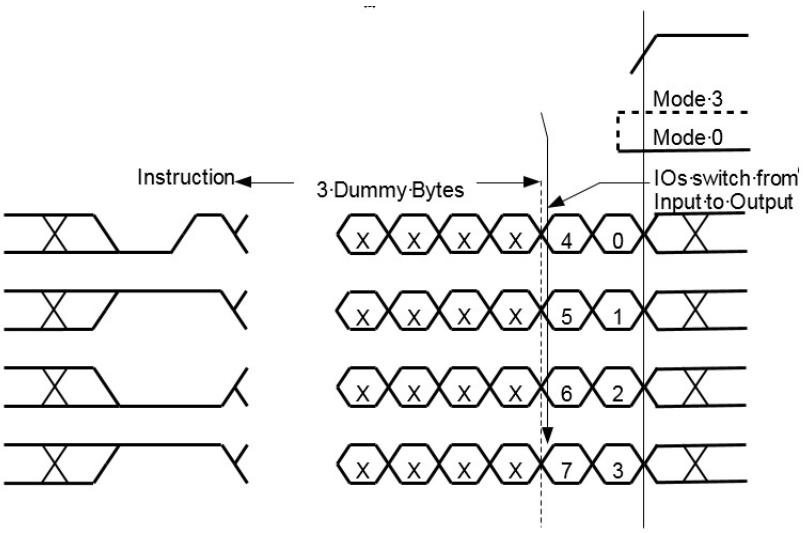


Figure 65: Device ID Instruction (QPI Mode)

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7.8.3 Read Manufacturer/Device ID (90h)

This instruction is an alternative to the Release Power-Down/Device ID (ABh) instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release Power-Down/Device ID (ABh) instruction.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 66. The Device ID values for the device are listed in Section 7.3. The instruction is completed by driving /CS high.

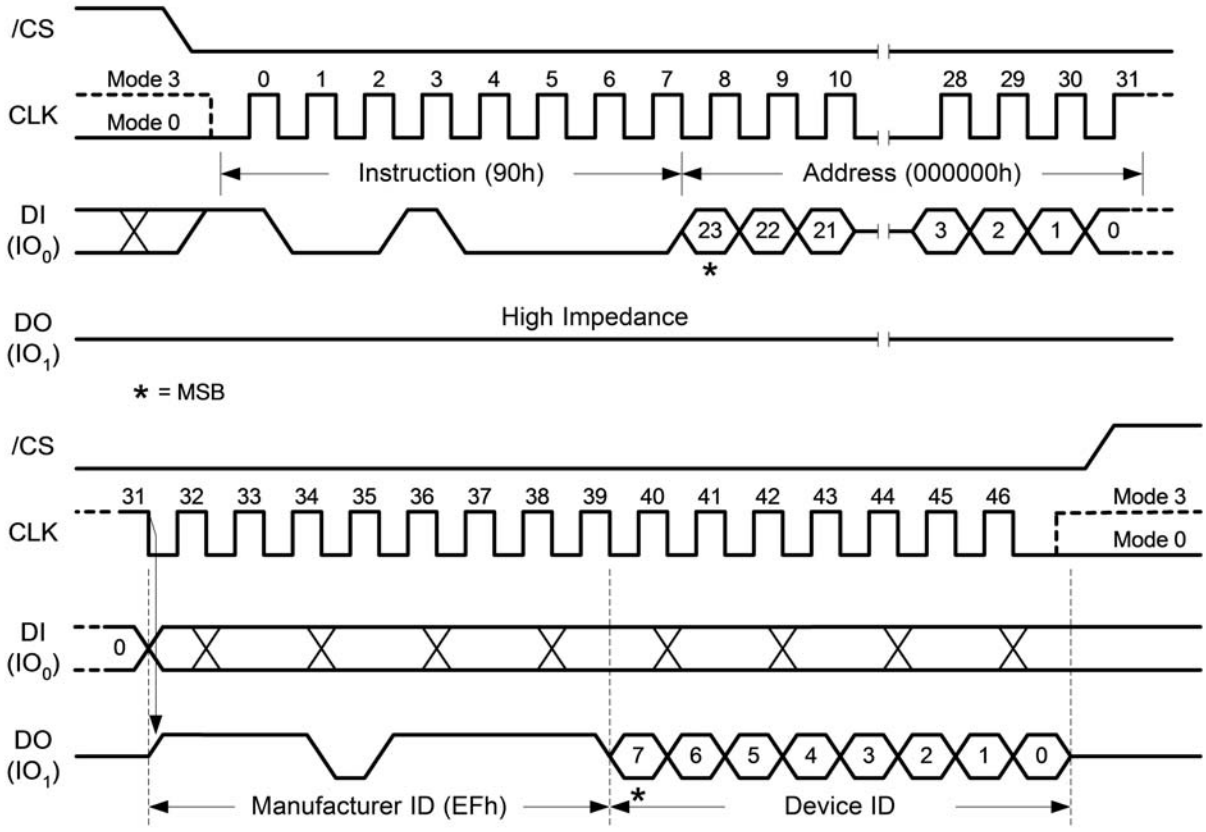


Figure 66: Read Manufacturer/Device ID Instruction (SPI Mode)

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7.8.4 Read Manufacturer/Device ID Dual I/O (92h)

This instruction is an alternative to the Read Manufacturer/Device ID (90h) instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The instruction format is similar to the Fast Read Dual I/O (BBh) instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 67.

The Device ID values for the W77Q32JW/W77Q16JW are listed in Section 7.3.

If the 24-bit address is initially set to 000001h the Device ID is read first, followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving the /CS pin high.

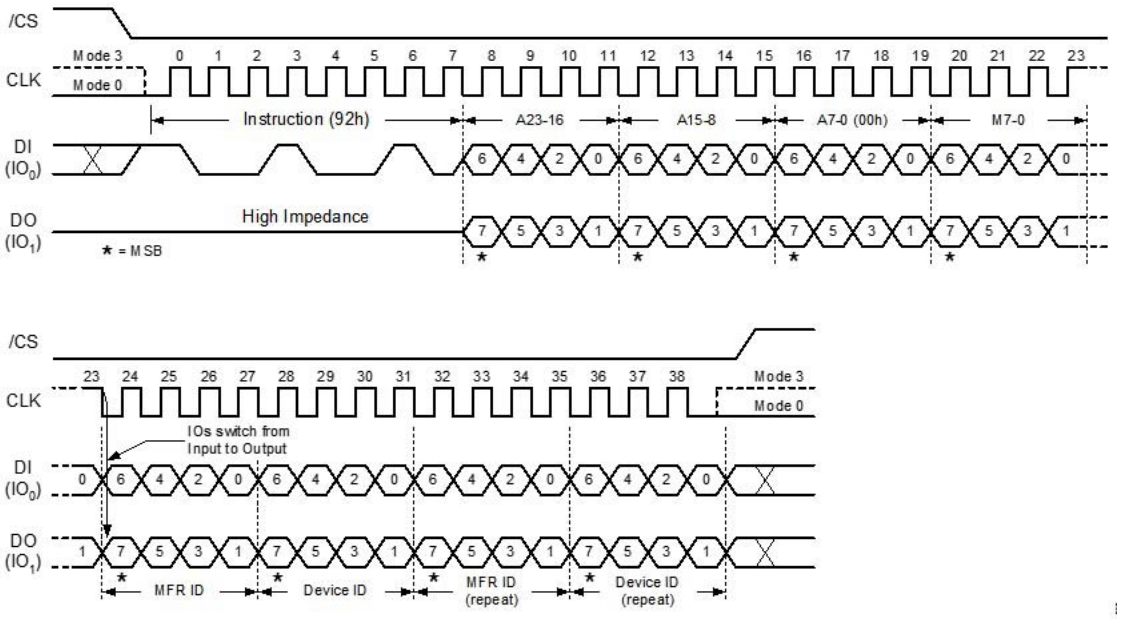


Figure 67: Read Manufacturer/Device ID Dual I/O Instruction (SPI Mode only)

Note: The Read Command Bypass Mode bits M(7-0) must be set to Fxh to be compatible with the Fast Read Dual I/O instruction.

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7.8.5 Read Manufacturer/Device ID Quad I/O (94h)

This instruction is an alternative to the Read Manufacturer/Device ID (90h) instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The instruction format is similar to the Fast Read Quad I/O (EBh) instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “94h” followed by four dummy cycles and then a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 68.

The Device ID values for the W77Q32JW/W77Q16JW are listed in Section 7.3.

If the 24-bit address is initially set to 000001h, the Device ID is read first, followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

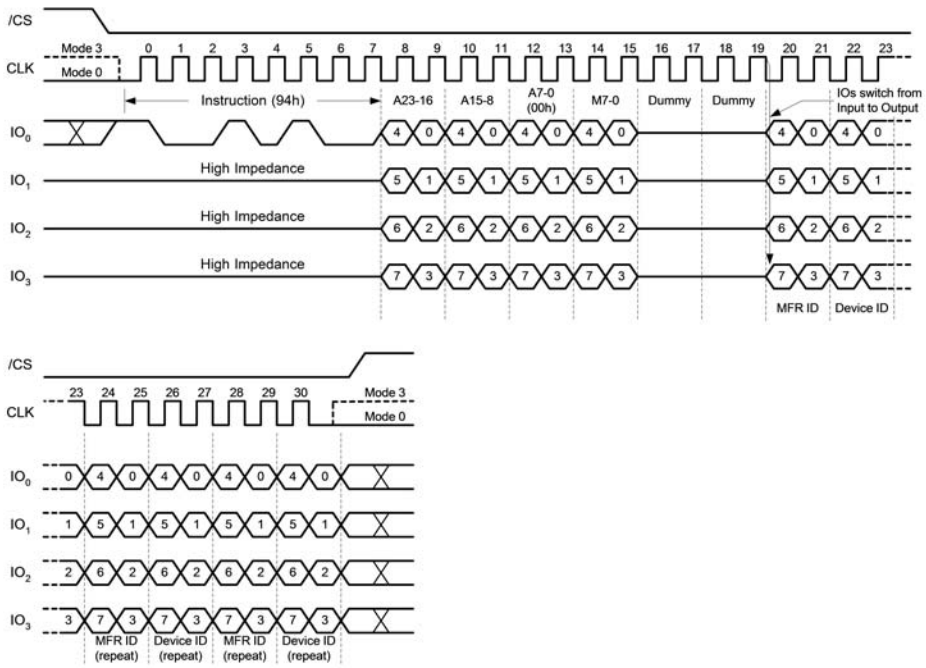


Figure 68: Read Manufacturer/Device ID Quad I/O Instruction (SPI Mode only)

Note: The “Read Command Bypass Mode” bits M(7-0) must be set to Fxh to be compatible with the Fast Read Quad I/O instruction.

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7.8.6 Read Unique ID Number (4Bh)

This instruction accesses a factory-set read-only 64-bit number that is unique to each W77Q32JW/W77Q16JW device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID Number instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 69.

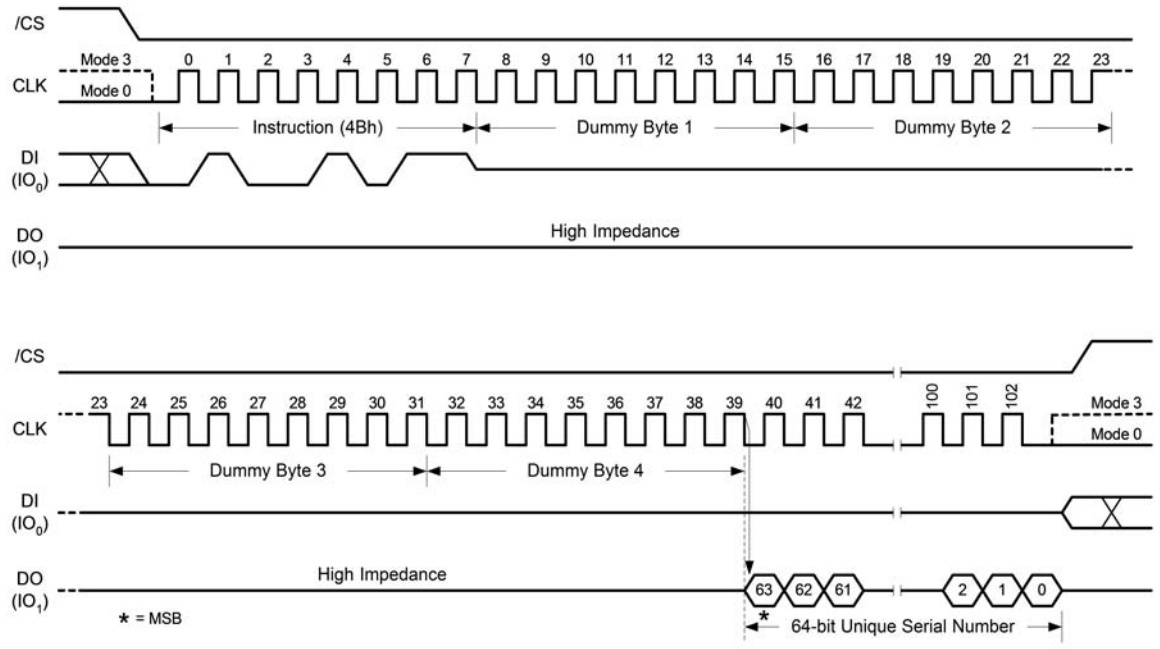


Figure 69: Read Unique ID (SPI Mode only)

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7.8.7 Read JEDEC ID (9Fh)

For compatibility reasons, the device provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC-assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 70 and Figure 71.

For memory type and capacity values, refer to Section 7.3.

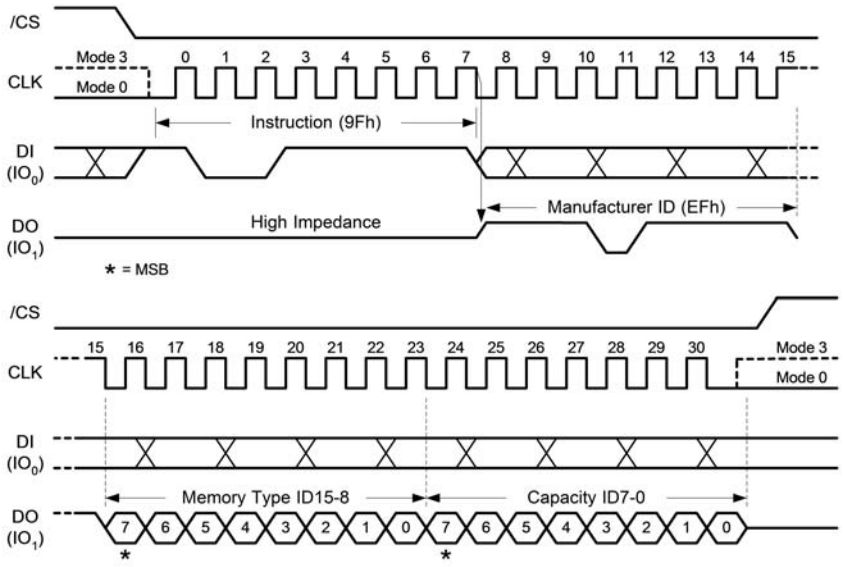


Figure 70: Read JEDEC ID Instruction (SPI Mode)

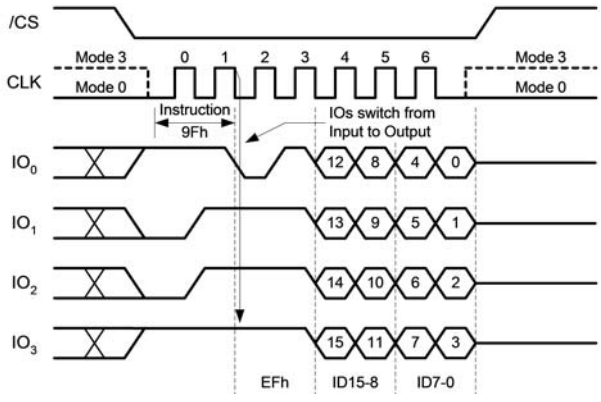


Figure 71: Read JEDEC ID Instruction (QPI Mode)

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7.8.8 Read SFDP Register (5Ah)

The W77Q32JW/W77Q16JW features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions, and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently, three PID tables are specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as with the JEDEC standard JESD216 published in 2011. Most Winbond SpiFlash Memories shipped after June 2011 (date code 1124 and beyond) support the SFDP feature as specified in the applicable datasheet.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight “dummy” clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 72. For SFDP register values and descriptions, refer to the Winbond Application Note for SFDP Definition Table.

Note: A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

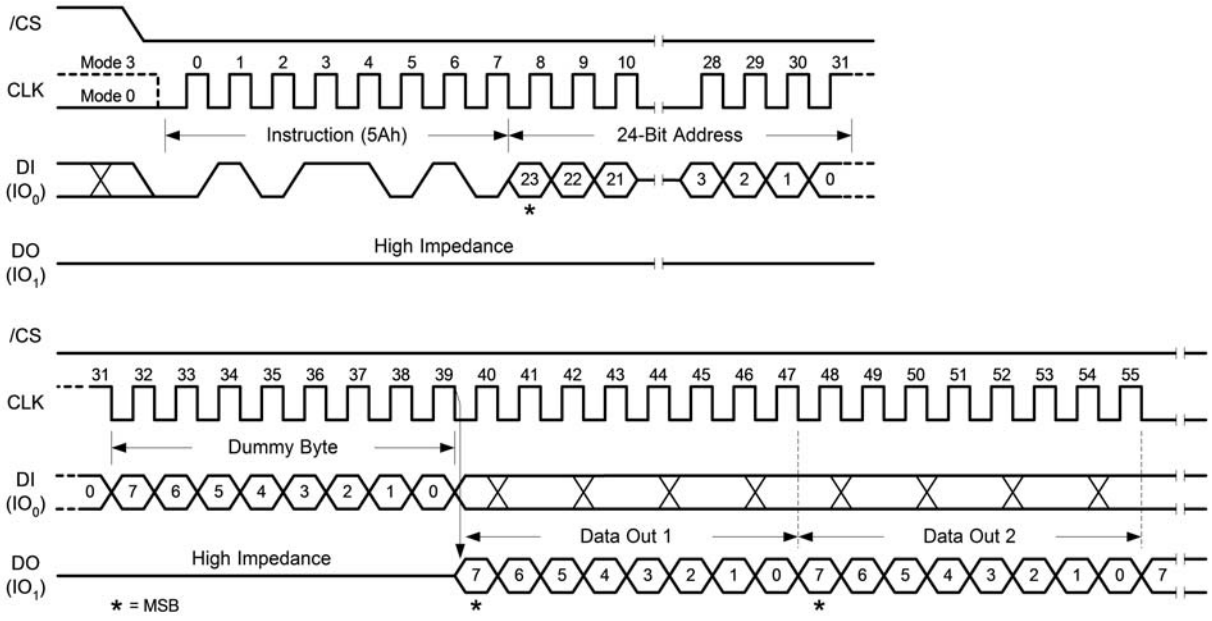


Figure 72: Read SFDP Register Instruction Sequence Diagram

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7.8.9 Erase Security Register (44h)

The W77Q32JW/W77Q16JW offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by system manufacturers to store security and other important information separately from the main memory array.

The instruction format is similar to the Sector Erase (20h) instruction. A Write Enable (06h) instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1).

The instruction is initiated by driving the /CS pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Don’t Care
Security Register #2	00h	0 0 1 0	0 0 0 0	Don’t Care
Security Register #3	00h	0 0 1 1	0 0 0 0	Don’t Care

The Erase Security Register instruction sequence is shown in Figure 73.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation commences for a time duration of t_{SE} (See AC Characteristics).

While the Erase Security Register cycle is in progress, the Read Status Register instruction (Section 7.5.4) may still be accessed for checking the status of the BUSY bit. The BUSY bit is 1 during the erase cycle and becomes 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

The Security Register Lock Bits (LB3, LB2, and LB1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked and Erase Security Register instruction to that register will be ignored. (Refer to Section 8.2.2.2 for detailed descriptions.)

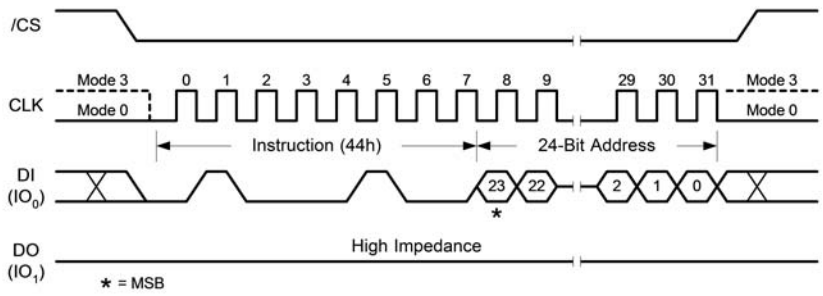


Figure 73: Erase Security Register Instruction (SPI Mode Only)

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7.8.10 Program Security Register (42h)

This instruction is similar to the Page Program (02h) instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable (06h) instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL = 1). The instruction is initiated by driving the /CS pin low, then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

The Program Security Register instruction sequence is shown in Figure 74.

The Security Register Lock Bits (LB3, LB2, and LB1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register is permanently locked, and Program Security Register instructions to that register will be ignored (refer to Section 8.2.2.2).

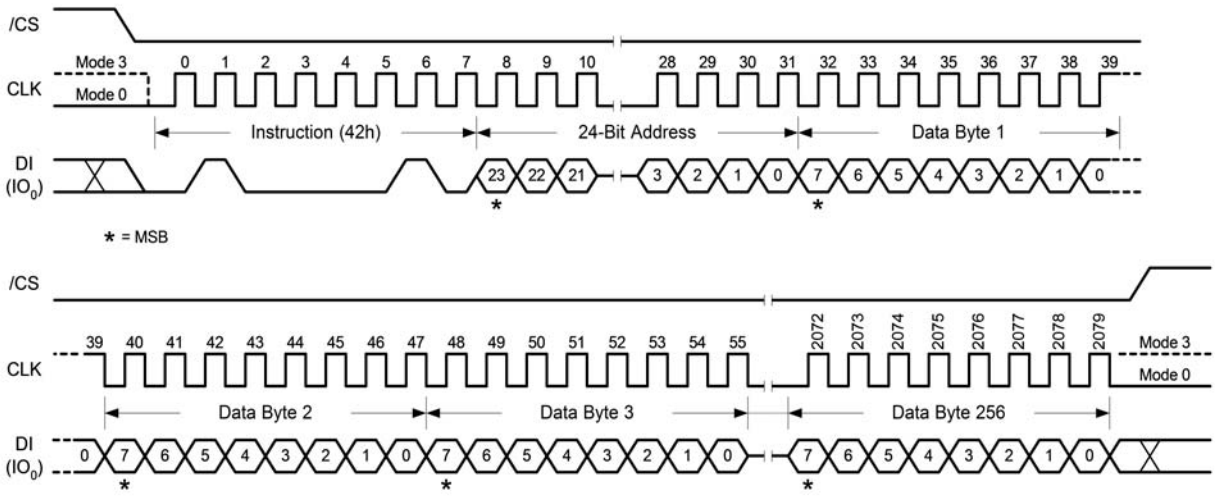


Figure 74: Program Security Register Instruction (SPI Mode Only))

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7.8.11 Read Security Register (48h)

This instruction is similar to the Fast Read (0Bh) instruction and allows one or more data bytes to be sequentially read from one of the four security registers.

The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first.

The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment.

The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 75.

If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY = 1), the instruction is ignored and will not have any effect on the current cycle.

The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

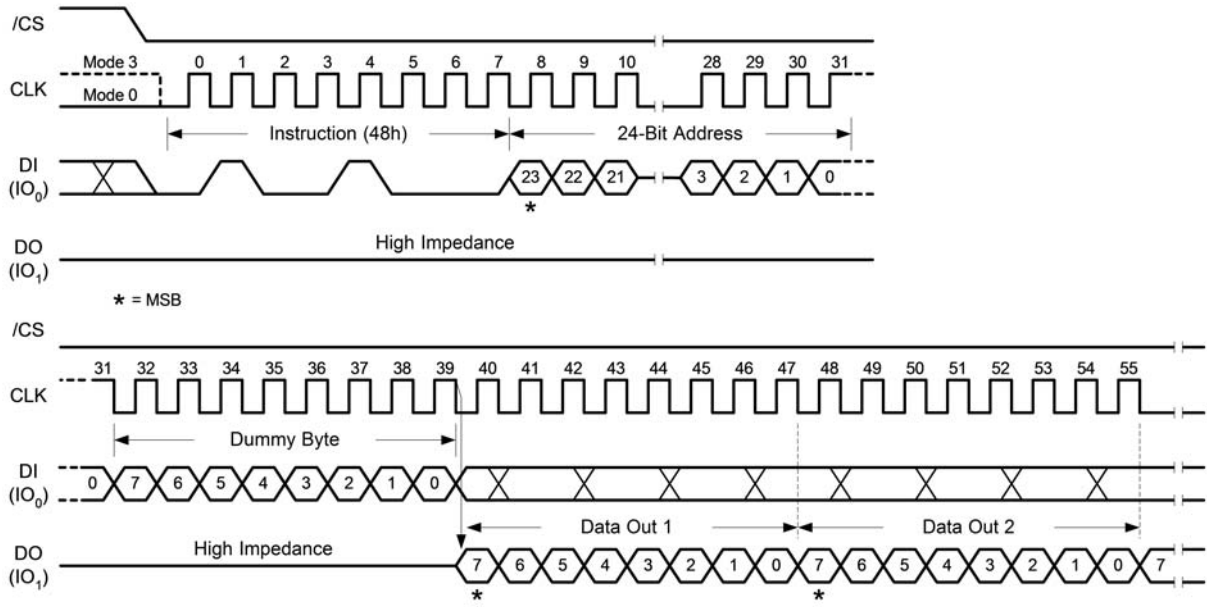


Figure 75: Read Security Register Instruction (SPI Mode Only))

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7.8.12 Enter QPI Mode (38h)

The W77Q32JW/W77Q16JW supports both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI Mode (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of Winbond serial flash memories. See Instruction Set Table 1 (Standard SPI Instructions) and Instruction Set Table 2 (Dual/Quad SPI Instructions) for all supported SPI commands.

In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 (SR2) must be set to 1 first, and an “Enter QPI Mode (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI Mode (38h)” instruction will be ignored and the device will remain in SPI mode.

See Instruction Set Table 3 (QPI Instructions) for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting remains unchanged.

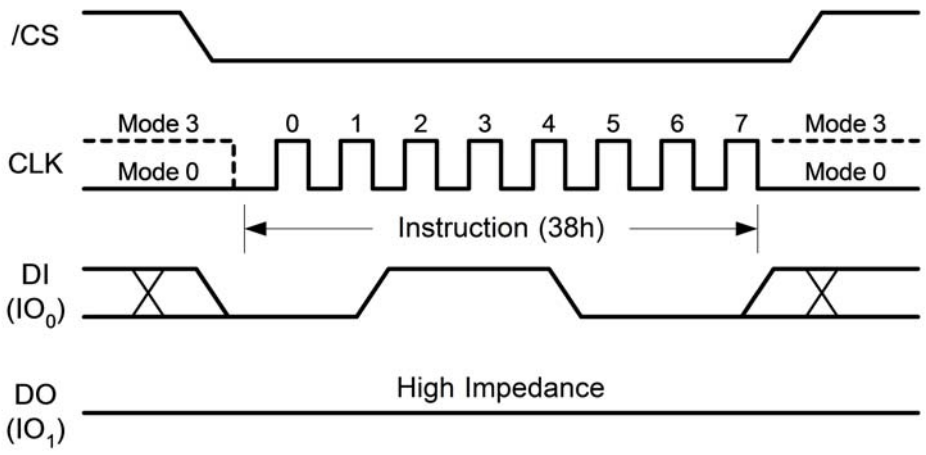


Figure 76: Enter QPI Instruction (SPI Mode only)

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7.8.13 Exit QPI Mode (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting remains unchanged.

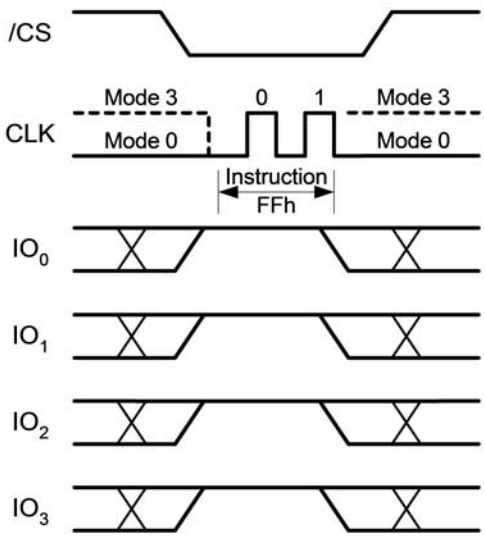


Figure 77: Exit QPI Instruction (QPI Mode only)

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7.8.14 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the W77Q32JW/W77Q16JW provide a software Reset instruction instead of a shared or dedicated hardware reset pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), Read Command Bypass Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

"Enable Reset (66h)" and "Reset Device (99h)" instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than "Reset Device (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset Device (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=35us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

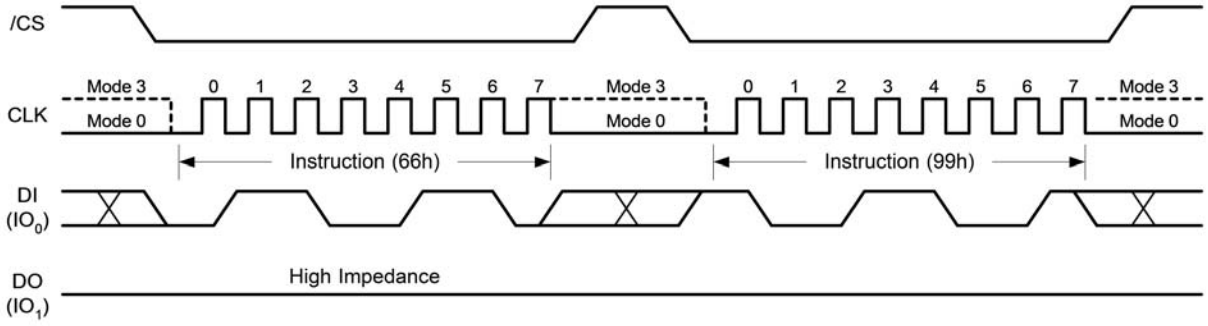


Figure 78: Enable Reset and Reset Instruction Sequence (SPI Mode)

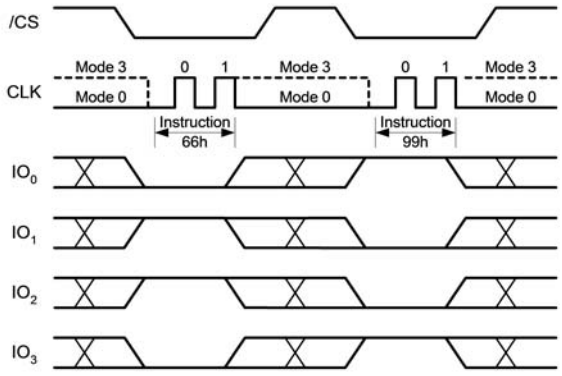


Figure 79: Enable Reset and Reset Instruction Sequence (QPI Mode)

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7.8.15 Write Extended Address Register (C5h)

This instruction is used to write to the Extended Address Register (EAD). When the device is in the 3-Byte Address Mode, this register is used as the 4th address byte A[31:24] to access logical memory regions beyond 128Mb.

To write the Extended Register bits, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Extended Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “C5h”, and then writing the Extended Register data byte as illustrated in Figure 80 and Figure 81.

Note: Writing to this register is only allowed when the device is in 3B-Addressing Mode.

For a 32M-bit Secure Flash Memory device, C5h is used to write only the A24 bit of the Extended Address Register. In this case, the remaining bits (A25-A31) remain unchanged (set to 0), regardless of the value given by the instruction.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register value is cleared to 0.

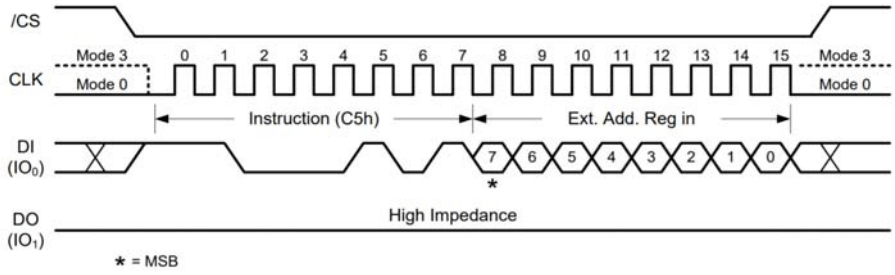


Figure 80: Write Extended Register Instruction (SPI Mode)

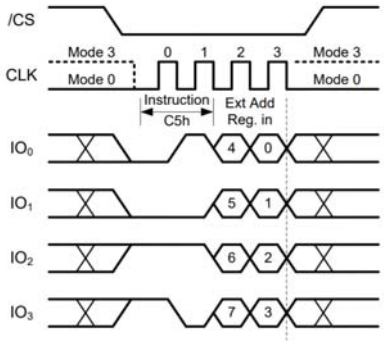


Figure 81: Write Extended Register Instruction (QPI Mode)

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8 REGISTERS

8.1 Acronyms

Table 6 summarizes the acronyms that are used to describe the different register field types in this chapter.

Table 6: Field Type Abbreviations

R/W	Read/Write
R	Read — data read from this address is not related to the data written to it.
W	Write — data written to this address is not related to the data read from it.
RO	Read-Only — writing to the register/bit is ignored.
HC	Hard-Coded value read — writing to the register/bit is ignored.
ROC	Read-Only, Clear bits — reading from the register clears all its bits.
WO	Write-Only — reading from the register/bit returns 0.
R/W1C	Read/Write 1 to Clear — writing 1 to a bit clears it to 0, writing 0 has no effect.
R/W1S	Read/Write 1 to Set — writing 1 to a bit sets its value to 1, writing 0 has no effect.

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8.2 Standard Flash Registers

Three Status and Configuration Registers, are provided for W77Q32JW/W77Q16JW.

The Read Status Register-1/2/3 instructions can be used to provide the status of the availability of the flash memory array, whether the device is write-enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/ Program Suspend status, and output driver strength.

The Write Status Register instruction (See Section 7.5.5) can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, Hold/ Reset functions, and output driver strength. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect/Lock bits (SRP, SRL), the Write Enable (06h) instruction, and during Standard/Dual SPI operations, the /WP pin.

Table 7 lists the device Security Status Registers.

Table 7: Register Map

REGISTER	DESCRIPTION
SR1	Status Register 1 (SR1)
SR2	Status Register 2 (SR2)
SR3	Status Register 3 (SR3)

Note: In the following register field description, the notation “Volatile/Non-Volatile Writable” means that this is a volatile register that loads its default reset value from non-volatile storage. Refer to Section 7.5.5 for details on updating the volatile or non-volatile versions of these registers.

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8.2.1 Status Register 1 (SR1)

Status Register 1 (SR1) contains the bits described in Table 8 and Figure 82:

Register:SR1

Table 8: SR1 Register Bit Description

BIT	NAME	TYPE	RESET	DESCRIPTION
7	SRP	R/W	0	**Status Register Protect:** Control the method of write protection.
6	SEC	R/W	0	**Sector Protect:** Controls whether Block Protect Bits protect 4KB sectors or 64KB blocks.
5	TB	R/W	0	**Top/Bottom Protect:** Controls the part of the array (Top or Bottom) protected by Block Protect Bits.
4	BP2	R/W	0	**Block Protect Bits:** Provide Write Protection control and status.
3	BP1	R/W	0	
2	BP0	R/W	0	
1	WEL	RO	0	**Write Enable Latch:** If set, a Write Enable instruction has been executed. Otherwise, the device is write disabled.
0	BUSY	RO	0	**Erase/Write In Progress:** If set, then the device is executing an instruction. Otherwise, the device is ready for the next instruction.

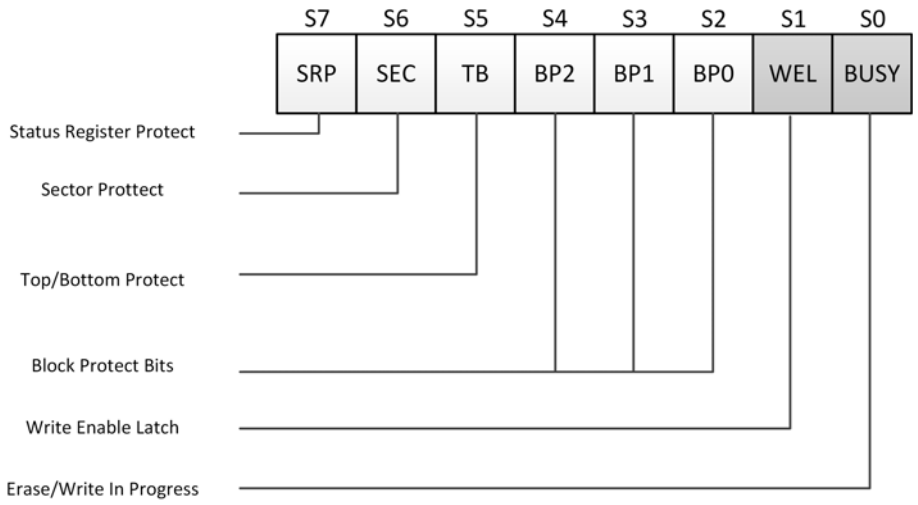


Figure 82: Status Register 1

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8.2.1.1. Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read-only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase/Program Security Register instructions or some of the Secure operations.

During this time, the device ignores further instructions except for the Read Status Register (see Section 7.5.4) and Erase/Program Suspend (75h) instruction (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics). When the Program, Erase or Write Status/Security Register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

8.2.1.2. Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read-only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security register.

8.2.1.3. Block Protect Bits (BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. All, none, or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection tables in Section 8.2.4).

Block Protect bits can be set using the Write Status Register Instruction (see Section 7.5.5 and t_W in AC characteristics). The factory default setting for the Block Protection Bits is 0, none of the array protected.

8.2.1.4. Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB = 0) or the Bottom (TB = 1) of the array as shown in the Status Register Memory Protection table (see Section 8.2.4). The factory default setting is TB = 0. The TB bit can be set with the Write Status Register Instruction (see Section 7.5.5) depending on the state of the SRP, SRL and WEL bits.

8.2.1.5. Sector/Block Protect Bit (SEC) – *Volatile/Non-Volatile Writable*

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect one of the following: 4 KB Sectors (SEC = 1) or 64 KB Blocks (SEC = 0) in the Top (TB = 0) or the Bottom (TB = 1) of the array as shown in the Status Register Memory Protection table (see Section 8.2.4). The default setting is SEC = 0.

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8.2.1.6. Status Register Protect (SRP, SRL)

The Status Register Protect bit (SRP) is a non-volatile read/write bit in the status register (S7). The SRP bit controls the method of write protection: software protection, or hardware protection.

The Status Register Lock bit (SRL) is a volatile/non-volatile read/write bit in the status register (S8). The SRL bit controls the method of write protection: temporary lock-down or permanently one time program.

Note: Setting the volatile SRL bit to 1 locks the Status Registers and thus cannot be reversed until the next reset cycle. Setting the non-volatile SRL bit to 1 is One-Time-Program (OTP) operation, and this bit cannot be cleared to 0 afterwards.

Table 9: Status Register Protect (SRP, SRL)

SRL	SRP	/WP	STATUS REGISTER	DESCRIPTION
0	0	X	Software Protection	The /WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL = 1. [Factory Default]
0	1	0	Hardware Protected	When the /WP pin is low, the Status Register is locked and cannot be written to.
0	1	1	Hardware Unprotected	When the /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL = 1.
1	X	X	Power Supply Lock-Down	The status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	X	X	One Time Program(2)	The Status Register is permanently protected and cannot be written to. (enabled by adding prefix command AAh, 55h).

1. When SRL =1, a power-down, power-up cycle will change SRL = 0 state.
2. Please contact Winbond for details regarding the special instruction sequence.

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8.2.2 Status Register 2 (SR2)

Status Register 2 (SR2) contains the bits described in Table 10 and Figure 83.

Register:SR2

Table 10: SR2 Register Bit Description

BIT	NAME	TYPE	RESET	DESCRIPTION
15	SUS	RO	0	**Erase/Program Suspend Status**
14	CMP	R/W	0	**Complement Protect:** If set, then prior array protection is reversed.
13	LB3	R/W1S	0	**Security Register Lock Bits**: Provides the write protect control and status to the Security Registers. Note: These bits are non-volatile OTP bits. Once set to 1 it cannot be cleared to 0.
12	LB2	R/W1S	0	
11	LB1	R/W1S	0	
10	(R)	RO	0	**Reserved**.
9	QE	R/W	0	**Quad Enable**: Permits Quad SPI and QPI operations.
8	SRL	R/W1S	0	**Security Lock Status Registers**: Controls the method of write protection

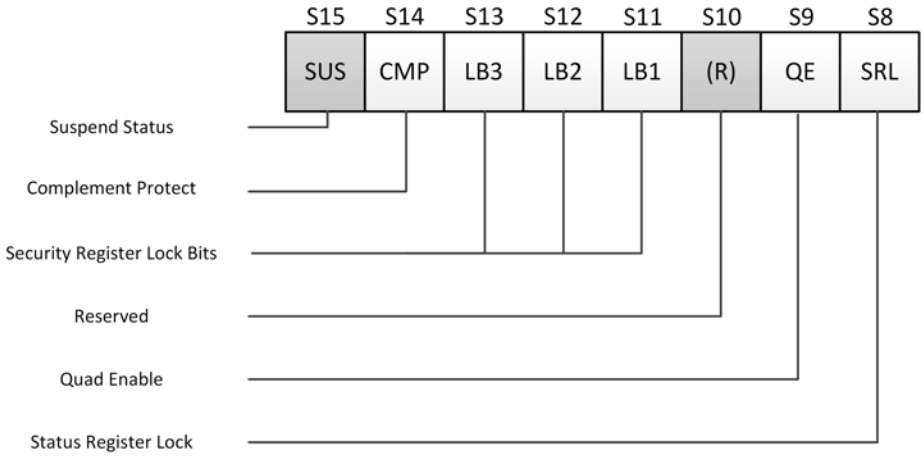


Figure 83: Status Register Lock (SRL)

See Section 8.2.1.6.

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8.2.2.1. Quad Enable (QE) – *Volatile/Non-Volatile Writable*

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options “R” or “S”), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1 (factory default for Quad Enabled part numbers with ordering option “Q”, “O” or “N”), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

The QE bit is required to be set to a 1 before issuing an Enter QPI Mode (38h) instruction to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command is ignored. When the device is in QPI mode, the QE bit remains 1. A Write Status Register command (see Section 7.5.5) in QPI mode cannot change QE bit from a “1” to a “0”.

8.2.2.2. Security Register Lock Bits (LB3, LB2, LB1) – *Volatile/Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction (see Section 7.5.5). LB3-1 are One Time Programmable (OTP), once set to 1; they cannot be cleared to 0, thus the corresponding 256-Byte Security Register becomes read-only permanently.

Note: On reset, the volatile register returns to its default value (loaded from the non-volatile register). Therefore it is OTP until the next reset. The non-volatile register is OTP.

8.2.2.3. Complement Protect (CMP) – *Volatile/Non-Volatile Writable*

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with the SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 is reversed. For instance, when CMP = 0, a top 64 KB block can be protected while the rest of the array is not; if CMP is then set to 1, the top 64 KB block becomes unprotected while the rest of the array becomes read-only. Refer to Table 12 and Table 13 for details. The default setting is CMP = 0.

8.2.2.4. Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read-only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by an Erase/Program Resume (7Ah) instruction as well as by a power-down, power-up cycle.

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8.2.3 Status Register 3 (SR3)

Status Register 3 (SR3) contains the bits described in Table 11 and Figure 84, below.

RegisterSR3

Table 11: SR3 Register Bit Description

BIT	NAME	TYPE	RESET	DESCRIPTION
23	HOLD/RST	R/W	0	**HOLD# or RSTI# Pin Function**: Determines whether the HOLD# or RSTI# function is implemented on the hardware pin for 8-pin packages.
22	DRV1	R/W	0	**Output Driver Strength**: Determines strength of the output driver for read operations.
21	DRV0	R/W	0	
20	(R)	RO	0	**Reserved**.
19	(R)	RO	0	
18	WPS	R/W	0	**Write Protect Selection**: If set, the device utilize Individual Block Locks in protecting a specific memory array area. Otherwise, it uses a combination of bits.
17	R	RO	0	**Reserved**.
16	A24	RO	0	**Extended Address Bit 24:** Indicates the extended address register bit 24. This extends the 24b address of any standard-Flash transaction (read/program/erase).

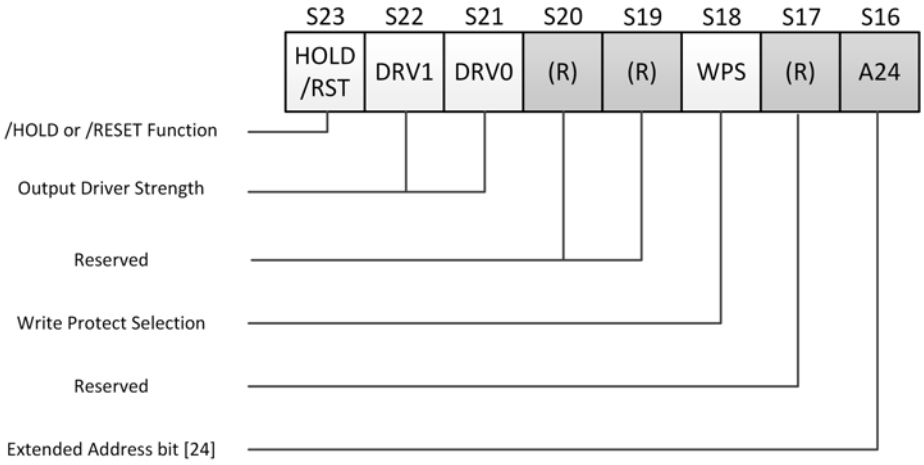


Figure 84: Standard Flash Status Register 3

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8.2.3.1. Extended Address bit (A24) - *Status Only*

The Extended Address Bit A24 extends the 3B address and allows access to logical addresses beyond 128MB.

This bit may be updated using the Write Extended Address Register (C5h) instruction.

8.2.3.2. Write Protect Selection (WPS) – *Volatile/Non-Volatile Writable*

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device uses the combination of CMP, SEC, TB, BP2, BP1, or BP0 bits to protect a specific area of the memory array.

When WPS = 1, the device utilizes the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

8.2.3.3. Output Driver Strength (DRV1, DRV0) – *Volatile/Non-Volatile Writable*

The DRV1 & DRV0 bits are used to determine the output driver strength for Read operations. The factory default for part numbers with ordering options “R”, “S”, “Q” or “O” is DRV1=’1 and DRV0=’1 which results in output driver strength of 25%. The factory default for part numbers with ordering option “N” is DRV1=’0 and DRV0=’0 which results in output driver strength of 75%.

DRV1, DRV0	DRIVER STRENGTH
0, 0	75%
0, 1	50%
1, 0	Reserved
1, 1	25%

8.2.3.4. HOLD# or RSTI# Pin Function (HOLD/RST) – *Volatile/Non-Volatile Writable*

The HOLD/RST bit is used to determine whether HOLD# or RSTI# function is implemented on the hardware pin for 8-pin packages. When HOLD/RST = 0 (factory default), the pin acts as HOLD#; when HOLD/RST = 1, the pin acts as RSTI#. However, HOLD# or RSTI# functions are only available when QE = 0. If QE is set to 1, the HOLD# and RSTI# functions are disabled; the pin acts as a dedicated data I/O pin.

8.2.3.5. Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a Write Status Register instruction (see Section 7.5.5), the Reserved Bits can be written as “0”, but this will have no effect.

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8.2.4 Write Protection Configurations

8.2.4.1. Status Register Memory Protection (WPS = 0, CMP = 0)

Table 12: Status Register Memory Protection (WPS = 0, CMP = 0)

STATUS REGISTER					W77Q32JW/W77Q16JW (32M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	63	3F0000h – 3FFFFFh	64KB	Upper 1/64
0	0	0	1	0	62 and 63	3E0000h – 3FFFFFh	128KB	Upper 1/32
0	0	0	1	1	60 through 63	3C0000h – 3FFFFFh	256KB	Upper 1/16
0	0	1	0	0	56 through 63	380000h – 3FFFFFh	512KB	Upper 1/8
0	0	1	0	1	48 through 63	300000h – 3FFFFFh	1MB	Upper 1/4
0	0	1	1	0	32 through 63	200000h – 3FFFFFh	2MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/64
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/32
0	1	0	1	1	0 through 3	000000h – 03FFFFh	256KB	Lower 1/16
0	1	1	0	0	0 through 7	000000h – 07FFFFh	512KB	Lower 1/8
0	1	1	0	1	0 through 15	000000h – 0FFFFFh	1MB	Lower 1/4
0	1	1	1	0	0 through 31	000000h – 1FFFFFh	2MB	Lower 1/2
X	X	1	1	1	0 through 63	000000h – 3FFFFFh	4MB	ALL
1	0	0	0	1	63	3FF000h – 3FFFFFh	4KB	U - 1/1024
1	0	0	1	0	63	3FE000h – 3FFFFFh	8KB	U - 1/512
1	0	0	1	1	63	3FC000h – 3FFFFFh	16KB	U - 1/256
1	0	1	0	X	63	3F8000h – 3FFFFFh	32KB	U - 1/128
1	1	0	0	1	0	000000h – 000FFFh	4KB	L - 1/1024
1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/512
1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/256
1	1	1	0	X	0	000000h – 007FFFh	32KB	L - 1/128

Notes:

- 'X' represents 'Don't Care'
- L = Lower, U = Upper
- If any Erase or Program instruction specifies a memory region that contains protected data portion, that instruction is ignored.

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8.2.4.2. Status Register Memory Protection (WPS = 0, CMP = 1)

Table 13: Status Register Memory Protection (WPS = 0, CMP = 1)

STATUS REGISTER					W77Q32JW/W77Q16JW (32M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	X	0	0	0	0 through 63	000000h – 3FFFFFh	4MB	ALL
0	0	0	0	1	0 through 62	000000h – 3EFFFFh	4,032KB	Lower 63/64
0	0	0	1	0	0 and 61	000000h – 3DFFFFh	3,968KB	Lower 31/32
0	0	0	1	1	0 through 59	000000h – 3BFFFFh	3,840KB	Lower 15/16
0	0	1	0	0	0 through 55	000000h – 37FFFFh	3,584KB	Lower 7/8
0	0	1	0	1	0 through 47	000000h – 2FFFFFh	3MB	Lower 3/4
0	0	1	1	0	0 through 31	000000h – 1FFFFFh	2MB	Lower 1/2
0	1	0	0	1	1 through 63	010000h – 3FFFFFh	4,032KB	Upper 63/64
0	1	0	1	0	2 and 63	020000h – 3FFFFFh	3,968KB	Upper 31/32
0	1	0	1	1	4 through 63	040000h – 3FFFFFh	3,840KB	Upper 15/16
0	1	1	0	0	8 through 63	080000h – 3FFFFFh	3,584KB	Upper 7/8
0	1	1	0	1	16 through 63	100000h – 3FFFFFh	3MB	Upper 3/4
0	1	1	1	0	32 through 63	200000h – 3FFFFFh	2MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 through 63	000000h – 3FEFFFh	4,092KB	L - 1023/1024
1	0	0	1	0	0 through 63	000000h – 3FDFFFh	4,088KB	L - 511/512
1	0	0	1	1	0 through 63	000000h – 3FBFFFh	4,080KB	L - 255/256
1	0	1	0	X	0 through 63	000000h – 3F7FFFh	4,064KB	L - 127/128
1	1	0	0	1	0 through 63	001000h – 3FFFFFh	4,092KB	U - 1023/1024
1	1	0	1	0	0 through 63	002000h – 3FFFFFh	4,088KB	U - 511/512
1	1	0	1	1	0 through 63	004000h – 3FFFFFh	4,080KB	U - 255/256
1	1	1	0	X	0 through 63	008000h – 3FFFFFh	4,064KB	U - 127/128

Notes:

- 'X' represents 'Don't Care'
- L = Lower, U = Upper
- If any Erase or Program instruction specifies a memory region that contains protected data portion, that instruction is ignored.

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8.2.4.3. Individual Block Memory Protection (WPS = 1)

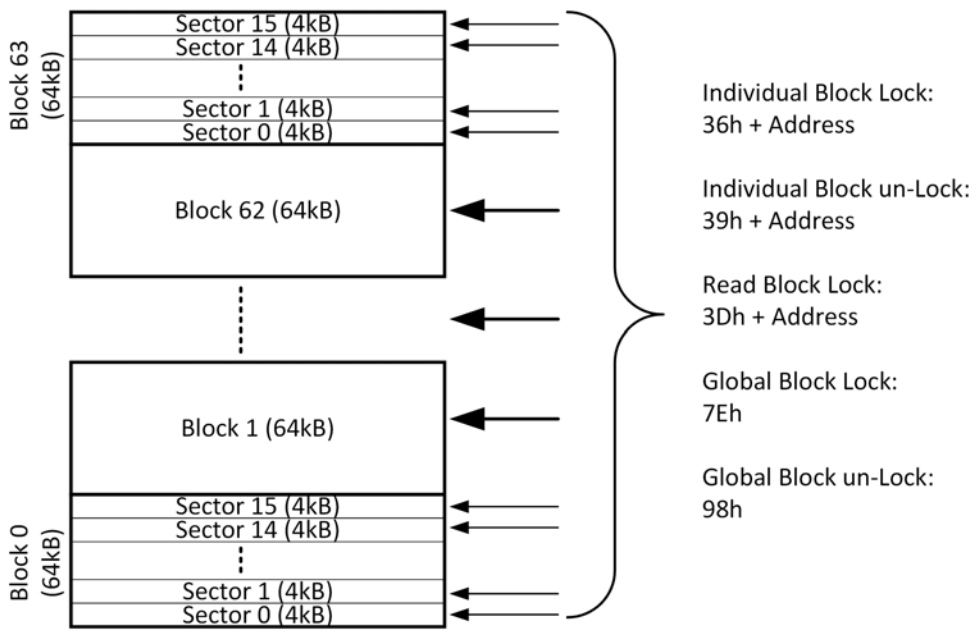


Figure 85: Individual Block/Sector Locks

Notes:

1.Individual Block/Sector protection is only valid when WPS = 1.
2.All individual block/sector lock bits are set to 1 by default after power up, all memory array is protected.

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9 ELECTRICAL CHARACTERISTICS

Notes: The product is not fully characterized. The specifications are subject to change and are not guaranteed.

9.1 Absolute Maximum Ratings

Table 14 describes the absolute maximum ratings for the device.

Table 14: Absolute Maximum Range

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to 2.5	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20 nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

Table 15 describes the operating ranges for the device.

Table 15: Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC	F_R = 133MHz, fR = 50MHz	1.7	1.95	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C

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9.3 Power-Up & Power-Down Timing and Requirements

Table 16 describes the timing and requirements for powering up and down.

Table 16: Power-Up & Power-Down Timing and Requirements

PARAMETER(1)	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to CS# Low	t_{VSL}	20		µs
Time Delay Before Write Instruction	t_{PUW}	5		ms
Write Inhibit Threshold Voltage	V_{WI}	1.0	1.4	V
The minimum duration for ensuring initialization will occur	t_{PWD}	100		us
VCC voltage needed to be below V_{PWD} for ensuring initialization will occur	V_{PWD}		0.8	V

1. These parameters are characterized only.

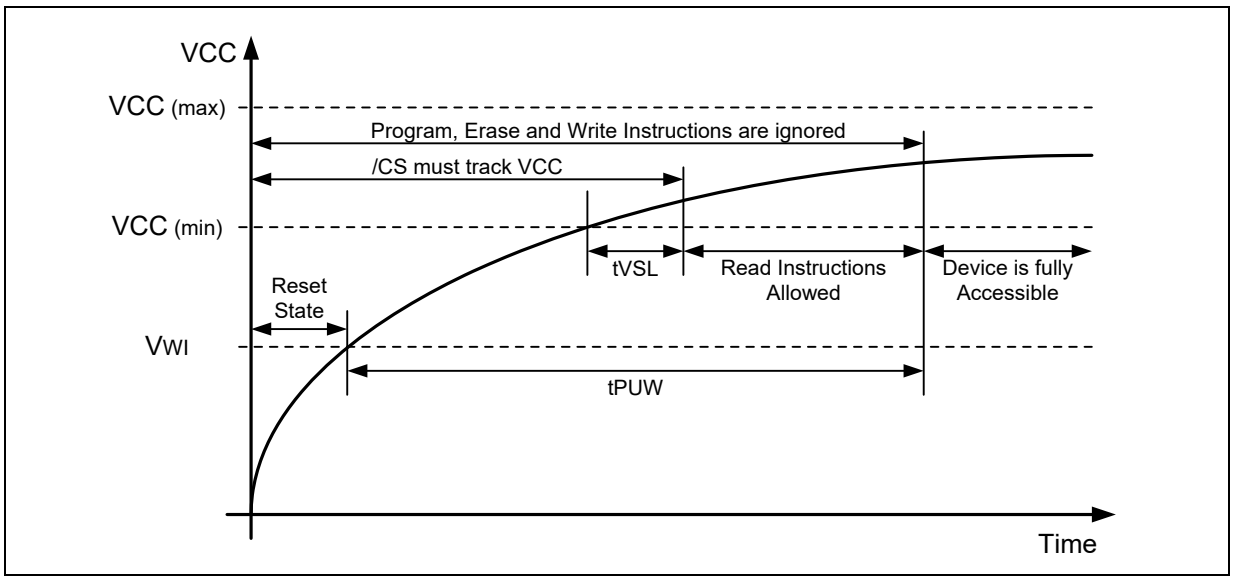


Figure 86: Power-up Timing and Voltage Levels

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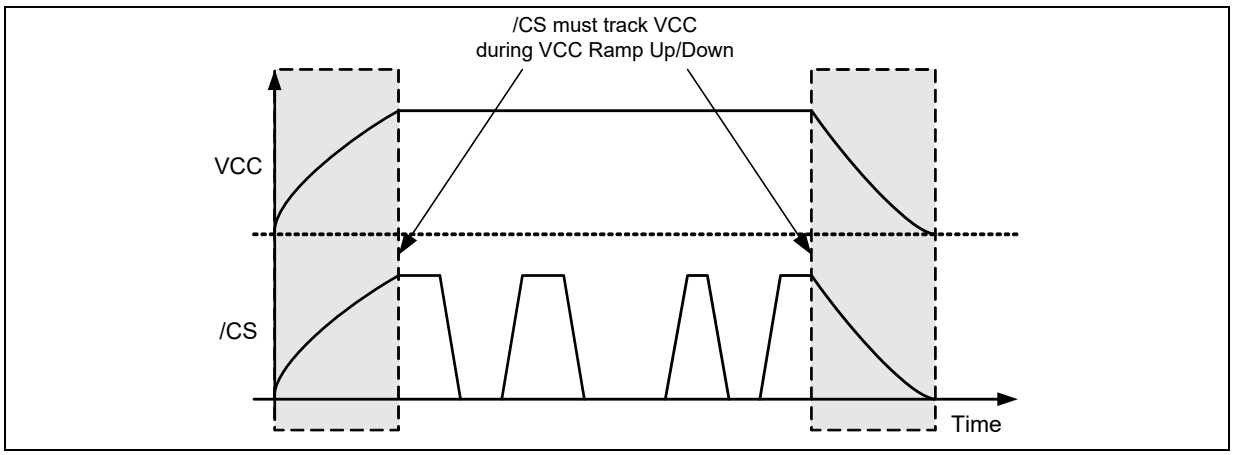


Figure 87: Power-up, Power-Down Requirement

For the length of a power cycle, the system must not initiate the power-up sequence until Vcc drops down to V_{PWD} and keeps a t_{PWD} for device to initialize correctly.

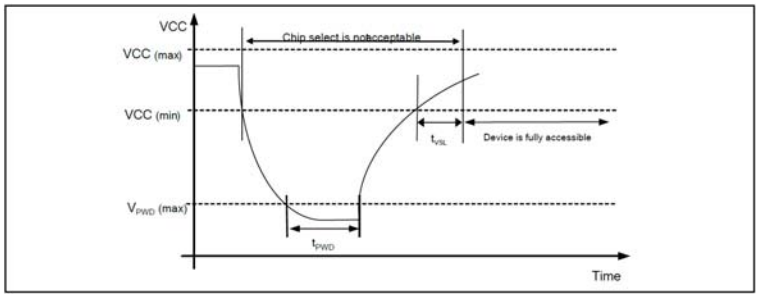


Figure 88: Power Cycle Requirement

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9.4 DC Electrical Characteristics

Table 17 describes the device's DC electrical characteristics.

Table 17: DC Electrical Characteristics:

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance(1)	Cin	VIN = 0V			6	pF
Output Capacitance	Cout	VOUT = 0V			8	pF
Input Leakage	ILI				±2	µA
I/O Leakage	Ilo				±2	µA
Standby Current	ICC1	/CS = VCC, VIN = GND or VCC		10	40	uA
Power-down Current (LFOSC disabled)	ICC2	/CS = VCC, VIN = GND or VCC		0.1	28	µA
Current Read Data / Dual / Quad 1MHz(2)	Icc3	C = 0.1 VCC / 0.9 VCC DO = Open		1	3	mA
Current Read Data / Dual / Quad 50MHz(2)	Icc3	C = 0.1 VCC / 0.9 VCC DO = Open		8	10	mA
Current Read Data / Dual /Quad 104MHz(2)	Icc3	C = 0.1 VCC / 0.9 VCC DO = Open		10	12	mA
Current Write Status Register	Icc4	/CS = VCC		15	20	mA
Current Page Program	Icc5	/CS = VCC		15	20	mA
Current Sector/Block Erase	Icc6	/CS = VCC		17	24	mA
Current Chip Erase	ICC7	/CS = VCC		20	27	mA
Input Low Voltage	VIL		–0.5		VCC x 0.3	V
Input High Voltage	VIH		VCC x 0.7		VCC + 0.6	V
Output Low Voltage	VOL	Iol = 100 µA			0.2	V
Output High Voltage	VOH	Ioh = –100 µA	VCC – 0.2			V

1.Tested on sample basis and specified through design and characterization data. TA=25°, VCC=1.8V.

2.Checker Board Pattern.

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9.5 AC Electrical Characteristics

9.5.1 AC Measurement Conditions

Table 18 describes the device's AC measurement conditions.

Table 18: AC Measurement Conditions Output Hi-Z is defined as the point where data out is no longer driven

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	in	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

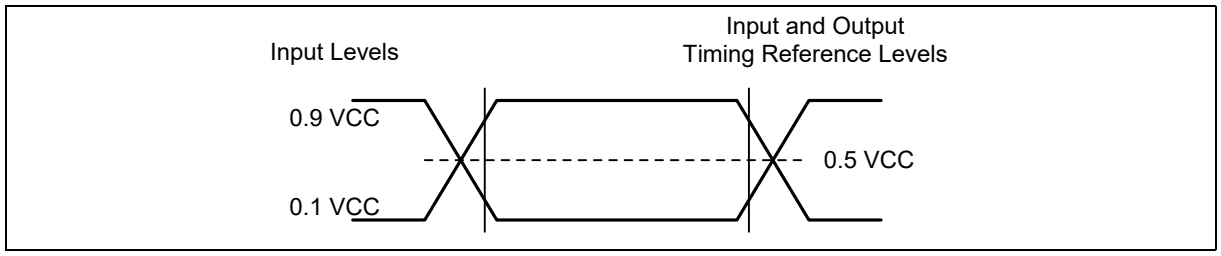


Figure 89: AC Measurement I/O Waveform

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9.5.2 General Characteristics

Table 19 describes the device's general AC characteristics.

Table 19: General Characteristics:

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Write Register Time	t_W			2	30	ms
Page Program Time (256 B)	t_{PP}			0.8	5	ms
Sector Erase Time (4 kB)	t_{SE}(1)			45	400	ms
Block Erase Time (32 kB)	t_{BE1}			120	1600	ms
Block Erase Time (64 kB)	t_{BE2}			200	2000	ms
Chip Erase Time (32Mb/16Mb)	t_{CE}			10/5	50/25	s

[1]Max Value t_{SE} with <50 K cycles is 200 ms and >50 K and <100 K cycles is 400 ms.

9.5.3 SPI Interface Characteristics

Table 20 describes the characteristics of the device's SPI interface.

Table 20: SPI Device Characteristics

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency Read Data (EBh) instruction (<85°C)	F_R	f_{C1}	D.C.		133	MHz
Clock frequency except Read Data (03h) & DTR instructions	F_R	f_{C1}	D.C.		104	MHz
Clock frequency Read Data (EBh) instruction (start address LS bits [1:0]=2'b11)	F_R	f_{C1}	D.C.		80	MHz
Clock frequency for JEDEC ID Read (9Fh) instruction	F_R	f_{C1}	D.C.		80	MHz
Clock frequency for DTR instructions	F_R	f_{C1}	D.C.		66	MHz
Clock frequency for Read data instruction (03h)	f_R	f_{C2}	D.C.		50	MHz
Clock High, Low Time for all instructions except for Read Data (03h)	t_{CLH}, t_{CLL}(1)		45% PC			ns
Clock High, Low Time for Read Data (03h) instruction	t_{CRLH}, t_{CRLL}(1)		45% PC			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
CS# Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	3			ns
CS# Not Active Hold Time relative to CLK	t_{CHSL}		3			ns

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Data In Setup Time	t_{DVCH}	t_{DSU}	1			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
CS# Active Hold Time relative to CLK	t_{CHSH}		3			ns
CS# Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
CS# Deselect Time (following Read)	t_{SHSL1}	t_{CSH}	10			ns
CS# Deselect Time (following Erase or Program or write	t_{SHSL2}	t_{CSH}	50			ns
Output Disable Time	$t_{SHQZ}^{(2)}$	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV}	t_V			6	ns
Output Hold Time	t_{CLQX}	t_{HO}	1.5			ns
HOLD# Active Setup Time relative to CLK	t_{HLCH}		5			ns
HOLD# Active Hold Time relative to CLK	t_{CHHH}		5			ns
HOLD# Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
HOLD# Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
HOLD# to Output Low-Z	$t_{HHQX}^{(2)}$	t_{LZ}			7	ns
HOLD# to Output High-Z	$t_{HLQZ}^{(2)}$	t_{HZ}			12	ns
Write Protect Setup Time Before CS# Low	$t_{WHSL}^{(3)}$		20			ns
Write Protect Hold Time After CS# High	$t_{SHWL}^{(3)}$		100			ns
CS# High to Power-down Mode	$t_{DP}^{(2)}$				3	µs
CS# High to Standby Mode without ID Read	$t_{RES1}^{(2)}$				35	µs
CS# High to next Instruction after Suspend	$t_{SUS}^{(2)}$				20	µs
CS# High to next Instruction after Reset	$t_{RST}^{(2)}$				35	µs
RSTI# / RSTIN# pin Low period to reset the device	$t_{RESET}^{(2)}$		1			µs

Notes:

1. Clock high + Clock low must be less than or equal to 45%Pc. Pc=1/$fc_{(max)}$.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP[1:0]=(0,1).
4. It is possible to reset the device with a shorter t_{RESET} (as short as a few hundred ns). A 1 us minimum is recommended to ensure reliable operation.
5. Tested on sample basis and specified through design and characterization data. T_A=25°, VCC=1.8V, 25% driver strength.
6. 4-Byte address alignment for Quad/QPI Read, start address from A[1:0]=(0,0).

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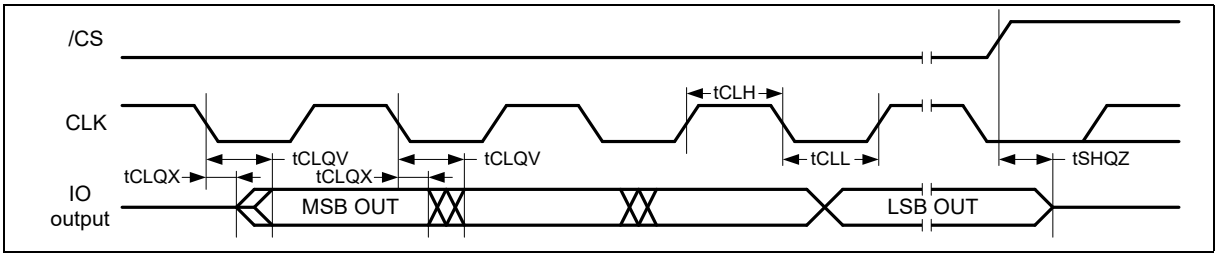


Figure 90: Serial Output Timing

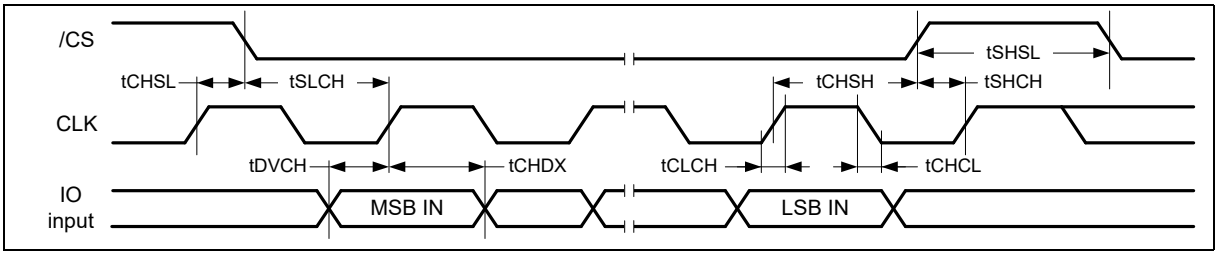


Figure 91: Serial Input Timing

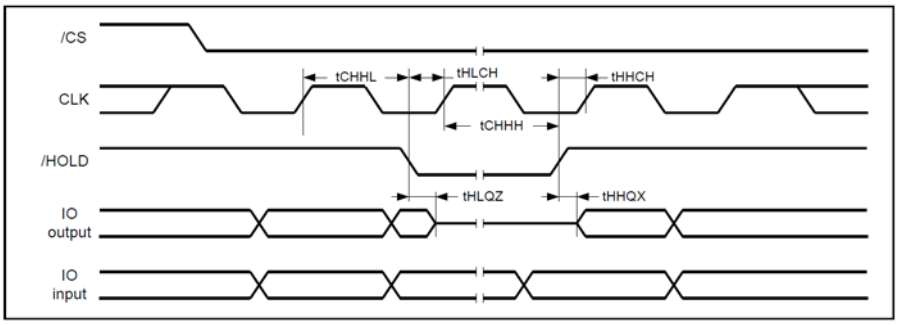


Figure 92: HOLD Timing

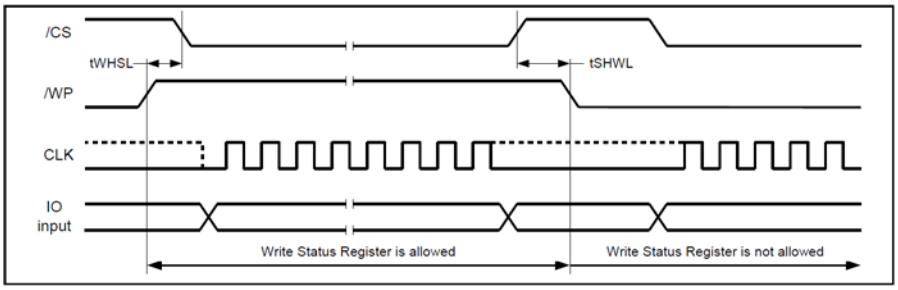
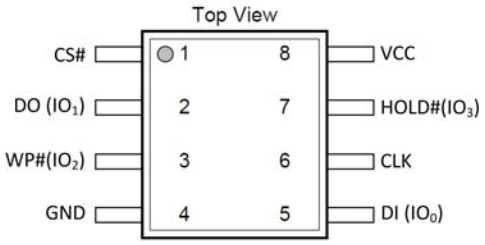


Figure 93: WP Timing

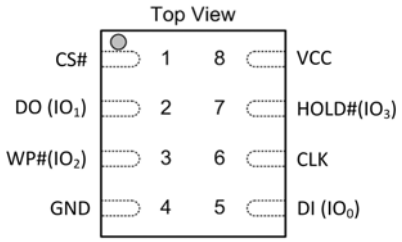
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10 PIN CONFIGURATIONS

10.1 Pin Configuration SOIC8 (208 mil)



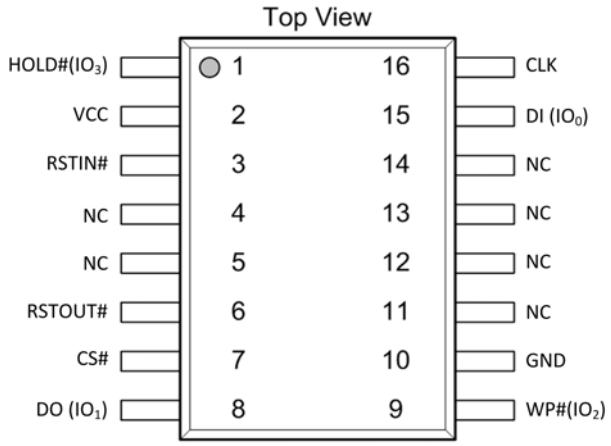
10.2 Pad Configuration WSON8 6x5 mm, XSON8 4x4 mm



PIN NO.	PIN NAME	I/O	FUNCTION
1	CS#	I	Chip Select Input
2	DO / IO1	I/O	Data Out (Single SPI), Data In/Out (Dual/Quad SPI)
3	IO2 / RSTO# / WP#	I/O	Data In/Out (Quad SPI) / Reset Output / Write Protect
4	GND		Common Power Ground
5	DI / IO0	I/O	Data In (Single SPI), Data In/Out (Dual/Quad SPI)
6	CLK	I	Serial Clock Input for SPI interfaces
7	IO3 / RSTI# / HOLD#	I/O	Data In/Out (Quad SPI) / Reset Input / HOLD#
8	VCC		Positive Power Supply

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10.3 Pin Configuration SOIC-16 (300 mil)



PIN NO.	PIN NAME	I/O	FUNCTION
1	IO3 / RSTI# / HOLD#	I/O	Data Input/Output (Quad SPI) / Reset Input / HOLD#
2	VCC		Positive Power Supply
3	RSTIN#	I	Dedicated Reset Input Pin
6	RSTOUT#	O	Dedicated Reset Output Pin
7	CS#	I	Chip Select Input
8	DO / IO1	I/O	Data Out (Single SPI), Data In/Out (Dual/Quad SPI)
9	IO2 / RSTO# / WP#	I/O	Data In/Out (Quad SPI) / Reset Output / Write Protect
10	GND		Common Power Ground
15	DI / IO0	I/O	Data In (Single SPI), Data In/Out (Dual/Quad SPI)
16	CLK	I	Serial Clock Input for SPI interfaces
Other	NC		Not Connected

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10.4 Pin Descriptions

10.4.1 Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation.

When CS# is high, the device is deselected and the Serial Data Output (DO, or IO0-3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress.

When CS# is brought low, the device will be selected, power consumption will increase to active levels, and instructions can be written to and data read from the device.

After power-up, CS# must transition from high to low before a new instruction will be accepted. The CS# input must track the VCC supply level at power-up and power-down (see "Write Protection Features, Figure 86, and Figure 87). If needed, a pull-up resister on the CS# pin can be used to accomplish this.

10.4.2 SPI Serial Data Input, Output and I/Os (DI, DO, IO0-3)

The W77Q32JW/W77Q16JW supports standard SPI, Dual SPI and Quad SPI operation.

Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device. Standard SPI also uses the unidirectional DO (output) to read data or status from the device.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device and read data or status from the device.

Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

Note: For STR (Single Transfer Rate) operations, data is driven on the DI, DO or IO0-3 pins on falling edge of CLK and sampled by the receiver on rising edge of CLK.

10.4.3 Serial Clock (CLK)

The Serial Clock Input (CLK) pin provides the timing for serial input and output operations for the SPI interface.

10.4.4 Write Protect (WP#)

The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected.

The WP# pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the WP# pin function is not available since this pin is used for IO2.

This pin has no effect on secure instructions and advanced write protection mechanisms.

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Note: This pin is available for backwards compatibility purposes, and should not be used by new designs.

10.4.5 HOLD (HOLD#)

The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When HOLD# is brought high, device operation can resume.

The HOLD# function can be useful when multiple devices are sharing the same SPI signals.

The HOLD# pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the HOLD# pin function is not available since this pin is used for IO3.

Note: This pin is available for backwards compatibility purposes, and should not be used by new designs.

10.4.6 Reset In (RSTI#)

The Reset Input pin (RSTI#) is used to hardware reset the device and trigger its reset sequence. This pin should be connected to platform reset.

This pin is active low. When pulled low for a minimum period of approx. 1us, the device will terminate any external or internal operations and return to its power-on state.

This pin is shared with IO3 used for Quad SPI modes. For 8-pin packages, when QE=0, the IO3 pin can be configured either as a HOLD# pin or as a RSTI# pin depending on Status Register setting. When QE=1, the HOLD# or RSTI# pin is not available for 8-pin configuration.

On larger packages, a dedicated RSTIN# pin is provided and it is independent of QE bit setting.

Pin functionality may be forced by RSTI_EN and RSTI_OVRD registers (regardless of the state of the QE bit).

Note: This pin has an internal weak pull-up resistor, and could be left floating or tied to Vcc if unused.

10.4.7 Reset Out (RSTO#)

The Reset Output pin (RSTO#) is provided to the system hardware designers to determine if the device is busy performing device initialization or internal reset. RSTO# pin will be pulled low through the Open-Drain connection during device power-on-reset (POR) period, as well as the device reset period (tRST) triggered by the hardware RSTI# or RSTIN# pins. It may also be triggered by the Authenticated Watchdog Timer function, when the timer expires. The RSTO# pin remains low while the device is executing its internal configuration and initialization.

The RSTO# pin is ***not*** affected by Software Reset (66h+99h instructions).

This pin is active low. While the RSTO# pin is pulled low, no command will be accepted by the device.

This pin is shared with IO2 used for Quad SPI modes. Pin functionality is selected by RSTO_EN register.

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Note: The shared RSTO# pin should not be used in conjunction with the shared RSTI# pin.

10.4.8 Dedicated Reset Input (RSTIN#)

The dedicated reset input pin (not shared with IO3) is available on larger packages (with more than 8 pins).

Note: This pin has an internal pull-up resistor, and could be left floating or tied to Vcc if unused.

See description for Reset In (RSTI#) pin.

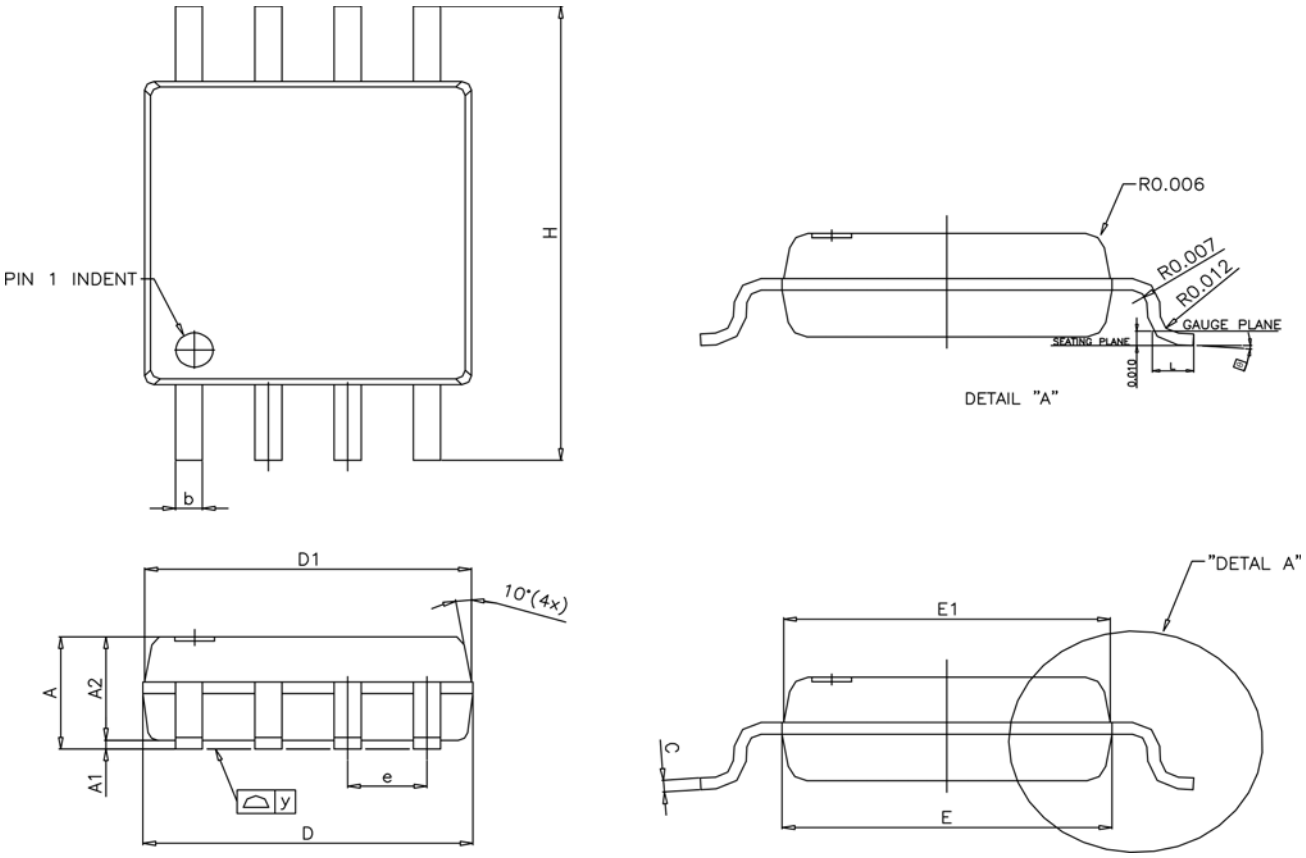
10.4.9 Dedicated Reset Out (RSTOUT#)

The dedicated reset output pin (not shared with IO2) is available on the larger packages (more than 8 pins). This pin is Open-Drain.
See description for Reset Out (RSTO#) pin.

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11 PACKAGE SPECIFICATIONS

11.1 8-Pin SOIC 208-mil (Package Code SS)

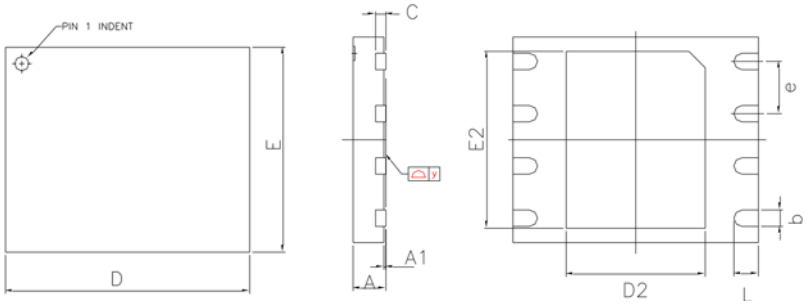


SYMBOL	DIMENSION IN MILLIMETERS			DIMENSION IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
b	0.35	0.42	0.48	0.014	0.017	0.019
C	0.19	0.2	0.25	0.007	0.008	0.010
D	5.18	5.28	5.38	0.204	0.208	0.212
D1	5.13	5.23	5.33	0.202	0.206	0.210
E	5.18	5.28	5.38	0.204	0.208	0.212
E1	5.13	5.23	5.33	0.202	0.206	0.210
e	-------	1.27	-------	-------	0.050	-------
H	7.70	7.90	8.10	0.303	0.311	0.319
L	0.50	0.65	0.80	0.020	0.026	0.031
y	-------	-------	0.10	-------	-------	0.004
θ	0°	-------	8°	0°	-------	8°

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11.2 8-Pad WSON 6x5-mm (Package Code ZP)

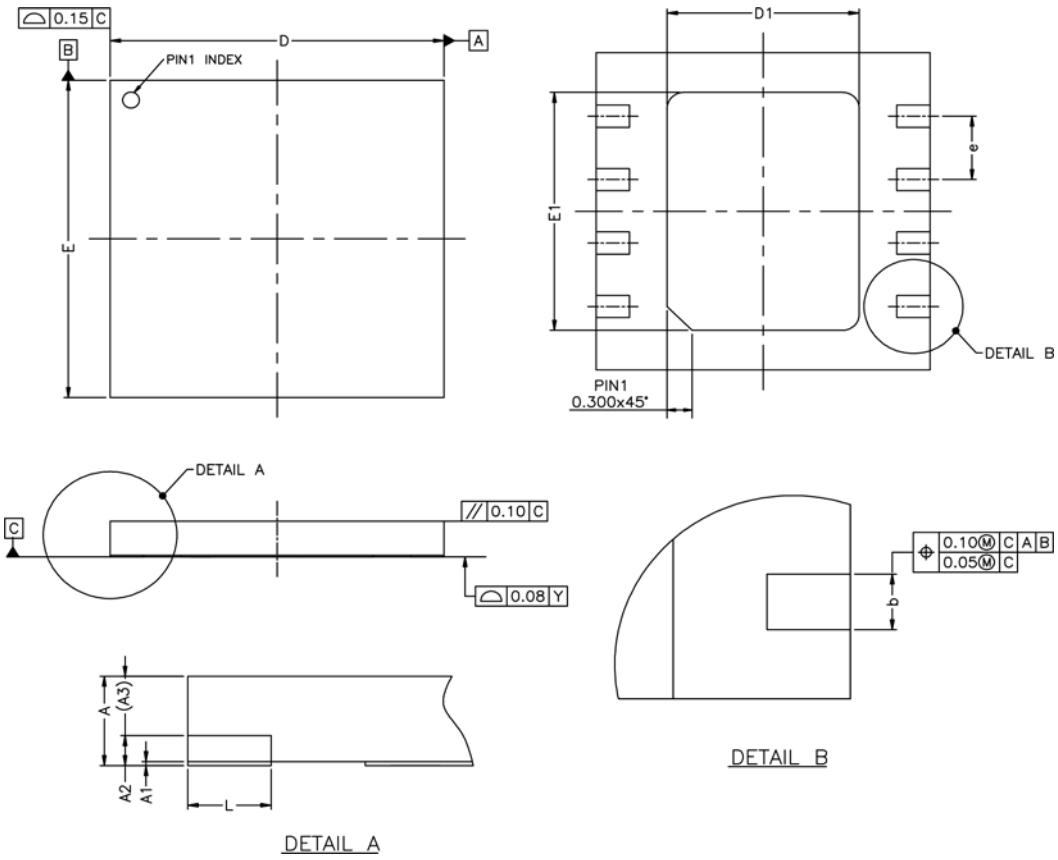
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.00	—	—	0.039
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.75	0.80	0.85	0.030	0.031	0.033
b	0.35	0.42	0.48	0.014	0.017	0.019
c	0.127 REF			0.005 REF		
D	5.18	5.28	5.38	0.204	0.208	0.212
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
e	—	1.27	—	—	0.050	—
L	0.50	0.65	0.80	0.020	0.026	0.031
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.0275	0.0295	0.0314
A1	0.00	0.02	0.05	0.0000	0.0007	0.0019
b	0.35	0.40	0.48	0.0137	0.0157	0.0188
C	——	0.20 REF.	——	——	0.0078REF.	——
D	5.90	6.00	6.10	0.2322	0.2362	0.2401
D2	3.35	3.40	3.45	0.1318	0.1338	0.1358
E	4.90	5.00	5.10	0.1929	0.1968	0.2007
E2	4.25	4.30	4.35	0.1673	0.1692	0.1712
e	——	1.27	——	——	0.05	——
L	0.55	0.60	0.65	0.0216	0.0236	0.0255
y	0.00	——	0.075	0.0000	——	0.0029

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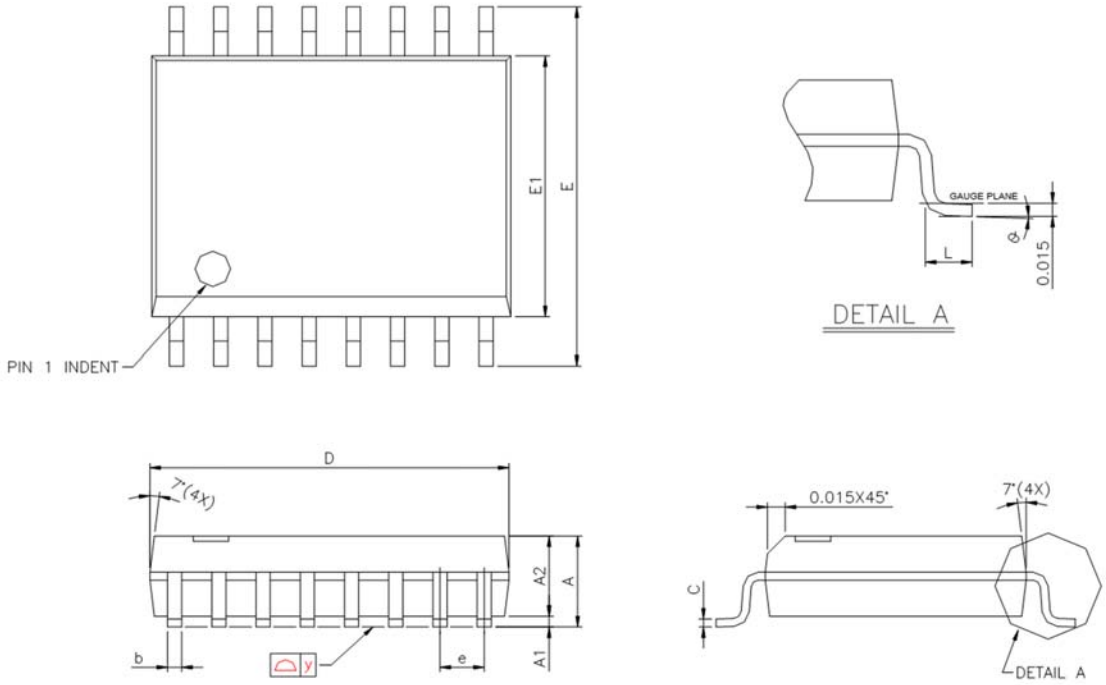
11.3 8-Pad XSON 4x4x0.45-mm (Package Code XG)



SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.40	0.45	0.50	0.0157	0.0177	0.0196
A1	0.00	0.02	0.05	0	0.0007	0.0019
A2	–	0.15	–	–	0.0059	–
A3	0.25	0.30	0.35	0.0098	0.0118	0.0137
b	0.25	0.30	0.35	0.0098	0.0118	0.0137
D	3.90	4.00	4.10	0.1535	0.1574	0.1614
D1	2.20	2.30	2.40	0.0866	0.0905	0.0944
E	3.90	4.00	4.10	0.1535	0.1574	0.1614
E1	2.90	3.00	3.10	0.1141	0.1181	0.1220
e	0.80 BSC			0.0314 BSC		
L	0.35	0.40	0.45	0.0137	0.0157	0.0177

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11.4 16-Pin SOIC 300-mil (Package Code SF)

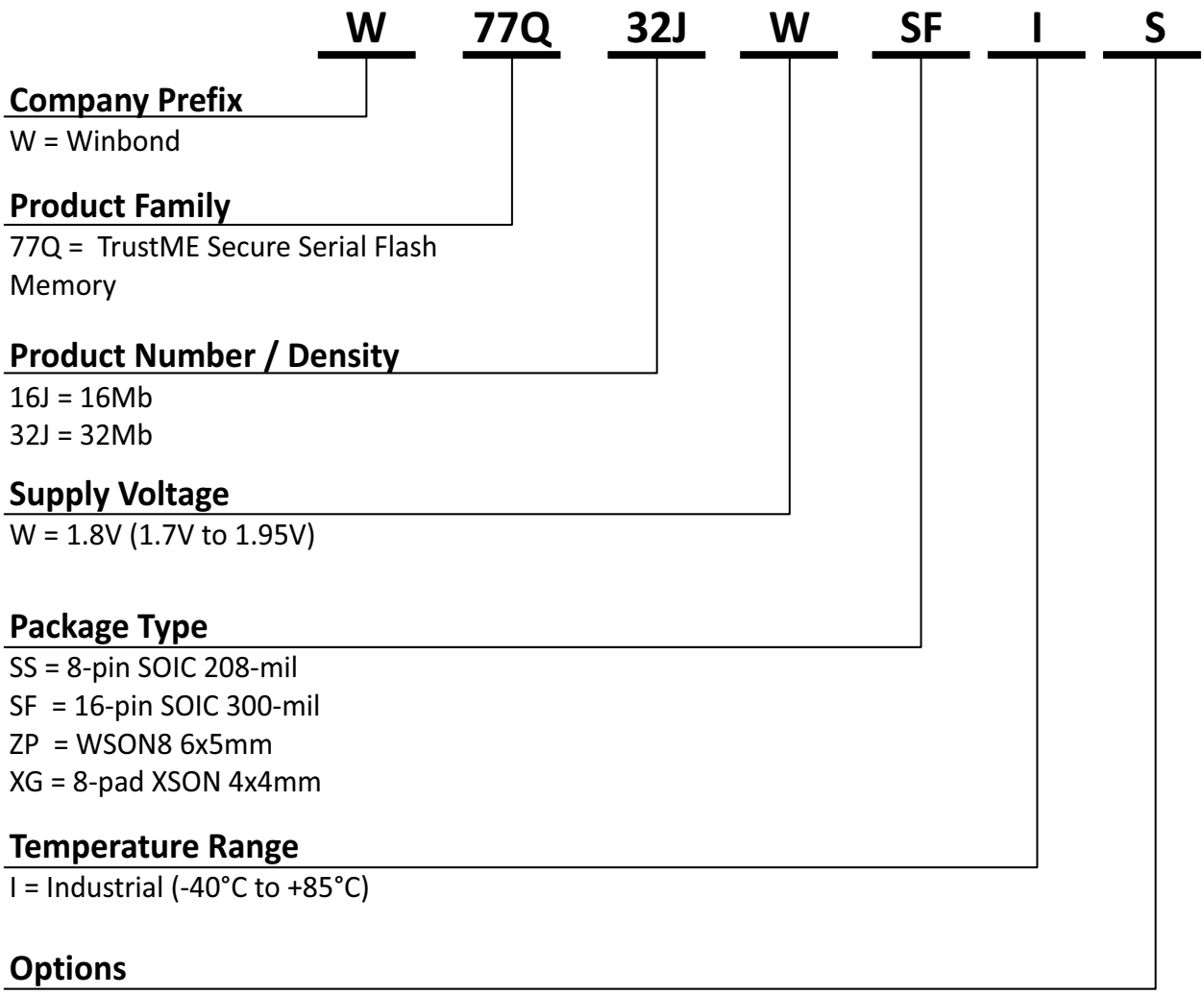


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	——	0.30	0.004	——	0.012
A2	——	2.31	——	——	0.091	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	10.08	10.31	10.49	0.397	0.406	0.413
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	——	1.27	——	——	0.050	——
L	0.38	0.81	1.27	0.015	0.032	0.050
y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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12. ORDERING INFORMATION

12.1 Product Number Encoding



Standard bulk shipments are in Tube (shape E).
Specify an alternative packing method, such as Tape and Rell (shape T), or Tray (shape S) when placing orders.

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12.2 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W77Q32JW/W77Q16JW Secure Serial NOR Flash Memory. Please contact Winbond for specific availability by density and package type and for other available options.

Winbond Secure Serial NOR Flash memories use the full part number for ordering. However, due to limited space, the top side marking on all packages is abbreviated as listed in the table.

Table 21: Valid Part Numbers and Top Side Marking

PACKAGE	DENSITY	PART NUMBER	TOP SIDE MARKING
SOIC16 300-mil	32Mb	W77Q32JWSFIS	77Q32JWSFIS
		W77Q32JWSFIO	77Q32JWSFIO
		W77Q32JWSFIN	77Q32JWSFIN
SOIC8 208-mil	16Mb	W77Q16JWSSIR	77Q16JWSSIR
		W77Q16JWSSIQ	77Q16JWSSIQ
	32Mb	W77Q32JWSSIR	77Q32JWSSIR
		W77Q32JWSSIQ	77Q32JWSSIQ
		W77Q32JWSSIN	77Q32JWSSIN
WSON8 6x5	16Mb	W77Q16JWZPIR	77Q16JWZPIR
		W77Q16JWZPIQ	77Q16JWZPIQ
	32Mb	W77Q32JWZPIR	77Q32JWZPIR
		W77Q32JWZPIQ	77Q32JWZPIQ
XSON8 4x4	32Mb	W77Q32JWXGIR	77Q32JWXGIR
		W77Q32JWXGIQ	77Q32JWXGIQ

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Document Revision History

REVISION	DATE	MODIFICATIONS
A	18-Dec-19	• Preliminary revision
A1	8-March-20	• Minor updates and clarifications.
A2	24-May-20	• Updated naming rule and Electrical Characteristics.
A3	23-July-20	• Updated naming rules • Updated Power-Up & Power-Down Timing and Requirements • Updated AC Timing (tCHDX)
A4	3-Aug-20	• Note on using Standard Write Protection with Security features
A5	17-Jan-21	• Electrical Characteristics: updated Icc1, Icc2, F_R • Updated Standard Serial Flash Instruction Set Tables • 16-Pin SOIC 300-mil (Package Code SF)
A6	11-Feb-21	• AC Electrical Characteristics - updated Icc6 and Icc7 • Valid Part Numbers and Top Side Marking - updated SpiStack™
A7	14-March-21	• Declassified Data-Sheet
A8	12-April-21	• Removed “Preliminary” notice • Updated SFDP Table • Removed SpiStack™ • Ordering Information - naming rule updated • Reset Out (RSTO#) - note about SW Reset
A9	29-April-21	• Clarified Standard-Flash Write Protection mapping to physical/logical memory
B	30-June-21	• Updated ordering information
C	17-Jan-22	• Reset In (RSTI#) has an internal pull-up • Set Read Parameters (C0h) - 2 dummy cycles are not supported • Set Burst with Wrap (77h) always drives 24 dummy bits • Removed automotive and wireless temperature ranges • Removed 8-Pin VSOP 208-mil package • Updated tce • Removed the SFDP table specification from Section 7. It is now specified in an application note. • Updated ordering information • Technical editing and formatting

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REVISION	DATE	MODIFICATIONS
C1	11-Apr-22	• Updated the enumerations for Output Driver Strength in Section 8.2.3.3 • Updated Icc2 • Added “N” ordering option for 75% Output Driver Strength and QE=1 fixed • Removed unsupported packages • Updated Ordering Information • Technical editing and formatting
D	9-May-22	• Updated the enumerations for Output Driver Strength in Section 8.2.3.3 • Updated Icc2 • Added “N” ordering option for 75% Output Driver Strength and QE=1 fixed • Removed unsupported packages • Updated Ordering Information • Technical editing and formatting
E	2-Apr-23	• Updated certification status • Block Diagram - added a diagram to describe the logical address space • Added Plain Access Memory Addressing section • Removed Host Software Reset functionality in Section 6.11 • Updated Icc1 and Icc2 • Updated tchsl description and waveform

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