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## 1. GENERAL DESCRIPTION

This LPDDR3 is a high-speed SDRAM device internally configured as an 8-Bank memory and contains 1,073,741,824 bits.

This LPDDR3 device uses a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

## 2. FEATURES

- $V_{DD1}$ = 1.7~1.95V
- $V_{DD2}$/$V_{DDCA}$/ $V_{DDQ}$ = 1.14V~1.30V
- Data width: x16 / x32
- Clock rate: up to 1066 MHz
- Data rate: up to 2133 Mbps
- 8 internal banks for concurrent operation
- 8*n* pre-fetch operation
- Burst length: 8
- Per Bank Refresh
- Partial Array Self-Refresh(PASR)
- On-die termination (ODT)
- Deep Power Down Mode (DPD Mode)
- Double data rate architecture
- Clock Stop capability
- Programmable Read and Write Latencies (RL/WL)
- Bidirectional differential data strobe
- Support Boundary Scan for connectivity test*
- Support package:
  VFBGA178 (11mm x11.5mm)
- Operating Temperature Range:
  -25°C ≤ $T_{CASE}$ ≤ 85°C
  -40°C ≤ $T_{CASE}$ ≤ 85°C

* For further information about Boundary Scan for connectivity test, please contact sales representative.

## 3. ORDER INFORMATION

| Part Number | VDD1/VDD2/VDDQ | I/O Width | Type | Others |
|---|---|---|---|---|
| W63AH6NBVABE | 1.8V/1.2V/1.2V | 16 | VFBGA178 | LPDDR3-1600, -25°C~85°C |
| W63AH6NBVACE | 1.8V/1.2V/1.2V | 16 | VFBGA178 | LPDDR3-1866, -25°C~85°C |
| W63AH6NBVADE | 1.8V/1.2V/1.2V | 16 | VFBGA178 | LPDDR3-2133, -25°C~85°C |
| W63AH6NBVABI | 1.8V/1.2V/1.2V | 16 | VFBGA178 | LPDDR3-1600, -40°C~85°C |
| W63AH6NBVACI | 1.8V/1.2V/1.2V | 16 | VFBGA178 | LPDDR3-1866, -40°C~85°C |
| W63AH6NBVADI | 1.8V/1.2V/1.2V | 16 | VFBGA178 | LPDDR3-2133, -40°C~85°C |
| W63AH2NBVABE | 1.8V/1.2V/1.2V | 32 | VFBGA178 | LPDDR3-1600, -25°C~85°C |
| W63AH2NBVACE | 1.8V/1.2V/1.2V | 32 | VFBGA178 | LPDDR3-1866, -25°C~85°C |
| W63AH2NBVADE | 1.8V/1.2V/1.2V | 32 | VFBGA178 | LPDDR3-2133, -25°C~85°C |
| W63AH2NBVABI | 1.8V/1.2V/1.2V | 32 | VFBGA178 | LPDDR3-1600, -40°C~85°C |
| W63AH2NBVACI | 1.8V/1.2V/1.2V | 32 | VFBGA178 | LPDDR3-1866, -40°C~85°C |
| W63AH2NBVADI | 1.8V/1.2V/1.2V | 32 | VFBGA178 | LPDDR3-2133, -40°C~85°C |


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## 4. BALL ASSIGNMENT

**[Top View]**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | DNU | DNU | VDD1 | VDD1 | VDD1 | VDD1 | | VDD2 | VDD2 | VDD1 | VDDQ | DNU | DNU | A |
| B | DNU | VSS | ZQ | NC | VSS | VSS | | DQ31<br>NC | DQ30<br>NC | DQ29<br>NC | DQ28<br>NC | VSS | DNU | B |
| C | | CA9 | VSS | NC | VSS | VSS | | DQ27<br>NC | DQ26<br>NC | DQ25<br>NC | DQ24<br>NC | VDDQ | | C |
| D | | CA8 | VSS | VDD2 | VDD2 | VDD2 | | DM3<br>NC | DQ15 | DQS3_t<br>NC | DQS3_c<br>NC | VSS | | D |
| E | | CA7 | CA6 | VSS | VSS | VSS | | VDDQ | DQ14 | DQ13 | DQ12 | VDDQ | | E |
| F | | VDDCA | CA5 | VSS | VSS | VSS | | DQ11 | DQ10 | DQ9 | DQ8 | VSS | | F |
| G | | VDDCA | VSS | VSS | VDD2 | VSS | | DM1 | VSS | DQS1_t | DQS1_c | VDDQ | | G |
| H | | VSS | VDDCA | VREF(CA) | VDD2 | VDD2 | | VDDQ | VDDQ | VSS | VDDQ | VDD2 | | H |
| J | | CK_c | CK_t | VSS | VDD2 | VDD2 | | ODT | VDDQ | VDDQ | VREF(DQ) | VSS | | J |
| K | | VSS | CKE | NC | VDD2 | VDD2 | | VDDQ | NC | VSS | VDDQ | VDD2 | | K |
| L | | VDDCA | CS_n | NC | VDD2 | VSS | | DM0 | VSS | DQS0_t | DQS0_c | VDDQ | | L |
| M | | VDDCA | CA4 | VSS | VSS | VSS | | DQ4 | DQ5 | DQ6 | DQ7 | VSS | | M |
| N | | CA2 | CA3 | VSS | VSS | VSS | | VDDQ | DQ1 | DQ2 | DQ3 | VDDQ | | N |
| P | | CA1 | VSS | VDD2 | VDD2 | VDD2 | | DM2<br>NC | DQ0 | DQS2_t<br>NC | DQS2_c<br>NC | VSS | | P |
| R | | CA0 | SEN | VSS | VSS | VSS | | DQ20<br>NC | DQ21<br>NC | DQ22<br>NC | DQ23<br>NC | VDDQ | | R |
| T | DNU | VSS | VSS | VSS | VSS | VSS | | DQ16<br>NC | DQ17<br>NC | DQ18<br>NC | DQ19<br>NC | VSS | DNU | T |
| U | DNU | DNU | VDD1 | VDD1 | VDD1 | VDD1 | | VDD2 | VDD2 | VDD1 | VDDQ | DNU | DNU | U |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |

| Ball Definition where 2 labels are present | |
|---|---|
| 1st Row<br>2nd Row | x32 device<br>x16 device |

| | |
|---|---|
| | Boundary Scan Enable |
| | Power |
| | Ground |
| | DQ/DQS DM |
| | CA/CS_n CKE |
| | Clock |
| | ODT |
| | ZQ |
| | Do Not Use NC |

**VFBGA178 Ball Assignments**


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# 5. BALL CONFIGURATION

## 5.1 Ball description

| Name | Type | Description |
|---|---|---|
| CK_t, CK_c | Input | **Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge.<br>Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c. |
| CKE | Input | **Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions.<br>CKE is considered part of the command code. See 7.5.1 **"Command Truth Table"** for command code descriptions.<br>CKE is sampled at the positive Clock edge. |
| CS_n | Input | **Chip Select:** CS_n is considered part of the command code. See 7.5.1 **"Command Truth Table"** for command code descriptions.<br>CS_n is sampled at the positive Clock edge. |
| CA[9:0] | Input | **DDR Command/Address Inputs:** Uni-directional command/address bus inputs.<br>CA is considered part of the command code. See 7.5.1 **"Command Truth Table"** for command code descriptions. |
| DQ[n:0] | I/O | **Data Inputs/Output:** Bi-directional data bus. DQ[15:0] for x16, DQ[31:0] for x32. |
| DQSn_t, DQSn_c | I/O | **Data Strobe (Bi-directional, Differential):**<br>The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data.<br>For x16, DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15.<br>For x32 DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15; DQS2_t and DQS2_c to the data on DQ16-23; DQS3_t and DQS3_c to the data on DQ24-31. |
| DMn | Input | **Input Data Mask:**<br>DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS_c).<br>For x16 and x32 devices, DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-15.<br>For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31. |
| ODT | Input | **On-Die Termination:** This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings. |
| $V_{DD1}$ | Supply | **Core Power Supply 1:** Core Power supply. |
| $V_{DD2}$ | Supply | **Core Power Supply 2:** Core Power supply. |
| $V_{DDCA}$ | Supply | **Input Receiver Power Supply:** Power supply for CA[9:0], CKE, CS_n, CK_t, and CK_c input buffers. |
| $V_{DDQ}$ | Supply | **I/O Power Supply:** Power supply for Data input/output buffers. |
| $V_{REF(CA)}$ | Supply | **Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA[9:0], CKE, CS_n, CK_t, and CK_c input buffers. |
| $V_{REF(DQ)}$ | Supply | **Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers. |
| $V_{SS}$ | Supply | **Ground:** Ground of core logic, input receivers and data input/output buffers. |
| ZQ | I/O | **Reference Pin for Output Drive Strength Calibration** |
| SEN | Input | **Scan Enable**: SEN must be asserted HIGH for enabling boundary scan function. Must be tied to Ground or NC (No Connection) when not in use. |
| NC | -- | **No Connection** |
| DNU | -- | **Do Not Use** |

**Note:** Data includes DQ and DM.


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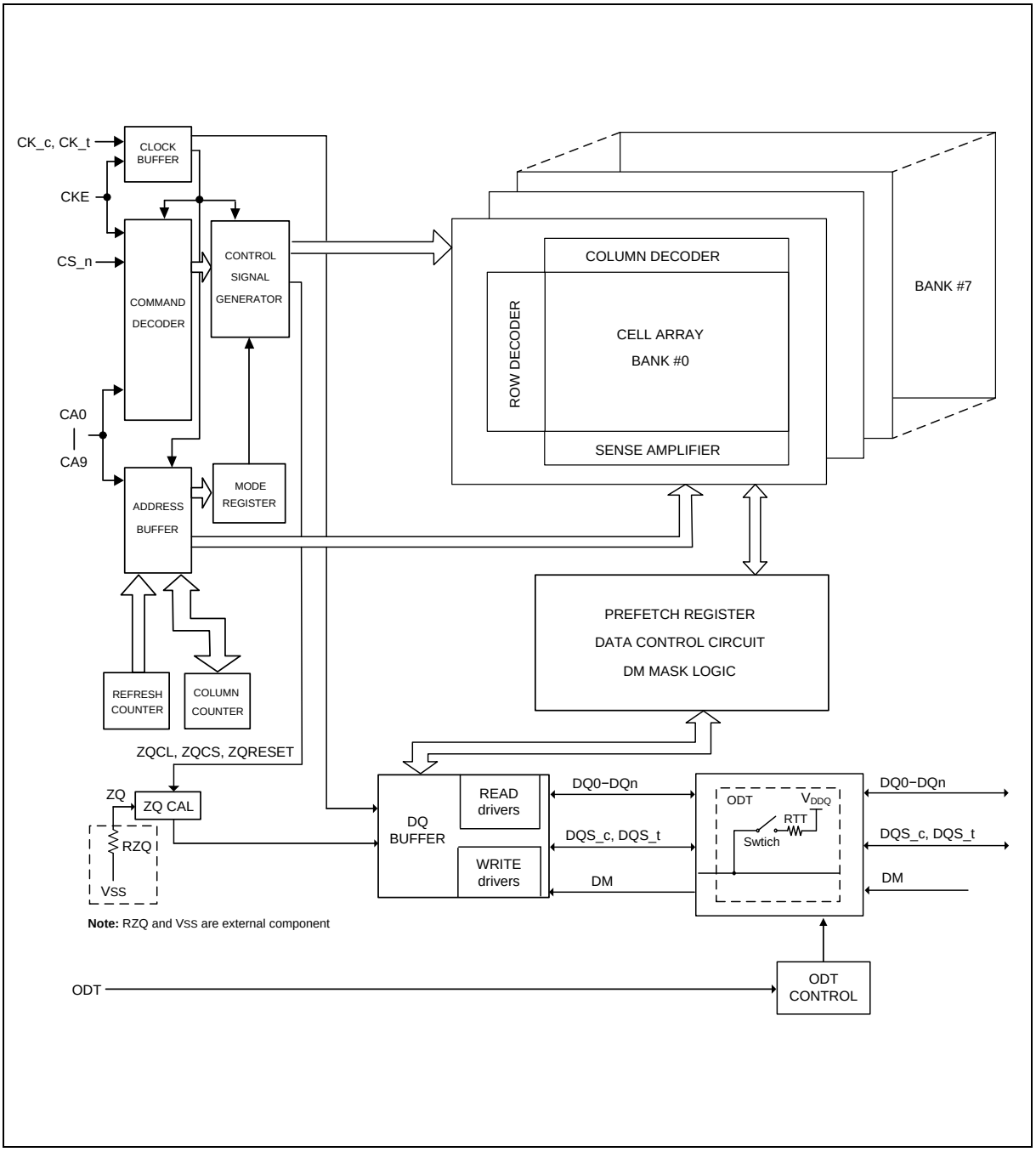
## 5.2 Addressing Table

| Density | | 1Gb |
|---|---|---|
| Number of Banks | | 8 |
| Bank Addresses | | BA0-BA2 |
| x16 | Row Addresses | R0-R12 |
| | Column Addresses*1 | C0-C9 |
| x32 | Row Addresses | R0-R12 |
| | Column Addresses*1 | C0-C8 |

**Notes:**

1. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
2. Row and Column Address values on the CA bus that are not used are “don’t care”.

## 6. BLOCK DIAGRAM




**Note:** RZQ and VSS are external component

# 7. FUNCTIONAL DESCRIPTION

For this LPDDR3 device, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

This device also uses double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 8*n* prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR3 SDRAM effectively consists of a single 8*n*-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to this LPDDR3 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Prior to normal operation, this LPDDR3 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

## 7.1 Simplified LPDDR3 State Diagram

LPDDR3-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see chapter 7.4 **"Command Definitions and Timing Diagrams"**.


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### 7.1.1 Simplified Bus Interface State Diagram

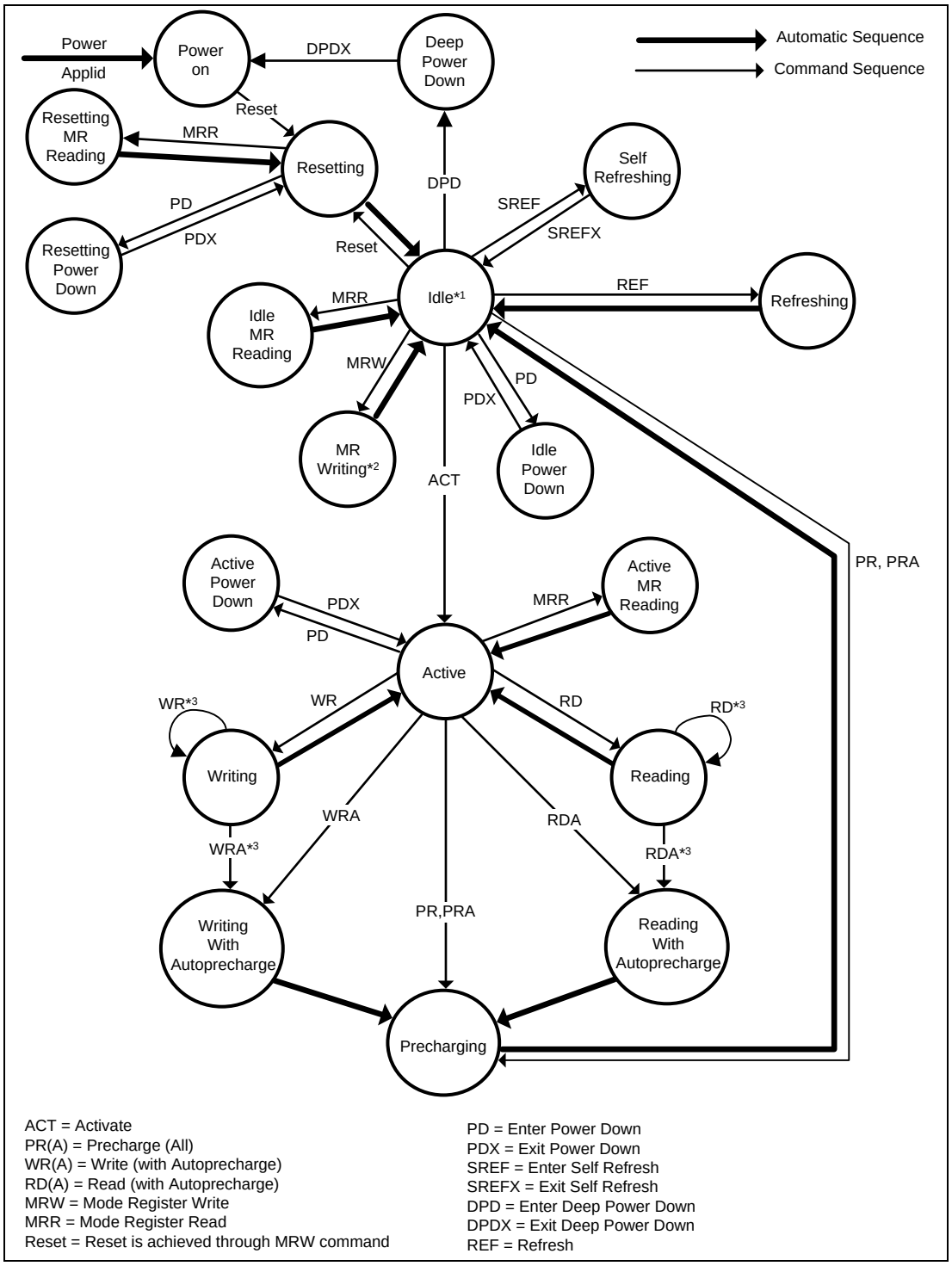



**Figure 1: Simplified Bus Interface State Diagram**

**Notes:**

1. In the Idle state, all banks are precharged.
2. In the case of MRW to enter CA Training mode or Write Leveling Mode, the state machine will not automatically return to the Idle state. In these cases an additional MRW command is required to exit either operating mode and return to the idle state. See the “CA Training Mode” or “Write Leveling Mode” sections.
3. Terminated bursts are not allowed. For these state transitions, the burst operation must be completed before the transition can occur.
4. Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one bank are not captured in full detail.

## 7.2 Power-up, Initialization, and Power-Off

### 7.2.1 Voltage Ramp and Device Initialization

The following sequence must be used to power up LPDDR3 device. Unless specified otherwise, this procedure is mandatory.

**1. Voltage Ramp**

While applying power (after Ta), CKE must be held LOW (≤ 0.2 × $V_{DDCA}$) and all other inputs must be between $V_{ILmin}$ and $V_{IHmax}$. The device outputs remain at High-Z while CKE is held LOW.

Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS_t and DQS_c voltage levels must be between VSS and $V_{DDQ}$ during voltage ramp to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between VSS and $V_{DDCA}$ during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in Table below.

**Voltage Ramp Conditions**

| After… | Applicable Conditions |
|---|---|
| Ta is reached | $V_{DD1}$ must be greater than $V_{DD2}$—200mV |
| | $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDCA}$—200mV |
| | $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDQ}$—200mV |
| | $V_{REF}$ must always be less than all other supply voltages |

**Notes:**

1. Ta is the point when any power supply first reaches 300 mV.
2. Noted conditions apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined operating ranges.
4. Power ramp duration $t_{INIT0}$ (Tb - Ta) must not exceed 20 mS.
5. The voltage difference between of VSS pin must not exceed 100 mV.

Beginning at Tb, CKE must remain LOW for at least $t_{INIT1}$, after which CKE can be asserted HIGH. The clock must be stable at least $t_{INIT2}$ prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS_n, and CA inputs must observe setup and hold requirements ($t_{IS}$, $t_{IH}$) with respect to the first rising clock edge (as well as to subsequent falling and rising edges).

If any MRR commands are issued, the clock period must be within the range defined for $t_{CKb}$. MRW commands can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, $t_{DQSCK}$) could have relaxed timings (such as $t_{DQSCKb}$) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least $t_{INIT3}$ (Td). The ODT input signal may be in undefined state until $t_{IS}$ before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal shall be statically held at either LOW or HIGH. The ODT input signal remains static until the power up initialization sequence is finished, including the expiration of $t_{ZQINIT}$.

**2. RESET Command:**

After $t_{INIT3}$ is satisfied, the MRW RESET command must be issued (Td).

A PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least $t_{INIT4}$ while keeping CKE asserted and issuing NOP commands. Only NOP commands are allowed during time $t_{INIT4}$.


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### 3. MRRs and Device Auto Initialization (DAI) Polling:

After tINIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications. MRR commands are only valid at this time if the CA bus does not need to be trained. CA Training may only begin after time Tf. User may issue MRR command to poll the DAI bit which will indicate if device auto initialization is complete; once DAI bit indicates completion, SDRAM is in idle state. Device will also be in idle state after tINIT5(max) has expired (whether or not DAI bit has been read by MRR command). As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured.

After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than tINIT5 after the RESET command. The controller must wait at least tINIT5(max) or until the DAI bit is set before proceeding.

### 4. ZQ Calibration:

If CA Training is not required, the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10) after time Tf. If CA Training is required, the CA Training may begin at time Tf. No other CA commands (other than RESET or NOP) may be issued prior to the completion of CA Training. At the completion of CA Training (Tf'), the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10).

This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after tZQINIT.

### 5. Normal Operation:

After tZQINIT (Tg), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in this specification.

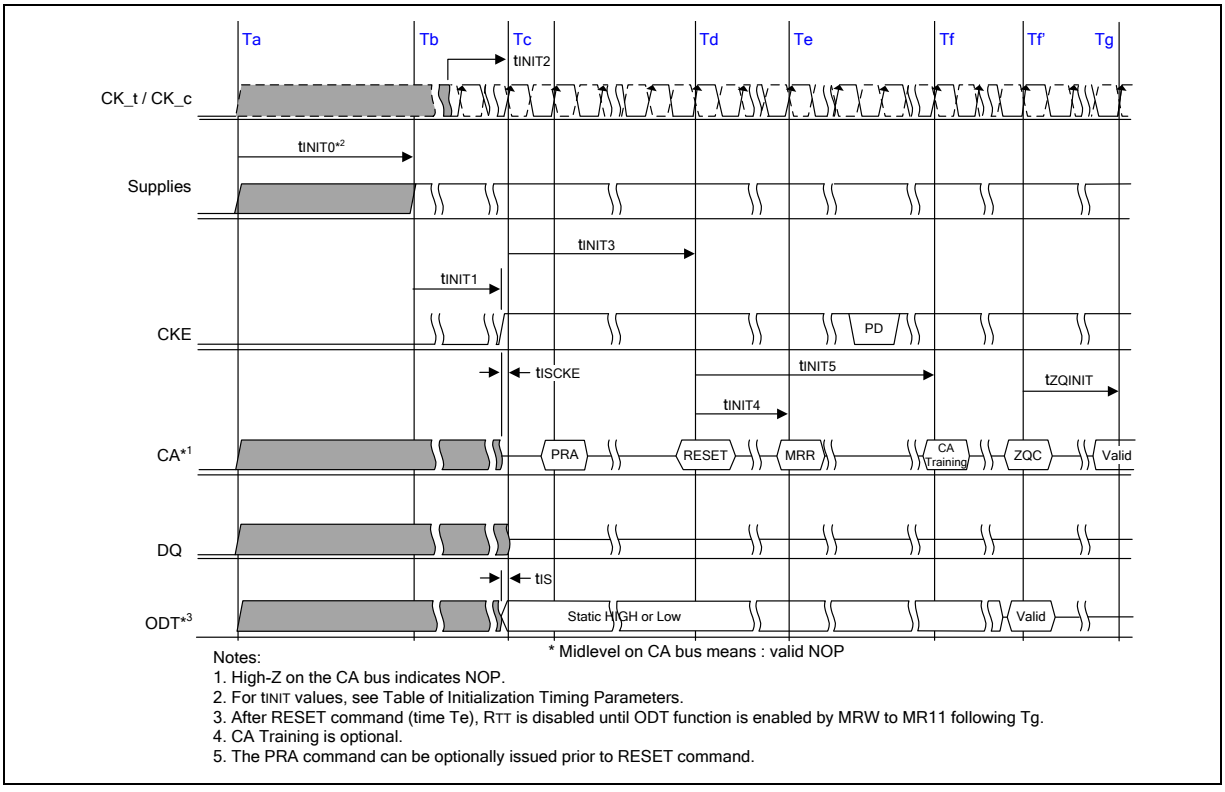



**Figure 2: Voltage Ramp and Initialization Sequence**

**Initialization Timing Parameters**

| Parameter | Value | | Unit | Comment |
|---|---|---|---|---|
| | Min | Max | | |
| tINIT0 | - | 20 | mS | Maximum voltage-ramp time |
| tINIT1 | 100 | - | nS | Minimum CKE LOW time after completion of voltage ramp |
| tINIT2 | 5 | - | tCK | Minimum stable clock before first CKE HIGH |
| tINIT3 | 200 | - | µS | Minimum idle time after first CKE assertion |
| tINIT4 | 1 | - | µS | Minimum idle time after RESET command |
| tINIT5*[1] | - | 10 | µS | Maximum duration of device auto initialization |
| tZQINIT | 1 | - | µS | ZQ initial calibration |
| tCKb | 18 | 100 | nS | Clock cycle time during boot |

**Note:**

1. If DAI bit is not read via MRR, SDRAM will be in idle state after tINIT5(max) has expired.

### 7.2.2 Initialization after Reset (without Power ramp)

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

### 7.2.3 Power-off Sequence

The following procedure is required to power off the device.

While power off, CKE must be held LOW (≤ 0.2 x VDDCA), all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS_t and DQS_c voltage levels must be between VSS and VDDQ during power-off sequence to avoid latch-up. CK_t, CK_c, CS_n and CA input levels must be between VSS and VDDCA during power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

**Power Supply conditions**

| Between… | Applicable Conditions |
|---|---|
| Tx and Tz | VDD1 must be greater than VDD2—200 mV |
| Tx and Tz | VDD1 must be greater than VDDCA—200 mV |
| Tx and Tz | VDD1 must be greater than VDDQ—200 mV |
| Tx and Tz | VREF must always be less than all other supply voltages |

The voltage difference between of VSS pin must not exceed 100 mV.

### 7.2.4 Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300 mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/µS between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

**Timing Parameters Power-Off**

| Symbol | Value | | Unit | Comment |
|---|---|---|---|---|
| | min | max | | |
| tPOFF | - | 2 | S | Maximum Power-Off Ramp Time |


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## 7.3 Mode Register Definition

### 7.3.1 Mode Register Assignment and Definition

The table listed below shows the mode registers for LPDDR3 SDRAM. Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

#### 7.3.1.1 Mode Register Assignment

| MR# | MA[7:0] | Function | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | $00_H$ | Device Info. | R | RL3 | WL (Set B) | (RFU) | RZQI | | (RFU) | | DAI |
| 1 | $01_H$ | Device Feature 1 | W | nWR (for AP) | | | (RFU) | | BL | | |
| 2 | $02_H$ | Device Feature 2 | W | WR Lev | WL Select | (RFU) | nWRE | RL & WL | | | |
| 3 | $03_H$ | I/O Config-1 | W | (RFU) | | | | DS | | | |
| 4 | $04_H$ | Refresh Rate | R | TUF | (RFU) | | | | Refresh Rate | | |
| 5 | $05_H$ | Basic Config-1 | R | Manufacturer ID | | | | | | | |
| 6 | $06_H$ | Basic Config-2 | R | Revision ID1 | | | | | | | |
| 7 | $07_H$ | Basic Config-3 | R | Revision ID2 | | | | | | | |
| 8 | $08_H$ | Basic Config-4 | R | I/O width | | Density | | | | Type | |
| 9 | $09_H$ | (Reserved) | W | (RFU) | | | | | | | |
| 10 | $0A_H$ | I/O Calibration | W | Calibration Code | | | | | | | |
| 11 | $0B_H$ | ODT Feature | - | (RFU) | | | | | PD CTL | DQ ODT | |
| 12:15 | $0C_H$~$0F_H$ | (Reserved) | - | (RFU) | | | | | | | |
| 16 | $10_H$ | PASR_Bank | W | PASR Bank Mask | | | | | | | |
| 17 | $11_H$ | PASR_Seg | W | PASR Segment Mask | | | | | | | |
| 18-31 | $12_H$~$1F_H$ | (Reserved) | - | (RFU) | | | | | | | |
| 32 | 20H | DQ Calibration Pattern A | R | DQ Calibration Pattern A | | | | | | | |
| 33:39 | $21_H$~$27_H$ | (Do Not Use) | - | | | | | | | | |
| 40 | 28H | DQ Calibration Pattern B | R | DQ Calibration Pattern B | | | | | | | |
| 41 | 29H | CA Training 1 | W | CA Training 1 | | | | | | | |
| 42 | 2AH | CA Training 2 | W | CA Training 2 | | | | | | | |
| 43:47 | $2B_H$~$2F_H$ | (Do Not Use) | - | | | | | | | | |
| 48 | 30H | CA Training 3 | W | CA Training 3 | | | | | | | |
| 49:62 | $31_H$~$3E_H$ | (Reserved) | - | (RFU) | | | | | | | |
| 63 | 3FH | Reset | W | X | | | | | | | |
| 64:255 | $40_H$~$FF_H$ | (Reserved) | - | (RFU) | | | | | | | |

**Notes:**

1. RFU bits shall be set to ‘0’ during mode register writes.
2. RFU bits shall be read as ‘0’ during mode register reads.
3. All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
4. All mode registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.


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### 7.3.2 MR0_Device Information (MA[7:0] = 00H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| RL3 | WL (Set B) Support | (RFU) | RZQI | | (RFU) | | DAI |

| | | | | |
|---|---|---|---|---|
| DAI (Device Auto-Initialization Status) | Read-only | OP0 | **$0_b$:** DAI complete<br>**$1_b$:** DAI still in progress | |
| RZQI<br>(Built in Self Test for RZQ Information) | Read-only | OP[4:3] | **$00_b$:** RZQ self test not executed.<br>**$01_b$:** ZQ-pin may connect to VDDCA or float<br>**$10_b$:** ZQ-pin may short to GND<br>**$11_b$:** ZQ-pin self test completed, no error condition detected<br>(ZQ-pin may not connect to VDDCA or float nor short to GND) | 1-4 |
| WL (Set B) Support | Read-only | OP[6] | **$0_b$:** DRAM does not support WL (Set B) | |
| RL3 Option Support | Read-only | OP[7] | **$0_b$:** DRAM does not support<br>RL=3, nWR=3, WL=1 | |

**Notes:**

1. RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.
2. If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR3 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ±1%).

### 7.3.3 MR1_Device Feature 1 (MA[7:0] = 01H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| nWR (for AP) | | | (RFU) | | BL | | |

| | | | | |
|---|---|---|---|---|
| BL | Write-only | OP[2:0] | **$011_b$:** BL8 (default)<br>**All others:** Reserved | |
| nWR | Write-only | OP[7:5] | If nWRE (MR2 OP<4>) = 0<br>**$001_b$:** nWR=3<br>**$100_b$:** nWR=6<br>**$110_b$:** nWR=8<br>**$111_b$:** nWR=9<br>If nWRE (MR2 OP<4>) = 1<br>**$000_b$:** nWR=10 (default)<br>**$001_b$:** nWR=11<br>**$010_b$:** nWR=12<br>**$100_b$:** nWR=14<br>**$110_b$:** nWR=16<br>**All others:** Reserved | 1 |

**Note:**

1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).


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#### 7.3.3.1 Burst Sequence

| C2 | C1 | C0 | BL | Burst Cycle Number and Burst Address Sequence | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| $0_b$ | $0_b$ | $0_b$ | 8 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| $0_b$ | $1_b$ | $0_b$ | | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 |
| 1b | $0_b$ | $0_b$ | | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| $1_b$ | $1_b$ | $0_b$ | | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 |

**Notes:**

1. C0 input is not present on CA bus. It is implied zero.
2. The burst address represents C2 – C0.

### 7.3.4 MR2_Device Feature 2 (MA[7:0] = 02H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| WR Lev | WL Select | (RFU) | nWRE | RL & WL | | | |

| | | | |
|---|---|---|---|
| RL & WL | Write-only | OP[3:0] | OP<6>=0 (WL Set A, default)<br>**$0001_b$:** (Reserved)<br>**$0100_b$:** RL = 6 / WL = 3 (≤400 MHz)<br>**$0110_b$:** RL = 8 / WL = 4 (≤533 MHz)<br>**$0111_b$:** RL = 9 / WL = 5 (≤600 MHz)<br>**$1000_b$:** RL = 10 / WL = 6 (≤667 MHz, default)<br>**$1001_b$:** RL = 11 / WL = 6 (≤733 MHz)<br>**$1010_b$:** RL = 12 / WL = 6 (≤800 MHz)<br>**$1100_b$:** RL = 14 / WL = 8 (≤933 MHz)<br>**$1110_b$:** RL = 16 / WL = 8 (≤1066 MHz)<br>**All others:** Reserved |
| nWRE | Write-only | OP[4] | **$0_b$:** enable nWR programming ≤ 9<br>**$1_b$:** enable nWR programming > 9 (default) |
| WL Select | Write-only | OP[6] | **$0_b$:** Select WL Set A (default)<br>**$1_b$:** (Reserved) |
| WR Leveling | Write-only | OP[7] | **$0_b$:** Disable (default)<br>**$1_b$:** Enable |


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### 7.3.5 MR3_I/O Configuration 1 (MA[7:0] = 03H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| (RFU) | | | | DS | | | |

| | | | |
|---|---|---|---|
| DS | Write-only | OP[3:0] | **$0001_b$:** 34.3Ωtypical pull-down/pull-up<br>**$0010_b$:** 40Ω typical pull-down/pull-up (default))<br>**$0011_b$:** 48Ω typical pull-down/pull-up<br>**$0100_b$:** 60Ω typical pull-down/pull-up<br>**$0110_b$:** 80Ω typical pull-down/pull-up<br>**$1001_b$:** 34.3Ω typical pull-down, 40Ω typical pull-up<br>**$1010_b$:** 40Ω typical pull-down, 48Ω typical pull-up<br>**$1011_b$:** 34.3Ω typical pull-down, 48Ω typical pull-up<br>**All others:** Reserved |

### 7.3.6 MR4_Device Temperature (MA[7:0] = 04H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| TUF | (RFU) | | | | SDRAM Refresh Rate | | |

| | | | |
|---|---|---|---|
| SDRAM Refresh Rate, Refresh Multiplier (RM) | Read-only | OP[2:0] | **$000_b$:** SDRAM Low temperature operating limit exceeded<br>**001b:** RM = 4; tREFIM = 4 x tREFI, tREFIMpb = 4 x tREFIpb, tREFWM = 4 x tREFW<br>**$010_b$:** RM = 2; tREFIM = 2 x tREFI, tREFIMpb = 2 x tREFIpb, tREFWM = 2 x tREFW<br>**$011_b$:** RM = 1; tREFIM = tREFI, tREFIMpb = tREFIpb, tREFWM = tREFW (≤ 85°C)<br>**$100_b$:** RM = 0.5; tREFIM = 0.5 x tREFI, tREFIMpb = 0.5 x tREFIpb, tREFWM = 0.5 x tREFW, do not de-rate SDRAM AC timing<br>**$101_b$:** RM= 0.25; tREFIM = 0.25 x tREFI, tREFIMpb = 0.25 x tREFIpb, tREFWM = 0.25 x tREFW, do not de-rate SDRAM AC timing<br>**$110_b$:** RM = 0.25; tREFIM = 0.25 x tREFI, tREFIMpb = 0.25 x tREFIpb, tREFWM = 0.25 x tREFW, de-rate SDRAM AC timing<br>**$111_b$:** SDRAM High temperature operating limit exceeded |
| Temperature Update Flag (TUF) | Read-only | OP7 | **$0_b$:** OP[2:0] value has not changed since last read of MR4<br>**$1_b$:** OP[2:0] value has changed since last read of MR4 |

**Notes:**

1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up. OP[2:0] bits are undefined after power-up.
3. If OP2 equals '1', the device temperature is greater than 85°C.
4. OP7 is set to '1' if OP[2:0] has changed at any time since the last read of MR4.
5. SDRAM might not operate properly when OP[2:0] = 000b or 111b.
6. For specified operating temperature range and maximum operating temperature, refer to **"Operating Temperature Range"** table.
7. LPDDR3 devices shall be derated by adding 1.875 nS to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating value in **"LPDDR3 AC Timing"** table. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8. See **"Temperature Sensor"** section for information on the recommended frequency of reading MR4.

### 7.3.7 MR5_Basic Configuration 1 (MA[7:0] = 05H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| LPDDR3 Manufacturer ID | | | | | | | |

| | | | |
|---|---|---|---|
| LPDDR3 Manufacturer ID | Read-only | OP[7:0] | 0000 1000b: Winbond |


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### 7.3.8 MR6_Basic Configuration 2 (MA[7:0] = 06H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| Revision ID1 | | | | | | | |

| | | | |
|---|---|---|---|
| Revision ID1 | Read-only | OP[7:0] | TBD |

**Note:** MR6 is vendor specific.

### 7.3.9 MR7_Basic Configuration 3 (MA[7:0] = 07H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| Revision ID2 | | | | | | | |

| | | | |
|---|---|---|---|
| Revision ID2 | Read-only | OP[7:0] | TBD |

**Note:** MR7 is vendor specific.

### 7.3.10 MR8_Basic Configuration 4 (MA[7:0] = 08H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| I/O width | | Density | | | | Type | |

| | | | |
|---|---|---|---|
| Type | Read-only | OP[1:0] | **$11_b$:** LPDDR3 SDRAM<br>**All others:** Reserved |
| Density | Read-only | OP[5:2] | **$0100_b$:** 1Gb<br>**All others:** Reserved |
| I/O width | Read-only | OP[7:6] | **$00_b$:** x32<br>**$01_b$:** x16<br>**All others:** Reserved |

### 7.3.11 MR9_(Reserved) (MA[7:0] = 09H)

### 7.3.12 MR10_Calibration (MA[7:0] = 0AH)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| Calibration Code | | | | | | | |

| | | | |
|---|---|---|---|
| Calibration Code | Write-only | OP[7:0] | **0xFF:** Calibration command after initialization<br>**0xAB:** Long calibration<br>**0x56:** Short calibration<br>**0xC3:** ZQ Reset<br>**All others:** Reserved |

**Notes:**
1. Host processor shall not write MR10 with “Reserved” values.
2. LPDDR3 devices shall ignore calibration command when a “Reserved” value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSS through RZQ, either the ZQ calibration function (see section 7.4.13.2 **“Mode Register Write ZQ Calibration Command”**) or default calibration (through the ZQRESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5. The MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.


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### 7.3.13 MR11_ODT Control (MA[7:0] = 0BH)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| RFU | | | | | PD CTL | DQ ODT | |

| | | | |
|---|---|---|---|
| DQ ODT | Write-only | OP[1:0] | **$00_b$:** Disable (Default)<br>**$01_b$:** RZQ /4<br>**$10_b$:** RZQ /2<br>**$11_b$:** RZQ /1 |
| PD Control | Write-only | OP[2] | **$0_b$:** ODT disabled by DRAM during power down (default)<br>**$1_b$:** ODT enabled by DRAM during power down |

### 7.3.14 MR12:15_(Reserved) (MA[7:0] = 0CH-OFH)

### 7.3.15 MR16_PASR_Bank Mask (MA[7:0] = 10H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| Bank Mask | | | | | | | |

| | | | |
|---|---|---|---|
| Bank [7:0] Mask | Write-only | OP[7:0] | **$0_b$:** Refresh enable to the bank (= unmasked, default)<br>**$1_b$:** Refresh blocked (= masked) |

| OP | Bank Mask | 8-Bank SDRAM |
|---|---|---|
| 0 | XXXXXXX1 | Bank 0 |
| 1 | XXXXXX1X | Bank 1 |
| 2 | XXXXX1XX | Bank 2 |
| 3 | XXXX1XXX | Bank 3 |
| 4 | XXX1XXXX | Bank 4 |
| 5 | XX1XXXXX | Bank 5 |
| 6 | X1XXXXXX | Bank 6 |
| 7 | 1XXXXXXX | Bank 7 |

### 7.3.16 MR17_PASR_Segment Mask (MA[7:0] = 11H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| Segment Mask | | | | | | | |

| | | | |
|---|---|---|---|
| Segment [7:0] Mask | Write-only | OP[7:0] | **$0_b$:** Refresh enable to the bank (= unmasked, default)<br>**$1_b$:** Refresh blocked (= masked) |

| Segment | OP | Segment Mask | R[12:10] |
|---|---|---|---|
| 0 | 0 | XXXXXXX1 | 000b |
| 1 | 1 | XXXXXX1X | 001b |
| 2 | 2 | XXXXX1XX | 010b |
| 3 | 3 | XXXX1XXX | 011b |
| 4 | 4 | XXX1XXXX | 100b |
| 5 | 5 | XX1XXXXX | 101b |
| 6 | 6 | X1XXXXXX | 110b |
| 7 | 7 | 1XXXXXXX | 111b |

**Note:**

1. This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.


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### 7.3.17 MR18:31_(Reserved) (MA[7:0] = 12H-1FH)

### 7.3.18 MR32_DQ Calibration Pattern A (MA[7:0] = 20H)

Reads to MR32 return DQ Calibration Pattern "A". See section 7.4.12.2 **"DQ Calibration"**.

### 7.3.19 MR33:39_( Do Not Use) (MA[7:0] = 21H-27H)

### 7.3.20 MR40_DQ Calibration Pattern B (MA[7:0] = 28H)

Reads to MR40 return DQ Calibration Pattern "B". See section 7.4.12.2 **"DQ Calibration"**.

### 7.3.21 MR41_ CA Training_1 (MA[7:0] = 29H)

Writes to MR41 enables CA Training. See section 7.4.13.3 **"Mode Register Write – CA Training Mode"**.

### 7.3.22 MR42_ CA Training_2 (MA[7:0] = 2AH)

Writes to MR42 exits CA Training. See section 7.4.13.3 **"Mode Register Write – CA Training Mode"**.

### 7.3.23 MR43:47_( Do Not Use) (MA[7:0] = 2BH-2FH)

### 7.3.24 MR48_ CA Training_3 (MA[7:0] = 30H)

Writes to MR48 enables CA Training. See section 7.4.13.3 **"Mode Register Write – CA Training Mode"**.

### 7.3.25 MR49:62_(Reserved) (MA[7:0] = 31H-3EH)

### 7.3.26 MR63_Reset (MA[7:0] = 3FH)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| X or 0xFC | | | | | | | |

**Note:**

1. For additional information on MRW RESET see section 7.4.13.1 **"Mode Register Write"**.

### 7.3.27 MR64:255_(Reserved) (MA[7:0] = 40H-FFH)


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## 7.4 Command Definitions and Timing Diagrams

### 7.4.1 Activate Command

The Activate command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 to BA2 are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The device can accept a Read or Write command at tRCD after the Activate command is issued. After a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between Activate commands to different banks is tRRD.

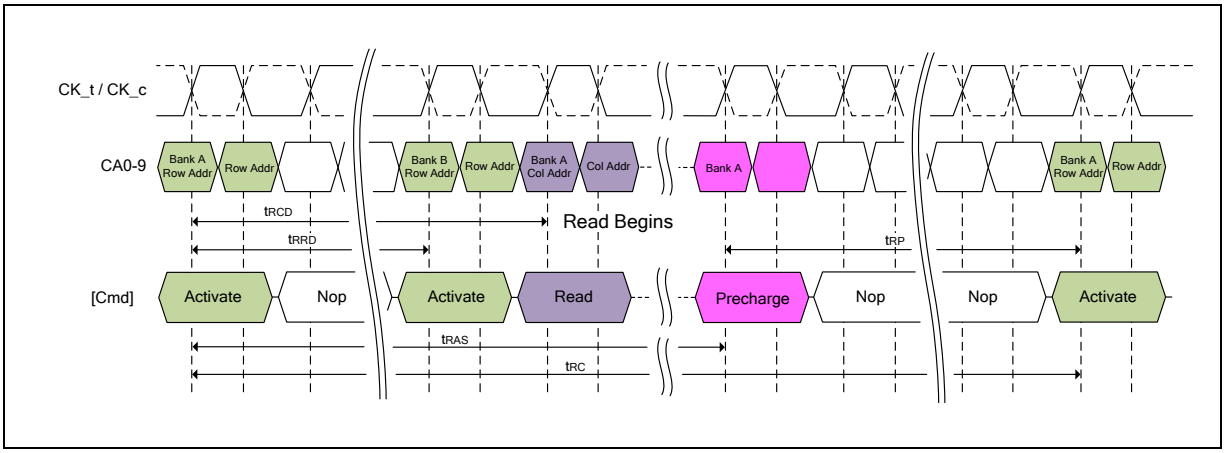



**Figure 3 - Activate Command**

**Note:**

1. A PRECHARGE-all command uses tRPab timing, while a single-bank PRECHARGE command uses tRPpb timing. In this figure, tRP is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

#### 7.4.1.1 8-Bank Device Operation

Certain restrictions on operation of the 8-bank LPDDR3 devices must be observed. There are two rules. One rule restricts the number of sequential Activate commands that can be issued; the other provides more time for RAS precharge for a Precharge All command. The rules are as follows:

**The 8-bank device Sequential Bank Activation Restriction**: No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting to clocks is done by dividing tFAW[nS] by tCK[nS], and rounding up to next integer value. As an example of the rolling window, if RU(tFAW/tCK) } is 10 clocks, and an Activate command is issued in clock N, no more than three further Activate commands can be issued at or between clock N+1 and N+9. REFpb also counts as bank activation for the purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceeds the tFAW time.

**The 8-bank device Precharge All Allowance**: tRP for a Precharge All command must equal tRPab, which is greater than tRPpb.

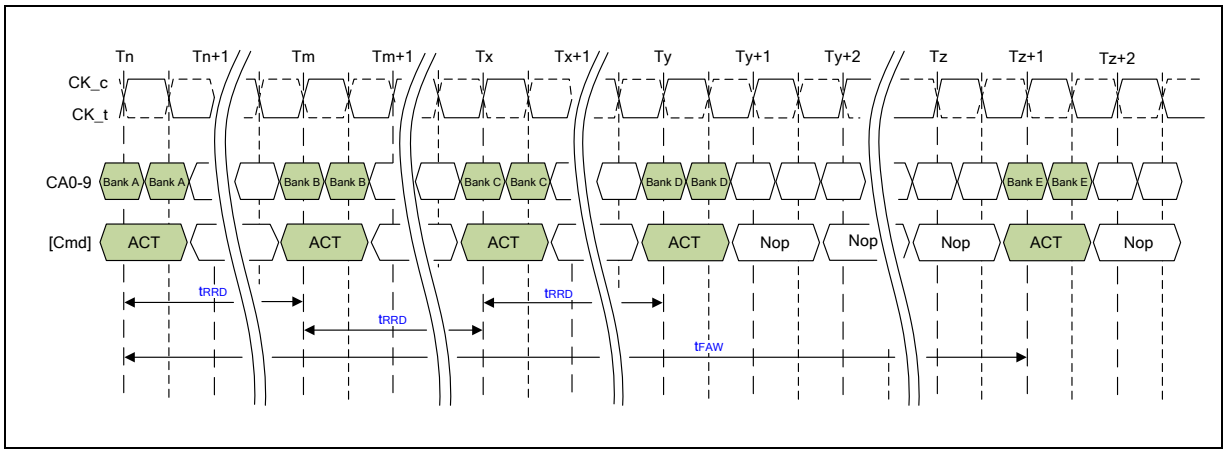



**Figure 4 - tFAW Timing**

### 7.4.2 Command Input Signal Timing Definition

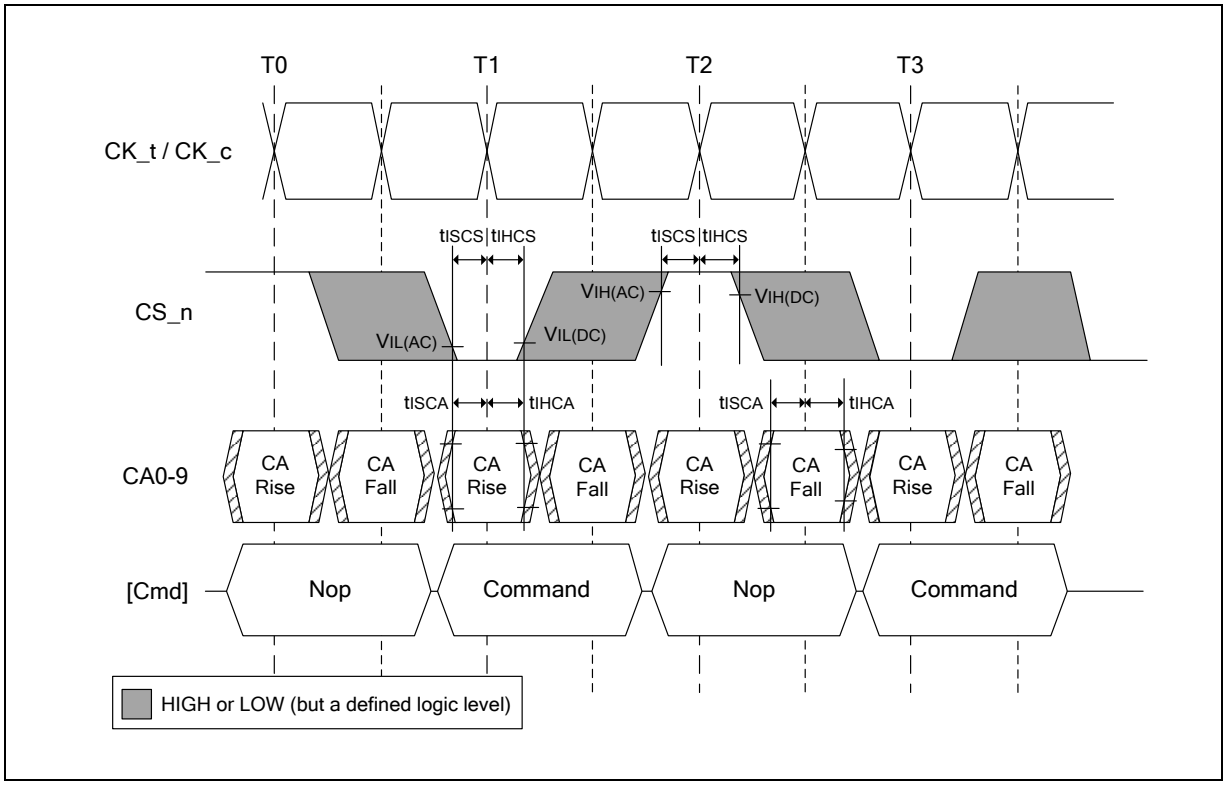



**Figure 5 - Command Input Setup and Hold Timing**

**Note:**

1. Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.


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#### 7.4.2.1 CKE Input Setup and Hold Timing

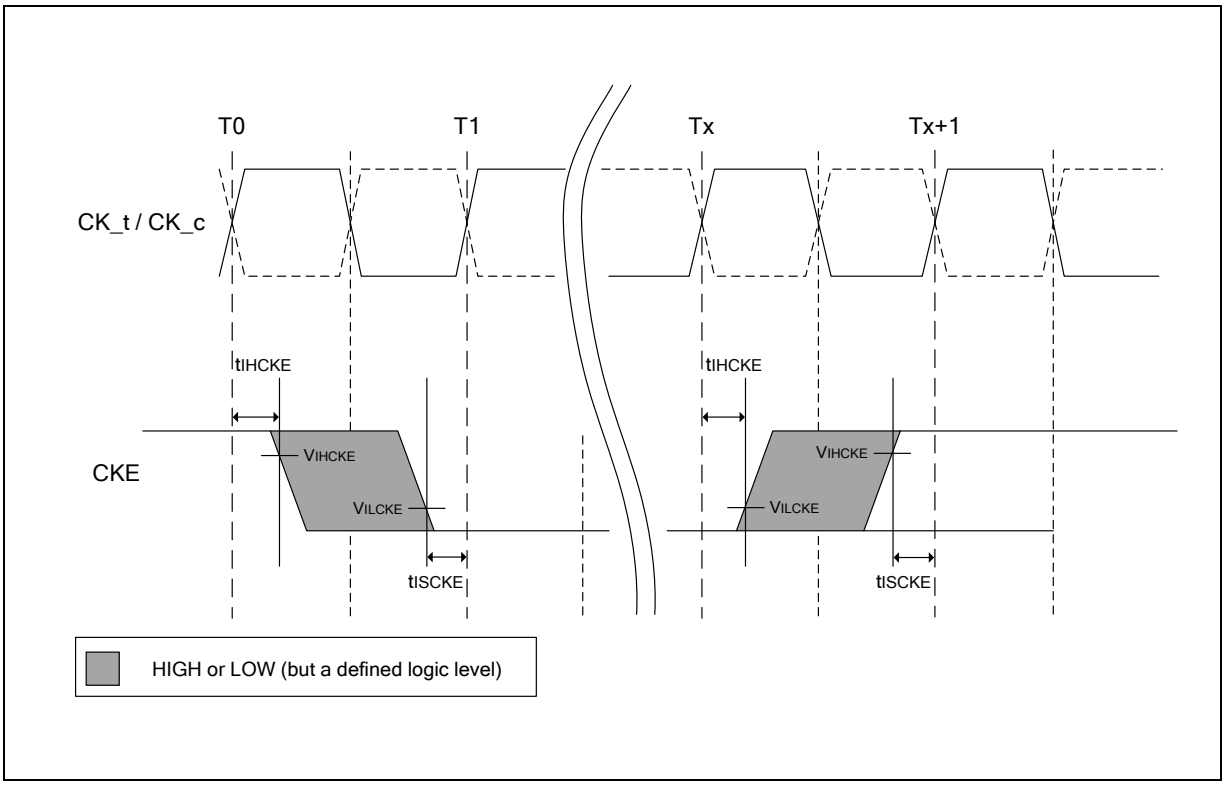



**Figure 6 - CKE Input Setup and Hold Timing**

**Note:**

1. After CKE is registered LOW, CKE signal level shall be maintained below $V_{ILCKE}$ for $t_{CKE}$ specification (LOW pulse width).
2. After CKE is registered HIGH, CKE signal level shall be maintained above $V_{IHCKE}$ for $t_{CKE}$ specification (HIGH pulse width).

### 7.4.3 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR3 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles. Burst interrupts are not allowed.

### 7.4.4 Burst Read Operation

The Burst Read command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs CA5r-CA6r and CA1f-CA9f determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the $t_{DQSCK}$ delay is measured. The first valid data is available RL x $t_{CK}$ + $t_{DQSCK}$ + $t_{DQSQ}$ after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW $t_{RPRE}$ before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.


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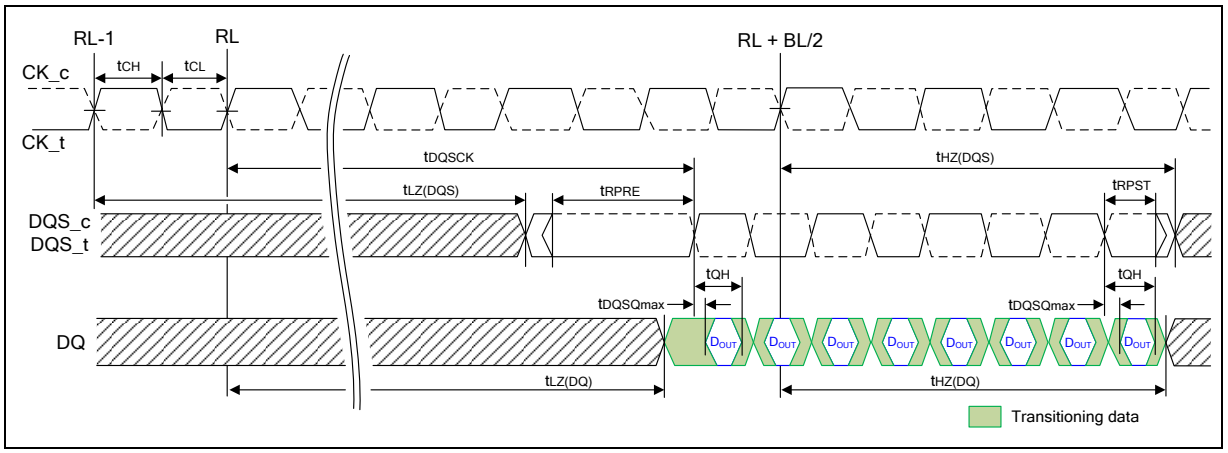



**Figure 7 - Read Output Timing**

**Notes:**

1. tDQSCK can span multiple clock periods.
2. An effective burst length of 8 is shown.

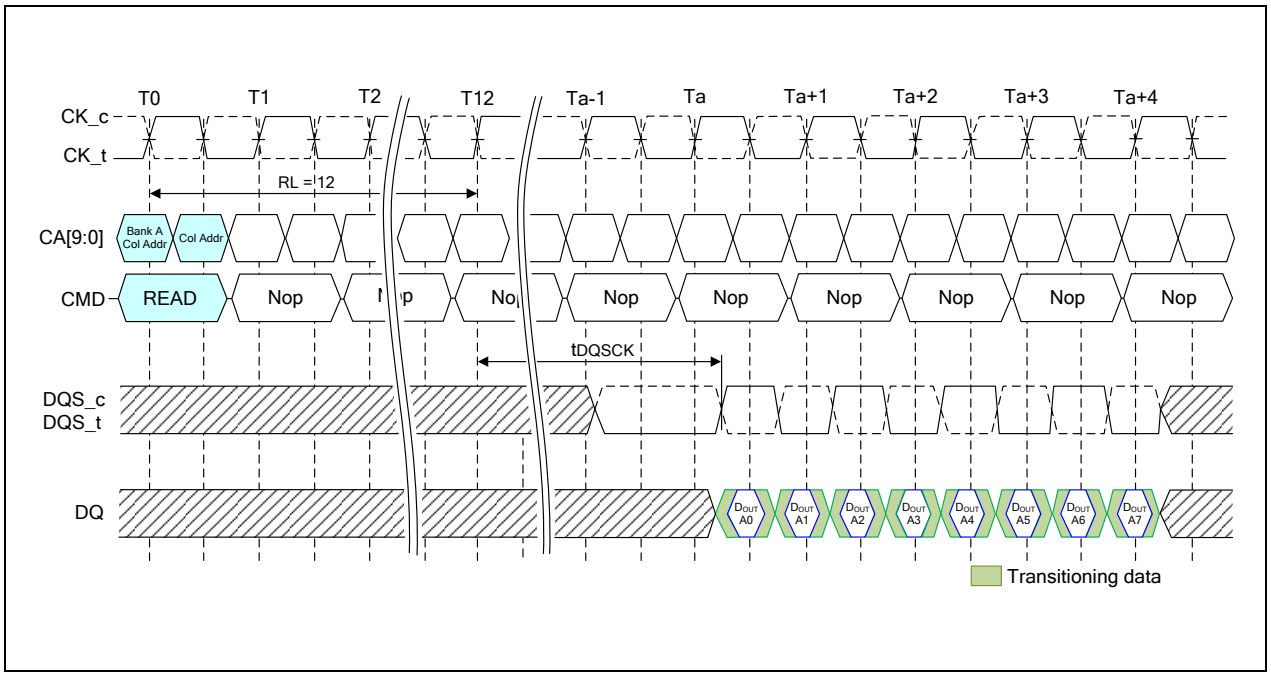



**Figure 8 - Burst Read: RL = 12, BL = 8, tDQSCK > tCK**


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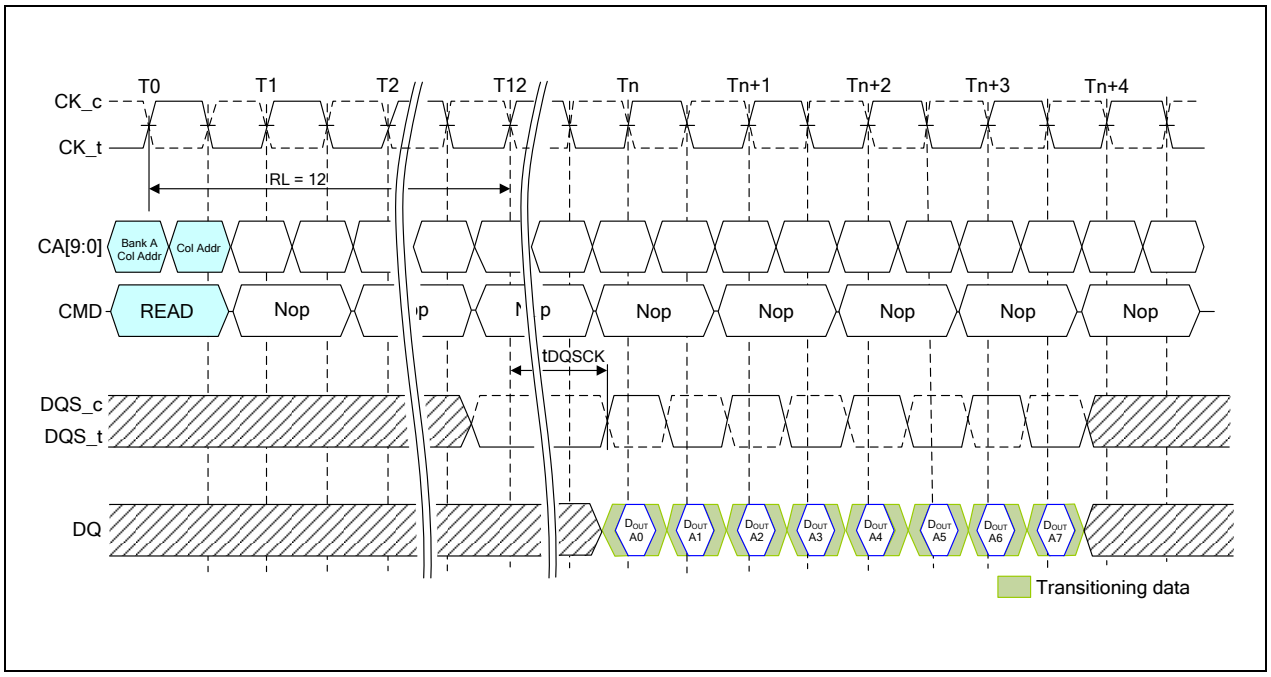



**Figure 9 - Burst Read: RL = 12, BL = 8, tDQSCK < tCK**

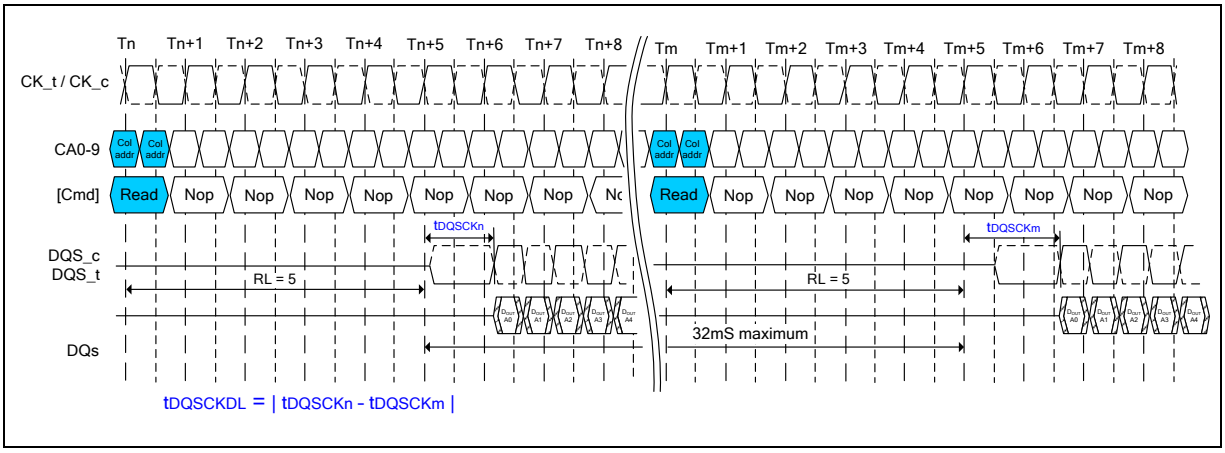



**Figure 10 - tDQSCKDL timing**

**Note:**

1. tDQSCKDLmax is defined as the maximum of ABS(tDQSCKn – tDQSCKm) for any {tDQSCKn , tDQSCKm} Pair within any 32mS rolling window.

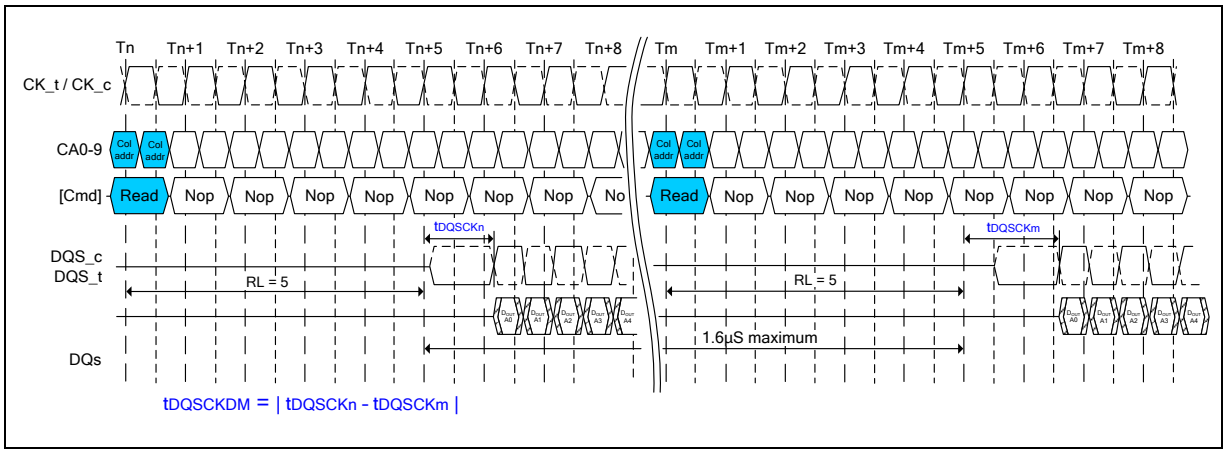



**Figure 11 - tDQSCKDM timing**

**Note:**

1. tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn,tDQSCKm} pair within any 1.6µS rolling window.

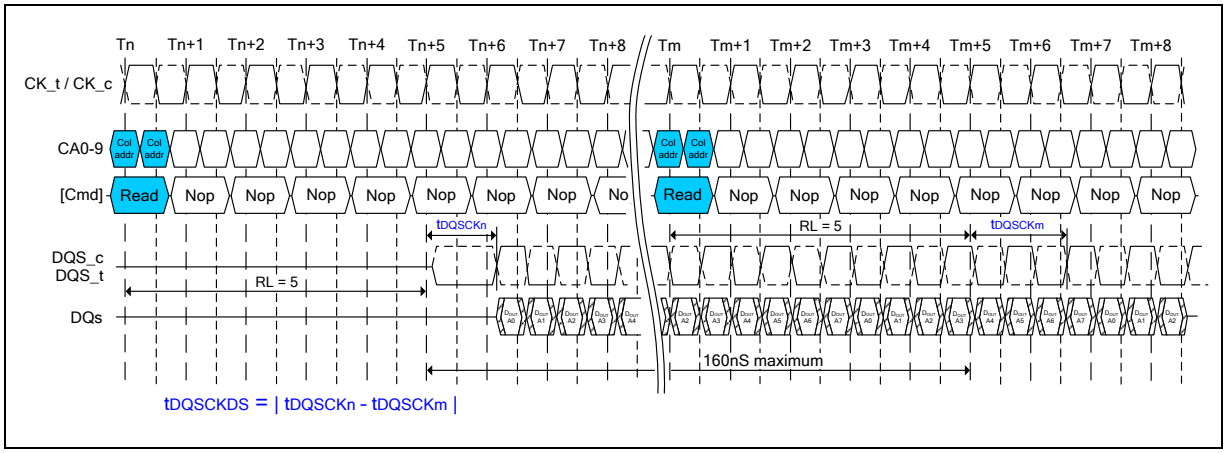



**Figure 12 - tDQSCKDS timing**

**Note:**

1. tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn ,tDQSCKm} pair for reads within a consecutive burst within any 160nS rolling window.

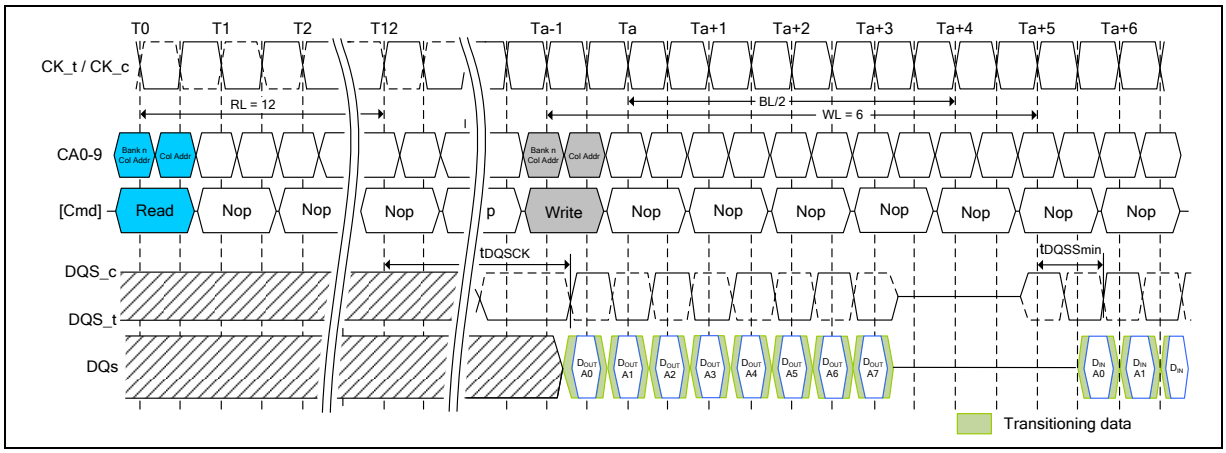



**Figure 13 - Burst Read Followed By Burst Write**

The minimum time from the burst Read command to the burst Write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum Read-to-Write latency is RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 - WL clock cycles.

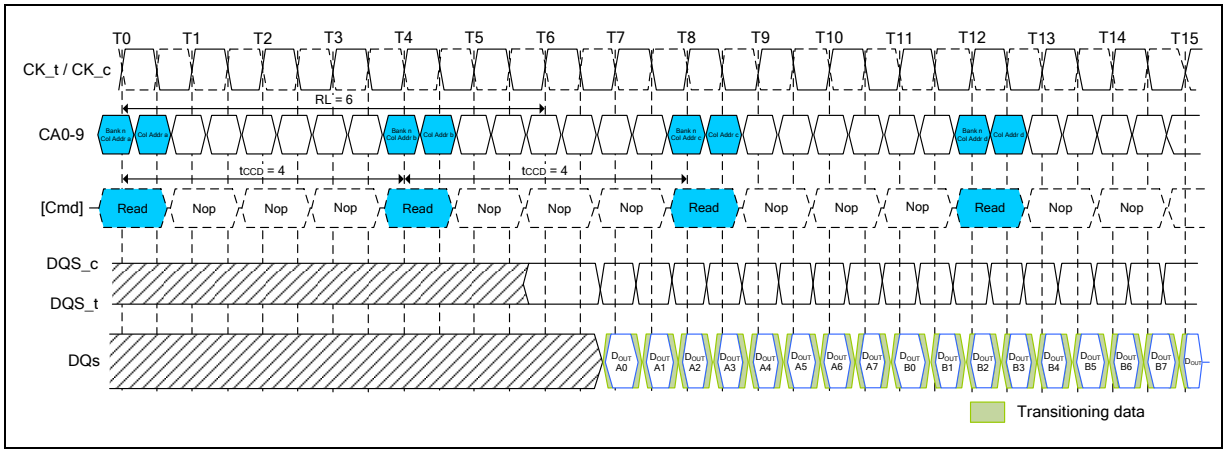



**Figure 14 - Seamless Burst Read**

The seamless burst Read operation is supported by enabling a Read command at every fourth clock cycle for BL = 8 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

### 7.4.5 Burst Write Operation

The Burst Write command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid data must be driven WL x tCK + tDQSS from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) must be driven for time tWPRE prior as shown in Figure 17 prior to data input. The burst cycle data bits must be applied to the DQ pins tDS prior to the associated edge of the DQS until the 8-bit burst length is completed. After a burst Write operation, tWR must be satisfied before a Precharge command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

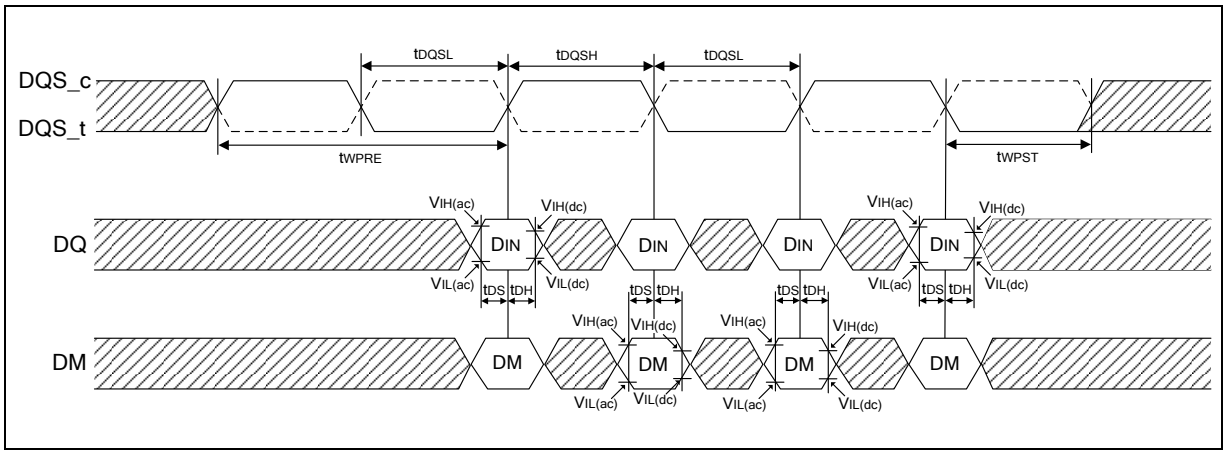



**Figure 15 - Data input (write) timing**

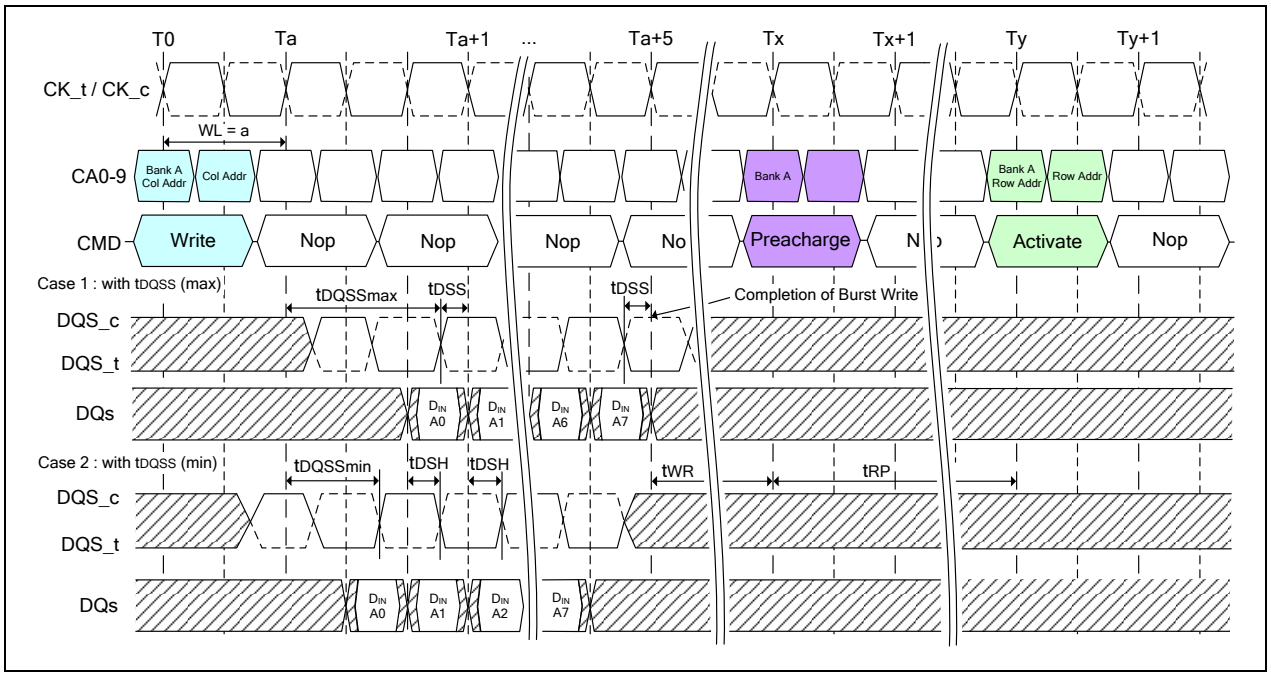



**Figure 16 - Burst Write**

### 7.4.5.1 $t_{WPRE}$ Calculation

The method for calculating $t_{WPRE}$ is shown in the figure below.

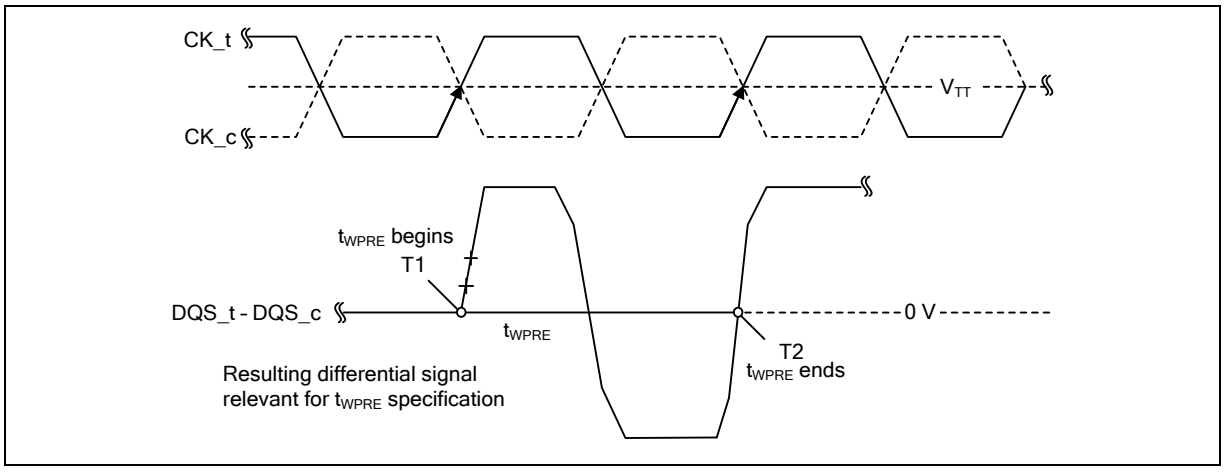



**Figure 17 - Method for calculating $t_{WPRE}$ Transitions and Endpoints**

### 7.4.5.2 $t_{WPST}$ Calculation

The method for calculating $t_{WPST}$ is shown in the figure below.

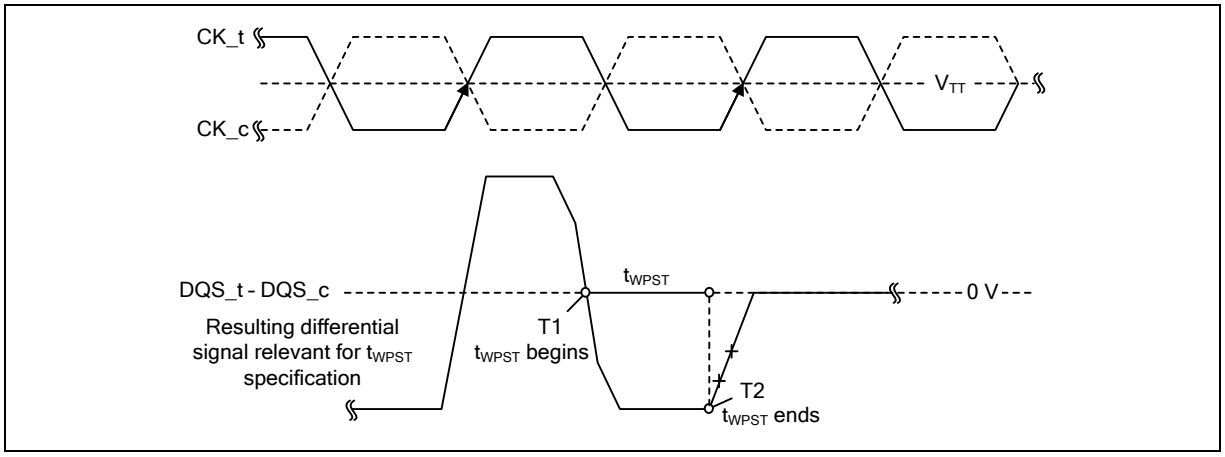



**Figure 18 - Method for calculating $t_{WPST}$ Transitions and Endpoints**

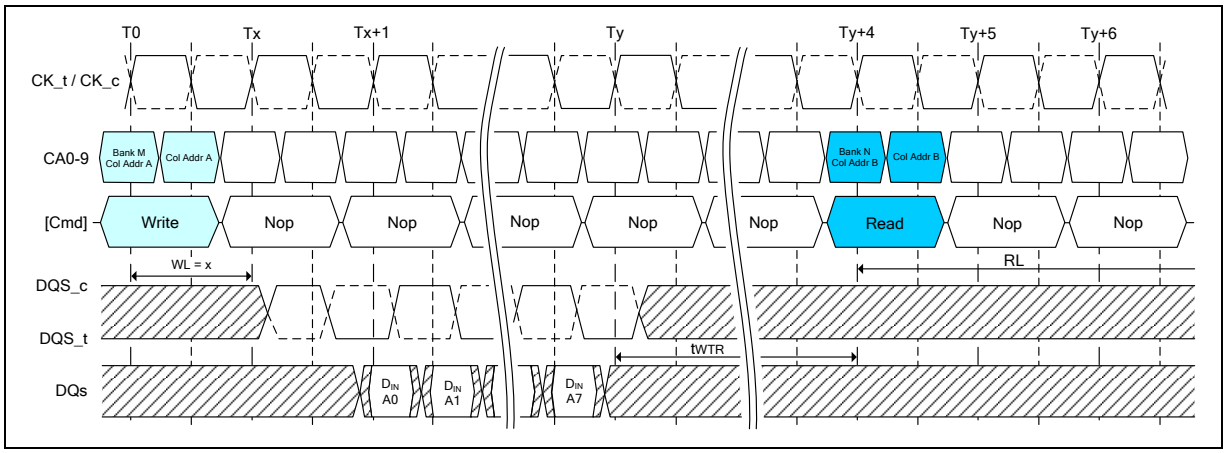



**Figure 19 - Burst Write Followed By Burst Read**

**Notes:**

1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU( tWTR/tCK)].
2. tWTR starts at the rising edge of the clock after the last valid input data.

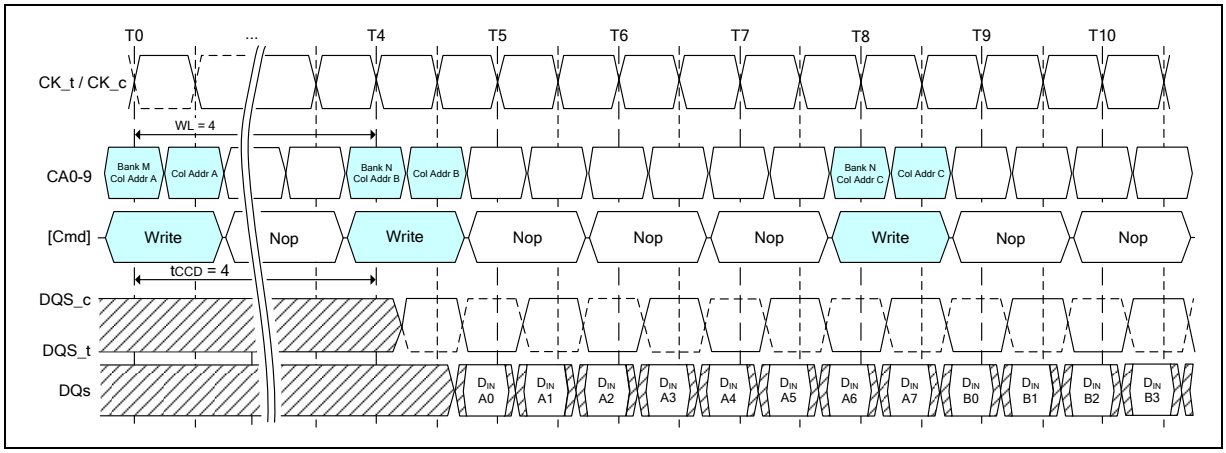



**Figure 20 - Seamless burst write: WL = 4, tCCD = 4**

**Note:**

1. The seamless burst write operation is supported by enabling a write command every four clocks for BL = 8 operation. This operation is allowed for any activated bank.

### 7.4.6 Write Data Mask

On LPDDR3 devices, one write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on LPDDR2 SDRAM. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data-mask loaded is identically to data-bit to ensure matched system timing.

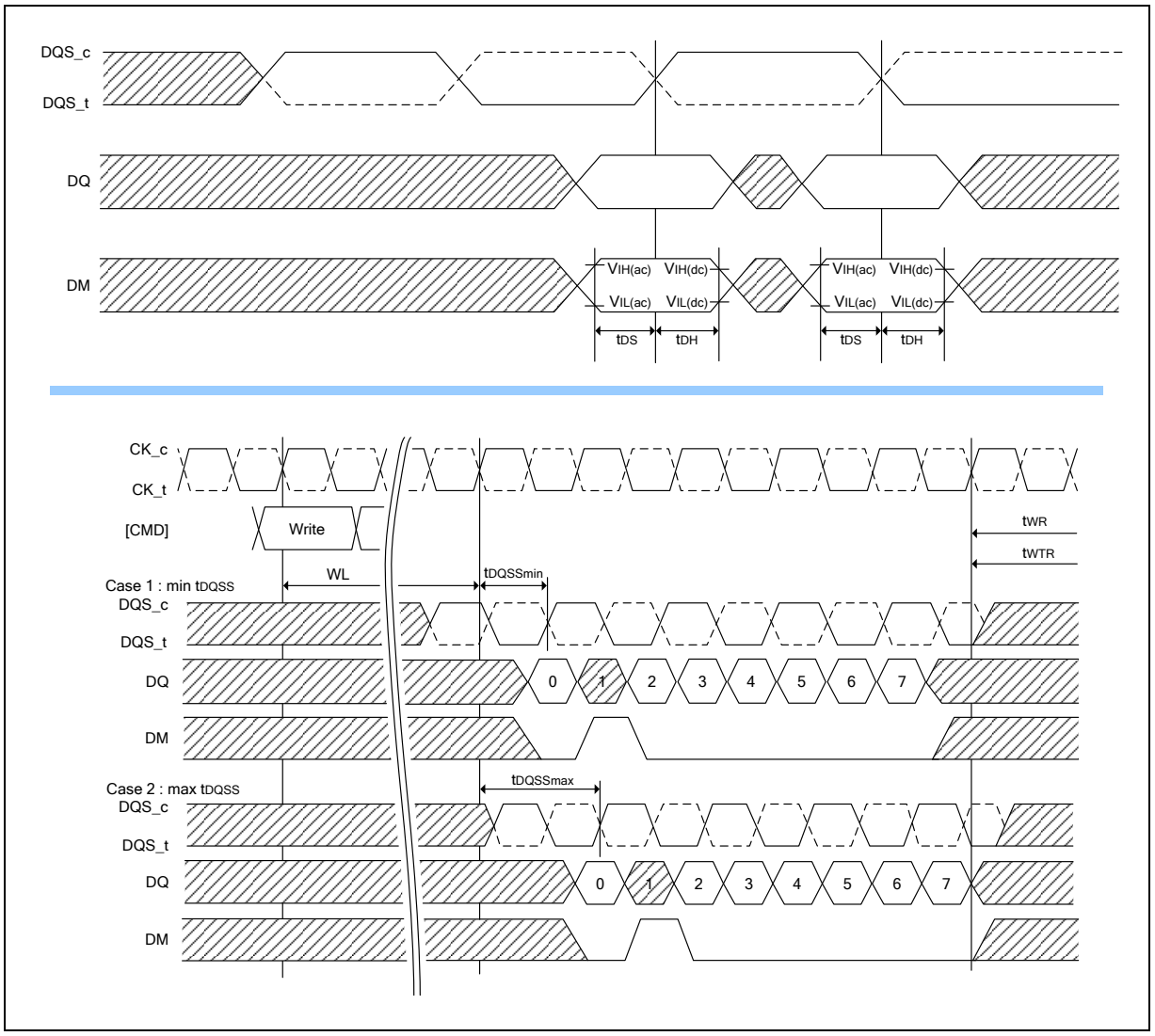



**Figure 21 - Data Mask Timing**

**Note:**

1. For the data mask function, BL = 8 is shown; the second data bit is masked.


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### 7.4.7 Precharge Operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated with CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bits, BA0, BA1, and BA2 are used to determine which bank(s) to precharge. The precharge bank(s) will be available for subsequent row access tRPab after an all-bank Precharge command is issued, or tRPpb after a single-bank Precharge command is issued.

To ensure that LPDDR3 devices can meet the instantaneous current demand required to operate, the row-precharge time for an all-bank Precharge (tRPab) will be longer than the row Precharge time for a single-bank Precharge (tRPpb). Activate to Precharge timing is shown in Figure 3.

**Bank selection for Precharge by address bits**

| AB (CA4r) | BA2 (CA9r) | BA1 (CA8r) | BA0 (CA7r) | Precharged Bank(s) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Bank 0 only |
| 0 | 0 | 0 | 1 | Bank 1 only |
| 0 | 0 | 1 | 0 | Bank 2 only |
| 0 | 0 | 1 | 1 | Bank 3 only |
| 0 | 1 | 0 | 0 | Bank 4 only |
| 0 | 1 | 0 | 1 | Bank 5 only |
| 0 | 1 | 1 | 0 | Bank 6 only |
| 0 | 1 | 1 | 1 | Bank 7 only |
| 1 | DON'T CARE | DON'T CARE | DON'T CARE | All Banks |

#### 7.4.7.1 Burst Read Operation Followed by Precharge

For the earliest possible precharge, the Precharge command can be issued BL/2 clock cycles after a Read command. A new bank Active command can be issued to the same bank after the row Precharge time (tRP) has elapsed. A Precharge command cannot be issued until after tRAS is satisfied. The minimum Read-to-Precharge time must also satisfy a minimum analog time from the rising clock edge that initiates the last 8-bit prefetch of a Read command. tRTP begins BL/2 - 4 clock cycles after the Read command. For LPDDR3 Read-to-Precharge timings see section 7.4.8.3 **"Precharge & Auto Precharge Clarification"** table.

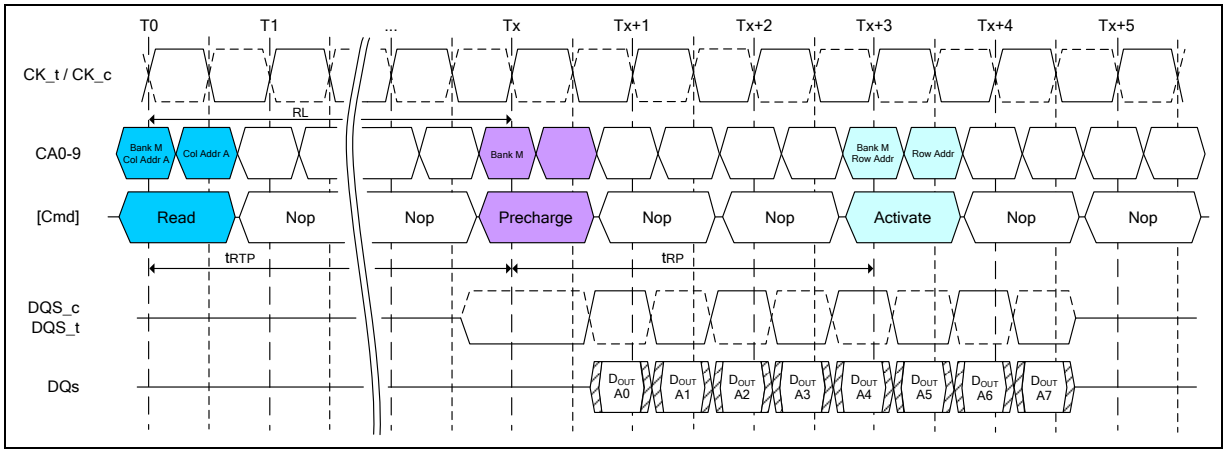



**Figure 22 - Burst Read Followed by Precharge**

### 7.4.7.2 Burst Write Followed by Precharge

For write cycles, a Write Recovery time (tWR) must be provided before a Precharge command can be issued. This delay is referenced from the last valid burst input data to the completion of the burst Write. A Precharge command must not be issued prior to the tWR delay. For LPDDR3 Write-to-Precharge timings see section 7.4.8.3 **"Precharge & Auto Precharge Clarification"** table.

LPDDR3 devices write data to the array in prefetch multiples (prefetch = 8). An internal write operation can only begin after a prefetch group has been completely latched, so tWR starts at prefetch boundaries. The minimum Write-to-Precharge time for command to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles.

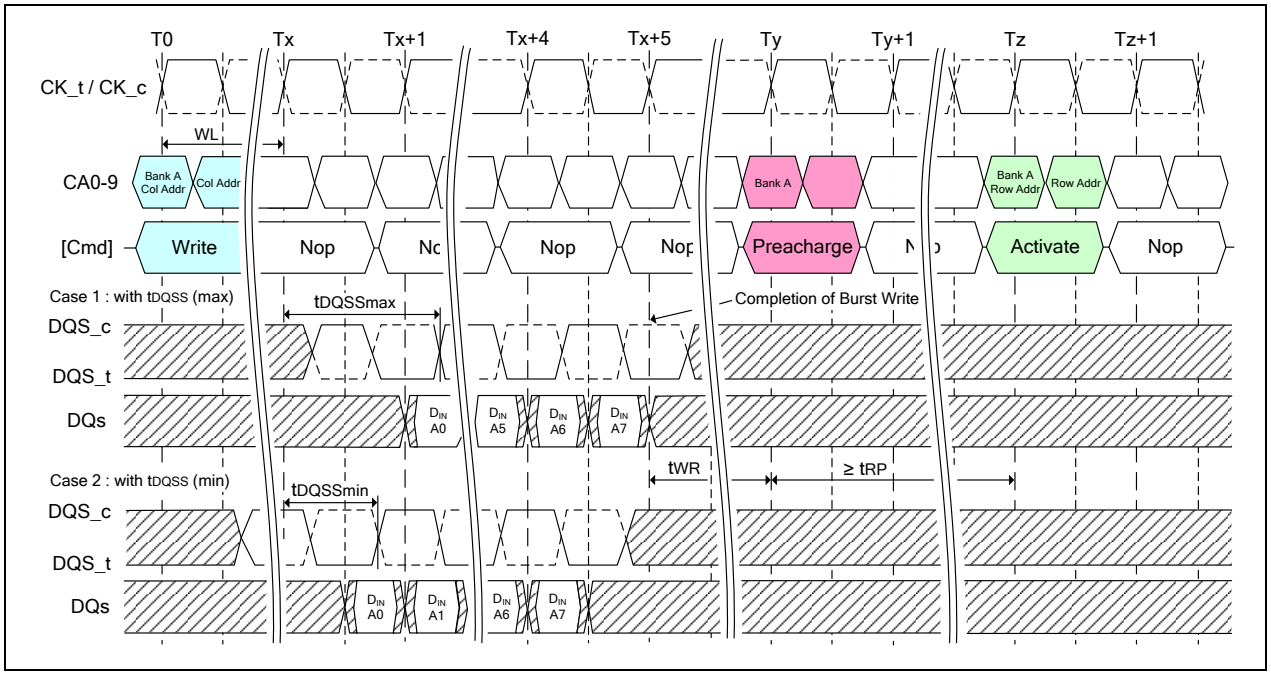



**Figure 23 - Burst Write Followed by Precharge**

### 7.4.8 Auto Precharge Operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is issued to the device, the AP bit (CA0f) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature enables the Precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

### 7.4.8.1 Burst Read with Auto-Precharge

If AP (CA0f) is HIGH when a Read command is issued, the Read with auto-precharge function is engaged. LPDDR3 devices start an auto-precharge operation on the rising edge of the clock BL/2 or BL/2 - 4 + RU(tRTP/tCK) clock cycles later than the Read with auto-precharge command, whichever is greater. For LPDDR3 auto-precharge calculations see section 7.4.8.3 **"Precharge & Auto Precharge Clarification"** table. Following an auto-precharge operation, an Activate command can be issued to the same bank if the following two conditions are satisfied simultaneously:

a) The RAS precharge time (tRP) has been satisfied from the clock at which the auto-precharge begins.

b) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

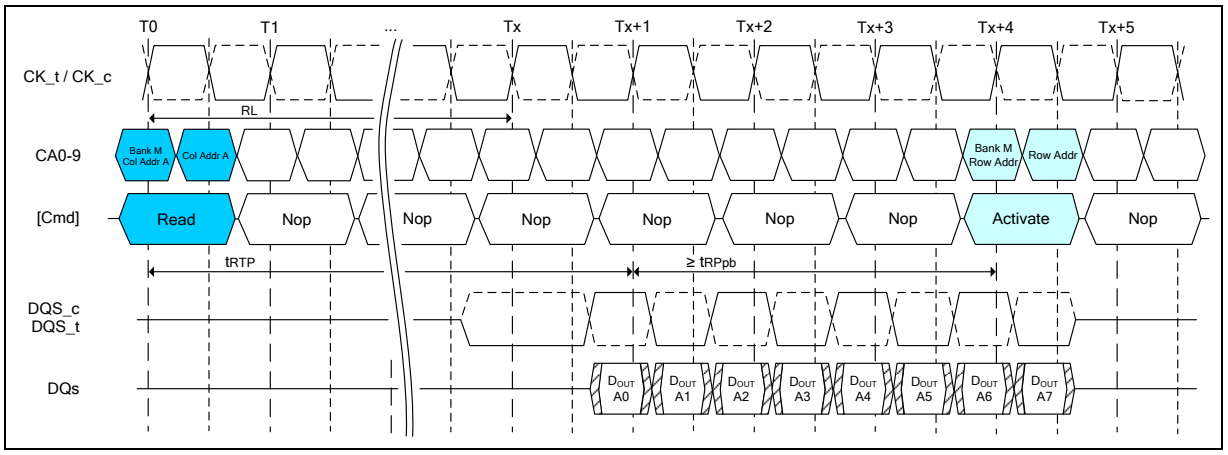



**Figure 24 - Burst Read with Auto Precharge**

### 7.4.8.2 Burst Write with Auto-Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with auto-precharge function is engaged. The device starts an auto-precharge on the rising edge tWR cycles after the completion of the burst write.

Following a Write with auto-precharge, an Activate command can be issued to the same bank if the following two conditions are met:

The RAS precharge time (tRP) has been satisfied from the clock at which the auto-precharge begins.

The RAS cycle time (tRC) from the previous bank activation has been satisfied.

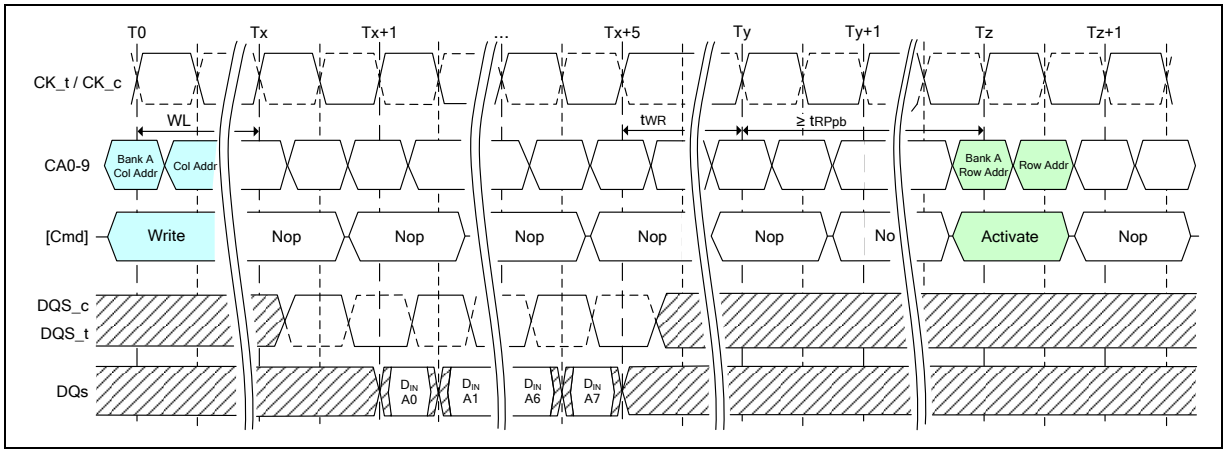



**Figure 25 - Burst Write with Auto Precharge**

### 7.4.8.3 Precharge & Auto Precharge Clarification

| From Command | To Command | Minimum Delay between "From Command" to "To Command" | Unit | Notes |
|---|---|---|---|---|
| Read | Precharge (to same Bank as Read) | BL/2 + max(4, RU(tRTP/tCK)) - 4 | CLK | 1 |
| | Precharge All | BL/2 + max(4, RU(tRTP/tCK)) - 4 | CLK | 1 |
| Read w/AP | Precharge (to same Bank as Read w/AP) | BL/2 + max(4, RU(tRTP/tCK)) - 4 | CLK | 1, 2 |
| | Precharge All | BL/2 + max(4, RU(tRTP/tCK)) - 4 | CLK | 1 |
| | Activate (to same Bank as Read w/AP) | BL/2 + max(4, RU(tRTP/tCK)) - 4 + RU(tRPpb/tCK) | CLK | 1 |
| | Write or Write w/AP (same bank) | Illegal | CLK | 3 |
| | Write or Write w/AP (different bank) | RL + BL/2 + RU(tDQSCKmax/tCK) - WL + 1 | CLK | 3 |
| | Read or Read w/AP (same bank) | Illegal | CLK | 3 |
| | Read or Read w/AP (different bank) | BL/2 | CLK | 3 |
| Write | Precharge (to same Bank as Write) | WL + BL/2 + RU(tWR/tCK) + 1 | CLK | 1 |
| | Precharge All | WL + BL/2 + RU(tWR/tCK) + 1 | CLK | 1 |
| Write w/AP | Precharge (to same Bank as Write w/AP) | WL + BL/2+ RU(tWR/tCK) + 1 | CLK | 1 |
| | Precharge All | WL + BL/2 + RU(tWR/tCK) + 1 | CLK | 1 |
| | Activate (to same Bank as Write w/AP) | WL + BL/2 + RU(tWR/tCK) + 1 + RU(tRPpb/tCK) | CLK | 1 |
| | Write or Write w/AP (same bank) | Illegal | CLK | 3 |
| | Write or Write w/AP (different bank) | BL/2 | CLK | 3 |
| | Read or Read w/AP (same bank) | Illegal | CLK | 3 |
| | Read or Read w/AP (different bank) | WL + BL/2 + RU(tWTR/tCK) + 1 | CLK | 3 |
| Precharge | Precharge (to same Bank as Precharge) | 1 | CLK | 1 |
| | Precharge All | 1 | CLK | 1 |
| Precharge All | Precharge | 1 | CLK | 1 |
| | Precharge All | 1 | CLK | 1 |

**Notes:**

1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.
2. Any command issued during the minimum delay time as specified in this table is illegal.
3. After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read and Write operations may not be interrupted or truncated.


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### 7.4.9 Refresh command

The Refresh command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. Per-bank Refresh is initiated with CA3 LOW at the rising edge of clock. All-bank Refresh is initiated with CA3 HIGH at the rising edge of clock.

A Per-bank Refresh command (REFpb) performs a per-bank refresh operation to the bank scheduled by the bank counter in the memory device. The bank sequence of per-bank Refresh is fixed to be a sequential round-robin: "0-1-2-3-4-5-6-7-0-1-...". The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET signal or at every exit from self refresh. Bank addressing for the per-bank Refresh count is the same as established for the single-bank Precharge command. A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank Refresh command.

The REFpb command must not be issued to the device until the following conditions are met (see 7.4.9.1 "**Refresh Command Scheduling Separation Requirements**" table):

- tRFCab has been satisfied after the prior REFab command
- tRFCpb has been satisfied after the prior REFpb command
- tRP has been satisfied after prior Precharge commands to that bank
- tRRD has been satisfied after the prior Activate command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command),

The target bank is inaccessible during per-bank Refresh cycle time (tRFCpb), however other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a Read or a Write command. When the per-bank Refresh cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, these conditions must be met (see 7.4.9.1 "**Refresh Command Scheduling Separation Requirements**" table):

- tRFCpb must be satisfied before issuing a REFab command
- tRFCpb must be satisfied before issuing an Activate command to the same bank
- tRRD must be satisfied before issuing an Activate command to a different bank
- tRFCpb must be satisfied before issuing another REFpb command

An all-bank Refresh command (REFab) issues a Refresh command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a Precharge-all command prior to issuing an all-bank Refresh command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met (see 7.4.9.1 "**Refresh Command Scheduling Separation Requirements**" table):

- tRFCab has been satisfied following the prior REFab command
- tRFCpb has been satisfied following the prior REFpb command
- tRP has been satisfied following the prior Precharge commands

When the all-bank Refresh cycle has completed, all banks will be idle. After issuing REFab:

- tRFCab latency must be satisfied before issuing an Activate command
- tRFCab latency must be satisfied before issuing a REFab or REFpb command


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#### 7.4.9.1 Refresh Command Scheduling Separation Requirements

| Symbol | Minimum Delay From… | To… | Note |
|---|---|---|---|
| tRFCab | REFab | REFab | |
| | | Activate command to any bank | |
| | | REFpb | |
| tRFCpb | REFpb | REFab | |
| | | Activate command to same bank as REFpb | |
| | | REFpb | |
| tRRD | REFpb | Activate command to different bank than REFpb | |
| | Activate | REFpb | 1 |
| | | Activate command to different bank than prior Activate command | |

**Note:**

1. A bank must be in the idle state before it is refreshed, so following an Activate command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.

In general, an all-bank Refresh command needs to be issued to the LPDDR3 SDRAM regularly every tREFI (or more precisely tREFIM = tREFI x RM, see MR4 setting) interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI (9 x tREFIM = 9 x RM x tREFI). A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”) , with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8, depending on Refresh mode, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI (9 x tREFIM = 9 x RM x tREFI). At any given time, a maximum of 16 REF commands can be issued within 2 x tREFI (2 x tREFIM = 2 x RM x tREFI)

And for per-bank refresh, a maximum 8 x 8 per-bank Refresh commands can be postponed or pulled in for scheduling efficiency. At any given time, a maximum of 2 x 8 x 8 per-bank Refresh commands can be issued within 2 x tREFI (2 x RM x tREFI)

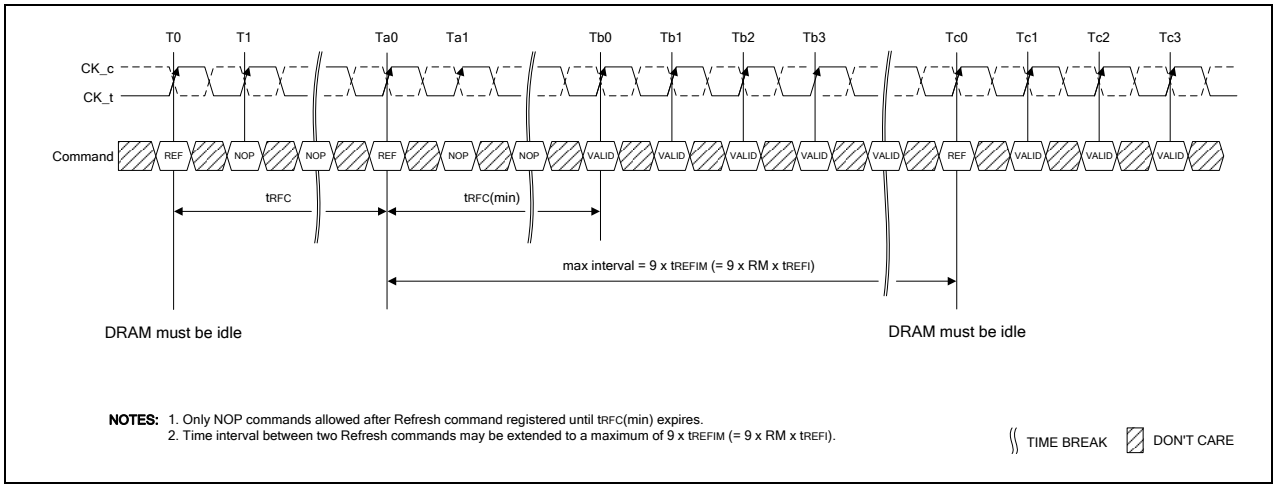



**Figure 26 – Refresh Command Timing**


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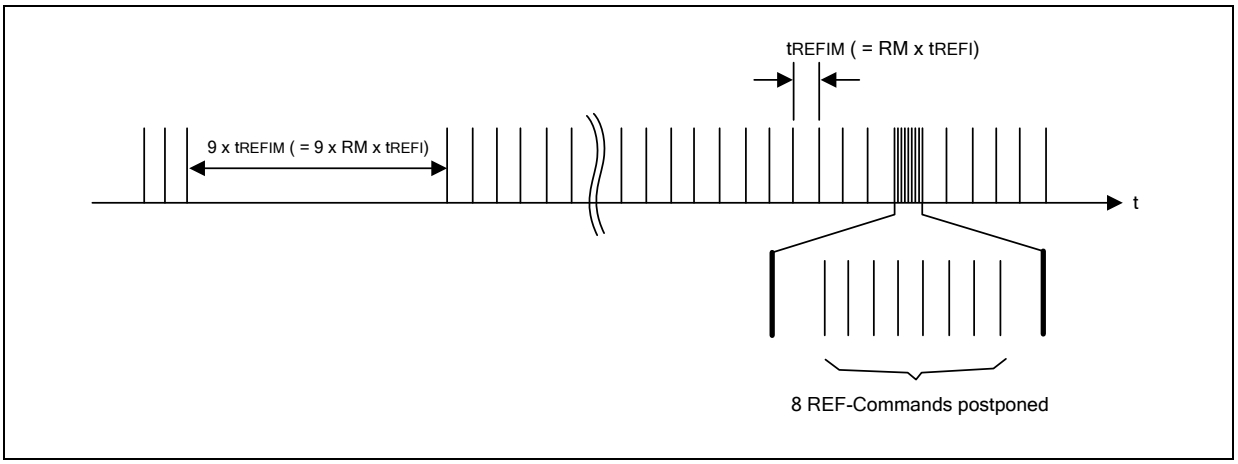



**Figure 27 – Postponing Refresh Commands**

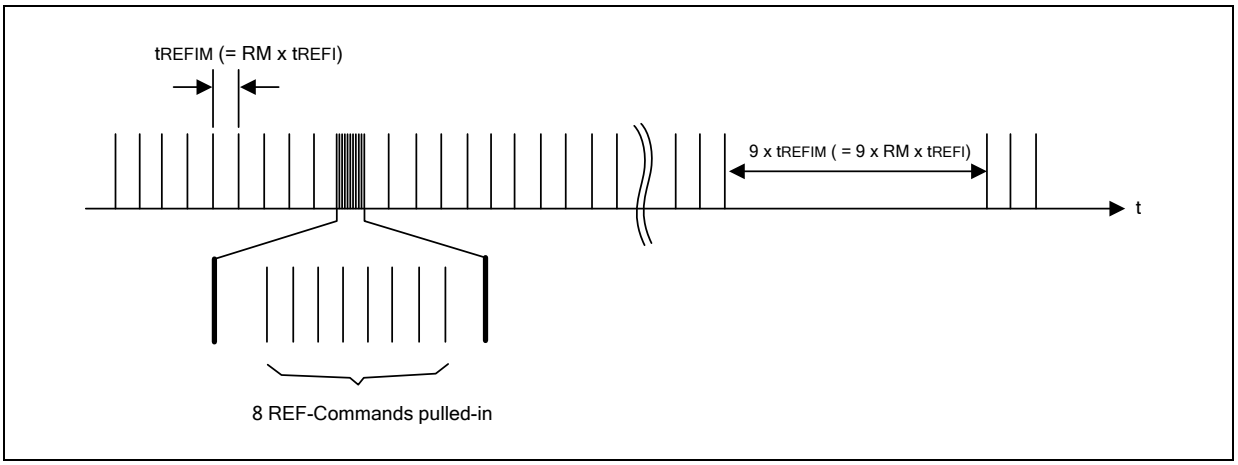



**Figure 28 – Pulling-in Refresh Commands**


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### 7.4.9.2 Refresh Requirements

(1) Minimum number of Refresh commands:

LPDDR3 requires a minimum number of R Refresh (REFab) commands within any rolling refresh window ($t_{REFW}$ = 32 mS @ MR4[2:0] = “011” or $T_{CASE}$ @ 85°C). Based on the setting in MR4 a refresh multiplier RM larger or smaller than 1 may apply. The refresh window then becomes $t_{REFWM}$ = RM x $t_{REFW}$ and the refresh interval becomes $t_{REFIM}$ = RM x $t_{REFI}$, refer to MR4 definition for details.

When using per-bank Refresh, a REFab command can be replaced by a full cycle of eight REFpb commands.

(2) Refresh Requirements and Self-Refresh:

Self refresh mode may be entered with a maximum of eight refresh commands being postponed. After exiting self-refresh mode with one or more refresh commands postponed, additional refresh commands may be postponed to the extent that the total number of postponed refresh commands (before and after the self refresh) will never exceed eight. During self-refresh mode, the number of postponed or pulled-in REF commands does not change.”

“The use of self refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self refresh mode. Upon exit from self refresh, the LPDDR3 SDRAM requires a minimum of one extra refresh command before it is put back into self refresh mode.”

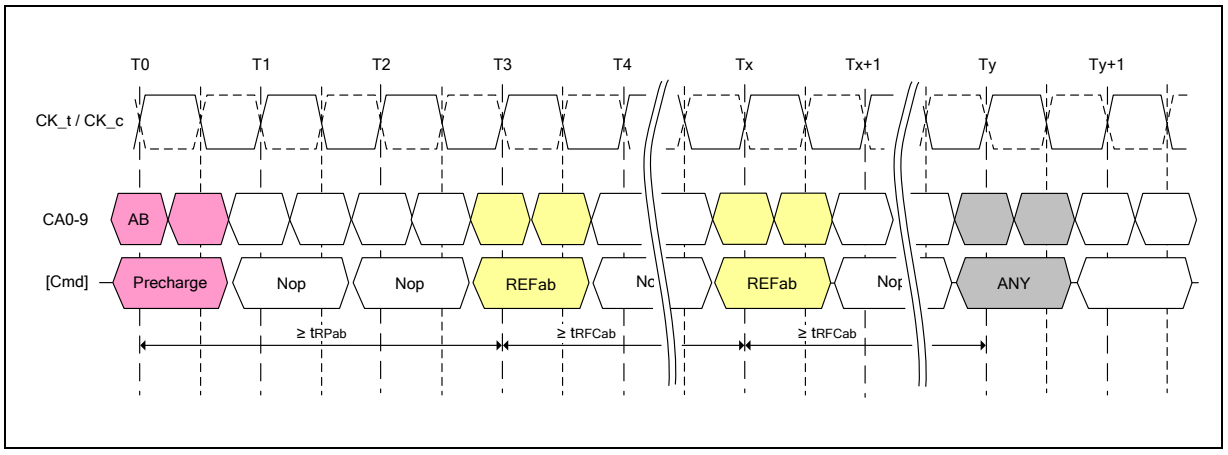



**Figure 29 - All-Bank Refresh Operation**

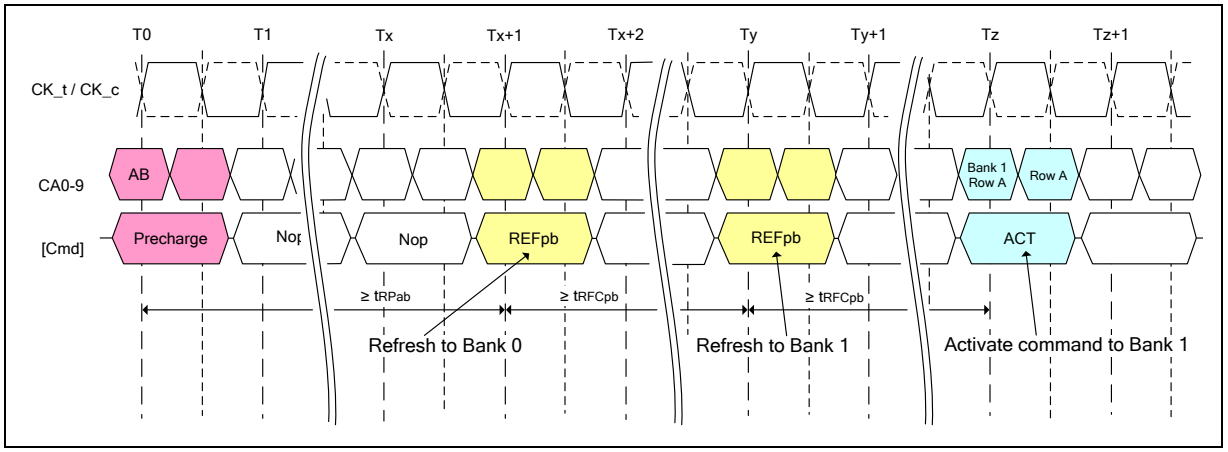



**Figure 30 - Per-Bank Refresh Operation**

**Notes:**

1. In the beginning of this example, the REFpb bank is pointing to bank 0.
2. Operations to banks other than the bank being refreshed are supported during the $t_{RFCpb}$ period.

### 7.4.10 Self Refresh Operation

The Self Refresh command can be used to retain data in the LPDDR3 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the SDRAM retains data without external clocking. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. CKE must not go LOW while MRR, MRW, Read, or Write operations are in progress. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP command are required after CKE is driven LOW, this timing period is defined as tCPDED. CKE LOW will result in deactivation of input receivers after tCPDED has expired. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR3 SDRAM devices can operate in Self Refresh in both the standard or extended temperature ranges. LPDDR3 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures.

Once the SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels. VDDQ may be turned off during Self Refresh. Prior to exiting Self Refresh, VDDQ must be within specified limits. VREFDQ and VREFCA may be at any level within minimum and maximum levels (see **Absolute Maximum DC Ratings**). However prior to exiting Self Refresh, VREFDQ and VREFCA must be within specified limits (see **Recommended DC Operating Conditions**). The SDRAM initiates a minimum of one all-bank Refresh command internally within tCKESR period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh operation to save power. The minimum time that the SDRAM must remain in Self Refresh mode is tCKESR,min. The user may change the external clock frequency or halt the external clock tCPDED after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 tCK prior to the positive clock edge that registers CKE HIGH. Once Self Refresh Exit is registered, a delay of at least tXSR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period tXSR for proper operation. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval tXSR. For the description of ODT operation and specifications during self-refresh entry and exit, see 7.4.14 **“On-Die Termination”** section.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.


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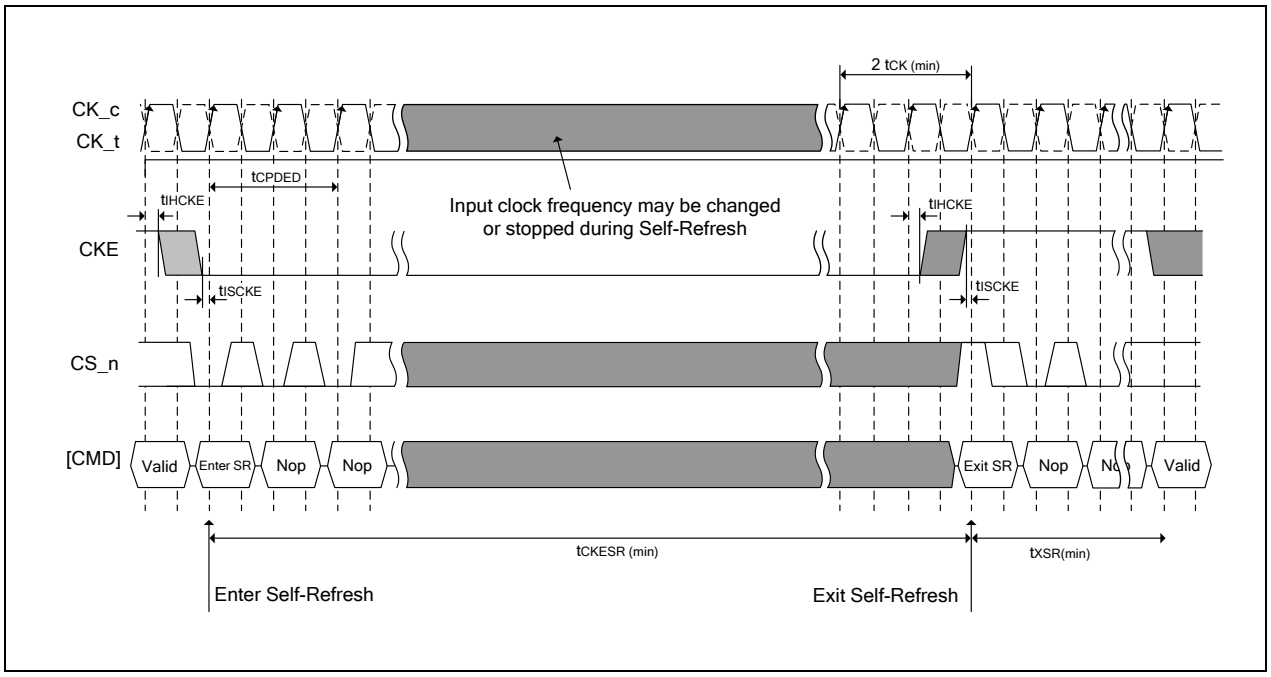



**Figure 31 - Self-Refresh Operation**

**Notes:**

1. Input clock frequency may be changed or can be stopped or floated during self-refresh, provided that upon exiting self-refresh, the clock is stable and within specified limits for a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the speed grade in use.
2. Device must be in the “All banks idle” state prior to entering Self Refresh mode.
3. $t_{XSR}$ begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after $t_{XSR}$ is satisfied. NOPs shall be issued during $t_{XSR}$.

### 7.4.11 Partial Array Self-Refresh (PASR)

#### 7.4.11.1 PASR Bank Masking

The LPDDR3 SDRAM has eight banks (additional banks may be required for higher densities). Each bank of an LPDDR3 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see **MR16_PASR_Bank Mask (MA[7:0] = 10H)** PASR Bank Masking definitions table.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is described in the following section.

#### 7.4.11.2 PASR Segment Masking

A segment masking scheme may be used in place of or in combination with bank masking scheme in LPDDR3 SDRAM. LPDDR3 devices utilize eight segments per bank. For segment masking bit assignments, see **MR17_PASR_Segment Mask (MA[7:0] = 11H)** PASR Segment Masking definitions table.

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, “masked”. Programming of segment mask bits is similar to the one of bank mask bits. Eight segments are used as listed in **MR17_PASR_Segment Mask (MA[7:0] = 11H)** PASR Segment Masking definitions table. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. Programming of bits in the reserved registers has no effect on the device operation.

**Example of Bank and Segment Masking use in LPDDR3 devices**

| | Segment Mask(MR17) | Bank 0 | Bank 1 | Bank 2 | Bank 3 | Bank 4 | Bank 5 | Bank 6 | Bank 7 |
|---|---|---|---|---|---|---|---|---|---|
| **BankMask (MR16)** | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| **Segment 0** | 0 | - | M | - | - | - | - | - | M |
| **Segment 1** | 0 | - | M | - | - | - | - | - | M |
| **Segment 2** | 1 | M | M | M | M | M | M | M | M |
| **Segment 3** | 0 | - | M | - | - | - | - | - | M |
| **Segment 4** | 0 | - | M | - | - | - | - | - | M |
| **Segment 5** | 0 | - | M | - | - | - | - | - | M |
| **Segment 6** | 0 | - | M | - | - | - | - | - | M |
| **Segment 7** | 1 | M | M | M | M | M | M | M | M |

**Note:**

This table illustrates an example of an 8-bank LPDDR3 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked


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### 7.4.12 Mode Register Read (MRR) Command

The Mode Register Read (MRR) command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f–CA0f and CA9r–CA4r. The mode register contents are available on the first data beat of DQ[7:0] after RL x tCK + tDQSCK + tDQSQ following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in the DQ Calibration specification. All DQS are toggled for the duration of the mode register read burst.

The MRR command has a burst length of eight. MRR operation (consisting of the MRR command and the corresponding data traffic) must be interrupted. The MRR command period is tMRR.

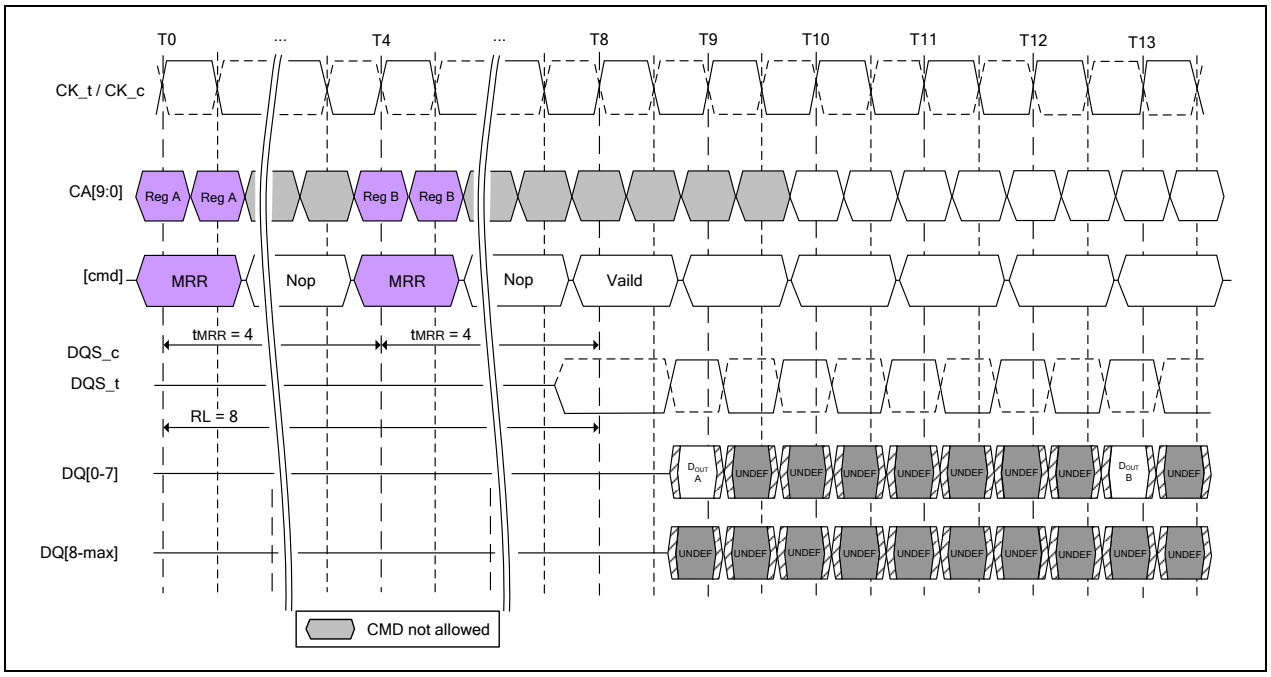



**Figure 32 - Mode Register Read timing example: RL = 8**

**Notes:**

1. MRRs to DQ calibration registers MR32 and MR40 are described in DQ calibration section.
2. Only the NOP command is supported during tMRR.
3. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
4. Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 8/2 + 1 - WL clock cycles.
5. Minimum Mode Register Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 8/2 + 1 clock cycles.
6. In this example, RL = 8 for illustration purposes only.

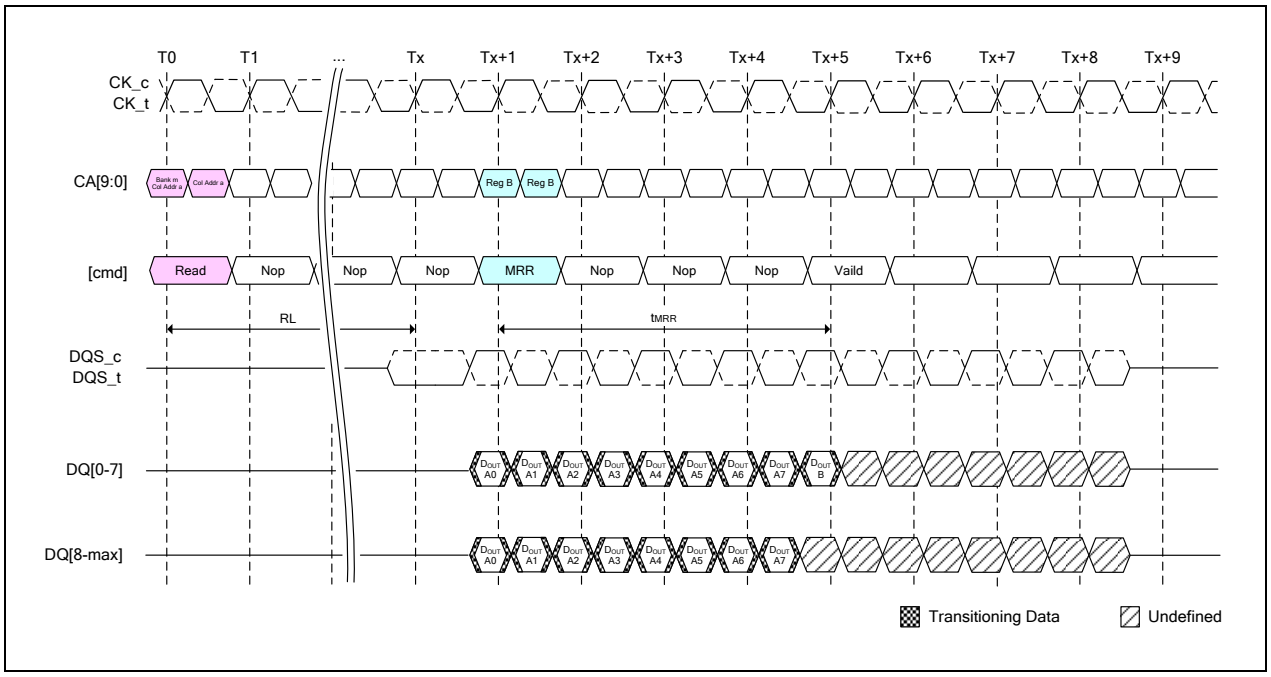



**Figure 33 - Read to MRR Timing**

**Notes:**

1. Only the NOP command is supported during tMRR.
2. The minimum number of clock cycles from the burst Read command to the MRR command is BL/2.

After a prior Read command, the MRR command must not be issued earlier than BL/2 clock cycles, or WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles after a prior Write command, as Read bursts and Write bursts must not be truncated by MRR.

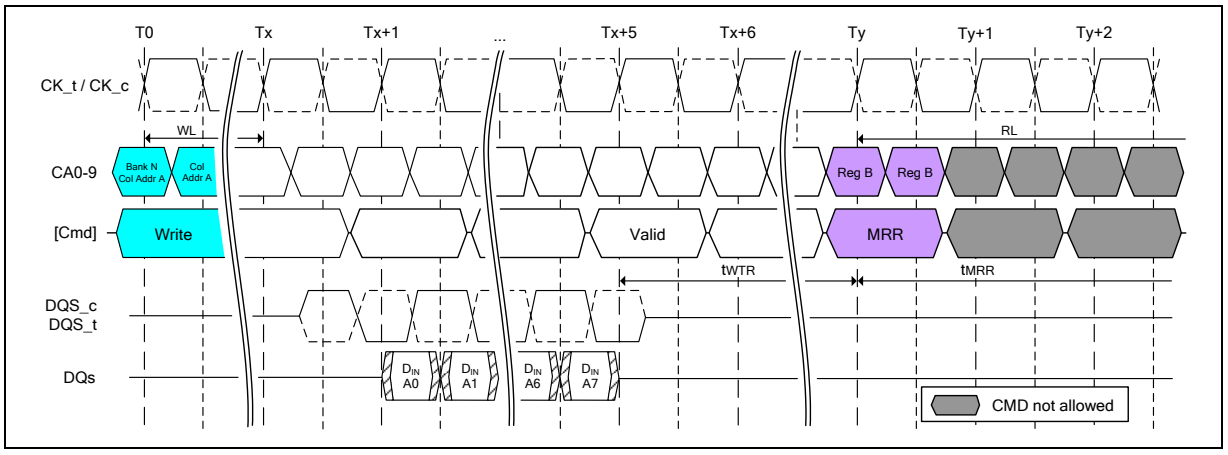



**Figure 34 - Burst Write Followed by MRR**

**Notes:**

1. The minimum number of clock cycles from the burst Write command to the MRR command is [WL + 1 + BL/2 + RU( tWTR/tCK)].
2. Only the NOP command is supported during tMRR.

Following the idle power-down state, an additional time, tMRRI, is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from standby, idle power-down mode.

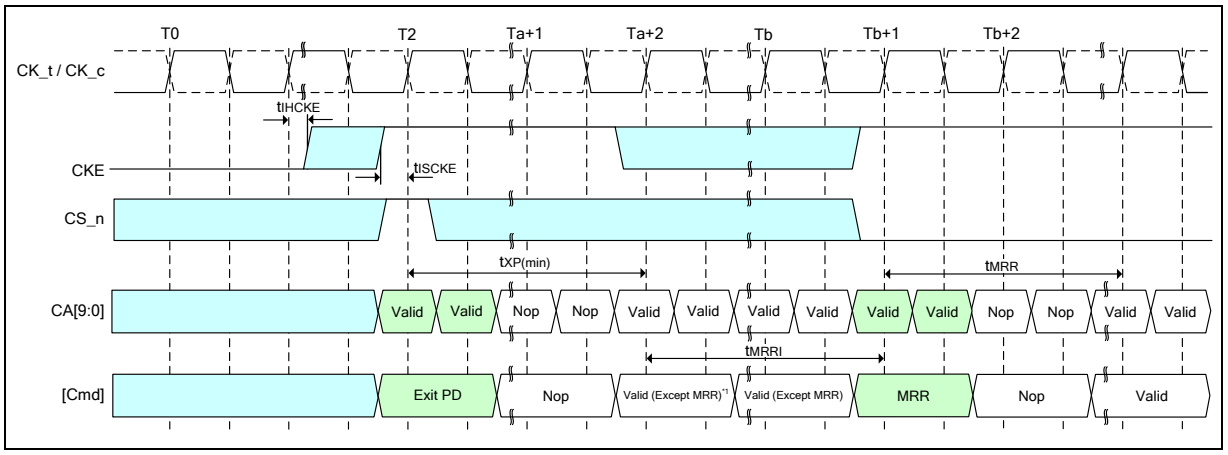



**Figure 35 - MRR Following Power-Down Idle State**

**Notes:**

1. Any valid command from the idle state except MRR.
2. tMMRI = tRCD.

#### 7.4.12.1 Temperature Sensor

LPDDR3 SDRAM features a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the extended temperature range and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature (See 8.2.3 **"Operating Temperature Range"** table) may be used to determine whether operating temperature requirements are being met.

LPDDR3 devices shall monitor device temperature and update MR4 according to $t_{TSI}$. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than $t_{TSI}$.

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification (See 8.2.3 **"Operating Temperature Range"** table) that applies for the standard or extended temperature ranges. For example, $T_{CASE}$ may be above 85°C when MR4[2:0] equals 011b. LPDDR3 devices shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller re-configures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval ($t_{TSI}$) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq 2°C$$

**Table of Temperature Sensor**

| Parameter | Symbol | Max/Min | Value | Unit |
|---|---|---|---|---|
| System Temperature Gradient | TempGradient | Max | System Dependent | °C/S |
| MR4 Read Interval | ReadInterval | Max | System Dependent | mS |
| Temperature Sensor Interval | $t_{TSI}$ | Max | 32 | mS |
| System Response Delay | SysRespDelay | Max | System Dependent | mS |
| Device Temperature Margin | TempMargin | Max | 2 | ºC |

For example, if TempGradient is 10°C/S and the SysRespDelay is 1 mS:

$$10°C/S \times (ReadInterval + 32mS + 1mS) \leq 2°C$$

In this case, ReadInterval shall be no greater than 167 mS.


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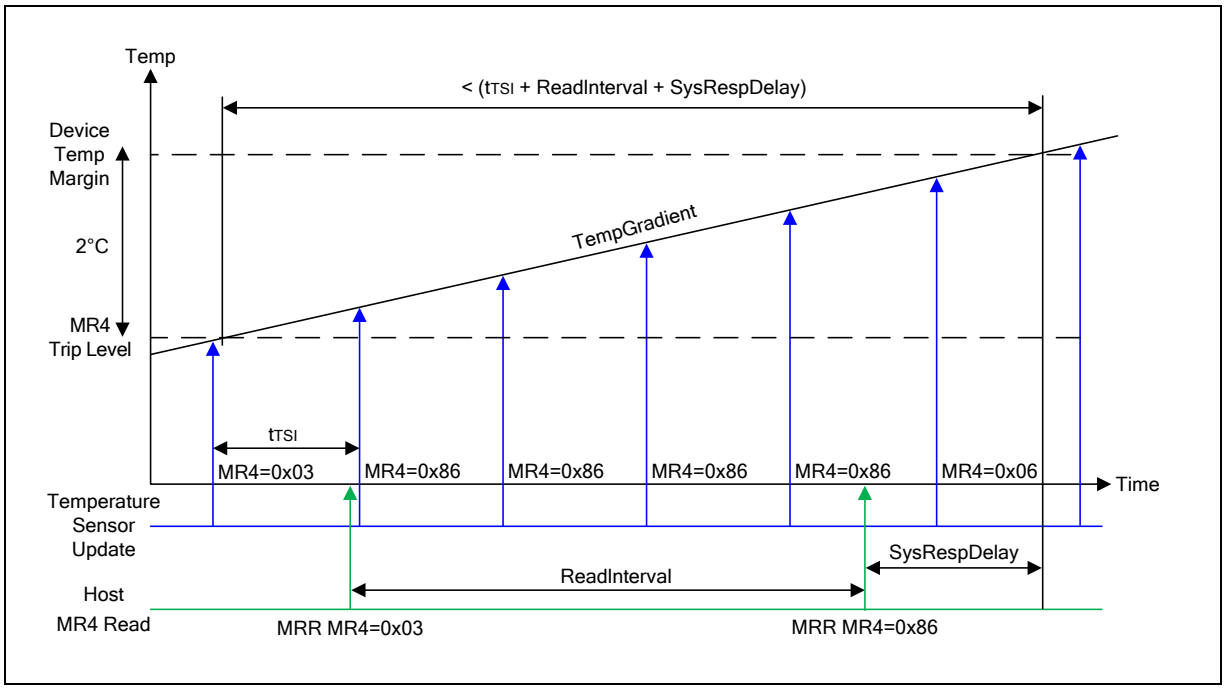



**Figure 36 - Temperature Sensor Timing**

### 7.4.12.2 DQ Calibration

LPDDR3 device features a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ[0] and DQ[8] for x16 devices, and DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices.

For x16 devices, DQ[7:1] and DQ[15:9] are showed the same information as DQ[0].

For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] are showed the same information as DQ[0].

**Table of Data Calibration Pattern Description**

| Pattern | Bit Time 0 | Bit Time 1 | Bit Time 2 | Bit Time 3 | Bit Time 4 | Bit Time 5 | Bit Time 6 | Bit Time 7 |
|---|---|---|---|---|---|---|---|---|
| Pattern “A” (MR32) | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| Pattern “B” (MR40) | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

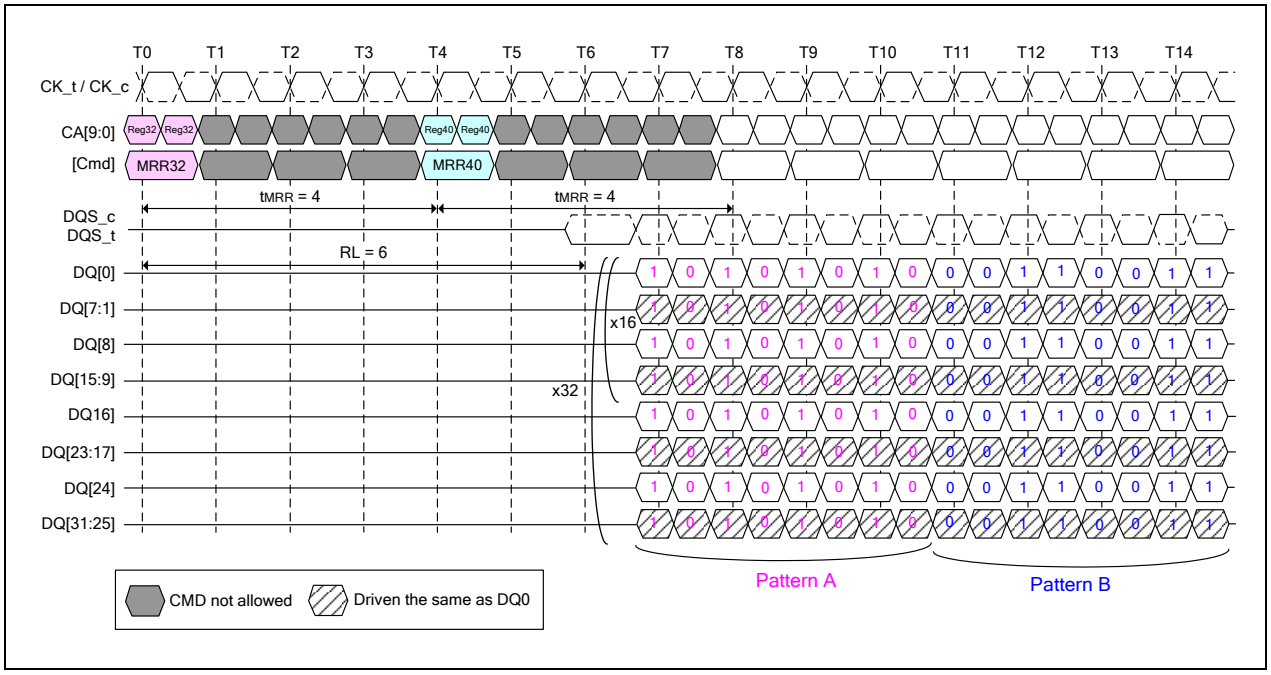



**Figure 37 - DQ Calibration Timing**

### 7.4.13 Mode Register Write (MRW) Command

The Mode Register Write (MRW) command is used to write configuration data to mode registers. The MRW command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f-CA0f, CA9r-CA4r. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by tMRW. Mode Register Writes to read-only registers have no impact on the functionality of the device.

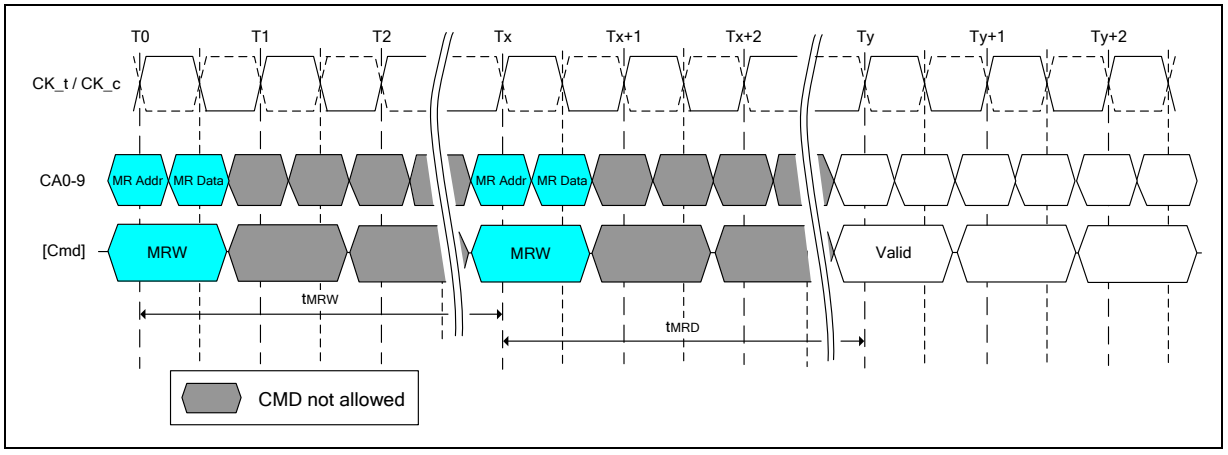



**Figure 38 - Mode Register Write Timing**

**Notes:**

1. At time Ty, the device is in the idle state.
2. Only the NOP command is supported during tMRW.

### 7.4.13.1 Mode Register Write

MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a Precharge-All command.

#### 7.4.13.1.1 MRW RESET

The MRW RESET command brings the device to the device auto-initialization (resetting) state in the power-on initialization sequence. The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command.

If the initialization is to be performed at-speed (greater than the recommended boot clock frequency), then CA Training may be necessary to ensure setup and hold timings. Since the MRW RESET command is required prior to CA Training it may be difficult to meet setup and hold requirements. User may however choose the OP code 0xFCh. This encoding ensures that no transitions are required on the CA bus between rising and falling clock edge. Prior to CA Training, it is recommended to hold the CA bus stable for one cycle prior to, and one cycle after, the issuance of the MRW RESET command to ensure setup and hold timings on the CA bus.

**Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)**

| Current State | Command | Intermediate State | Next State |
|---|---|---|---|
| All Banks Idle | MRR | Mode Register Reading (All Banks Idle) | All Banks Idle |
| | MRW | Mode Register Writing (All Banks Idle) | All Banks Idle |
| | MRW (RESET) | Resetting (Device Auto-Initialization) | All Banks Idle |
| Bank(s) Active | MRR | Mode Register Reading (Bank(s) Active) | Bank(s) Active |
| | MRW | Not Allowed | Not Allowed |
| | MRW (RESET) | Not Allowed | Not Allowed |

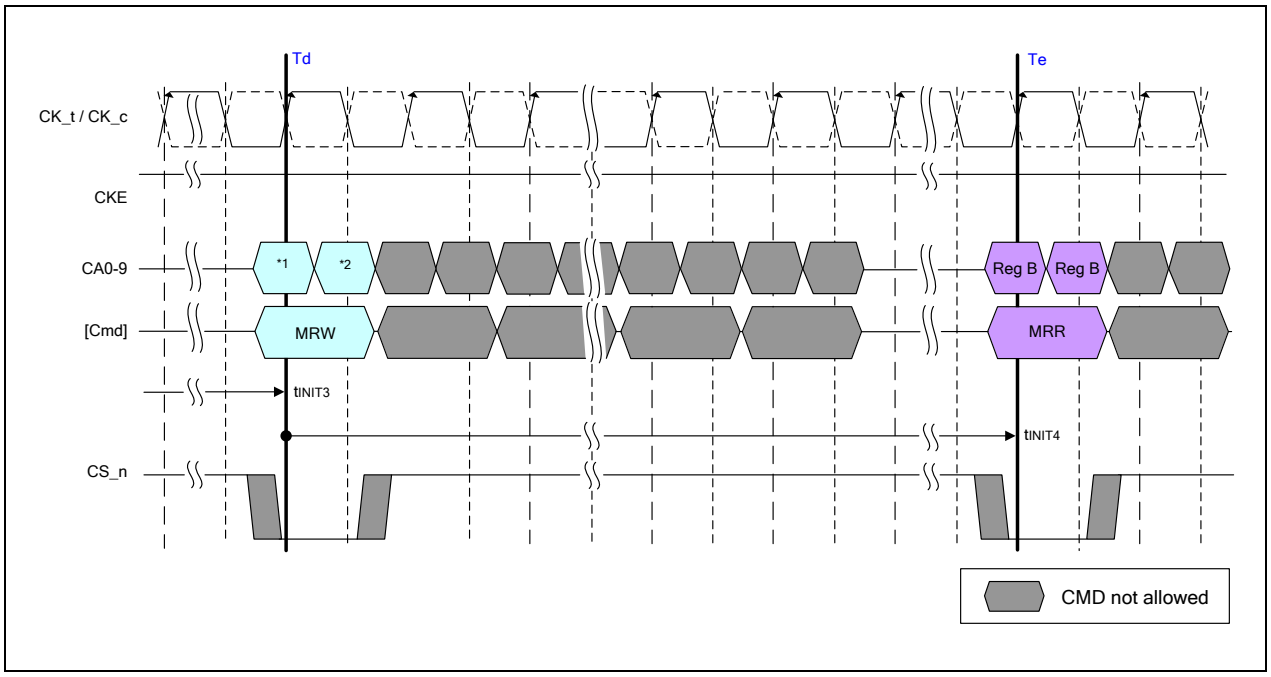



**Figure 39 - Mode Register Write Timing for MRW RESET**

**Notes:**
1. CA [9:0] = 3F0h.
2. CA [9:0] = 3F0h or xxxh.

### 7.4.13.2 Mode Register Write ZQ Calibration Command

The MRW command is used to initiate the ZQ Calibration command. This command is used to calibrate the output driver impedance and on-die termination across process, temperature, and voltage. LPDDR3 devices support ZQ calibration.

There are four ZQ calibration commands and related timings times, tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT is for initialization calibration, tZQRESET is for resetting ZQ to the default output impedance, tZQCL is for long calibration(s), and tZQCS is for short calibration(s).

The Initialization ZQ calibration (ZQINIT) must be performed for LPDDR3. ZQINIT provides an output impedance accuracy of ±15%. After initialization, the ZQ Calibration Long (ZQCL) can be used to re-calibrate the system to an output impedance accuracy of ±15%. A ZQ Calibration Short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system. The ZQ Reset command (ZQRESET) resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQCorrection) of output impedance error within tZQCS for all speed bins, assuming the maximum sensitivities specified are met. The appropriate interval between ZQCS commands can be determined from using these tables and system-specific parameters.

LPDDR3 devices are subject to temperature drift rate (Tdriftrate) and voltage drift rate (Vdriftrate) in various applications. To accommodate drift rates and calculate the necessary interval ZQCS command, apply the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)} = CalibrationInterval$$

where TSens = max(dRONdT) and VSens = max(dRONdV) define temperature and voltage sensitivities.

For example, if TSens = 0.75% / °C, VSens = 0.20% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

A ZQ Calibration command can only be issued when the device is in idle state with all banks precharged. ODT shall be disabled via the mode register or the ODT pin prior to issuing a ZQ calibration command. No other activities can be performed on the data bus and the data bus shall be un-terminated during the calibration period (tZQINIT, tZQCL, or tZQCS). The quiet time on the data bus helps to accurately calibrate output impedance. There is no required quiet time after the ZQRESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ pin circuitry is disabled to reduce power consumption. In systems sharing a ZQ resistor between devices, the controller must prevent tZQINIT, tZQCS, and tZQCL overlap between the devices. ZQRESET overlap is acceptable.

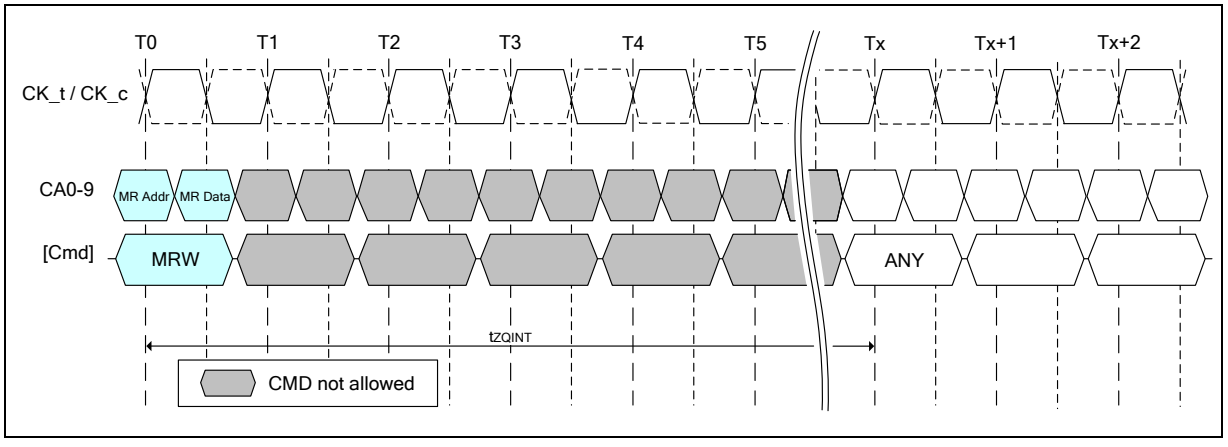



**Figure 40 - ZQ Initialization Timing**

**Notes:**

1. Only the NOP command is supported during ZQ calibration.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.


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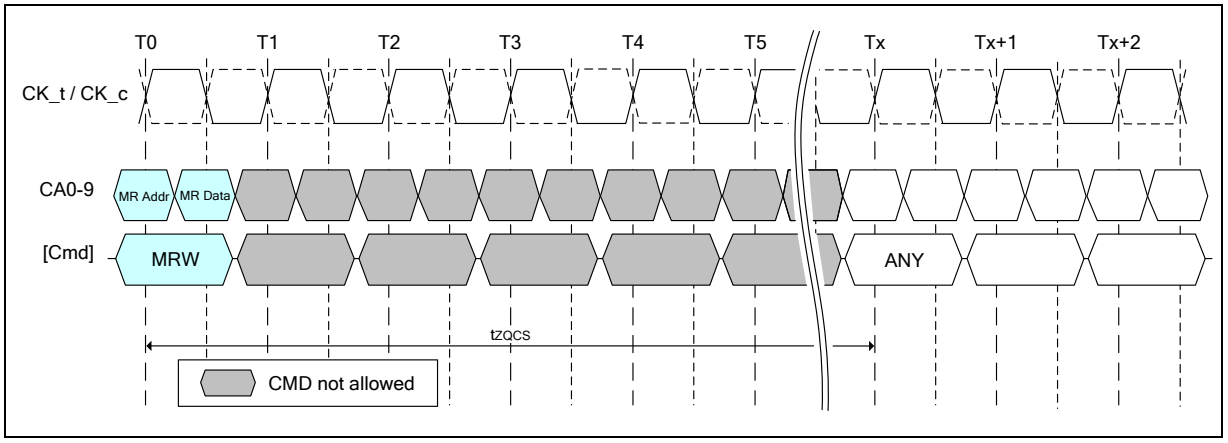



**Figure 41 - ZQ Calibration Short Timing**

**Notes:**

1. Only the NOP command is supported during ZQ calibration.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

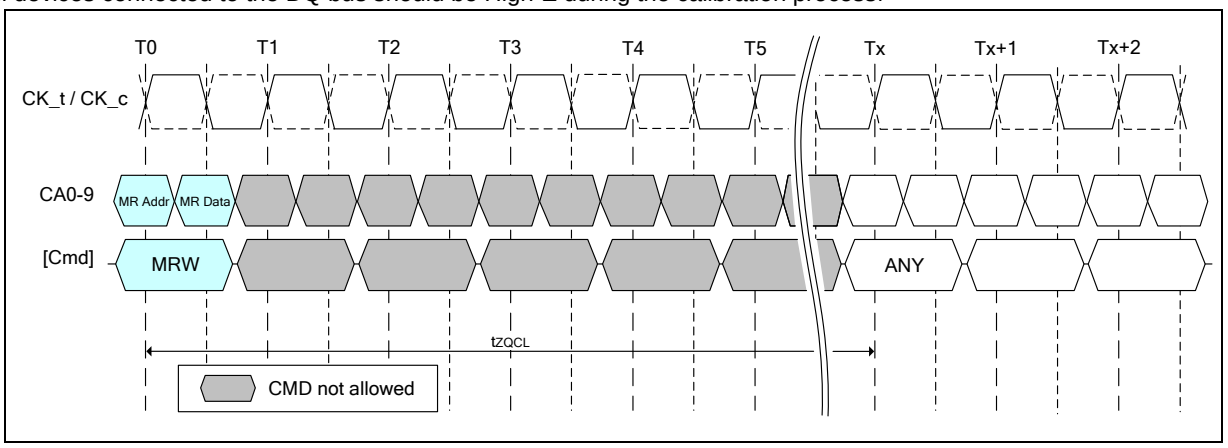



**Figure 42 - ZQ Calibration Long Timing**

**Notes:**

1. Only the NOP command is supported during ZQ calibration.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

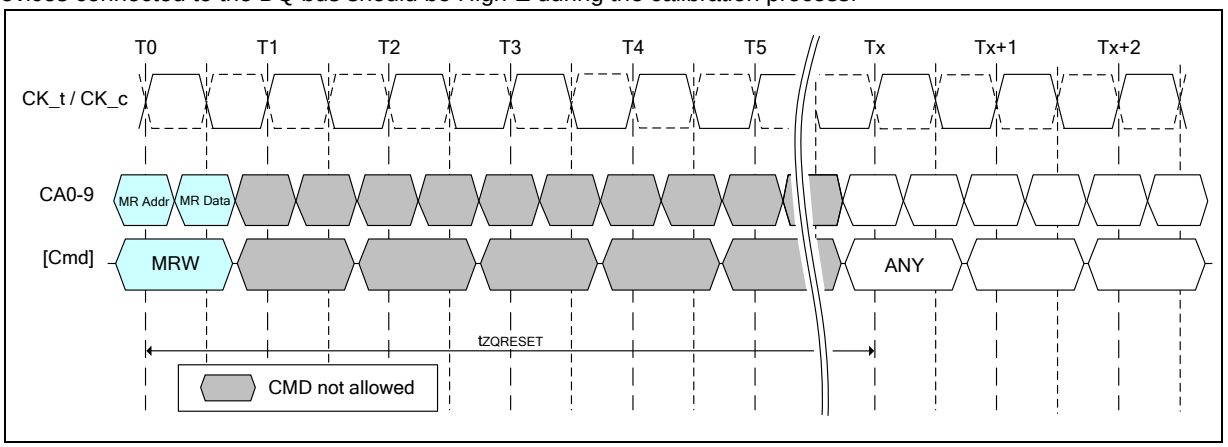



**Figure 43 - ZQ Calibration Reset Timing**

**Notes:**

1. Only the NOP command is supported during ZQ calibration.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.


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#### 7.4.13.2.1 ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, a RZQ ± 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited (See section 8.3 **"Input/Output Capacitance"** table).

### 7.4.13.3 Mode Register Write – CA Training Mode

Because CA inputs operate as double data rate, it may be difficult for memory controller to satisfy CA input setup/hold timings at higher frequency. A CA Training mechanism is provided.

#### 7.4.13.3.1 CA Training Sequence

a) CA Training mode entry: Mode Register Write to MR41
b) CA training session: Calibrate CA0, CA1, CA2, CA3, CA5, CA6, CA7 and CA8 (see the CA to DQ mapping (CA Training mode enabled with MR41) table in next page)
c) CA to DQ mapping change: Mode register Write to MR48
d) Additional CA Training session: Calibrate remaining CA pins (CA4 and CA9) (see the CA to DQ mapping (CA Training mode is enabled with MR48) table in next page)
e) CA Training mode exit: Mode register Write to MR42

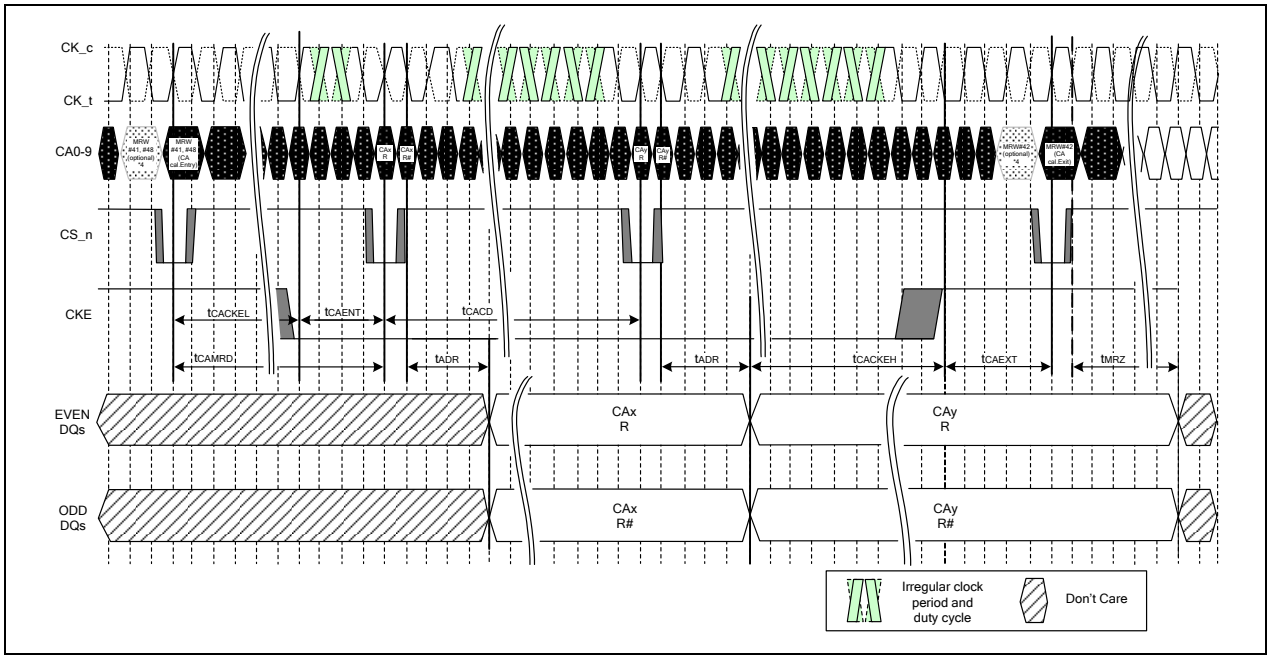



**Figure 44 – CA Training Timing Chart**

**Notes:**

1. Unused DQ must be valid HIGH or LOW during data output period. Unused DQ may transition at the same time as the active DQ. DQS must remain static and not transition.
2. CA to DQ mapping change via MR 48 omitted here for clarity of the timing diagram. Both MR41 and MR48 training sequences must be completed before exiting the training mode (MR42). To enable a CA to DQ mapping change, CKE must be driven HIGH prior to issuance of the MRW 48 command.
3. Because data out control is asynchronous and will be an analog delay from when all the CA data is available, tADR and tMRZ are defined from CK_t falling edge.
4. It is recommended to hold the CA bus stable for one cycle prior to and one cycle after the issuance of the MRW CA training entry/exit command to ensure setup and hold timings on the CA bus.
5. Clock phase may be adjusted in CA training mode while CS_n is high and CKE is low resulting in an irregular clock with shorter/longer periods and pulse widths.

The LPDDR3 SDRAM may not properly recognize a Mode Register Write command at normal operation frequency before CA Training is finished. Special encodings are provided for CA Training mode enable/disable. MR41 and MR42 encodings are selected so that rising edge and falling edge values are the same. The LPDDR3 SDRAM will recognize MR41 and MR42 at normal operation frequency even before CA timing adjustment is finished.

Calibration data will be output through DQ pins. CA to DQ mapping is described in CA to DQ mapping (CA Training mode enabled with MR41) table.

After timing calibration with MR41 is finished, users will issue MRW to MR48 and calibrate remaining CA pins (CA4 and CA9) using (DQ0/DQ1 and DQ8/DQ9) as calibration data output pins. See the CA to DQ mapping (CA Training mode is enabled with MR48) table.

CA Training timing values are specified in section 8.8.1 **"LPDDR3 AC Timing"** Table.

**CA Training mode enable (MR41(29H, 0010 1001b), OP=A4H(1010 0100b))**

| | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 | CA8 | CA9 |
|---|---|---|---|---|---|---|---|---|---|---|
| Rising Edge | L | L | L | L | H | L | L | H | L | H |
| Falling Edge | L | L | L | L | H | L | L | H | L | H |

**CA Training mode disable (MR42(2AH, 0010 1010b), OP=A8H(1010 1000b))**

| | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 | CA8 | CA9 |
|---|---|---|---|---|---|---|---|---|---|---|
| Rising Edge | L | L | L | L | L | H | L | H | L | H |
| Falling Edge | L | L | L | L | L | H | L | H | L | H |

**CA to DQ mapping (CA Training mode enabled with MR41)**

| CA0 | CA1 | CA2 | CA3 | CA5 | CA6 | CA7 | CA8 | Clock edge |
|---|---|---|---|---|---|---|---|---|
| DQ0 | DQ2 | DQ4 | DQ6 | DQ8 | DQ10 | DQ12 | DQ14 | CK_t rising edge |
| DQ1 | DQ3 | DQ5 | DQ7 | DQ9 | DQ11 | DQ13 | DQ15 | CK_t falling edge |

**CA Training mode enable (MR48(30H, 0011 0000b), OP=C0H(1100 0000b))**

| | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 | CA8 | CA9 |
|---|---|---|---|---|---|---|---|---|---|---|
| Rising Edge | L | L | L | L | L | L | L | L | H | H |
| Falling Edge | L | L | L | L | L | L | L | L | H | H |

**CA to DQ mapping (CA Training mode is enabled with MR48)**

| CA4 | CA9 | Clock edge |
|---|---|---|
| DQ0 | DQ8 | CK_t rising edge |
| DQ1 | DQ9 | CK_t falling edge |

**Note:** Other DQs must have valid output (either HIGH or LOW)


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### 7.4.13.4 Mode Register Write – WR Leveling Mode

In order to provide for improved signal integrity performance, the LPDDR3 SDRAM provides a write leveling feature to compensate for timing skew, affecting timing parameters such as tDQSS, tDSS, and tDSH.

The memory controller uses the write leveling feature to receive feedback from the SDRAM allowing it to adjust the clock to data strobe signal relationship for each DQS_t/DQS_c signal pair. The memory controller performing the leveling must have adjustable delay setting on DQS_t/DQS_c signal pair to align the rising edge of DQS signals with that of the clock signal at the DRAM pin. The DRAM asynchronously feeds back CLK, sampled with the rising edge of DQS signals. The controller repeatedly delays DQS signals until a transition from 0 to 1 is detected. The DQS signals delay established through this exercise ensures the tDQSS specification can be met.

All DQS signals may have to be leveled independently. During Write Leveling operations each DQS signal latches the clock with a rising strobe edge and drives the result on all DQ[n] of its respective byte.

The LPDDR3 SDRAM enters into write leveling mode when mode register MR2[7] is set HIGH. When entering write leveling mode, the state of the DQ pins is undefined. During write leveling mode, only NOP commands are allowed, or MRW command to exit write leveling operation. Upon completion of the write leveling operation, the DRAM exits from write leveling mode when MR2[7] is reset LOW.

The controller will drive DQS_t LOW and DQS_c HIGH after a delay of tWLDQSEN. After time tWLMRD, the controller provides DQS signal input which is used by the DRAM to sample the clock signal driven from the controller. The delay time tWLMRD(max) is controller dependent. The DRAM samples the clock input with the rising edge of DQS and provides asynchronous feedback on all the DQ bits after time tWLO. The controller samples this information and either increment or decrement the DQS_t and/or DQS_c delay settings and launches the next DQS/DQS# pulse. The sample time and trigger time is controller dependent. Once the following DQS_t/DQS_c transition is sampled, the controller locks the strobe delay settings, and write leveling is achieved for the device. Figure 45 describes the timing for the write leveling operation.

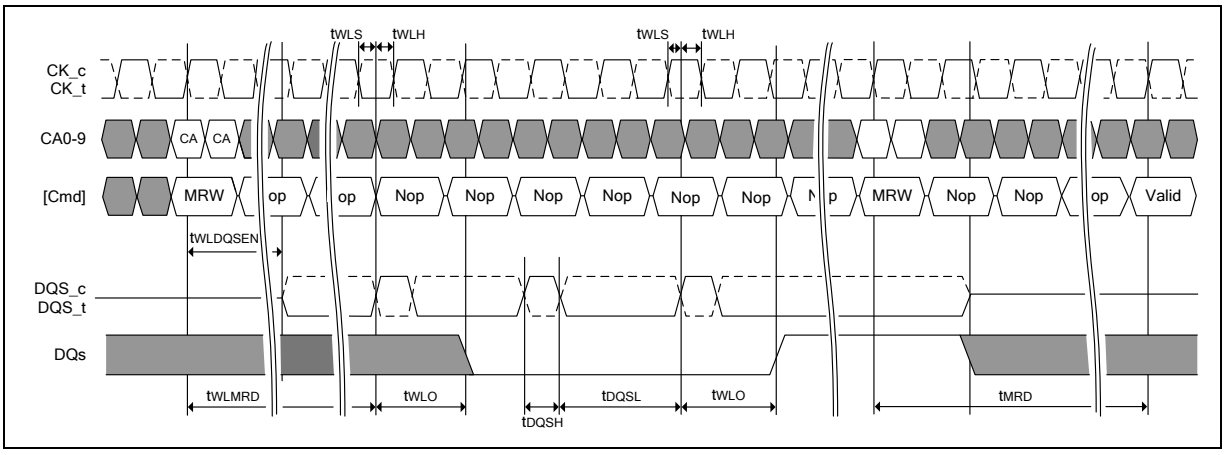



**Figure 45 - Write Leveling Timing**

### 7.4.14 On-Die Termination

ODT (On-Die Termination) is a feature of the LPDDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS_t, DQS_c and DM via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. Unlike other command inputs, the ODT pin directly controls ODT operation and is not sampled by the clock.

The ODT feature is turned off and not supported in Self-Refresh and Deep Power Down modes. ODT operation can optionally be enabled during CKE Power Down via a mode register. Note that if ODT is enabled during Power Down mode VDDQ may not be turned off during Power Down. The DRAM will also disable termination during read operations.

A simple functional representation of the DRAM ODT feature is shown below.

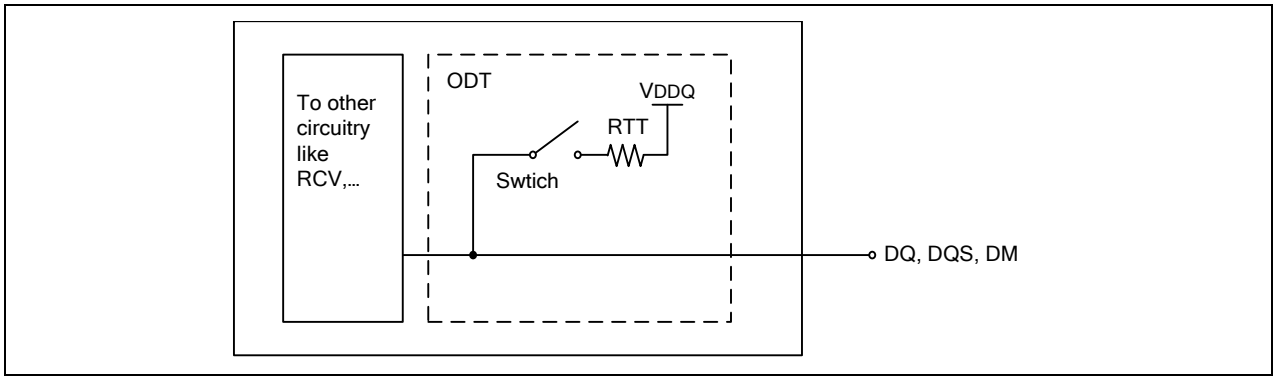



**Figure 46 - Functional Representation of ODT**

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other mode register control information. The value of RTT is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Register MR11 is programmed to disable ODT, in self-refresh, in deep power down, in CKE power down (mode register option) and during read operations.

#### 7.4.14.1 ODT Mode register

The ODT Mode is enabled if MR11 OP<1:0> are non zero. In this case, the value of RTT is determined by the settings of those bits. The ODT Mode is disabled if MR11 OP<1:0> are zero.

MR11 OP<2> determines whether ODT, if enabled through MR11 OP<1:0>, will operate during CKE power down.

#### 7.4.14.2 Asynchronous ODT

The ODT feature is controlled asynchronously based on the status of the ODT pin, except ODT is off when:

- ODT is disabled through MR11 OP<1:0>.
- DRAM is performing a read operation (RD or MRR).
- DRAM is in CKE Power Down and MR11 OP<2> is zero.
- DRAM is in Self-Refresh or Deep Power Down modes.
- DRAM is in CA Training Mode.

In asynchronous ODT mode, the following timing parameters apply when ODT operation is controlled by the ODT pin: tODTon,min,max, tODToff,min,max.

Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn on time (tODTon,max) is the point in time when the ODT resistance is fully on. tODTon,min and tODTon,max are measured from ODT pin high.

Minimum RTT turn-off time (tODToff,min) is the point in time when the device termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (tODToff,max) is the point in time when the on-die termination has reached high impedance. tODToff,min and tODToff,max are measured from ODT pin low.


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#### 7.4.14.3 ODT During Read Operations (RD or MRR)

During read operations, LPDDR3 SDRAM will disable termination and disable ODT control through the ODT pin. After read operations are completed, ODT control is resumed through the ODT pin (if ODT Mode is enabled).

#### 7.4.14.4 ODT During Power Down

When MR11 OP<2> is zero, termination control through the ODT pin will be disabled when the DRAM enters CKE power down. After a power down command is registered, termination will be disabled within a time window specified by tODTd,min,max. After a power down exit command is registered, termination will be enabled within a time window specified by tODTe,min,max.

Minimum RTT disable time (tODTd,min) is the point in time when the device termination circuit will no longer be controlled by the ODT pin. Maximum ODT disable time (tODTd,max) is the point in time when the on-die termination will be in high impedance.

Minimum RTT enable time (tODTe,min) is the point in time when the device termination circuit will no longer be in high impedance. The ODT pin shall control the device termination circuit after maximum ODT enable time (tODTe,max) is satisfied.

When MR11 OP<2> is enabled and MR11 OP<1:0> are non zero, ODT operation is supported during CKE power down with ODT control through the ODT pin.

#### 7.4.14.5 ODT During Self Refresh

LPDDR3 SDRAM disables the ODT function during self refresh. After a self refresh command is registered, termination will be disabled within a time window specified by tODTd,min,max. After a self refresh exit command is registered, termination will be enabled within a time window specified by tODTe,min,max.

#### 7.4.14.6 ODT During Deep Power Down

LPDDR3 SDRAM disables the ODT function during deep power down. After a deep power down command is registered, termination will be disabled within a time window specified by tODTd,min,max.

#### 7.4.14.7 ODT During CA Training and Write Leveling

During CA Training Mode, LPDDR3 SDRAM will disable on-die termination and ignore the state of the ODT control pin. For ODT operation during Write Leveling mode, refer to the table below for termination activation and deactivation for DQ and DQS_t/DQS_c.

**DRAM Termination Function In Write Leveling Mode**

| ODT pin | DQS_t/DQS_c termination | DQ termination |
|---|---|---|
| De-asserted | OFF | OFF |
| Asserted | ON | OFF |

If ODT is enabled, the ODT pin must be high, in Write Leveling mode.

**ODT States Truth Table**

| | Write | Read/DQ Cal | ZQ Cal | CA Training | Write Level |
|---|---|---|---|---|---|
| DQ Termination | Enabled | Disabled | Disabled | Disabled | Disabled |
| DQS Termination | Enabled | Disabled | Disabled | Disabled | Enabled |

**Note:** ODT is enabled with MR11[1:0]=01b, 10b, or 11b and ODT pin HIGH. ODT is disabled with MR11[1:0]=00b or ODT pin LOW.


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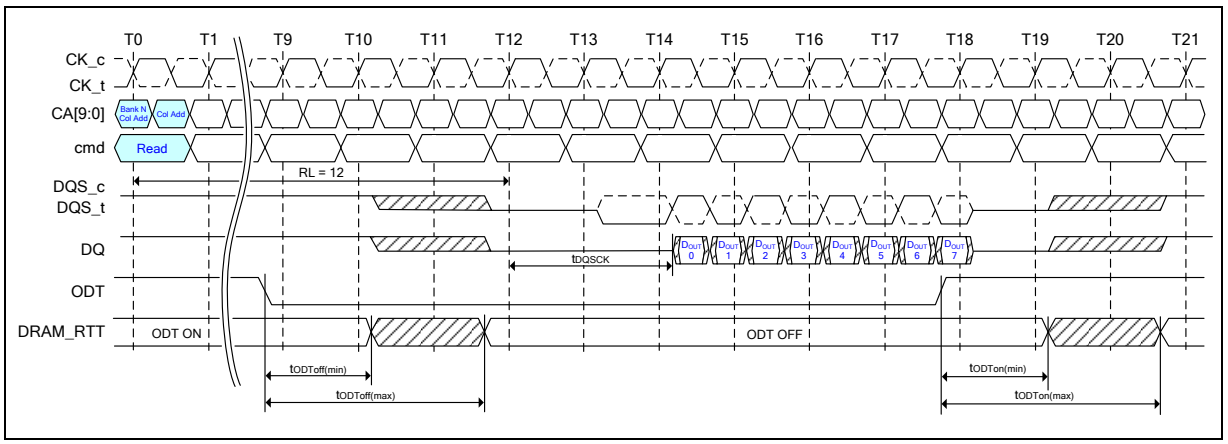



**Figure 47 – Asynchronous ODT Timing Example for RL = 12**

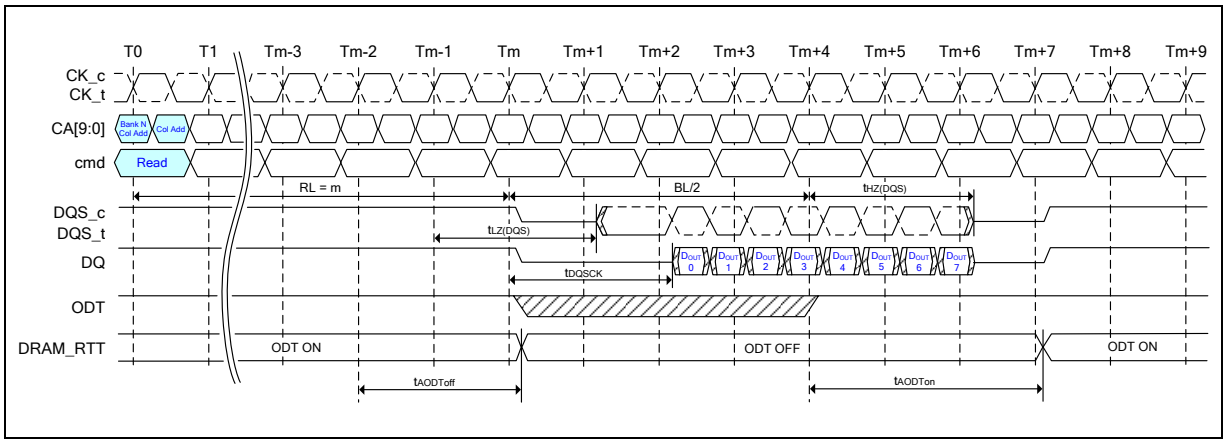



**Figure 48 - Automatic ODT Timing During READ Operation Example for RL = m**

**Notes:**

1. The automatic RTT turn-off delay, tAODToff, is referenced from the rising edge of "RL-2" clock at Tm-2.
2. The automatic RTT turn-on delay, tAODTon, is referenced from the rising edge of "RL+ BL/2" clock at Tm+4.

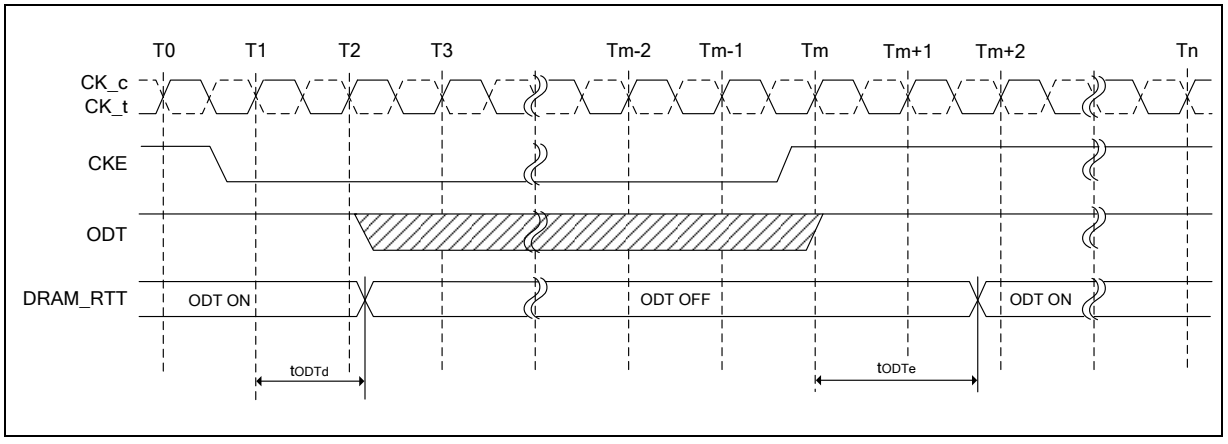



**Figure 49 –ODT Timing During Power Down, Self Refresh, Deep Power Down Entry/Exit Example**

**Notes:**

1. Upon exit of Deep Power Down mode, a complete power-up initialization sequence is required.
2. tODTd has a different value if the command at T1 is normal Power Down entry, Deep Power Down entry or Self Refresh entry; see section 8.8.1 **"LPDDR3 AC Timing"** Table**.**

### 7.4.15 Power-Down

Power-down is entered synchronously when CKE is registered LOW and CS_n is HIGH at the rising edge of clock. CKE must not go LOW while MRR, MRW, Read, or Write operations are in progress. CKE can go LOW while any other operations such as row activation, Precharge, auto precharge, or Refresh are in progress, but the power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in Figure 50 to Figure 61.

Entering power-down deactivates the input and output buffers, excluding CKE. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as tCPDED. CKE LOW will result in deactivation of input receivers after tCPDED has expired. In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care”. CKE LOW must be maintained until tCKE,min is satisfied. VREFCA must be maintained at a valid level during power-down.

VDDQ can be turned off during power-down. If VDDQ is turned off, VREFDQ must also be turned off. Prior to exiting power-down, both VDDQ and VREFDQ must be within their respective minimum/maximum operating ranges.

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in the Refresh command section.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE,min is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. For the description of ODT operation and specifications during power-down entry and exit, see section 7.4.14 “**On-Die Termination**”.

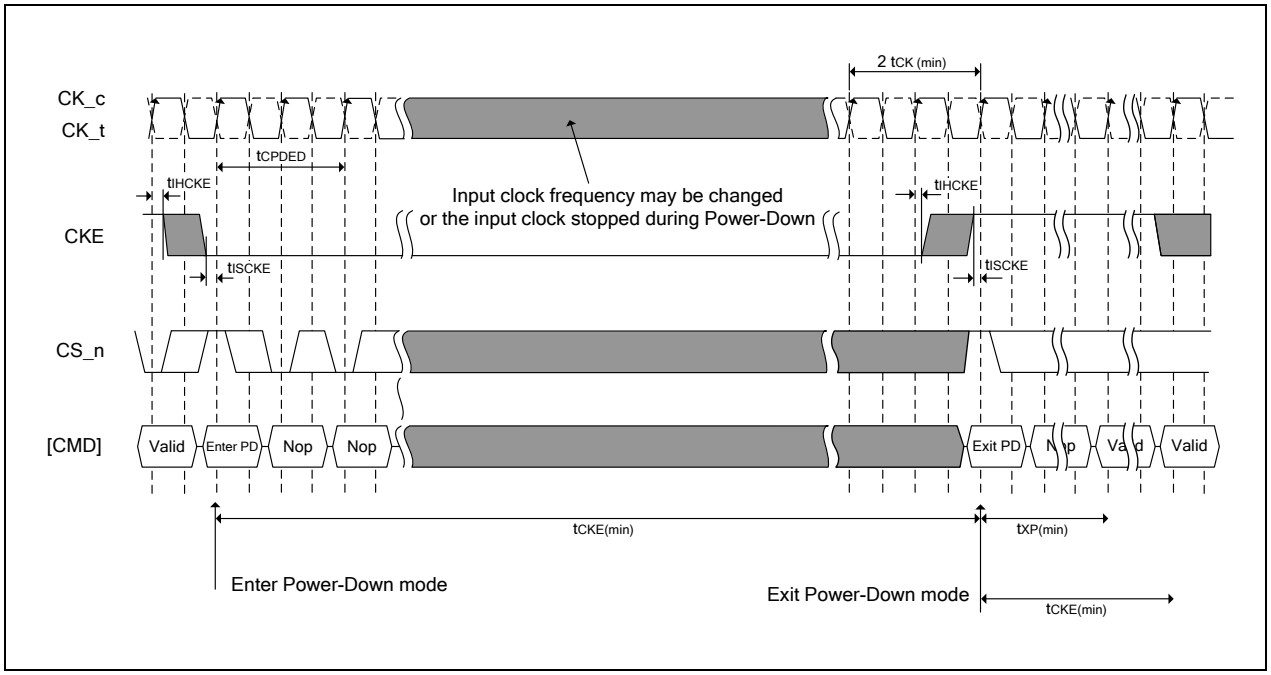



**Figure 50 - Basic Power-Down Entry and Exit Timing**

**Note:**

Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

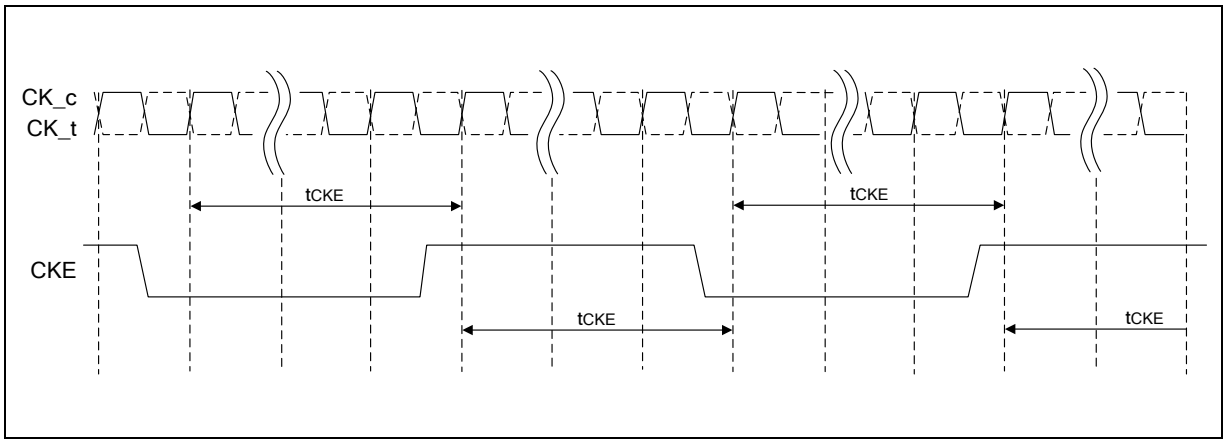



**Figure 51 - CKE-Intensive Environment**

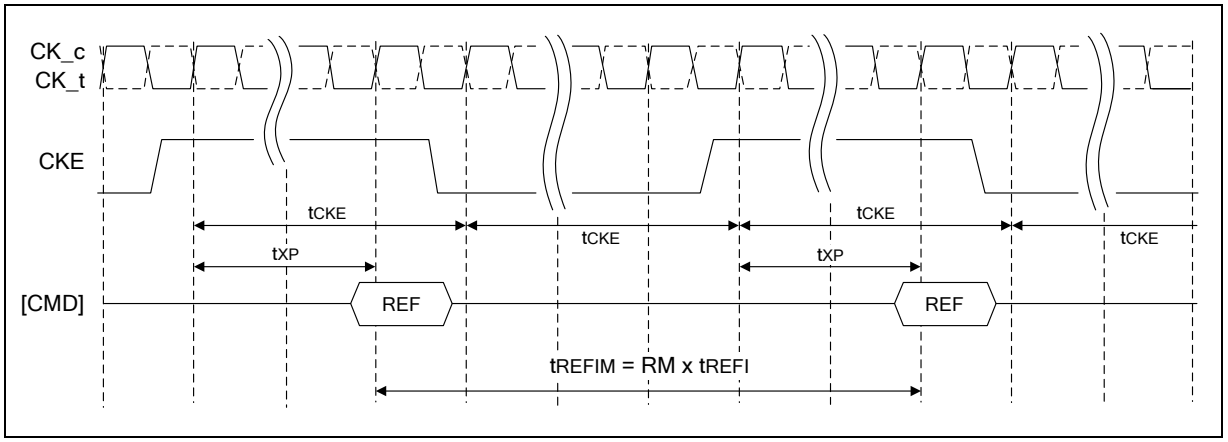



**Figure 52 - Refresh-to-Refresh Timing in CKE-Intensive Environments**

**Note:**
The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

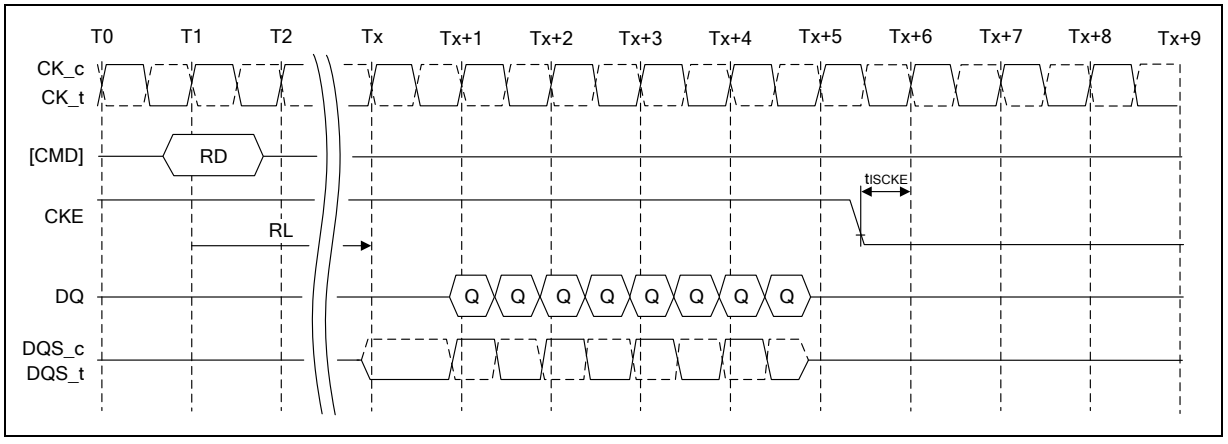



**Figure 53 - Read to Power-Down Entry**

**Notes:**
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 clock cycles after the clock on which the Read command is registered.

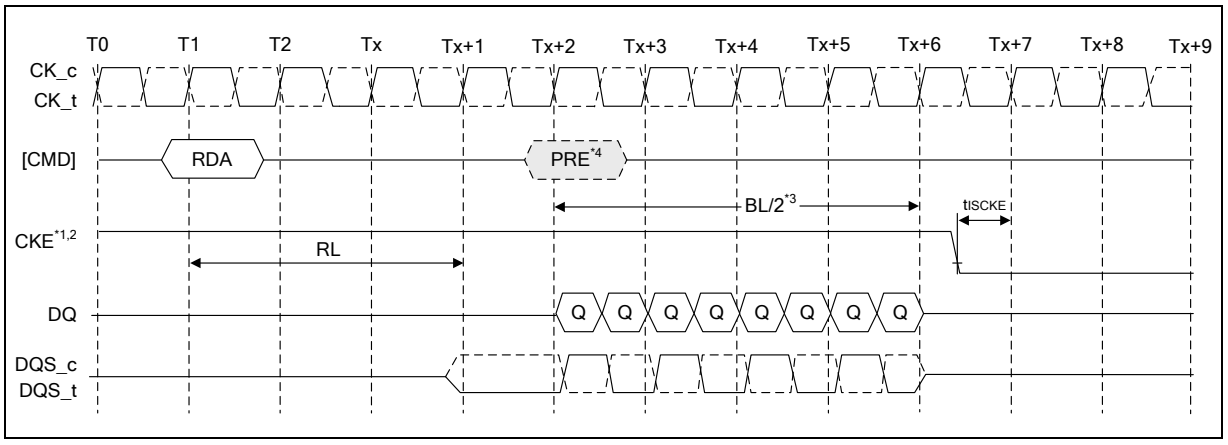



**Figure 54 - Read with Auto Precharge to Power-Down Entry**

**Notes:**

1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at RL + RU(tDQSCK/tCK)+ BL/2 + 1 clock cycles after the clock on which the Read command is registered.
3. BL/2 with tRTP = 7.5nS and tRAS(MIN) is satisfied.
4. Start internal Precharge.

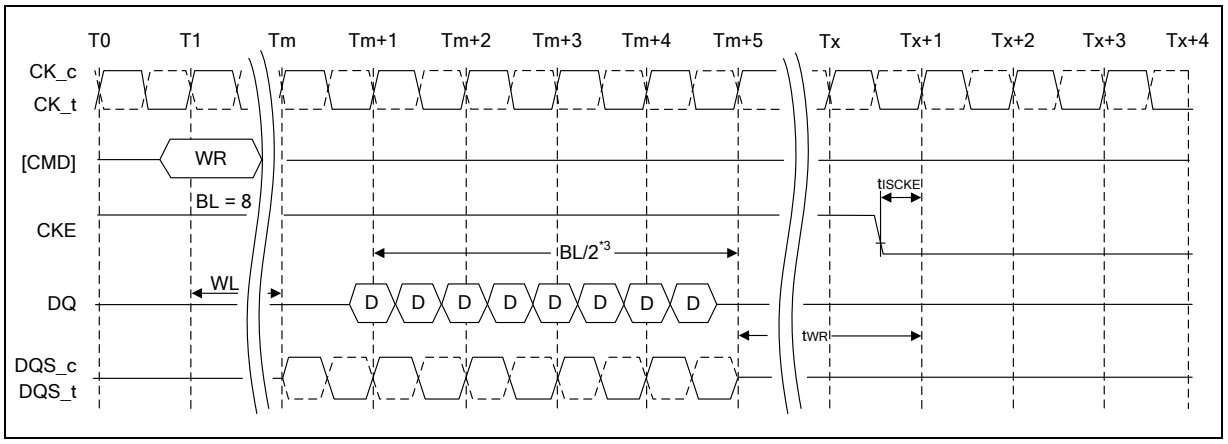



**Figure 55 - Write to Power-Down Entry**

**Note:**

CKE can be registered LOW at WL + 1 + BL/2 + RU(tWR/tCK) clock cycles after the clock on which the Write command is registered.

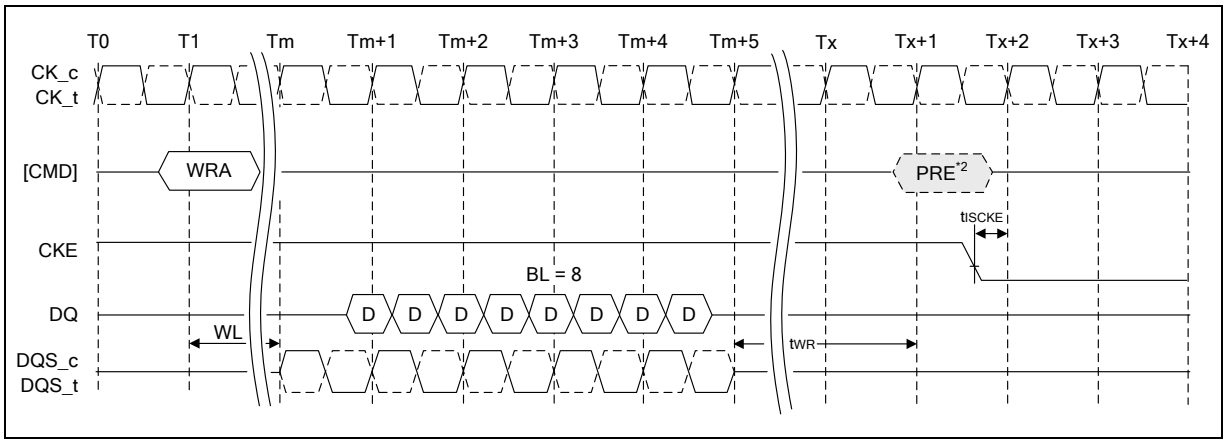



**Figure 56 - Write with Auto Precharge to Power-Down Entry**

**Notes:**

1. CKE can be registered LOW at WL + 1 + BL/2 + RU(tWR/tCK) + 1 clock cycles after the Write command is registered.
2. Start internal Precharge.

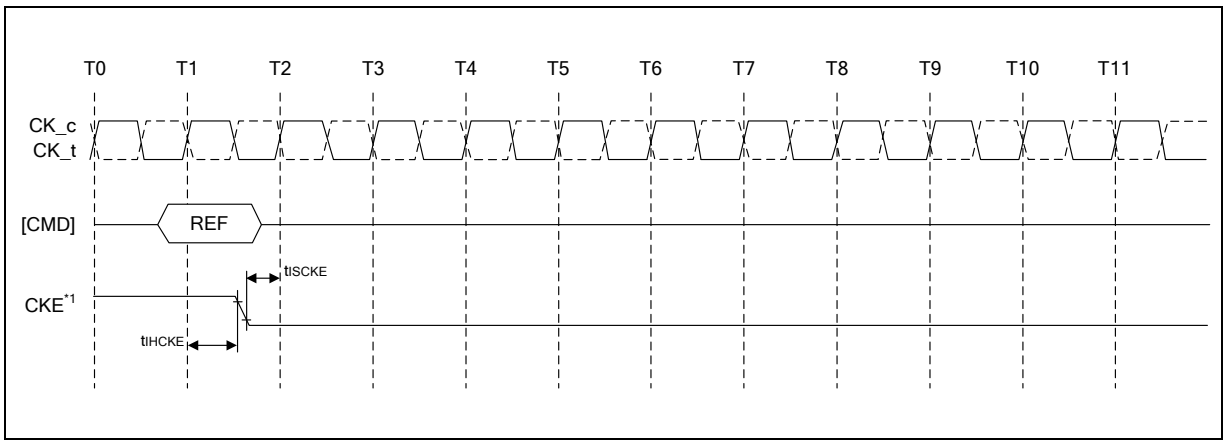



**Figure 57 - Refresh Command to Power-Down Entry**

**Note:**

1. CKE can go LOW tIHCKE after the clock on which the Refresh command is registered.

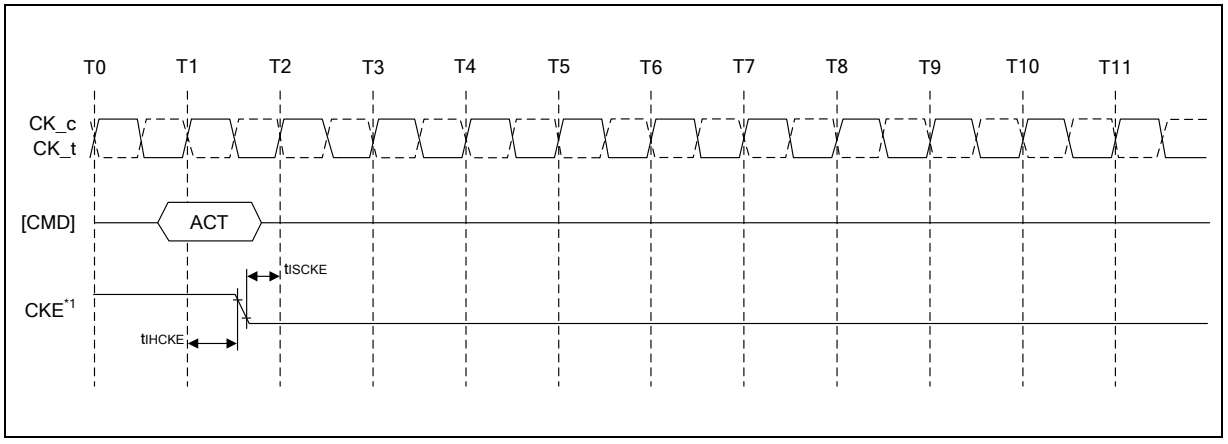



**Figure 58 - Activate Command to Power-Down Entry**

**Note:**

1. CKE can go LOW at tIHCKE after the clock on which the Activate command is registered.

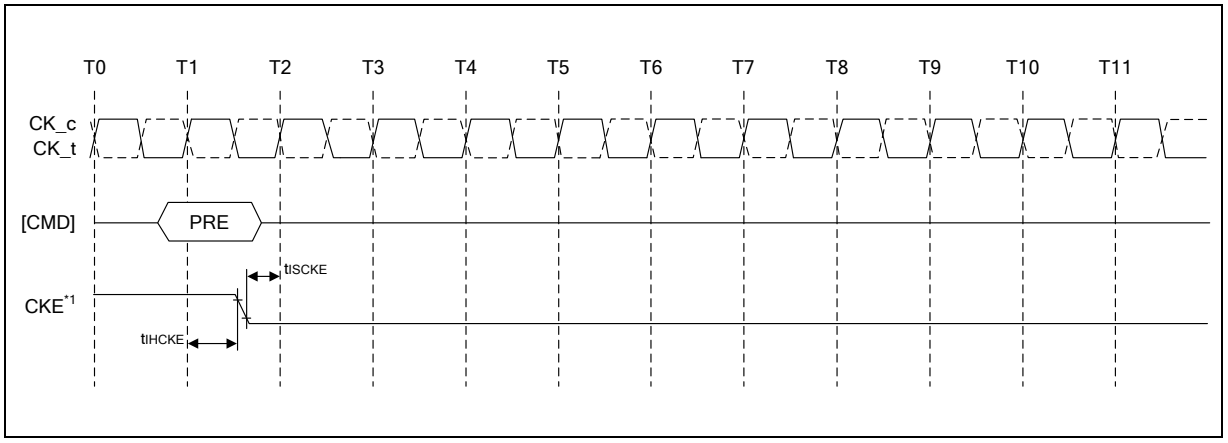



**Figure 59 - Precharge Command to Power-Down Entry**

**Note:**

CKE can go LOW tIHCKE after the clock on which the Precharge command is registered.

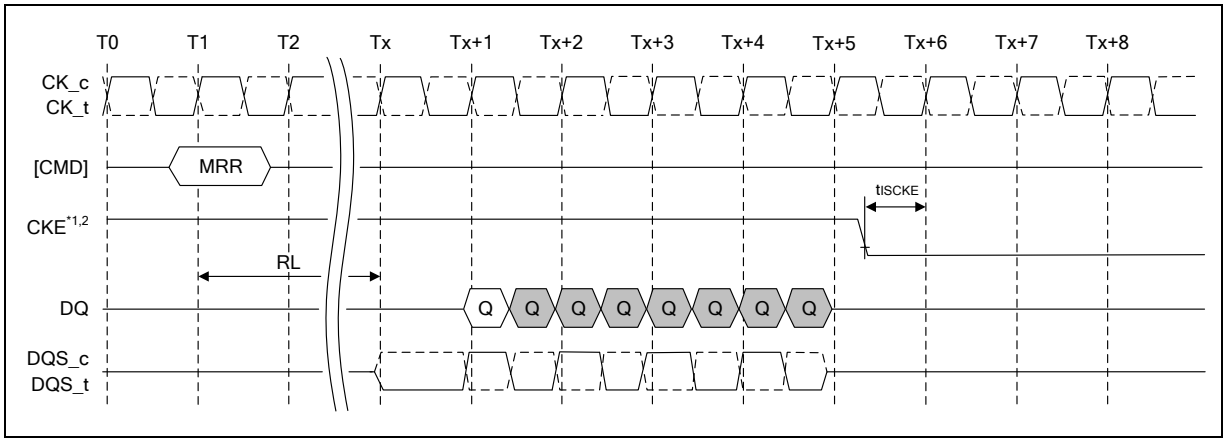



**Figure 60 - MRR to Power-Down Entry**

**Notes:**

1. CKE can be registered LOW RL + RU(tDQSCK/tCK)+ BL/2 + 1 clock cycles after the clock on which the MRR command is registered.
2. CKE should be held high until the end of the burst operation.

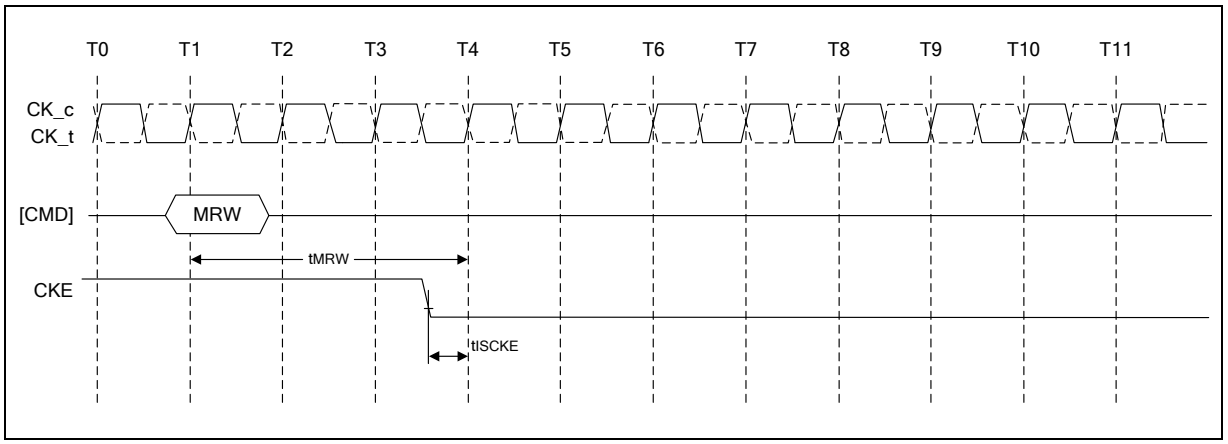



**Figure 61 - MRW to Power-Down Entry**

**Note:**

CKE can be registered LOW tMRW after the clock on which the MRW command is registered.

### 7.4.16 Deep Power-Down

Deep Power-Down is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW. The contents of the SDRAM will be lost upon entry into Deep Power-Down mode.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, and this timing period is defined as tCPDED.

CKE LOW will result in deactivation of command and address receivers after tCPDED has expired. All power supplies must be within specified limits prior to exiting Deep Power-Down. VREFDQ and VREFCA may be at any level within minimum and maximum levels (See **"Absolute Maximum DC Ratings"**). However prior to exiting Deep Power-Down, VREF must be within specified limits (See **"Recommended DC Operating Conditions"**).

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting tISCKE with a stable clock input. The SDRAM must be fully re-initialized as described in the power up initialization sequence. The SDRAM is ready for normal operation after the initialization sequence is completed. For the description of ODT operation and specifications during DPD entry and exit, see section 7.4.14 **"On-Die Termination"**.

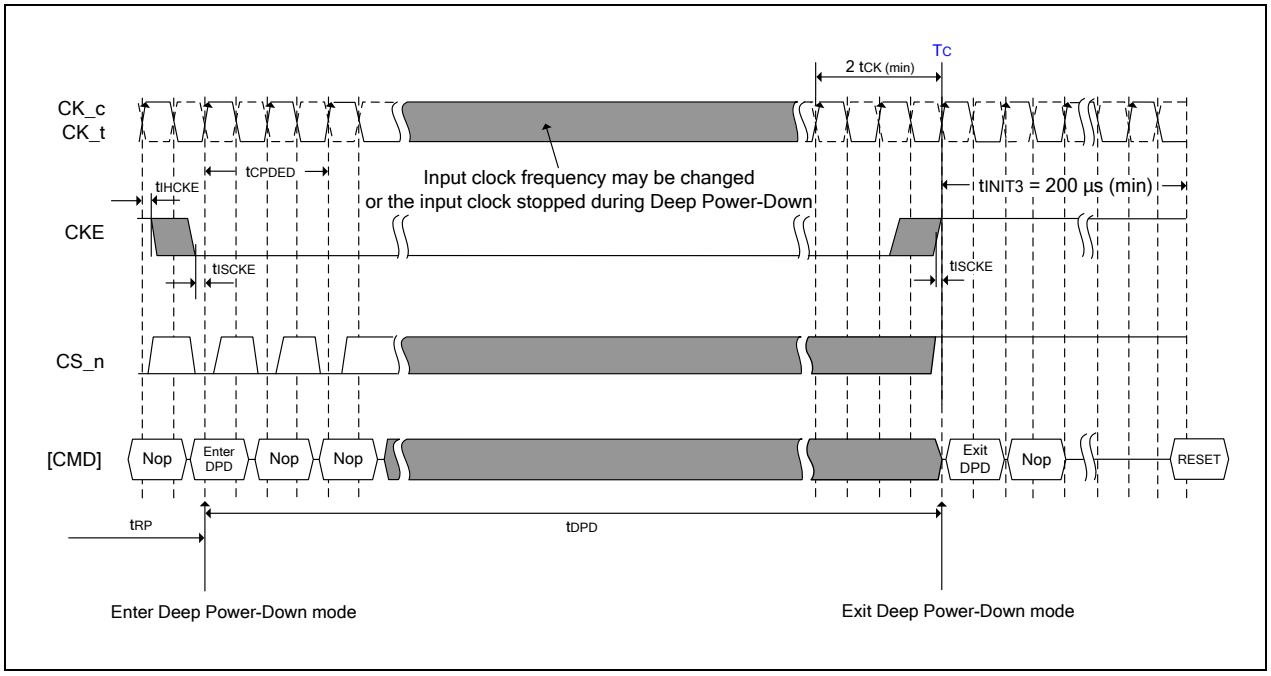



**Figure 62 - Deep power down entry and exit timing diagram**

**Notes:**

1. Initialization sequence may start at any time after Tc.
2. tINIT3, and Tc refer to timings in the LPDDR3 initialization sequence. For more detail, see Power-Up and Initialization.
3. Input clock frequency may be changed or the input clock can be stopped or floated during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

### 7.4.17 Input clock stop and frequency change

LPDDR3 SDRAMs support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(abs)min}$ is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate, or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions ($t_{RCD}$, $t_{RP}$) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE LOW under the following conditions:

- CK_t is held LOW and CK_c is held HIGH or both are floated during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions ($t_{RCD}$, $t_{RP}$) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR3 devices support input clock frequency change during CKE HIGH under the following conditions:

- $t_{CK(abs)min}$ is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions ($t_{RCD}$, $t_{WR}$, $t_{WRA}$, $t_{RP}$, $t_{MRW}$, $t_{MRR}$, etc.) have been met prior to changing the frequency;
- CS_n shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR3 device is ready for normal operation after the clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 x $t_{CK}$ + $t_{XP}$.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- CS_n shall be held HIGH during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions ($t_{RCD}$, $t_{WR}$, $t_{WRA}$, $t_{RP}$, $t_{MRW}$, $t_{MRR}$, etc.) have been met prior to stopping the clock;
- The LPDDR3 device is ready for normal operation after the clock is restarted and satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 x $t_{CK}$ + $t_{XP}$.


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### 7.4.18 No Operation Command

The purpose of the No Operation command (NOP) is to prevent the LPDDR3 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

## 7.5 Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

### 7.5.1 Command Truth Table

| | SDR Command Pins | | | DDR CA Pins (10) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SDRAM Command | CKE | | CS_n | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 | CA8 | CA9 | CK_t EDGE |
| | CK_t(n-1) | CK_t(n) | | | | | | | | | | | | |
| MRW | H | H | L | L | L | L | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | ↑ |
| | | | X | MA6 | MA7 | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | OP6 | OP7 | ↓ |
| MRR | H | H | L | L | L | L | H | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | ↑ |
| | | | X | MA6 | MA7 | X | | | | | | | | ↓ |
| Refresh (per bank) | H | H | L | L | L | H | L | X | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| Refresh (all bank) | H | H | L | L | L | H | H | X | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| Enter Self Refresh | H | L | L | L | L | H | X | | | | | | | ↑ |
| | X | | X | X | | | | | | | | | | ↓ |
| Activate (bank) | H | H | L | L | H | R8 | R9 | R10 | R11 | R12 | BA0 | BA1 | BA2 | ↑ |
| | | | X | R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | X | X | ↓ |
| Write (bank) | H | H | L | H | L | L | RFU | RFU | C1 | C2 | BA0 | BA1 | BA2 | ↑ |
| | | | X | AP*[3] | C3 | C4 | C5 | C6 | C7 | C8 | C9 | X | X | ↓ |
| Read (bank) | H | H | L | H | L | H | RFU | RFU | C1 | C2 | BA0 | BA1 | BA2 | ↑ |
| | | | X | AP*[3] | C3 | C4 | C5 | C6 | C7 | C8 | C9 | X | X | ↓ |
| Precharge[11] (per bank, all bank) | H | H | L | H | H | L | H | AB*[11] | X | X | BA0 | BA1 | BA2 | ↑ |
| | | | X | X | X | X | X | X | X | X | X | X | X | ↓ |
| Enter Deep Power Down | H | L | L | H | H | L | X | | | | | | | ↑ |
| | X | | X | X | | | | | | | | | | ↓ |
| NOP | H | H | L | H | H | H | X | | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| Maintain PD, SREF, DPD (NOP) See note 4 | L | L | L | H | H | H | X | | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| NOP | H | H | H | X | | | | | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| Maintain PD, SREF, DPD See note 4 | L | L | X | X | | | | | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| Enter Power Down | H | L | H | X | | | | | | | | | | ↑ |
| | X | | X | X | | | | | | | | | | ↓ |
| Exit PD, SREF,DPD | L | H | H | X | | | | | | | | | | ↑ |
| | X | | X | X | | | | | | | | | | ↓ |

**Notes:**

1. All LPDDR3 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3. AP "high" during a Read or Write command indicates that an auto-precharge will occur to the bank associated with the Read or Write command.
4. "X" means "H or L (but a defined logic level)", except when the LPDDR3 SDRAM is in PD, SREF, or DPD, in which case CS_n, CK_t/CK_c, and CA can be floated after the required tCPDED time is satisfied, and until the required exit procedure is initiated as described in the respective entry/exit procedure.
5. Self refresh exit and Deep Power Down exit are asynchronous.
6. VREF must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.
7. CAxr refers to command/address bit "x" on the rising edge of clock.
8. CAxf refers to command/address bit "x" on the falling edge of clock.
9. CS_n and CKE are sampled at the rising edge of clock.
10. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
11. AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is don't care.
12. When CS_n is HIGH, LPDDR3 CA bus can be floated.

### 7.5.2 CKE Truth Table

| Device Current State*3 | CKEn-1*4 | CKEn*4 | CS_n*5 | Command n*6 | Operation n*6 | Device Next State | Notes |
|---|---|---|---|---|---|---|---|
| Active Power Down | L | L | X | X | Maintain Active Power Down | Active Power Down | |
| | L | H | H | NOP | Exit Active Power Down | Active | 7 |
| Idle Power Down | L | L | X | X | Maintain Idle Power Down | Idle Power Down | |
| | L | H | H | NOP | Exit Idle Power Down | Idle | 7 |
| Resetting Power Down | L | L | X | X | Maintain Resetting Power Down | Resetting Power Down | |
| | L | H | H | NOP | Exit Resetting Power Down | Idle or Resetting | 7, 10 |
| Deep Power Down | L | L | X | X | Maintain Deep Power Down | Deep Power Down | |
| | L | H | H | NOP | Exit Deep Power Down | Power On | 9 |
| Self Refresh | L | L | X | X | Maintain Self Refresh | Self Refresh | |
| | L | H | H | NOP | Exit Self Refresh | Idle | 8 |
| Bank(s) Active | H | L | H | NOP | Enter Active Power Down | Active Power Down | |
| All Banks Idle | H | L | H | NOP | Enter Idle Power Down | Idle Power Dow | 11 |
| | H | L | L | Enter Self Refresh | Enter Self Refresh | Self Refresh | |
| | H | L | L | Deep Power Down | Enter Deep Power Down | Deep Power Down | |
| Resetting | H | L | H | NOP | Enter Resetting Power Down | Resetting Power Down | |
| | H | H | Refer to the Command Truth Table | | | | |

**Notes:**

1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
2. 'X' means 'Don't care'.
3. "Current state" is the state of the LPDDR3 device immediately prior to clock edge n.
4. "CKEn" is the logic state of CKE at clock rising edge n; "CKEn-1" was the state of CKE at the previous clock edge.
5. "CS_n" is the logic state of CS_n at the clock rising edge n;
6. "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
7. Power Down exit time (tXP) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the tXP period.
8. Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the tXSR time.
9. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
10. Upon exiting Resetting Power Down, the device will return to the idle state if tINIT5 has expired.
11. In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to VDDQ.


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### 7.5.3 State Truth Tables

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

**Current State Bank n - Command to Bank n**

| Current State | Command | Operation | Next State | Notes |
|---|---|---|---|---|
| Any | NOP | Continue previous operation | Current State | |
| Idle | Activate | Select and activate row | Active | |
| | Refresh (Per Bank) | Begin to refresh | Refreshing(Per Bank) | 6 |
| | Refresh (All Bank) | Begin to refresh | Refreshing(All Bank) | 7 |
| | MRW | Write value to Mode Register | MR Writing | 7 |
| | MRR | Read value from Mode Register | Idle<br>MR Reading | |
| | Reset | Begin Device Auto-Initialization | Resetting | 8 |
| | Precharge | Deactivate row in bank or banks | Precharging | 9, 14 |
| Row Active | Read | Select column, and start read burst | Reading | 11 |
| | Write | Select column, and start write burst | Writing | 11 |
| | MRR | Read value from Mode Register | Active<br>MR Reading | |
| | Precharge | Deactivate row in bank or banks | Precharging | 9 |
| Reading | Read | Select column, and start new read burst | Reading | 10, 11 |
| | Write | Select column, and start write burst | Writing | 10, 11, 12 |
| Writing | Write | Select column, and start new write burst | Writing | 10, 11 |
| | Read | Select column, and start read burst | Reading | 10, 11, 13 |
| Power On | Reset | Begin Device Auto-Initialization | Resetting | 8 |
| Resetting | MRR | Read value from Mode Register | Resetting MR Reading | |

**Notes:**

1. The table applies when both CKEn-1 and CKEn are HIGH, and after $t_{XSR}$ or $t_{XP}$ has been met if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   Idle: The bank or banks have been precharged, and $t_{RP}$ has been met.
   Active: A row in the bank has been activated, and $t_{RCD}$ has been met. No data bursts / accesses and no register accesses are in progress.
   Reading: A Read burst has been initiated, with Auto Precharge disabled.
   Writing: A Write burst has been initiated, with Auto Precharge disabled.
4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and according to Current State Bank n - Command to Bank m.
   Precharging: starts with the registration of a Precharge command and ends when $t_{RP}$ is met. Once $t_{RP}$ is met, the bank will be in the idle state.
   Row Activating: starts with registration of an Activate command and ends when $t_{RCD}$ is met. Once $t_{RCD}$ is met, the bank will be in the 'Active' state.
   Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when $t_{RP}$ has been met. Once $t_{RP}$ has been met, the bank will be in the idle state.
   Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when $t_{RP}$ has been met. Once $t_{RP}$ is met, the bank will be in the idle state.


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5. The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.

   Refreshing (Per Bank): starts with registration of a Refresh (Per Bank) command and ends when $t_{RFCpb}$ is met. Once $t_{RFCpb}$ is met, the bank will be in an 'idle' state.

   Refreshing (All Bank): starts with registration of a Refresh (All Bank) command and ends when $t_{RFCab}$ is met. Once $t_{RFCab}$ is met, the device will be in an 'all banks idle' state.

   Idle MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the idle state.

   Resetting MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the Resetting state.

   Active MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the Active state.

   MR Writing: starts with the registration of a MRW com**m**and and ends when $t_{MRW}$ has been met. Once $t_{MRW}$ has been met, the bank will be in the idle state.

   Precharging All: starts with the registration of a Precharge-All command and ends when $t_{RP}$ is met. Once $t_{RP}$ is met, the bank will be in the idle state.
6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific reset command is achieved through Mode Register Write command.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
11. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
12. A Write command may be applied after the completion of the Read burst; burst terminates are not permitted.
13. A Read command may be applied after the completion of the Write burst; burst terminates are not permitted.
14. If a Precharge command is issued to a bank in the idle state, $t_{RP}$ shall still apply.

**Current State Bank n - Command to Bank m**

| Current State of Bank n | Command for Bank m | Operation | Next State for Bank m | Notes |
|---|---|---|---|---|
| Any | NOP | Continue previous operation | Current State of Bank m | |
| Idle | Any | Any command allowed to Bank m | - | 18 |
| Row Activating, Active, or Precharging | Activate | Select and activate row in Bank m | Active | 6 |
| | Read | Select column, and start read burst from Bank m | Reading | 7 |
| | Write | Select column, and start write burst to Bank m | Writing | 7 |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| | MRR | Read value from Mode Register | Idle MR Reading or Active MR Reading | 9, 10, 12 |
| Reading (Autoprecharge disabled) | Read | Select column, and start read burst from Bank m | Reading | 7 |
| | Write | Select column, and start write burst to Bank m | Writing | 7, 13 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Writing (Autoprecharge disabled) | Read | Select column, and start read burst from Bank m | Reading | 7, 15 |
| | Write | Select column, and start write burst to Bank m | Writing | 7 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Reading with Autoprecharge | Read | Select column, and start read burst from Bank m | Reading | 7, 14 |
| | Write | Select column, and start write burst to Bank m | Writing | 7, 13, 14 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Writing with Autoprecharge | Read | Select column, and start read burst from Bank m | Reading | 7, 14, 15 |
| | Write | Select column, and start write burst to Bank m | Writing | 7, 14 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Power On | Reset | Begin Device Auto-Initialization | Resetting | 11, 16 |
| Resetting | MRR | Read value from Mode Register | Resetting MR Reading | |

**Notes:**

1. The table applies when both CKEn-1 and CKEn are HIGH, and after $t_{XSR}$ or $t_{XP}$ has been met if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   Idle: the bank has been precharged, and $t_{RP}$ has been met.
   Active: a row in the bank has been activated, and $t_{RCD}$ has been met. No data bursts/accesses and no register accesses are in progress.
   Reading: a Read burst has been initiated, with Auto Precharge disabled.
   Writing: a Write burst has been initiated, with Auto Precharge disabled.


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4. Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

   Idle MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the idle state.

   Resetting MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the Resetting state.

   Active MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the Active state.

   MR Writing: starts with the registration of a MRW command and ends when $t_{MRW}$ has been met. Once $t_{MRW}$ has been met, the bank will be in the idle state.
6. $t_{RRD}$ must be met between Activate command to Bank n and a subsequent Activate command to Bank m. Additionally, in the case of multiple banks activated, $t_{FAW}$ must be satisfied.
7. Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9. MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when $t_{RCD}$ is met).
10. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when $t_{RP}$ is met.
11. Not bank-specific; requires that all banks are idle and no bursts are in progress.
12. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon $t_{RCD}$ and $t_{RP}$ respectively.
13. A Write command may be applied after the completion of the Read burst, burst terminates are not permitted.
14. Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions described in the precharge and auto-precharge clarification table are followed.
15. A Read command may be applied after the completion of the Write burst; burst terminates are not permitted.
16. Reset command is achieved through Mode Register Write command.

### 7.5.4 Data Mask Truth Table

| Name (Functional) | DM | DQs | Note |
|---|---|---|---|
| Write enable | L | Valid | 1 |
| Write inhibit | H | X | 1 |

**Note:**

1. Used to mask write data, provided coincident with the corresponding data.


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# 8. ELECTRICAL CHARACTERISTIC

## 8.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{DD1}$ supply voltage relative to $V_{SS}$ | $V_{DD1}$ | -0.4 | +2.3 | V | 1 |
| $V_{DD2}$ supply voltage relative to $V_{SS}$ | $V_{DD2}$ | -0.4 | +1.6 | V | 1 |
| $V_{DDCA}$ supply voltage relative to $V_{SS}$ | $V_{DDCA}$ | -0.4 | +1.6 | V | 1, 2 |
| $V_{DDQ}$ supply voltage relative to $V_{SS}$ | $V_{DDQ}$ | -0.4 | +1.6 | V | 1, 3 |
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -0.4 | +1.6 | V | |
| Storage Temperature | $T_{STG}$ | -55 | +125 | °C | 4 |

**Notes:**

1. See "Voltage Ramp" in section 7.2.1 **"Voltage Ramp and Device Initialization"** for relationships between power supplies.
2. $V_{REFCA} \leq 0.6 \times V_{DDCA}$; however, $V_{REFCA}$ may be ≥ $V_{DDCA}$ provided that $V_{REFCA} \leq 300mV$.
3. $V_{REFDQ} \leq 0.7 \times V_{DDQ}$; however, $V_{REFDQ}$ may be ≥ $V_{DDQ}$ provided that $V_{REFDQ} \leq 300mV$.
4. Storage Temperature is the case surface temperature on the center/top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.

## 8.2 AC & DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

### 8.2.1 Recommended DC Operating Conditions

#### 8.2.1.1 Recommended DC Operating Conditions

| Symbol | Voltage | | | DRAM | Unit |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| $V_{DD1}$ | 1.70 | 1.80 | 1.95 | Core Power1 | V |
| $V_{DD2}$ | 1.14 | 1.20 | 1.30 | Core Power2 | V |
| $V_{DDCA}$ | 1.14 | 1.20 | 1.30 | Input Buffer Power | V |
| $V_{DDQ}$ | 1.14 | 1.20 | 1.30 | I/O Buffer Power | V |

**Notes:**

1. $V_{DD1}$ uses significantly less power than $V_{DD2}$.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1MHz at the DRAM pin.
3. All parts list in order information table (section 3) will not guarantee to meet functional and AC specification if the DC operation conditions out of range mentioned in above table.


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### 8.2.2 Input Leakage Current

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input Leakage current | IL | -2 | 2 | µA | 1, 2 |
| VREF supply leakage current | IVREF | -1 | 1 | µA | 3, 4 |

**Notes:**

1. For CA, CKE, CS_n, CK_t, CK_c. Any input 0V ≤ $V_{IN}$ ≤ $V_{DDCA}$. (All other pins not under test = 0V)
2. Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.
3. The minimum limit requirement is for testing purposes. The leakage current on $V_{REFCA}$ and $V_{REFDQ}$ pins should be minimal.
4. $V_{REFDQ}$ = $V_{DDQ}$/2 or $V_{REFCA}$ = $V_{DDCA}$/2. (All other pins not under test = 0V)

### 8.2.3 Operating Temperature Range

| Parameter/Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Standard | $T_{OPER}$ | -40 | 85 | °C |
| Extended | | 85 | 105 | °C |

**Notes:**

1. Operating Temperature is the case surface temperature on the center-top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.
2. Some applications require operation of LPDDR3 in the maximum temperature conditions in the Extended Temperature Range between 85°C and 105°C. For LPDDR3 devices, some derating is necessary to operate in this range. See **MR4_Device Temperature (MA[7:0] = 04H)** table.
3. Either the device operating temperature or the temperature sensor (See section 7.4.12.1 **"Temperature Sensor**") may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the $T_{OPER}$ rating that applies for the Standard or Extended Temperature Ranges. For example, $T_{CASE}$ may be above 85ºC when the temperature sensor indicates a temperature of less than 85°C.
4. All parts list in order information table (section 3) will not guarantee to meet functional and AC specification if operating temperature out of the range in order information table.

### 8.2.4 AC and DC Input Measurement Levels

#### 8.2.4.1 AC and DC Logic Input Levels for Single-Ended Signals

##### 8.2.4.1.1 Single-Ended AC and DC Input Levels for CA and CS_n Inputs

| Symbol | Parameter | 1600 | | 1866/2133 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $V_{IHCA}$(AC) | AC input logic high | VREF + 0.150 | Note 2 | VREF + 0.135 | Note 2 | V | 1, 2 |
| $V_{ILCA}$(AC) | AC input logic low | Note 2 | Vref - 0.150 | Note 2 | VREF - 0.135 | V | 1, 2 |
| $V_{IHCA}$(DC) | DC input logic high | VREF + 0.100 | VDDCA | VREF + 0.100 | VDDCA | V | 1 |
| $V_{ILCA}$(DC) | DC input logic low | VSS | VREF - 0.100 | VSS | VREF - 0.100 | V | 1 |
| $V_{REFCA}$(DC) | Reference Voltage for CA and CS_n inputs | 0.49 * VDDCA | 0.51 * VDDCA | 0.49 * VDDCA | 0.51 * VDDCA | V | 3, 4 |

**Notes:**

1. For CA and CS_n input only pins. $V_{REF}$ = $V_{REFCA(DC)}$.
2. See section 8.2.5.5 **"Overshoot and Undershoot Specifications"**.
3. The ac peak noise on $V_{REFCA}$ may not allow $V_{REFCA}$ to deviate from $V_{REFCA(DC)}$ by more than ± 1% $V_{DDCA}$ (for reference: approx. ± 12 mV).
4. For reference: approx. $V_{DDCA}$/2 ± 12 mV.


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#### 8.2.4.1.2 Single-Ended AC and DC Input Levels for CKE

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $V_{IHCKE}$ | CKE Input High Level | 0.65 * VDDCA | Note 1 | V | 1 |
| $V_{ILCKE}$ | CKE Input Low Level | Note 1 | 0.35 * VDDCA | V | 1 |

**Note 1:** See section 8.2.5.5 **"Overshoot and Undershoot Specifications"**.

#### 8.2.4.1.3 Single-Ended AC and DC Input Levels for DQ and DM

| Symbol | Parameter | 1600 | | 1866/2133 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| VIHDQ(AC) | AC input logic high | VREF + 0.150 | Note 2 | VREF + 0.135 | Note 2 | V | 1, 2, 5 |
| VILDQ(AC) | AC input logic low | Note 2 | VREF - 0.150 | Note 2 | VREF - 0.135 | V | 1, 2, 5 |
| VIHDQ(DC) | DC input logic high | VREF + 0.100 | VDDQ | VREF + 0.100 | VDDQ | V | 1 |
| VILDQ(DC) | DC input logic low | VSSQ | VREF - 0.100 | VSSQ | VREF - 0.100 | V | 1 |
| VREFDQ(DC) (DQ ODT disabled) | Reference Voltage for DQ, DM inputs | 0.49 * VDDQ | 0.51 * VDDQ | 0.49 * VDDQ | 0.51 * VDDQ | V | 3, 4 |
| VREFDQ(DC) (DQ ODT enabled) | Reference Voltage for DQ, DM inputs | VODTR/2 - 0.01 * VDDQ | VODTR/2 + 0.01 * VDDQ | VODTR/2 - 0.01 * VDDQ | VODTR/2 + 0.01 * VDDQ | V | 3, 5, 6 |

**Notes:**

1. For DQ input only pads. VREF = VREFDQ(DC).
2. See section 8.2.5.5 **"Overshoot and Undershoot Specifications"**.
3. The ac peak noise on VREFDQ may not allow VREFDQ to deviate from VREFDQ(DC) by more than ± 1% VDDQ (for reference: approx. ±12 mV).
4. For reference: approx. VDDQ/2 ± 12 mV.
5. For reference: approx. VODTR/2 ± 12 mV.
6. The nominal mode register programmed value for RODT and the nominal controller output impedance RON are used for the calculation of VODTR. For testing purposes a controller RON value of 50 Ω is used.

   $V_{ODTR} = [(2 R_{ON} + R_{TT}) / (R_{ON} + R_{TT})] \times V_{DDQ}$

### 8.2.4.2 VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are illustrated in below figure. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise). VDD stands for VDDCA for VREFCA and VDDQ for VREFDQ. VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDDCA also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in 8.2.4.1.1 **"Single-Ended AC and DC Input Levels for CA and CS_n Inputs"** table. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than ± 1% VDD. VREF(t) cannot track noise on VDDQ or VDDCA if this would send VREF outside these specifications.


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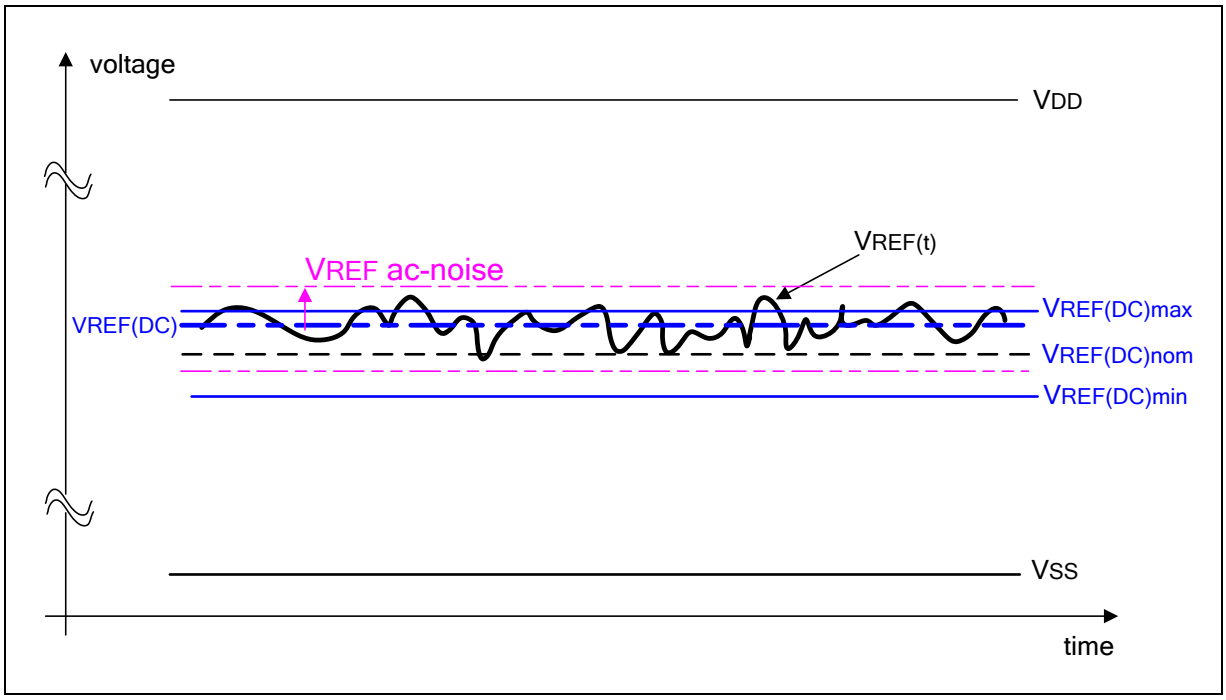



**Figure 63 – Illustration of VREF(DC) tolerance and VREF ac-noise limits**

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF. "VREF" shall be understood as VREF(DC), as defined in above figure.

This clarifies that dc-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of input signals.

This also clarifies that the LPDDR3 setup/hold specification and derating values need to include time and voltage associated with VREF ac-noise. Timing and voltage effects due to ac-noise on VREF up to the specified limit (± 1% of VDD) are included in LPDDR3 timings and their associated deratings.

### 8.2.4.3 Input Signal

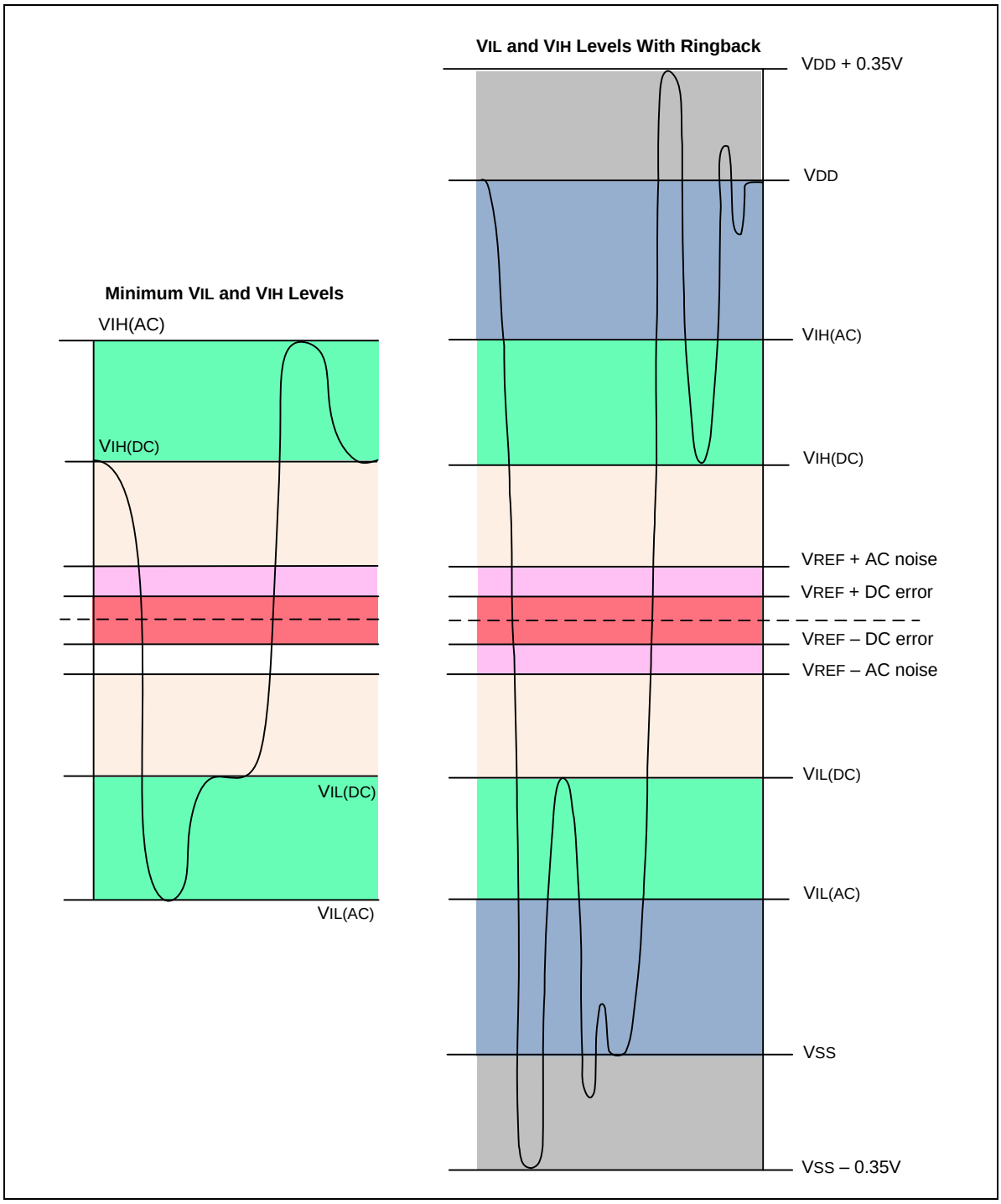



**Figure 64 – LPDDR3 Input Signal**

**Notes:**

1. Numbers reflect nominal values.
2. For CA0-9, CK_t, CK_c, and CS_n, VDD stands for VDDCA. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.

#### 8.2.4.4 AC and DC Logic Input Levels for Differential Signals

##### 8.2.4.4.1 Differential Signal Definition

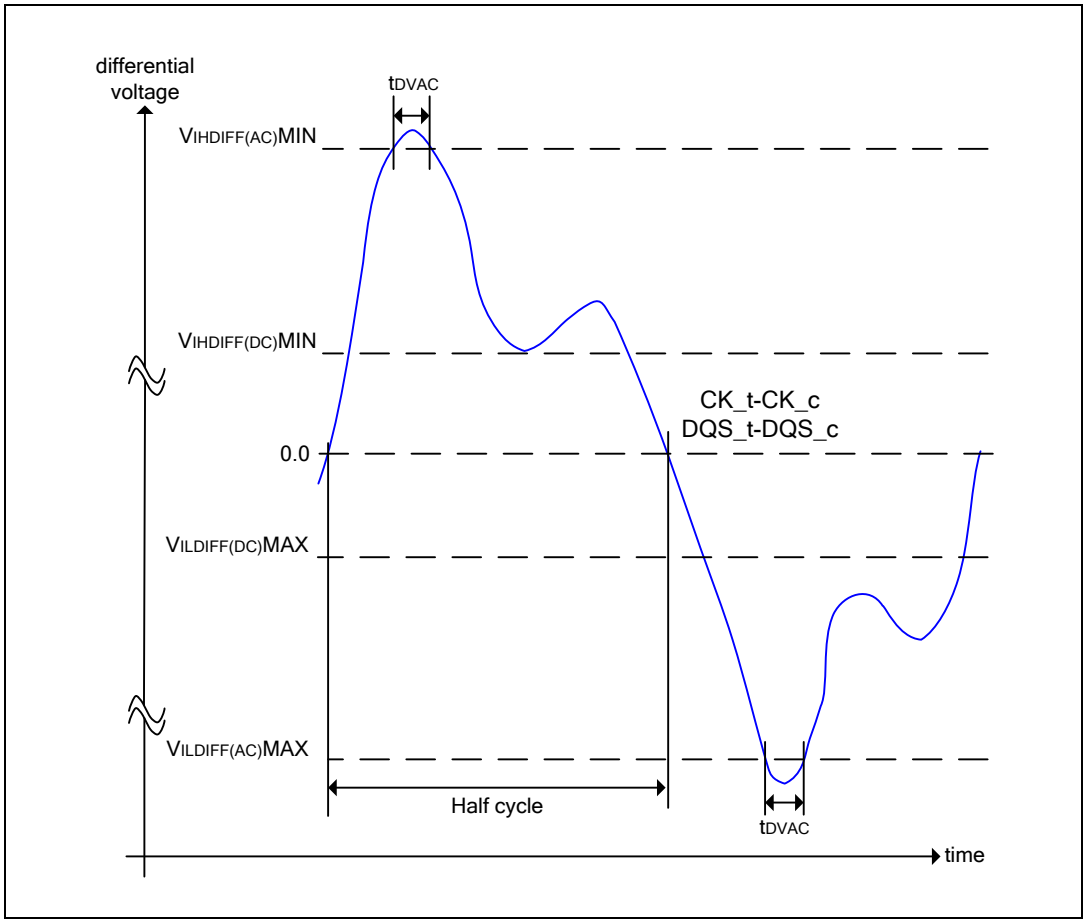



**Figure 65 – Definition of Differential ac-swing and "time above ac-level" tDVAC**

##### 8.2.4.4.2 Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c)

**Differential AC and DC Input Levels**

| Symbol | Parameter | Value | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| VIHdiff(dc) | Differential input high | 2 x (VIH(dc) - VREF) | Note 3 | V | 1 |
| VILdiff(dc) | Differential input logic low | Note 3 | 2 x (VIL(dc) - VREF) | V | 1 |
| VIHdiff(ac) | Differential input high ac | 2 x (VIH(ac) - VREF) | Note 3 | V | 2 |
| VILdiff(ac) | Differential input low ac | Note 3 | 2 x (VIL(ac) - VREF) | V | 2 |

**Notes:**

1. Used to define a differential signal slew-rate. For CK_t - CK_c use VIH/VIL(dc) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(dc) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
2. For CK_t - CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.2.5.5 **"Overshoot and Undershoot Specifications"**.
4. For CK_t and CK_c, VREF = VREFCA(DC). For DQS_t and DQS_c, VREF = VREFDQ(DC).

**Allowed time before ringback $t_{DVAC}$ for CK_t/CK_c and DQS_t/DQS_c**

| Slew Rate [V/nS] | $t_{DVAC}$ [pS] @ $\|V_{IH/Ldiff(ac)}\|$ = 300mV 1600Mbps | | $t_{DVAC}$ [pS] @ $\|V_{IH/Ldiff(ac)}\|$ = 270mV 1866Mbps | | $t_{DVAC}$ [pS] @ $\|V_{IH/Ldiff(ac)}\|$ = 270mV 2133Mbps | |
|---|---|---|---|---|---|---|
| | min | max | min | max | min | max |
| > 8.0 | 48 | - | 40 | - | 34 | - |
| 8.0 | 48 | - | 40 | - | 34 | - |
| 7.0 | 46 | - | 39 | - | 33 | - |
| 6.0 | 43 | - | 36 | - | 30 | - |
| 5.0 | 40 | - | 33 | - | 27 | - |
| 4.0 | 35 | - | 29 | - | 23 | - |
| 3.0 | 27 | - | 21 | - | 15 | - |
| < 3.0 | 27 | - | 21 | - | 15 | - |

#### 8.2.4.5 Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c shall meet $V_{SEH(ac)min}$ / $V_{SEL(ac)max}$ in every half-cycle.

DQS_t, DQS_c shall meet $V_{SEH(ac)min}$ / $V_{SEL(ac)max}$ in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

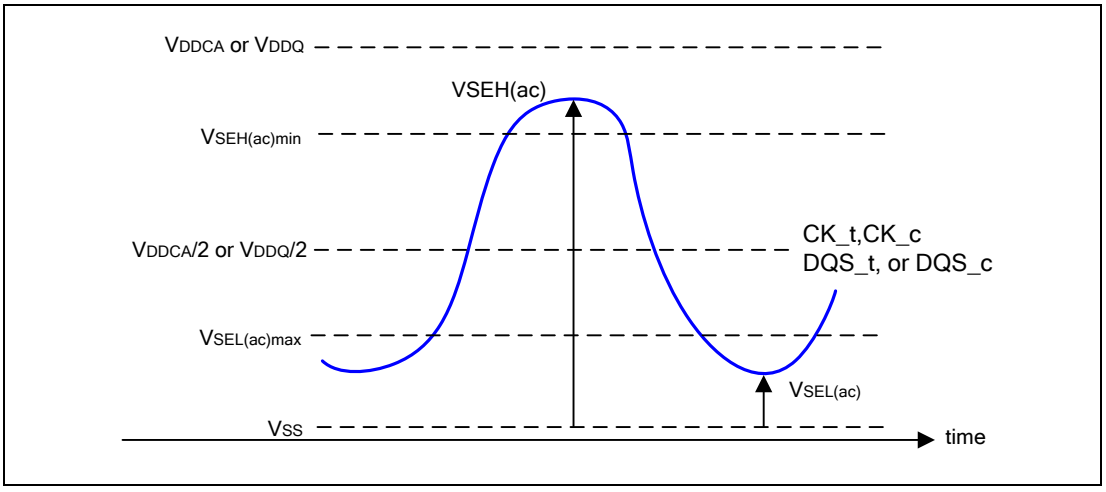



**Figure 66 – Single-Ended Requirement for Differential Signals**

Note that while CA and DQ signal requirements are with respect to $V_{REF}$, the single-ended components of differential signals have a requirement with respect to $V_{DDQ}/2$ for DQS_t, DQS_c and $V_{DDCA}/2$ for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL(ac)max}$, $V_{SEH(ac)min}$ has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.


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The signal ended requirements for CK_t, CK_c, DQS_t and DQS_c are found in 8.2.4.1.1 **"Single-Ended AC and DC Input Levels for CA and CS_n Inputs"** table and 8.2.4.1.3 **"Single-Ended AC and DC Input Levels for DQ and DM"** table, respectively.

**Table of Single-ended levels for CK_t, DQS_t, CK_c, DQS_c**

| Symbol | Parameter | Value | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{SEH(AC150)}$ | Single-ended high-level for strobes | ($V_{DDQ}$/2) + 0.150 | Note 3 | V | 1, 2 |
| | Single-ended high-level for CK_t, CK_c | ($V_{DDCA}$/2) + 0.150 | Note 3 | V | 1, 2 |
| $V_{SEL(AC150)}$ | Single-ended low-level for strobes | Note 3 | ($V_{DDQ}$/2) - 0.150 | V | 1, 2 |
| | Single-ended low-level for CK_t, CK_c | Note 3 | ($V_{DDCA}$/2) - 0.150 | V | 1, 2 |
| $V_{SEH(AC135)}$ | Single-ended high-level for strobes | ($V_{DDQ}$/2) + 0.135 | Note 3 | V | 1, 2 |
| | Single-ended high-level for CK_t, CK_c | ($V_{DDCA}$/2) + 0.135 | Note 3 | V | 1, 2 |
| $V_{SEL(AC135)}$ | Single-ended low-level for strobes | Note 3 | ($V_{DDQ}$/2) - 0.135 | V | 1, 2 |
| | Single-ended low-level for CK_t, CK_c | Note 3 | ($V_{DDCA}$/2) - 0.135 | V | 1, 2 |

**Notes:**

1. For CK_t, CK_c use $V_{SEH}$/$V_{SEL}$(ac) of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}$/$V_{IL}$(ac) of DQs.
2. $V_{IH}$(ac)/$V_{IL}$(ac) for DQs is based on $V_{REFDQ}$; $V_{SEH}$(ac)/$V_{SEL}$(ac) for CA is based on $V_{REFCA}$; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH}$(dc) max, $V_{IL}$(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.2.5.5 **"Overshoot and Undershoot Specifications"**.

### 8.2.4.6 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements of above Single-ended levels for CK_t, DQS_t, CK_c, DQS_c table. The differential input cross point voltage $V_{IX}$ is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

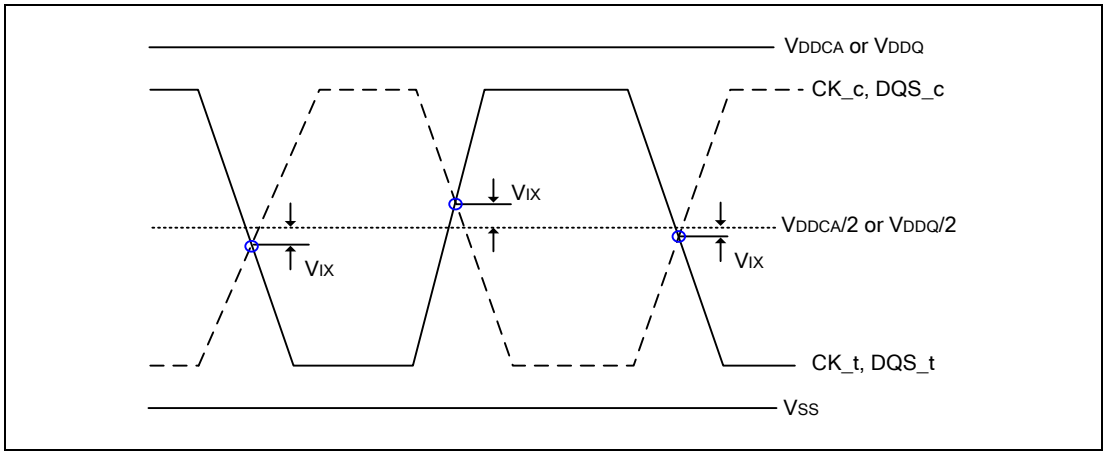



**Figure 67 – $V_{IX}$ Definition**


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**Table of Cross point voltage for differential input signals (CK, DQS)**

| Symbol | Parameter | Value | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IXCA}$ | Differential Input Cross Point Voltage relative to $V_{DDCA}/2$ for CK_t, CK_c | - 120 | 120 | mV | 1, 2 |
| $V_{IXDQ}$ | Differential Input Cross Point Voltage relative to $V_{DDQ}/2$ for DQS_t, DQS_c | - 120 | 120 | mV | 1, 2 |

**Notes:**

1. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × $V_{DD}$ of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in $V_{DD}$. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
2. For CK_t and CK_c, $V_{REF}$ = $V_{REFCA(DC)}$. For DQS_t and DQS_c, $V_{REF}$ = $V_{REFDQ(DC)}$.

### 8.2.4.7 Slew Rate Definitions for Single-Ended Input Signals

See section 8.8.2 **"CA and CS_n Setup, Hold and Derating"** for single-ended slew rate definitions for address and command signals.

See section 8.8.3 **"Data Setup, Hold and Slew Rate Derating"** for single-ended slew rate definitions for data signals.

### 8.2.4.8 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in below table and figure.

**Table of Differential Input Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | from | to | |
| Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c). | $V_{ILdiffmax}$ | $V_{IHdiffmin}$ | [$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTRdiff |
| Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c). | $V_{IHdiffmin}$ | $V_{ILdiffmax}$ | [$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTFdiff |
| **Note:** The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds. | | | |

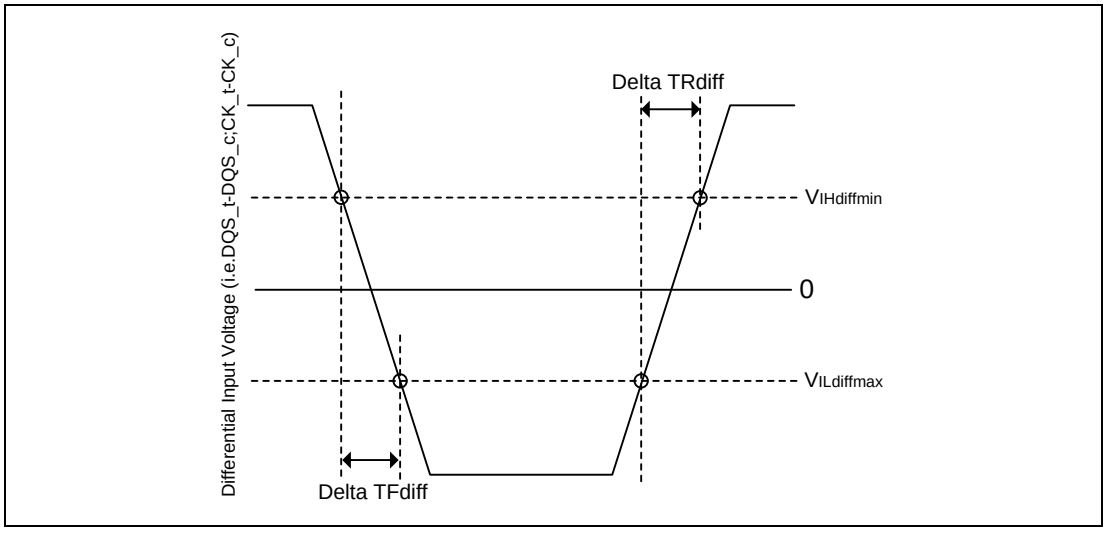



**Figure 68 – Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t, CK_c**


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### 8.2.5 AC and DC Output Measurement Levels

#### 8.2.5.1 Single Ended AC and DC Output Levels

**Table of Single-Ended AC and DC Output Levels**

| Symbol | Parameter | Value | | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH(DC)}$ | DC output high measurement level (for IV curve linearity) | 0.9 x $V_{DDQ}$ | | V | 1 |
| $V_{OL(DC)}$ ODT disabled | DC output low measurement level (for IV curve linearity) | 0.1 x $V_{DDQ}$ | | V | 2 |
| $V_{OL(DC)}$ ODT enabled | DC output low measurement level (for IV curve linearity) | $V_{DDQ}$ x [0.1 + 0.9 x ($R_{ON}$ / ($R_{TT}$ + $R_{ON}$))] | | V | 3 |
| $V_{OH(AC)}$ | AC output high measurement level (for output slew rate) | $V_{REFDQ}$ + 0.12 | | V | |
| $V_{OL(AC)}$ | AC output low measurement level (for output slew rate) | $V_{REFDQ}$ - 0.12 | | V | |
| IOZ | Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled;0V ≤ Vout ≤ VDDQ) | Min | -5 | µA | |
| | | Max | +5 | | |
| $MM_{PUPD}$ | Delta $R_{ON}$ between pull-up and pull-down for DQ/DM | Min | -15 | % | |
| | | Max | +15 | | |

**Notes:**

1. $I_{OH}$ = -0.1mA.
2. $I_{OL}$ = +0.1mA.
3. The min value is derived when using $R_{TT}$, min and $R_{ON,max}$ (±30% uncalibrated, ±15% calibrated).

#### 8.2.5.2 Differential AC and DC Output Levels

**Table of Differential AC and DC Output Levels of (DQS_t, DQS_c)**

| Symbol | Parameter | Value | Unit | Notes |
|---|---|---|---|---|
| $V_{OHdiff(AC)}$ | AC differential output high measurement level (for output SR) | + 0.20 x VDDQ | V | 1 |
| $V_{OLdiff(AC)}$ | AC differential output low measurement level (for output SR) | - 0.20 x VDDQ | V | 2 |

**Notes:**

1. $I_{OH}$ = -0.1mA.
2. $I_{OL}$ = +0.1mA.

#### 8.2.5.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in below table and figure.

**Table of Single-Ended Output Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | from | to | |
| Single-ended output slew rate for rising edge | $V_{OL(AC)}$ | $V_{OH(AC)}$ | [$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTRse |
| Single-ended output slew rate for falling edge | $V_{OH(AC)}$ | $V_{OL(AC)}$ | [$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTFse |
| **Note:** Output slew rate is verified by design and characterization, and may not be subject to production test. | | | |


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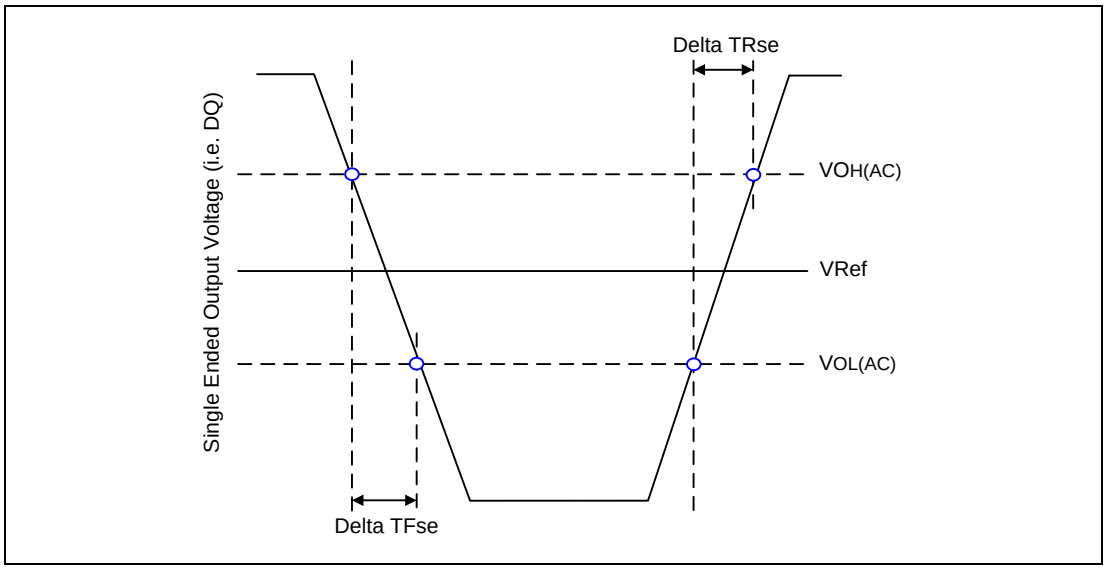



**Figure 69 – Single Ended Output Slew Rate Definition**

**Table of Output Slew Rate (Single-Ended)**

| Parameter | Symbol | Value | | Units |
|---|---|---|---|---|
| | | Min*1 | Max*2 | |
| Single-ended Output Slew Rate ($R_{ON}$ = 40Ω ± 30%) | SRQse | 1.5 | 4.0 | V/nS |
| Output slew-rate matching Ratio (Pull-up to Pull-down) | | 0.7 | 1.4 | |

**Description:**

**SR:** Slew Rate

**Q:** Query Output (like in DQ, which stands for Data-in, Query-Output)

**se:** Single-ended Signals

**Notes:**

1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
4. Slew rates are measured under normal SSO conditions, with 50% of DQ signals per data byte switching.


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### 8.2.5.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in below table and figure.

**Table of Differential Output Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | from | to | |
| Differential output slew rate for rising edge | VOLdiff(AC) | VOHdiff(AC) | [VOHdiff(AC) - VOLdiff(AC)] / DeltaTRdiff |
| Differential output slew rate for falling edge | VOHdiff(AC) | VOLdiff(AC) | [VOHdiff(AC) - VOLdiff(AC)] / DeltaTFdiff |
| **Note:** Output slew rate is verified by design and characterization, and may not be subject to production test. | | | |

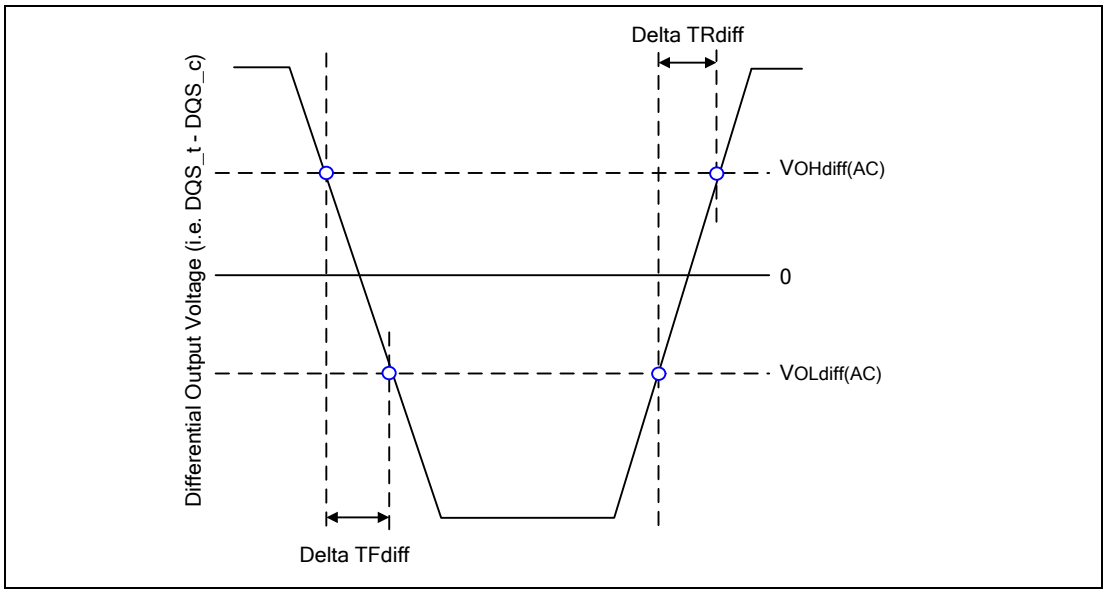



**Figure 70 – Differential Output Slew Rate Definition**

**Table of Differential Output Slew Rate**

| Parameter | Symbol | Value | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| Differential Output Slew Rate (RON = 40Ω ± 30%) | SRQdiff | 3.0 | 8.0 | V/nS |

**Description:**

**SR:** Slew Rate

**Q:** Query Output (like in DQ, which stands for Data-in, Query-Output)

**diff:** Differential Signals

**Notes:**

1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC).
3. Slew rates are measured under normal SSO conditions, with 50% of DQ signals per data byte switching.


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### 8.2.5.5 Overshoot and Undershoot Specifications

**Table of AC Overshoot/Undershoot Specification**

| Parameter | | 1600 | 1866 | 2133 | Unit |
|---|---|---|---|---|---|
| Maximum peak amplitude allowed for overshoot area. (See figure below) | Max | 0.35 | | | V |
| Maximum peak amplitude allowed for undershoot area. (See figure below) | Max | 0.35 | | | V |
| Maximum area above VDD. (See figure below) | Max | 0.10 | | | V-nS |
| Maximum area below VSS. (See figure below) | Max | 0.10 | | | V-nS |

**Notes:**
1. VDD stands for VDDCA for CA[9:0], CK_t, CK_c, CS_n and CKE. VDD stands for VDDQ for DQ, DM, ODT, DQS_t and DQS_c.
2. Maximum peak amplitude values are referenced from actual VDD and VSS values.
3. Maximum area values are referenced from maximum operating VDD and VSS values.

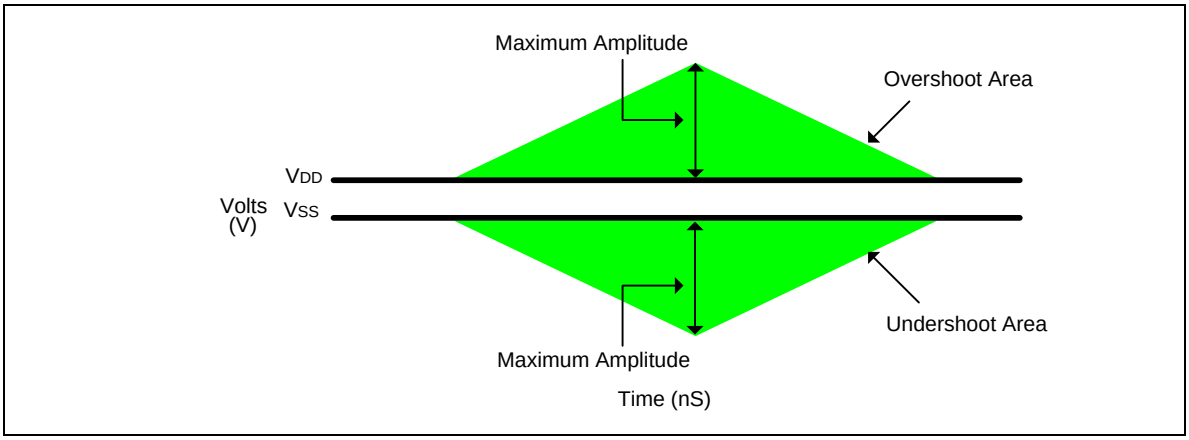



**Figure 71 – Overshoot and Undershoot Definition**

**Notes:**
1. *V*DD stands for *V*DDCA for CA[9:0], CK_t, CK_c, CS_n, and CKE. *V*DD stands for *V*DDQ for DQ, DM, ODT, DQS_t, and DQS_c.
2. Absolute maximum requirements apply.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.


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### 8.2.6 Output buffer characteristics

#### 8.2.6.1 HSUL_12 Driver Output Timing Reference Load

The timing reference loads are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

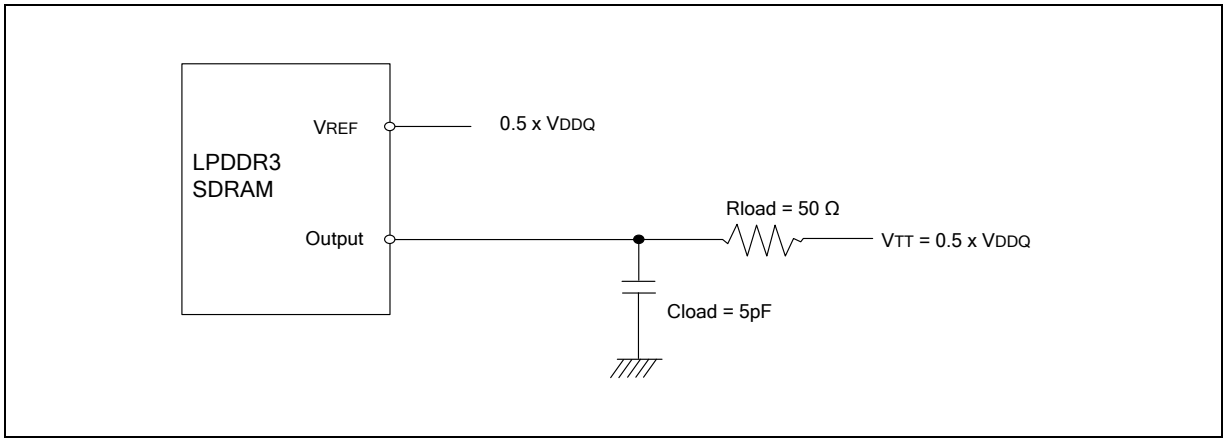



**Figure 72 – HSUL_12 Driver Output Reference Load for Timing and Slew Rate**

**Note:**

All output timing parameter values (like tDQSCK, tDQSQ, tQHS, tHZ, tRPRE etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

#### 8.2.6.2 $R_{ONPU}$ and $R_{ONPD}$ Resistor Definition

$$R_{ONPU} = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

Note: This is under the condition that $R_{ONPD}$ is turned off

$$R_{ONPD} = \frac{Vout}{ABS(Iout)}$$

Note: This is under the condition that $R_{ONPU}$ is turned off

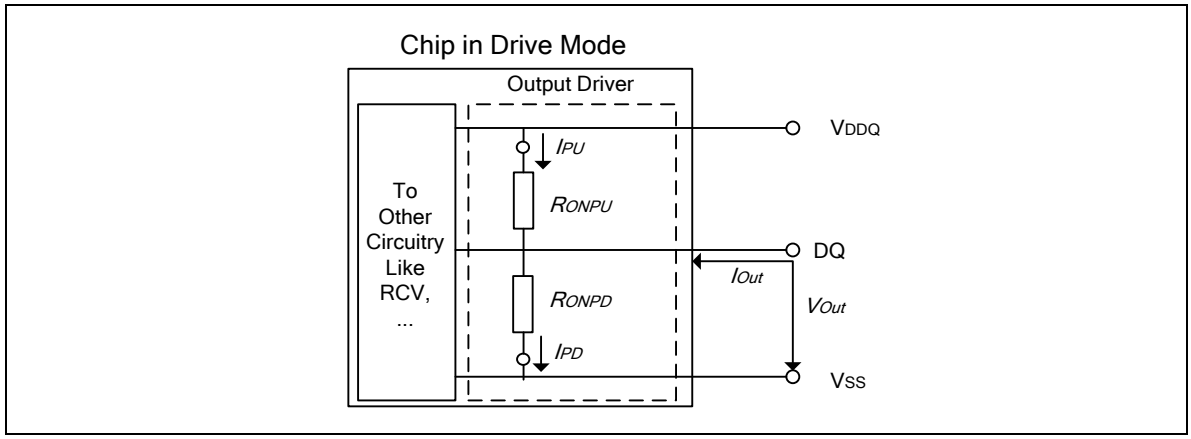



**Figure 73 – Output Driver Definition of Voltages and Currents**


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### 8.2.6.3 $R_{ONPU}$ and $R_{ONPD}$ Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

**Table of Output Driver DC Electrical Characteristics with ZQ Calibration**

| $R_{ON,NOM}$ | Resistor | Vout | Min | Nom | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 34.3Ω | $R_{ON34PD}$ | 0.5 x $V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}$/7 | 1, 2, 3, 4 |
| | $R_{ON34PU}$ | 0.5 x $V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}$/7 | 1, 2, 3, 4 |
| 40.0Ω | $R_{ON40PD}$ | 0.5 x $V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}$/6 | 1, 2, 3, 4 |
| | $R_{ON40PU}$ | 0.5 x $V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}$/6 | 1, 2, 3, 4 |
| 48.0Ω | $R_{ON48PD}$ | 0.5 x $V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}$/5 | 1, 2, 3, 4 |
| | $R_{ON48PU}$ | 0.5 x $V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}$/5 | 1, 2, 3, 4 |
| 60.0Ω | $R_{ON60PD}$ | 0.5 x $V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}$/4 | 1, 2, 3, 4 |
| | $R_{ON60PU}$ | 0.5 x $V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}$/4 | 1, 2, 3, 4 |
| 80.0Ω | $R_{ON80PD}$ | 0.5 x $V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}$/3 | 1, 2, 3, 4 |
| | $R_{ON80PU}$ | 0.5 x $V_{DDQ}$ | 0.85 | 1.00 | 1.15 | $R_{ZQ}$/3 | 1, 2, 3, 4 |
| Mismatch between pull-up and pull-down | $MM_{PUPD}$ | | -15.00 | | +15.00 | % | 1, 2, 3, 4, 5 |

**Notes:**

1. Across entire operating temperature range, after calibration.
2. RZQ = 240Ω.
3. The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.
5. Measurement definition for mismatch between pull-up and pull-down: MMPUPD: Measure $R_{ONPU}$ and $R_{ONPD}$, both at 0.5 x VDDQ:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ONNOM}} \times 100$$

For example, with $MM_{PUPD(max)}$ = 15% and $R_{ONPD}$ = 0.85, $R_{ONPU}$ must be less than 1.0.

6. Output driver strength measured without ODT.

### 8.2.6.4 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the tables shown below.

**Table of Output Driver Sensitivity Definition**

| Resistor | Vout | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $R_{ONPD}$ | 0.5 x VDDQ | 85 – (dRONdT × \|ΔT\| ) – (dRONdV × \|ΔV\| ) | 115 + (dRONdT × \| ΔT\| ) + (dRONdV × \|ΔV\|) | % | 1, 2 |
| $R_{ONPU}$ | | | | | |
| $R_{TT}$ | 0.5 x VDDQ | 85 – (dRTTdT × \|ΔT\| ) – (dRTTdV × \|ΔV\| ) | 115 + (dRTTdT × \| ΔT\| ) + (dRTTdV × \|ΔV\|) | % | 1, 2 |

**Notes:**

1. ΔT = T – T (@calibration), ΔV = V – V(@ calibration).
2. $dR_{ON}dT$ and $dR_{ON}dV$, $dR_{TT}dV$ and $dR_{TT}dT$ are not subject to production test but are verified by design and characterization.

**Table of Output Driver Temperature and Voltage Sensitivity**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $dR_{ON}dT$ | $R_{ON}$ Temperature Sensitivity | 0.00 | 0.75 | % / °C |
| $dR_{ON}dV$ | $R_{ON}$ Voltage Sensitivity | 0.00 | 0.20 | % / mV |
| $dR_{TT}dT$ | $R_{TT}$ Temperature Sensitivity | 0.00 | 0.75 | % / °C |
| $dR_{TT}dV$ | $R_{TT}$ Voltage Sensitivity | 0.00 | 0.20 | % / mV |


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#### 8.2.6.5 $R_{ONPU}$ and $R_{ONPD}$ Characteristics without ZQ Calibration

Output driver impedance $R_{ON}$ is defined by design and characterization as default setting.

**Table of Output Driver DC Electrical Characteristics without ZQ Calibration**

| $R_{ON,NOM}$ | Resistor | Vout | Min | Nom | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 34.3Ω | $R_{ON34PD}$ | 0.5 x $V_{DDQ}$ | 24 | 34.3 | 44.6 | Ω | 1 |
| | $R_{ON34PU}$ | 0.5 x $V_{DDQ}$ | 24 | 34.3 | 44.6 | Ω | 1 |
| 40.0Ω | $R_{ON40PD}$ | 0.5 x $V_{DDQ}$ | 28 | 40 | 52 | Ω | 1 |
| | $R_{ON40PU}$ | 0.5 x $V_{DDQ}$ | 28 | 40 | 52 | Ω | 1 |
| 48.0Ω | $R_{ON48PD}$ | 0.5 x $V_{DDQ}$ | 33.6 | 48 | 62.4 | Ω | 1 |
| | $R_{ON48PU}$ | 0.5 x $V_{DDQ}$ | 33.6 | 48 | 62.4 | Ω | 1 |
| 60.0Ω | $R_{ON60PD}$ | 0.5 x $V_{DDQ}$ | 42 | 60 | 78 | Ω | 1 |
| | $R_{ON60PU}$ | 0.5 x $V_{DDQ}$ | 42 | 60 | 78 | Ω | 1 |
| 80.0Ω | $R_{ON80PD}$ | 0.5 x $V_{DDQ}$ | 56 | 80 | 104 | Ω | 1 |
| | $R_{ON80PU}$ | 0.5 x $V_{DDQ}$ | 56 | 80 | 104 | Ω | 1 |

**Note 1:** Across entire operating temperature range, without calibration.


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### 8.2.6.6 $R_{ZQ}$ I-V Curve

**Table of $R_{ZQ}$ I-V Curve**

| Voltage[V] | $R_{ON}$ = 240Ω ($R_{ZQ}$) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Pull-Down | | | | Pull-Up | | | |
| | Current [mA] / $R_{ON}$ [Ohms] | | | | Current [mA] / $R_{ON}$ [Ohms] | | | |
| | default value after ZQReset | | With Calibration | | default value after ZQReset | | With Calibration | |
| | Min | Max | Min | Max | Min | Max | Min | Max |
| | [mA] | [mA] | [mA] | [mA] | [mA] | [mA] | [mA] | [mA] |
| 0.00 | 0.00 | 0.00 | n/a | n/a | 0.00 | 0.00 | n/a | n/a |
| 0.05 | 0.17 | 0.35 | n/a | n/a | -0.17 | -0.35 | n/a | n/a |
| 0.10 | 0.34 | 0.70 | n/a | n/a | -0.34 | -0.70 | n/a | n/a |
| 0.15 | 0.50 | 1.03 | n/a | n/a | -0.50 | -1.03 | n/a | n/a |
| 0.20 | 0.67 | 1.39 | n/a | n/a | -0.67 | -1.39 | n/a | n/a |
| 0.25 | 0.83 | 1.73 | n/a | n/a | -0.83 | -1.73 | n/a | n/a |
| 0.30 | 0.97 | 2.05 | n/a | n/a | -0.97 | -2.05 | n/a | n/a |
| 0.35 | 1.13 | 2.39 | n/a | n/a | -1.13 | -2.39 | n/a | n/a |
| 0.40 | 1.26 | 2.71 | n/a | n/a | -1.26 | -2.71 | n/a | n/a |
| 0.45 | 1.39 | 3.01 | n/a | n/a | -1.39 | -3.01 | n/a | n/a |
| 0.50 | 1.51 | 3.32 | n/a | n/a | -1.51 | -3.32 | n/a | n/a |
| 0.55 | 1.63 | 3.63 | n/a | n/a | -1.63 | -3.63 | n/a | n/a |
| 0.60 | 1.73 | 3.93 | 2.17 | 2.94 | -1.73 | -3.93 | -2.17 | -2.94 |
| 0.65 | 1.82 | 4.21 | n/a | n/a | -1.82 | -4.21 | n/a | n/a |
| 0.70 | 1.90 | 4.49 | n/a | n/a | -1.90 | -4.49 | n/a | n/a |
| 0.75 | 1.97 | 4.74 | n/a | n/a | -1.97 | -4.74 | n/a | n/a |
| 0.80 | 2.03 | 4.99 | n/a | n/a | -2.03 | -4.99 | n/a | n/a |
| 0.85 | 2.07 | 5.21 | n/a | n/a | -2.07 | -5.21 | n/a | n/a |
| 0.90 | 2.11 | 5.41 | n/a | n/a | -2.11 | -5.41 | n/a | n/a |
| 0.95 | 2.13 | 5.59 | n/a | n/a | -2.13 | -5.59 | n/a | n/a |
| 1.00 | 2.17 | 5.72 | n/a | n/a | -2.17 | -5.72 | n/a | n/a |
| 1.05 | 2.19 | 5.84 | n/a | n/a | -2.19 | -5.84 | n/a | n/a |
| 1.10 | 2.21 | 5.95 | n/a | n/a | -2.21 | -5.95 | n/a | n/a |
| 1.15 | 2.23 | 6.03 | n/a | n/a | -2.23 | -6.03 | n/a | n/a |
| 1.20 | 2.25 | 6.11 | n/a | n/a | -2.25 | -6.11 | n/a | n/a |

**Note:** The I-V curve of $R_{ZQ}$ is not tested.


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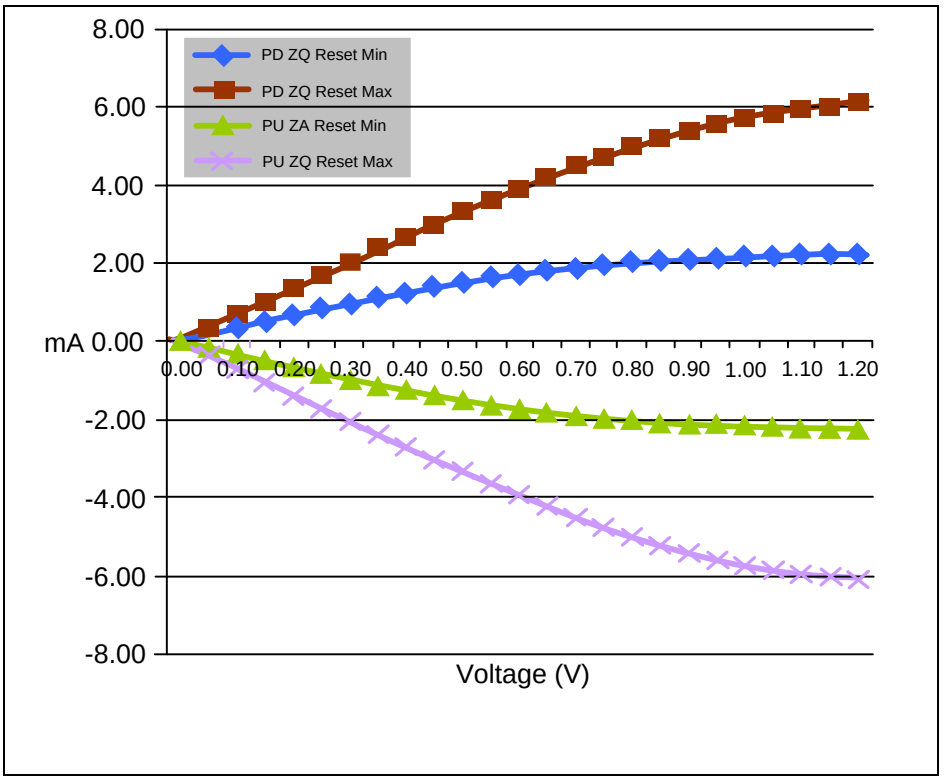



**Figure 74 – I-V Curve after ZQ Reset**

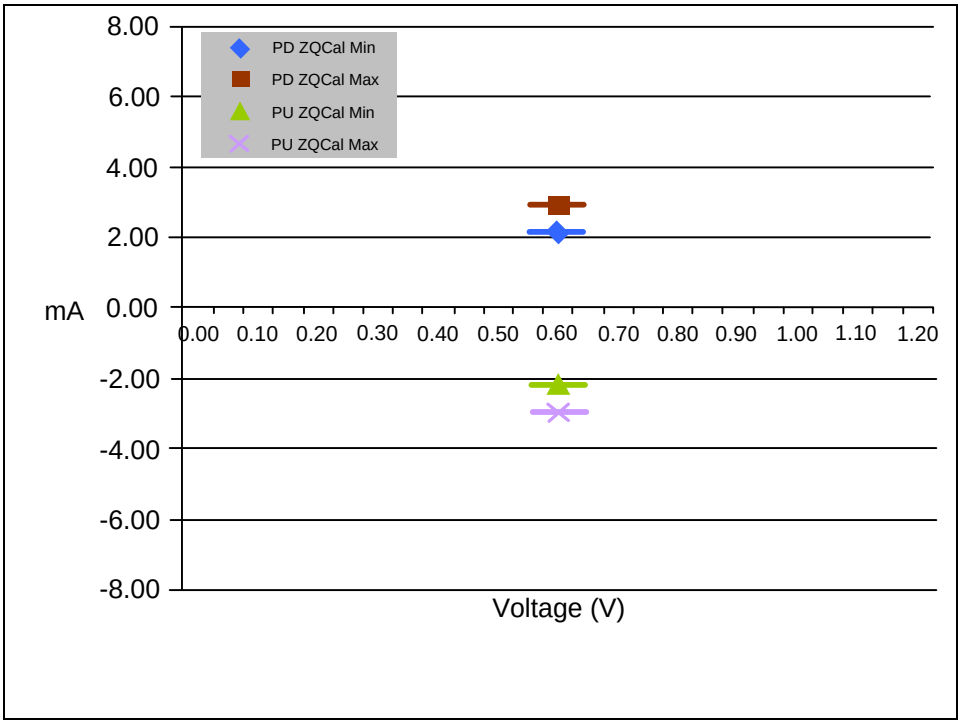



**Figure 75 – I-V Curve after Calibration**

### 8.2.6.7 ODT Levels and I-V Characteristics

On-Die Termination effective resistance, $R_{TT}$, is defined by mode register MR11[1:0]. ODT is applied to the DQ, DM, and DQS_t/DQS_c pins. A functional representation of the on-die termination is shown in the figure below.

$R_{TT}$ is defined by the following formula:

$R_{TTPU} = (V_{DDQ} - V_{Out}) / | I_{Out} |$

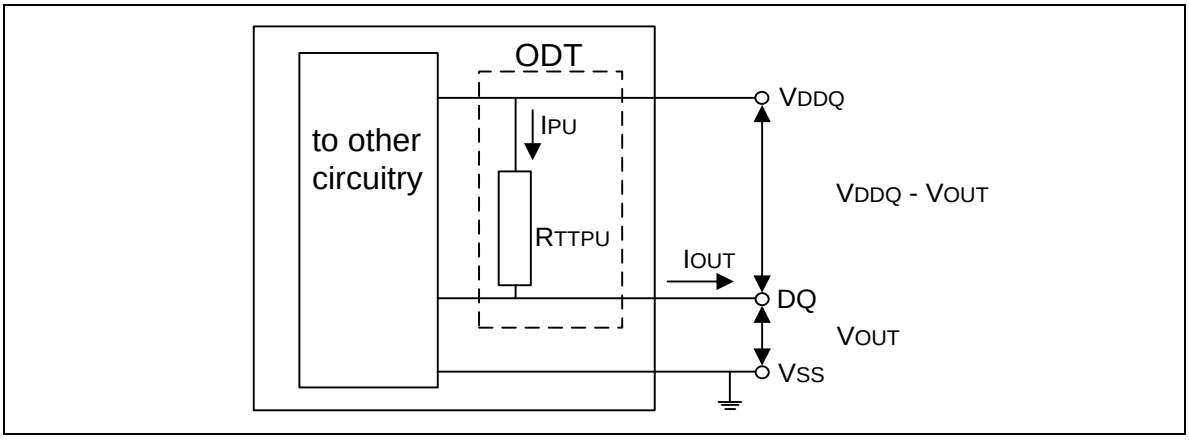



**Figure 76 –Functional representation of On-Die Termination**

**Table of ODT DC Electrical Characteristics, assuming $R_{ZQ}$ = 240 ohm after proper ZQ calibration**

| $R_{TT}$ (ohm) | $V_{OUT}$ (V) | $I_{OUT}$ | |
|---|---|---|---|
| | | Min(mA) | Max(mA) |
| $R_{ZQ}/1$ | 0.6 | -2.17 | -2.94 |
| $R_{ZQ}/2$ | 0.6 | -4.34 | -5.88 |
| $R_{ZQ}/4$ | 0.6 | -8.68 | -11.76 |


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## 8.3 Input/Output Capacitance

**Table of Input/Output Capacitance**

| Parameter | Symbol | Min | Max | Units | Note |
|---|---|---|---|---|---|
| Input capacitance, CK_t and CK_c | $C_{CK}$ | 0.5 | 1.2 | pF | 1, 2 |
| Input capacitance delta, CK_t and CK_c | $C_{DCK}$ | 0 | 0.15 | pF | 1, 2, 3 |
| Input capacitance, all other input-only pins | $C_I$ | 0.5 | 1.1 | pF | 1, 2, 4 |
| Input capacitance delta, all other input-only pins | $C_{DI}$ | -0.2 | 0.2 | pF | 1, 2, 5 |
| Input/output capacitance, DQ, DM, DQS_t, DQS_c | $C_{IO}$ | 1.0 | 1.8 | pF | 1, 2, 6, 7 |
| Input/output capacitance delta, DQS_t, DQS_c | $C_{DDQS}$ | 0 | 0.2 | pF | 1, 2, 7, 8 |
| Input/output capacitance delta, DQ, DM | $C_{DIO}$ | -0.25 | 0.25 | pF | 1, 2, 7, 9 |
| Input/output capacitance, ZQ Pin | $C_{ZQ}$ | 0 | 2.0 | pF | 1, 2 |

**Notes:**

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with $V_{DD1}$, $V_{DD2}$, $V_{DDQ}$, $V_{SS}$ applied and all other pins floating.
3. Absolute value of $C_{CK_t} - C_{CK_c}$.
4. CI applies to CS_n, CKE, CA0-CA9, ODT
5. $C_{DI} = C_I - 0.5 * (C_{CK_t} + C_{CK_c})$.
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP3-OP0 = 0001b (34.3 Ω typical).
8. Absolute value of $C_{DQS_t}$ and $C_{DQS_c}$.
9. $C_{DIO} = C_{IO} - 0.5 * (C_{DQS_t} + C_{DQS_c})$ in byte lane.


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## 8.4 IDD Specification Parameters and Test Conditions

### 8.4.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW: $V_{IN} \leq V_{IL(DC)}$ MAX
HIGH: $V_{IN} \geq V_{IH(DC)}$ MIN
STABLE: Inputs are stable at a HIGH or LOW level
SWITCHING: See tables below.

**Table of Definition of Switching for CA Input Signals**

| Switching for CA | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | CK_t (RISING) / CK_c (FALLING) | CK_t (FALLING) / CK_c (RISING) | CK_t (RISING) / CK_c (FALLING) | CK_t (FALLING) / CK_c (RISING) | CK_t (RISING) / CK_c (FALLING) | CK_t (FALLING) / CK_c (RISING) | CK_t (RISING) / CK_c (FALLING) | CK_t (FALLING) / CK_c (RISING) |
| Cycle | N | | N+1 | | N+2 | | N+3 | |
| CS_n | HIGH | | HIGH | | HIGH | | HIGH | |
| CA0 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA1 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA2 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA3 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA4 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA5 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA6 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA7 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA8 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA9 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |

**Notes:**

1. CS_n must always be driven HIGH.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.


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**Table of Definition of Switching for $I_{DD4R}$**

| Clock | CKE | CS_n | Clock Cycle Number | Command | CA0-CA2 | CA3-CA9 | All DQ |
|---|---|---|---|---|---|---|---|
| Rising | HIGH | LOW | N | Read_Rising | HLH | LHLHLHL | L |
| Falling | HIGH | LOW | N | Read_Falling | LLL | LLLLLLL | L |
| Rising | HIGH | HIGH | N + 1 | NOP | LLL | LLLLLLL | H |
| Falling | HIGH | HIGH | N + 1 | NOP | LLL | LLLLLLL | L |
| Rising | HIGH | HIGH | N + 2 | NOP | LLL | LLLLLLL | H |
| Falling | HIGH | HIGH | N + 2 | NOP | LLL | LLLLLLL | H |
| Rising | HIGH | HIGH | N + 3 | NOP | LLL | LLLLLLL | H |
| Falling | HIGH | HIGH | N + 3 | NOP | HLH | HLHLLHL | L |
| Rising | HIGH | LOW | N + 4 | Read_Rising | HLH | HLHLLHL | H |
| Falling | HIGH | LOW | N + 4 | Read_Falling | LHH | HHHHHHH | H |
| Rising | HIGH | HIGH | N + 5 | NOP | HHH | HHHHHHH | H |
| Falling | HIGH | HIGH | N + 5 | NOP | HHH | HHHHHHH | L |
| Rising | HIGH | HIGH | N + 6 | NOP | HHH | HHHHHHH | L |
| Falling | HIGH | HIGH | N + 6 | NOP | HHH | HHHHHHH | L |
| Rising | HIGH | HIGH | N + 7 | NOP | HHH | HHHHHHH | H |
| Falling | HIGH | HIGH | N + 7 | NOP | HLH | LHLHLHL | L |

**Notes:**

1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. The above pattern (N, N+1...) is used continuously during $I_{DD}$ measurement for $I_{DD4R}$.

**Table of Definition of Switching for $I_{DD4W}$**

| Clock | CKE | CS_n | Clock Cycle Number | Command | CA0-CA2 | CA3-CA9 | All DQ |
|---|---|---|---|---|---|---|---|
| Rising | HIGH | LOW | N | Write_Rising | HLL | LHLHLHL | L |
| Falling | HIGH | LOW | N | Write_Falling | LLL | LLLLLLL | L |
| Rising | HIGH | HIGH | N + 1 | NOP | LLL | LLLLLLL | H |
| Falling | HIGH | HIGH | N + 1 | NOP | LLL | LLLLLLL | L |
| Rising | HIGH | HIGH | N + 2 | NOP | LLL | LLLLLLL | H |
| Falling | HIGH | HIGH | N + 2 | NOP | LLL | LLLLLLL | H |
| Rising | HIGH | HIGH | N + 3 | NOP | LLL | LLLLLLL | H |
| Falling | HIGH | HIGH | N + 3 | NOP | HLL | HLHLLHL | L |
| Rising | HIGH | LOW | N + 4 | Write_Rising | HLL | HLHLLHL | H |
| Falling | HIGH | LOW | N + 4 | Write_Falling | LHH | HHHHHHH | H |
| Rising | HIGH | HIGH | N + 5 | NOP | HHH | HHHHHHH | H |
| Falling | HIGH | HIGH | N + 5 | NOP | HHH | HHHHHHH | L |
| Rising | HIGH | HIGH | N + 6 | NOP | HHH | HHHHHHH | L |
| Falling | HIGH | HIGH | N + 6 | NOP | HHH | HHHHHHH | L |
| Rising | HIGH | HIGH | N + 7 | NOP | HHH | HHHHHHH | H |
| Falling | HIGH | HIGH | N + 7 | NOP | HLL | LHLHLHL | L |

**Notes:**

1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The above pattern (N, N+1...) is used continuously during $I_{DD}$ measurement for $I_{DD4W}$.


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### 8.4.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range.

#### 8.4.2.1 IDD Specification Parameters and Operating Conditions (85°C, x16, x32)

Notes: 1, 2, 3 apply for all values

| Parameter/Condition | Symbol | Power Supply | 800 MHz | 933 MHz | 1066 MHz | Unit | Notes |
|---|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD01 | VDD1 | 7 | 7 | 7 | mA | |
| | IDD02 | VDD2 | 36 | 37 | 39 | mA | |
| | IDD0,in | VDDCA VDDQ | 8 | 8 | 8 | mA | 3 |
| **Idle power-down standby current:** tCK = tCKmin; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD2P1 | VDD1 | 0.3 | 0.3 | 0.3 | mA | |
| | IDD2P2 | VDD2 | 2 | 2 | 2 | mA | |
| | IDD2P,in | VDDCA VDDQ | 50 | 50 | 50 | µA | 3 |
| **Idle power-down standby current with clock stop:** CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled | IDD2PS1 | VDD1 | 0.3 | 0.3 | 0.3 | mA | |
| | IDD2PS2 | VDD2 | 2 | 2 | 2 | mA | |
| | IDD2PS,in | VDDCA VDDQ | 50 | 50 | 50 | µA | 3 |
| **Idle non power-down standby current:** tCK = tCKmin; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD2N1 | VDD1 | 0.9 | 0.9 | 0.9 | mA | |
| | IDD2N2 | VDD2 | 9 | 10 | 11 | mA | |
| | IDD2N,in | VDDCA VDDQ | 8 | 8 | 8 | mA | 3 |
| **Idle non power-down standby current with clock stopped:** CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled | IDD2NS1 | VDD1 | 0.9 | 0.9 | 0.9 | mA | |
| | IDD2NS2 | VDD2 | 4 | 4 | 4 | mA | |
| | IDD2NS,in | VDDCA VDDQ | 8 | 8 | 8 | mA | 3 |
| **Active power-down standby current:** tCK = tCKmin; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD3P1 | VDD1 | 1.1 | 1.1 | 1.1 | mA | |
| | IDD3P2 | VDD2 | 5 | 5 | 5 | mA | |
| | IDD3P,in | VDDCA VDDQ | 50 | 50 | 50 | µA | 3 |


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IDD Specification Parameters and Operating Conditions, (Continued)

| Parameter/Condition | Symbol | Power Supply | 800 MHz | 933 MHz | 1066 MHz | Unit | Notes |
|---|---|---|---|---|---|---|---|
| **Active power-down standby current with clock stop:**<br>CK_t = LOW, CK_c = HIGH;<br>CKE is LOW; CS_n is HIGH;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | $I_{DD3PS1}$ | $V_{DD1}$ | 1.1 | 1.1 | 1.1 | mA | |
| | $I_{DD3PS2}$ | $V_{DD2}$ | 5 | 5 | 5 | mA | |
| | $I_{DD3PS,in}$ | $V_{DDCA}$<br>$V_{DDQ}$ | 50 | 50 | 50 | µA | 4 |
| **Active non power-down standby current:**<br>$t_{CK} = t_{CKmin}$;<br>CKE is HIGH; CS_n is HIGH;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled | $I_{DD3N1}$ | $V_{DD1}$ | 1.3 | 1.3 | 1.3 | mA | |
| | $I_{DD3N2}$ | $V_{DD2}$ | 13 | 14 | 15 | mA | |
| | $I_{DD3N,in}$ | $V_{DDCA}$<br>$V_{DDQ}$ | 8 | 8 | 8 | mA | 4 |
| **Active non power-down standby current with clock stopped:**<br>CK_t = LOW, CK_c = HIGH;<br>CKE is HIGH; CS_n is HIGH;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | $I_{DD3NS1}$ | $V_{DD1}$ | 1.3 | 1.3 | 1.3 | mA | |
| | $I_{DD3NS2}$ | $V_{DD2}$ | 5 | 5 | 5 | mA | |
| | $I_{DD3NS,in}$ | $V_{DDCA}$<br>$V_{DDQ}$ | 8 | 8 | 8 | mA | 4 |
| **Operating burst READ current:**<br>$t_{CK} = t_{CKmin}$;<br>CS_n is HIGH between valid commands;<br>One bank is active;<br>BL = 8; RL = RL (MIN);<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled | $I_{DD4R1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | mA | |
| | $I_{DD4R2}$ | $V_{DD2}$ | 162 | 186 | 210 | mA | |
| | $I_{DD4R,in}$ | $V_{DDCA}$ | 8 | 8 | 8 | mA | |
| **Operating burst WRITE current:**<br>$t_{CK} = t_{CKmin}$;<br>CS_n is HIGH between valid commands;<br>One bank is active;<br>BL = 8; WL = WLmin;<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled | $I_{DD4W1}$ | $V_{DD1}$ | 1.5 | 1.5 | 1.5 | mA | |
| | $I_{DD4W2}$ | $V_{DD2}$ | 163 | 189 | 215 | mA | |
| | $I_{DD4W,in}$ | $V_{DDCA}$<br>$V_{DDQ}$ | 34 | 34 | 34 | mA | 4 |
| **All-bank REFRESH burst current:**<br>$t_{CK} = t_{CKmin}$;<br>CKE is HIGH between valid commands;<br>$t_{RC} = t_{RFCabmin}$;<br>Burst refresh;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled | $I_{DD51}$ | $V_{DD1}$ | 18 | 18 | 18 | mA | |
| | $I_{DD52}$ | $V_{DD2}$ | 60 | 62 | 63 | mA | |
| | $I_{DD5,in}$ | $V_{DDCA}$<br>$V_{DDQ}$ | 8 | 8 | 8 | mA | 4 |


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IDD Specification Parameters and Operating Conditions, (Continued)

| Parameter/Condition | Symbol | Power Supply | 800 MHz | 933 MHz | 1066 MHz | Unit | Notes |
|---|---|---|---|---|---|---|---|
| **All-bank REFRESH average current:** | $I_{DD5AB1}$ | $V_{DD1}$ | 1.22 | 1.22 | 1.22 | mA | |
| $t_{CK} = t_{CKmin}$; | $I_{DD5AB2}$ | $V_{DD2}$ | 10.5 | 11 | 12 | mA | |
| CKE is HIGH between valid commands; $t_{RC} = RM \times t_{REFI}$; CA bus inputs are switching; Data bus inputs are stable ODT disabled | $I_{DD5AB,in}$ | $V_{DDCA}$ $V_{DDQ}$ | 8 | 8 | 8 | mA | 4 |
| **Per-bank REFRESH average current:** | $I_{DD5PB1}$ | $V_{DD1}$ | 1.3 | 1.3 | 1.3 | mA | |
| $t_{CK} = t_{CKmin}$; | $I_{DD5PB2}$ | $V_{DD2}$ | 11 | 11 | 12 | mA | |
| CKE is HIGH between valid commands; $t_{RC} = RM \times t_{REFI}/8$; CA bus inputs are switching; Data bus inputs are stable ODT disabled | $I_{DD5PB,in}$ | $V_{DDCA}$ $V_{DDQ}$ | 8 | 8 | 8 | mA | 4 |
| **Deep power-down current:** | $I_{DD81}$ | $V_{DD1}$ | 50 | 50 | 50 | µA | |
| CK_t = LOW, CK_c = HIGH; | $I_{DD82}$ | $V_{DD2}$ | 50 | 50 | 50 | µA | |
| CKE is LOW; CA bus inputs are stable; Data bus inputs are stable ODT disabled | $I_{DD8,in}$ | $V_{DDCA}$ $V_{DDQ}$ | 50 | 50 | 50 | µA | 4 |

**Notes:**

1. Published $I_{DD}$ values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000b.
3. $I_{DD}$ current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of $V_{DDQ}$ and $V_{DDCA}$.
5. For all $I_{DD}$ measurements, $V_{IHCKE} = 0.8 \times V_{DDCA}$, $V_{ILCKE} = 0.2 \times V_{DDCA}$.


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#### 8.4.2.2 IDD6 Partial Array Self-Refresh Current (x16, x32)

| Parameter | | Symbol | Power Supply | 85 °C | Condition | Unit |
|---|---|---|---|---|---|---|
| IDD6 Partial Array Self-Refresh Current | Full Array | $IDD6_1$ | VDD1 | 600 | **Self refresh current**<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>ODT disabled | µA |
| | | $IDD6_2$ | VDD2 | 3000 | | |
| | | $IDD6_{IN}$ | VDDCA<br>VDDQ | 50 | | |
| | 1/2 Array | $IDD6_1$ | VDD1 | 500 | | µA |
| | | $IDD6_2$ | VDD2 | 2500 | | |
| | | $IDD6_{IN}$ | VDDCA<br>VDDQ | 50 | | |
| | 1/4 Array | $IDD6_1$ | VDD1 | 400 | | µA |
| | | $IDD6_2$ | VDD2 | 2300 | | |
| | | $IDD6_{IN}$ | VDDCA<br>VDDQ | 50 | | |
| | 1/8 Array | $IDD6_1$ | VDD1 | 350 | | µA |
| | | $IDD6_2$ | VDD2 | 2200 | | |
| | | $IDD6_{IN}$ | VDDCA<br>VDDQ | 50 | | |

**Notes:**
1. IDD6 currents are measured using bank-masking only.
2. IDD values published are the maximum of the distribution of the arithmetic mean.

## 8.5 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR3 device.

### 8.5.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left[ \sum_{j=1}^{N} tCK_j \right] / N$$

$$where \qquad N = 200$$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to ± 1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

### 8.5.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.


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### 8.5.3 Definition for $t_{CH(avg)}$ and $t_{CL(avg)}$

$t_{CH(avg)}$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left[\sum_{j=1}^{N} tCH_j\right] / (N \times tCK(avg))$$

$$where \qquad N = 200$$

$t_{CL(avg)}$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left[\sum_{j=1}^{N} tCL_j\right] / (N \times tCK(avg))$$

$$where \qquad N = 200$$

### 8.5.4 Definition for $t_{JIT(per)}$

$t_{JIT(per)}$ is the single period jitter defined as the largest deviation of any signal $t_{CK}$ from $t_{CK(avg)}$.
$t_{JIT(per)}$ = Min/max of {$t_{CKi}$ - $t_{CK(avg)}$ where i = 1 to 200}.
$t_{JIT(per),act}$ is the actual clock jitter for a given system.
$t_{JIT(per),allowed}$ is the specified allowed clock period jitter.
$t_{JIT(per)}$ is not subject to production test.

### 8.5.5 Definition for $t_{JIT(cc)}$

$t_{JIT(cc)}$ is defined as the absolute difference in clock period between two consecutive clock cycles.
$t_{JIT(cc)}$ = Max of |{$t_{CKi+1}$ - $t_{CKi}$}|.
$t_{JIT(cc)}$ defines the cycle to cycle jitter.
$t_{JIT(cc)}$ is not subject to production test.

### 8.5.6 Definition for $t_{ERR(nper)}$

$t_{ERR(nper)}$ is defined as the cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$.
$t_{ERR(nper),act}$ is the actual clock jitter over n cycles for a given system.
$t_{ERR(nper),allowed}$ is the specified allowed clock period jitter over n cycles.
$t_{ERR(nper)}$ is not subject to production test.

$$tERR(nper) = \left[\sum_{j=i}^{i+n-1} tCK_j\right] - n \times tCK(avg)$$

$t_{ERR(nper),min}$ can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

$t_{ERR(nper),max}$ can be calculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations, $t_{ERR(nper)}$ tables can be generated for each $t_{JIT(per),act}$ value.


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### 8.5.7 Definition for Duty Cycle Jitter tJIT(duty)

tJIT(duty) is defined with absolute and average specification of tCH / tCL.

t*JIT(duty),min* = *MIN*((*tCH*(*abs*),*min* – *tCH*(*avg*),*min*),(*tCL*(*abs*),*min* – *tCL*(*avg*),*min*)) x *tCK*(*avg*)

*tJIT*(*duty*),*max* = *MAX*((*tCH*(*abs*),*max* – *tCH*(*avg*),*max*),(*tCL*(*abs*),*max* – *tCL*(*avg*),*max*)) x *tCK*(*avg*)

### 8.5.8 Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

**Table of Definition for tCK(abs), tCH(abs), and tCL(abs)**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| Absolute Clock Period | tCK(abs) | tCK(avg),min + tJIT(per),min | pS |
| Absolute Clock HIGH Pulse Width | tCH(abs) | tCH(avg),min + tJIT(duty),min / tCK(avg)min | tCK(avg) |
| Absolute Clock LOW Pulse Width | tCL(abs) | tCL(avg),min + tJIT(duty),min / tCK(avg)min | tCK(avg) |

**Notes:**

1. tCK(avg),min is expressed is pS for this table.
2. tJIT(duty),min is a negative value.

## 8.6 Period Clock Jitter

LPDDR3 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in section 8.8.1 **"LPDDR3 AC Timing** **"** table and how to determine cycle time de-rating and clock cycle de-rating.

### 8.6.1 Clock period jitter effects on core timing parameters (tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR3 device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

#### 8.6.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in nS) required if the equation results in a positive value for a core timing parameter.

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

#### 8.6.1.2 Clock cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter.

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

### 8.6.2 Clock jitter effects on Command/Address timing parameters (tISCA, tIHCA, tISCS, tIHCS, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

### 8.6.3 Clock jitter effects on Read timing parameters

#### 8.6.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}\right)$$

For example,

if the measured jitter into a LPDDR3-1600 device has tCK(avg) = 1250 pS, tJIT(per),act,min = -92 pS and tJIT(per),act,max = + 134 pS, then

tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (134 - 100)/1250= .8728 tCK(avg)

#### 8.6.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3, m=0–31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per)).

#### 8.6.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min.

These parameters determine absolute Data-Valid Window (DVW) at the LPDDR3 device pin.

Absolute min DVW @ LPDDR3 device pin=

min { ( tQSH(abs)min – tDQSQmax) , ( tQSL(abs)min – tDQSQmax) }

This minimum DVW shall be met at the target frequency regardless of clock jitter.


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#### 8.6.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by $t_{CL(abs)}$. Therefore $t_{RPST(abs)min}$ can be specified by $t_{CL(abs)min}$.

$t_{RPST(abs)min} = t_{CL(abs)min} – 0.05 = t_{QSL(abs)min}$

### 8.6.4 Clock jitter effects on Write timing parameters

#### 8.6.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3, m=0–31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c: n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, as the setup and hold are relative to the clock signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

#### 8.6.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, as the setup and hold of the data strobes are relative to the corresponding clock signal crossing. Regardless of clock jitter values, these values shall be met.

#### 8.6.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter $t_{JIT(per),act}$ of the input clock in excess of the allowed period jitter $t_{JIT(per),allowed}$.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per),act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per),act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,

If the measured jitter into a LPDDR3-1600 device has $t_{CK(avg)}$ = 1250 pS, $t_{JIT(per),act,min}$ = -93 pS and $t_{JIT(per),act,max}$ = + 134 pS, then

$t_{DQSS,(min,derated)} = 0.75 - (t_{JIT(per),act,min} - t_{JIT(per),allowed,min})/t_{CK(avg)} = 0.75 - (-93+ 100)/1250 = .7444\ t_{CK(avg)}$

and

$t_{DQSS,(max,derated)} = 1.25 - (t_{JIT(per),act,max} - t_{JIT(per),allowed,max})/t_{CK(avg)} = 1.25 - (134 - 100)/1250 = 1.2228\ t_{CK(avg)}$


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## 8.7 Refresh Requirements

### 8.7.1 Refresh Requirement Parameters

| Parameter | | Symbol | 1 Gb | Unit |
|---|---|---|---|---|
| Number of Banks | | | 8 | |
| Refresh Window TCASE ≤ 85°C | | tREFW | 32 | mS |
| Refresh Window 1/2-Rate Refresh | | tREFW | 16 | mS |
| Refresh Window 1/4-Rate Refresh | | tREFW | 8 | mS |
| Required number of Refresh commands (min) | | R | 4,096 | |
| Average time between Refresh commands (for reference only) TCASE ≤ 85°C | REFab | tREFI | 7.8 | µS |
| | REFpb | tREFIpb | 0.975 | µS |
| Refresh Cycle time | | tRFCab | 130 | nS |
| Per Bank Refresh Cycle time | | tRFCpb | 60 | nS |

### 8.7.2 LPDDR3 Read and Write Latencies

| Parameter | Value | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Max. Clock Frequency | 400 | 533 | 600 | 667 | 733 | 800 | 933 | 1066 | MHz |
| Max. Data Rate | 800 | 1066 | 1200 | 1333 | 1466 | 1600 | 1866 | 2133 | MT/S |
| Average Clock Period | 2.5 | 1.875 | 1.667 | 1.5 | 1.364 | 1.25 | 1.071 | 0.938 | nS |
| Read Latency | 6 | 8 | 9 | 10 | 11 | 12 | 14 | 16 | tCK(avg) |
| Write Latency (Set A) | 3 | 4 | 5 | 6 | 6 | 6 | 8 | 8 | tCK(avg) |


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## 8.8 AC Timings

### 8.8.1 LPDDR3 AC Timing

(Notes 1, 2 and 3 apply to all parameters)

| Parameter | Symbol | min / max | Data Rate | | | Unit |
|---|---|---|---|---|---|---|
| | | | 1600 | 1866 | 2133 | |
| Max. clock Frequency | fCK | - | 800 | 933 | 1066 | MHz |
| **Clock Timing** | | | | | | |
| Average clock period | tCK(avg) | MIN | 1.25 | 1.071 | 0.938 | nS |
| | | MAX | 100 | | | |
| Average HIGH pulse width | tCH(avg) | MIN | 0.45 | | | tCK(avg) |
| | | MAX | 0.55 | | | |
| Average LOW pulse width | tCL(avg) | MIN | 0.45 | | | tCK(avg) |
| | | MAX | 0.55 | | | |
| Absolute clock period | tCK(abs) | MIN | tCK(avg)min + tJIT(per)min | | | nS |
| Absolute clock HIGH pulse width | tCH(abs), allowed | MIN | 0.43 | | | tCK(avg) |
| | | MAX | 0.57 | | | |
| Absolute clock LOW pulse width | tCL(abs), (allowed) | MIN | 0.43 | | | tCK(avg) |
| | | MAX | 0.57 | | | |
| Clock Period Jitter (with supported jitter) | tJIT(per), (allowed) | MIN | -70 | -60 | -50 | pS |
| | | MAX | 70 | 60 | 50 | |
| Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter) | tJIT(cc), allowed | MAX | 140 | 120 | 100 | pS |
| Duty cycle Jitter (with supported jitter) | tJIT(duty), allowed | MIN | min((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) * tCK(avg) | | | pS |
| | | MAX | max((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) * tCK(avg) | | | pS |
| Cumulative error across 2 cycles | tERR(2per), (allowed) | MIN | -103 | -88 | -74 | pS |
| | | MAX | 103 | 88 | 74 | |
| Cumulative error across 3 cycles | tERR(3per), (allowed) | MIN | -122 | -105 | -87 | pS |
| | | MAX | 122 | 105 | 87 | |
| Cumulative error across 4 cycles | tERR(4per), (allowed) | MIN | -136 | -117 | -97 | pS |
| | | MAX | 136 | 117 | 97 | |
| Cumulative error across 5 cycles | tERR(5per), (allowed) | MIN | -147 | -126 | -105 | pS |
| | | MAX | 147 | 126 | 105 | |
| Cumulative error across 6 cycles | tERR(6per), (allowed) | MIN | -155 | -133 | -111 | pS |
| | | MAX | 155 | 133 | 111 | |
| Cumulative error across 7 cycles | tERR(7per), (allowed) | MIN | -163 | -139 | -116 | pS |
| | | MAX | 163 | 139 | 116 | |
| Cumulative error across 8 cycles | tERR(8per), (allowed) | MIN | -169 | -145 | -121 | pS |
| | | MAX | 169 | 145 | 121 | |
| Cumulative error across 9 cycles | tERR(9per), (allowed) | MIN | -175 | -150 | -125 | pS |
| | | MAX | 175 | 150 | 125 | |
| Cumulative error across 10 cycles | tERR(10per), (allowed) | MIN | -180 | -154 | -128 | pS |
| | | MAX | 180 | 154 | 128 | |
| Cumulative error across 11 cycles | tERR(11per), (allowed) | MIN | -184 | -158 | -132 | pS |
| | | MAX | 184 | 158 | 132 | |
| Cumulative error across 12 cycles | tERR(12per), (allowed) | MIN | -188 | -161 | -134 | pS |
| | | MAX | 188 | 161 | 134 | |
| Cumulative error across n = 13, 14 , 15…, 19, 20 cycles | tERR(nper), (allowed) | MIN | tERR(nper),allowed MIN = (1 + 0.68ln(n)) x tJIT(per),allowed MIN | | | pS |
| | | MAX | tERR(nper),allowed,max = (1 + 0.68ln(n)) x tJIT(per),allowed MAX | | | |


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| | | | | | | |
|---|---|---|---|---|---|---|
| **ZQ Calibration Parameters** | | | | | | |
| Initialization calibration time | tZQINIT | MIN | 1 | | | µS |
| Long calibration time | tZQCL | MIN | 360 | | | nS |
| Short calibration time | tZQCS | MIN | 90 | | | nS |
| Calibration Reset time | tZQRESET | MIN | max(50nS,3nCK) | | | nS |
| **Read Parameters**[*4] | | | | | | |
| DQS output access time from CK_t/CK_c | tDQSCK | MIN | 2500 | | | pS |
| | | MAX | 5500 | | | |
| DQSCK delta short[*5] | tDQSCKDS | MAX | 220 | 190 | 165 | pS |
| DQSCK delta medium[*6] | tDQSCKDM | MAX | 511 | 435 | 380 | pS |
| DQSCK delta long[*7] | tDQSCKDL | MAX | 614 | 525 | 460 | pS |
| DQS-DQ skew | tDQSQ | MAX | 135 | 115 | 100 | pS |
| DQS output High pulse width | tQSH | MIN | tCH(abs) - 0.05 | | | tCK(avg) |
| DQS output Low pulse width | tQSL | MIN | tCL(abs) - 0.05 | | | tCK(avg) |
| DQ/DQS output hold time from DQS | tQH | MIN | min(tQSH, tQSL) | | | tCK(avg) |
| Read preamble[*8,10] | tRPRE | MIN | 0.9 | | | tCK(avg) |
| Read postamble[*8,11] | tRPST | MIN | 0.3 | | | tCK(avg) |
| DQS Low-Z from clock[*8] | tLZ(DQS) | MIN | tDQSCK(MIN) - 300 | | | pS |
| DQ Low-Z from clock[*8] | tLZ(DQ) | MIN | tDQSCK(MIN) - 300 | | | pS |
| DQS High-Z from clock[*8] | tHZ(DQS) | MAX | tDQSCK(MAX) - 100 | | | pS |
| DQ High-Z from clock[*8] | tHZ(DQ) | MAX | tDQSCK(MAX) + (1.4 x tDQSQ(MAX)) | | | pS |
| **Write Parameters**[*4] | | | | | | |
| DQ and DM input hold time (VREF based) | tDH | MIN | 150 | 130 | 115 | pS |
| DQ and DM input setup time (VREF based) | tDS | MIN | 150 | 130 | 115 | pS |
| DQ and DM input pulse width | tDIPW | MIN | 0.35 | | | tCK(avg) |
| Write command to 1st DQS latching transition | tDQSS | MIN | 0.75 | | | tCK(avg) |
| | | MAX | 1.25 | | | |
| DQS input high-level width | tDQSH | MIN | 0.4 | | | tCK(avg) |
| DQS input low-level width | tDQSL | MIN | 0.4 | | | tCK(avg) |
| DQS falling edge to CK setup time | tDSS | MIN | 0.2 | | | tCK(avg) |
| DQS falling edge hold time from CK | tDSH | MIN | 0.2 | | | tCK(avg) |
| Write postamble | tWPST | MIN | 0.4 | | | tCK(avg) |
| Write preamble | tWPRE | MIN | 0.8 | | | tCK(avg) |
| **CKE Input Parameters** | | | | | | |
| CKE minimum. pulse width (HIGH and LOWpulse width) | tCKE | MIN | max(7.5nS,3nCK) | | | nS |
| CKE input setup time | tISCKE[*12] | MIN | 0.25 | | | tCK(avg) |
| CKE input hold time | tIHCKE[*13] | MIN | 0.25 | | | tCK(avg) |
| Command path disable delay | tCPDED | MIN | 2 | | | tCK(avg) |
| **Command Address Input Parameters**[*4] | | | | | | |
| Address and control input setup time | tISCA[*14] | MIN | 150 | 130 | 115 | pS |
| Address and control input hold time | tIHCA[*14] | MIN | 150 | 130 | 115 | pS |
| CS_n input setup time | tISCS[*14] | MIN | 270 | 230 | 205 | pS |
| CS_n input hold time | tIHCS[*14] | MIN | 270 | 230 | 205 | pS |
| Address and control input pulse width | tIPWCA | MIN | 0.35 | | | tCK(avg) |
| CS_n input pulse width | tIPWCS | MIN | 0.7 | | | tCK(avg) |
| **Boot Parameters (10 MHz–55 MHz)**[*15, 16, 17] | | | | | | |
| Clock Cycle Time | tCKb | MAX | 100 | | | nS |
| | | MIN | 18 | | | |
| CKE Input setup time | tISCKEb | MIN | 2.5 | | | nS |
| CKE Input hold time | tIHCKEb | MIN | 2.5 | | | nS |
| Address and control input setup time | tISb | MIN | 1150 | | | pS |

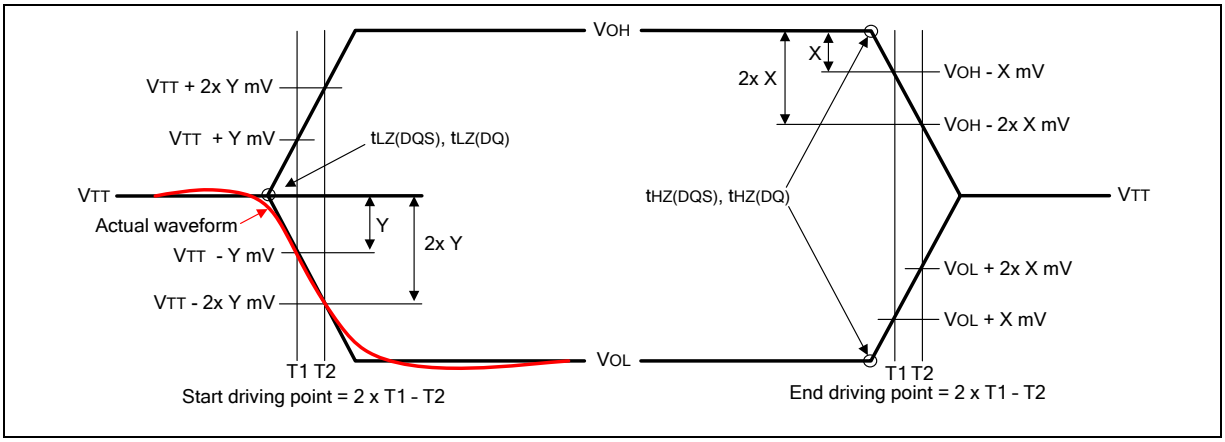

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| | | | | | | |
|---|---|---|---|---|---|---|
| Address and control input hold time | tIHb | MIN | 1150 | | | pS |
| DQS output data access time from CK_t/CK_c | tDQSCKb | MIN | 2.0 | | | nS |
| | | MAX | 10.0 | | | |
| Data strobe edge to output data edge | tDQSQb | MAX | 1.2 | | | nS |
| **Mode Register Parameters** | | | | | | |
| Mode Register Write command period | tMRW | MIN | 10 | | | tCK(avg) |
| Mode Register Read command period | tMRR | MIN | 4 | | | tCK(avg) |
| Additional time after tXP has expired until MRR command may be issued | tMRRI | MIN | tRCD(MIN) | | | nS |
| **Core Parameters*18** | | | | | | |
| Read Latency | RL | MIN | 12 | 14 | 16 | tCK(avg) |
| Write Latency (set A) | WL | MIN | 6 | 8 | 8 | tCK(avg) |
| Activate to Activate command period | tRC | MIN | tRAS + tRPab (with all-bank precharge)<br>tRAS + tRPpb (with per-bank precharge) | | | nS |
| CKE minimum pulse width during Self Refresh (low pulse width during Self Refresh) | tCKESR | MIN | max(15nS,3nCK) | | | nS |
| Self Refresh exit to next valid command delay | tXSR | MIN | max(tRFCab +10nS,2nCK) | | | nS |
| Exit power-down to next valid command delay | tXP | MIN | max(7.5nS,3nCK) | | | nS |
| CAS-to-CAS delay | tCCD | MIN | 4 | | | tCK(avg) |
| Internal Read to Precharge command delay | tRTP | MIN | max(7.5nS,4nCK) | | | nS |
| RAS to CAS Delay | tRCD (typ) | MIN | max(18nS,3nCK) | | | nS |
| Row precharge time (single bank) | tRPpb (typ) | MIN | max(18nS,3nCK) | | | nS |
| Row precharge time (all banks) | tRPab (typ) | MIN | max(21nS,3nCK) | | | nS |
| Row active time | tRAS | MIN | max(42nS,3nCK) | | | nS |
| | | MAX | min(70.2 , 9 x RM x tREFI) | | | µS |
| Write Recovery Time | tWR | MIN | max(15nS,4nCK) | | | nS |
| Internal Write-to-Read command delay | tWTR | MIN | max(7.5nS,4nCK) | | | nS |
| Active bank A to active bank B | tRRD | MIN | max(10nS,2nCK) | | | nS |
| Four-bank Activate Window | tFAW | MIN | max(50nS,8nCK) | | | nS |
| Minimum deep power-down time | tDPD | MIN | 500 | | | µS |
| **ODT Parameters** | | | | | | |
| Asynchronous RTT turn-on delay from ODT input | tODTon | MIN | 1.75 | | | nS |
| | | MAX | 3.5 | | | |
| Asynchronous RTT turn-off delay from ODT input | tODToff | MIN | 1.75 | | | nS |
| | | MAX | 3.5 | | | |
| Automatic RTT turn-on delay after Read data | tAODTon | MAX | tDQSCK + 1.4 × tDQSQ,max + tCK(avg,min) | | | pS |
| Automatic RTT turn-off delay after Read data | tAODToff | MIN | tDQSCK,min - 300 | | | pS |
| RTT disable delay from power down entry | tODTd | MAX | 12 | | | nS |
| RTT disable delay from self-refresh, and deep power down entry | tODTd | MAX | 12 + 0.5 tCK | | | nS |
| RTT enable delay from power down and self refresh exit | tODTe | MAX | 12 | | | nS |
| **CA Training Parameters** | | | | | | |
| First CA calibration command after CA calibration mode is programmed | tCAMRD | MIN | 20 | | | tCK(avg) |
| First CA calibration command after CKE is LOW | tCAENT | MIN | 10 | | | tCK(avg) |
| CA calibration exit command after CKE is HIGH | tCAEXT | MIN | 10 | | | tCK(avg) |
| CKE LOW after CA calibration mode is programmed | tCACKEL | MIN | 10 | | | tCK(avg) |
| CKE HIGH after the last CA calibration results are driven | tCACKEH | MIN | 10 | | | tCK(avg) |
| Data out delay after CA training calibration command is programmed | tADR | MAX | 20 | | | nS |
| MRW CA exit command to DQ tri-state | tMRZ | MIN | 3 | | | nS |
| CA calibration command to CA calibration command delay | tCACD | MIN | RU(tADR+2 × tCK) | | | tCK(avg) |

| Write Leveling Parameters | | | | | | |
|---|---|---|---|---|---|---|
| DQS_t/DQS_c delay after write leveling mode is programmed | tWLDQSEN | MIN | 25 | | | nS |
| | | MAX | - | | | |
| First DQS_t/DQS_c edge after write leveling mode is programmed | tWLMRD | MIN | 40 | | | nS |
| | | MAX | - | | | |
| Write leveling output delay | tWLO | MIN | 0 | | | nS |
| | | MAX | 20 | | | |
| Write leveling hold time | tWLH | MIN | 175 | 150 | 135 | pS |
| Write leveling setup time | tWLS | MIN | 175 | 150 | 135 | pS |
| Mode register set command delay | tMRD | MIN | max(14nS, 10nCK ) | | | nS |
| | | MAX | - | | | |
| **Temperature Derating**[17] | | | | | | |
| DQS output access time from CK_t/CK_c (derated) | tDQSC | MAX | 5620 | | | pS |
| RAS-to-CAS delay (derated) | tRCD | MIN | tRCD + 1.875 | | | nS |
| Activate -to- Activate command period (derated) | tRC | MIN | tRC + 1.875 | | | nS |
| Row active time (derated) | tRAS | MIN | tRAS + 1.875 | | | nS |
| Row precharge time (derated) | tRP | MIN | tRP + 1.875 | | | nS |
| Active bank A to active bank B (derated) | tRRD | MIN | tRRD + 1.875 | | | nS |

**Notes:**

1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
2. All AC timings assume an input slew rate of 2 V/nS for single ended signals.
3. Measured with 4 V/nS differential CK_t/CK_c slew rate and nominal VIX.
4. Read, Write, and input setup and hold values are referenced to VREF.
5. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160nS rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/S. Values do not include clock jitter.
6. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µS rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/S. Values do not include clock jitter.
7. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32mS rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/S. Values do not include clock jitter.
8. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). The figure below shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.




**Output Transition Timing**

9. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t/DQS_c.

10. Measured from the point when DQS_t/DQS_c begins driving the signal to the point when DQS_t/DQS_c begins driving the first rising strobe edge.
11. Measured from the last falling strobe edge of DQS_t/DQS_c to the point when DQS_t/DQS_c finishes driving the signal.
12. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK_t/CK_c crossing.
13. CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching a HIGH/LOW voltage level.
14. Input set-up/hold time for signal (CA[9:0], CS_n).
15. To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is $t_{CKb}$).
16. The LPDDR3 device will set some mode register default values upon receiving a RESET (MRW) command as specified in “Mode Register Definition”.
17. The output skew parameters are measured with default output impedance settings using the reference load.
18. The minimum $t_{CK}$ column applies only when $t_{CK}$ is greater than 6nS.
19. All parts list in order information table (section 3) will not guarantee to meet functional and AC specification if the $t_{CK(avg)}$ out of range mentioned in above table.

### 8.8.2 CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total $t_{IS}$ (setup time) and $t_{IH}$ (hold time) required is calculated by adding the datasheet $t_{IS}$(base) and $t_{IH}$(base) value (see the CA and CS-n Setup and Hold Base-Values tables) to the $\Delta t_{IS}$ and $\Delta t_{IH}$ derating value (see the Derating values $t_{IS}/t_{IH}$ - ac/dc based AC150 and AC135 tables) respectively. Example: $t_{IS}$ (total setup time) = $t_{IS}$(base) + $\Delta t_{IS}$.

Setup ($t_{IS}$) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup ($t_{IS}$) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 77). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 79).

Hold ($t_{IH}$) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold ($t_{IH}$) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 78). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 80).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time $t_{VAC}$ (see the Required time $t_{VAC}$ above $V_{IH(ac)}$ {below $V_{IL(ac)}$} for valid transition for CA table).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the Derating values $t_{IS}/t_{IH}$ - ac/dc based AC150 and AC135 tables, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

**Table of CA Setup and Hold Base-Values**

| Unit [pS] | Data Rate | | | reference |
|---|---|---|---|---|
| | 1600 | 1866 | 2133 | |
| $t_{ISCA(base)}$ | 75 | - | - | $V_{IH/L(ac)} = V_{REF(dc)} \pm 150mV$ |
| $t_{ISCA(base)}$ | - | 62.5 | 47.5 | $V_{IH/L(ac)} = V_{REF(dc)} \pm 135mV$ |
| $t_{IHCA(base)}$ | 100 | 80 | 65 | $V_{IH/L(dc)} = V_{REF(dc)} \pm 100mV$ |

**Note:** AC/DC referenced for 2V/nS CA slew rate and 4V/nS differential CK_t-CK_c slew rate.

**Table of CS_n Setup and Hold Base-Values**

| Unit [pS] | Data Rate | | | reference |
|---|---|---|---|---|
| | 1600 | 1866 | 2133 | |
| $t_{ISCS(base)}$ | 195 | - | - | $V_{IH/L(ac)} = V_{REF(dc)} \pm 150mV$ |
| $t_{ISCS(base)}$ | - | 162.5 | 137.5 | $V_{IH/L(ac)} = V_{REF(dc)} \pm 135mV$ |
| $t_{IHCS(base)}$ | 220 | 180 | 155 | $V_{IH/L(dc)} = V_{REF(dc)} \pm 100mV$ |

**Note:** AC/DC referenced for 2V/nS CS_n slew rate and 4V/nS differential CK_t-CK_c slew rate.


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**Table of Derating values $t_{IS}/t_{IH}$ - ac/dc based AC150**

| $\Delta t_{ISCA}$, $\Delta t_{IHCA}$, $\Delta t_{ISCS}$, $\Delta t_{IHCS}$ derating in [pS] AC/DC based<br>AC150 Threshold ≥ $V_{IH(ac)} = V_{REF(dc)} + 150mV$, $V_{IL(ac)} = V_{REF(dc)} - 150mV$<br>DC100 Threshold ≥ $VI_{H(dc)} = V_{REF(dc)} + 100mV$, $V_{IL(dc)} = V_{REF(dc)} - 100mV$ | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CA, CS_n Slew Rate V/nS | CK_t, CK_c Differential Slew Rate | | | | | | | | | | | |
| | 8.0 V/nS | | 7.0 V/nS | | 6.0 V/nS | | 5.0 V/nS | | 4.0 V/nS | | 3.0 V/nS | |
| | $\Delta t_{IS}$ | $\Delta t_{IH}$ | $\Delta t_{IS}$ | $\Delta t_{IH}$ | $\Delta t_{IS}$ | $\Delta t_{IH}$ | $\Delta t_{IS}$ | $\Delta t_{IH}$ | $\Delta t_{IS}$ | $\Delta t_{IH}$ | $\Delta t_{IS}$ | $\Delta t_{IH}$ |
| **4.0** | 38 | 25 | 38 | 25 | 38 | 25 | 38 | 25 | 38 | 25 | - | - |
| **3.0** | - | - | 25 | 17 | 25 | 17 | 25 | 17 | 25 | 17 | 38 | 29 |
| **2.0** | - | - | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 13 | 13 |
| **1.5** | - | - | - | - | - | - | -25 | -17 | -25 | -17 | -12 | -4 |

**Note:** Cell contents '-' are defined as not supported.

**Table of Derating Values $t_{IS}/t_{IH}$ - ac/dc Based AC135**

| $\Delta t_{ISCA}$, $\Delta t_{IHCA}$, $\Delta t_{ISCS}$, $\Delta t_{IHCS}$ derating in [pS] AC/DC based<br>AC135 Threshold ≥ $V_{IH(ac)} = V_{REF(dc)} + 135mV$, $V_{IL(ac)} = V_{REF(dc)} - 135mV$<br>DC100 Threshold ≥ $VI_{H(dc)} = V_{REF(dc)} + 100mV$, $V_{IL(dc)} = V_{REF(dc)} - 100mV$ | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CA, CS_n Slew Rate V/nS | CK_t, CK_c Differential Slew Rate | | | | | | | | | | | |
| | 8.0 V/nS | | 7.0 V/nS | | 6.0 V/nS | | 5.0 V/nS | | 4.0 V/nS | | 3.0 V/nS | |
| | $\Delta t_{IS}$ | $\Delta t_{IH}$ | $\Delta t_{IS}$ | $\Delta t_{IH}$ | $\Delta t_{IS}$ | $\Delta t_{IH}$ | $\Delta t_{IS}$ | $\Delta t_{IH}$ | $\Delta t_{IS}$ | $\Delta t_{IH}$ | $\Delta t_{IS}$ | $\Delta t_{IH}$ |
| **4.0** | 34 | 25 | 34 | 25 | 34 | 25 | 34 | 25 | 34 | 25 | - | - |
| **3.0** | - | - | 23 | 17 | 23 | 17 | 23 | 17 | 23 | 17 | 34 | 29 |
| **2.0** | - | - | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 11 | 13 |
| **1.5** | - | - | - | - | - | - | -23 | -17 | -23 | -17 | -12 | -4 |

**Note:** Cell contents '-' are defined as not supported.

**Table of Required time $t_{VAC}$ above $V_{IH(ac)}$ {below $V_{IL(ac)}$} for valid transition for CA**

| Slew Rate [V/nS] | $t_{VAC}$ [pS] @ 150mV 1600Mbps | | $t_{VAC}$ [pS] @ 135mV 1866Mbps | | $t_{VAC}$ [pS] @ 135mV 2133Mbps | |
|---|---|---|---|---|---|---|
| | min | max | min | max | min | max |
| **> 4.0** | 48 | - | 40 | - | 34 | - |
| **4.0** | 48 | - | 40 | - | 34 | - |
| **3.5** | 46 | - | 39 | - | 33 | - |
| **3.0** | 43 | - | 36 | - | 30 | - |
| **2.5** | 40 | - | 33 | - | 27 | - |
| **2.0** | 35 | - | 29 | - | 23 | - |
| **1.5** | 27 | - | 21 | - | 15 | - |
| **<1.5** | 27 | - | 21 | - | 15 | - |


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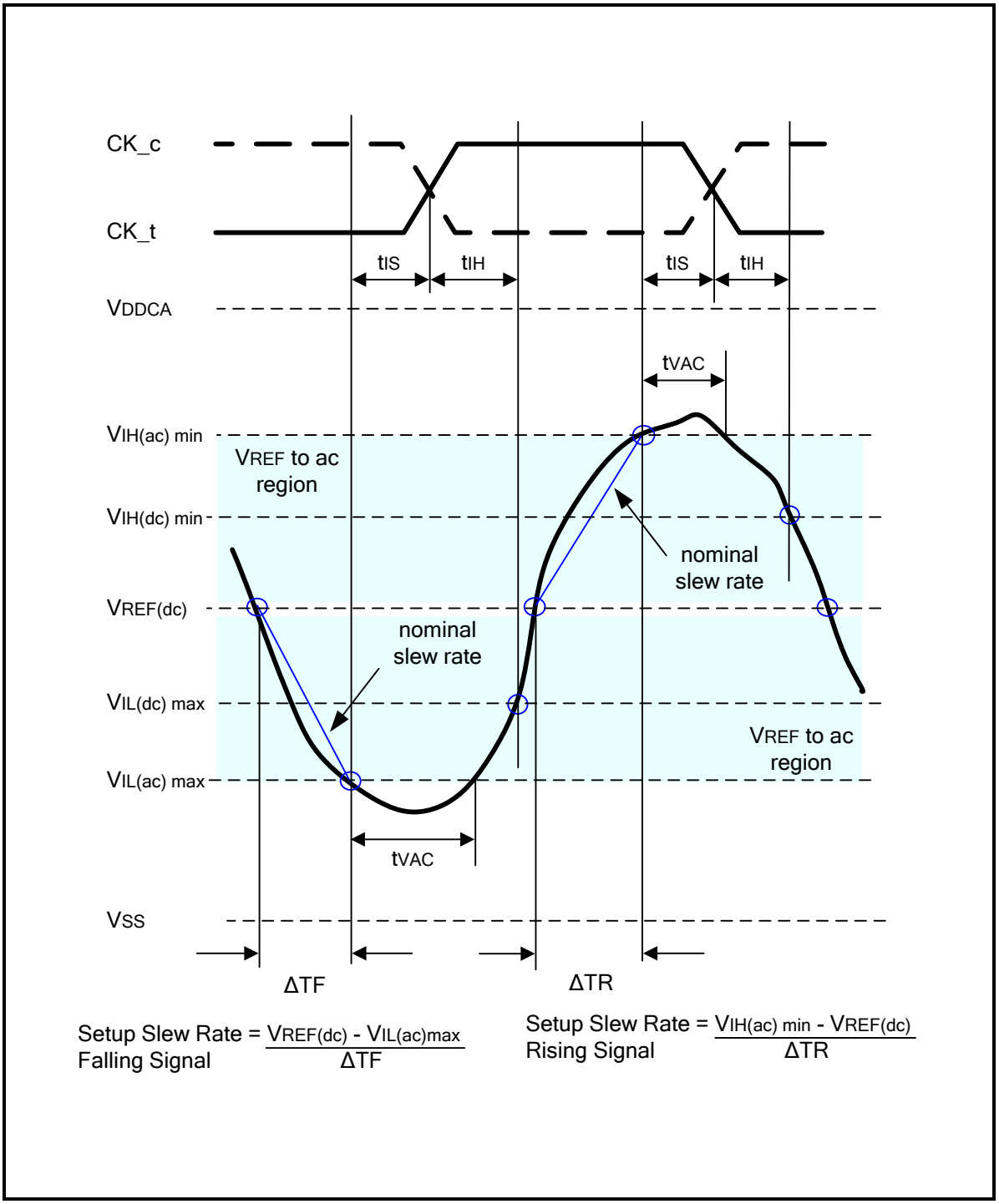



**Figure 77 - Nominal slew rate and $t_{VAC}$ for setup time $t_{IS}$ for CA and CS_n with respect to clock**


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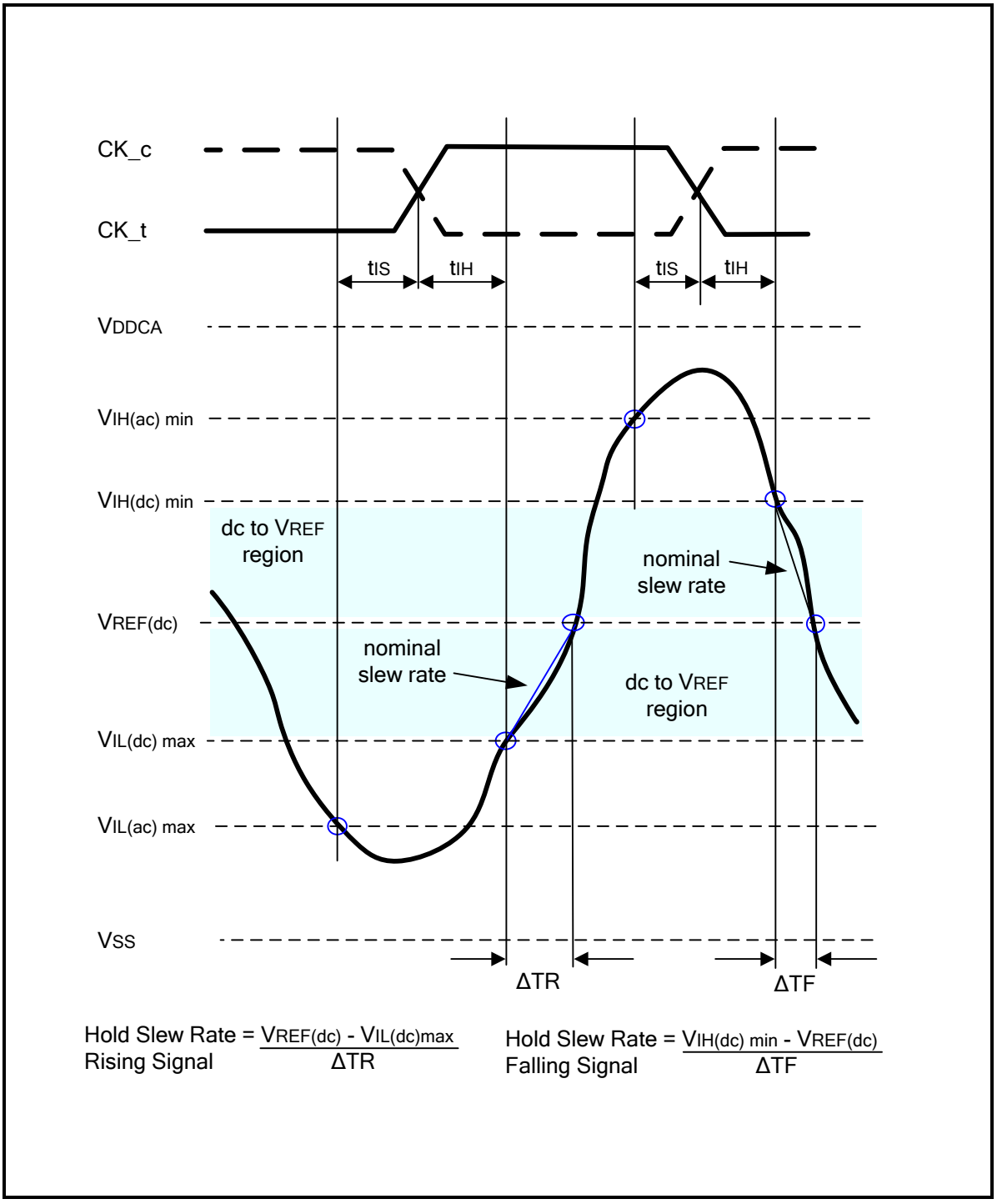



**Figure 78 - Nominal slew rate for hold time $t_{IH}$ for CA and CS_n with respect to clock**


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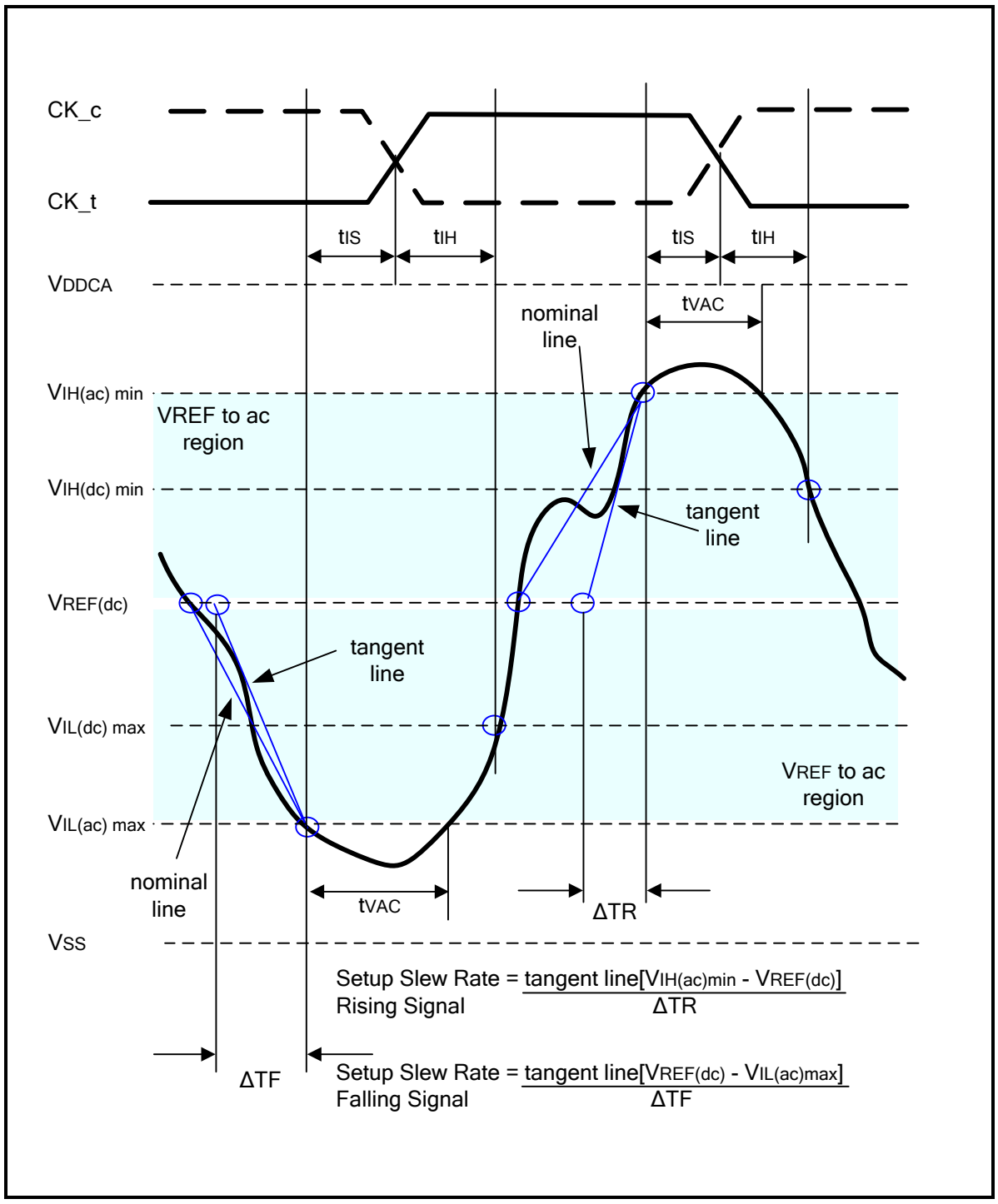



**Figure 79 - Tangent line for setup time $t_{IS}$ for CA and CS_n with respect to clock**


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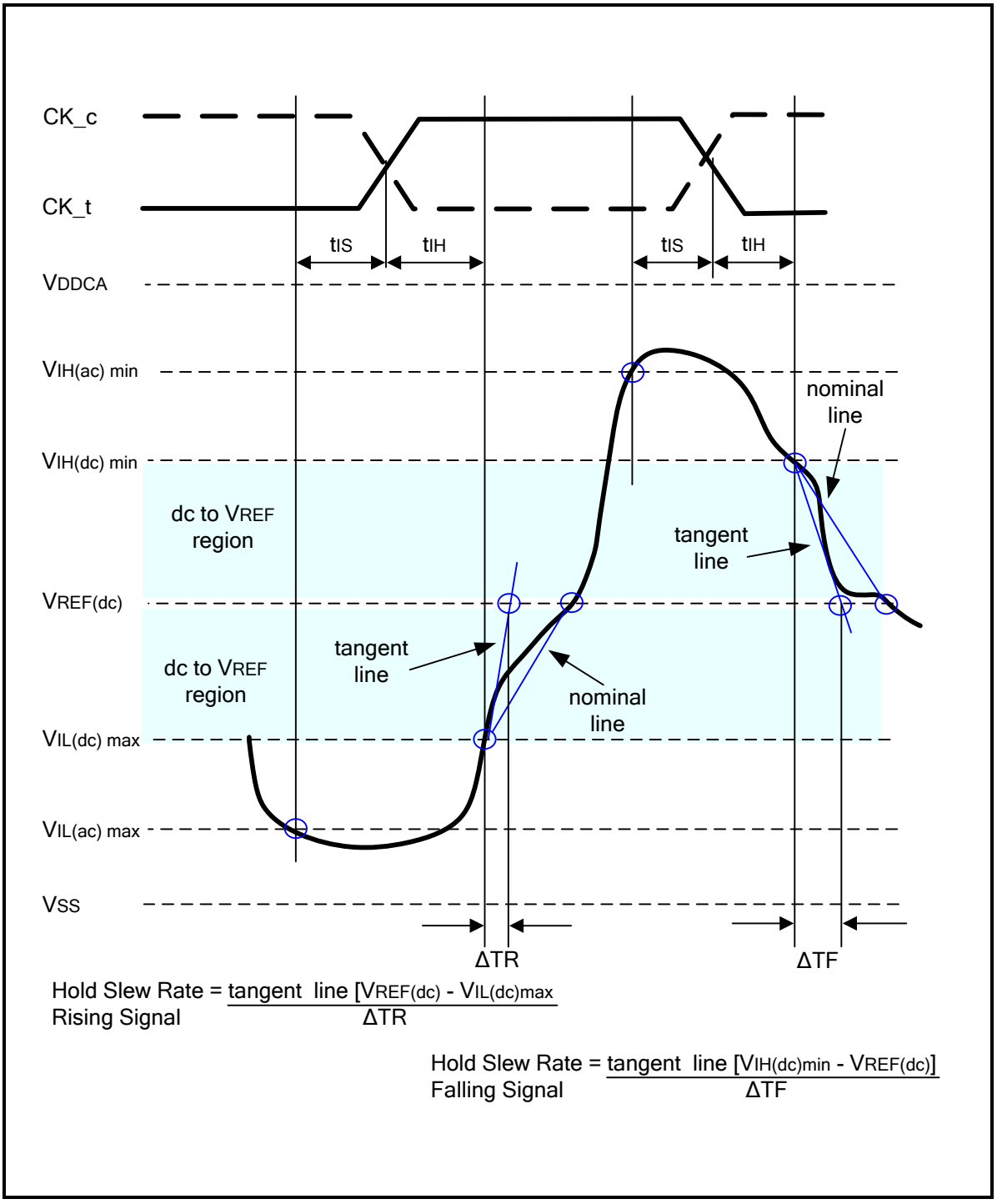



**Figure 80 - Tangent line for hold time $t_{IH}$ for CA and CS_n with respect to clock**


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### 8.8.3 Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total $t_{DS}$ (setup time) and $t_{DH}$ (hold time) required is calculated by adding the data sheet $t_{DS}$(base) and $t_{DH}$(base) value (see the Data Setup and Hold Base-Values table) to the $\Delta t_{DS}$ and $\Delta t_{DH}$ derating value (see the Derating values LPDDR3 $t_{DS}/t_{DH}$ - ac/dc based AC150 and AC135 tables) respectively. Example: $t_{DS}$ (total setup time) = $t_{DS}$(base) + $\Delta t_{DS}$.

Setup ($t_{DS}$) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup ($t_{DS}$) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure 81). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 83).

Hold ($t_{DH}$) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold ($t_{DH}$) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}$min and the first crossing of $V_{REF(dc)}$) (see Figure 82). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 84).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time $t_{VAC}$ (see Required time $t_{VAC}$ above $V_{IH(ac)}$ {below $V_{IL(ac)}$} for valid transition for DQ, DM Table).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the Derating values LPDDR3 $t_{DS}/t_{DH}$ - ac/dc based AC150 and AC135 tables, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

**Table of Data Setup and Hold Base-Values**

| Unit [pS] | Data Rate | | | reference |
|---|---|---|---|---|
| | 1600 | 1866 | 2133 | |
| $t_{DS(base)}$ | 75 | - | - | $V_{IH/L(ac)} = V_{REF(dc)} \pm 150mV$ |
| $t_{DS(base)}$ | - | 62.5 | 47.5 | $V_{IH/L(ac)} = V_{REF(dc)} \pm 135mV$ |
| $t_{DH(base)}$ | 100 | 80 | 65 | $V_{IH/L(dc)} = V_{REF(dc)} \pm 100mV$ |

**Note:** AC/DC referenced for 2V/nS DQ, DM slew rate and 4V/nS differential DQS_t-DQS_c slew rate and nominal VIX.


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**Table of Derating values LPDDR3 $t_{DS}/t_{DH}$ - ac/dc based AC150**

| $\Delta t_{DS}$, $\Delta t_{DH}$ derating in [pS] AC/DC based<br>AC150 Threshold ≥ $V_{IH(ac)} = V_{REF(dc)} + 150mV$, $V_{IL(ac)} = V_{REF(dc)} - 150mV$<br>DC100 Threshold ≥ $V_{IH(dc)} = V_{REF(dc)} + 100mV$, $V_{IL(dc)} = V_{REF(dc)} - 100mV$ | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DQ, DM Slew Rate V/nS | DQS_t, DQS_c Differential Slew Rate | | | | | | | | | | | |
| | 8.0 V/nS | | 7.0 V/nS | | 6.0 V/nS | | 5.0 V/nS | | 4.0 V/nS | | 3.0 V/nS | |
| | $\Delta t_{DS}$ | $\Delta t_{DH}$ | $\Delta t_{DS}$ | $\Delta t_{DH}$ | $\Delta t_{DS}$ | $\Delta t_{DH}$ | $\Delta t_{DS}$ | $\Delta t_{DH}$ | $\Delta t_{DS}$ | $\Delta t_{DH}$ | $\Delta t_{DS}$ | $\Delta t_{DH}$ |
| **4.0** | 38 | 25 | 38 | 25 | 38 | 25 | 38 | 25 | 38 | 25 | - | - |
| **3.0** | - | - | 25 | 17 | 25 | 17 | 25 | 17 | 25 | 17 | 38 | 29 |
| **2.0** | - | - | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 13 | 13 |
| **1.5** | - | - | - | - | - | - | -25 | -17 | -25 | -17 | -12 | -4 |

**Note:** Cell contents '-' are defined as not supported.

**Table of Derating values LPDDR3 $t_{DS}/t_{DH}$ - ac/dc based AC135**

| $\Delta t_{DS}$, $\Delta t_{DH}$ derating in [pS] AC/DC based<br>AC135 Threshold -> $V_{IH(ac)} = V_{REF(dc)} + 135mV$, $V_{IL(ac)} = V_{REF(dc)} - 135mV$<br>DC100 Threshold -> $V_{IH(dc)} = V_{REF(dc)} + 100mV$, $V_{IL(dc)} = V_{REF(dc)} - 100mV$ | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DQ, DM Slew Rate V/nS | DQS_t, DQS_c Differential Slew Rate | | | | | | | | | | | |
| | 8.0 V/nS | | 7.0 V/nS | | 6.0 V/nS | | 5.0 V/nS | | 4.0 V/nS | | 3.0 V/nS | |
| | $\Delta t_{DS}$ | $\Delta t_{DH}$ | $\Delta t_{DS}$ | $\Delta t_{DH}$ | $\Delta t_{DS}$ | $\Delta t_{DH}$ | $\Delta t_{DS}$ | $\Delta t_{DH}$ | $\Delta t_{DS}$ | $\Delta t_{DH}$ | $\Delta t_{DS}$ | $\Delta t_{DH}$ |
| **4.0** | 34 | 25 | 34 | 25 | 34 | 25 | 34 | 25 | 34 | 25 | - | - |
| **3.0** | - | - | 23 | 17 | 23 | 17 | 23 | 17 | 23 | 17 | 34 | 29 |
| **2.0** | - | - | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 11 | 13 |
| **1.5** | - | - | - | - | - | - | -23 | -17 | -23 | -17 | -12 | -4 |

**Note:** Cell contents '-' are defined as not supported.

**Table of Required time $t_{VAC}$ above $V_{IH(ac)}$ {below $V_{IL(ac)}$} for valid transition for DQ, DM**

| Slew Rate [V/nS] | $t_{VAC}$ [pS] @ 150mV 1600Mbps | | $t_{VAC}$ [pS] @ 135mV 1866Mbps | | $t_{VAC}$ [pS] @ 135mV 2133Mbps | |
|---|---|---|---|---|---|---|
| | min | max | min | max | min | max |
| **> 4.0** | 48 | - | 40 | - | 34 | - |
| **4.0** | 48 | - | 40 | - | 34 | - |
| **3.5** | 46 | - | 39 | - | 33 | - |
| **3.0** | 43 | - | 36 | - | 30 | - |
| **2.5** | 40 | - | 33 | - | 27 | - |
| **2.0** | 35 | - | 29 | - | 23 | - |
| **1.5** | 27 | - | 21 | - | 15 | - |
| **<1.5** | 27 | - | 21 | - | 15 | - |


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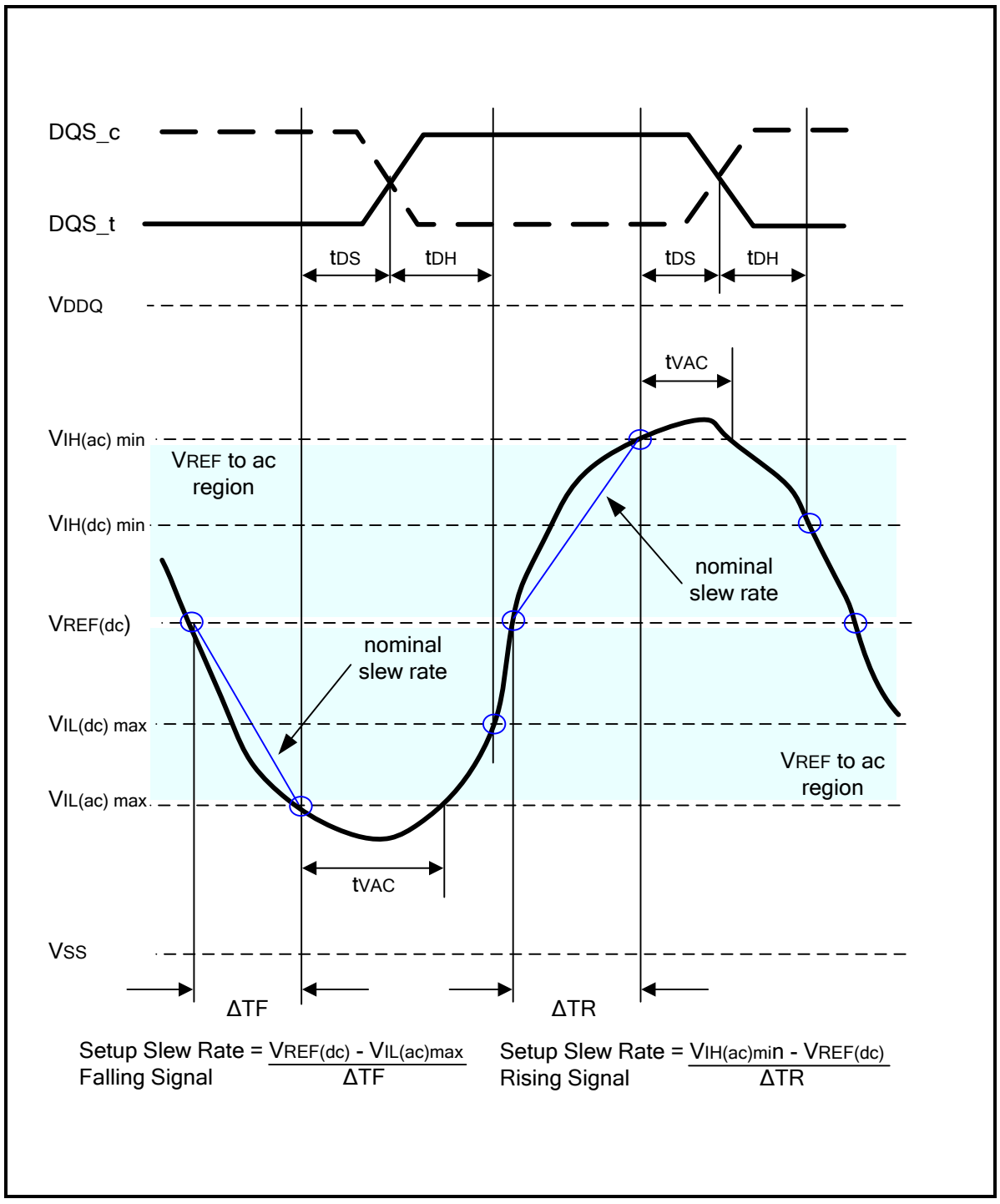



**Figure 81 - Nominal slew rate and $t_{VAC}$ for setup time $t_{DS}$ for DQ with respect to strobe**


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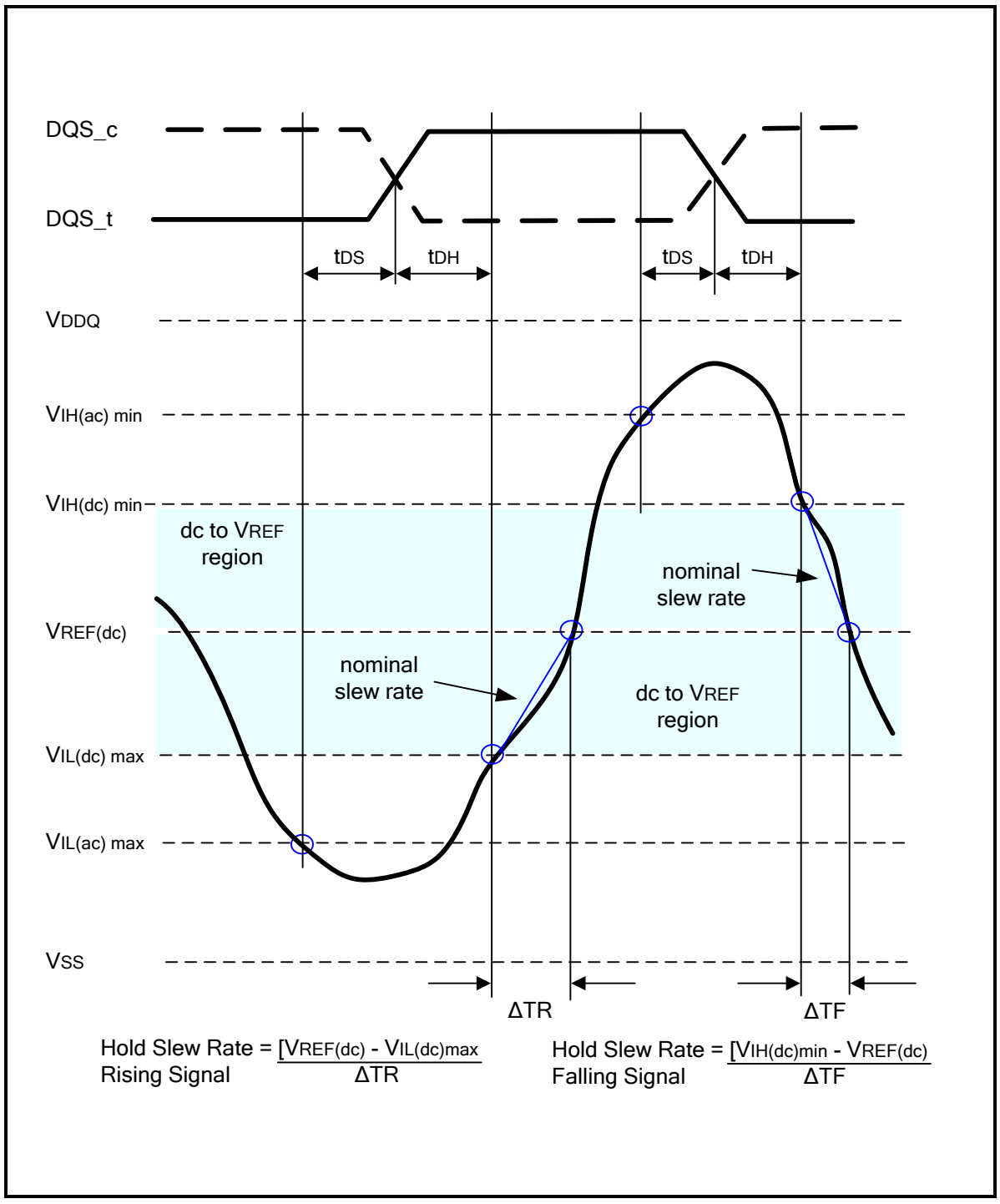



**Figure 82 - Nominal slew rate for hold time $t_{DH}$ for DQ with respect to strobe**


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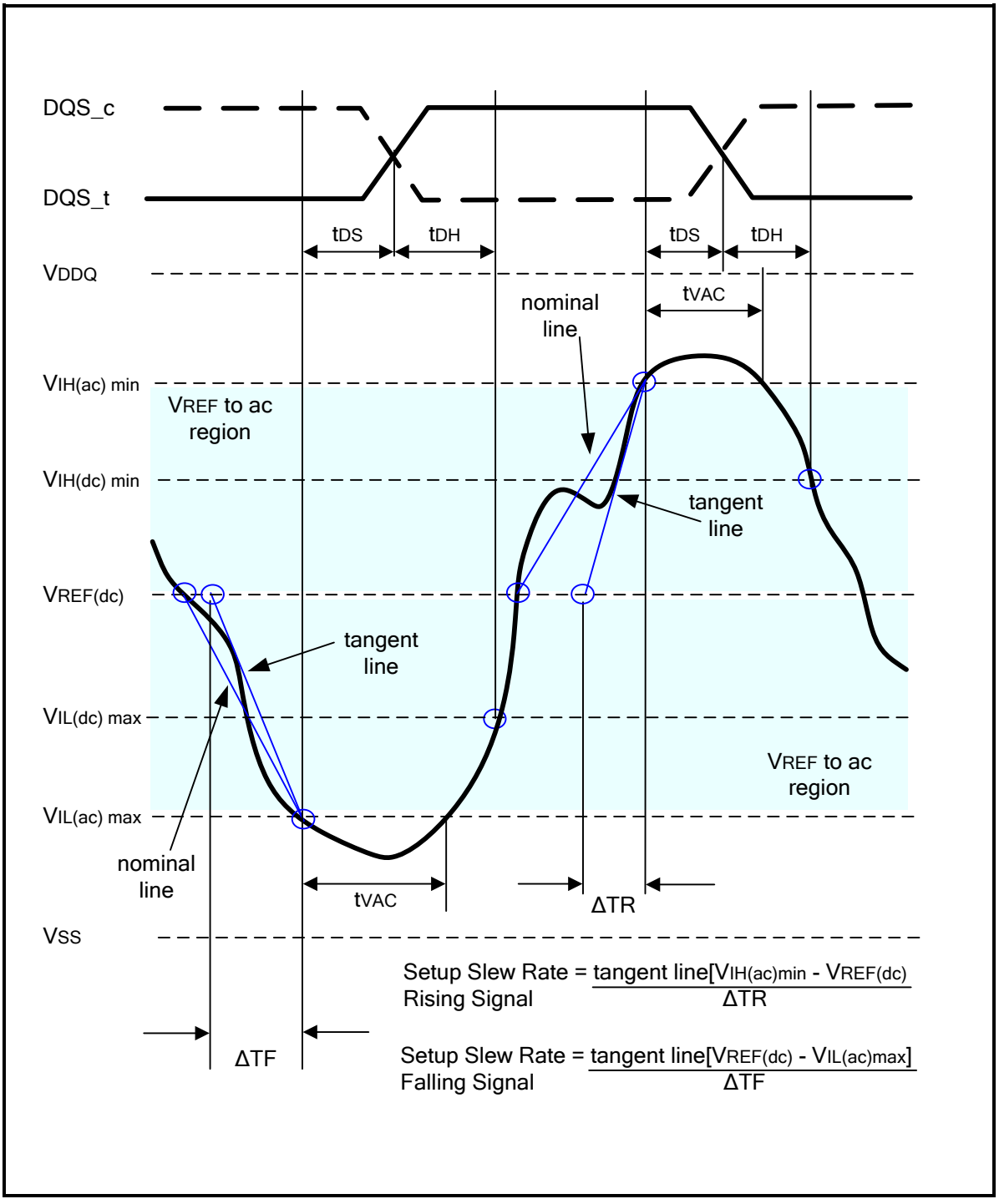



**Figure 83 - Tangent line for setup time $t_{DS}$ for DQ with respect to strobe**


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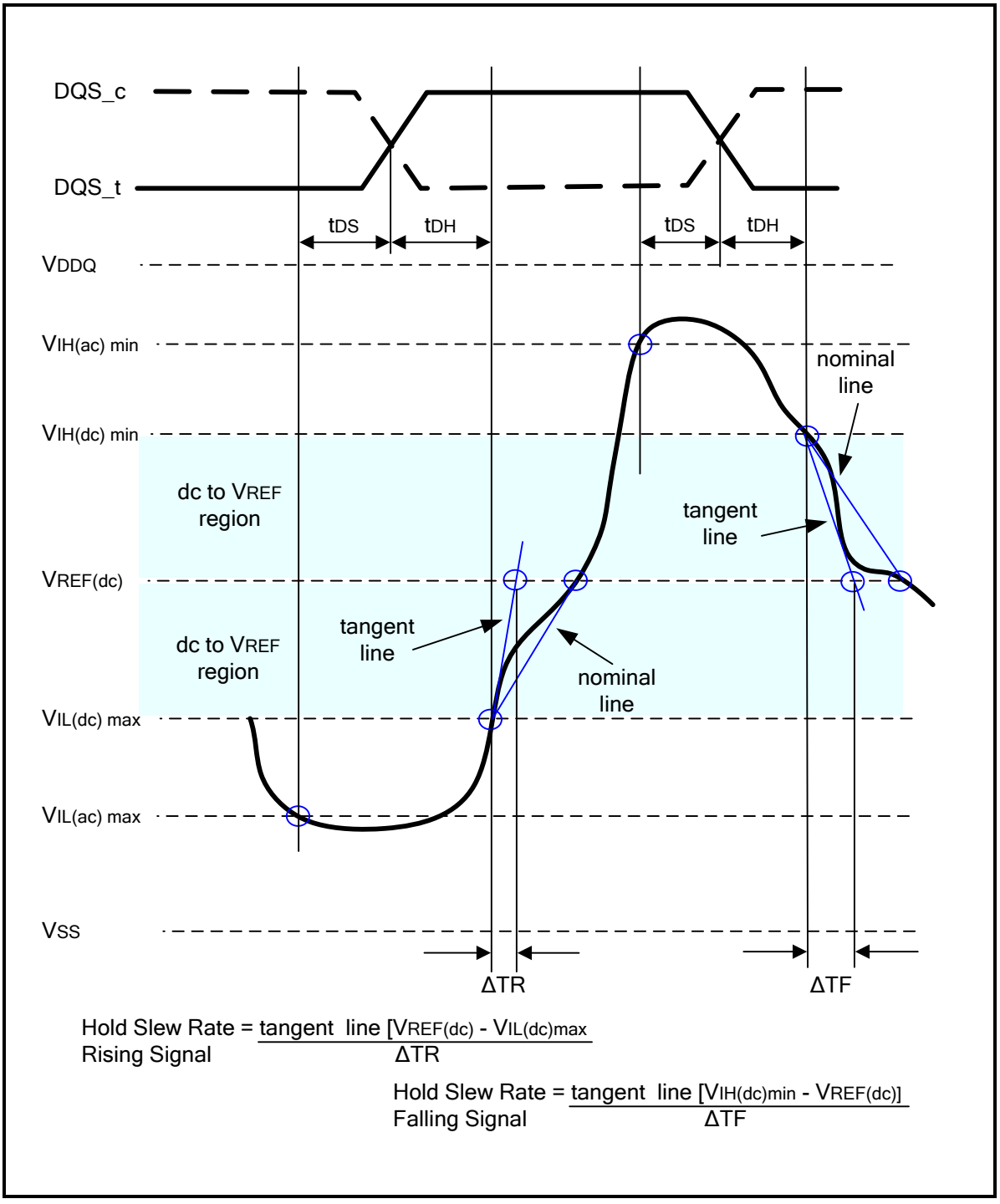
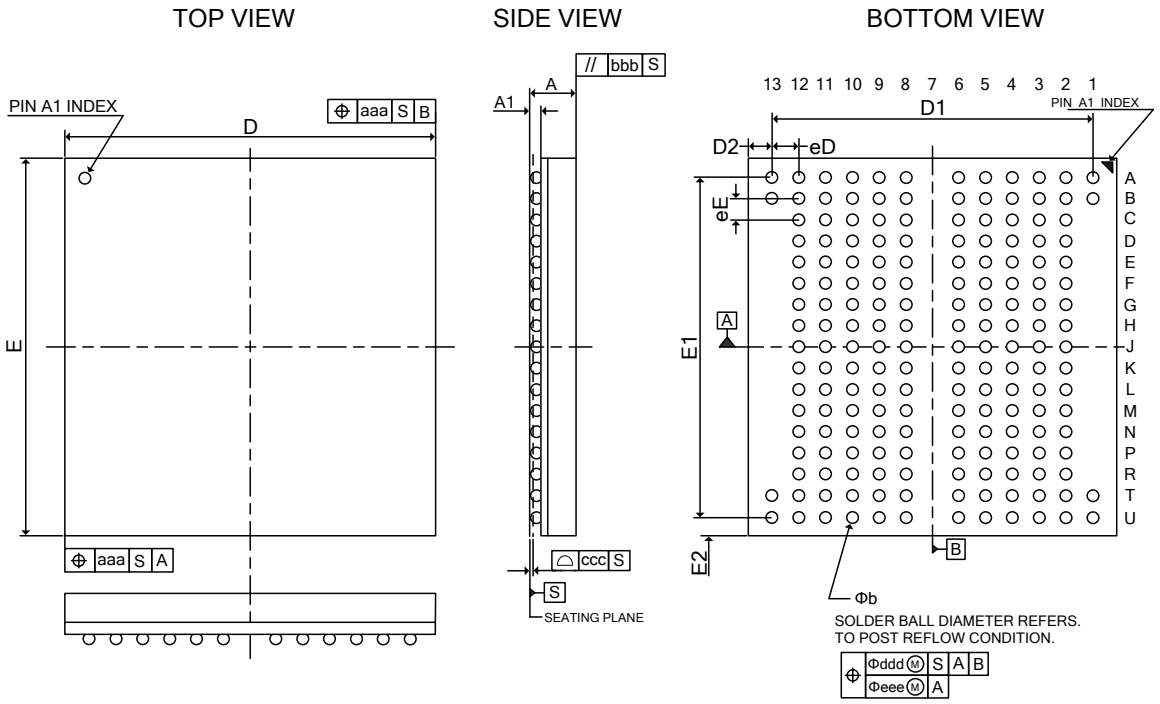



**Figure 84 - Tangent line for hold time $t_{DH}$ for DQ with respect to strobe**


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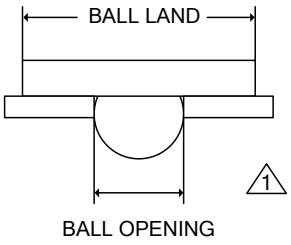
## 9. PACKAGE DIMENSIONS

### Package Outline VFBGA 178 Ball (11x11.5 mm$^2$) Solder ball size: 0.3mm




Controlling Dimension: Millimeters

| SYMBOL | DIMENSION (MM) | | | DIMENSION (Inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| A1 | 0.18 | 0.23 | 0.28 | 0.007 | 0.009 | 0.011 |
| b | 0.26 | 0.31 | 0.36 | 0.010 | 0.012 | 0.014 |
| D | 10.90 | 11.00 | 11.10 | 0.429 | 0.433 | 0.437 |
| E | 11.40 | 11.50 | 11.60 | 0.449 | 0.453 | 0.457 |
| D1 | 9.60 BSC. | | | 0.378 BSC. | | |
| E1 | 10.40 BSC. | | | 0.409 BSC. | | |
| D2 | 0.70 BSC. | | | 0.028 BSC. | | |
| E2 | 0.55 BSC. | | | 0.022 BSC. | | |
| eD | 0.80 BSC. | | | 0.032 BSC. | | |
| eE | 0.65 BSC. | | | 0.026 BSC. | | |
| aaa | --- | --- | 0.15 | --- | --- | 0.006 |
| bbb | --- | --- | 0.10 | --- | --- | 0.004 |
| ccc | --- | --- | 0.10 | --- | --- | 0.004 |
| ddd | --- | --- | 0.15 | --- | --- | 0.006 |
| eee | --- | --- | 0.05 | --- | --- | 0.002 |




Note:
1. Ball land: 0.38mm, Ball opening: 0.28mm,
   PCB Ball land suggested ≤ 0.38mm


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## 10. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A01-001 | May 30, 2019 | All | Initial formal datasheet |
| A01-002 | Jul. 24, 2019 | 97 | Revise 800 & 1066 MHz $I_{DD5AB1}$ spec value (1mA ---> 1.22mA) |
| | | | Revise 800 MHz $I_{DD5AB2}$ spec value (11mA ---> 10.5mA) |
| A01-003 | Dec. 03, 2019 | 5, 74, 75, 79, 85, 95~97, 104~107, 109, 110, 115, 116 | Add four of 933 MHz x16 and 32 VFBGA178 package part numbers and DC/AC spec |
| A01-004 | Apr. 13, 2020 | 95 | Update $IDD2N_1$ and $IDD2NS_1$ IDD parameters current spec values |
| A01-005 | Jul. 28, 2020 | 95~98 | Update all related to $VDD_1$ portion IDD parameters current spec values except $IDD0_1$, $IDD5_1$ and $IDD8_1$ |
| | | 98 | Update $IDD6_2$ of 1/2, 1/4 & 1/8 Array PASR current spec values |

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