W29N01GZ/W
1G-BIT 1.8V
NAND FLASH MEMORY

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1. GENERAL DESCRIPTION

The W29N01GZ/W (1G-bit) NAND Flash memory provides a storage solution for embedded systems with limited space, pins and power. It is ideal for code shadowing to RAM, solid state applications and storing media data such as, voice, video, text and photos. The device operates on a single 1.7V to 1.95V power supply with active current consumption as low as 25mA and 10uA for CMOS standby current.

The memory array totals 138,412,032 bytes, and organized into 1,024 erasable blocks of 135,168 bytes. Each block consists of 64 programmable pages of 2,112-bytes each. Each page consists of 2,048-bytes for the main data storage area and 64-bytes for the spare data area (The spare area is typically used for error management functions).

The W29N01GZ/W supports the standard NAND flash memory interface using the multiplexed 8-bit bus to transfer data, addresses, and command instructions. The five control signals, CLE, ALE, #CE, #RE and #WE handle the bus interface protocol. Also, the device has two other signal pins, the #WP (Write Protect) and the RY/#BY (Ready/Busy) for monitoring the device status.

2. FEATURES

- **Basic Features**
  - Density : 1Gbit (Single chip solution)
  - Vcc : 1.7V to 1.95V
  - Bus width : X8 X16
  - Operating temperature
    - Industrial: - 40°C to 85°C
- **Single-Level Cell (SLC) technology.**
- **Organization**
  - Density: 1G-bit/128M-byte
  - Page size
    - 2,112 bytes (2048 + 64 bytes)
    - 1,056 words(1024 +32 words)
  - Block size
    - 64 pages (128K + 4K bytes)
    - 64 pages(64K +2K words)
- **Highest Performance**
  - Read performance (Max.)
    - Random read: 25us
    - Sequential read cycle: 35ns
  - Write Erase performance
    - Page program time: 300us(typ.)
    - Block erase time: 2ms(typ.)
  - Endurance 100,000 Erase/Program Cycles(1)
  - 10-years data retention
- **Command set**
  - Standard NAND command set
  - Additional command support
    - Sequential Cache Read
    - Random Cache Read
    - Cache Program
    - Copy Back
    - OTP Data Program
    - OTP Data Lock by Page
    - OTP Data Read
  - Contact Winbond for block Lock feature
- **Lowest power consumption**
  - Read: 10mA(typ.)
  - Program/Erase: 10mA(typ.)
  - CMOS standby: 10uA(typ.)
- **Space Efficient Packaging**
  - 48-ball VFBGA
  - Contact Winbond for stacked packages/KGD

Note:

1. **Endurance specification is based on 1bit/528 byte ECC (Error Correcting Code).**

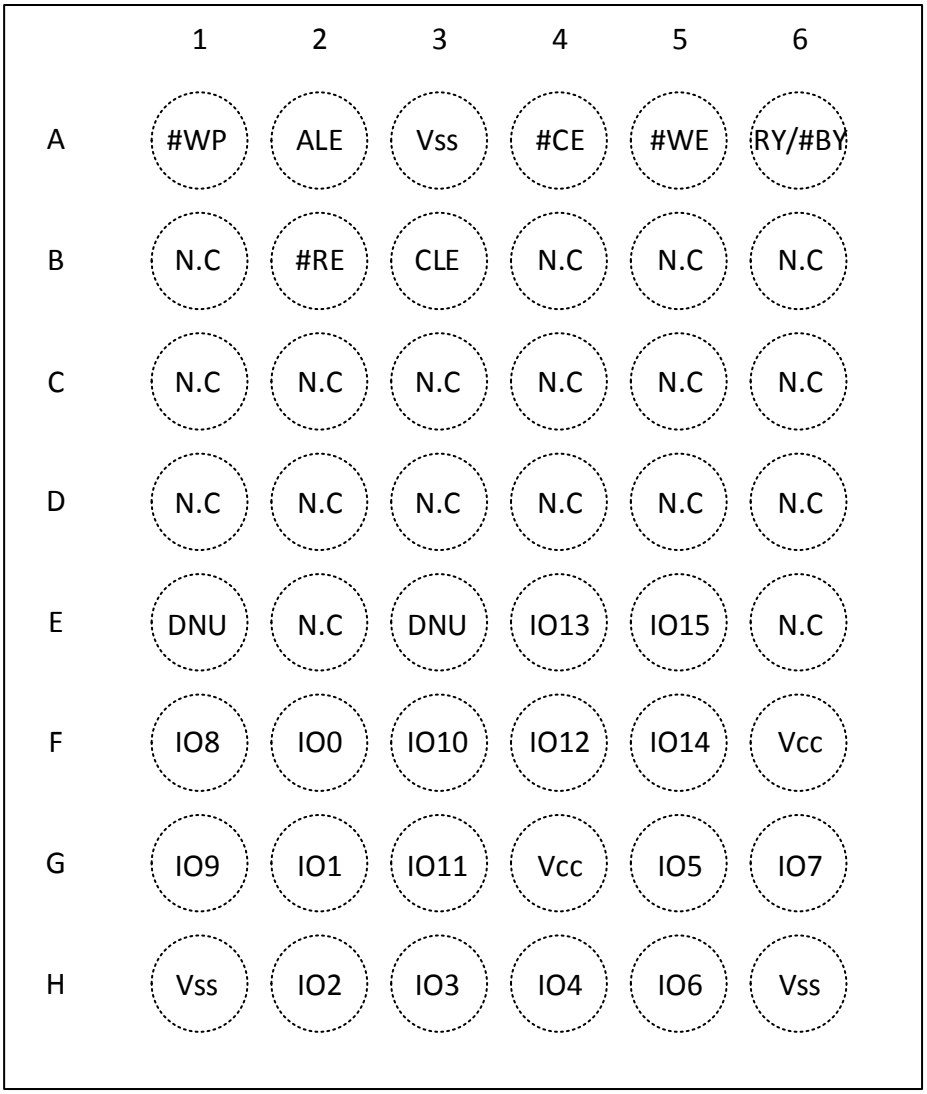
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3. PACKAGE TYPES AND PIN CONFIGURATIONS

W29N01GZ/W is offered in a 48-ball VFBGA package (Code D) as shown in Figure 3-1 , respectively. Package diagrams and dimensions are illustrated in Section: Package Dimensions.

3.1 Pin assignment 48 ball VFBGA（X8/X16）

Top View, ball down



Note: For x8 product, IO8 to IO15 are N.C

Figure 3-1 Pin Assignment 48-ball VFBGA (Package Code B)

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3.2 Pin Descriptions

PIN NAME	I/O	FUNCTION
#WP	I	Write Protect
ALE	I	Address Latch Enable
#CE	I	Chip Enable
#WE	I	Write Enable
RY/#BY	O	Ready/Busy
#RE	I	Read Enable
CLE	I	Command Latch Enable
I/O[0-7] I/O[0-15]	I/O	Data Input/Output (X8 X16)
Vcc	Supply	Power supply
Vss	Supply	Ground
DNU	-	Do Not Use: DNUs must be left unconnected.
N.C	-	No Connect

Table 3-1 Pin Descriptions

Note:

1. **Connect all Vcc and Vss pins to power supply or ground. Do not leave Vcc or Vss disconnected.**

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4. PIN DESCRIPTIONS

4.1 Chip Enable (#CE)

#CE pin enables and disables device operation. When #CE is high the device is disabled and the I/O pins are set to high impedance and enters into standby mode if not busy. When #CE is set low the device will be enabled, power consumption will increase to active levels and the device is ready for Read and Write operations.

4.2 Write Enable (#WE)

#WE pin enables the device to control write operations to input pins of the device. Such as, command instructions, addresses and data that are latched on the rising edge of #WE.

4.3 Read Enable (#RE)

#RE pin controls serial data output from the pre-loaded Data Register. Valid data is present on the I/O bus after the tREA period from the falling edge of #RE. Column addresses are incremented for each #RE pulse.

4.4 Address Latch Enable (ALE)

ALE pin controls address input to the address register of the device. When ALE is active high, addresses are latched via the I/O pins on the rising edge of #WE.

4.5 Command Latch Enable (CLE)

CLE pin controls command input to the command register of the device. When CLE is active high, commands are latched into the command register via I/O pins on the rising edge of #WE.

4.6 Write Protect (#WP)

#WP pin can be used to prevent the inadvertent program/erase to the device. When #WP pin is active low, all program/erase operations are disabled.

4.7 Ready/Busy (RY/#BY)

RY/#BY pin indicates the device status. When RY/#BY output is low, it indicates that the device is processing either a program, erase or read operations. When it returns to high, those operations have completed. RY/#BY pin is an open drain.

4.8 Input and Output (I/Ox)

I/Ox bi-directional pins are used for the following; command, address and data operations.

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5. BLOCK DIAGRAM

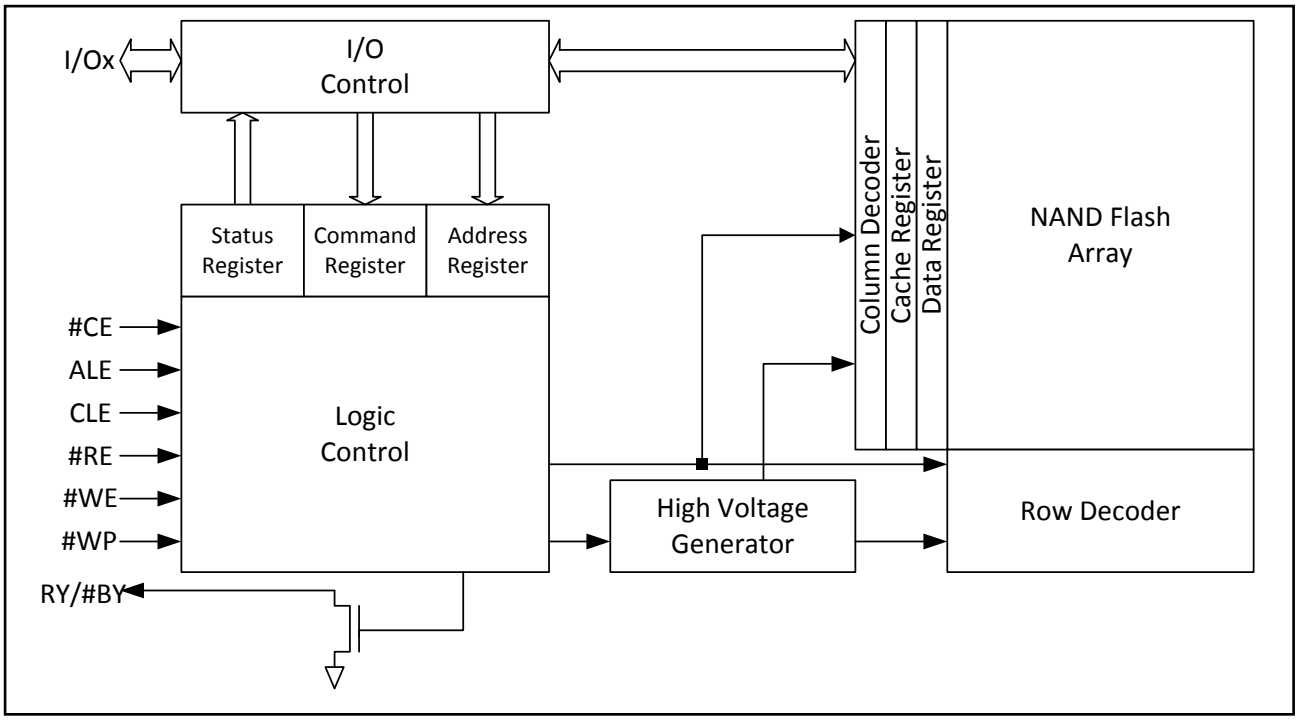


Figure 5-1 NAND Flash Memory Block Diagram

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6. MEMORY ARRAY ORGANIZATION

6.1 X8 Array Organization

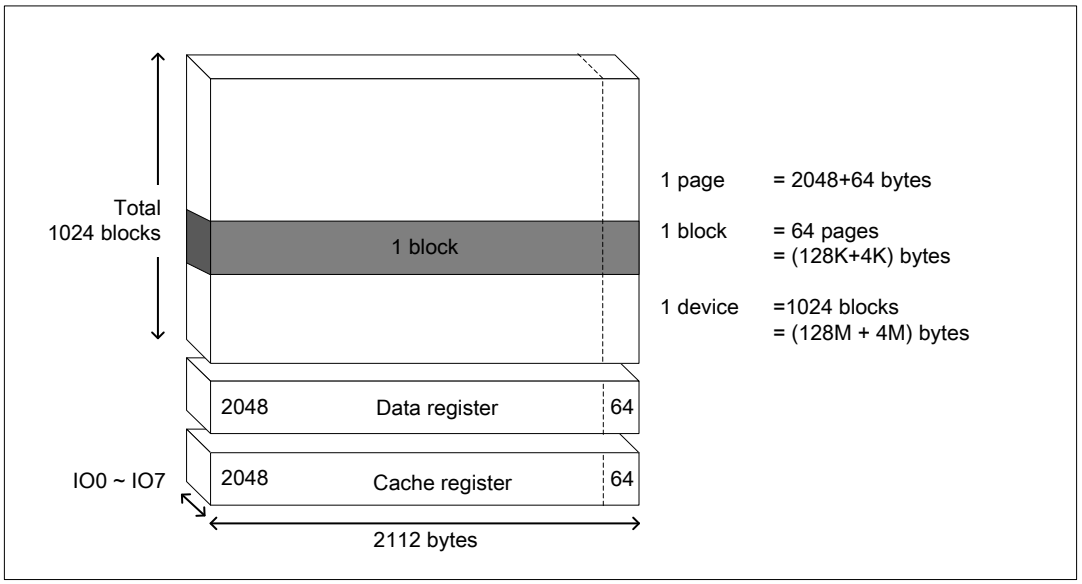


Figure 6-1 Array Organization(X8)

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st cycle	A7	A6	A5	A4	A3	A2	A1	A0
2nd cycle	L	L	L	L	A11	A10	A9	A8
3rd cycle	A19	A18	A17	A16	A15	A14	A13	A12
4th cycle	A27	A26	A25	A24	A23	A22	A21	A20

Table 6-1 Addressing(X8)

Notes:

1. **"L" indicates a low condition, which must be held during the address cycle to insure correct processing.**
2. **A0 to A11 during the 1st and 2nd cycles are column addresses. A12 to A27 during the 3rd and 4th cycles are row addresses.**
3. **The device ignores any additional address inputs that exceed the device's requirement.**

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6.2 X16 Array Organization

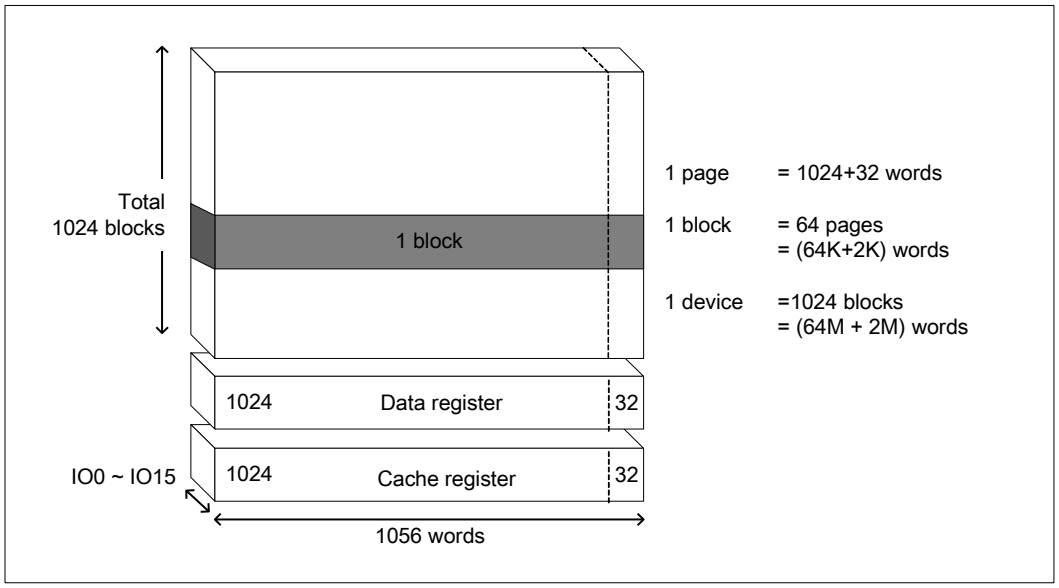


Figure 6-2 Array Organization(X16)

	I/O8~15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st cycle	L	A7	A6	A5	A4	A3	A2	A1	A0
2nd cycle	L	L	L	L	L	L	A10	A9	A8
3rd cycle	L	A18	A17	A16	A15	A14	A13	A12	A11
4th cycle	L	A26	A25	A24	A23	A22	A21	A20	A19

Table 6-2 Addressing(X16)

NOTE:

1. **"L" must to be held Low during the address cycle is inputted**
2. **A0 to A10 of 1st and 2nd cycle are column address, A11 to A26 of 3rd and 4th cycle are row address**
3. **The device ignores any additional address input than the device is required**

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7. MODE SELECTION TABLE

MODE		CLE	ALE	#CE	#WE	#RE	#WP
Read mode	Command input	H	L	L		H	X
	Address input	L	H	L		H	X
Write mode	Command input	H	L	L		H	H
	Address input	L	H	L		H	H
Data input		L	L	L		H	H
Sequential Read and Data output		L	L	L	H		X
During read (busy)		X	X	X	X	H	X
During program (busy)		X	X	X	X	X	H
During erase (busy)		X	X	X	X	X	H
Write protect		X	X	X	X	X	L
Standby		X	X	H	X	X	0V/Vcc

Table 7-1 Mode Selection

Notes:

1. **"H" indicates a HIGH input level, "L" indicates a LOW input level, and "X" indicates a Don't Care Level.**
2. **#WP should be biased to CMOS HIGH or LOW for standby.**

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8. COMMAND TABLE

COMMAND	1st CYCLE	2nd CYCLE	Acceptable during busy
PAGE READ	00h	30h	
READ for COPY BACK	00h	35h	
SEQUENTIAL CACHE READ	31h		
RANDOM CACHE READ	00h	31h	
LAST ADDRESS CACHE READ	3Fh		
READ ID	90h		
READ STATUS	70h		Yes
RESET	FFh		Yes
PAGE PROGRAM	80h	10h	
PROGRAM for COPY BACK	85h	10h	
CACHE PROGRAM	80h	15h	
BLOCK ERASE	60h	D0h	
RANDOM DATA INPUT(1)	85h		
RANDOM DATA OUTPUT(1)	05h	E0h	
READ PARAMETER PAGE	ECh		
READ UNIQUE ID	EDh		
GET FEATURES	EEh		
SET FEATURES	EFh		
OTP DATA PROTECT	A5h	10h	
OTP DATA PROGRAM	A0h	10h	
OTP DATA READ	AFh	30h	

Table 8-1 Command Table

Notes:

4. **RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.**
5. **Any commands that are not in the above table are considered as undefined and are prohibited as inputs.**

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9. DEVICE OPERATIONS

9.1 READ operation

9.1.1 PAGE READ (00h-30h)

When the device powers on, the default is READ mode. This operation can also be entered by writing 00h command to the command register, and then write four address cycles, followed by writing 30h command. After writing 30h command, the data is transferred from NAND array to Data Register during tR. Data transfer progress can be done by monitoring the status of the RY/#BY signal output. RY/#BY signal will be LOW during data transfer. Also, there is an alternate method by using the READ STATUS (70h) command. If the READ STATUS command is issued during read operation, the Read (00h) command must be re-issued to read out the data from Data Register. When the data transfer is complete, RY/#BY signal goes HIGH, and the data can be read from Data Register by toggling #RE. Read is sequential from initial column address to the end of the page. (See Figure 9-1)

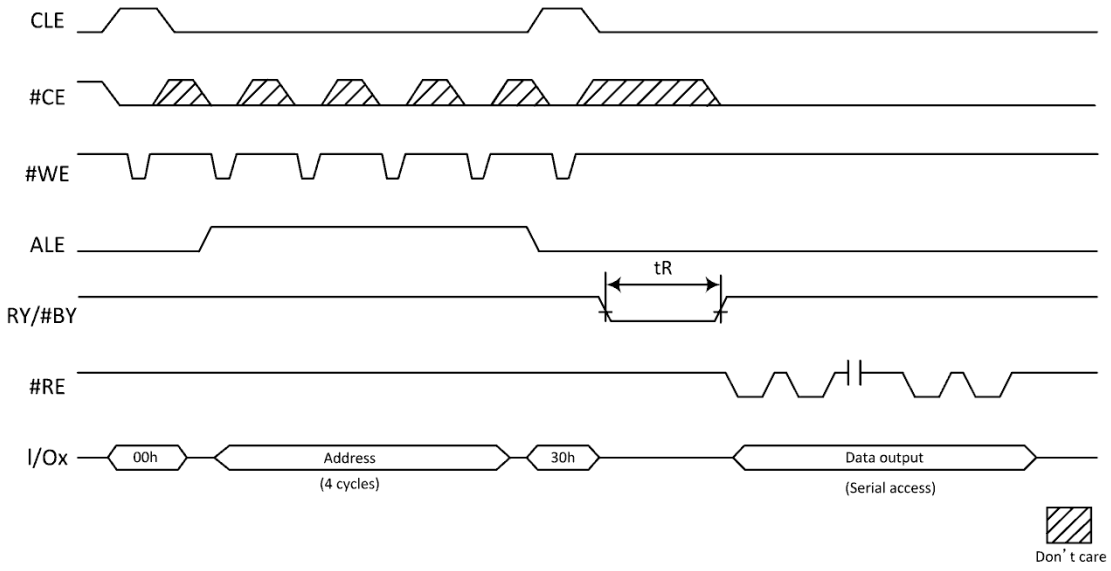


Figure 9-1 Page Read Operations

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9.1.2 CACHE READ OPERATIONS

To obtain a higher degree of performance read operations, the device's Cache and Data Register can be used independent of each other. Data can be read out from the Cache Register, while array data is transferred from the NAND Array to the Data Register.

The CACHE READ mode starts with issuing a PAGE READ command (00h-30h) to transfer a page of data from NAND array to the Cache Register. RY/#BY signal will go LOW during data transfer indicating a busy status. Copying the next page of data from the NAND array to the Data Register while making the Cache Register page data available is done by issuing either a SEQUENTIAL CACHE READ (31h) or RANDOM CACHE READ (00h-31h) command. The SEQUENTIAL CACHE READ mode will copy the next page of data in sequence from the NAND array to the Data Register or use the RANDOM CACHE READ mode (00h-31h) to copy a random page of data from NAND array to the Data Register. The RY/#BY signal goes LOW for a period of tRCBSY during the page data transfer from NAND array to the Data Register. When RY/#BY goes HIGH, this means that the Cache Register data is available and can be read out of the Cache Register by toggling #RE, which starts at address column 0. If it is desired to start at a different column address, a RANDOM DATA OUTPUT (05h-E0h) command can be used to change the column address to read out the data.

At this point in the procedure when completing the read of the desired number of bytes, one of two things can be chosen. Continue CACHE READ (31h or 00h-31h) operations or end the CACHE READ mode with a LAST ADDRESS CACHE READ (3Fh) command.

To continue with the read operations, execute the CACHE READ (31h or 00h-31h) command. The RY/#BY signal goes LOW for the period of tRCBSY while data is copied from Data Register to the Cache Register and the next page of data starts being copied from the NAND array to the Data Register. When RY/#BY signal goes HIGH signifying that the Cache Register data is available, at this time #RE can start toggling to output the desired data starting at column 0 address or using the RANDOM DATA OUPUT command for random column address access.

To terminate the CACHE READ operations a LAST ADDRESS CACHE READ (3Fh) command is issued, RY/#BY signal goes LOW and the Data Register contents is copied to the Cache Register. At the completion of the Data Register to Cache Register transfer, RY/#BY goes HIGH indicating data is available at the output of the Cache Register. At this point Data can be read by toggling #RE starting at column address 0 or using the RANDOM DATA OUPUT command for random column address access. The device NAND array is ready for next command set.

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9.1.2.1. SEQUENTIAL CACHE READ (31h)

The SEQUENTIAL CACHE READ (31h) copies the next page of data in sequence within block to the Data Register while the previous page of data in the Cache Register is available for output. This is done by issuing the command (31h), RY/#BY signal goes LOW and the STATUS REGISTER bits 6 and 5 = “00” for the period of tRCBSY. When RY/#BY signal goes HIGH and STATUS REGISTER bits 6 and 5 = “10”, data at the Cache Register is available. The data can be read out from the Cache Register by toggling #RE, starting address is column 0 or by using the RANDOM DATA OUPUT command for random column address access.

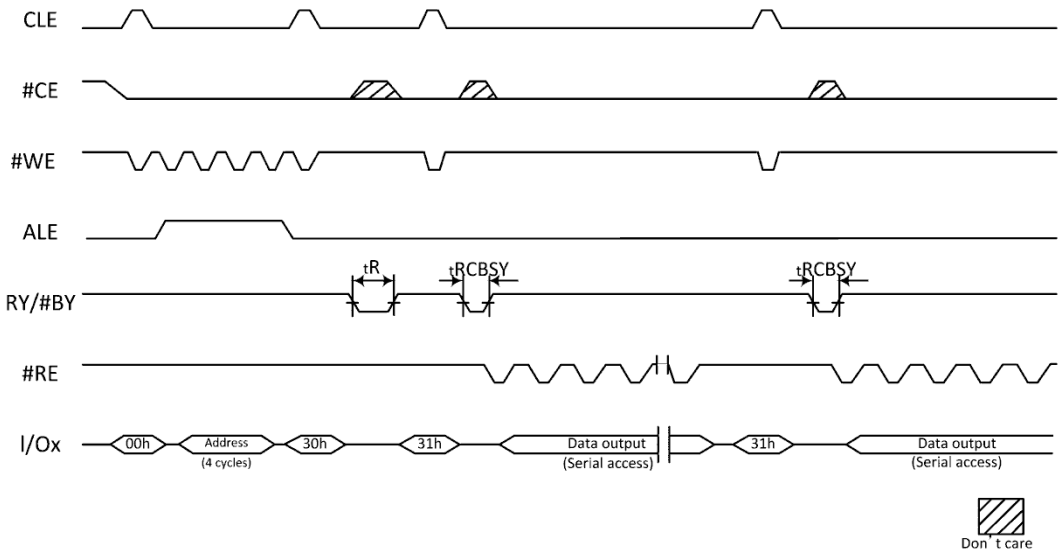


Figure 9-2 Sequential Cache Read Operations

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9.1.2.2. RANDOM CACHE READ (00h-31h)

The RANDOM CACHE READ (00h-31h) will copy a particular page from NAND array to the Data Register while the previous page of data is available at the Cache Register output. Perform this function by first issuing the 00h command to the Command Register, then writing the four address cycles for the desired page of data to the Address Register. Then write the 31h command to the Command Register. Note; the column address bits are ignored.

After the RANDOM CACHE READ command is issued, RY/#BY signal goes LOW and STATUS REGISTER bits 6 and 5 equal “00” for the period of tRCBSY. When RY/#BY signal goes HIGH and STATUS REGISTER bits 6 and 5 equal “10”, the page data in the Cache Register is available. The data can read out from the Cache Register by toggling #RE, the starting column address will be 0 or use the RANDOM DATA OUTPUT (05h-E0h) command change the column address to start reading out the data.

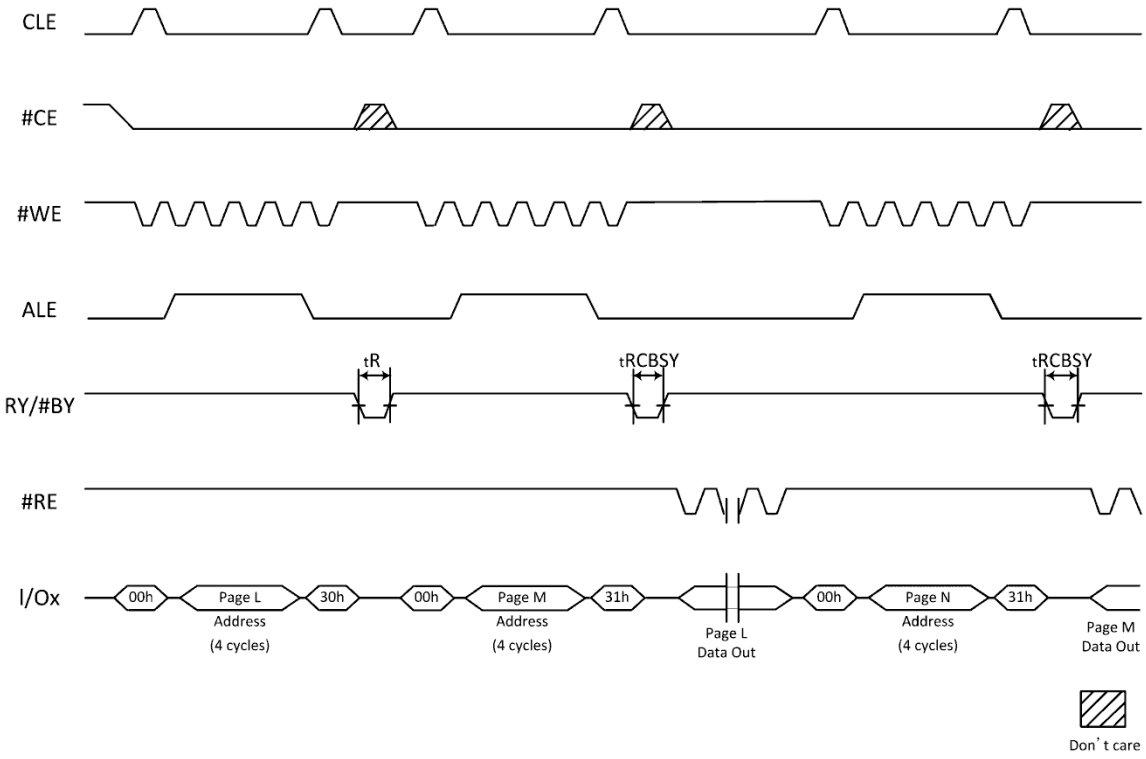


Figure 9-3 Random Cache Read Operation

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9.1.2.3. LAST ADDRESS CACHE READ (3Fh)

The LAST ADDRESS CACHE READ (3Fh) copies a page of data from the Data Register to the Cache Register without starting the another cache read. After writing the 3Fh command, RY/#BY signal goes LOW and STATUS REGISTER bits 6 and 5 equals “00” for the period of tRCBSY. When RY/#BY signal goes HIGH and STATUS REGISTER bits 6 and 5 equals “11”, the Cache Register data is available, and the device NAND array is in ready state. The data can read out from the Cache Register by toggling #RE, starting at address column 0 or RANDOM DATA OUTPUT (05h-E0h) command to change the column address to read out the data.

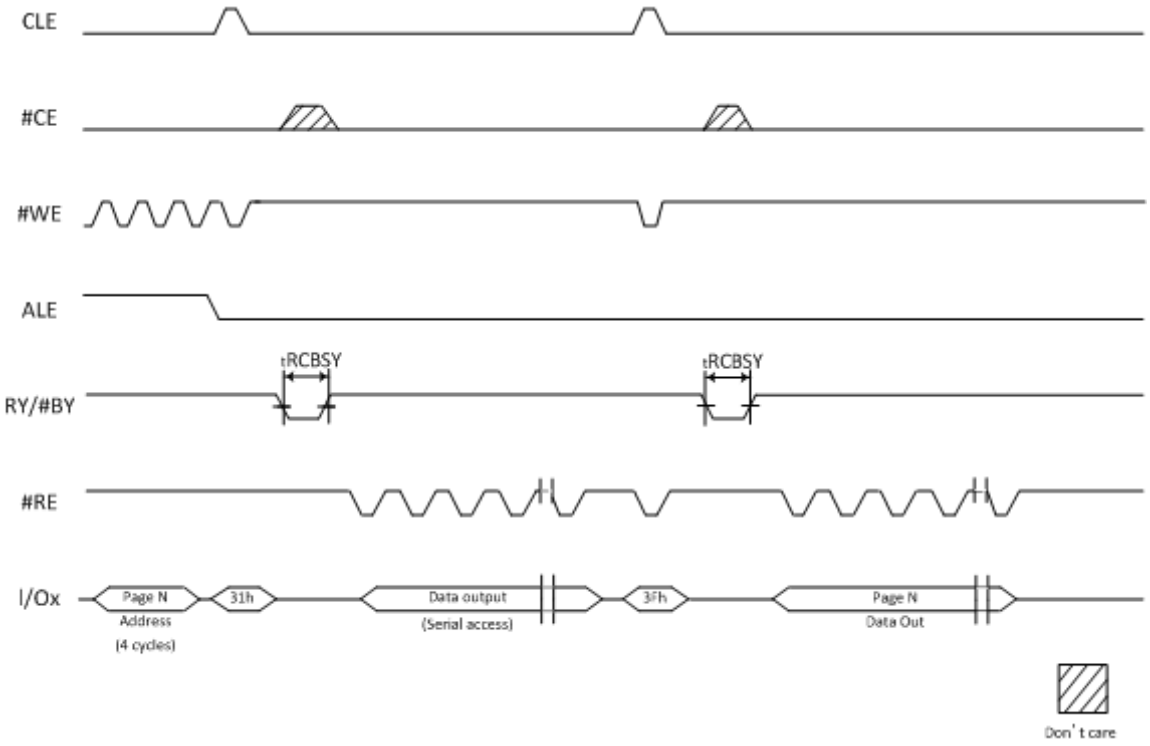


Figure 9-4 Last Address Cache Read Operation

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9.1.3 RANDOM DATA OUTPUT (05h-E0h)

The RANDOM DATA OUTPUT allows the selection of random column addresses to read out data from a single or multiple of addresses. The use of the RANDOM DATA OUTPUT command is available after the PAGE READ (00h-30h) sequence by writing the 05h command following by the 2 cycle column address and then the E0h command. Toggling #RE will output data sequentially. The RANDOM DATA OUTPUT command can be issued multiple times, but limited to the current loaded page.

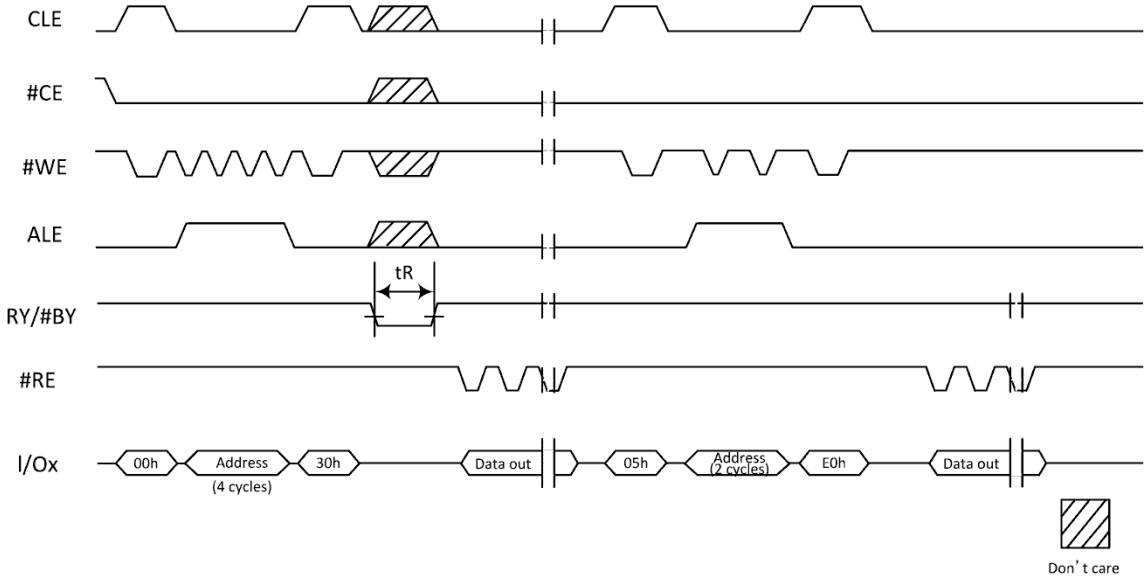


Figure 9-5 Random Data Output

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9.1.4 READ ID (90h)

READ ID command is comprised of two modes determined by the input address, device (00h) or ONFI (20h) identification information. To enter the READ ID mode, write 90h to the Command Register followed by a 00h address cycle, then toggle #RE for 5 single byte cycles, the W29N01GZ/W pre-programmed code includes the Manufacturer ID, Device ID, and Product-Specific Information (see Table 9.1). If the READ ID command is followed by 20h address, the output code includes 4 single byte cycles of ONFI identifying information (see Table 9.2). The device remains in the READ ID mode until the next valid command is issued.

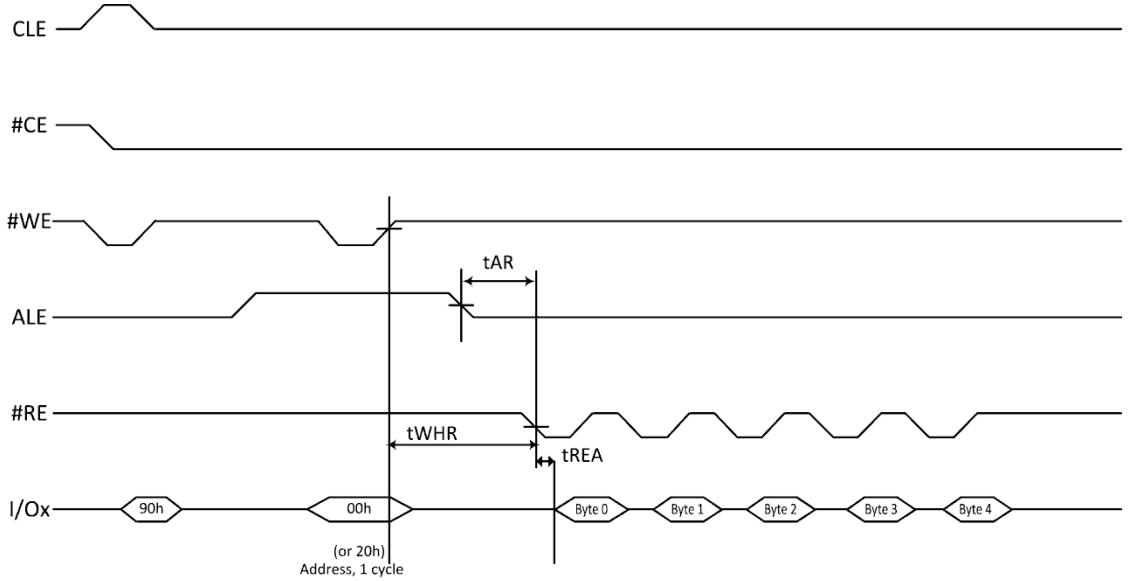


Figure 9-6 Read ID

# of Byte/Cycles	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle	5th Byte/Cycle
X8	EFh	A1h	80h	15h.	00h.
X16	EFh	B1h	80h	55h	00h
Description	MFR ID	Device ID	Cache Programming Supported	Page Size:2KB Spare Area Size:64B BLK Size w/o Spare:128KB Organized:X8 X16 Serial Access:35ns	

Table 9-1 Device ID and configuration codes for Address 00h

# of Byte/Cycles	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle
Code	4Fh	4Eh	46h	49h

Table 9-2 ONFI identifying codes for Address 20h

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9.1.5 READ PARAMETER PAGE (ECh)

READ PARAMETER PAGE can read out the device's parameter data structure, such as, manufacturer information, device organization, timing parameters, key features, and other pertinent device parameters. The data structure is stored with at least three copies in the device's parameter page. Figure 9-7 shows the READ PARAMETER PAGE timing. The RANDOM DATA OUTPUT (05h-E0h) command is supported during data output.

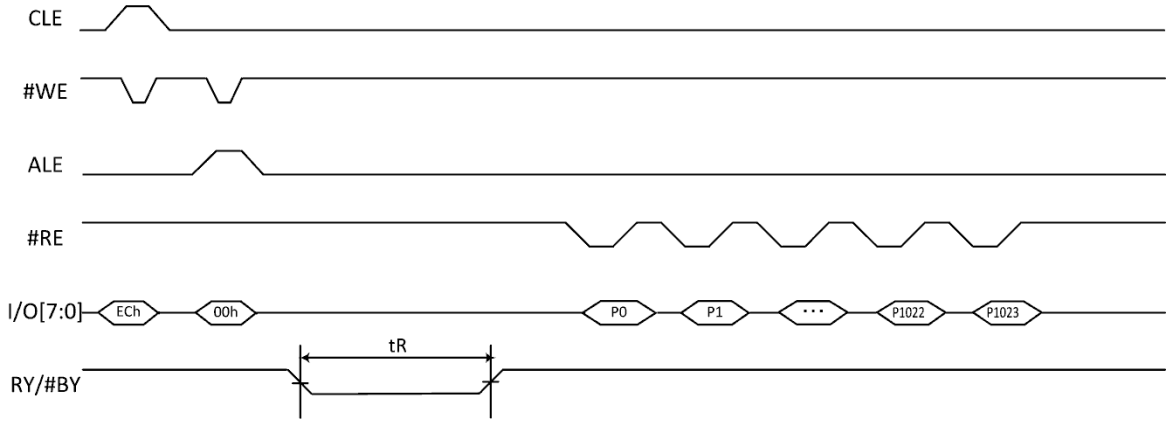


Figure 9-7 Read Parameter Page

Byte	Description		Value
0-3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4-5	Revision number		02h, 00h
6-7	Features supported	W29N01GZ (x8) W29N01GW (x16)	10h, 00h 11h, 00h
8-9	Optional commands supported		37h, 00h
10-31	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32-43	Device manufacturer		57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44-63	Device model	W29N01GZ (x8)	57h, 32h, 39h, 4Eh, 30h, 31h, 47h, 5Ah, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		W29N01GW(X16)	57h, 32h, 39h, 4Eh, 30h, 31h, 47h, 57h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		EFh
65-66	Date code		00h, 00h
67-79	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80-83	# of data bytes per page		00h, 08h, 00h, 00h
84-85	# of spare bytes per page		40h, 00h
86-89	# of data bytes per partial page		00h, 02h, 00h, 00h
90-91	# of spare bytes per partial page		10h, 00h

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Byte	Description	Value
92-95	# of pages per block	40h, 00h, 00h, 00h
96-99	# of blocks per unit	00h, 04h, 00h, 00h
100	# of logical units	01h
101	# of address cycles	22h
102	# of bits per cell	01h
103-104	Bad blocks maximum per unit	14h, 00h
105-106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108-109	Block endurance for guaranteed valid blocks	00h, 00h
110	# of programs per page	04h
111	Partial programming attributes	00h
112	# of ECC bits	01h
113	# of interleaved address bits	00h
114	Interleaved operation attributes	00h
115-127	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
128	I/O pin capacitance	0Ah
129-130	Timing mode support	07h, 00h
131-132	Program cache timing	07h, 00h
133-134	Maximum page program time	BCh, 02h
135-136	Maximum block erase time	10h, 27h
137-138	Maximum random read time	19h, 00h
139-140	tCCS minimum	46h, 00h
141-163	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
164-165	Vendor specific revision #	01h,00h
166-253	Vendor specific	00h
254-255	Integrity CRC	Set at shipment
256-511	Value of bytes 0-255	
512-767	Value of bytes 0-255	
>767	Additional redundant parameter pages	

Table 9-3 Parameter Page Output Value

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9.1.6 READ STATUS (70h)

The W29N01GZ/W has an 8-bit Status Register which can be read during device operation. Refer to Table 9.4 for specific Status Register definitions. After writing 70h command to the Command Register, read cycles will only read from the Status Register. The status can be read from I/O[7:0] outputs, as long as #CE and #RE are LOW. Note; #RE does not need to be toggled for Status Register read. The Command Register remains in status read mode until another command is issued. To change to normal read mode, issue the PAGE READ (00h) command. After the PAGE READ command is issued, data output starts from the initial column address.

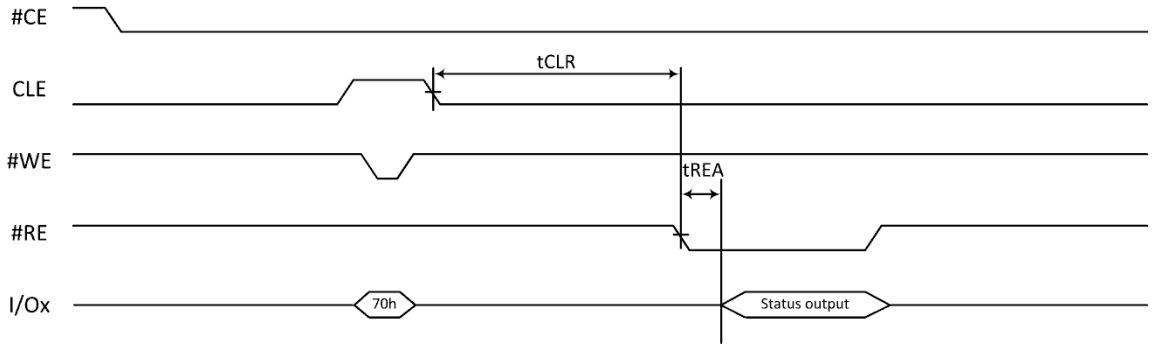


Figure 9-8 Read Status Operation

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SR bit	Page Read	Cache Read	Page Program	Cache Program	Block Erase	Definition
I/O 0	Not Use	Not Use	Pass/Fail	Pass/Fail(N)	Pass/Fail	0=Successful Program/Erase 1=Error in Program/Erase
I/O 1	Not Use	Not Use	Not Use	Pass/Fail(N-1)	Not Use	0=Successful Program 1=Error in Program
I/O 2	Not Use	Not Use	Not Use	Not Use	Not Use	0
I/O 3	Not Use	Not Use	Not Use	Not Use	Not Use	0
I/O 4	Not Use	Not Use	Not Use	Not Use	Not Use	0
I/O 5	Ready/Busy	Ready/Busy[1]	Ready/Busy	Ready/Busy	Ready/Busy	Ready = 1 Busy = 0
I/O 6	Ready/Busy	Cache Ready/Busy[2]	Ready/Busy	Cache Ready/Busy	Ready/Busy	Ready = 1 Busy = 0
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Unprotected = 1 Protected = 0

Table 9-4 Status Register Bit Definition

Notes:

1. **SR bit 5 is 0 during the actual programming operation. If cache mode is used, this bit will be 1 when all internal operations are complete.**
2. **SR bit 6 is 1 when the Cache Register is ready to accept new data. RY/#BY follows bit 6.**

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9.1.7 READ UNIQUE ID (EDh)

The W29N01GZ/W NAND Flash device has a method to uniquely identify each NAND Flash device by using the READ UNIQUE ID command. The format of the ID is limitless, but the ID for every NAND Flash device manufactured, will be guaranteed to be unique.

Numerous NAND controllers typically use proprietary error correction code (ECC) schemes. In these cases Winbond cannot protect unique ID data with factory programmed ECC. However, to ensure data reliability, Winbond will program the NAND Flash devices with 16 bytes of unique ID code, starting at byte 0 on the page, immediately followed by 16 bytes of the complement of that unique ID. The combination of these two actions is then repeated 16 times. This means the final copy of the unique ID will resides at location byte 511. At this point an XOR or exclusive operation can be performed on the first copy of the unique ID and its complement. If the unique ID is good, the results should yield all the bits as 1s. In the event that any of the bits are 0 after the XOR operation, the procedure can be repeated on a subsequent copy of the unique ID data.

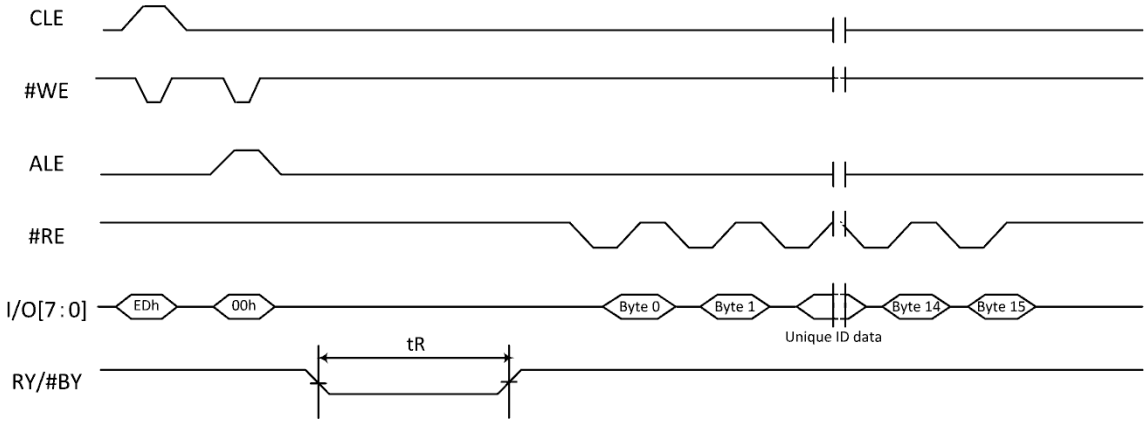


Figure 9-9 Read Unique ID

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9.2 PROGRAM operation

9.2.1 PAGE PROGRAM (80h-10h)

The W29N01GZ/W Page Program command will program pages sequentially within a block, from the lower order page address to higher order page address. Programming pages out of sequence is prohibited. The W29N01GX supports partial-page programming operations up to 4 times before an erase is required if partitioning a page. Note; programming a single bit more than once without first erasing it is not supported.

9.2.2 SERIAL DATA INPUT (80h)

Page Program operation starts with the execution of the Serial Data Input command (80h) to the Command Register, following next by inputting four address cycles and then the data is loaded. Serial data is loaded to Cache Register with each #WE cycle. The Program command (10h) is written to the Command Register after the serial data input is finished. At this time the internal write state controller automatically executes the algorithms for program and verifies operations. Once the programming starts, determining the completion of the program process can be done by monitoring the RY/#BY output or the Status Register Bit 6, which will follow the RY/#BY signal. RY/#BY will stay LOW during the internal array programming operation during the period of (tPROG). During page program operation, only two commands are available, READ STATUS (70h) and RESET (FFh). When the device status goes to the ready state, Status Register Bit 0 (I/O0) indicates whether the program operation passed (Bit0=0) or failed (Bit0=1), (see Figure 9-10). The Command Register remains in read status mode until the next command is issued.

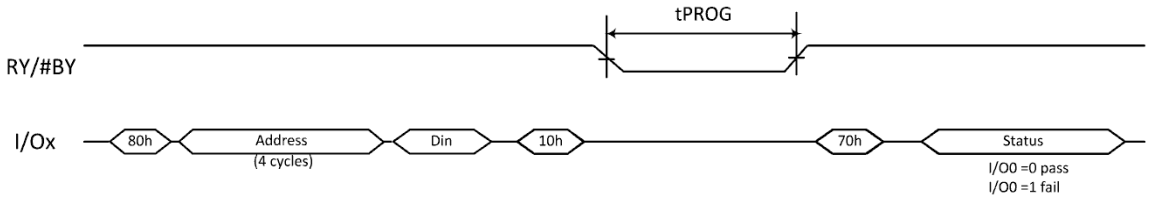


Figure 9-10 Page Program

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9.2.3 RANDOM DATA INPUT (85h)

After the Page Program (80h) execution of the initial data has been loaded into the Cache Register, if the need for additional writing of data is required, using the RANDOM DATA INPUT (85h) command can perform this function to a new column address prior to the Program (10h) command. The RANDOM Data INPUT command can be issued multiple times in the same page (See Figure 9-11).

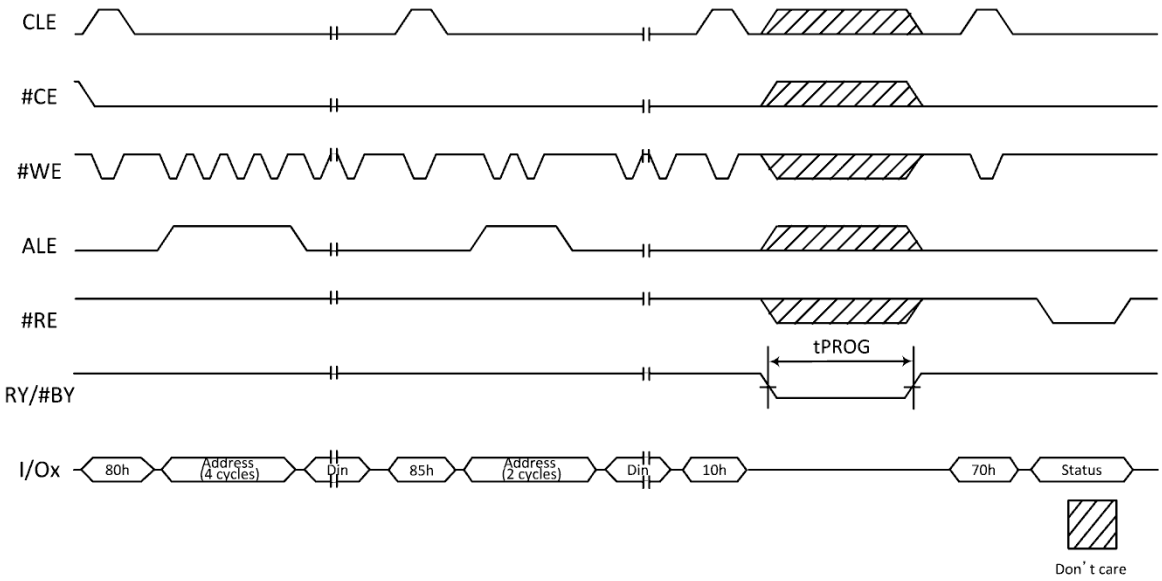


Figure 9-11 Random Data Input

9.2.4 CACHE PROGRAM (80h-15h)

CACHE PROGEAM (80h) command is started by writing the command to the Command Register. The next writes should be four cycles of address, and then either writing a full or partial page of input data into the Cache Register. Issuing the CACHE PROGRAM (15h) command to the Command Register, starting transferring data from the Cache Register to the Data Register on the rising edge of #WE and RY/#BY will go LOW. Programming to the array starts after the data has been copied into the Data Register and RY/#BY returns to HIGH.

When RY/#BY returns to HIGH, the next input data can be written to the Cache Register by issuing another CACHE PROGRAM command series. The time RY/#BY goes LOW, is typical controlled by the actual programming time. The time for the first programming pass equals the time it takes to transfer the data from the Cache Register to the Data Register. On the second and subsequent programming passes, data transfer from the Cache Register to the Data Register is held until Data Register content is programming into the NAND array.

The CACHE PROGRAM command can cross block address boundaries. RANDOM DATA INPUT (85h) commands are permitted with CACHE PROGRAM operations. Status Register's Cache RY/#BY Bit 6 (I/O6) can be read after issuing the READ STATUS (70h) command for confirming when the Cache Register is ready or busy. RY/#BY, always follows Status Register Bit 6 (I/O6). Status Register's RY/#BY Bit 5 (I/O5) can be polled to determine whether the array programming is in progress or completed for the current programming cycle.

If only RY/#BY is used for detecting programming status, the last page of the program sequence must use the PAGE PROGRAM (10h) command instead of the CACHE PROGRAM (15h) command. If the

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CACHE PROGRAM (15h) command is used every time, including the last page programming, Status Register's Bit 5 (I/O5) must be used to determine when programming is complete.

Status Register's Pass/Fail, Bit 0 (I/O0) returns the pass/fail status for the previous page when Status Register's Bit 6 (I/O6) equals a "1" (ready state). The pass/fail status of the current PROGRAM operation is returned with Status Register's Bit 0 (I/O0) when Bit 5 (I/O5) of the Status Register equals a "1" (ready state) as shown in Figure 9-12 and 9-13.

Note: The CACHE PROGRAM command cannot be used on blocks 0-3 if used as boot blocks.

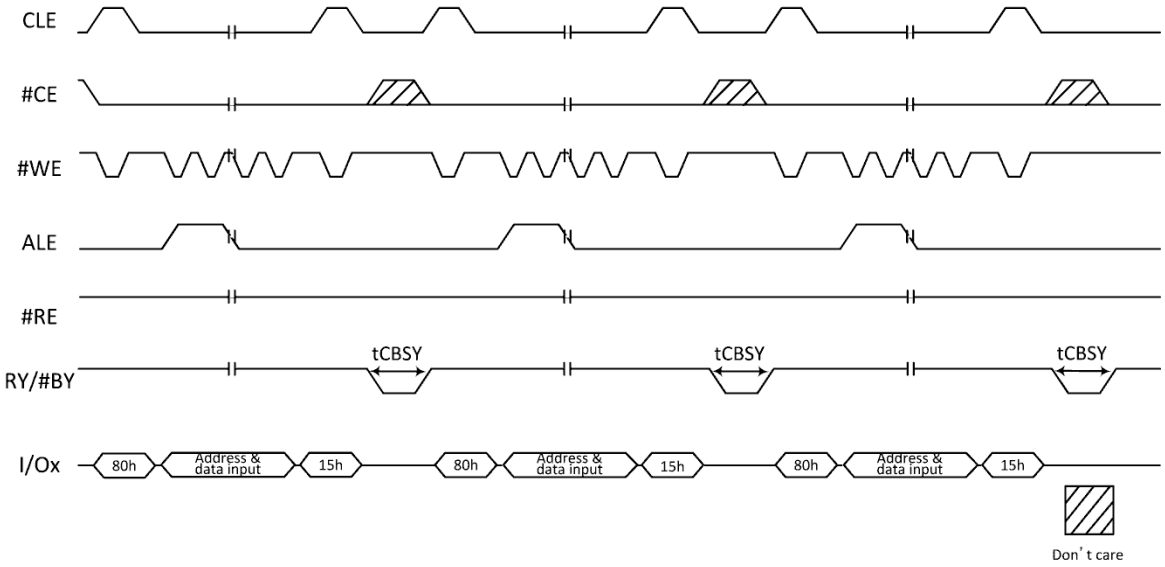


Figure 9-12 Cache Program Start

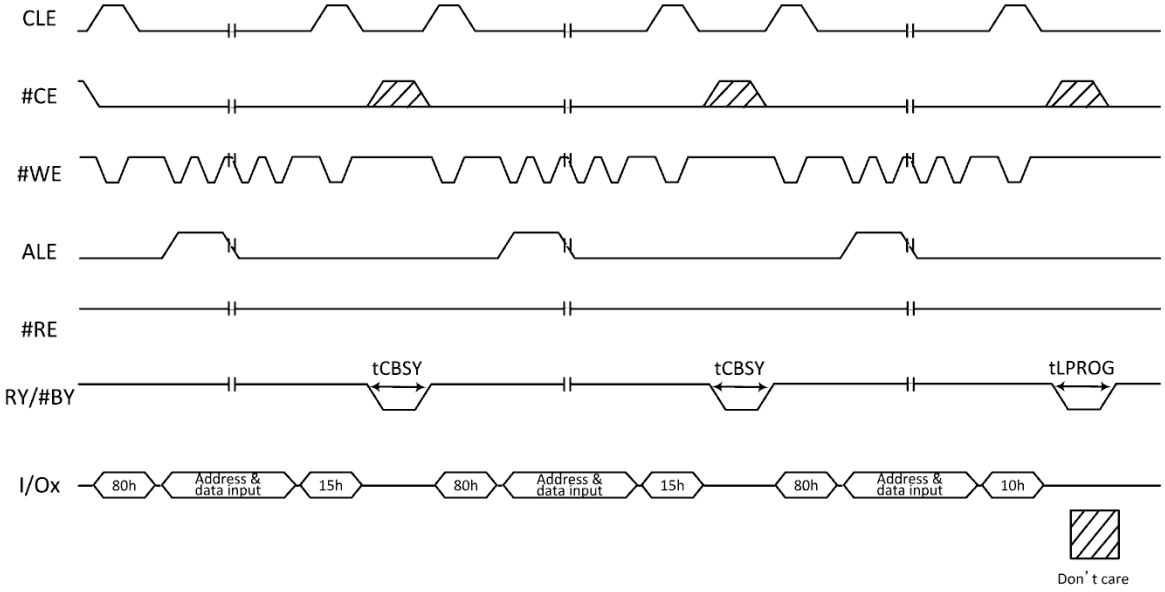


Figure 9-13 Cache Program End

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9.3 COPY BACK operation

Copy Back operations require two command sets. Issue a READ for COPY BACK (00h-35h) command first, then the PROGRAM for COPY BACK (85h-10h) command.

9.3.1 READ for COPY BACK (00h-35h)

The READ for COPY BACK command is used together with the PROGRAM for COPY BACK (85h-10h) command. To start execution, READ for COPY BACK (00h) command is written to the Command Register, followed by the four cycles of the source page address. To start the transfer of the selected page data from the memory array to the Cache Register, write the 35h command to the Command Register.

After execution of the READ for COPY BACK command sequence and RY/#BY returns to HIGH marking the completion of the operation, the transferred data from the source page into the Cache Register may be read out by toggling #RE. Data is output sequentially from the column address that was originally specified with the READ for COPY BACK command. RANDOM DATA OUTPUT (05h-E0h) commands can be issued multiple times without any limitation after READ for COPY BACK command has been executed (see Figures 9-14 and 9-15).

At this point the device is in ready state to accept the PROGRAM for COPY BACK command.

9.3.2 PROGRAM for COPY BACK (85h-10h)

After the READ for COPY BACK command operation has been completed and RY/#BY goes HIGH, the PROGRAM for COPY BACK command can be written to the Command Register. The command results in the transfer of data from the Cache Register to the Data Register, then internal operations start programming of the new destination page. The sequence would be, write 85h to the Command Register, followed by the four cycle destination page address to the NAND array. Next write the 10h command to the Command Register; this will signal the internal controller to automatically start to program the data to new destination page. During this programming time, RY/#BY will go LOW. The READ STATUS command can be used instead of the RY/#BY signal to determine when the program is complete. When Status Register Bit 6 (I/O6) equals to “1”, Status Register Bit 0 (I/O0) will indicate if the operation was successful or not.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for COPY BACK command for modifying the original data. Once the data is copied into the Cache Register using the READ for COPY BACK (00h-35h) command, follow by writing the RANDOM DATA INPUT (85h) command, along with the address of the data to be changed. The data to be changed is placed on the external data pins. This operation copies the data into the Cache Register. Once the 10h command is written to the Command Register, the original data and the modified data are transferred to the Data Register, and programming of the new page commences. The RANDOM DATA INPUT command can be issued numerous times without limitation, as necessary before starting the programming sequence with 10h command.

Since COPY BACK operations do not use external memory and the data of source page might include a bit errors, a competent ECC scheme should be developed to check the data before programming data to a new destination page.

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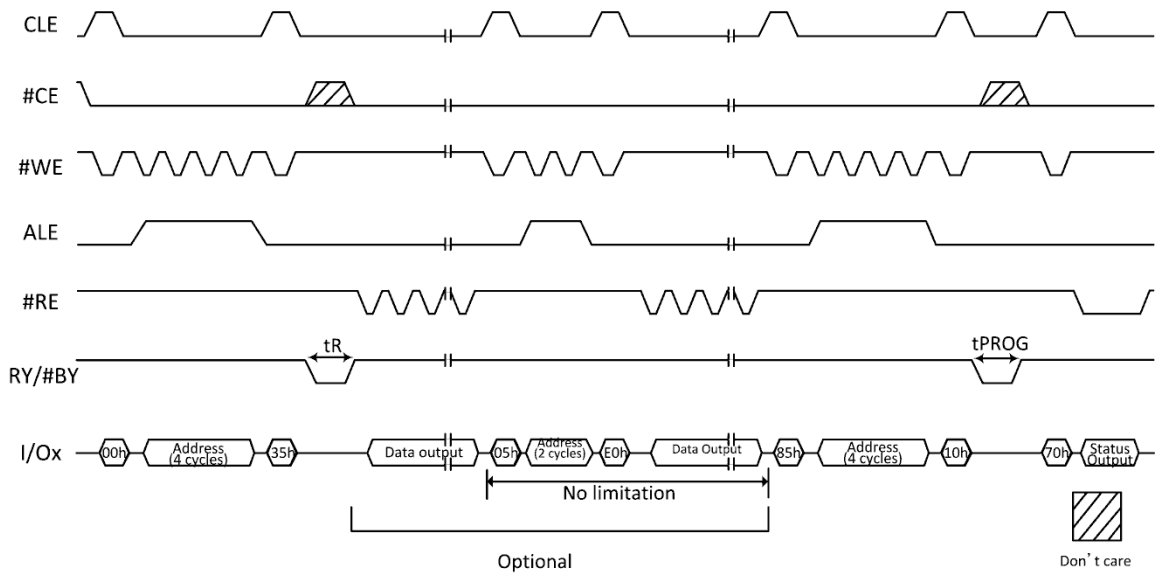


Figure 9-14 Copy Back Program Operation

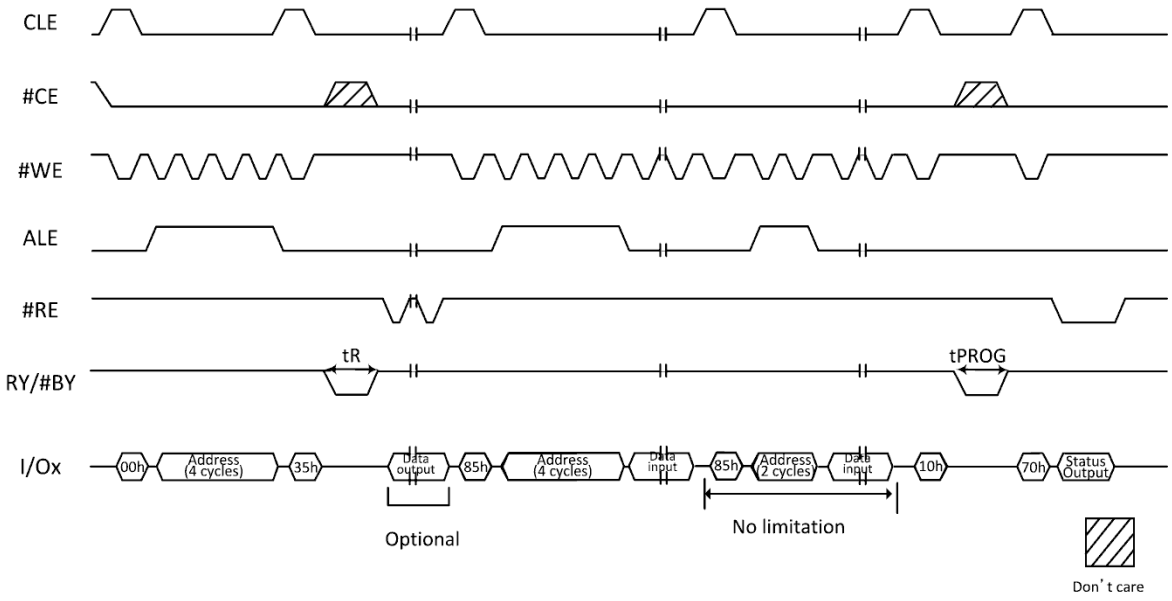


Figure 9-15 Copy Back Operation with Random Data Input

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9.4 BLOCK ERASE operation

9.4.1 BLOCK ERASE (60h-D0h)

Erase operations happen at the architectural block unit. This W29N01GZ/W has 1024 erase blocks. Each block is organized into 64 pages (2112 bytes/page,1056words/page), 132K bytes (128K + 4K bytes)/block,66Kwords(64K+2K words)/block The BLOCK ERASE command operates on a block by block basis.

Erase Setup command (60h) is written to the Command Register. Next, the two cycle block address is written to the device. The page address bits are loaded during address block address cycle, but are ignored. The Erase Confirm command (D0h) is written to the Command Register at the rising edge of #WE, RY/#BY goes LOW and the internal controller automatically handles the block erase sequence of operation. RY/#BY goes LOW during Block Erase internal operations for a period of tBERS,

The READ STATUS (70h) command can be used for confirm block erase status. When Status Register Bit6 (I/O6) becomes to “1”, block erase operation is finished. Status Register Bit0 (I/O0) will indicate a pass/fail condition (see Figure 9-16).

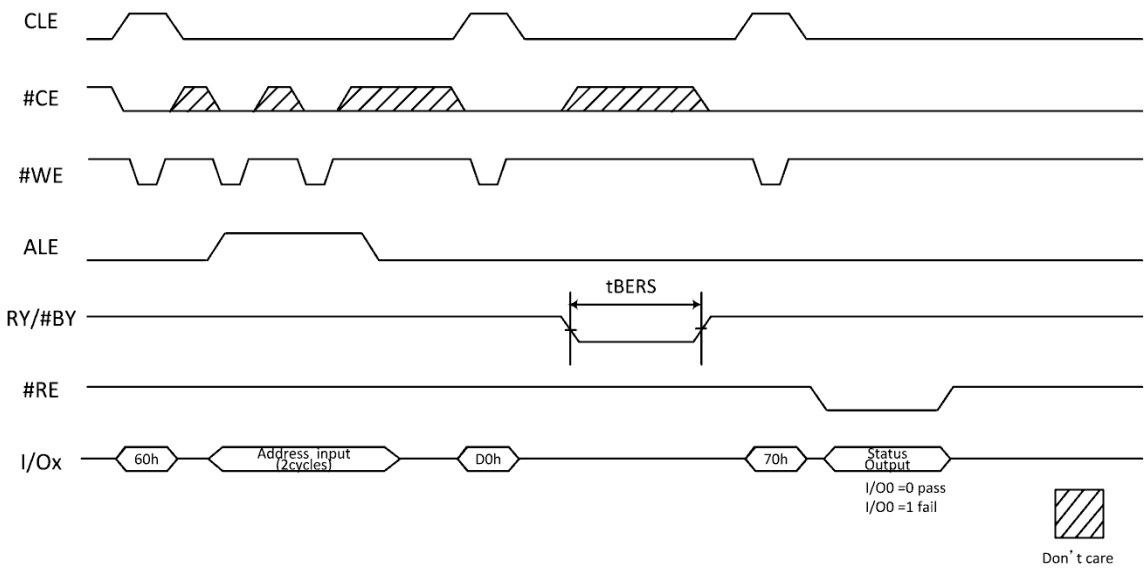


Figure 9-16 Block Erase Operation

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9.5 RESET operation

9.5.1 RESET (FFh)

READ, PROGRAM, and ERASE commands can be aborted by the RESET (FFh) command during the time the W29N01GZ/W is in the busy state. The Reset operation puts the device into a known status. The data that is processed in either the programming or erasing operations are no longer valid. This means the data can be partially programmed or erased and therefore data is invalid. The Command Register is cleared and is ready to accept next command. The Data Register and Cache Register contents are marked invalid.

The Status Register indicates a value of E0h when #WP is HIGH; otherwise a value of 60h when #WP is LOW. After RESET command is written to the command register, RY/#BY goes LOW for a period of tRST (see Figure 9-17).

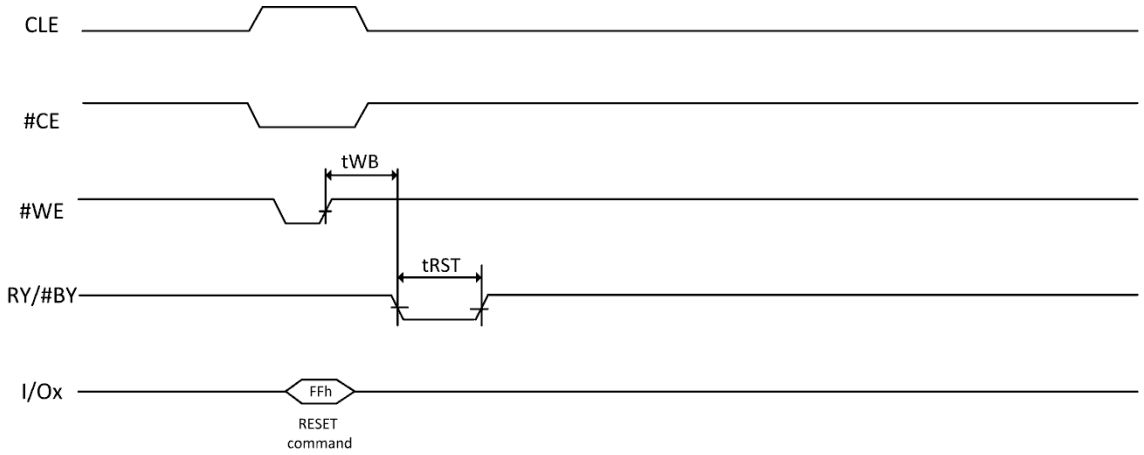


Figure 9-17 Reset Operation

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9.6 FEATURE OPERATION

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to change the NAND Flash device behavior from the default power on settings. These commands use a one-byte feature address to determine which feature is to be read or modified. A range of 0 to 255 defines all features; each is described in the features table (see Table 9.4 thru 9.7). The GET FEATURES (EEh) command reads 4-Byte parameter in the features table (See GET FEATURES function). The SET FEATURES (EFh) command places the 4-Byte parameter in the features table (See SET FEATURES function).When a feature set is volatile, meaning it remains active by default until the device is powered off. The set feature remains the set even if a RESET (FFh) command is issued.

Feature address	Description
00h	N.A
01h	Timing mode
02h-7Fh	Reserved
80h	Vendor specific parameter : Programmable I/O drive strength
81h	Vendor specific parameter : Programmable RY/#BY pull-down strength
82h-FFh	Reserved

Table 9-5 Features

Feature Address 01h: Timing Mode

Sub feature parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Timing mode	Mode 0 (default)	Reserved (0)					0	0	0	00h	1
	Mode 1	Reserved (0)					0	0	1	01h	1
	Mode 2	Reserved (0)					0	1	0	02h	1
	Mode 3	Reserved (0)					0	1	1	03h	2
	Mode 4	Reserved (0)					1	0	0	04h	2
	Mode 5	Reserved (0)					1	0	1	05h	2
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Table 9-6 Feature Address 01h

Notes:

1. **Timing mode is set to mode 0 by default. The timing mode should be selected to indicate the maximum speed at which the device will receive addresses, commands, and data cycles. The five supported settings for the timing mode are shown. The device returns to mode 0 when a power cycle has occurred. Supported timing modes are reported in the parameter page.**
2. **Not supported.**

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Feature Address 80h: Programmable I/O Drive Strength

Sub feature parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Table 9-7 Feature Address 80h

Note:

1. **The default drive strength setting is Full strength. The Programmable I/O Drive Strength mode is used to change from the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive-strength settings. The device returns to the default drive strength mode when a power cycle has occurred. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.**

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Feature Address 81h: Programmable RY/#BY Pull-down Strength

Sub feature parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
RY/#BY pull-down strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Table 9-8 Feature Address 81h

Note:

1. **The default programmable RY/#BY pull-down strength is set to Full strength. The pull-down strength is used to change the RY/#BY pull-down strength. RY/#BY pull-down strength should be selected based on expected loading of RY/#BY. The four supported pull-down strength settings are shown. The device returns to the default pull-down strength when a power cycle has occurred.**

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9.6.1 GET FEATURES (EEh)

The GET FEATURES command returns the device feature settings including those previously set by the SET FEATURES command. To use the Get Feature mode write the command (EEh) to the Command Register followed by the single cycle byte Feature Address. RY/#BY will goes LOW for the period of tFEAT. If Read Status (70h) command is issued for monitoring the process completion status, Read Command (00h) has to be executed to re-establish data output mode. Once, RY/#BY goes HIGH, the device feature settings can be read by toggling #RE. The device remains in Feature Mode until another valid command is issued to Command Register. See Figure 9-18.

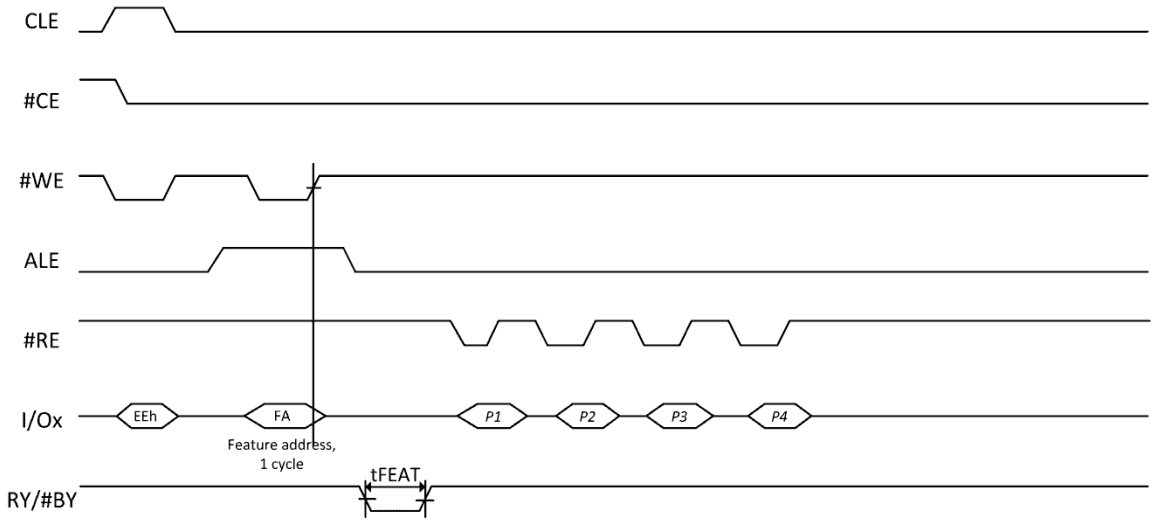


Figure 9-18 Get Feature Operation

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9.6.2 SET FEATURES (EFh)

The SET FEATURES command sets the behavior parameters by selecting a specified feature address. To change device behavioral parameters, execute Set Feature command by writing EFh to the Command Register, followed by the single cycle feature address. Each feature parameter (P0-P3) is latched at the rising edge of each #WE. The RY/#BY signal will go LOW during the period of tFEAT while the four feature parameters are stored. The Read Status (70h) command can be issued for monitoring the progress status of this operation. The parameters are stored in device until the device goes through a power on cycle. The device remains in feature mode until another valid command is issued to Command Register.

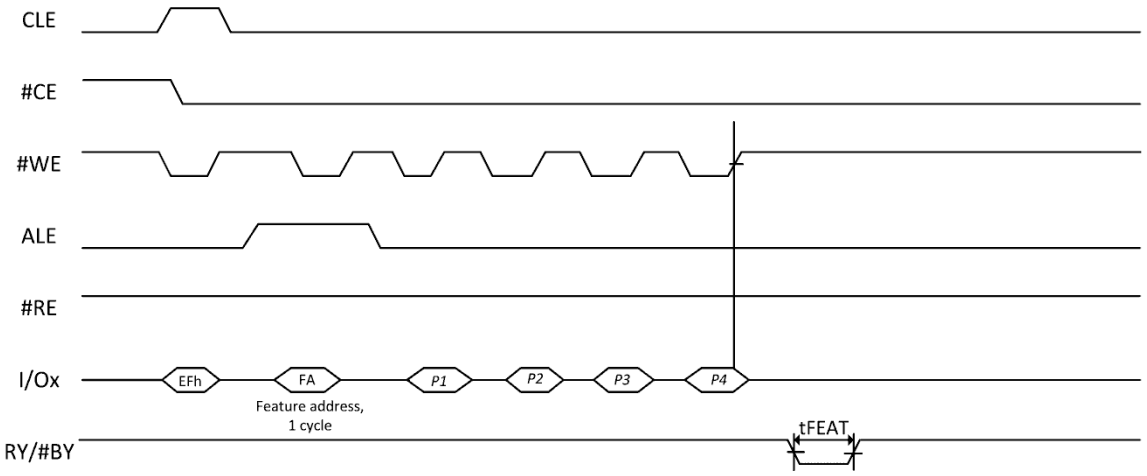


Figure 9-19 Set Feature Operation

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9.7 ONE TIME PROGRAMMABLE (OTP) area

The device has One-Time Programmable (OTP) memory area comprised of ten pages (2112 bytes/page). This entire range of pages is functionally guaranteed. Only the OTP commands can access the OTP area. When the device ships from Winbond, the OTP area is in an erase state (all bits equal “1”). In the OTP area, programming or partial-page programming is done only by programming “0” bits. The OTP area cannot be erased, therefore protecting the area only prevent further programming.

OTP area programming and protection have two separate commands. The OTP DATA PROGRAM (A0h-10h) command is used to program an OTP page. Programming an entire page as one operation or up to four partial-page programming sequences is available. Programming other OTP pages can be done in the same way. The OTP DATA PROTECT (A5h-10h) command will permanently protected the OTP area from further programming operations. The OTP DATA READ command (AFh-30h) can read the OTP area with or without protection set. Note; there is no erase command for OTP area.

9.7.1 OTP DATA PROGRAM (A0h-10h)

Programming the OTP area can be done using the OTP DATA PROGRAM (A0h-10h) command. An entire page can be programmed at once or up to four partial page programming sequences per page.

This command enables programming into the offset of an OTP page by using the two bytes of Column Address [11:0]. If OTP area is protected by OTP DATA PROTECT command, the programming the OTP area will not be executed, and RY/#BY goes LOW for a period of tOBSY.

To use this command sequence, the A0h command is written to Command Register. Then issue the four address cycles that are column address of first two cycles and range page address[0B:02] of the two remaining cycles. Then write 1 to 2112 bytes of data, followed by program confirmation command (10h) is written to Command Register. At this point the internal controller automatically executes the algorithms for program and verify. The RY/#BY will go LOW during the program execution for the period of (tPROG). Program verification only detects 1’s that are not successfully programmed to 0’s.

If OTP area is not protected, RANDOM DATA INPUT commands can be used during OTP program operations.

READ STATUS (70h) command is valid during the OTP program operation. For this operation, Status Register Bit5 and Bit6 (I/O5 and I/O6, respectively) will follow same state as RY/#BY. If the OTP area is protected, Status Register Bit7 (I/O7) will equal “0”; otherwise it is a “1”. After the device is in the ready state, Status Register Bit0 (I/O0) indicates whether the operation passed or failed.

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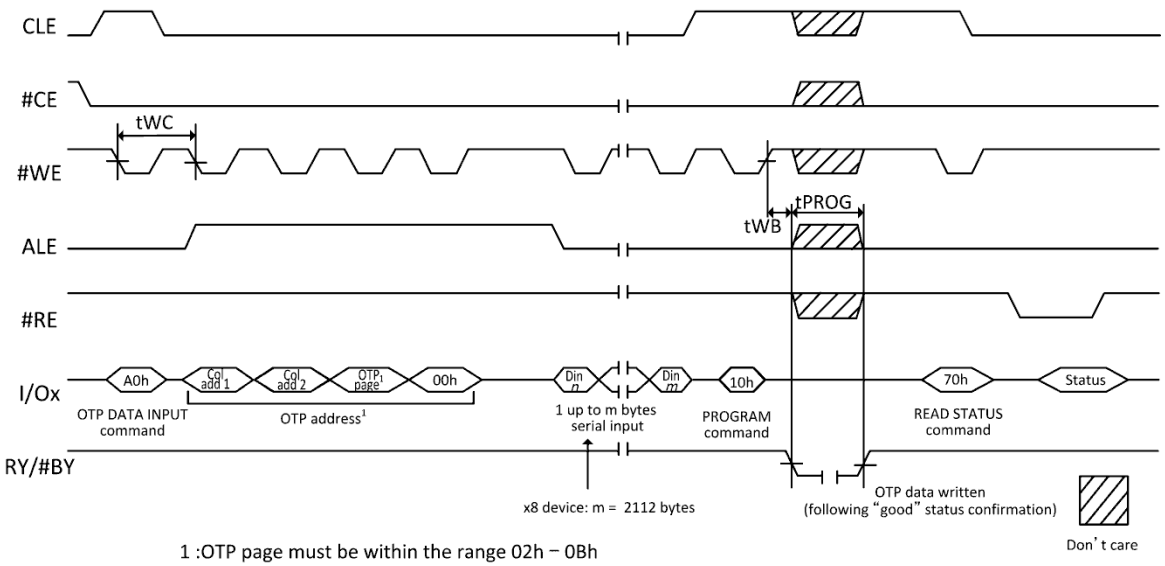


Figure 9-20 OTP Data Program

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9.7.2 OTP DATA PROTECT (A5h-10h)

To protect the data in OTP area used the OTP DATA PROTECT (A5h-10h) command. After the OTP area is protected, the OTP area cannot be unprotected and no additional data can be programmed to the OTP area.

To use this command, A5h is written to the Command Register. Then issues the four address cycles with the following address code: 00h-00h-01h-00h. Finalized by writing the protect confirmation command (10h) to the Command Register. The RY/#BY signal will go LOW during this protection process, a period similar with page program time (tPROG).

READ STATUS (70h) command is valid during the OTP protect operation. For this operation, Status Register Bit5 and Bit6 (I/O5 and I/O6, respectively) will indicate same state as the RY/#BY. After the device go to the ready state, Status Register Bit0 (I/O0) indicates whether the operation passed or failed.

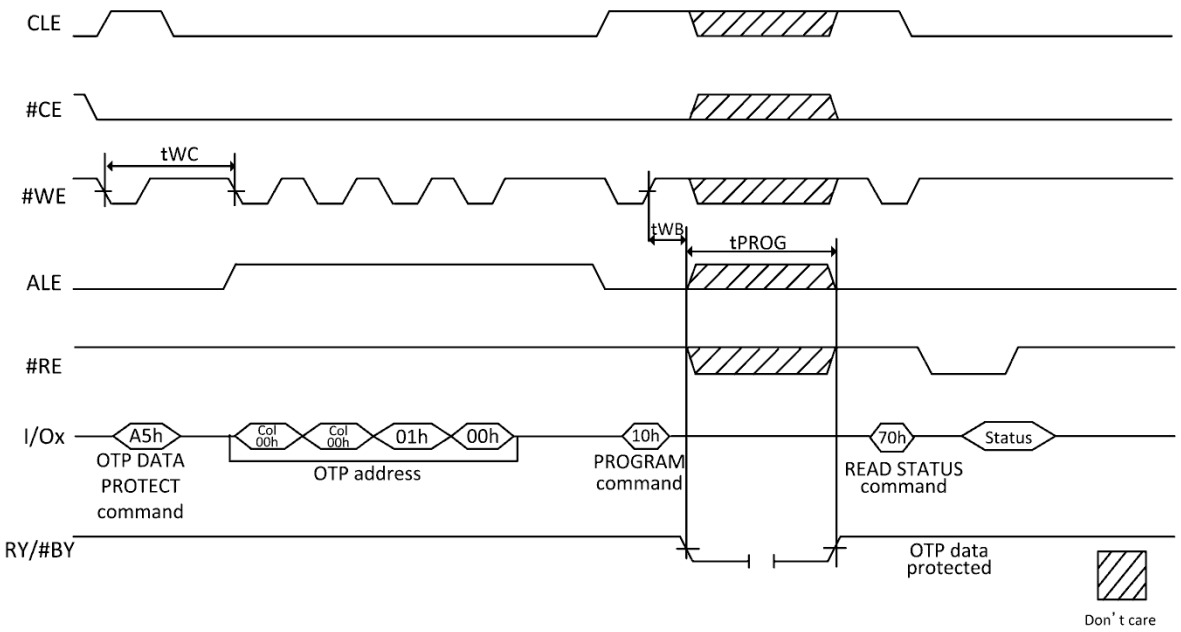


Figure 9-21 OTP Data Protect

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9.7.3 OTP DATA READ (AFh-30h)

This command can read the data from OTP pages. The read capability from OTP area is available with or without OTP area protection.

To use this command sequence, AFh command is written to Command Register. Then issue four address cycles comprised of the column address (first two cycles) and the range page address [0B:02] for the remaining two cycles. Once the address is written, perform the read confirmation command (30h) to the Command Register. The RY/#BY signal will go LOW while the OTP data is transferred from OTP area to Data Register during the period of (tR). The RANDOM DATA OUTPUT command can use during OTP data read operations. Read timing of OTP data read is the same as the typical PAGE READ timing.

READ STATUS and RESET command are valid during OTP data read operation. For this operation, Status Register Bit5 and Bit6 (I/O5 and I/O6, respectively) indicate the same as the RY/#BY signal. Additional OTP pages can be read by repeating OTP DATA READ command.

If OTP DATA READ command is followed by CACHE READ operation, the RESET command has to be executed prior to issuing the CACHE READ commands. RESET time can be up to 5µs.

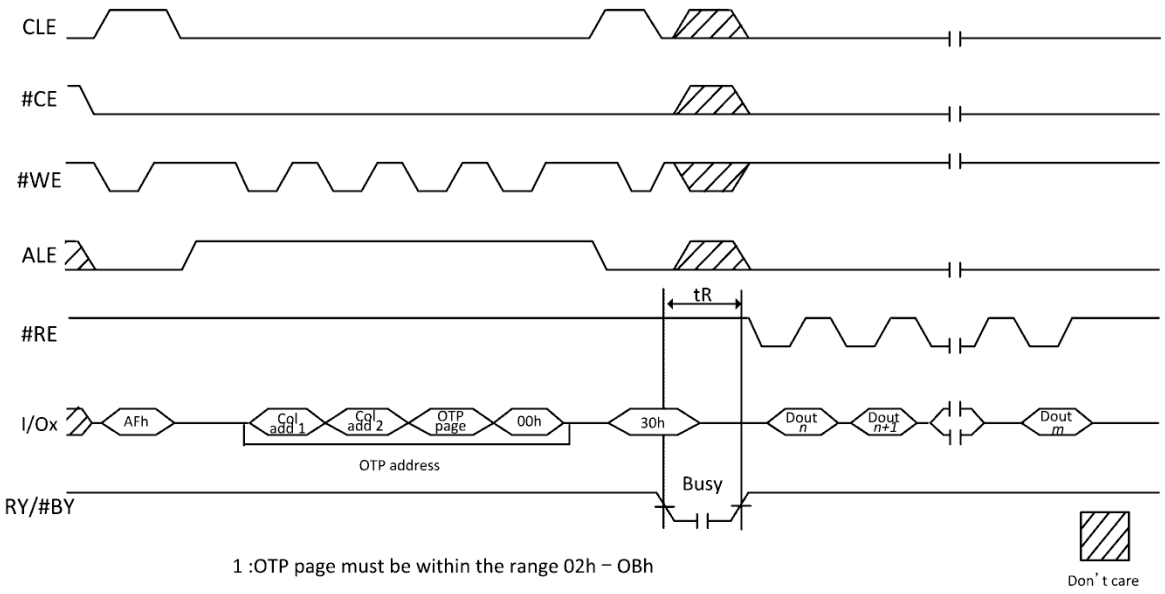


Figure 9-22 OTP Data Read

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9.8 WRITE PROTECT

#WP pin can enable or disable program and erase commands preventing or allowing program and erase operations. Figure 9-23 to 9-28 shows the enabling or disabling timing with #WP setup time (tWW) that is from rising or falling edge of #WP to latch the first commands. After first command is latched, #WP pin must not toggle until the command operation is complete and the device is in the ready state. (Status Register Bit5 (I/O5) equal 1.

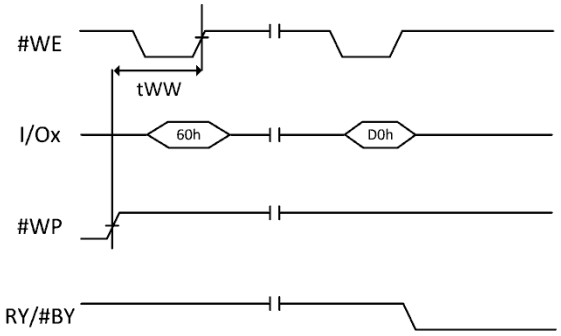


Figure 9-23 Erase Enable

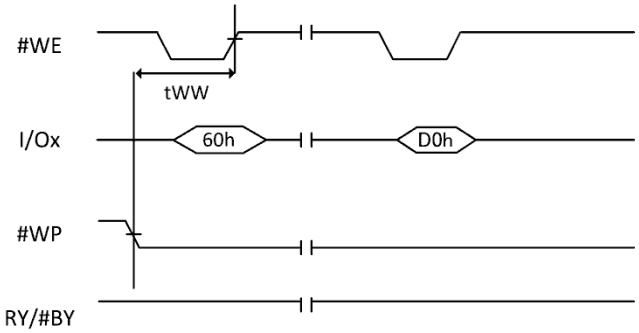


Figure 9-24 Erase Disable

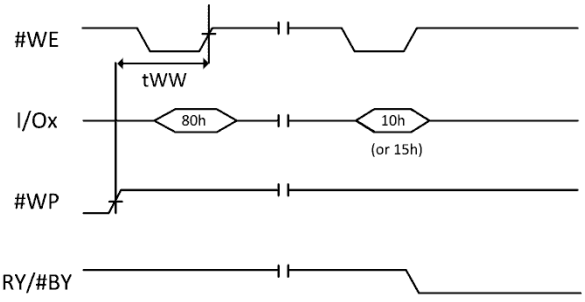


Figure 9-25 Program Enable

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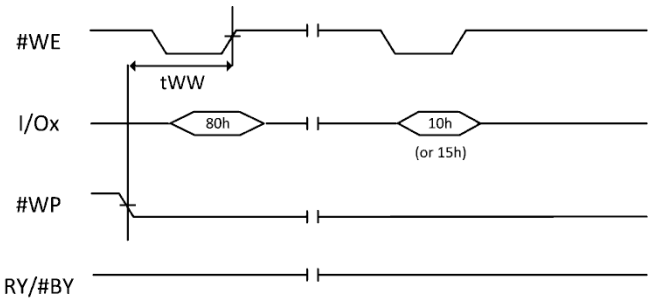


Figure 9-26 Program Disable

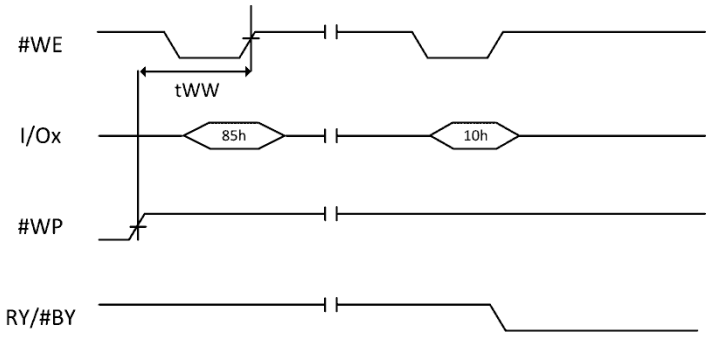


Figure 9-27 Program for Copy Back Enable

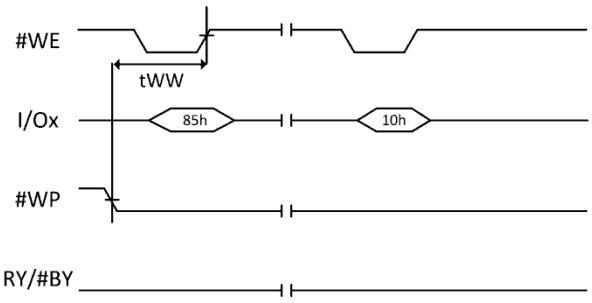


Figure 9-28 Program for Copy Back Disable

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9.9 BLOCK LOCK

The device has block lock feature that can protect the entire device or user can indicate a ranges of blocks from program and erase operations. Using this feature offers increased functionality and flexibility data protection to prevent unexpected program and erase operations. Contact to Winbond for using this feature.

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10. ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +2.4	V
Voltage Applied to Any Pin	VIN	Relative to Ground	–0.6 to +2.4	V
Storage Temperature	TSTG		–65 to +150	°C
Short circuit output current, I/Os			5	mA

Table 10-1 Absolute Maximum Ratings

Notes:

1. **Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.**
2. **Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.**
3. **This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.**

10.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC		1.7	1.95	V
Ambient Temperature, Operating	TA	Industrial	-40	+85	°C

Table 10-2 Operating Ranges

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10.3 Device power-up timing

The device is designed to avoid unexpected program/erase operations during power transitions. When the device is powered on, the system has to wait until the ready state. #WP is recommended to VIL for preventing unexpected Program and Erase operations during power-transition until Vcc is stable. The RY/#BY will become valid after 50µs from the Vcc ramp start, and at least 10µs after Vcc reaches minimum Vcc level. The first command has to be a RESET command after the device is powered on. Before issuing RESET command, the system has to wait until the RY/#BY goes HIGH, or wait at least 100µs after Vcc reaches minimum Vcc. After issuing the RESET command, the busy time is 1ms maximum. RY/#BY polling or READ STATUS command can monitor the reset busy period. After completing this procedure, the device is initialized and ready for the operation (See Figure 10-1).

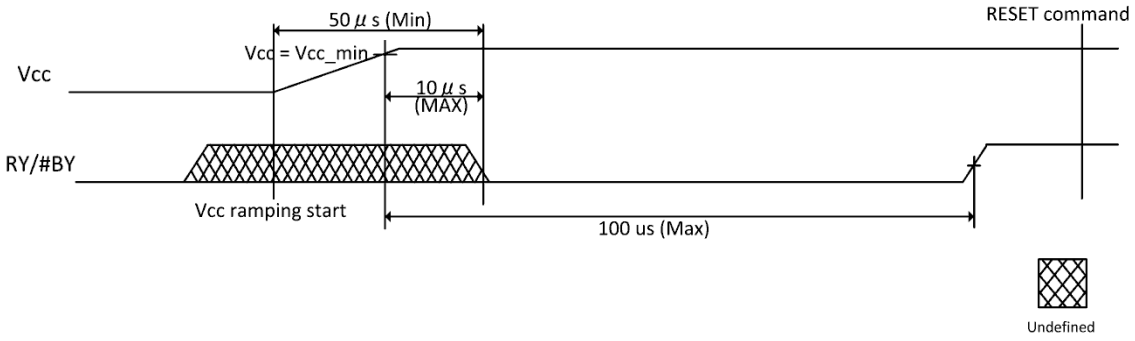


Figure 10-1 RY/#BY Behavior During Power-On

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10.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	

Sequential Read current	Icc1	tRC= tRC MIN
		#CE=VIL
		IOUT=0mA
			-	10	25	mA

Program current	Icc2	-	-	10	25	mA
Erase current	Icc3	-	-	10	25	mA
Standby current (TTL)	ISB1	#CE=VIH #WP=0V/Vcc	-	-	1	mA
Standby current (CMOS)	ISB2	#CE=Vcc – 0.2V #WP=0V/Vcc	-	10	50	µA
Input leakage current	ILI	VIN= 0 V to Vcc	-	-	±10	µA
Output leakage current	ILO	VOUT=0V to Vcc	-	-	±10	µA
Input high voltage	VIH	I/O7~0, #CE,#WE,#RE, #WP,CLE,ALE	0.8 x Vcc	-	Vcc + 0.3	V
Input low voltage	VIL	-	-0.3	-	0.2 x Vcc	V
Output high voltage(1)	VOH	IOH=--100µA	Vcc-0.1	-	-	V
Output low voltage(1)	VOL	IOL=100µA	-	-	0.1	V
Output low current	IOL(RY/#BY)	VOL=0.2V	3	4		mA

Table 10-3 DC Electrical Characteristics

Note:

1. **VOH and VOL may need to be relaxed if I/O drive strength is not set to full.**
2. **IOL (RY/#BY) may need to be relaxed if RY/#BY pull-down strength is not set to full**

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10.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Input Capacitance(1), (2)	CIN	-	10	pF
Input/Output Capacitance(1), (2)	CIO	-	10	pF
Input Rise and Fall Times	TR/TF	-	2.5	ns
Input Pulse Voltages	-	0 to VCC		V
Input/Output timing Voltage	-	Vcc/2		V
Output load (1)	CL	1TTL GATE and CL=30pF		-

Table 10-4 AC Measurement Conditions

Notes:

1. **Verified on device characterization , not 100% tested**
2. **Test conditions TA=25'C, f=1MHz, VIN=0V**

10.6 AC timing characteristics for Command, Address and Data Input

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
ALE to Data Loading Time	tADL	100	-	ns
ALE Hold Time	tALH	10	-	ns
ALE setup Time	tALS	15	-	ns
#CE Hold Time	tCH	10	-	ns
CLE Hold Time	tCLH	5	-	ns
CLE setup Time	tCLS	15	-	ns
#CE setup Time	tCS	25	-	ns
Data Hold Time	tDH	5	-	ns
Data setup Time	tDS	15	-	ns
Write Cycle Time	tWC	25	-	ns
#WE High Hold Time	tWH	15	-	ns
#WE Pulse Width	tWP	17	-	ns
#WP setup Time	tWW	100	-	ns

Table 10-5 AC timing characteristics for Command, Address and Data Input

Note:

1. **tADL is the time from the #WE rising edge of final address cycle to the #WE rising edge of first data cycle.**

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10.7 AC timing characteristics for Operation

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
ALE to #RE Delay	tAR	10	-	ns
#CE Access Time	tCEA	-	30	ns
#CE HIGH to Output High-Z(1)	tCHZ	-	45	ns
CLE to #RE Delay	tCLR	10	-	ns
#CE HIGH to Output Hold	tCOH	15	-	ns
Cache Busy in Cache Read mode	tRCBSY	3	tR	µs
Output High-Z to #RE LOW	tIR	0	-	ns
Data Transfer from Cell to Data Register	tR	-	25	µs
READ Cycle Time	tRC	35	-	ns
#RE Access Time	tREA	-	25	ns
#RE HIGH Hold Time	tREH	15	-	ns
#RE HIGH to Output Hold	tRHOH	15	-	ns
#RE HIGH to #WE LOW	tRHW	100	-	ns
#RE HIGH to Output High-Z(1)	tRHZ	-	100	ns
#RE LOW to output hold	tRLOH	5	-	ns
#RE Pulse Width	tRP	17	-	ns
Ready to #RE LOW	tRR	20	-	ns
Reset Time (READ/PROGRAM/ERASE)(2)	tRST	-	5/10/500	µs
#WE HIGH to Busy(3)	tWB	-	100	ns
#WE HIGH to #RE LOW	tWHR	80	-	ns

Table 10-6 AC timing characteristics for Operation

Notes: AC characteristics may need to be relaxed if I/O drive strength is not set to "full."

1. **Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 % tested**
2. **The first time the RESET (FFh) command is issued while the device is idle, the device will go busy for a maximum of 1ms. Thereafter, the device goes busy for a maximum of 5 μs.**
3. **Do not issue new command during tWB, even if RY/#BY is ready.**

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10.8 Program and Erase Characteristics

PARAMETER	SYMBOL	SPEC		UNIT
		TYP	MAX	
Number of partial page programs	NoP	-	4	cycles
Page Program time	tPROG	300	700	µs
Busy Time for Cache program (1)	tCBSY	3	700	µs
Busy Time for SET FEATURES /GET FEATURES	tFEAT	-	1	µs
Busy Time for program/erase at locked block	tLBSY	-	3	µs
Busy Time for OTP program when OTP is protected	tOBSY	-	30	µs
Block Erase Time	tBERS	2	10	ms
Last Page Program time (2)	tLPROG	-	-	-

Table 10-7 Program and Erase Characteristics

Note:

1. **tCBSY maximum time depends on timing between internal program complete and data-in.**
2. **tLPROG = Last Page program time (tPROG) + Last -1 Page program time (tPROG) – Last page Address, Command and Data load time.**

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11. TIMING DIAGRAMS

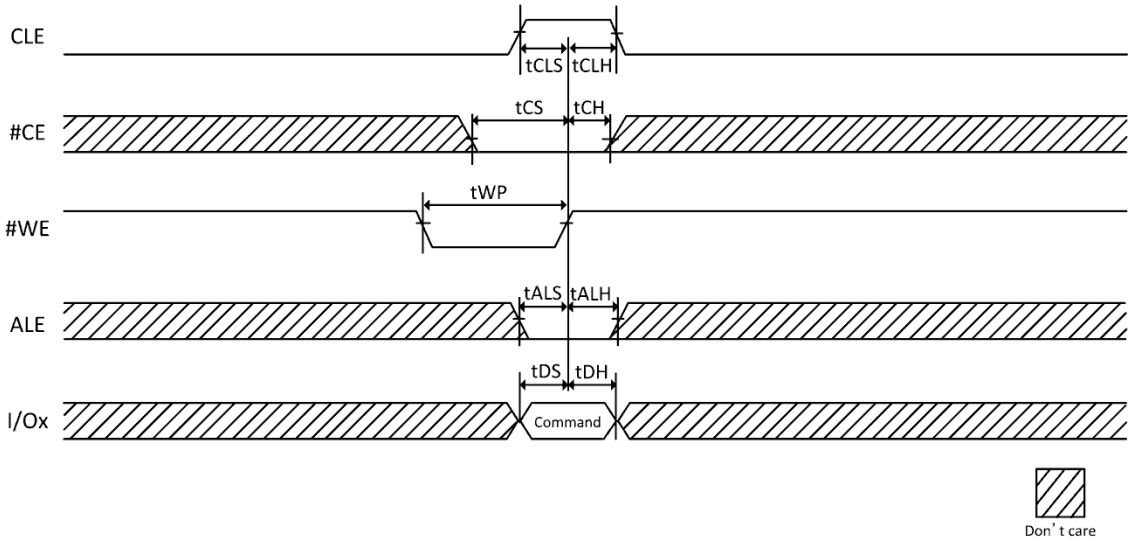


Figure 11-1 Command Latch Cycle

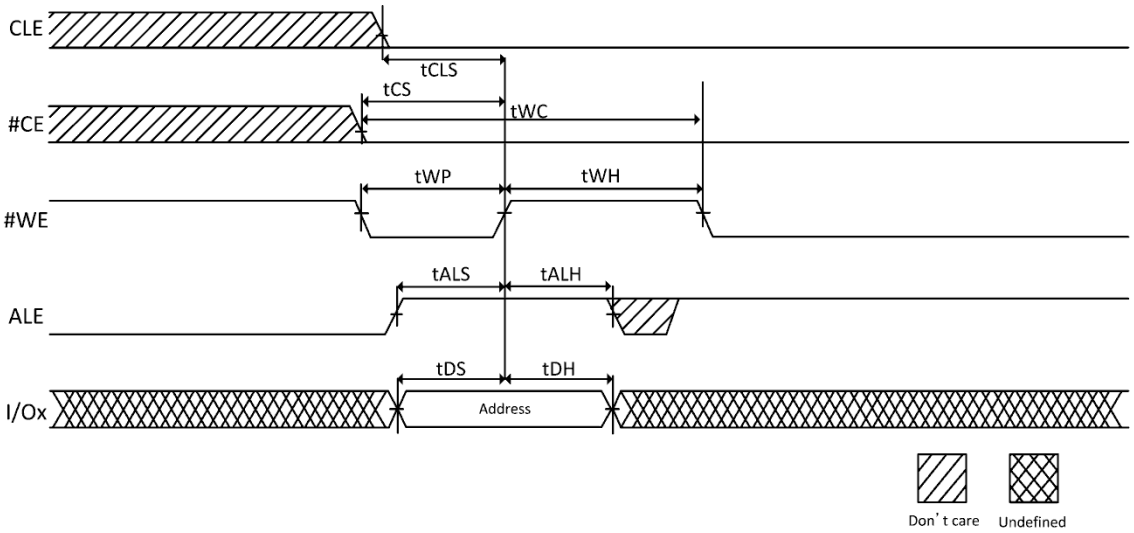


Figure 11-2 Address Latch Cycle

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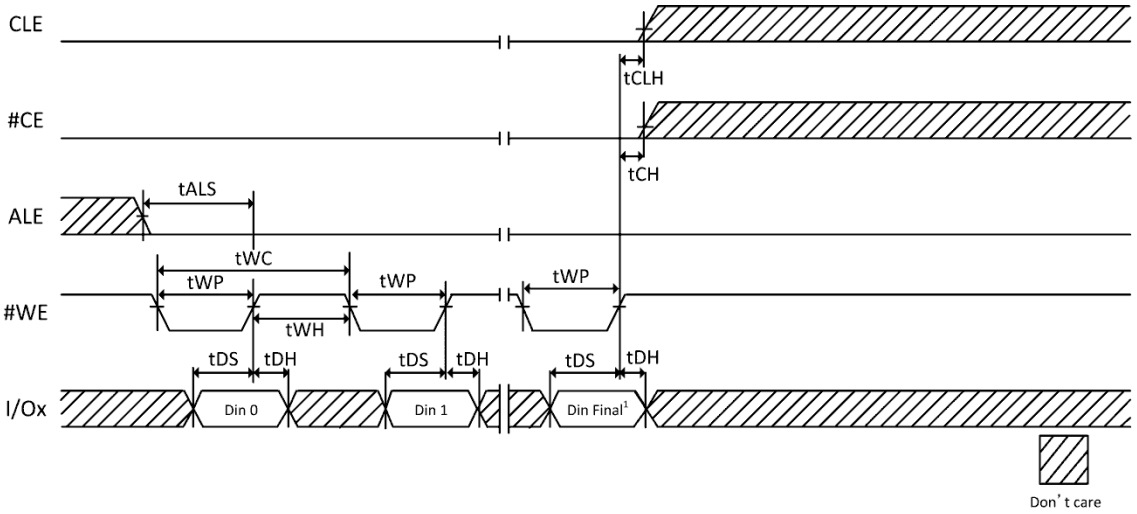


Figure 11-3 Data Latch Cycle

Note:

1. **Din Final = 2,111(x8)**

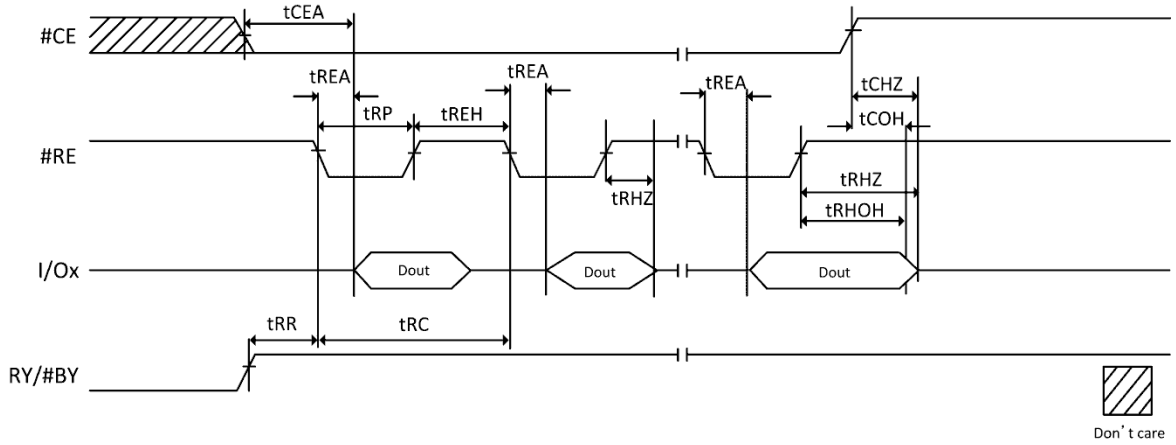


Figure 11-4 Serial Access Cycle after Read

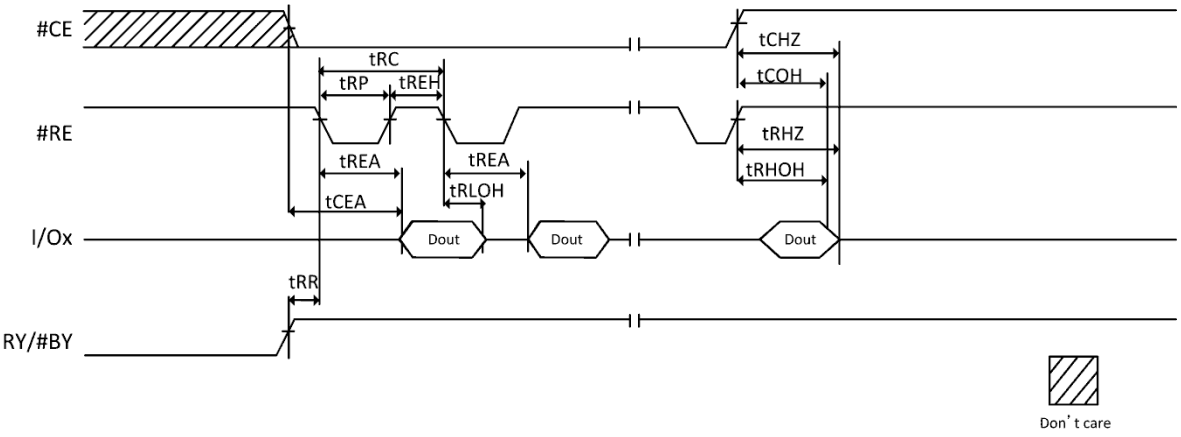


Figure 11-5 Serial Access Cycle after Read (EDO)

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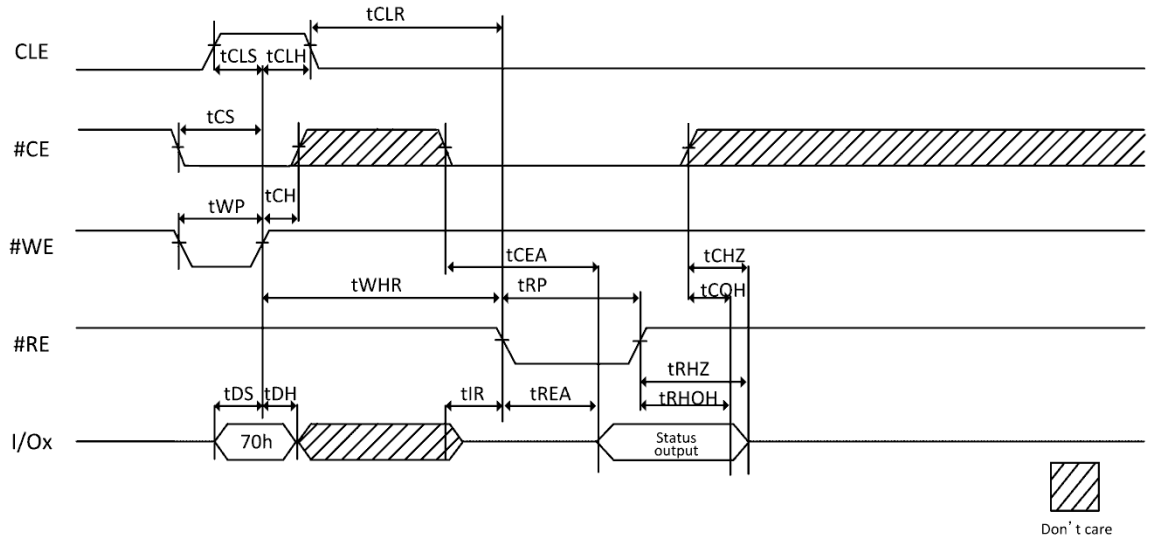


Figure 11-6 Read Status Operation

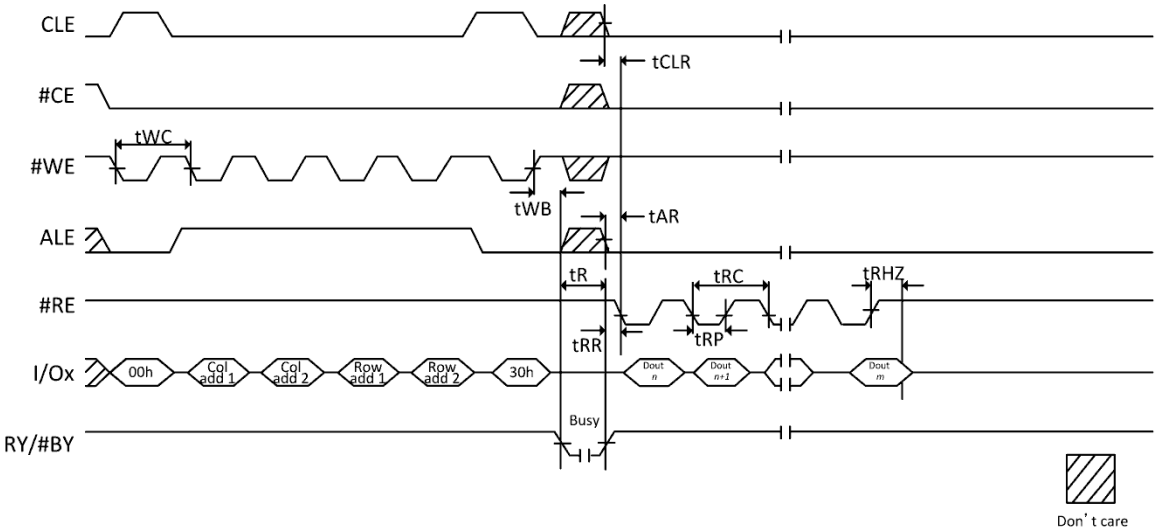


Figure 11-7 Page Read Operation

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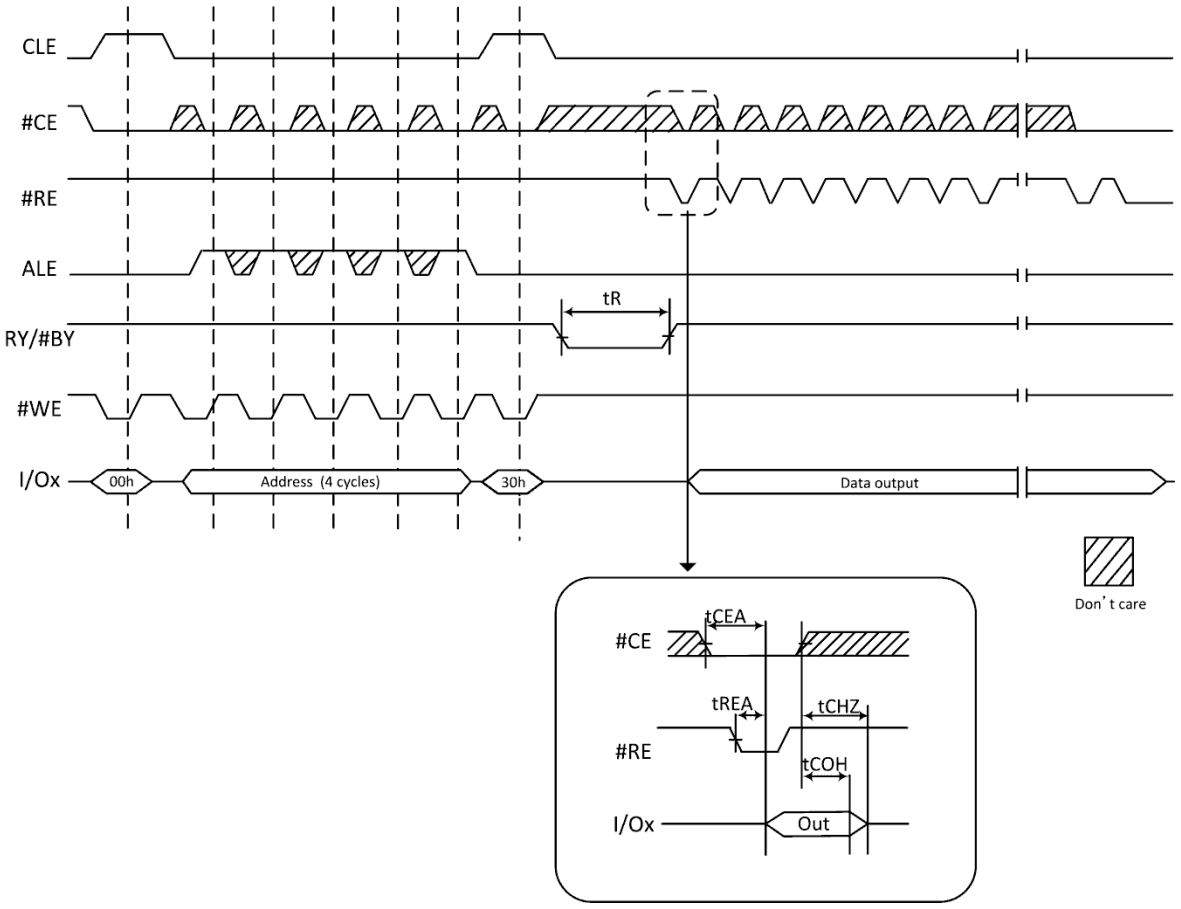


Figure 11-8 #CE Don't Care Read Operation

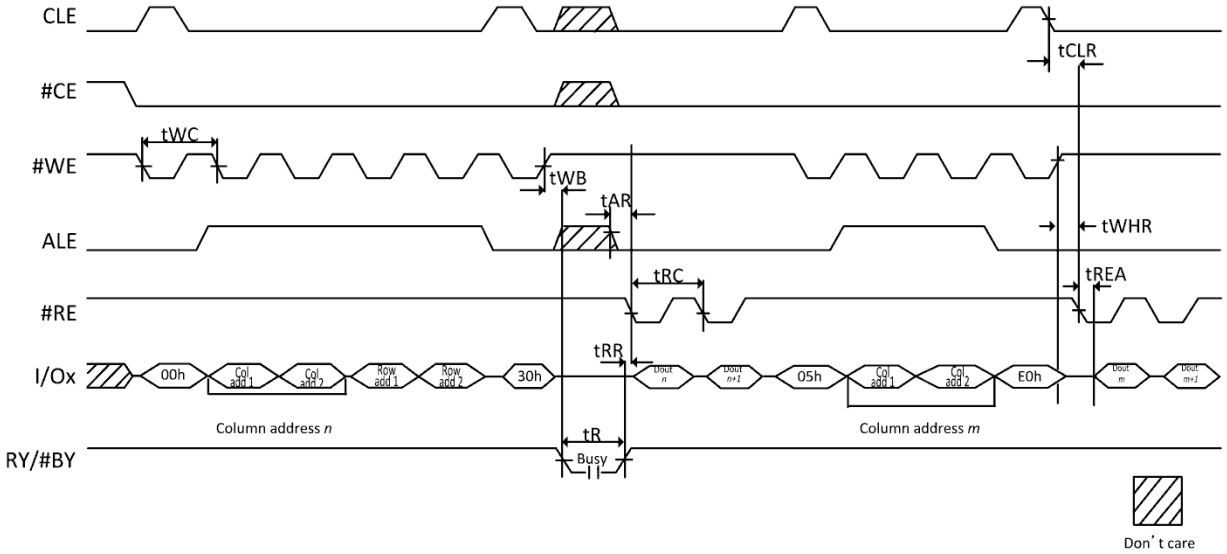


Figure 11-9 Random Data Output Operation

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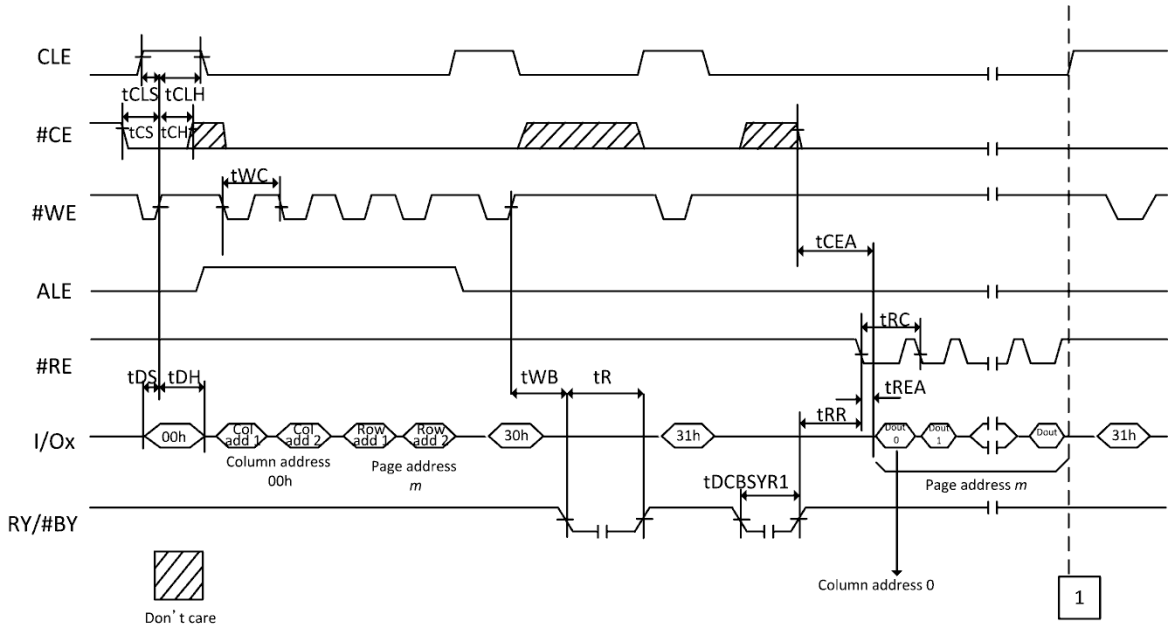


Figure 11-10 Cache Read Operation (1/2)

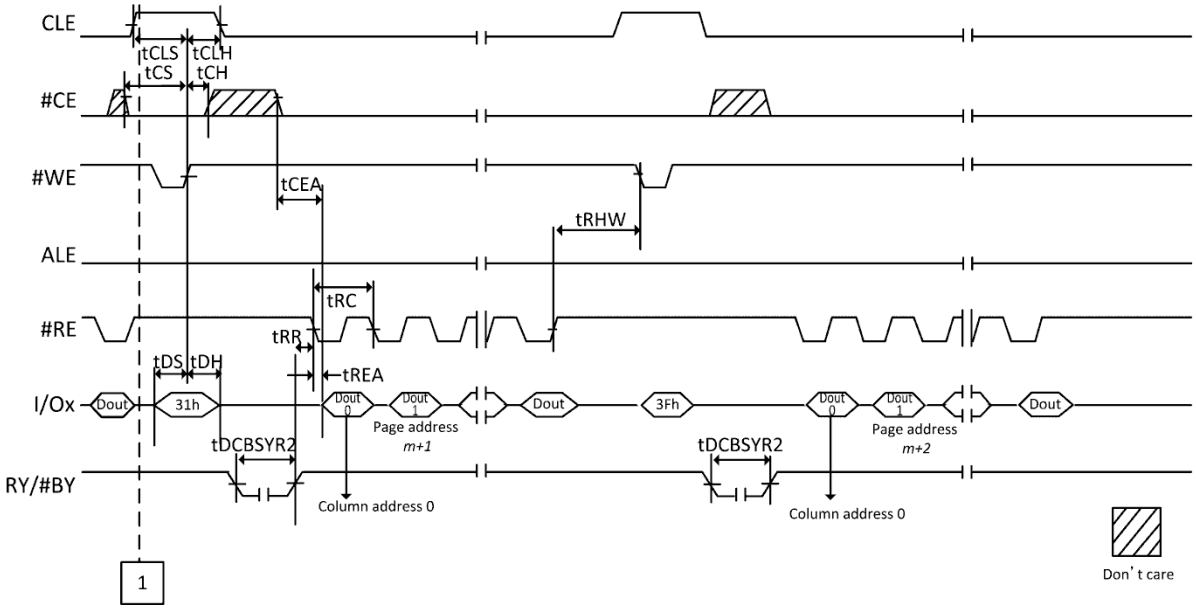


Figure 11-11 Cache Read Operation (2/2)

Note:

1. **See Table 9.1 for actual value.**

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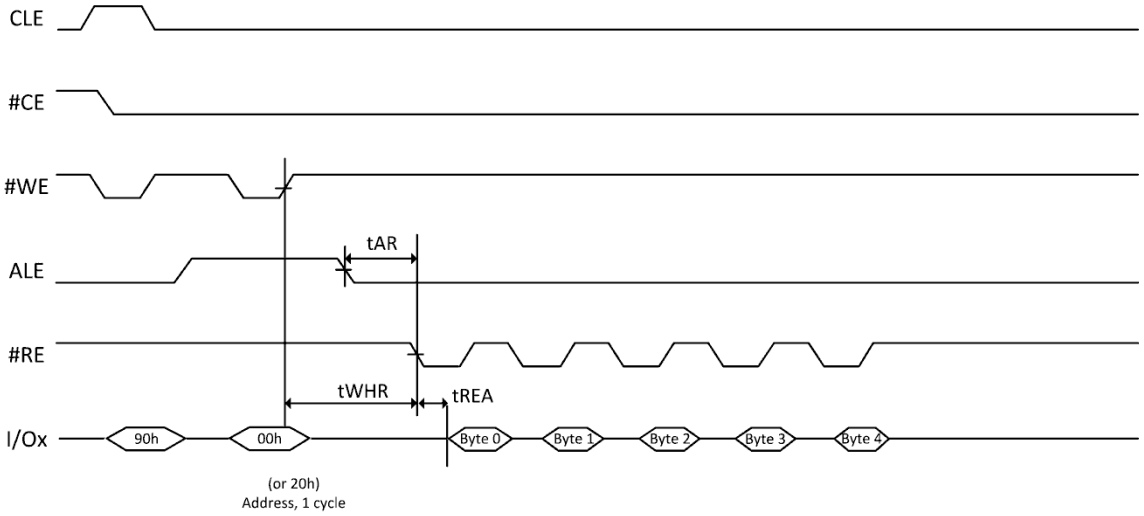


Figure 11-12 Read ID

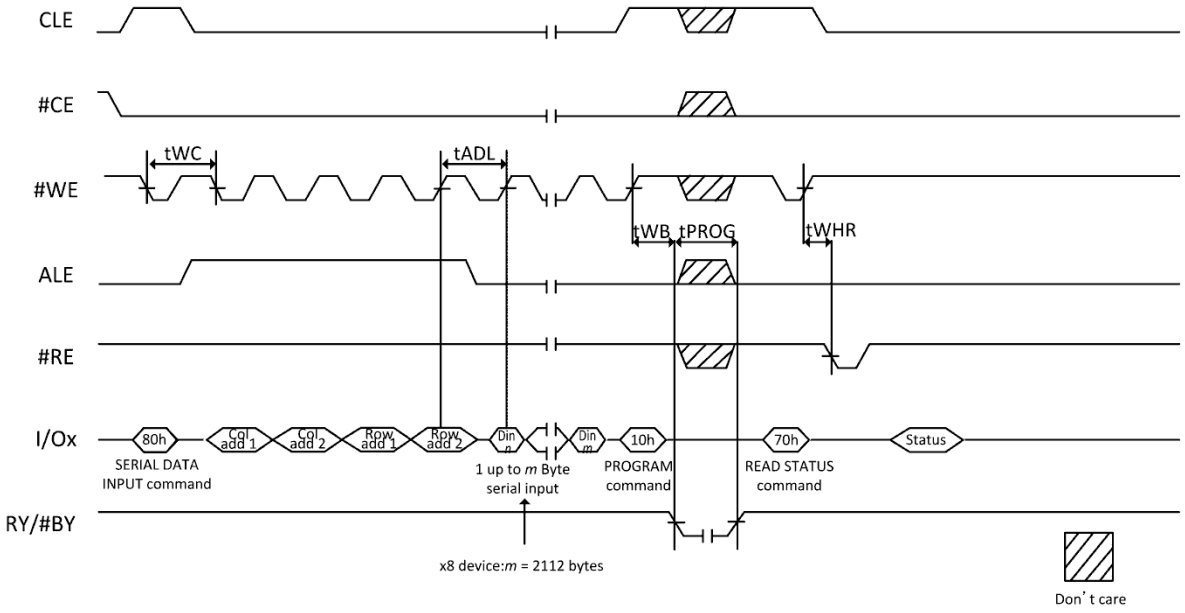


Figure 11-13 Page Program

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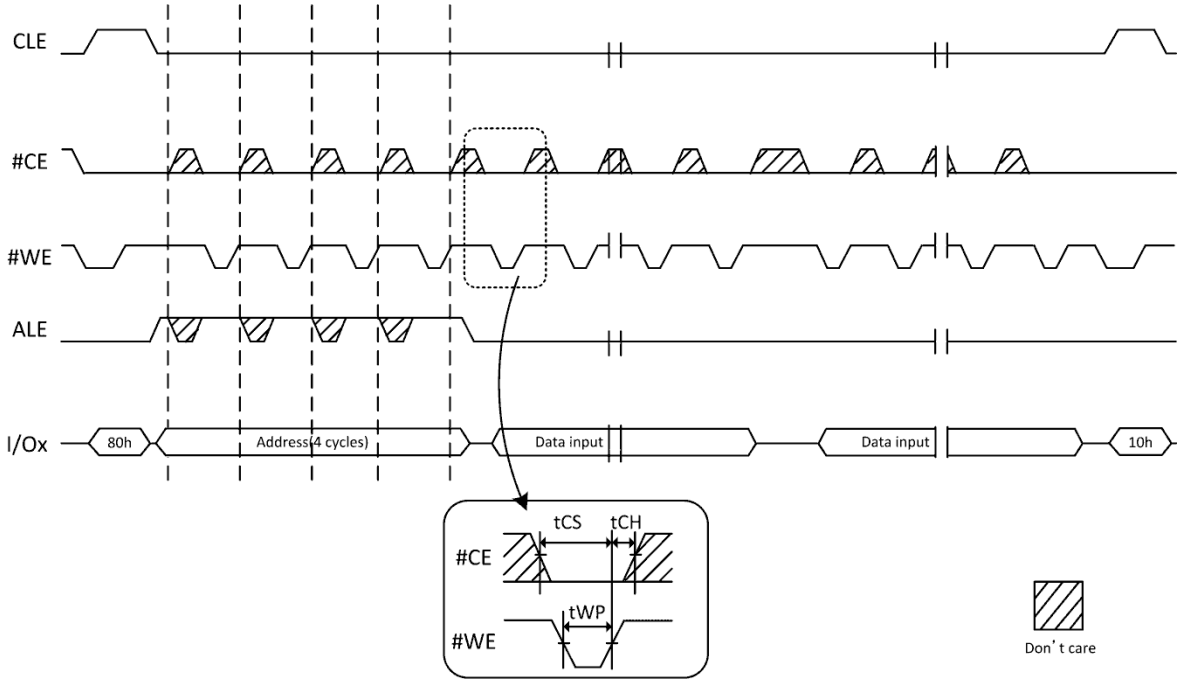


Figure 11-14 #CE Don't Care Page Program Operation

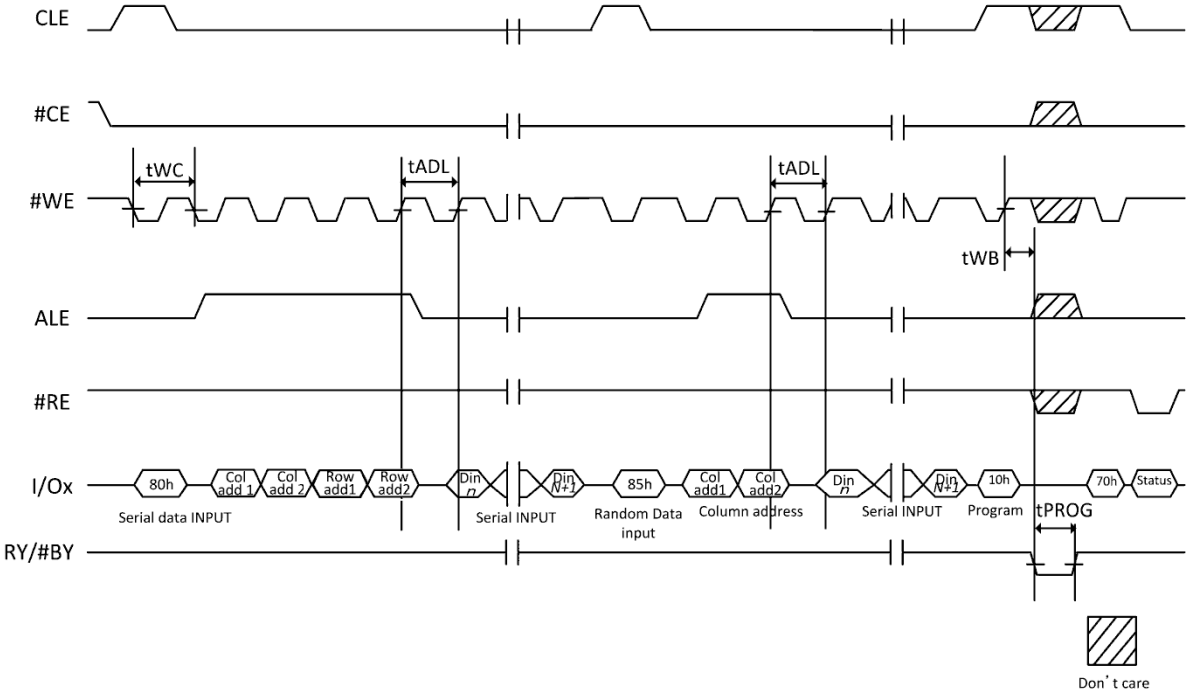


Figure 11-15 Page Program with Random Data Input

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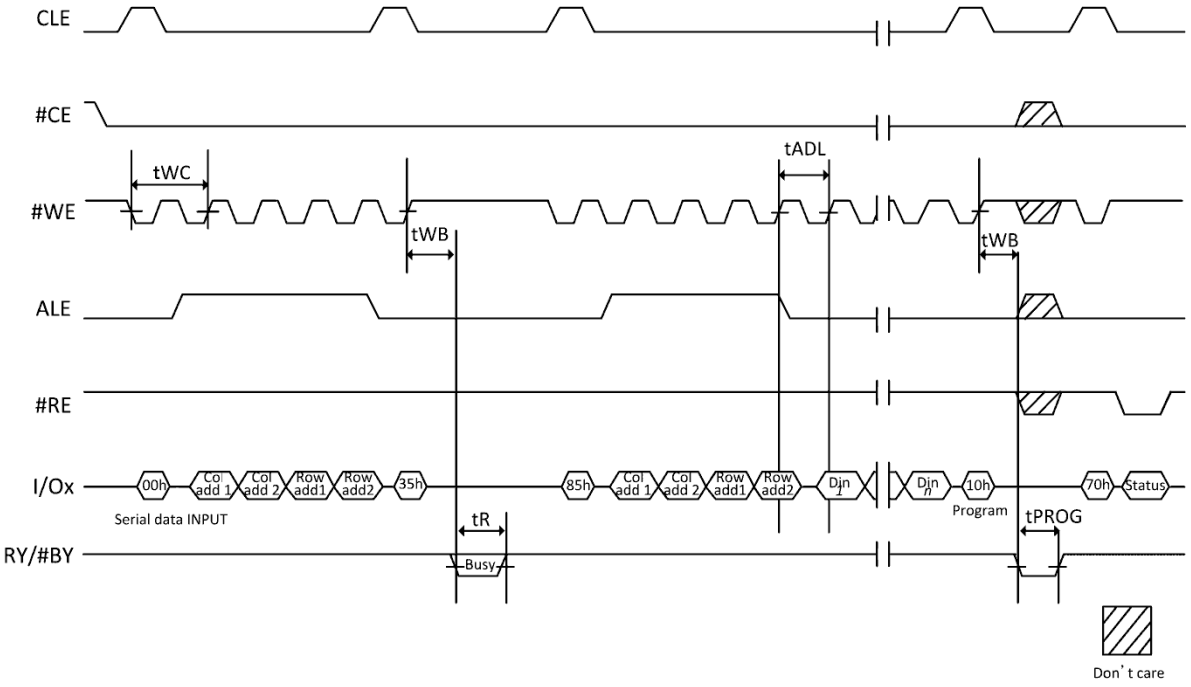


Figure 11-16 Copy Back

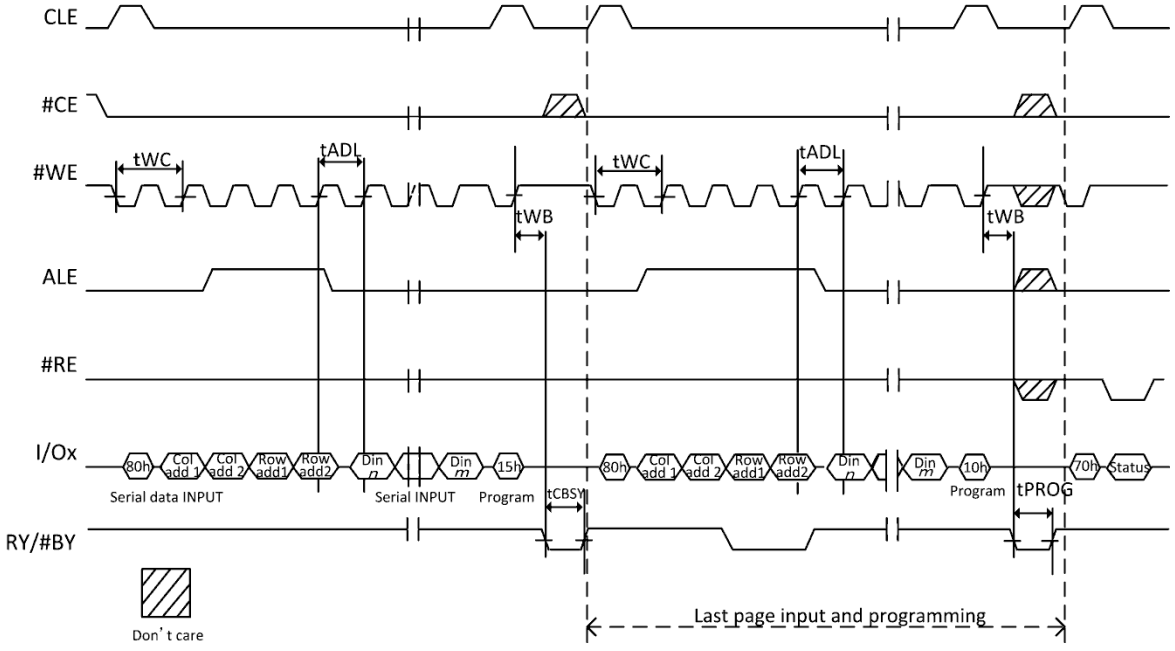


Figure 11-17 Cache Program

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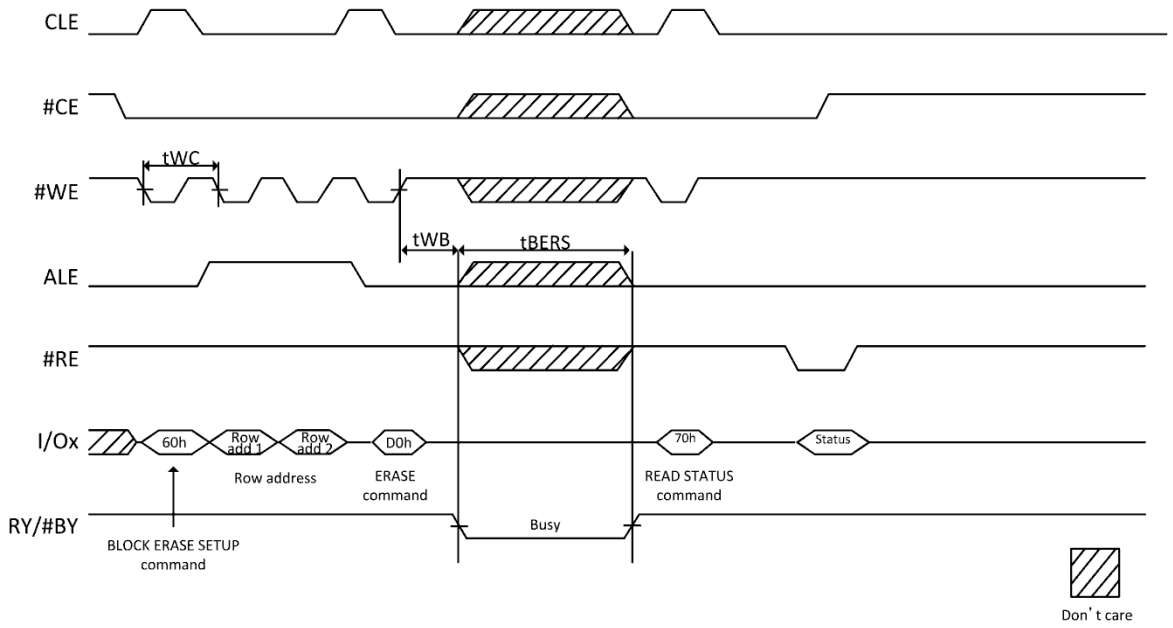


Figure 11-18 Block Erase

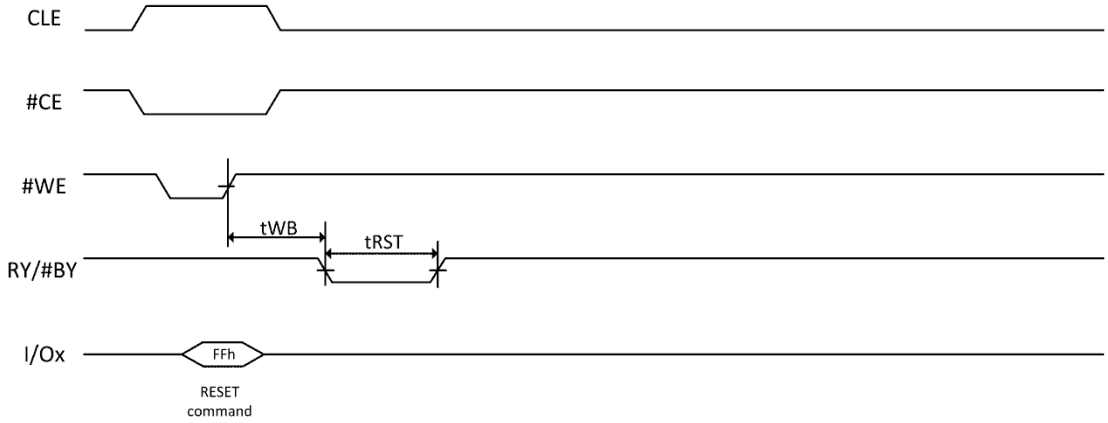


Figure 11-19 Reset

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12. INVALID BLOCK MANAGEMENT

12.1 Invalid blocks

The W29N01GZ/W may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks (See Table 12.1). An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	1004	1024	blocks

Table 12-1 Valid Block Number

12.2 Initial invalid blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The W29N01GZ/W has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are marked. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. The initial invalid block information cannot be recovered if inadvertently erased. Therefore, software should be created to initially check for invalid blocks by reading the marked locations before performing any program or erase operation, and create a table of initial invalid blocks as following flow chart

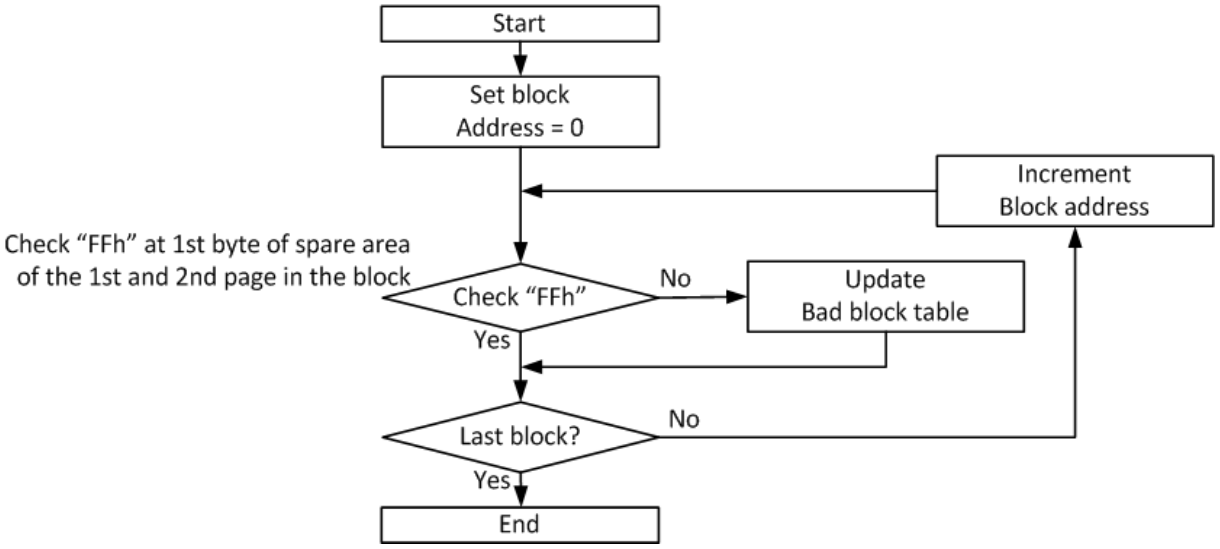


Figure 12-1 flow chart of create initial invalid block table

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12.3 Error in operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each program and erase operation, check the status read to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 1-bit ECC per 528 bytes of data to ensure data recovery.

Operation	Detection and recommended procedure
Erase	Status read after erase → Block Replacement
Program	Status read after program → Block Replacement
Read	Verify ECC → ECC correction

Table 12-2 Block failure

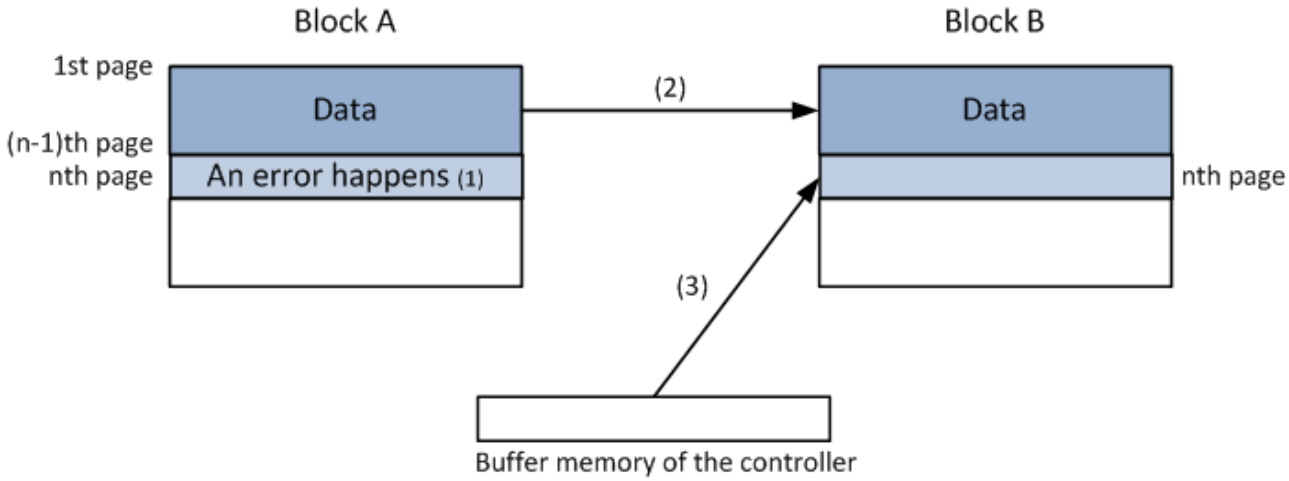


Figure 12-2 Bad block Replacement

Note:

1. **An error happens in the nth page of block A during program or erase operation.**
2. **Copy the data in block A to the same location of block B which is valid block.**
3. **Copy the nth page data of block A in the buffer memory to the nth page of block B**
4. **Creating or updating bad block table for preventing further program or erase to block A**

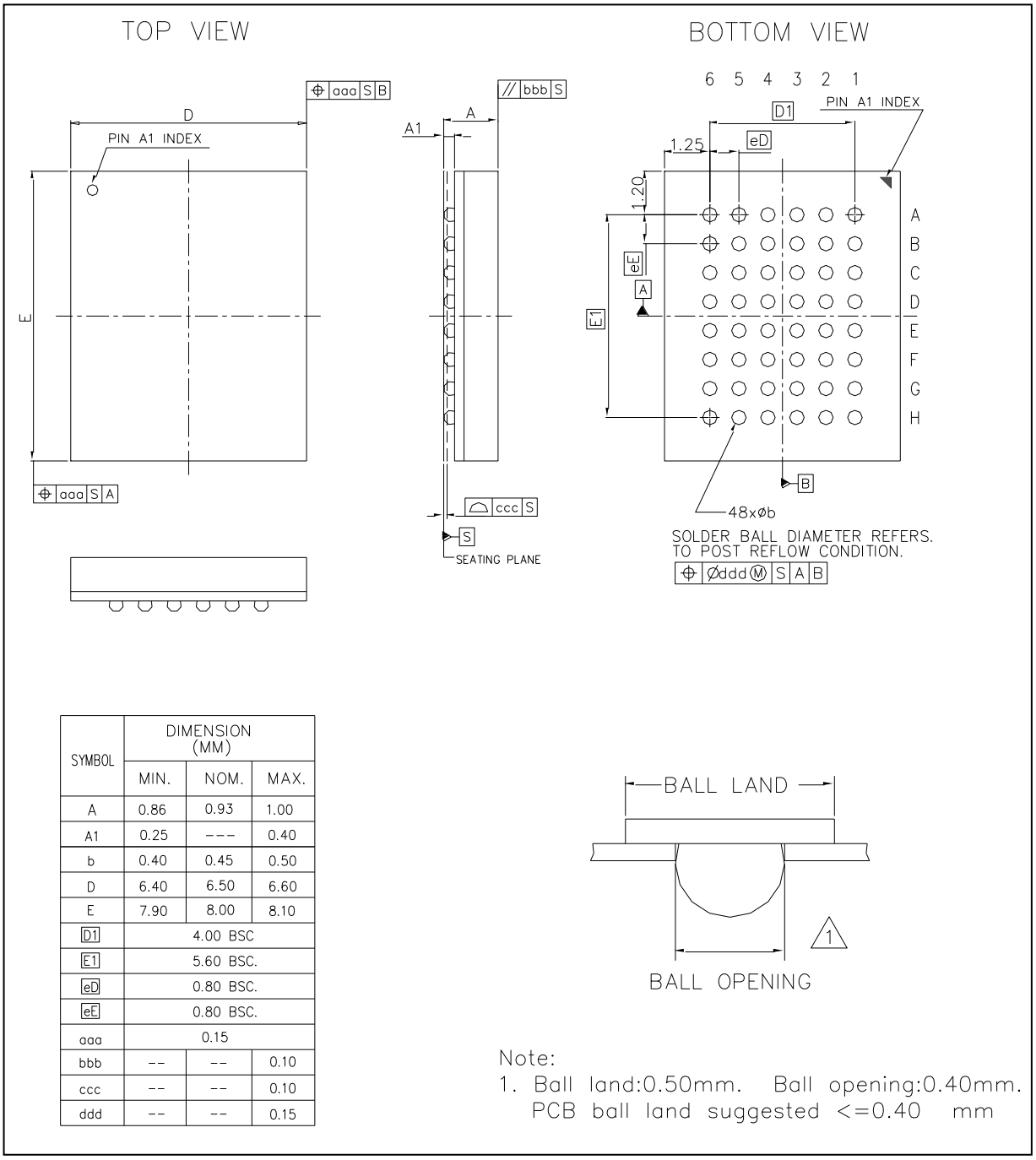
12.4 Addressing in program operation

The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. The lower order page is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.

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13. PACKAGE DIMENSIONS

13.1 VFBGA48Ball (8X6.5 MM^2, Ball pitch: 0.8mm, Ø=0.45mm)



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.86	0.93	1.00
A1	0.25	---	0.40
b	0.40	0.45	0.50
D	6.40	6.50	6.60
E	7.90	8.00	8.10
D1	4.00 BSC		
E1	5.60 BSC.		
eD	0.80 BSC.		
eE	0.80 BSC.		
aaa	0.15		
bbb	--	--	0.10
ccc	--	--	0.10
ddd	--	--	0.15

Note:
1. Ball land:0.50mm. Ball opening:0.40mm.
   PCB ball land suggested <=0.40 mm

Figure 13-1 Fine-Pitch Ball Grid Array 48-Ball (8x6.5mm)

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14. ORDERING INFORMATION

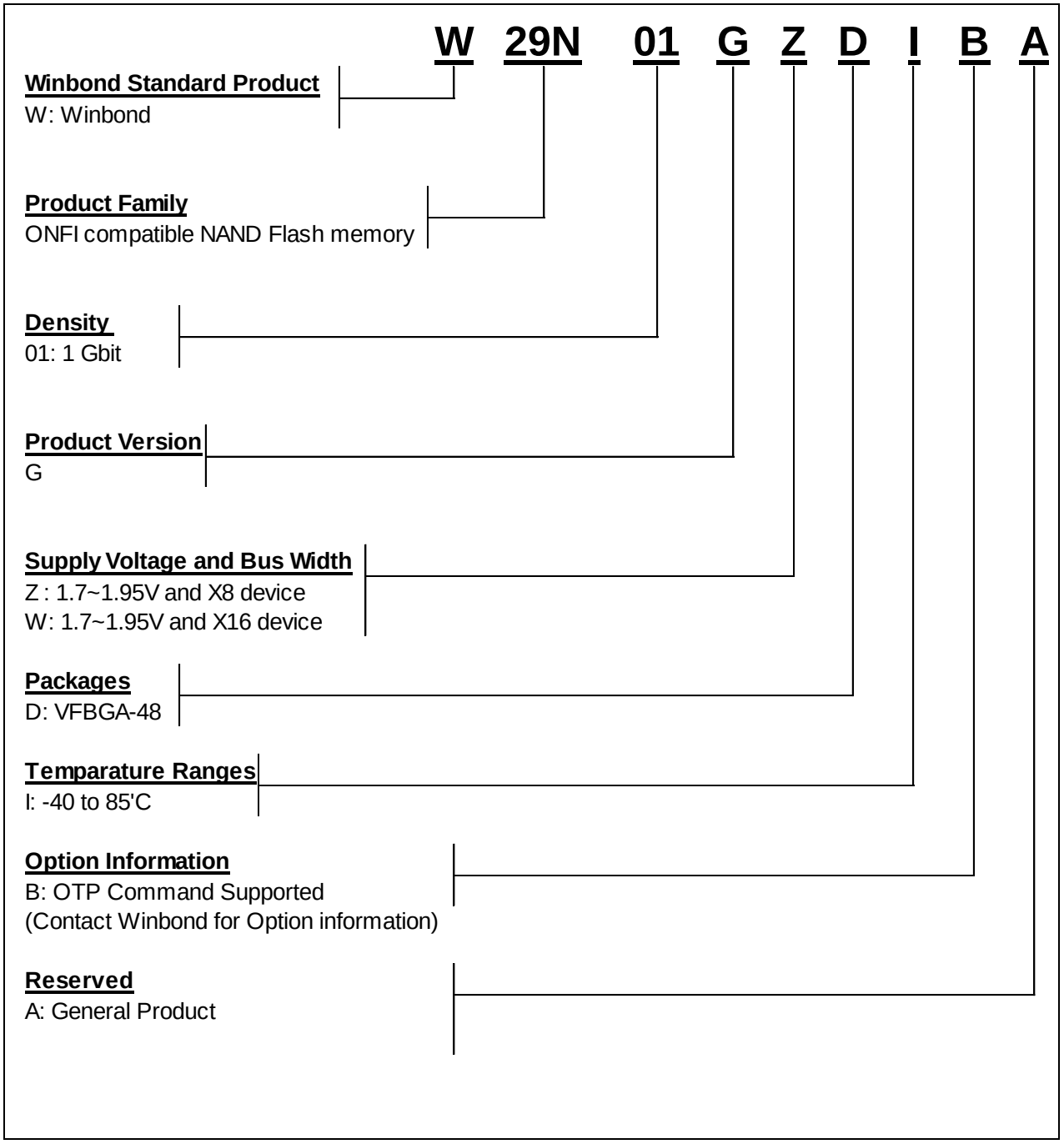


Figure 14-1 Ordering Part Number Description

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15. VALID PART NUMBERS

The following table provides the valid part numbers for the W29N01GZ/W NAND Flash Memory. Please contact Winbond for specific availability by density and package type. Winbond NAND Flash memories use a 12-digit Product Number for ordering.

Part Numbers for Industrial Temperature:

PACKAGE TYPE	DENSITY	BUS WIDTH	PRODUCT NUMBER	TOP SIDE MARKING
D VFBGA-48	1G-bit	X8	W29N01GZDIBA	W29N01GZDIBA
D VFBGA-48	1G-bit	X16	W29N01GWDIBA	W29N01GWDIBA

Table 15-1 Part Numbers for Industrial Temperature

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16. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	10/22/13		New Create Preliminary
B	10/25/13		Correct typo
C	12/24/13	52 41	tRCBSY : max 3us -> max tR OTP : ONFI OTP Remove commercial grade
D	08/07/14	- 41	W29N01Gx → W29N01GZ/W OTP : Legacy OTP
E	08/08/14	65, 66	Update Ordering Part Number
F	11/07/14		Remove “Advanced Information”, “Preliminary”
G	02/01/16	23, 47	Update Parameter Page Output Value Update Notes of Absolute Maximum Ratings
H	09/14/16	50	tWC : min 35ns -> min 25ns TR/TF : max 5ns -> 2.5ns
I	12/01/17	9	Change description of DNU
J	01/11/18	64	Update Package Dimension of VFBGA-48

Table 16-1 History Table

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