2.5 / 3 / 3.3 V
512K-BIT
SERIAL FLASH MEMORY WITH
4KB SECTORS AND DUAL I/O SPI

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深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com
微信扫码咨询客服

winbond

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1. GENERAL DESCRIPTION

The W25X05CL (512K-bit) Serial Flash memories provide a storage solution for systems with limited space, pins and power. The 25X series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code download applications as well as storing voice, text and data. The devices operate on a single 2.3V to 3.6V power supply with current consumption as low as 1mA active and 1µA for power-down. All devices are offered in space-saving packages.

The W25X05CL arrays are organized into 256 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. The W25X05CL have 16 erasable sectors, 2 erasable 32KB blocks and 1 erasable 64KB blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25X05CL support the standard Serial Peripheral Interface (SPI), and a high performance dual output as well as Dual I/O SPI: Serial Clock, Chip Select, Serial Data DI (I/O0), DO (I/O1). SPI clock frequencies up to 104MHz are supported allowing equivalent clock rates of 208MHz when using the Fast Read Dual Output instruction. These transfer rates are comparable to those of 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 16-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protect, with top or bottom array control features, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

2. FEATURES

- **Family of Serial Flash Memories**
  - W25X05CL: 512K-bit/64K-byte (65,536)
  - 256-bytes per programmable page
  - Uniform erasable 4KB, 32KB & 64KB regions.
- **SPI with Single / Dual Outputs / I/O**
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO0, IO1, /WP, /Hold
- **Data Transfer up to 208M-bits / second**
  - Clock operation to 104MHz
  - 208MHz equivalent Dual I/O SPI
  - Auto-increment Read capability
- **Efficient "Continuous Read Mode"**
  - Low Instruction overhead
  - Continuous Read
  - As few as 16 clocks to address memory
  - Allows true XIP (execute in place) operation
- **Software and Hardware Write Protection**
  - Write-Protect all or portion of memory
  - Enable/Disable protection with /WP pin
  - Top or bottom array protection
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4/32/64-kbytes)
  - Page program up to 256 bytes <1ms
  - More than 100,000 erase/write cycles
  - More than 20-year data retention
- **Low Power, Wide Temperature Range**
  - Single 2.3V to 3.6V supply
  - 1mA active current, <1µA Power-down(typ.)
  - -40° to +85°C operating range
- **Space Efficient Packaging**
  - 8-pin SOIC / VSOP 150-mil
  - 8-pin TSSOP 173-mil
  - 8-pad USON 2x3-mm
  - Contact Winbond for KGD and other options

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3. PIN CONFIGURATION SOIC 150-MIL, VSOP 150-MIL, TSSOP 173-MIL

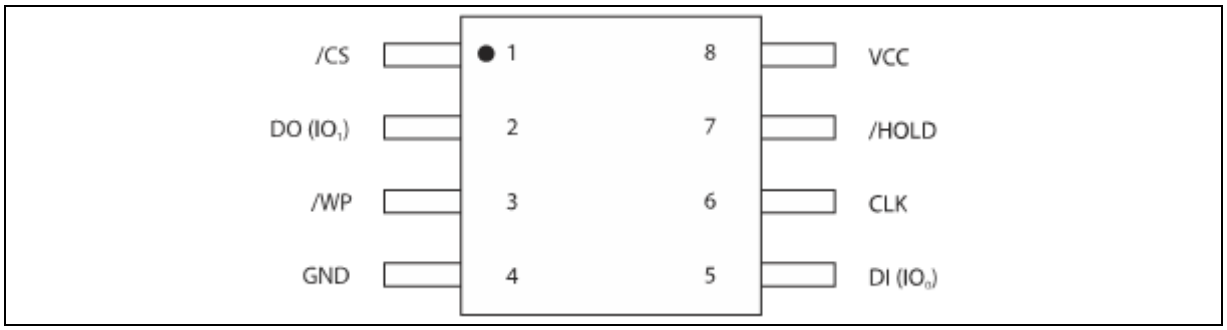


Figure 1a. W25X05CL Pin Assignments, 8-pin SOIC 150-mil, VSOP 150-mil and TSSOP8 173-mil (Package Code SN, SV and SD)

4. PAD CONFIGURATION USON 2X3-MM

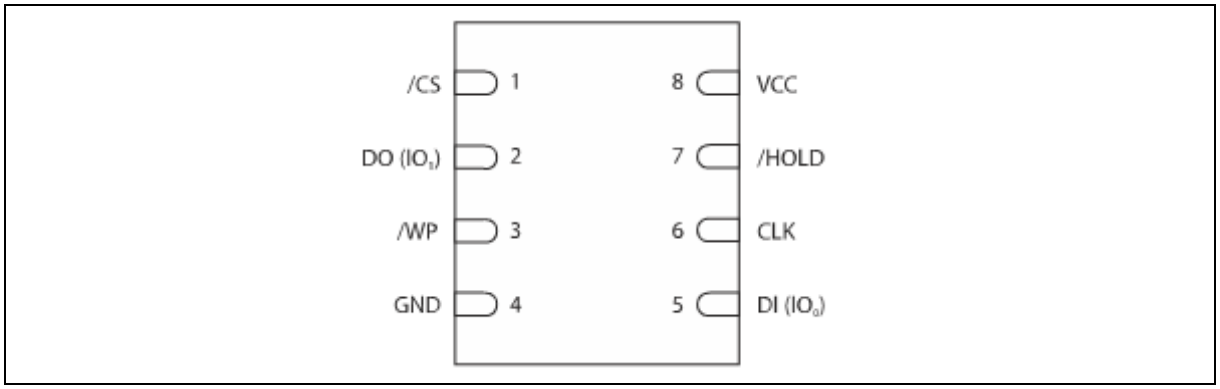


Figure 1b. W25X05CL Pad Assignments USON 2x3-MM (Package Code UX)

5. PIN DESCRIPTION SOIC\VSOP 150-MIL AND USON 2X3-MM

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Input / Output(1)
3	/WP	I	Write Protect Input
4	GND		Ground
5	DI (IO0)	I/O	Data Input / Output(1)
6	CLK	I	Serial Clock Input
7	/HOLD	I	Hold Input
8	VCC		Power Supply

Note:

1 IO0 and IO1 are used for Standard and Dual SPI instructions

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5.1 Package Types

W25X05CL are offered in 8-pin plastic 150-mil width SOIC (package code SN), 150-mil width VSOP8 (package code SV) and 173-mil width TSSOP (package code SD) and 2x3-mm USON (package code UX). Refer to see figures 1a and 1b, respectively.

5.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Power-up Timing and Write inhibit threshold” and Figure 26). If needed, a pull-up resister on /CS can be used to accomplish this.

5.3 Serial Data Input, Output and IOs (DI, DO, IO0 and IO1)

The W25X05CL support standard SPI and Dual SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

5.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (TB, BP1 and BP0) bits and Status Register Protect (SRP) bit, a portion or the entire memory array can be hardware protected. The /WP pin is active low.

5.5 HOLD (/HOLD)

The Hold (/HOLD) pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals.

5.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

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6. BLOCK DIAGRAM

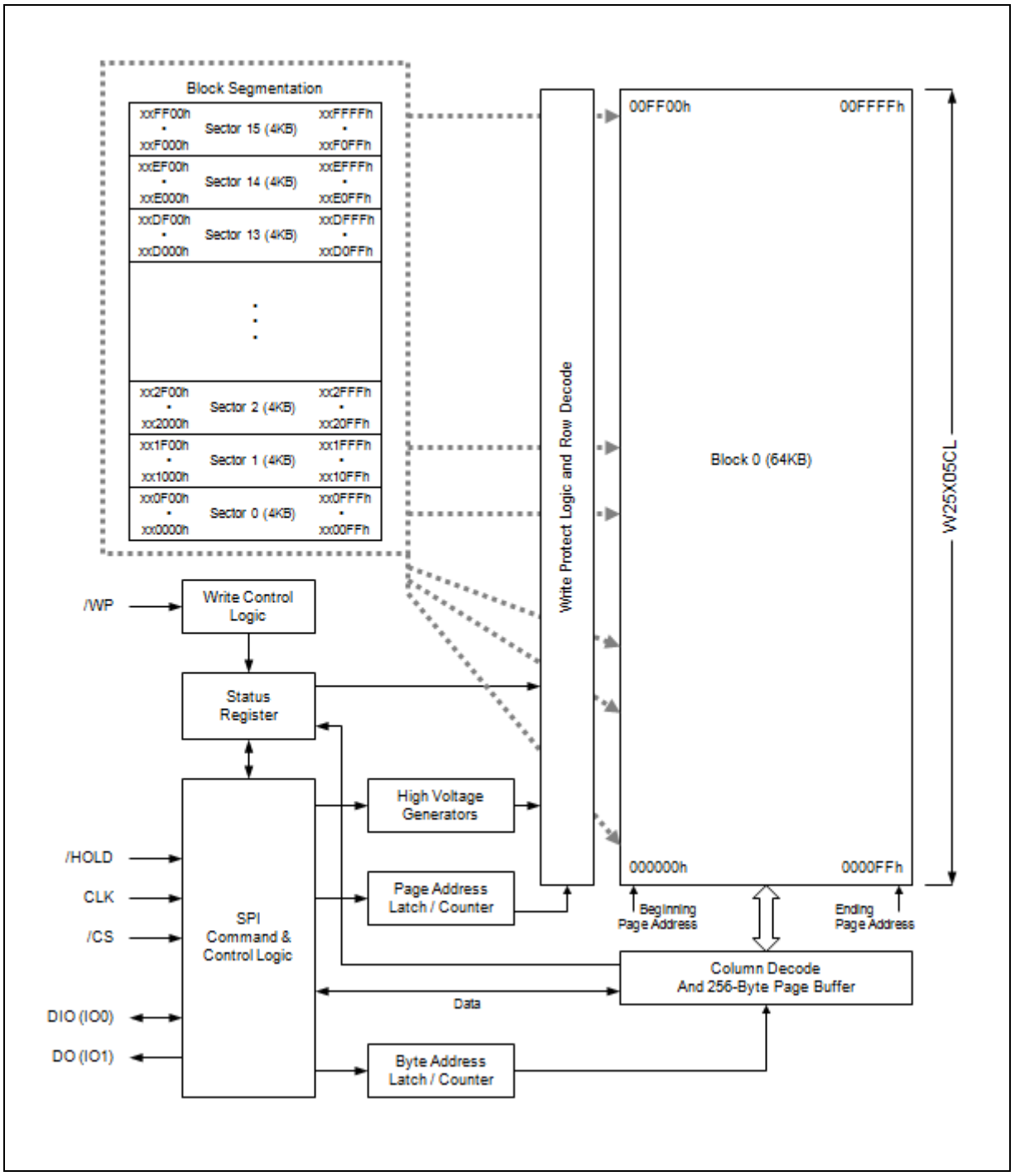


Figure 2. W25X05CL Serial Flash Memory Block Diagram

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7. FUNCTIONAL DESCRIPTION

7.1 SPI OPERATIONS

7.1.1 Standard SPI Instructions

The W25X05CL are accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3 the CLK signal is normally high on the falling and rising edges of /CS.

7.1.2 Dual SPI Instructions

The W25X05CL support Dual SPI operation when using the “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)” instructions. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

7.1.3 Hold Function

The /HOLD signal allows the W25X05CL operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK.

During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input/Output (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

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7.2 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25X05CL provide several means to protect data from inadvertent writes.

7.2.1 Write Protect Features

- Device resets when VCC is below threshold.
- Time delay write disable after Power-up.
- Write enable/disable instructions.
- Automatic write disable after program and erase.
- Software and Hardware (/WP pin) write protection using Status Register.
- Write Protection using Power-down instruction.

Upon power-up or at power-down, the W25X05CL will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 26). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed, a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (TB, BP1 and BP0) bits. These allow a portion small as 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

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8. CONTROL AND STATUS REGISTERS

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, and the state of write protection. The Write Status Register instruction can be used to configure the device write protection features.

8.1 STATUS REGISTER

8.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

8.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions finished: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

8.1.3 Block Protect Bits (BP1, BP0)

The Block Protect Bits (BP1 and BP0) are non-volatile read/write bits in the status register (S3 and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tw in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected. The Block Protect bits cannot be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

8.1.4 Top/Bottom Block Protect (TB)

The Top/Bottom bit (TB) controls if the Block Protect Bits (BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The TB bit is non-volatile and the factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction provided that the Write Enable instruction has been issued. The TB bit cannot be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

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8.1.5 Reserved Bits

Status register bit location S6 and S4 are reserved for future use. Current devices will read 0 for this bit location. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

8.1.6 Status Register Protect (SRP)

The Status Register Protect (SRP) bit is a non-volatile read/write bit in status register (S7) that can be used in conjunction with the Write Protect (/WP) pin to disable writes to status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

SRP	/WP	Status Register	Description
0	X	Software Protection	/WP pin has no control, The Status register can be written to after a Write Enable instruction WEL = 1. [Factory Default]
1	0	Hardware Protected	When /WP pin is low the Status Register locked and can't be written to.
1	1	Hardware Unprotected	When /WP pin is high the status register is unlocked and can be written to after a Write Enable instruction WEL = 1.

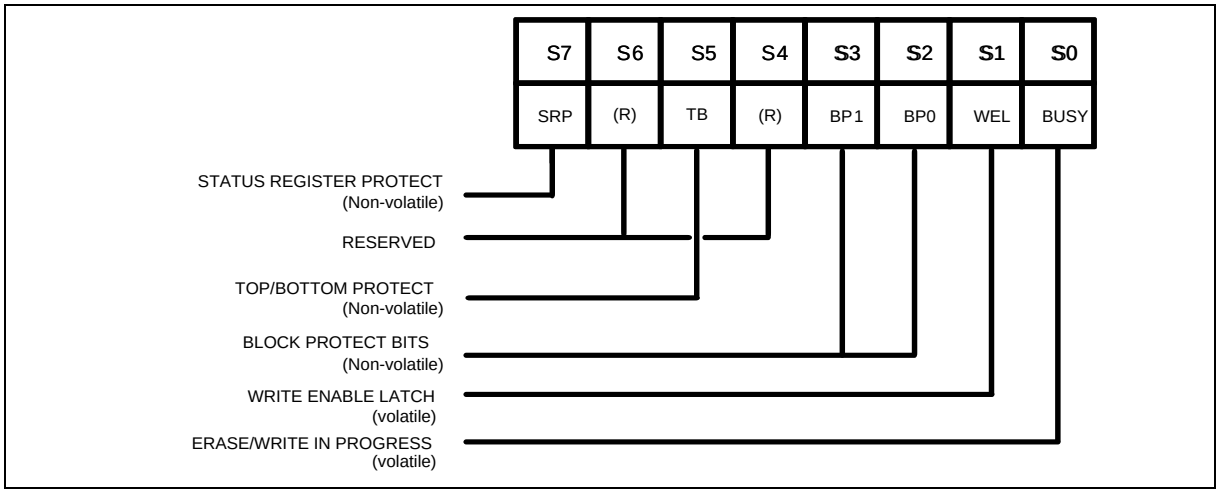


Figure 3. Status Register Bit Locations

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8.1.7 Status Register Memory Protection

STATUS REGISTER(1)			W25X05CL (512K-BIT) MEMORY PROTECTION			
TB	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
x	0	0	NONE	NONE	NONE	NONE
x	0	1	0	000000h - 00FFFFh	64KB	ALL
x	1	0	0	000000h - 00FFFFh	64KB	ALL
x	1	1	0	000000h - 00FFFFh	64KB	ALL

Note:
1. x = don't care
2. If any erase or program command specifies a memory region that contains protected data portion, this command will be ignore.

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INSTRUCTIONS

The instruction set of the W25X05CL consists of twenty basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 25. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.1.8 Manufacturer and Device Identification

MANUFACTURER ID	**(M7-M0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7-ID0)**	**(ID15-ID0)**
Instruction	**ABh, 90h, 92h**	**9Fh**
W25X05CL	05h	3010h

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8.1.9 Instruction Set (1)

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	N-BYTES
Write Enable	**06h**						
Write Enable for Volatile Status Register	**50h**						
Write Disable	**04h**						
Read Status Register	**05h**	(S7–S0)(1)					(2)
Write Status Register	**01h**	(S7–S0)					
Read Data	**03h**	A23–A16	A15–A8	A7–A0	(D7–D0)	(Next byte)	continuous
Fast Read	**0Bh**	A23–A16	A15–A8	A7–A0	dummy	(D7–D0)	(Next Byte) continuous
Fast Read Dual Output	**3Bh**	A23–A16	A15–A8	A7–A0	dummy	(D7-D0, …)(5)	(one byte per 4 clocks, continuous)
Fast Read Dual I/O	**BBh**	A23-A8(6)	A7-A0, M7-M0(6)	(D7-D0, …)(5)			
Page Program	**02h**	A23–A16	A15–A8	A7–A0	(D7–D0)	(Next byte)	Up to 256 bytes
Sector Erase (4KB)	**20h**	A23–A16	A15–A8	A7–A0			
Block Erase (32KB)	**52h**	A23–A16	A15–A8	A7–A0			
Block Erase (64KB)	**D8h**	A23–A16	A15–A8	A7–A0			
Chip Erase	**C7h/60h**						
Power-down	**B9h**						
Release Power-down / Device ID	**ABh**	dummy	dummy	dummy	(ID7-ID0)(4)		
Manufacturer/ Device ID (3)	**90h**	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	
Manufacturer/Device ID by Dual I/O	**92h**	A23-A8	A7-A0, M[7:0]	(MF[7:0], ID[7:0])			
JEDEC ID	**9Fh**	(M7-M0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity			
Read Unique ID	**4Bh**	dummy	dummy	dummy	dummy	(ID63-ID0)	

Notes:

1 Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
2 The Status Register contents will repeat continuously until /CS terminates the instruction.
3 See Manufacturer and Device Identification table for Device ID information.
4 The Device ID will repeat continuously until /CS terminates the instruction.
5 Dual Output and Dual I/O data
  IO0 = (D6, D4, D2, D0)
  IO1 = (D7, D5, D3, D1)
6 Dual Input Address
  IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
  IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

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8.1.10 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

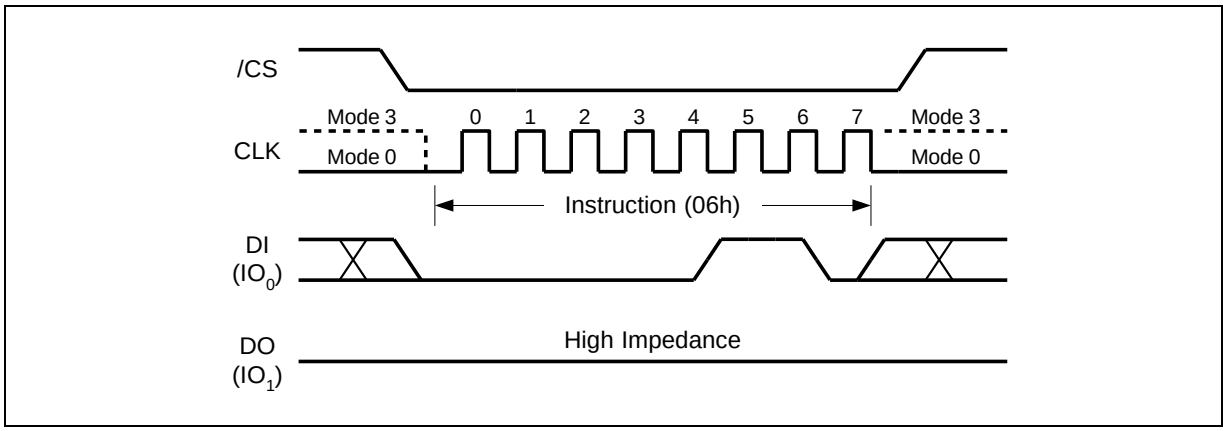


Figure 4. Write Enable Instruction Sequence Diagram

8.1.11 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 8.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 5) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

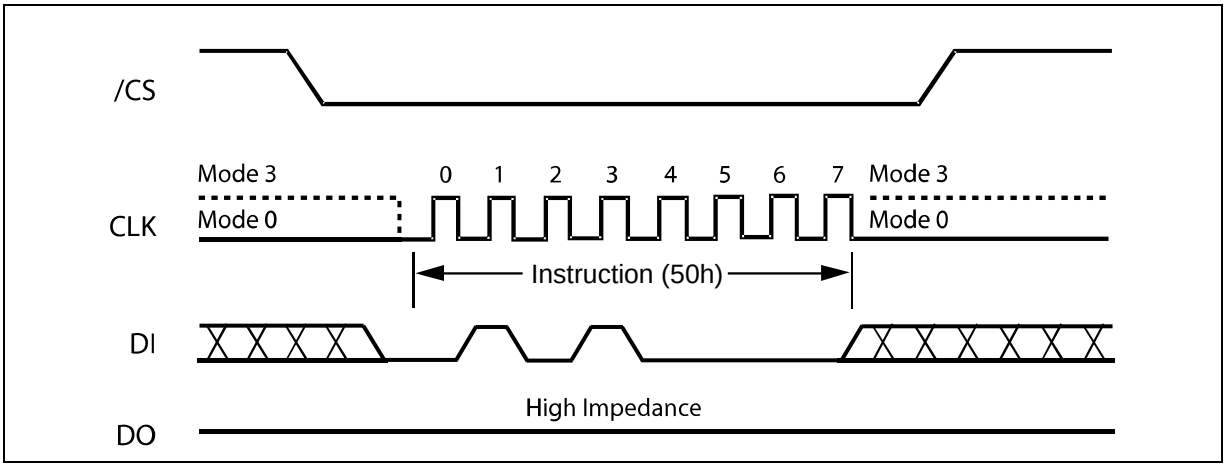


Figure 5. Write Enable for Volatile Status Register Instruction Sequence Diagram

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8.1.12 Write Disable (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions. Write Disable instruction can also be used to invalidate the Write Enable for Volatile Status Register instruction

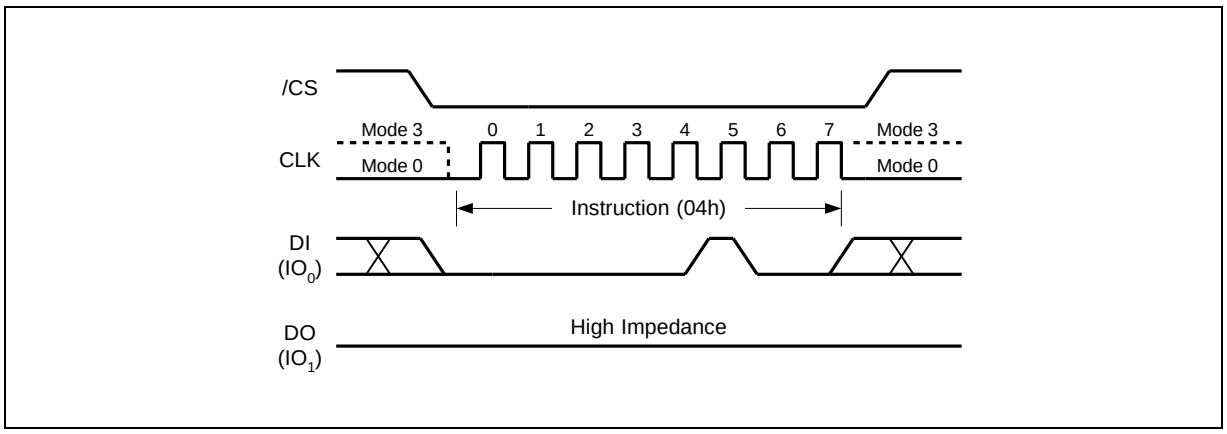


Figure 6. Write Disable Instruction Sequence Diagram

8.1.13 Read Status Register (05h)

The Read Status Register instruction allows the 8-bit Status Register to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 6. The Status Register bits are shown in figure 3 and include the BUSY, WEL, BP1, BP0, TB and SRP bits (see description of the Status Register earlier in this datasheet).

The Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 7. The instruction is completed by driving /CS high.

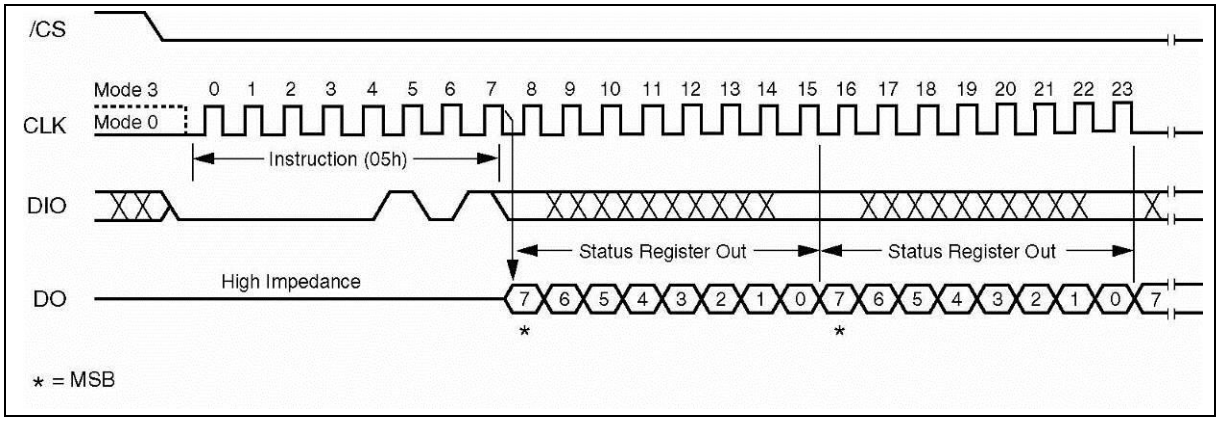


Figure 7. Read Status Register Instruction Sequence Diagram

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8.1.14 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in figure 8. The Status Register bits are shown in figure 3 and described earlier in this datasheet.

Only non-volatile Status Register bits SRP, TB, BP1 and BP0 (bits 7, 5, 3 and 2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Write Status Register instruction will not be executed. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (TB, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table). The Write Status Register instruction also allows the Status Register Protect bit (SRP) to be set. This bit is used in conjunction with the Write Protect (/WP) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

During volatile Status Register write operation (50h combined with 01h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

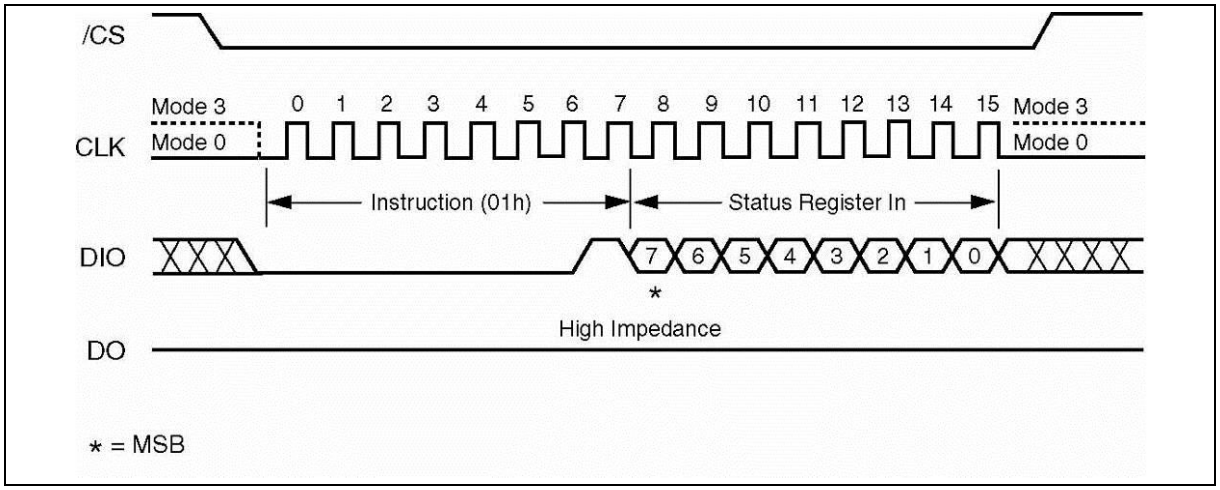


Figure 8. Write Status Register Instruction Sequence Diagram

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8.1.15 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in figure 9. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

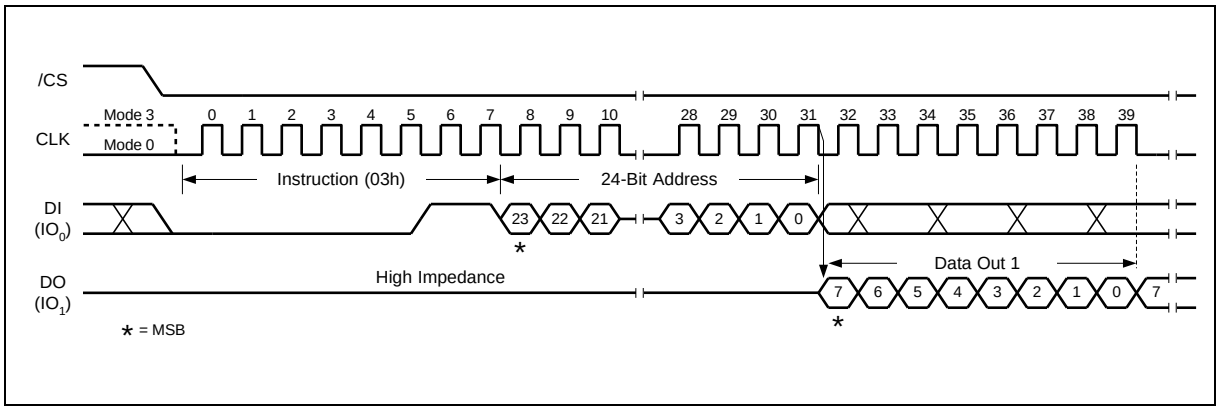


Figure 9. Read Data Instruction Sequence Diagram

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8.1.16 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 10. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DI pin is a “don’t care”.

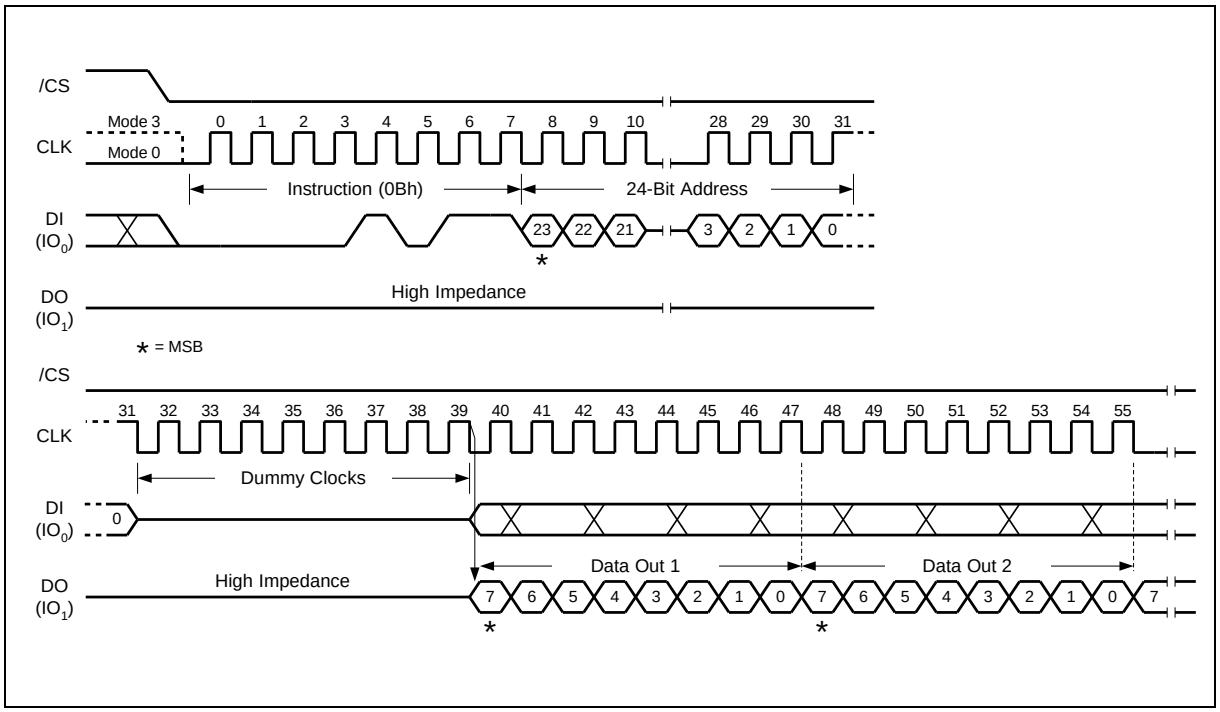


Figure 10. Fast Read Instruction Sequence Diagram

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8.1.17 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, IO_0 and IO_1. This allows data to be transferred from the W25X05CL at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

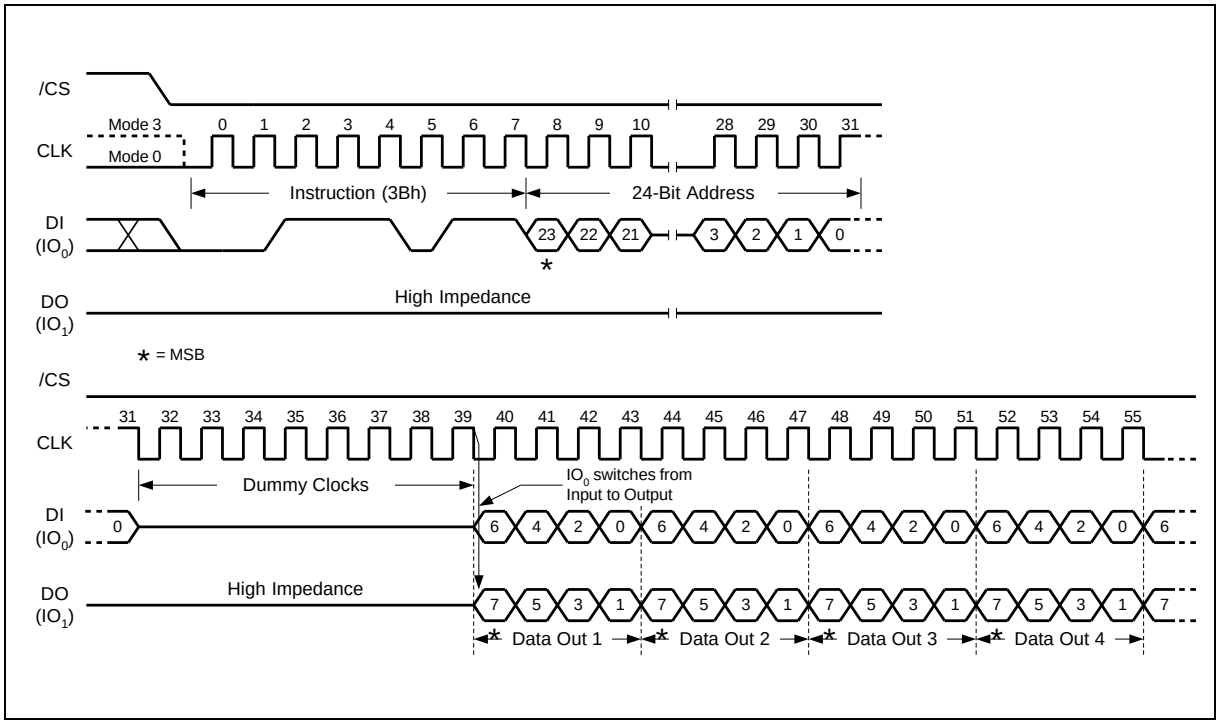


Figure 11. Fast Read Dual Output Instruction Sequence Diagram

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8.1.18 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in figure 12a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in figure 12b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M7-0) before issuing normal instructions (See 9.2.12 for detail descriptions).

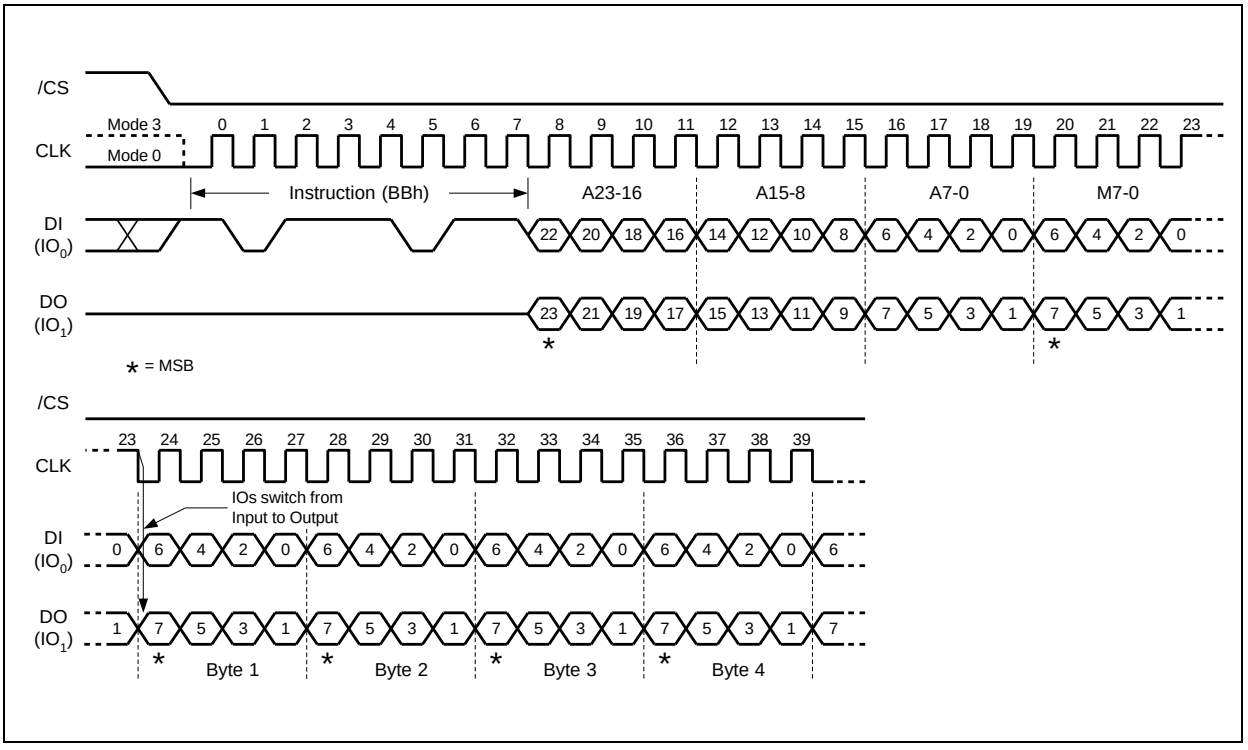


Figure 12a. Fast Read Dual I/O Instruction Sequence (Initial instruction or previous M5-4 ≠ 10)

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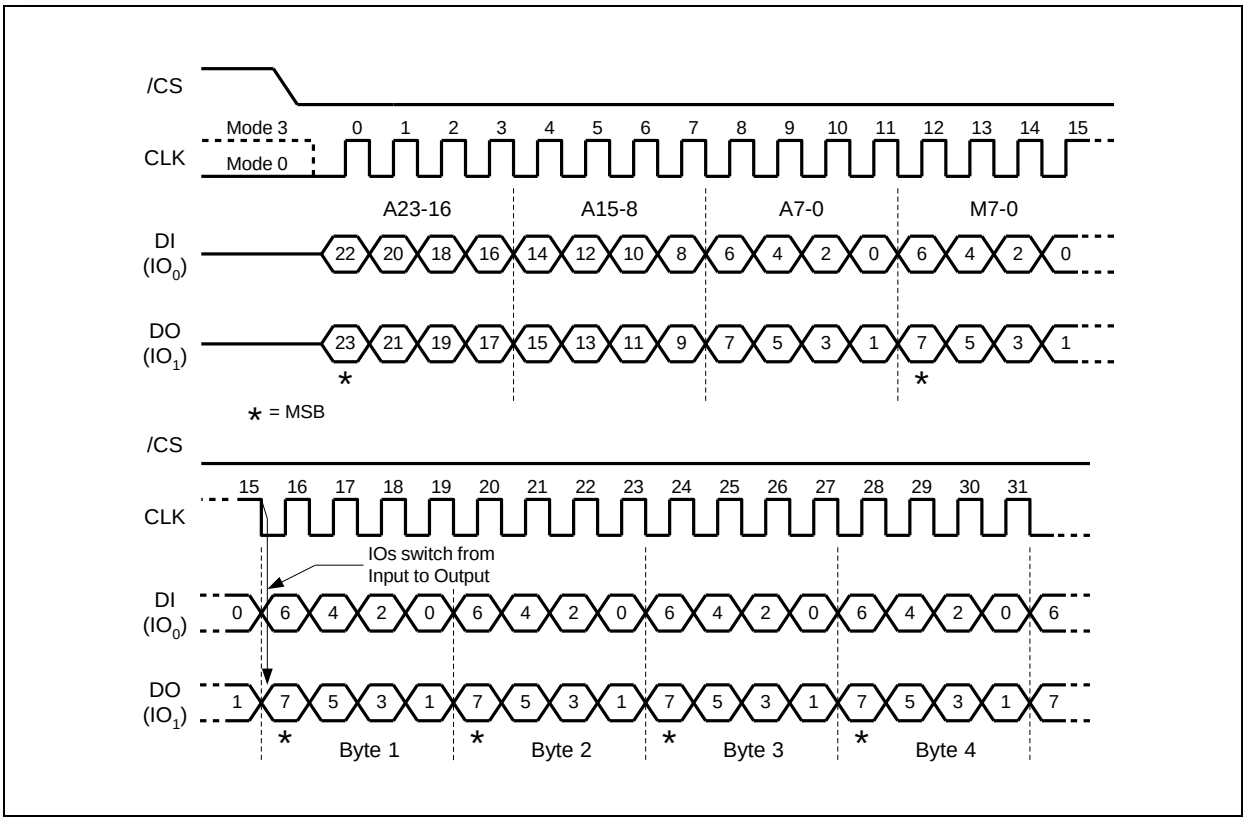


Figure 12b. Fast Read Dual I/O Instruction Sequence (Previous instruction set M5-4 = 10)

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8.1.19 Continuous Read Mode Bits (M7-0)

The “Continuous Read Mode” bits are used in conjunction with the “Fast Read Dual I/O” instruction to provide the highest random Flash memory access rate with minimum SPI instruction overhead, thus allow true XIP (execute in place) to be performed on serial flash devices.

M7-0 need to be set by the Dual I/O Read instruction. M5-4 are used to control whether the 8-bit SPI instruction code BBh is needed or not for the next command. When M5-4 = (1,0), the next command will be treated same as the current Dual I/O Read command without needing the 8-bit instruction code; when M5-4 do not equal to (1,0), the device returns to normal SPI mode, all commands can be accepted. M7-6 and M3-0 are reserved bits for future use, either 0 or 1 values can be used.

8.1.20 Continuous Read Mode Reset (FFFFh)

Continuous Read Mode Reset instruction can be used to set M4 = 1, thus the device will release the Continuous Read Mode and return to normal SPI operation, as shown in figure 13.

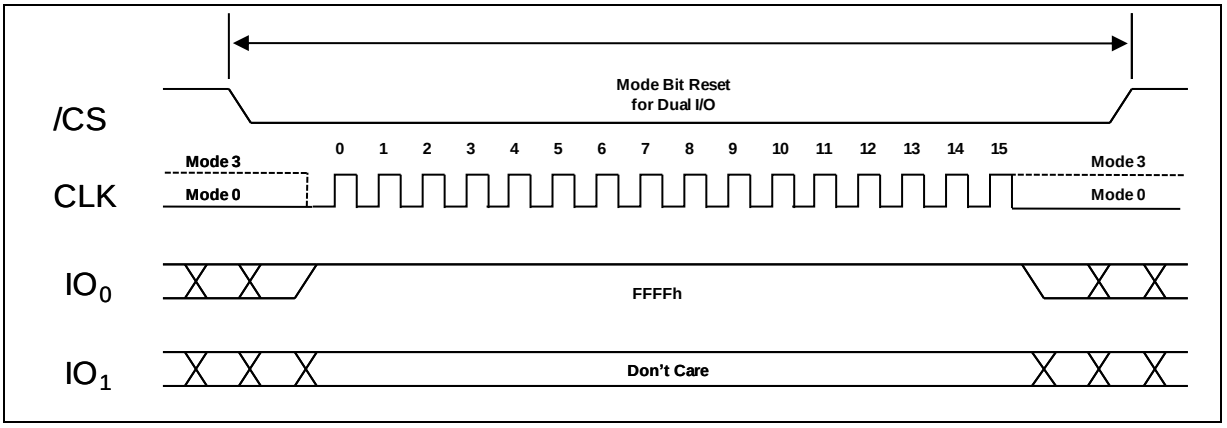


Figure 13. Continuous Read Mode Reset for Fast Read Dual I/O

Since W25X05CL does not have a hardware Reset pin, so if the controller resets while W25X05CL are set to Continuous Mode Read, the W25X05CL will not recognize any initial standard SPI instructions from the controller. To address this possibility, it is recommended to issue a Continuous Read Mode Reset instruction as the first instruction after a system Reset. Doing so will release the device from the Continuous Read Mode and allow Standard SPI instructions to be recognized.

To reset “Continuous Read Mode” during Dual I/O operation, sixteen clocks are needed to shift in instruction “FFFFh”.

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8.1.21 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL = 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP1, and BP0) bits (see Status Register Memory Protection table).

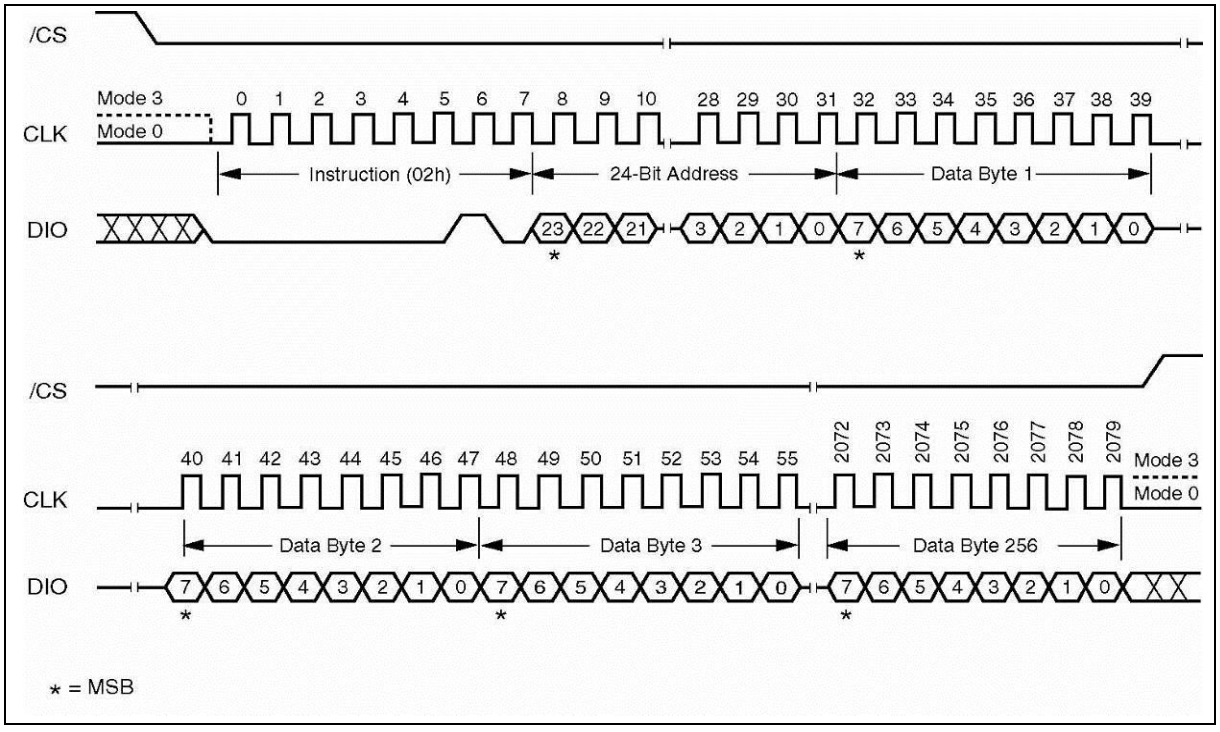


Figure 14. Page Program Instruction Sequence Diagram

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8.1.22 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0) (see Figure 2). The Sector Erase instruction sequence is shown in figure 15.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP1, and BP0) bits (see Status Register Memory Protection table).

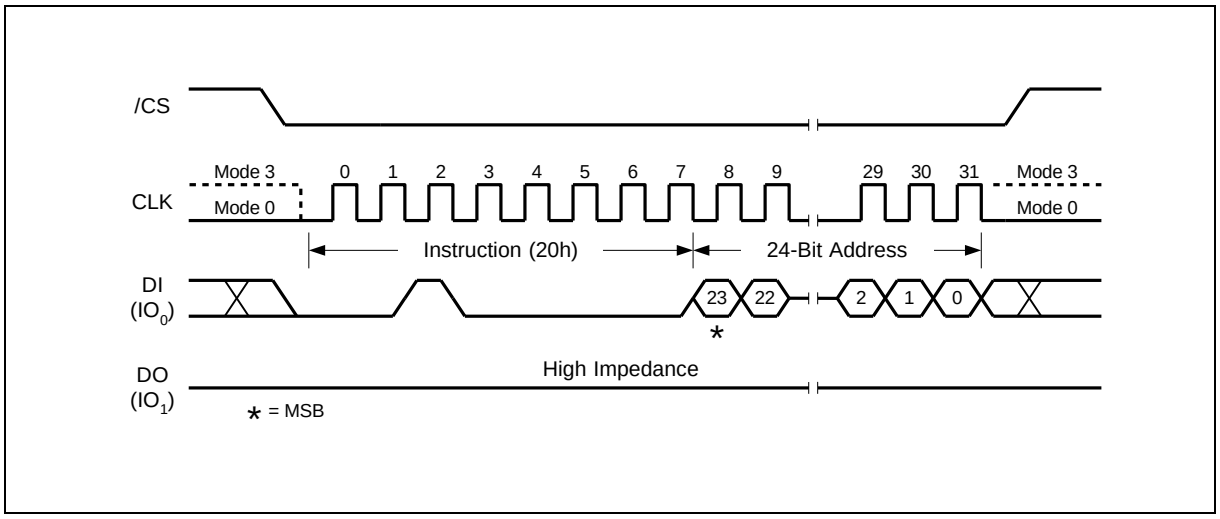


Figure 15. Sector Erase Instruction Sequence Diagram

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8.1.23 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0) (see Figure 2). The Block Erase instruction sequence is shown in figure 16.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE1} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP1, and BP0) bits (see Status Register Memory Protection table).

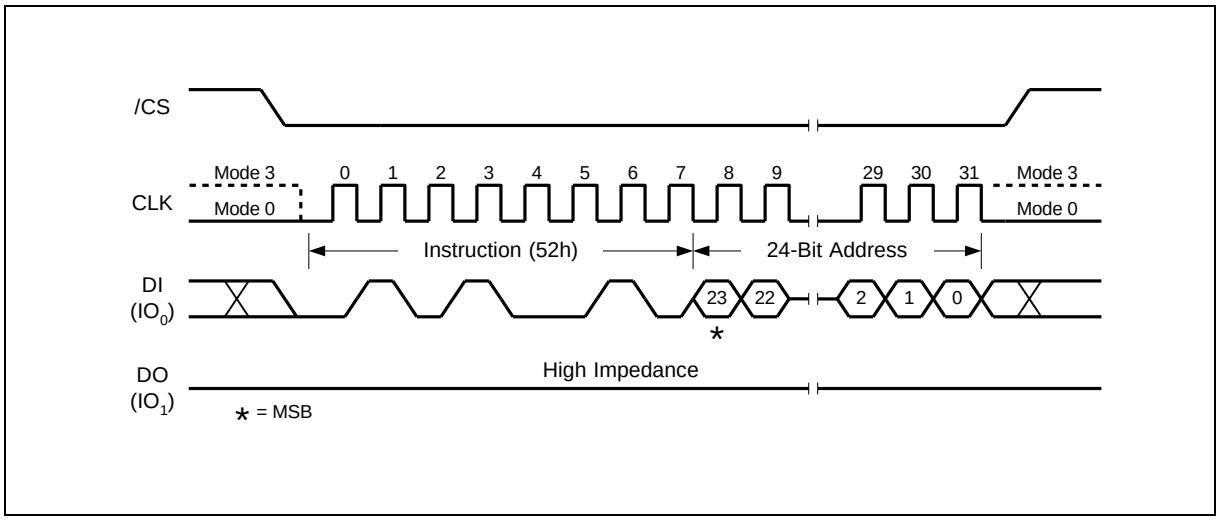


Figure 16. 32KB Block Erase Instruction Sequence Diagram

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8.1.24 Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0) (see Figure 2). The Block Erase instruction sequence is shown in figure 17.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP1, and BP0) bits (see Status Register Memory Protection table).

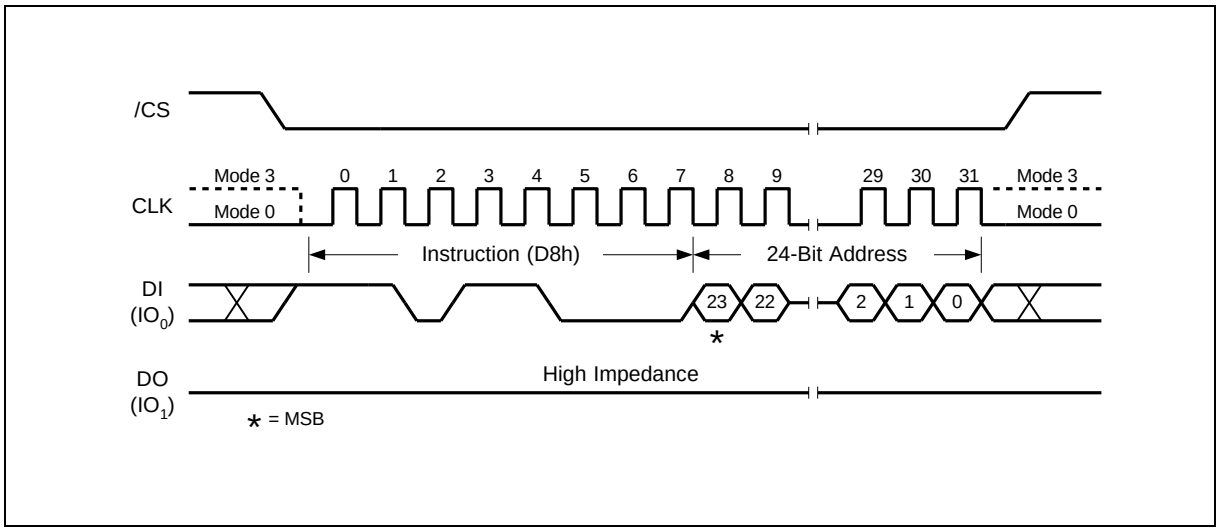


Figure 17. Block Erase Instruction Sequence Diagram

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8.1.25 Chip Erase (C7h or 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in figure 18.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (TB, BP1 and BP0) bits (see Status Register Memory Protection table).

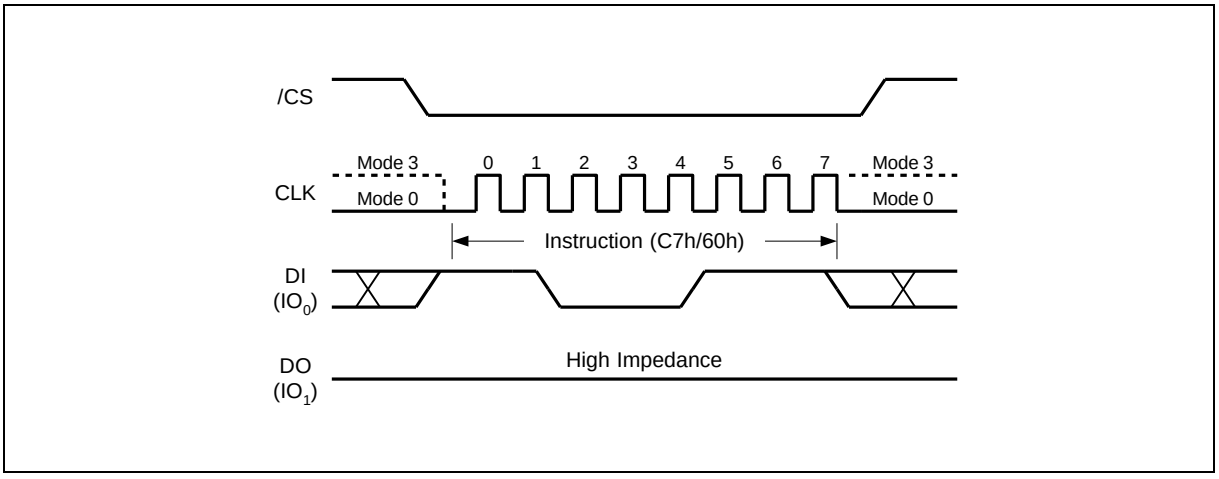


Figure 18. Chip Erase Instruction Sequence Diagram

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8.1.26 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in figure 19.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

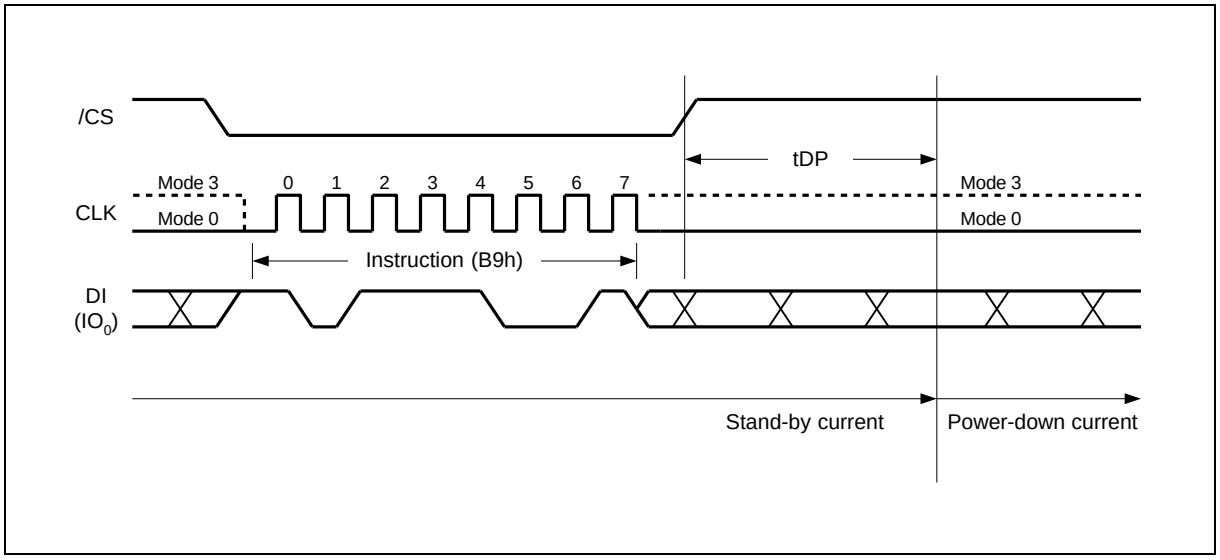


Figure 19. Deep Power-down Instruction Sequence Diagram

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8.1.27 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, obtain the devices electronic identification (ID) number or do both.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in figure 20. Release from power-down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 20. The Device ID values for the W25X05CL are listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in figure 21, except that after /CS is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted.

If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle

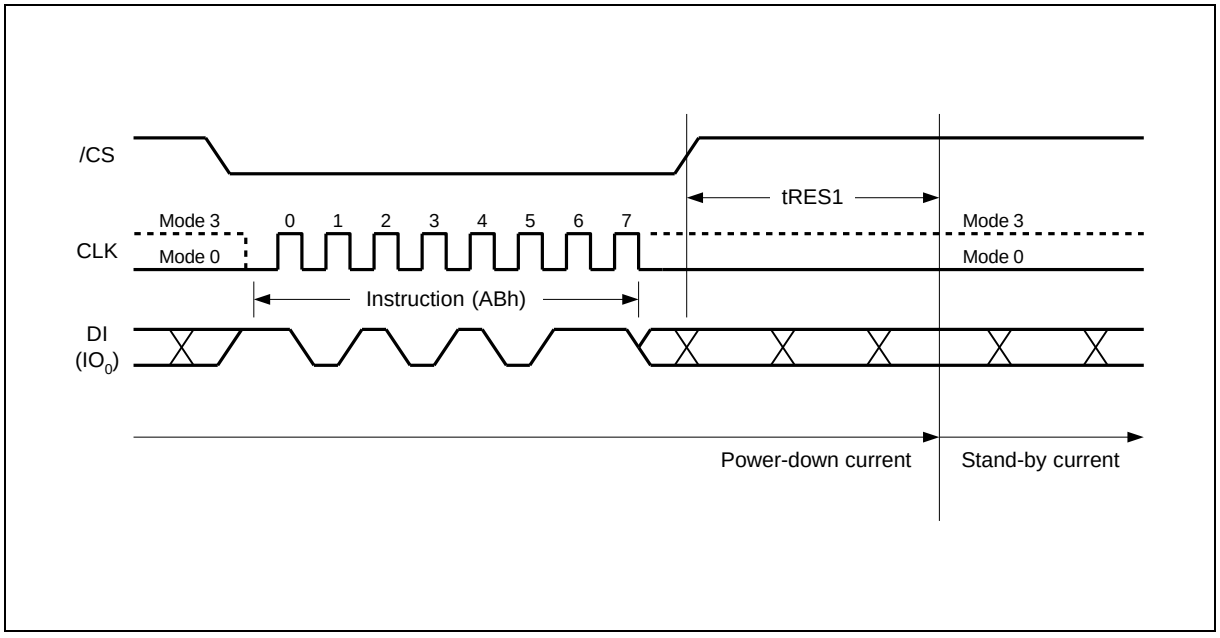


Figure 20. Release Power-down Instruction Sequence

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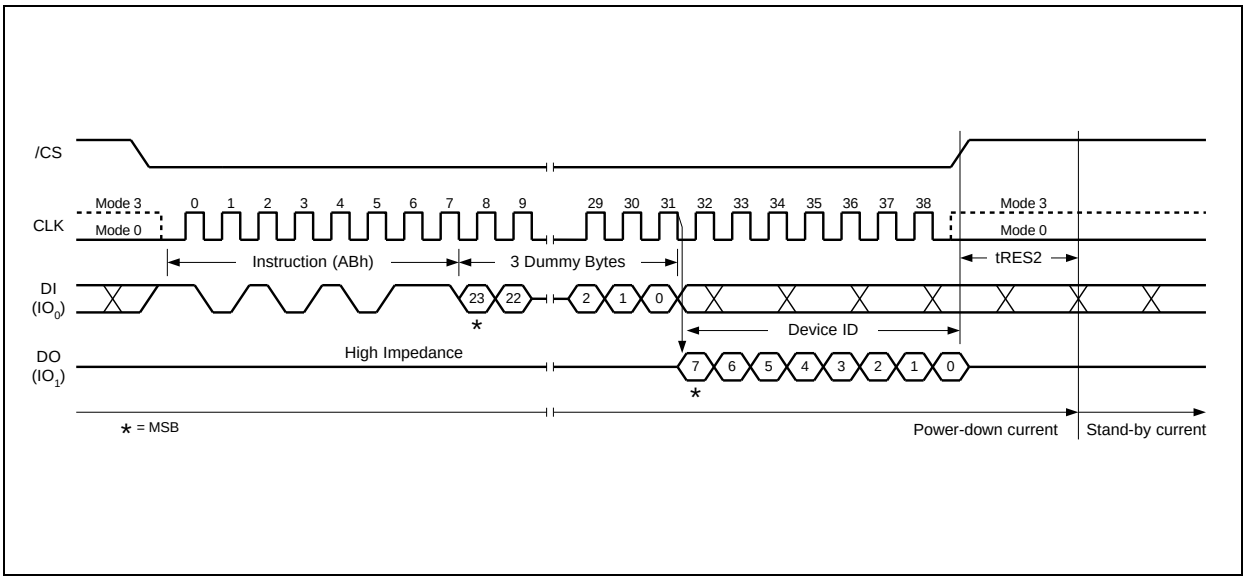


Figure 21. Release Power-down / Device ID Instruction Sequence Diagram

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8.1.28 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down/ Device ID instruction that provides both JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 22. The Device ID values for the W25X05CL are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

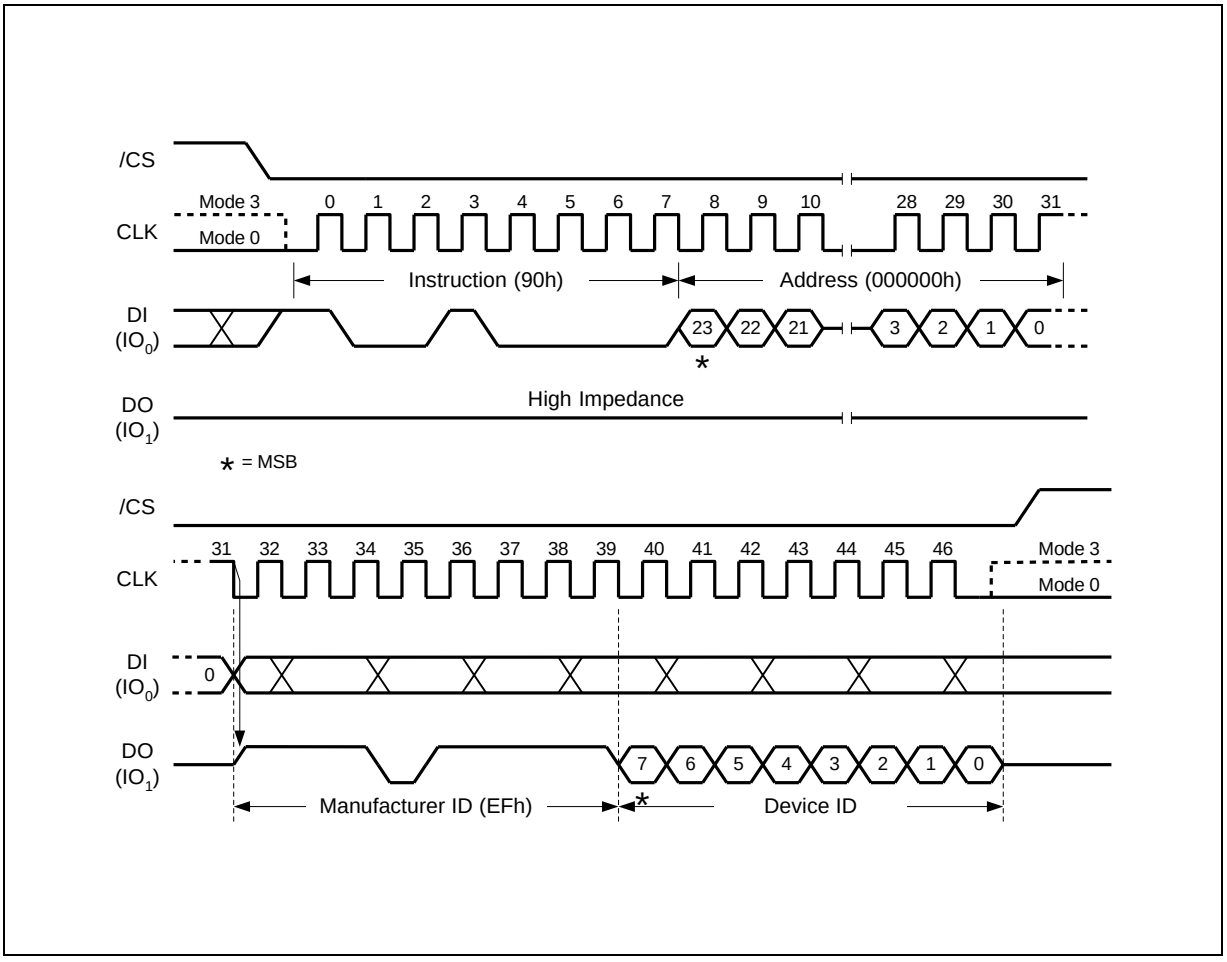


Figure 22. Read Manufacturer / Device ID Diagram

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8.1.29 Read Manufacturer / Device ID Dual I/O (92h)

The Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24-bit address (A23-A0) of 000000h, 8-bit Continuous Read Mode Bits, with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in figure 28. The Device ID values for the W25X05CL are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

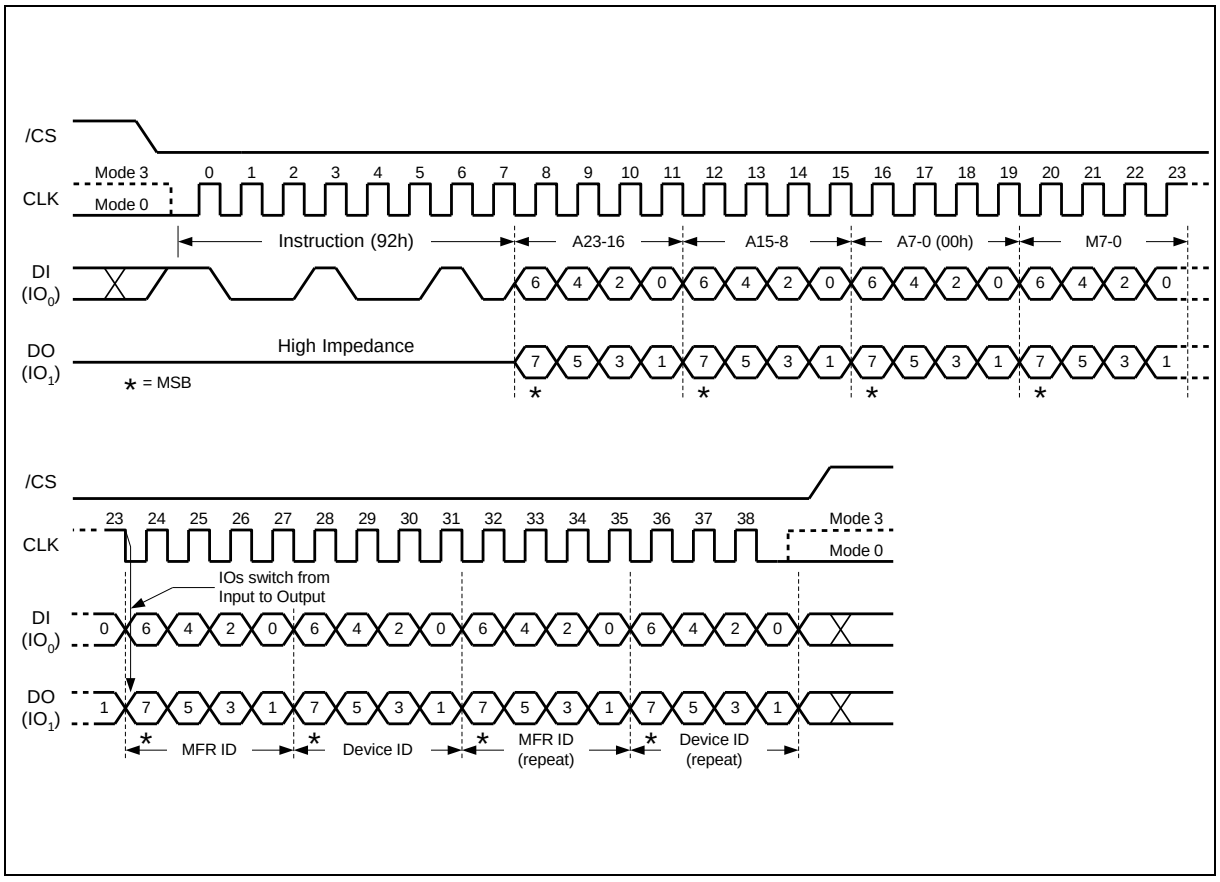


Figure 23. Read Manufacturer / Device ID Dual I/O Diagram

Note:

1. “Continuous Read Mode” bits M7-0 must be set to FXh to be compatible with Fast Read Dual I/O instruction.

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8.1.30 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each W25X05CL device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in figure 24.

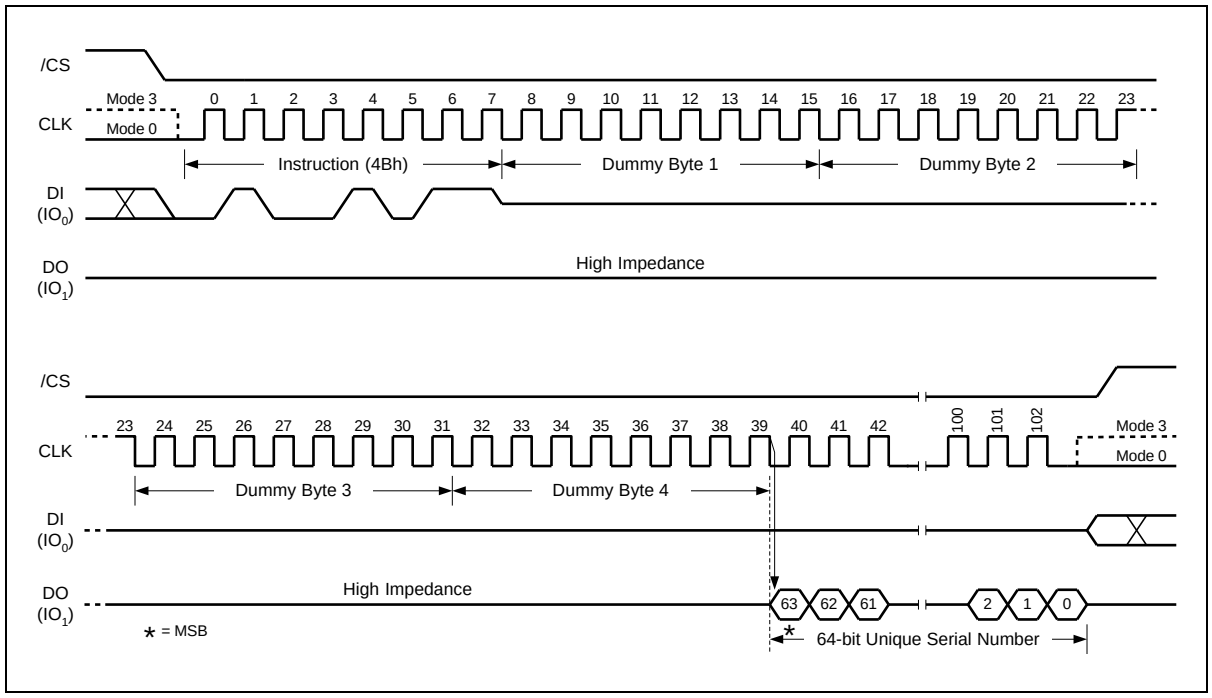


Figure 24. Read Unique ID Number Instruction Sequence

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8.1.31 JEDEC ID (9Fh)

For compatibility reasons, the W25X05CL provide several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 25. For memory type and capacity values refer to Manufacturer and Device Identification table.

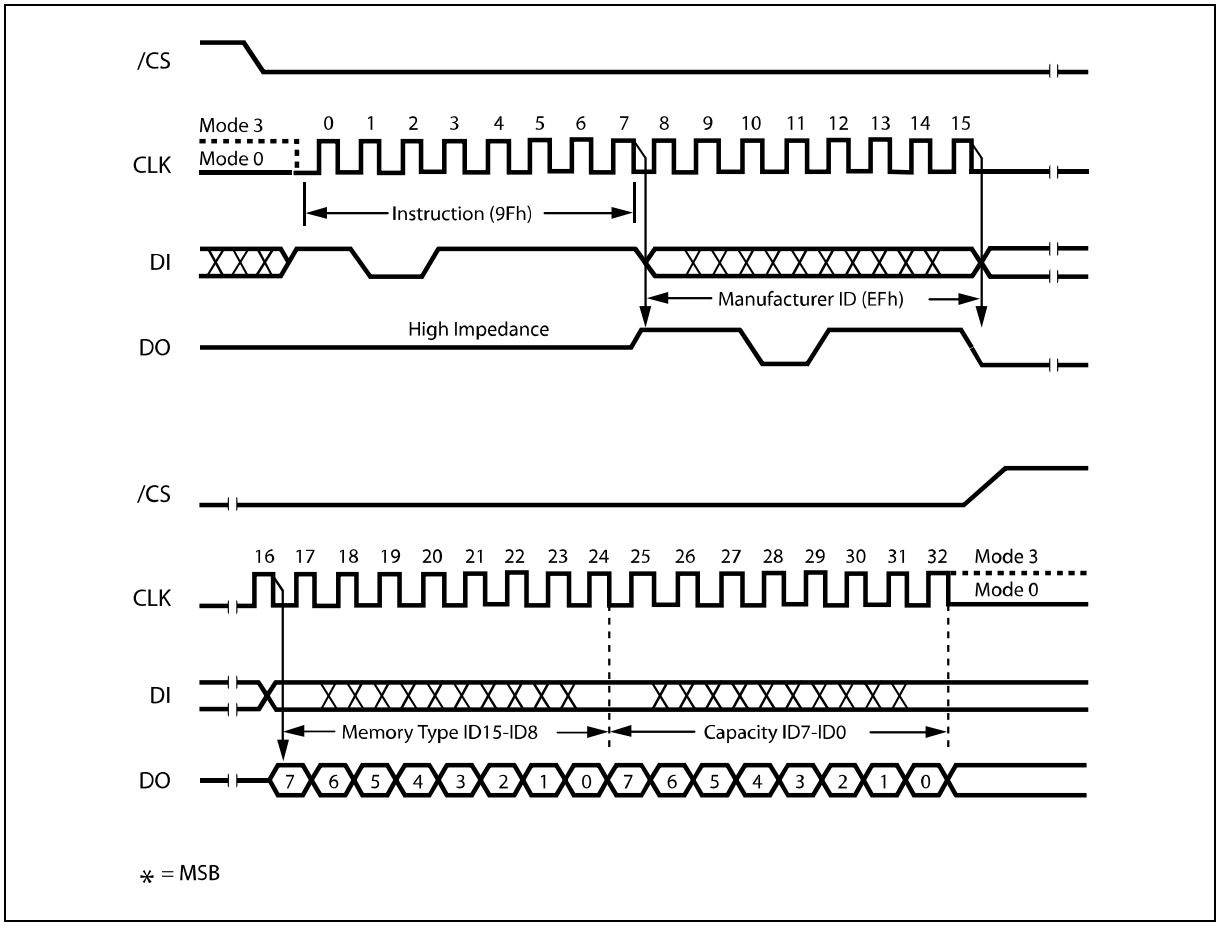


Figure 25. Read JEDEC ID

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9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Rating(1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	**VCC**		–0.6 to +4.6	V
Voltage Applied to Any Pin	**VIO**	Relative to Ground	–0.6 to VCC +0.4	V
Transient Voltage on any Pin	**VIOT**	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	**TSTG**		–65 to +150	°C
Lead Temperature	**TLEAD**		See Note (2)	°C
Electrostatic Discharge Voltage	**VESD**	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	**VCC**	F_R = 80MHz, f_R = 33MHz F_R = 104MHz, f_R = 50MHz	2.3 2.7	2.7 3.6	V
Ambient Temperature, Operating	**TA**	Industrial	–40	+85	°C

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9.3 Power-up Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}(1)	10		µs
Time Delay Before Write Instruction	t_{PUW}(1)	5		ms
Write Inhibit Threshold Voltage	V_{WI}(1)	1.0	2.0	V

Note:

1. These parameters are characterized only.

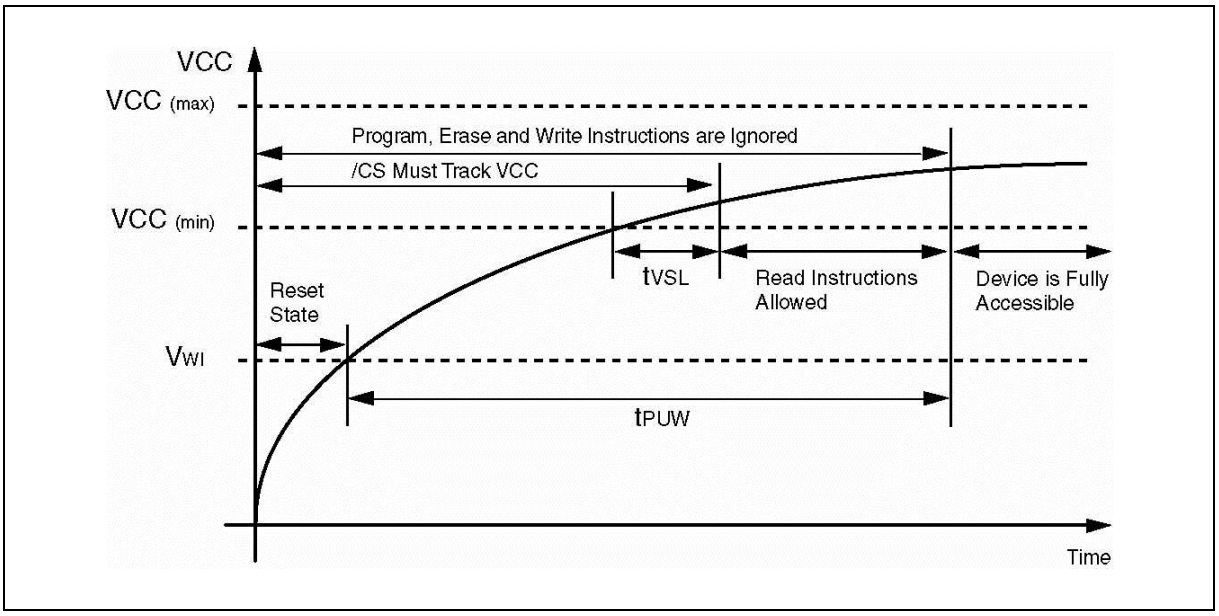


Figure 26a. Power-up Timing and Voltage Levels

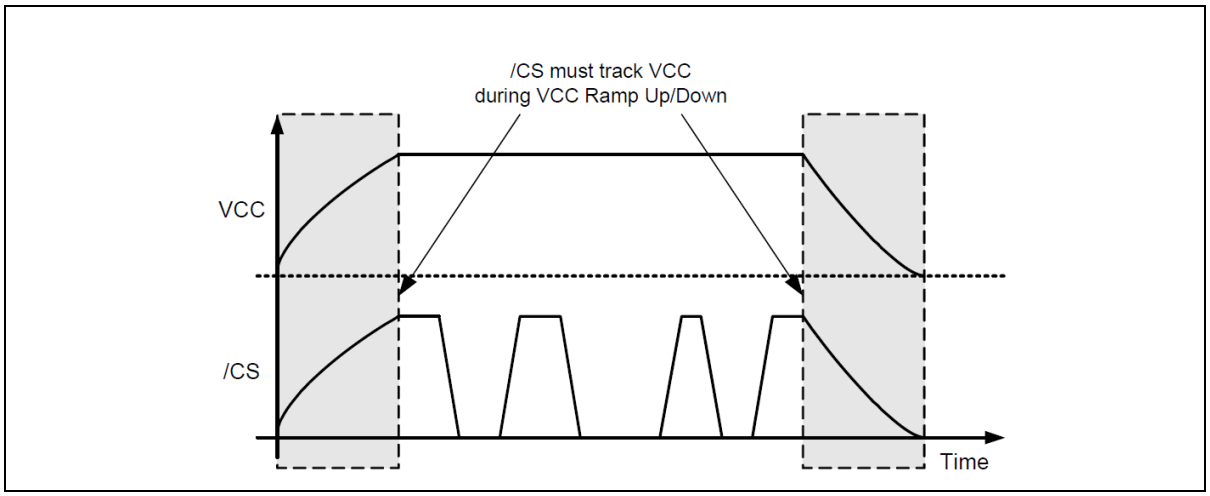


Figure 26b. Power-up, Power-Down Requirement

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9.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}[1]	V_{IN} = 0V[2]			6	pF
Output Capacitance	C_{OUT}[1]	V_{OUT} = 0V[2]			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		10	50	µA
Power-down Current	I_{CC2}	/CS = VCC, VIN = GND or VCC		1	5	µA
Current Read Data / Dual Output 1MHz[2]	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		1/3	4/8	mA
Current Read Data / Dual Output 33MHz[2]	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		4/5	8/10	mA
Current Read Data / Dual Output 80MHz[2]	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		5/6	10/12	mA
Current Read Data / Dual Output 104MHz[2]	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		6/7	12/14	mA
Current Write Status Register	I_{CC4}	/CS = VCC		8	12	mA
Current Page Program	I_{CC5}	/CS = VCC		10	15	mA
Current Sector/Block Erase	I_{CC6}	/CS = VCC		10	15	mA
Current Chip Erase	I_{CC7}	/CS = VCC		10	15	mA
Input Low Voltage	V_{IL}		–0.5		VCCx0.3	V
Input High Voltage	V_{IH}		VCCx0.7			V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC–0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA=25°C, VCC=3.0V.
2. Checker Board Pattern.

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9.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

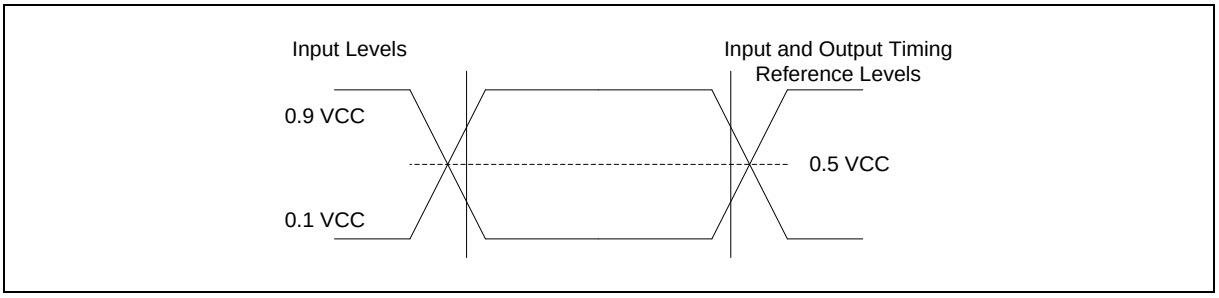


Figure 27. AC Measurement I/O Waveform

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9.6 AC Electrical Characteristics

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for all instructions, except Read Data (03h) 2.7V-3.6V VCC & Industrial Temperature	**F_R**	f_c	D.C.		104	MHz
Clock frequency for all instructions, except Read Data (03h) 2.3V-2.7V VCC & Industrial Temperature	**F_R**	f_c	D.C.		80	MHz
Clock freq. Read Data instruction 03h 2.7V-3.6V VCC & Industrial Temperature	**f_R**		D.C.		50	MHz
Clock freq. Read Data instruction 03h 2.3V-2.7V VCC & Industrial Temperature	**f_R**		D.C.		33	MHz
Clock High, Low Time, for Fast Read (0Bh, 3Bh) / other instructions except Read Data (03h)	**t_{CLH}, t_{CLL}(1)**		4			ns
Clock High, Low Time for Read Data (03h) instruction	**t_{CRLH}, t_{CRLL}(1)**		6			ns
Clock Rise Time peak to peak	**t_{CLCH}(2)**		0.1			V/ns
Clock Fall Time peak to peak	**t_{CHCL}(2)**		0.1			V/ns
/CS Active Setup Time relative to CLK	**t_{SLCH}**	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	**t_{CHSL}**		5			ns
Data In Setup Time	**t_{DVCH}**	t_{DSU}	2			ns
Data In Hold Time	**t_{CHDX}**	t_{DH}	5			ns
/CS Active Hold Time relative to CLK	**t_{CHSH}**		5			ns
/CS Not Active Setup Time relative to CLK	**t_{SHCH}**		5			ns
/CS Deselect Time (for Array Read → Array Read)	**t_{SHSL1}**	t_{CSH}	50			ns
/CS Deselect Time (for Erase/Program → Read SR) Volatile Status Register Write Time	**t_{SHSL2}**	t_{CSH}	100 50			ns
Output Disable Time	**t_{SHQZ}(2)**	t_{DIS}			7	ns
Clock Low to Output Valid	**t_{CLQV1}**	t_{V1}			8	ns
Clock Low to Output Valid (for Read ID instructions)	**t_{CLQV2}**	t_{V2}			8	ns

Continued – next page

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AC Electrical Characteristics (cont'd)

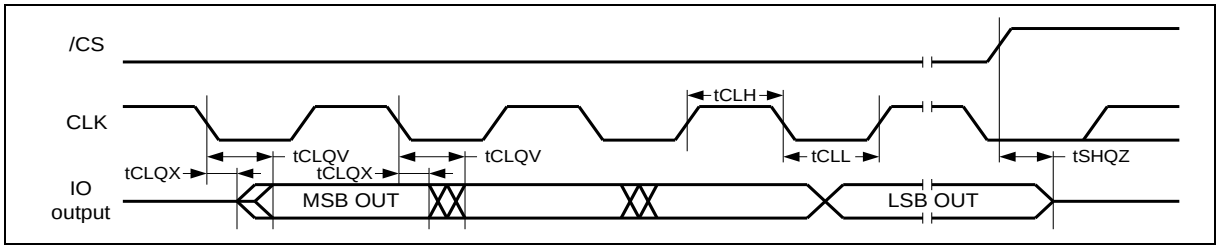
DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Output Hold Time	t_{CLQX}	tHO	0			ns
/HOLD Active Setup Time relative to CLK	t_{HLCH}		5			ns
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	t_{HHQX}(2)	tLZ			7	ns
/HOLD to Output High-Z	t_{HLQZ}(2)	tHZ			12	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}(3)		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}(3)		100			ns
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without Electronic Signature Read	t_{RES1}(2)				3	µs
/CS High to Standby Mode with Electronic Signature Read	t_{RES2}(2)				1.8	µs
Write Status Register Time	t_W			10	15	ms
Byte Program Time (First Byte) (4)	t_{BP1}			15	30	µs
Additional Byte Program Time (After First Byte) (4)	t_{BP2}			2.5	5	µs
Page Program Time	t_{PP}			0.4	0.8	ms
Sector Erase Time (4KB)	t_{SE}			30	300	ms
Block Erase Time (32KB)	t_{BE_1}			120	800	ms
Block Erase Time (64KB)	t_{BE_2}			150	1,000	ms
Chip Erase Time W25X05CL	t_{CE}			0.25	1	s

Notes:

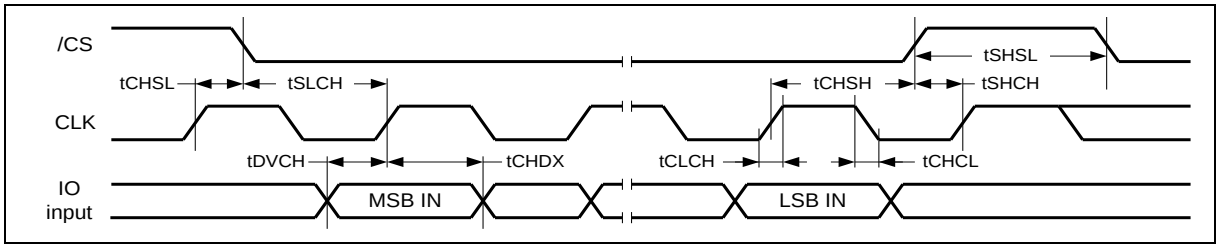
1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP is set to 1.
4. For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.

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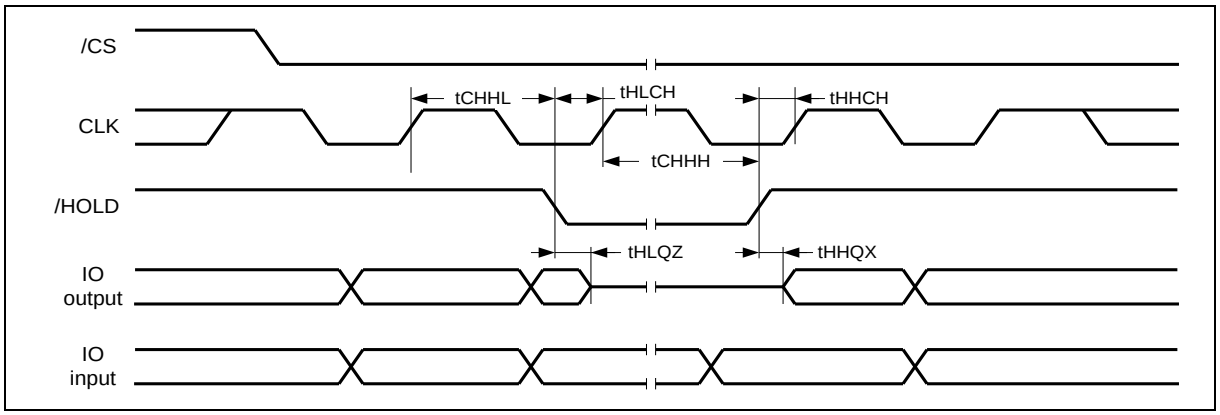
9.7 Serial Output Timing



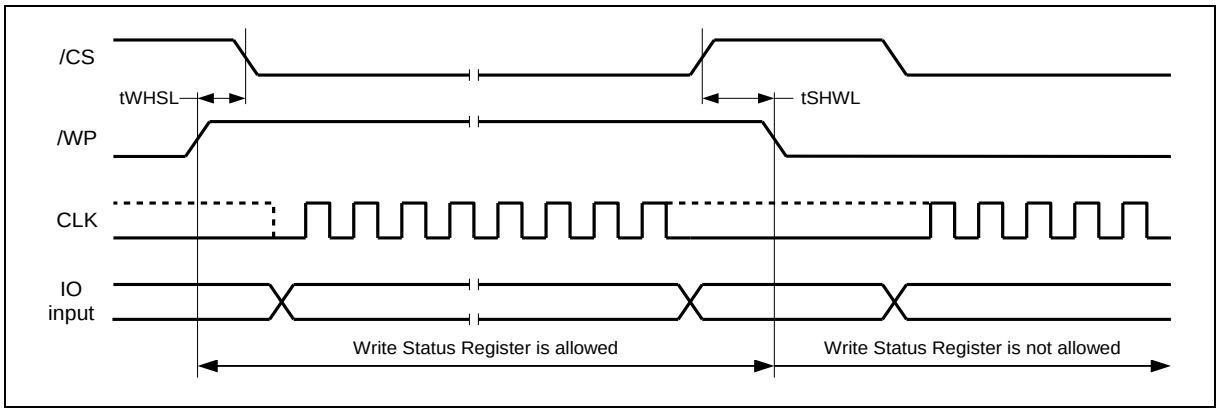
9.8 Serial Input Timing



9.9 /HOLD Timing



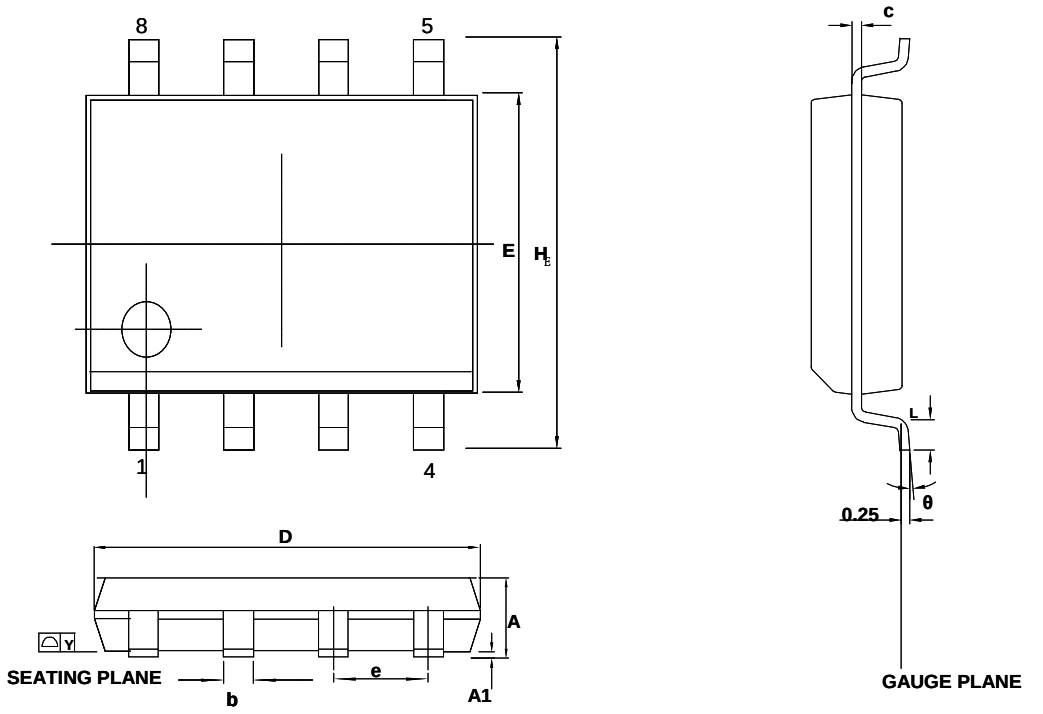
9.10 /WP Timing



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10. PACKAGE SPECIFICATION

10.1 8-Pin SOIC 150-mil (Package Code SN)

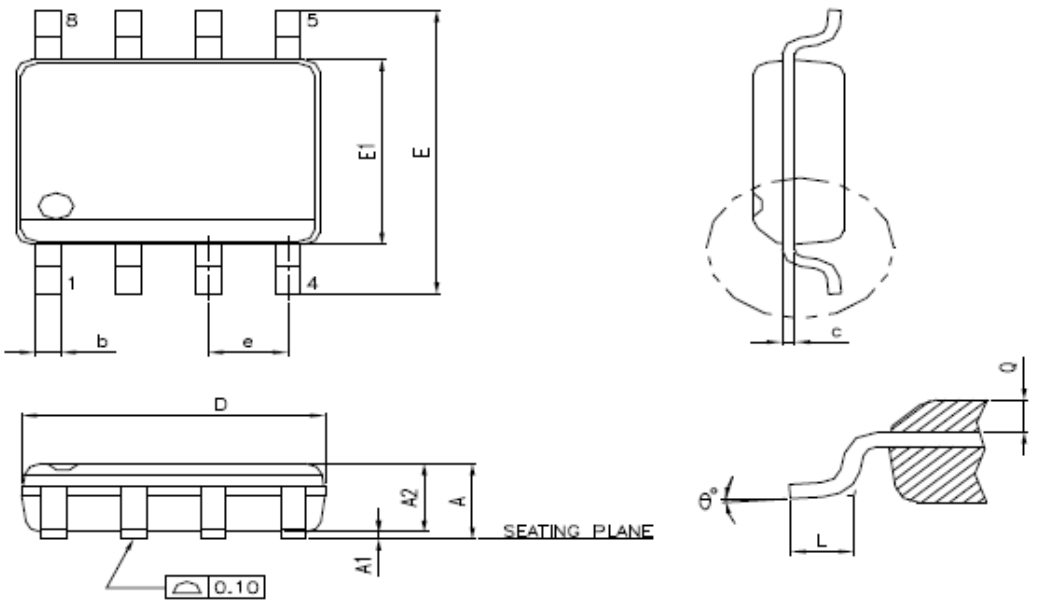


SYMBOL	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E(3)	3.80	4.00	0.150	0.157
D(3)	4.80	5.00	0.188	0.196
e(2)	1.27 BSC		0.050 BSC	
H_E	5.80	6.20	0.228	0.244
Y(4)	-	0.10	-	0.004
L	0.40	1.27	0.016	0.050
θ°	0°	10°	0°	10°

Notes:
1. Controlling dimensions: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads coplanarity with respect to seating plane shall be within 0.004 inches.

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10.2 8-Pin VSOP8 150-mil (Package Code SV)



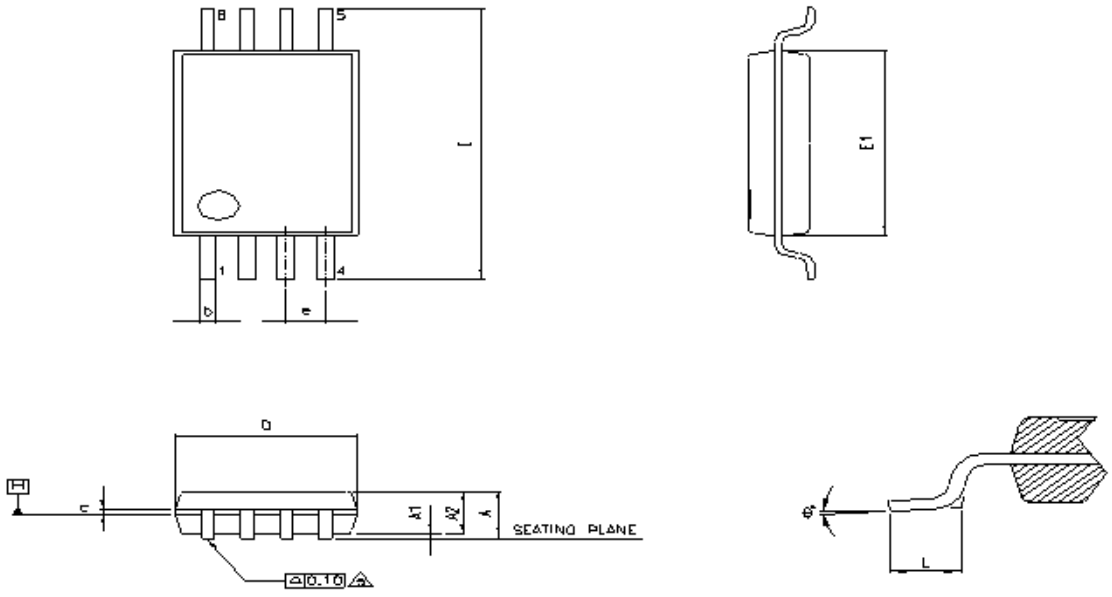
SYMBOL	MILLIMETER			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	—	—	0.90	—	—	0.035
A1	0.01	0.05	—	0.0004	0.002	—
A2	—	0.8	—	—	0.031	—
Q	0.19	0.20	0.21	0.007	0.008	0.008
b	0.33	—	0.51	0.33	—	0.020
c	0.125 BSC			0.005 BSC		
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27BSC			0.050 BSC		
L	0.40	0.71	1.27	0.016	0.028	0.050
θ	0°	—	10°	0°	—	10°

Notes:

1. Dimension “D” does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.018 inches [0.15mm] per side.
2. Dimension “E1” does not include interlead Flash, interlead Flash shall not exceed 0.010 inches [0.25mm] per side.

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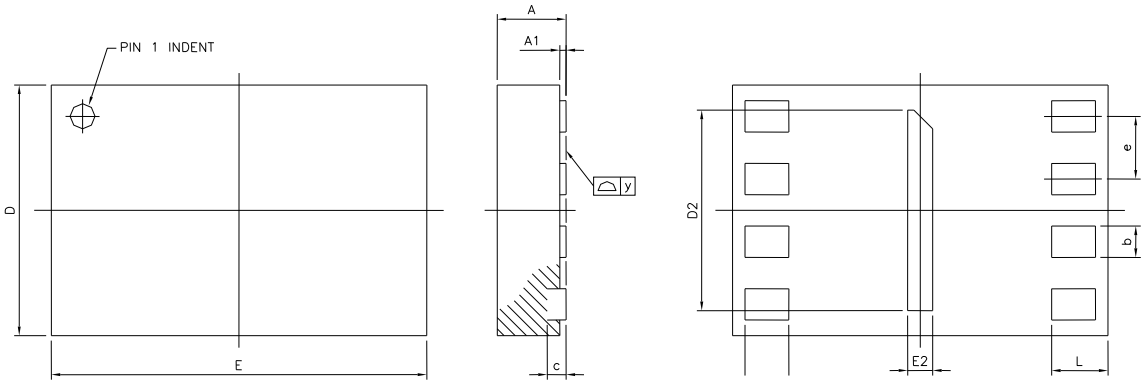
10.3 8-Pin TSSOP8 173-mil (Package Code SD)



SYMBOL	MILLIMETER			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.030	0.040	0.041
D	2.90	3.00	3.10	0.114	0.118	0.122
E		6.40 BSC			0.252 BSC	
E1	4.30	4.40	4.50	0.169	0.173	0.177
L	0.45	0.60	0.75	0.0177	0.0236	0.295
θ°	0°	—	8°	0°	—	8°
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.003	—	0.008
e		0.65 BSC			0.026 BSC	
L1		1.00 REF			0.039 REF	

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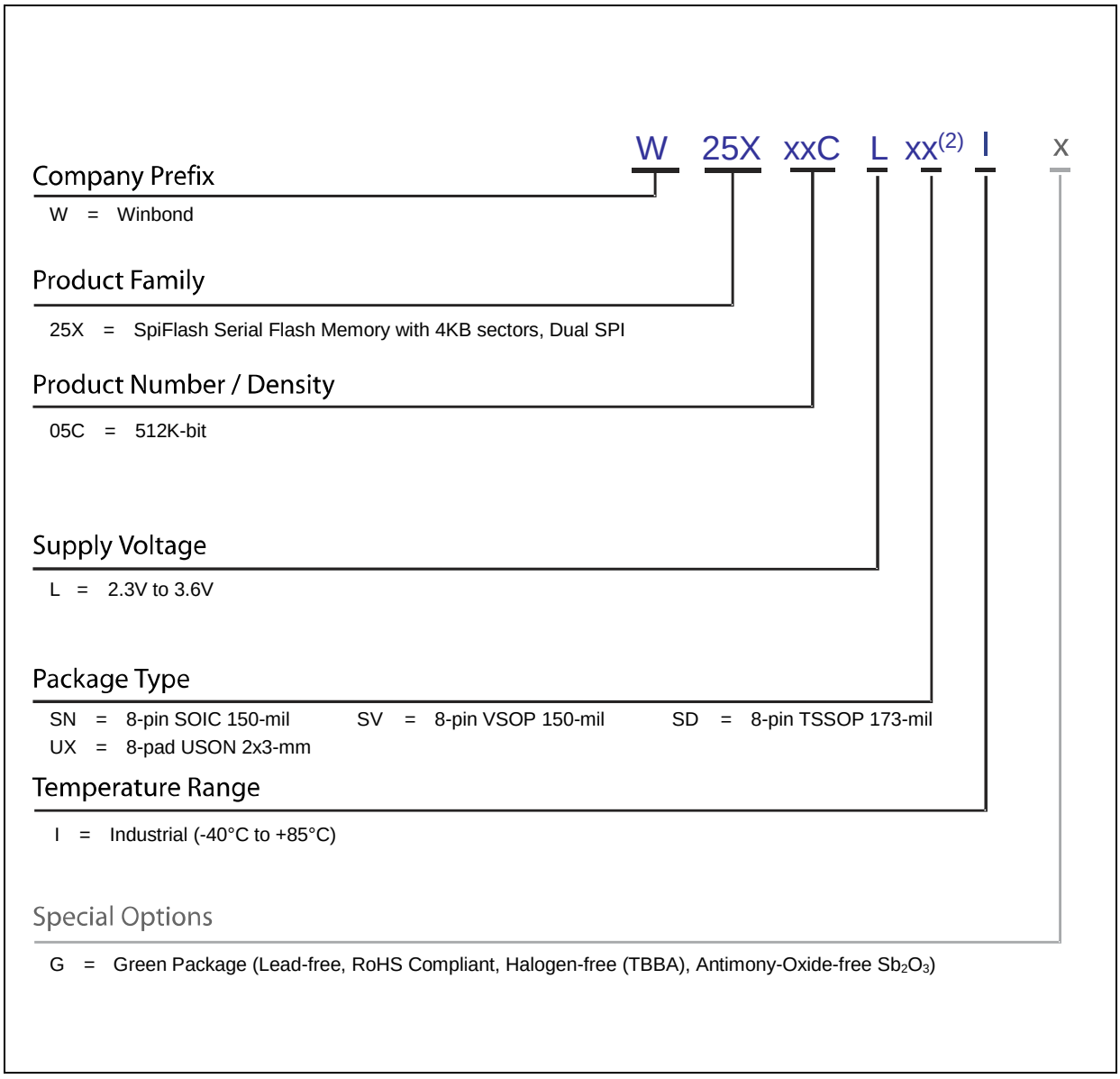
10.4 8-Pad USON 2x3-mm (Package Code UX)



SYMBOL	MILLIMETER			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
C	—	0.15 REF	—	—	0.006 REF	—
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	1.55	1.60	1.65	0.061	0.063	0.065
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	0.15	0.20	0.25	0.006	0.008	0.010
e	—	0.50	—	—	0.020	—
L	0.40	0.45	0.50	0.016	0.018	0.020
L1	—	0.10	—	—	0.004	—
L3	0.30	0.35	0.40	0.012	0.014	0.016
y	0.00	—	0.075	0.000	—	0.003

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Tel:150-1290-5940
Email:sales@manduic.com

11. ORDERING INFORMATION(1)



Notes:

1a. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T) or Tray (shape S), when placing orders.

1b. The "W" prefix is not included on the part marking.

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11.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25X05CL SpiFlash Memories. Please contact *Winbond* for specific availability by density and package type. *Winbond* SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated number less than 10-digit.

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150-mil	512K-bit	W25X05CLSNIG	25X05CLNIG
SV VSOP-8 150-mil	512K-bit	W25X05CLSVIG	25X05CLVIG
SD TSSOP 173-mil	512K-bit	W25X05CLSDIG	25X05CLDIG
UX(1) USON-8 2X3mm	512K-bit	W25X05CLUXIG	0Hxxx 0Gxxx

Notes:

1. USON package type UX has special top marking due to size limitation.
   0 = 512Kb, H = W25X C series; 2.5V; 0 = Standard parts, G = Green

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12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	2012/08/06	All	New Create
B	2012/08/28	P.46	Update WSON package specification
C	2012/10/15	P.44	Update VSOP package specification
D	2012/11/13	All	Remove WSON package specification
E	2012/11/28	P.46	Update USON package specification

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Tel:150-1290-5940
Email:sales@manduic.com