3.0V 1G-BIT (DUAL DIE) SERIAL NOR FLASH MEMORY WITH DUAL/QUAD SPI, QPI & DTR

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1. GENERAL DESCRIPTIONS

The W25Q01JV (two x 512M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 1µA for power-down. All devices are offered in space-saving packages.

The W25Q01JV device is a two 512M-bit stack die that supports linear addressing for the full 1G-bit memory address range.

The W25Q01JV array is organized into 524,288 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q01JV has 32,768 erasable 4KB sectors and 2,048 erasable 64KB blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

The W25Q01JV support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI, Quad Peripheral Interface (QPI) as well as Double Transfer Rate (DTR): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 133MHz are supported allowing equivalent clock rates of 266MHz (133MHz x 2) for Dual I/O and 532MHz (133MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

Each 512M-bit die also has their individual (independent) 'Status only' Status Register bits including BUSY bit, SUS bit ,that provides the current state of the die.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

2. FEATURES

- **New Family of SpiFlash Memories**
  - W25Q01JV: two 1G-bit / 128M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - SPI/QPI DTR (Double Transfer Rate) Read
  - 3 or 4-Byte Addressing Mode
  - Software & Hardware Reset(1)
- **Highest Performance Serial Flash**
  - 133MHz Standard/Dual/Quad SPI clocks
  - 266/532MHz equivalent Dual/Quad SPI
  - 66MB/S continuous data transfer rate
  - Min. 100K Program-Erase cycles
  - More than 20-year data retention
- **Low Power, Wide Temperature Range**
  - Single 2.7V to 3.6V supply
  - <2µA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down
  - Special OTP protection
  - Top/Bottom, Complement array protection
  - Individual Block/Sector array protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Bytes Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging(2)**
  - 8-pad WSON 8x6-mm
  - 16-pin SOIC 300-mil (additional /RESET pin)
  - 24-ball TFBGA 8x6-mm(5x5 ball array)
  - Contact Winbond for KGD and other options

Note: 1. Hardware /RESET pin is only available on TFBGA or SOIC16 packages
2. Please contact Winbond for other packages.

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3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1 Pad Configuration WSON 8x6-mm

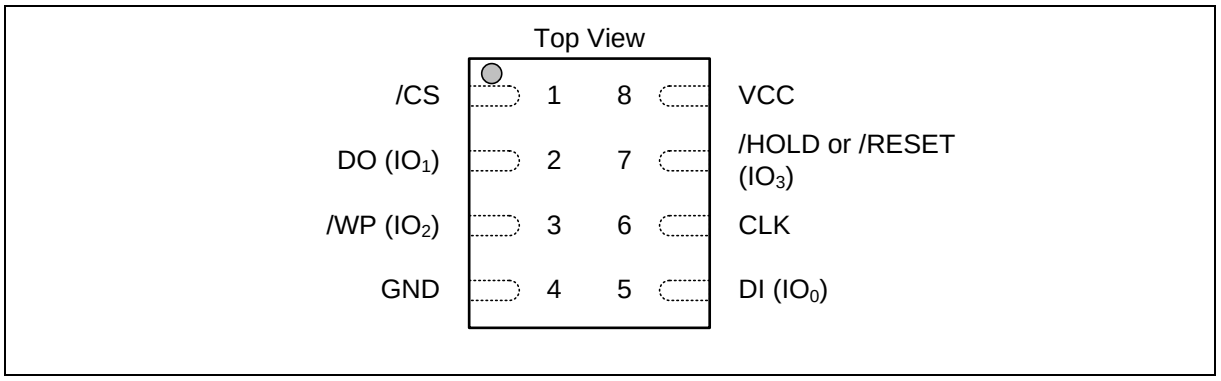


Figure 1a. W25Q01JV Pad Assignments, 8-pad WSON 8x6-mm (Package Code ZE)

3.2 Pad Description WSON 8x6-mm

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

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3.3 Pin Configuration SOIC 300-mil

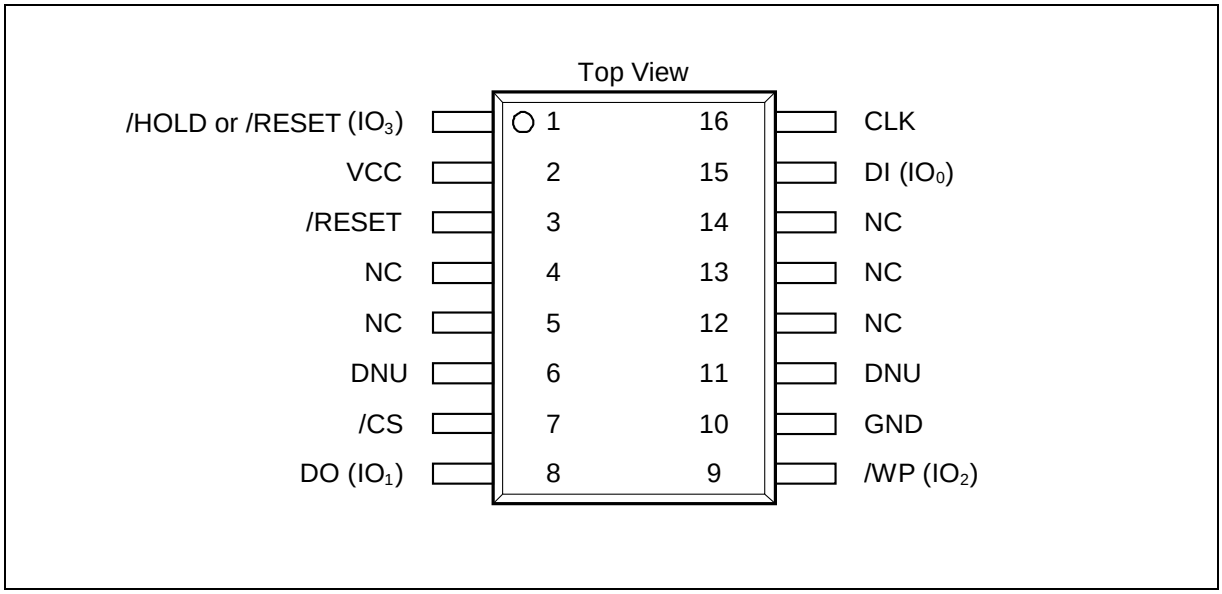


Figure 1b. W25Q512JV Pin Assignments, 16-pin SOIC 300-mil (Package Code F)

3.1 Pin Description SOIC 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
2	VCC		Power Supply
3	/RESET	I	Reset Input(3)
4	N/C		No Connect
5	N/C		No Connect
6	DNU		Do Not Use
7	/CS	I	Chip Select Input
8	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
9	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
10	GND		Ground
11	DNU		Do Not Use
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
16	CLK	I	Serial Clock Input

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

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3. The /RESET pin on SOIC-16 package is a dedicated hardware reset pin regardless of device settings. If the reset function is not used, this pin can be left floating in the system.

3.2 Ball Configuration TFBGA 8x6-mm (5x5 Ball Array)

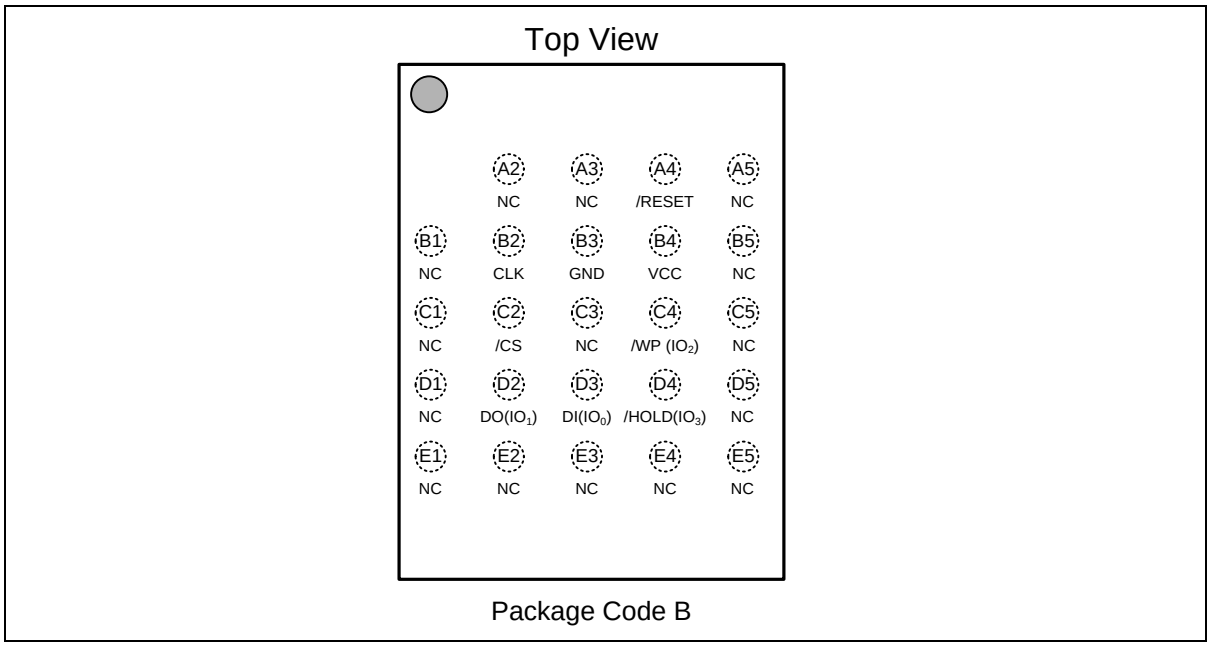


Figure 1c. W25Q01JV Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code B)

3.3 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
A4	/RESET	I	Reset Input(3)
B2	CLK	I	Serial Clock Input
B3	GND		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
D2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
D3	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
D4	/HOLD (IO3) /RESET	I/O	Hold or Reset Input (Data Input Output 3)(2)
Multiple	NC		No Connect / DNU (Do Not Use)

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions

2. IO0 – IO3 are used for Quad SPI instructions (factory default for Quad Enabled part numbers with ordering option “IQ”).

3. The /RESET pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, this pin can be left floating or connected to VCC in the system.

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4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 58). If needed a pull-up resistor on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q01JV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, TB, BP3, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See Figure 1a-c for the pin configuration of Quad I/O operation.

4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See Figure 1a-c for the pin configuration of Quad I/O operation.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

4.6 Reset (/RESET)

The /RESET pin allows the device to be reset by the controller. For 8-pin packages, when QE=0, the IO3 pin can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. When QE=1, the /HOLD or /RESET function is not available for 8-pin configuration.

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A dedicated hardware /RESET pin is available on SOIC-16 and TFBGA packages. When it's driven low for a minimum period of ~1µS, this device will terminate any external or internal operations and return to its power-on state.

Note: Hardware /RESET pin is available on SOIC-16 or TFBGA; please contact Winbond for this package.

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5. BLOCK DIAGRAM

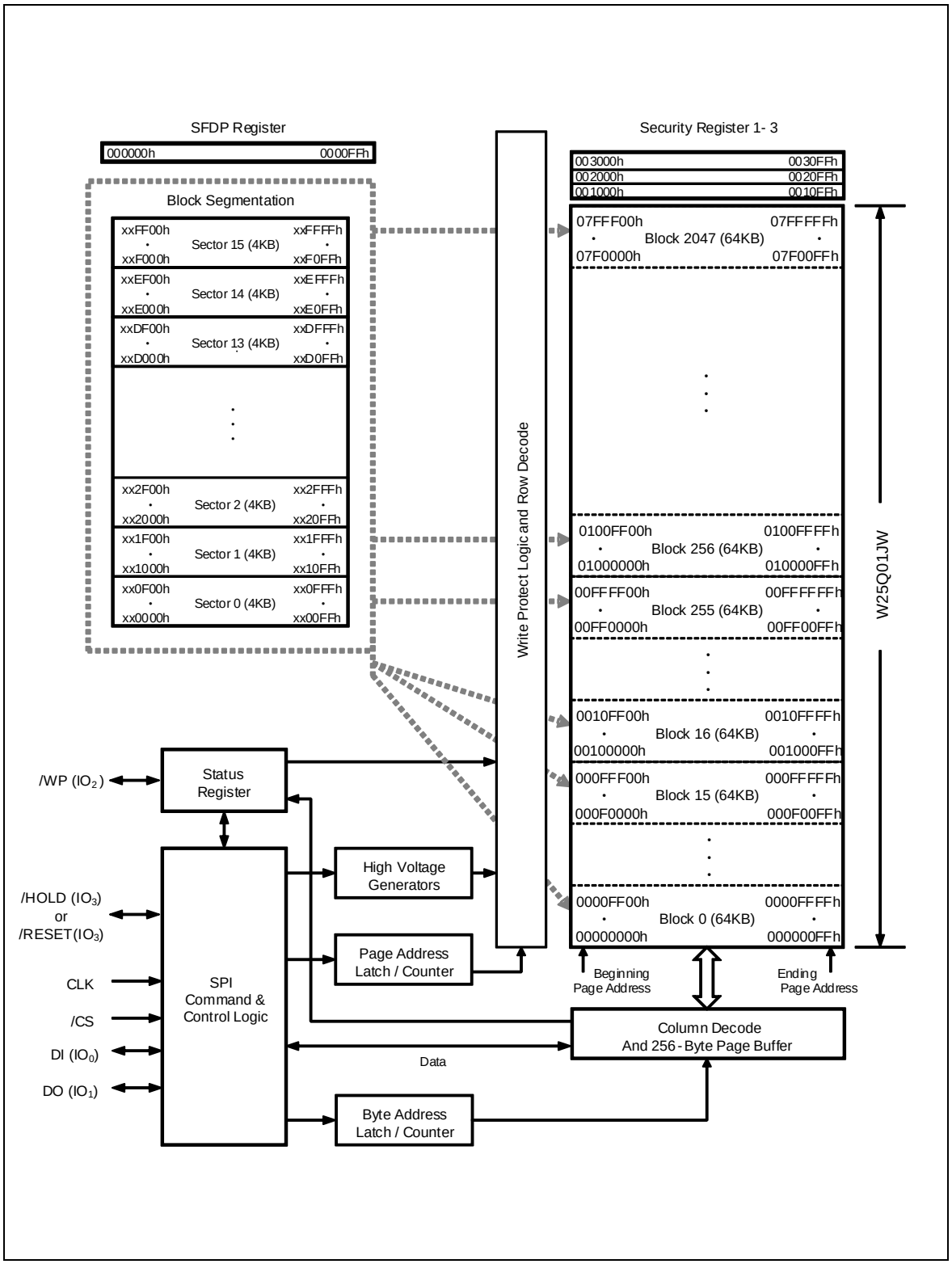
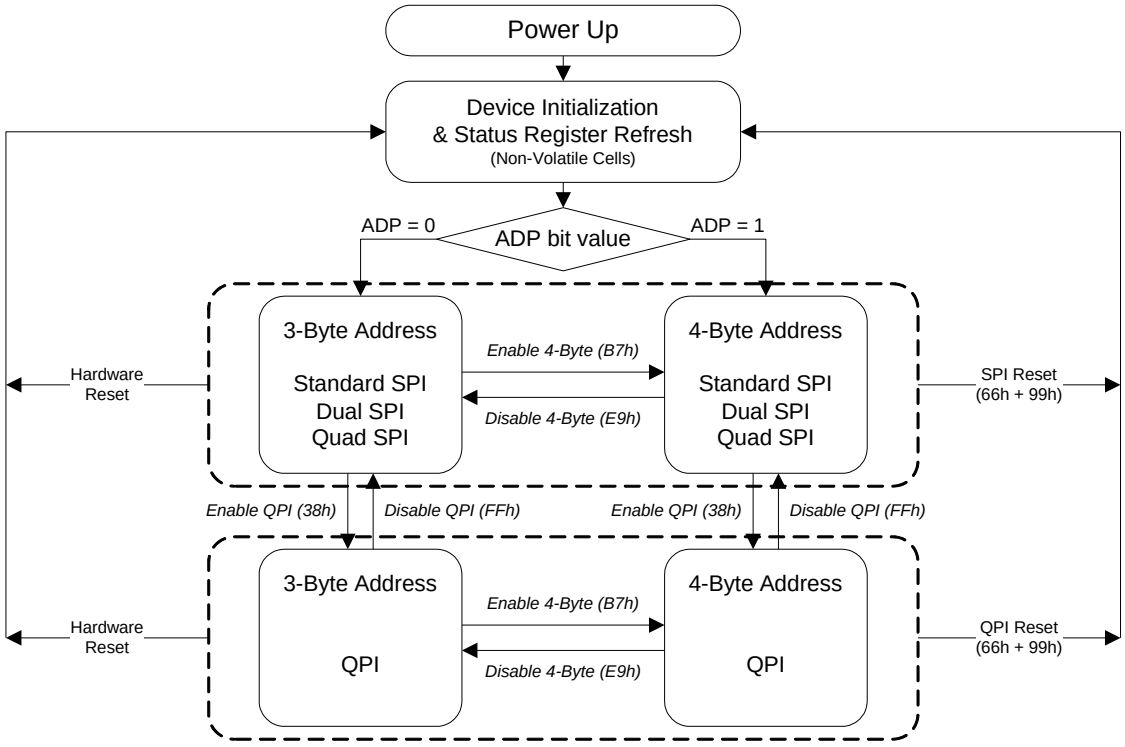


Figure 2. W25Q01JV Serial Flash Memory Block Diagram

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6. FUNCTIONAL DESCRIPTIONS

6.1 SPI / QPI Operations



Note: ADP bit in the Status Register is only used to determine 3-Byte or 4-Byte address modes during power up. Changing ADP bit value will not switch the address modes during normal operation.

Figure 3. W25Q01JV Serial Flash Memory Operation Diagram

6.1.1 Standard SPI Instructions

The W25Q01JV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.2 Dual SPI Instructions

The W25Q01JV supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

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6.1.3 Quad SPI Instructions

The W25Q01JV supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.1.4 QPI Instructions

The W25Q01JV supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” instruction, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See Figure 3 for the device operation modes.

6.1.5 SPI / QPI DTR Read Instructions

To effectively improve the read operation throughput without increasing the serial clock frequency, W25Q01JV introduces multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

6.1.6 3-Byte / 4-Byte Address Modes

Upon power up, the W25Q01JV can operate in either 3-Byte Address Mode or 4-Byte Address Mode, depending on the Non-Volatile Status Register Bit ADP (S17) setting. If ADP=0, the device will operate in 3-Byte Address Mode; if ADP=1, the device will operate in 4-Byte Address Mode. The factory default value for ADP is 0.

To switch between the 3-Byte or 4-Byte Address Modes, “Enter 4-Byte Mode (B7h)” or “Exit 4-Byte Mode (E9h)” instructions must be used. The current address mode is indicated by the Status Register Bit ADS (S16).

W25Q01JV also supports a set of basic SPI instructions which requires dedicated 4-Byte address regardless the device Address Mode setting. Please refer to Instruction Set Tables for details.

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6.1.7 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25Q01JV operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as /HOLD pin or data I/O pin. When QE=0 (factory default), the pin is /HOLD, when QE=1, the pin will become an I/O pin, /HOLD function is no longer available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.1.8 Software Reset & Hardware /RESET pin

The W25Q01JV can be reset to the initial power-on state by a software Reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS (t_{RST}) to reset. No command will be accepted during the reset period.

For the WSON-8 package types, W25Q01JV can also be configured to utilize a hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for /HOLD pin function or /RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Drive the /RESET pin low for a minimum period of ~1us (tRESET*) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any command input.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pins.

For the SOIC-16 & TFBGA package, W25Q01JV provides a dedicated /RESET pin in addition to the /HOLD (IO_3) pin as illustrated in Figure 1b. Drive the /RESET pin low for a minimum period of ~1us (tRESET*) will reset the device to its initial power-on state. The HOLD/RST bit or QE bit in the Status Register will not affect the function of this dedicated /RESET pin.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of ~1us (tRESET*) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and/or /HOLD).

Note:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated /RESET pin on the SOIC-16 & TFBGA package. If the reset function is not used, this pin can be left floating in the system.

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6.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q01JV provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Registers
- Additional Individual Block/Sector Locks for array protection
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

  * Note: This feature is available upon special flow. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q01JV will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 43). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed, a pull-up resistor on /CS pin can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

The W25Q01JV also provides another Write Protect method using the Individual Block Locks. Each 64KB block (except the top and bottom blocks, total of 2044 blocks) and each 4KB sector within the top/bottom blocks (total of 64 sectors) are equipped with an Individual Block Lock bit. When the lock bit is 0, the corresponding sector or block can be erased or programmed; when the lock bit is set to 1, Erase or Program commands issued to the corresponding sector or block will be ignored. When the device is powered on, all Individual Block Lock bits will be 1, so the entire memory array is protected from Erase/Program. An “Individual Block Unlock (39h)” instruction must be issued to unlock any specific sector or block.

The WPS bit in Status Register-3 is used to decide which Write Protect scheme should be used. When WPS=0 (factory default), the device will only utilize CMP, TB, BP[3:0] bits to protect specific areas of the array; when WPS=1, the device will utilize the Individual Block Locks for write protection.

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7. STATUS AND CONFIGURATION REGISTERS

Three Status Registers Status/Configuration Registers are provided for W25Q01JV. The Read Status Register-1/2/3 instructions are used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up and current Address Mode. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, Hold/Reset functions, output driver strength and power-up Address Mode. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

The write to registers (without input address) instructions will write simultaneously to both the die registers as long as both die are not busy. Each die through Read Status Register instructions will provide its own status for BUSY and SUS status only. The two die stack operation of Read/Write Status and Configuration Registers are detailed on Two Die Stack Operations section.

7.1 Status Registers

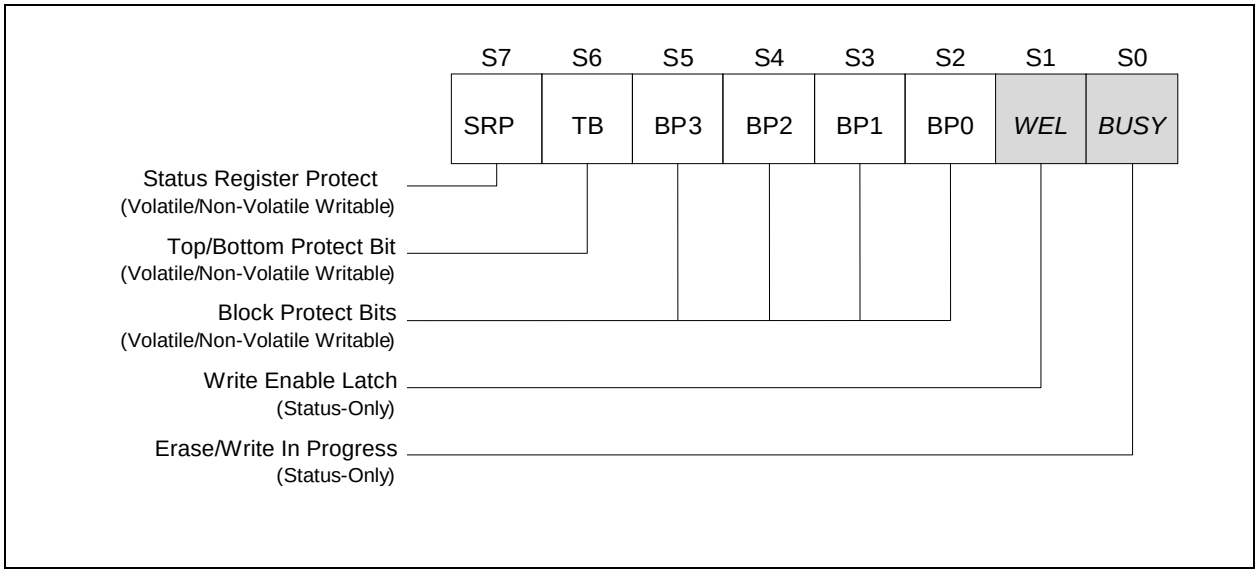


Figure 4a. Status Register-1

7.1.1 Program/Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions. Read Status Register instruction can always be used to poll the BUSY status during internal operations to determine if the operation has finished.

The two die stack operation of BUSY bit is detailed on Two Die Stack Operations section, please refer to Application Note: AN0000035.

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7.1.2 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

The two die stack operation of WEL bit is detailed on Two Die Stack Operations Application; please refer to Application Note: AN0000035.

7.1.3 Block Protect Bits (BP3, BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP3, BP2, BP1, BP0) are non-volatile read/write bits in the status register (S5, S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tw in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.1.4 Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP3, BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP, SRL and WEL bits.

7.1.5 Complement Protect (CMP) – *Volatile/Non-Volatile Writable*

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with TB, BP3, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by TB, BP3, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

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7.1.6 Status Register Protect (SRP, SRL) – *Volatile/Non-Volatile Writable*

The Status Register Protect bits (SRP) is non-volatile read/write bits in the status register (S7). The SRP bit controls the method of write protection: software protection or hardware protection. The Status Register Lock bits (SRL) is non-volatile/volatile read/write bits in the status register (S8). The SRL bit controls the method of write protection: temporary lock-down or permanently one time program.

SRL	SRP	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	X	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	X	X	One Time Program(2)	Status Register is permanently protected and cannot be written to. (**enabled by adding prefix command AAh, 55h)**

1. When SRL =1, a power-down, power-up cycle will change SRL =0 state.
2. Please contact Winbond for details regarding the special instruction sequence.

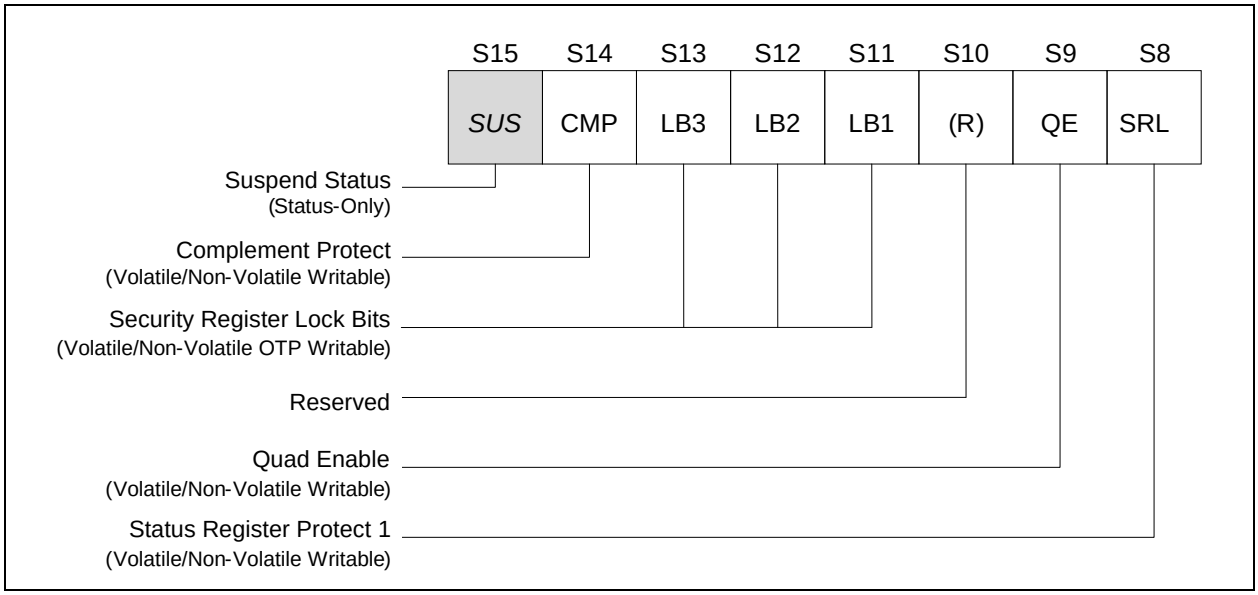


Figure 4b. Status Register-2

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7.1.7 Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

The two die stack operation of WEL bit is detailed on Two Die Stack Operations Application Note: AN0000035..

7.1.8 Security Register Lock Bits (LB3, LB2, LB1) –*Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1,SFDP Lock Bit) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11,S10) that provide the write protect control and status to the Security Registers. The default state of LB[3:1] is 0, Security Registers are unlocked. LB[3:1] can be set to 1 individually using the Write Status Register instruction. LB[3:1] are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

7.1.9 Quad Enable (QE) – *Volatile/Non-Volatile Writable*

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that enables Quad SPI operation. When the QE bit is set to a 0 state (factory default), the /WP pin and /HOLD are enabled, the device operates in Standard/Dual SPI modes. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled, the device operates in Standard/Dual/Quad SPI modes.

QE bit is required to be set to a 1 before issuing an "Enter QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A "Write Status Register" command in QPI mode cannot change QE bit from a "1" to a "0".

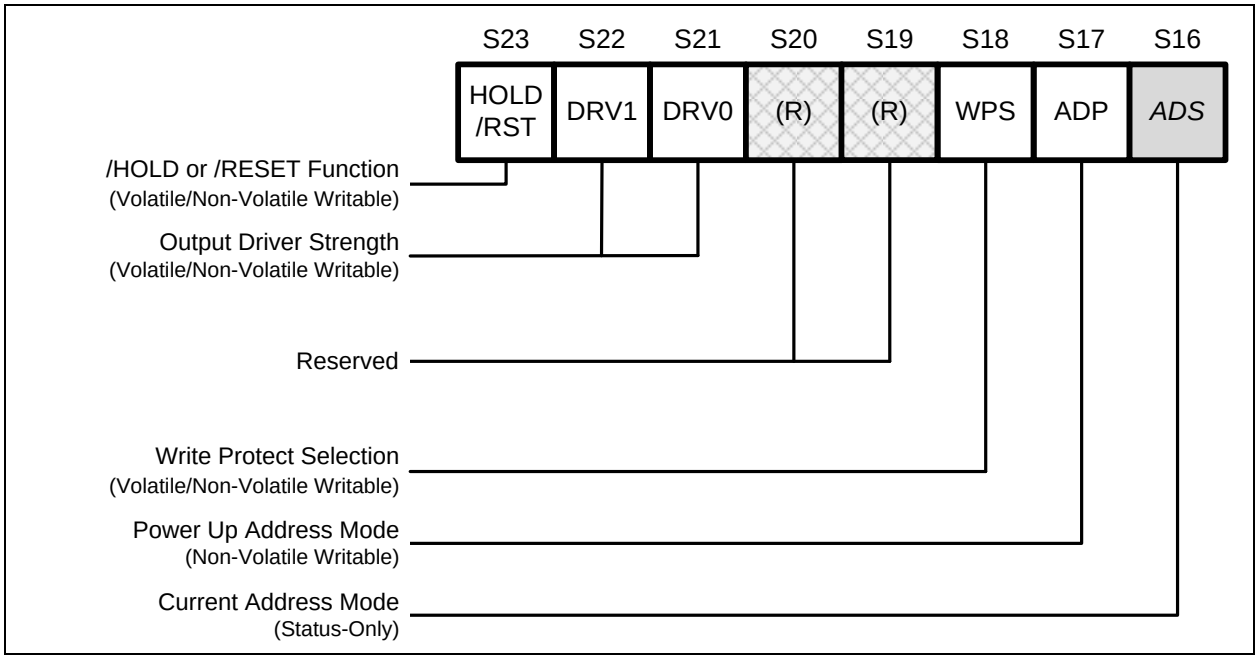


Figure 4c. Status Register-3

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7.1.10 Current Address Mode (ADS) – *Status Only*

The Current Address Mode bit is a read only bit in the Status Register-3 that indicates which address mode the device is currently operating in. When ADS=0, the device is in the 3-Byte Address Mode, when ADS=1, the device is in the 4-Byte Address Mode.

7.1.11 Power-Up Address Mode (ADP) – *Non-Volatile Writable*

The ADP bit is a non-volatile bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period, and it is only writable by the non-volatile Write Status sequence (06h + 11h). When ADP=0 (factory default), the device will power up into 3-Byte Address Mode. When ADP=1, the device will power up into 4-Byte Address Mode directly.

7.1.12 Write Protect Selection (WPS) – *Volatile/Non-Volatile Writable*

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, TB, BP[3:0] bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

7.1.13 Output Driver Strength (DRV1, DRV0) – *Volatile/Non-Volatile Writable*

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Driver Strength
0, 0	100%
0, 1	75%
1, 0	50%(default setting)
1, 1	25%

7.1.14 /HOLD or /RESET Pin Function (HOLD/RST) – *Volatile/Non-Volatile Writable*

The HOLD/RST bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

7.1.15 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

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7.1.16 W25Q01JV Status Register Memory Protection (WPS = 0, CMP = 0)

STATUS REGISTER					W25Q01JV (1G-BIT / 128M-BYTE) MEMORY PROTECTION(1)			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
0	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	2047	07FF0000h - 07FFFFFFh	64KB	Upper 1/2048
0	0	0	1	0	2046 thru 2047	07FE0000h - 07FFFFFFh	128KB	Upper 1/1024
0	0	0	1	1	2044 thru 2047	07FC0000h - 07FFFFFFh	256KB	Upper 1/512
0	0	1	0	0	2040 thru 2047	07F80000h - 07FFFFFFh	512KB	Upper 1/256
0	0	1	0	1	2032 thru 2047	07F00000h - 07FFFFFFh	1MB	Upper 1/128
0	0	1	1	0	2016 thru 2047	07E00000h - 07FFFFFFh	2MB	Upper 1/64
0	0	1	1	1	1984 thru 2047	07C00000h - 07FFFFFFh	4MB	Upper 1/32
0	1	0	0	0	1920 thru 2047	07800000h - 07FFFFFFh	8MB	Upper 1/16
0	1	0	0	1	1792 thru 2047	07000000h - 07FFFFFFh	16MB	Upper 1/8
0	1	0	1	0	1536 thru 2047	06000000h - 07FFFFFFh	32MB	Upper 1/4
0	1	0	1	1	1024 thru 2047	04000000h - 07FFFFFFh	64MB	Upper 1/2
0	1	1	0	0	0 thru 2047	00000000h - 07FFFFFFh	128MB	ALL
0	1	1	0	1	0 thru 2047	00000000h - 07FFFFFFh	128MB	ALL
0	1	1	1	0	0 thru 2047	00000000h - 07FFFFFFh	128MB	ALL
0	1	1	1	1	0 thru 2047	00000000h - 07FFFFFFh	128MB	ALL
1	0	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	0	00000000h - 0000FFFFh	64KB	Lower 1/2048
1	0	0	1	0	0 thru 1	00000000h - 0001FFFFh	128KB	Lower 1/1024
1	0	0	1	1	0 thru 3	00000000h - 0003FFFFh	256KB	Lower 1/512
1	0	1	0	0	0 thru 7	00000000h - 0007FFFFh	512KB	Lower 1/256
1	0	1	0	1	0 thru 15	00000000h - 000FFFFFh	1MB	Lower 1/128
1	0	1	1	0	0 thru 31	00000000h - 001FFFFFh	2MB	Lower 1/64
1	0	1	1	1	0 thru 63	00000000h - 003FFFFFh	4MB	Lower 1/32
1	1	0	0	0	0 thru 127	00000000h - 007FFFFFh	8MB	Lower 1/16
1	1	0	0	1	0 thru 255	00000000h - 00FFFFFFh	16MB	Lower 1/8
1	1	0	1	0	0 thru 511	00000000h - 01FFFFFFh	32MB	Lower 1/4
1	1	0	1	1	0 thru 1023	00000000h - 03FFFFFFh	64MB	Lower 1/2
1	1	1	0	0	0 thru 2047	00000000h - 07FFFFFFh	128MB	ALL
1	1	1	0	1	0 thru 2047	00000000h - 07FFFFFFh	128MB	ALL
1	1	1	1	0	0 thru 2047	00000000h - 07FFFFFFh	128MB	ALL
1	1	1	1	1	0 thru 2047	00000000h - 07FFFFFFh	128MB	ALL

Notes:

1. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

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7.1.17 W25Q01JV Status Register Memory Protection (WPS = 0, CMP = 1)

STATUS REGISTER					W25Q01JV (1G-BIT / 128M-BYTE) MEMORY PROTECTION(1)			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
0	0	0	0	0	ALL	00000000h - 07FFFFFFh	ALL	ALL
0	0	0	0	1	0 thru 2046	00000000h - 07FEFFFFh	131,008KB	Lower 2047/2048
0	0	0	1	0	0 thru 2045	00000000h - 07FDFFFFh	130,944KB	Lower 1023/1024
0	0	0	1	1	0 thru 2043	00000000h - 07FBFFFFh	130,816KB	Lower 511/512
0	0	1	0	0	0 thru 2039	00000000h - 07F7FFFFh	130,560KB	Lower 255/256
0	0	1	0	1	0 thru 2031	00000000h - 07EFFFFFh	127MB	Lower 127/128
0	0	1	1	0	0 thru 2015	00000000h - 07DFFFFFh	126MB	Lower 63/64
0	0	1	1	1	0 thru 1983	00000000h - 07BFFFFFh	124MB	Lower 31/32
0	1	0	0	0	0 thru 1919	00000000h - 077FFFFFh	120MB	Lower 15/16
0	1	0	0	1	0 thru 1791	00000000h - 06FFFFFFh	112MB	Lower 7/8
0	1	0	1	0	0 thru 1535	00000000h - 05FFFFFFh	96MB	Lower 3/4
0	1	0	1	1	0 thru 1023	00000000h - 03FFFFFFh	64MB	Lower 1/2
0	1	1	0	0	NONE	NONE	NONE	NONE
0	1	1	0	1	NONE	NONE	NONE	NONE
0	1	1	1	0	NONE	NONE	NONE	NONE
0	1	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	0	ALL	00000000h - 07FFFFFFh	ALL	ALL
1	0	0	0	1	1 thru 2047	00010000h - 07FFFFFFh	131,008KB	Upper 2047/2048
1	0	0	1	0	2 thru 2047	00020000h - 07FFFFFFh	130,944KB	Upper 1023/1024
1	0	0	1	1	4 thru 2047	00040000h - 07FFFFFFh	130,816KB	Upper 511/512
1	0	1	0	0	8 thru 2047	00080000h - 07FFFFFFh	130,560KB	Upper 255/256
1	0	1	0	1	16 thru 2047	00100000h - 07FFFFFFh	127MB	Upper 127/128
1	0	1	1	0	32 thru 2047	00200000h - 07FFFFFFh	126MB	Upper 63/64
1	0	1	1	1	64 thru 2047	00400000h - 07FFFFFFh	124MB	Upper 31/32
1	1	0	0	0	128 thru 2047	00800000h - 07FFFFFFh	120MB	Upper 15/16
1	1	0	0	1	256 thru 2047	01000000h - 07FFFFFFh	112MB	Upper 7/8
1	1	0	1	0	512 thru 2047	02000000h - 07FFFFFFh	96MB	Upper 3/4
1	1	0	1	1	1024 thru 2047	04000000h - 07FFFFFFh	64MB	Upper 1/2
1	1	1	0	0	NONE	NONE	NONE	NONE
1	1	1	0	1	NONE	NONE	NONE	NONE
1	1	1	1	0	NONE	NONE	NONE	NONE
1	1	1	1	1	NONE	NONE	NONE	NONE

Notes:

1. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

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7.1.18 W25Q01JV Individual Block Memory Protection (WPS=1)

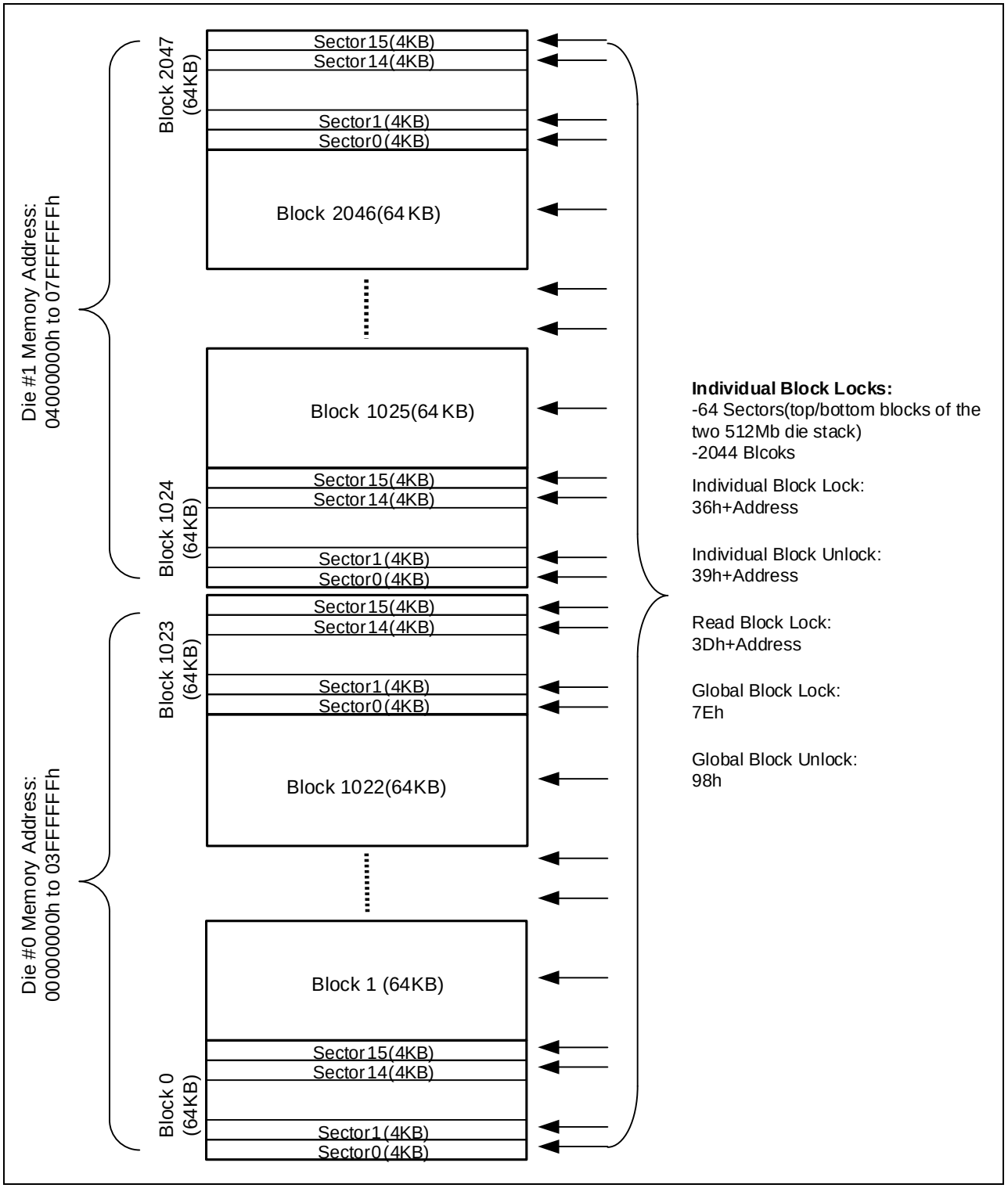


Figure 4d. Individual Block/Sector Locks

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Notes:
1. Individual Block/Sector protection is only valid when WPS=1.
2. All individual block/sector lock bits are set to 1 by default after power up, all memory array is protected.

8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25Q01JV consists of 64 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1-4). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI instruction set of the W25Q01JV consists of 42 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table 5-7). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked through IO[3:0] pins provides the instruction code. Data on all four IO pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI instructions, addresses, data and dummy bytes are using all four IO pins to transfer every byte of data with every two serial clocks (CLK).

For SPI/QPI DTR Read instructions, the address input is sampled on both rising and falling edges of the clock; the data output is also ready on both edges of the clock.

SPI/QPI Protocol	3-Byte Address Mode (ADS=0)	4-Byte Address Mode (ADS=1)
Standard/Dual/Quad SPI	Instruction Set Table 1, 2 & 7	Instruction Set Table 3, 4 & 8
QPI	Instruction Set Table 5 & 9	Instruction Set Table 6 & 10

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 5 through 57. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.1 Device ID and Instruction Set Tables

8.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7 - ID0)**	**(ID15 - ID0)**
Instruction	**ABh, 90h, 92h, 94h**	**9Fh**
W25Q01JV-IM	20h	7021h

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8.2 SPI Instructions

8.2.1 Following Upper/Lower Die Instruction (Flows Previous Instruction Located)(1,15)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Read Status Register-1	**05h**	(S7-S0)(2)					
Read Status Register-2	**35h**	(S15-S8)(2)					
Read Status Register-3	**15h**	(S23-S16)(2)					
Read SFDP Register	**5Ah**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase / Program Suspend	**75h(15)**						
Erase / Program Resume	**7Ah(15)**						

8.2.2 Con-Current Instruction (Both Die Accept, W/O Address) (1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Read Unique ID	**4Bh**	Dummy	Dummy	Dummy	Dummy	Dummy	(UID63-0)
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Chip Erase	**C7h/60h**						
Write Status Register-1(4)	**01h**	(S7-S0)(4)					
Write Status Register-2	**31h**	(S15-S8)					
Write Status Register-3	**11h**	(S23-S16)					
Global Block Lock	**7Eh(15)**						
Global Block Unlock	**98h(15)**						
Power-down	**B9h**						
Enter 4-Byte Address Mode	**B7h**						
Exit 4-Byte Address Mode	**E9h**						
Enable Reset	**66h**						
Reset Device	**99h**						
Software Die Select	**C2h(15)**	Die ID#					

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8.2.3 Linear Address Instruction: (Read/Write/Erase; 3byte Address Mode) (1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)		
Read Data with 4-Byte Address	**13h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Fast Read with 4-Byte Address	**0Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Page Program with 4-Byte Address	**12h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		2	
Sector Erase (4KB) with 4-Byte Address	**21h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB) with 4-Byte Address	**DCh**	A31-A24	A23-A16	A15-A8	A7-A0		
Erase Security Register	**44h**(5)	A23-A16	A15-A8	A7-A0			
Program Security Register	**42h**(5)	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Read Security Register	**48h**(5)	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Read Block Lock	**3Dh**	A23-A16	A15-A8	A7-A0	(L7-L0)		
Individual Block Lock	**36h**	A23-A16	A15-A8	A7-A0			
Individual Block Unlock	**39h**	A23-A16	A15-A8	A7-A0			

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
Number of Clock(1-1-2)	**8**	**8**	**8**	**8**	**8**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(7)	…	…		
Fast Read Dual Output with 4-Byte Address	**3Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(7)	…	
Number of Clock(1-2-2)	**8**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Mftr./Device ID Dual I/O	**92h**	A23-A16	A15-A8	00	Dummy(11)	(MF7-MF0)	(ID7-ID0)			
Fast Read Dual I/O	**BBh**	A23-A16	A15-A8	A7-A0	Dummy(11)	(D7-D0)	…			
Fast Read Dual I/O with 4-Byte Address	**BCh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(11)	(D7-D0)	…		
Number of Clock(1-1-4)	**8**	**8**	**8**	**8**	**2**	**2**	**2**	**2**	**2**	**2**
Quad Input Page Program	**32h**	A23-A16	A15-A8	A7-A0	(D7-D0)(9)	(D7-D0)(3)	…			
Quad Page Program with 4-Byte Address	**34h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	…	…		
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)(9)	…
Fast Read Quad Output with 4-Byte Address	**6Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)(9)
Number of Clock(1-4-4)	**8**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Mftr./Device ID Quad I/O	**94h**	A23-A16	A15-A8	00	Dummy(11)	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)	
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	Dummy(11)	Dummy	Dummy	(D7-D0)	…	
Fast Read Quad I/O with 4-Byte Address	**ECh**	A31-A24	A23-A16	A15-A8	A7-A0f	Dummy(11)	Dummy	Dummy	(D7-D0)	…

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8.2.4 Linear address Instruction: (read/write/erase; 4byte Address Mode)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Read Data	**03h**	**A31-A24**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Read Data with 4-Byte Address	**13h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Fast Read with 4-Byte Address	**0Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Page Program	**02h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Page Program with 4-Byte Address	**12h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Sector Erase (4KB)	**20h**	A31-A24	A23-A16	A15-A8	A7-A0		
Sector Erase (4KB) with 4-Byte Address	**21h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB) with 4-Byte Address	**DCh**	A31-A24	A23-A16	A15-A8	A7-A0		
Erase Security Register(5)	**44h**	A31-A24	A23-A16	A15-A8	A7-A0		
Program Security Register(5)	**42h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Read Security Register(5)	**48h**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Read Block Lock	**3Dh**	A31-A24	A23-A16	A15-A8	A7-A0	(L7-L0)	
Individual Block Lock	**36h**	A31-A24	A23-A16	A15-A8	A7-A0		
Individual Block Unlock	**39h**	A31-A24	A23-A16	A15-A8	A7-A0		

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte9
Number of Clock(1-1-2)	**8**	**8**	**8**	**8**	**8**	**8**	**4**	**4**	
Fast Read Dual Output	**3Bh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0,…)(7)		
Fast Read Dual Output with 4-Byte Address	**3Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0,…)(7)		
Number of Clock(1-2-2)	**8**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	
Mfr./Device ID Dual I/O	**92h**	A31-A24	A23-A16	A15-A8	00	Dummy(11)	(MF7-MF0)	(ID7-ID0)	
Fast Read Dual I/O	**BBh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(11)	(D7-D0)		
Fast Read Dual I/O with 4-Byte Address	**BCh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(11)	(D7-D0)		
Number of Clock(1-1-4)	**8**	**8**	**8**	**8**	**8**	**4**	**4**	**4**	
Quad Input Page Program	**32h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)(9)	(D7-D0)(3)..		
Quad Page Program with 4-Byte Address	**34h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)(9)	…		
Fast Read Quad Output	**6Bh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(9)	
Fast Read Quad Output with 4-Byte Address	**6Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(9)	
Number of Clock(1-4-4)	**8**	**2**	**2**	**2**	**2**	**2**	**4**	**2**	**2**
Mfr./Device ID Quad I/O	**94h**	A31-A24	A23-A16	A15-A8	00	Dummy(11)	Dummy	(MF7-MF0)	(ID7-ID0)
Fast Read Quad I/O	**EBh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(11)	Dummy	(D7-D0)	
Fast Read Quad I/O with 4-Byte Address	**ECh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(11)	Dummy	(D7-D0)	
Set Burst with Wrap	**77h**	Dummy	Dummy	Dummy	W7-W0				

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8.3 QPI mode instruction:

8.3.1 Following Upper/Lower Die Instruction (Flows Previous Instruction Located)(15)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
NUMBER OF CLOCK (4-4-4)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Read Status Register-1	**05h**	(S7-S0)(2)					
Read Status Register-2	**35h**	(S15-S8)(2)					
Read Status Register-3	**15h**	(S23-S16)(2)					

8.3.2 Con-Current Instruction (Both Die Accept, W/O Address) (1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (4-4-4)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Set Read Parameters	**C0h**	P7-P0					
Chip Erase	**C7h/60h**						
Write Status Register-1(4)	**01h**	(S7-S0)(4)					
Write Status Register-2	**31h**	(S15-S8)					
Write Status Register-3	**11h**	(S23-S16)					
Global Block Lock	**7Eh**						
Global Block Unlock	**98h**						
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Enter 4-Byte Address Mode	**B7h**						
Exit 4-Byte Address Mode	**E9h**						
Enable Reset	**66h**						
Reset Device	**99h**						
Exit QPI Mode	**FFh**						
Software Die Select	**C2h(15)**						

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8.3.3 Linear Address Instruction: (Read/Write/Erase; 3/4byte Address)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (4-4-4)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy(12)	(D7-D0)	
Burst Read with Wrap(16)	**0Ch**	A23-A16	A15-A8	A7-A0	Dummy(13)	(D7-D0)	
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0(14)	(D7-D0)	
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0(9)	D7-D0(3)	
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0			
Read Block Lock	**3Dh**	A23-A16	A15-A8	A7-A0	(L7-L0)		
Individual Block Lock	**36h**	A23-A16	A15-A8	A7-A0			
Individual Block Unlock	**39h**	A23-A16	A15-A8	A7-A0			

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (4-4-4)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Fast Read	**0Bh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(12)	(D7-D0)
Burst Read with Wrap(16)	**0Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(13)	(D7-D0)
Fast Read Quad I/O	**EBh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(14)	(D7-D0)
Page Program	**02h**	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0(9)	D7-D0(3)
Sector Erase (4KB)	**20h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A31-A24	A23-A16	A15-A8	A7-A0		
Read Block Lock	**3Dh**	A31-A24	A23-A16	A15-A8	A7-A0	(L7-L0)	
Individual Block Lock	**36h**	A31-A24	A23-A16	A15-A8	A7-A0		
Individual Block Unlock	**39h**	A31-A24	A23-A16	A15-A8	A7-A0		

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8.4 DTR with Linear address Instruction:

8.4.1 DTR with SPI Instructions, 3-Byte Address Mode

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	8	4	4	4	6	4	4
DTR Fast Read	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Number of Clock(1-2-2)	8	2	2	2	2	4	2
DTR Fast Read Dual I/O	**BDh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)
Number of Clock(1-4-4)	8	1	1	1	1	7	1
DTR Fast Read Quad I/O	**EDh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

8.4.2 DTR with SPI Instructions, 4-Byte Address Mode

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	8	4	4	4	4	4	4
DTR Fast Read	**0Dh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Number of Clock(1-2-2)	8	4	4	2	4	2	2
DTR Fast Read Dual I/O	**BDh**	A31-A16	A15-A0	M7-M0	Dummy	(D7-D0)	….
Number of Clock(1-4-4)	8	2	2	1	7	2	1
DTR Fast Read Quad I/O	**EDh**	A31-A16	A15-A0	M7-M0	Dummy	(D7-D0)…	

8.4.3 DTR with QPI Instructions, 3-Byte Address Mode

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clo9ck (4-4-4)	2	1	1	1	8	1	1
DTR Read with Wrap(13)	**0Eh**	A23-A16	A15-A8	A7-0	Dummy	(D7-D0)	…
DTR Fast Read I/O	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Number of Clock (4-4-4)	2	1	1	1	1	7	1
DTR Fast Read I/O	**EDh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

8.4.4 DTR with QPI Instructions, 4-Byte Address Mode

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Number of Clock (4-4-4)	2	1	1	1	1	8	1	1
DTR Read with Wrap(13)	**0Eh**	A31-A24	A23-A16	A15-A8	A7-0	Dummy	(D7-D0)	
DTR Fast Read I/O	**0Dh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Number of Clock (4-4-4)	2	1	1	1	1	1	7	1
DTR Fast Read I/O	**EDh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

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Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "***D7-D0***" indicate data output from the device on either 1, 2 or 4 IO pins. . "D7-D0" indicates single I/O pin; "D7-D0 /2" indicates 2 I/O pins; "D7-D0 /4" indicates 4 I/O pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Write Status Register-1 (01h) can also be used to program Status Register-1&2, see section 8.2.5.
5. Security Register Address:
   Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address
6. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
7. Dual SPI data input/output format:
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
8. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap input format:
   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x, x
9. Quad SPI data input/output format:
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)
10. Fast Read Quad I/O data output format:
    IO0 = (x, x, x, x, D4, D0, D4, D0)
    IO1 = (x, x, x, x, D5, D1, D5, D1)
    IO2 = (x, x, x, x, D6, D2, D6, D2)
    IO3 = (x, x, x, x, D7, D3, D7, D3)
11. QPI Command, Address, Data input/output format:

CLK # 0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*
IO0 = C4,	C0,	A20,	A16,	A12,	A8,	A4,	A0,	D4,	D0,	D4,	D0
IO1 = C5,	C1,	A21,	A17,	A13,	A9,	A5,	A1,	D5,	D1,	D5,	D1
IO2 = C6,	C2,	A22,	A18,	A14,	A10,	A6,	A2,	D6,	D2,	D6,	D2
IO3 = C7,	C3,	A23,	A19,	A15,	A11,	A7,	A3,	D7,	D3,	D7,	D3

12. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.
13. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.
14. The first dummy is M7-M0 should be set to FFh/Fxh; once read command bypass mode is not used
15. The two die stack operation is detailed on Two Die Stack Operations Application, please refer please refer to Application Note: AN0000035.

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8.5 Instruction Descriptions

8.5.1 Write Enable (06h)

The Write Enable instruction (Figure 5) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

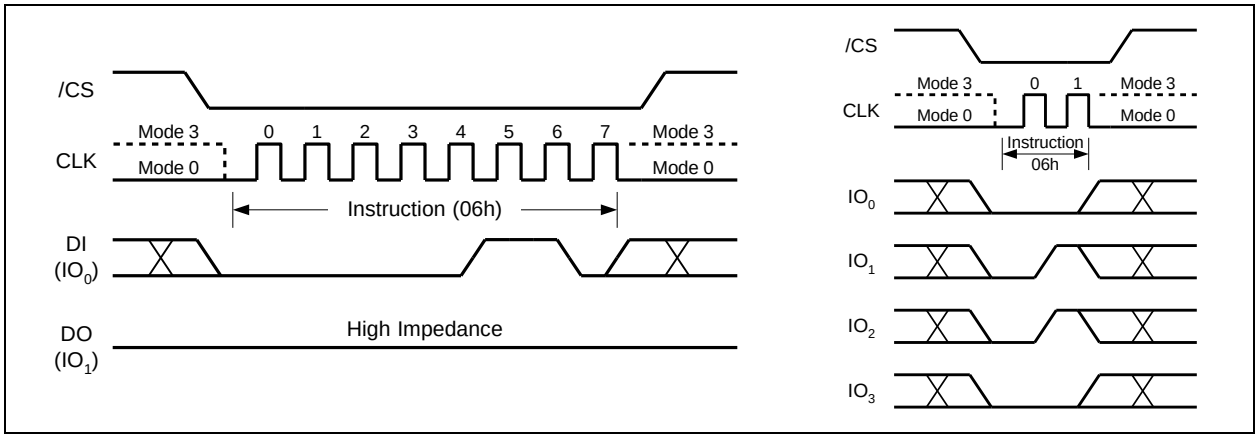


Figure 5. Write Enable Instruction for SPI Mode (left) or QPI Mode (right)

8.5.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 7.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 6) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

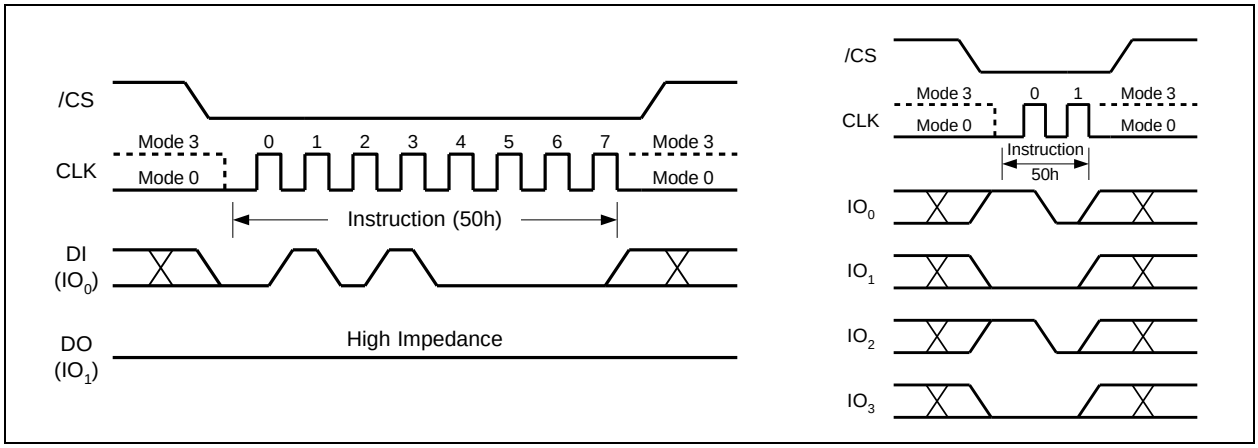


Figure 6. Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)

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8.5.3 Write Disable (04h)

The Write Disable instruction (Figure 7) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

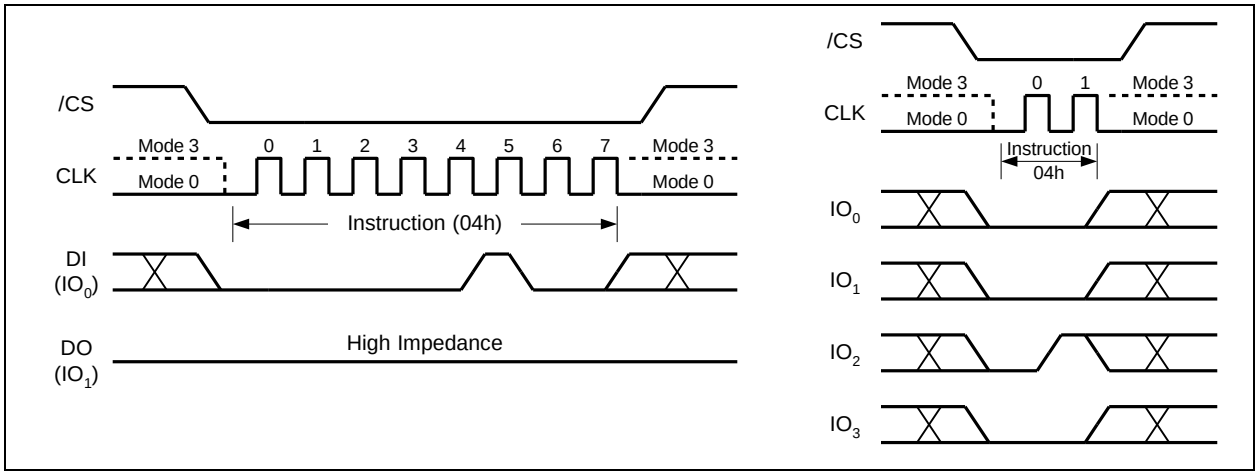


Figure 7. Write Disable Instruction for SPI Mode (left) or QPI Mode (right)

8.5.4 Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 8. Refer to section 7.1 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 8. The instruction is completed by driving /CS high.

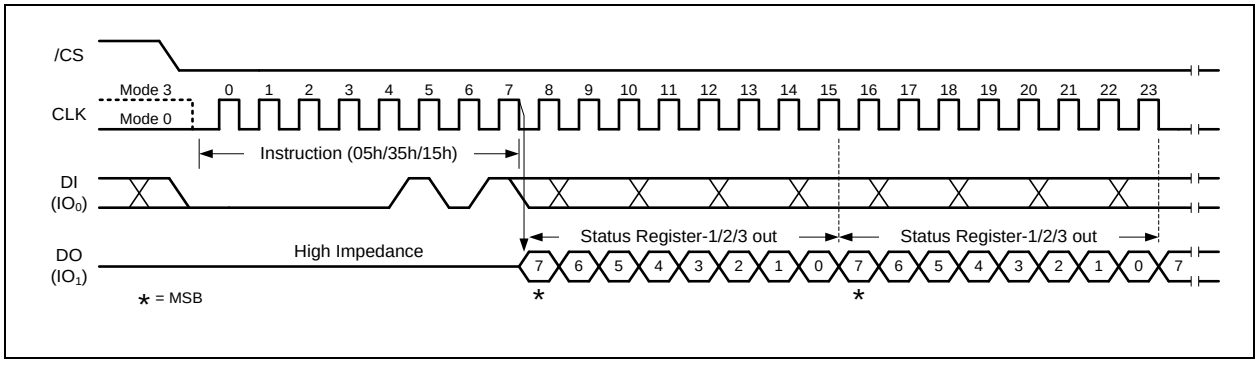


Figure 8a. Read Status Register Instruction (SPI Mode)

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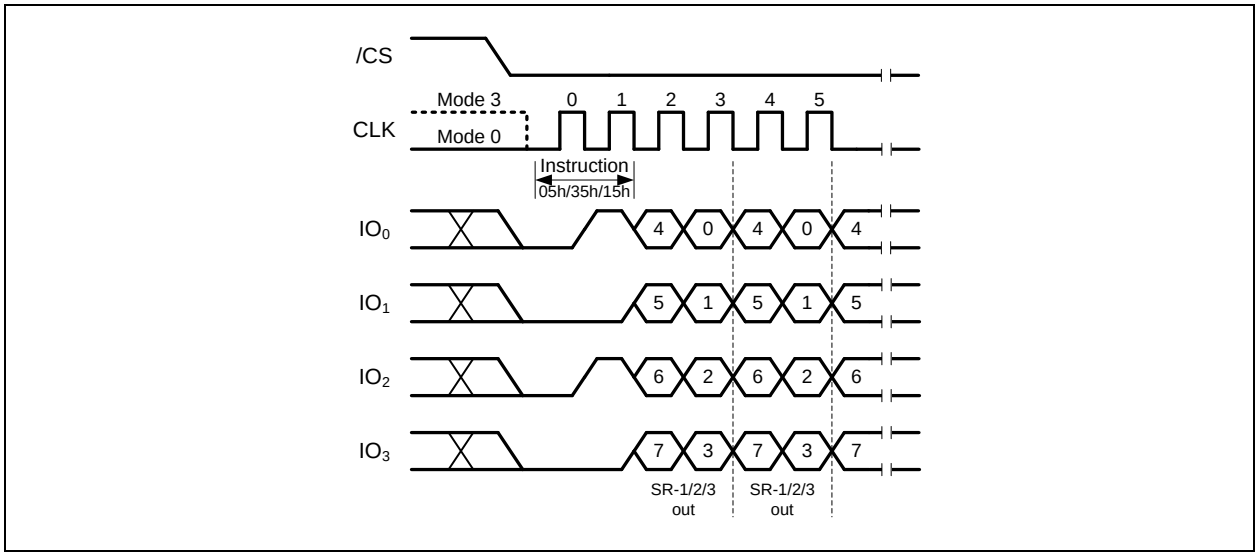


Figure 8b. Read Status Register Instruction (QPI Mode)

8.5.5 Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP, TB, BP[3:0] in Status Register-1; CMP, LB[3:1], QE, SRL in Status Register-2; HOLD/RST, DRV1, DRV0, WPS & ADP in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in Figure 9a & 9b.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRL and LB[3:1] cannot be changed from “1” to “0” because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

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The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.

Refer to section 7.1 for Status Register descriptions. Factory default for all status Register bits are 0.

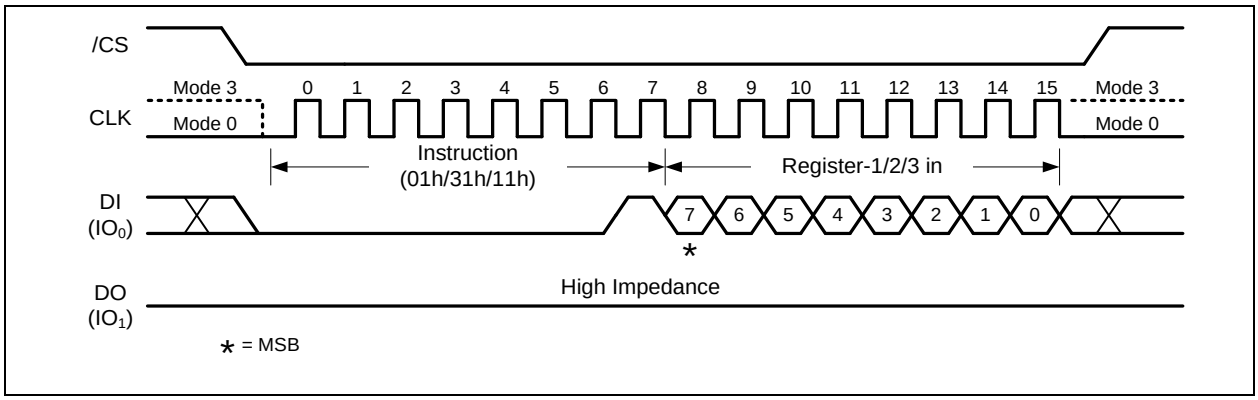


Figure 9a. Write Status Register-1/2/3 Instruction (SPI Mode)

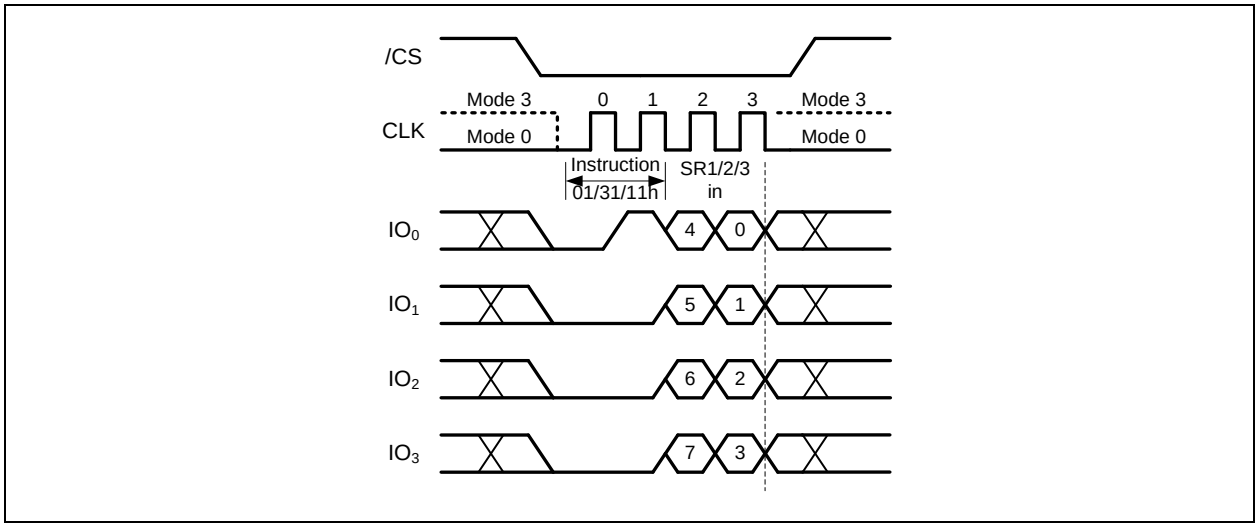


Figure 9b. Write Status Register-1/2/3 Instruction (QPI Mode)

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The W25Q01JV is also backward compatible to Winbond's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Status Register-1 (01h)" command. To complete the Write Status Register-1&2 instruction, the /CS pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 9c & 9d. If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1, the Status Register-2 will not be affected (Previous generations will clear CMP and QE bits).

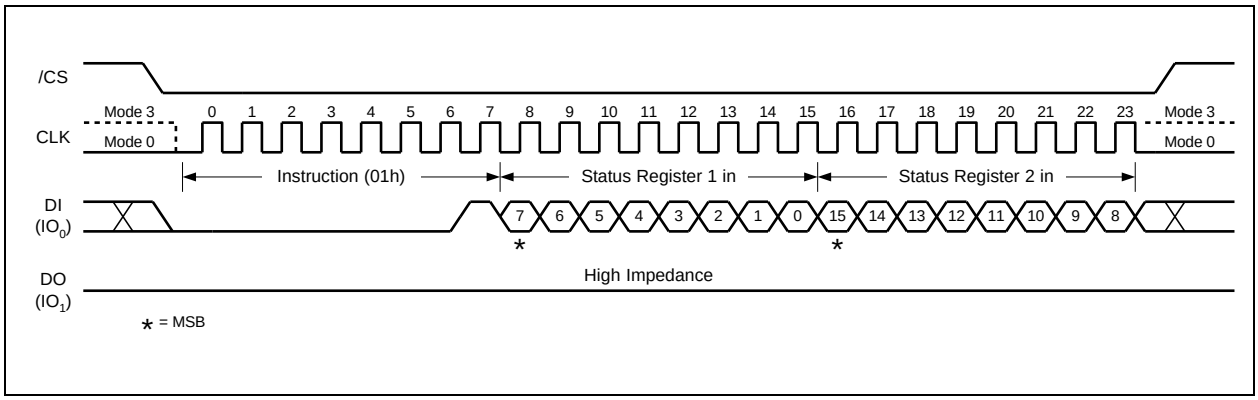


Figure 9c. Write Status Register-1/2 Instruction (SPI Mode)

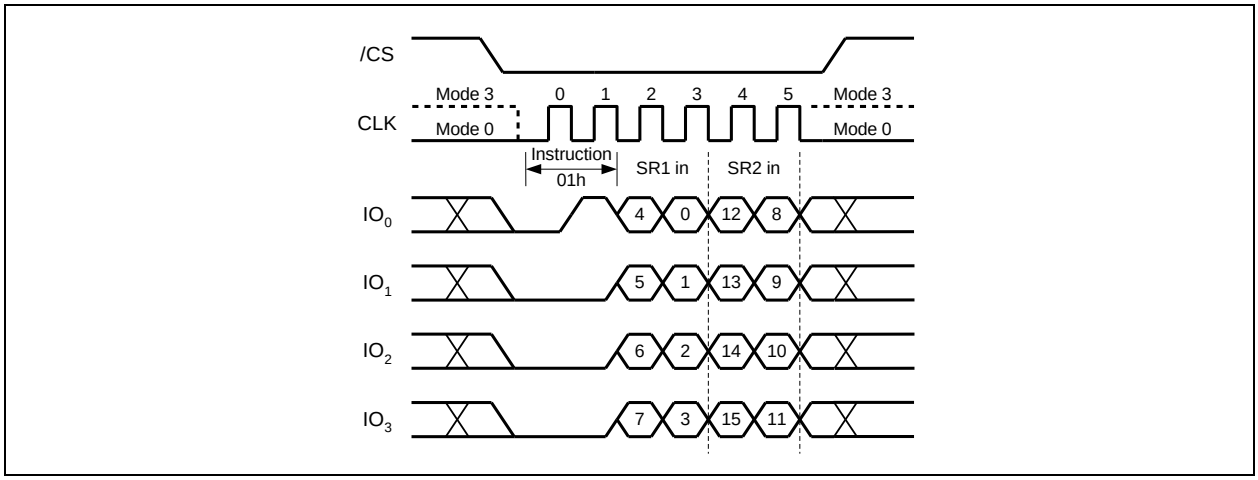


Figure 9d. Write Status Register-1/2 Instruction (QPI Mode)

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8.5.6 Enter 4-Byte Address Mode (B7h)

The Enter 4-Byte Address Mode instruction (Figure 12) will allow 32-bit address (A31-A0) to be used to access the memory array beyond 128Mb. The Enter 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code “B7h” into the DI pin and then driving /CS high.

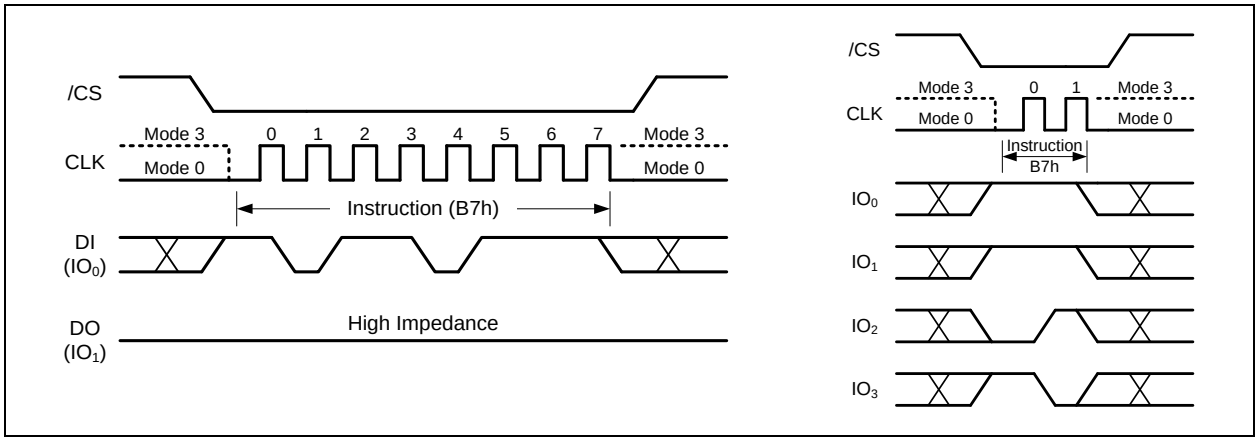


Figure 12. Enter 4-Byte Address Mode instruction for SPI Mode (left) or QPI Mode (right)

8.5.7 Exit 4-Byte Address Mode (E9h)

The Exit 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code “E9h” into the DI pin and then driving /CS high.

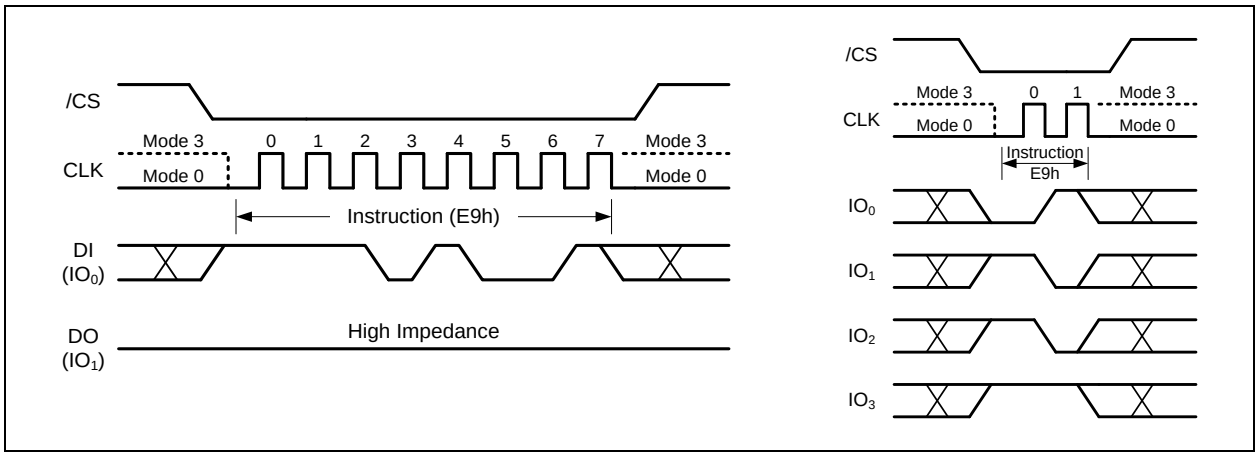


Figure 13. Exit 4-Byte Address Mode instruction for SPI Mode (left) or QPI Mode (right)

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8.5.8 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 32/24-bit address (A31/A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 14. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

The Read Data (03h) instruction is only supported in Standard SPI mode.

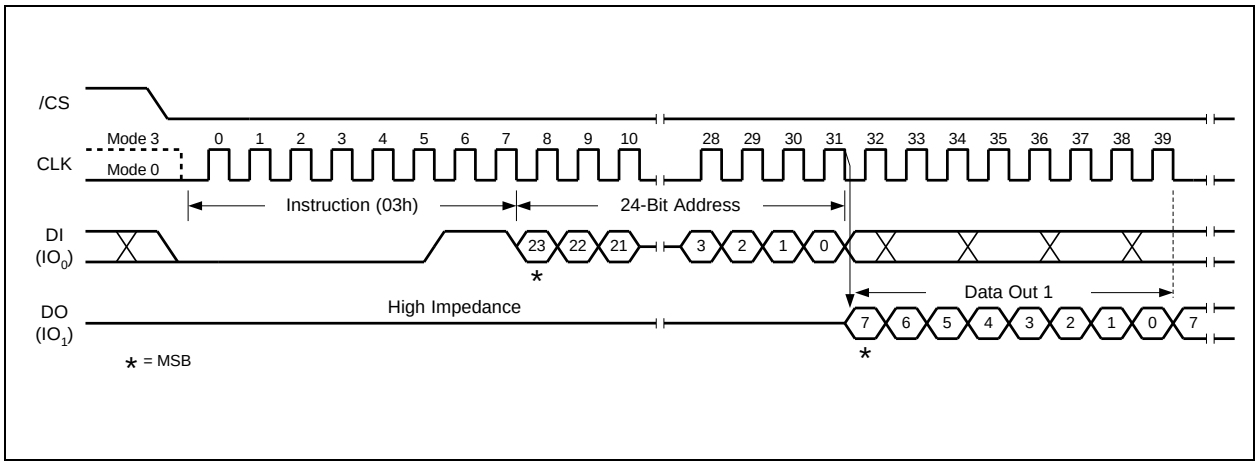


Figure 14. Read Data Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.5.9 Read Data with 4-Byte Address (13h)

The Read Data with 4-Byte Address instruction is similar to the Read Data (03h) instruction. Instead of 24-bit address, 32-bit address is needed following the instruction code 13h. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

The Read Data with 4-Byte Address instruction sequence is shown in Figure 15. If this instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data with 4-Byte Address instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

The Read Data with 4-Byte Address (13h) instruction is only supported in Standard SPI mode.

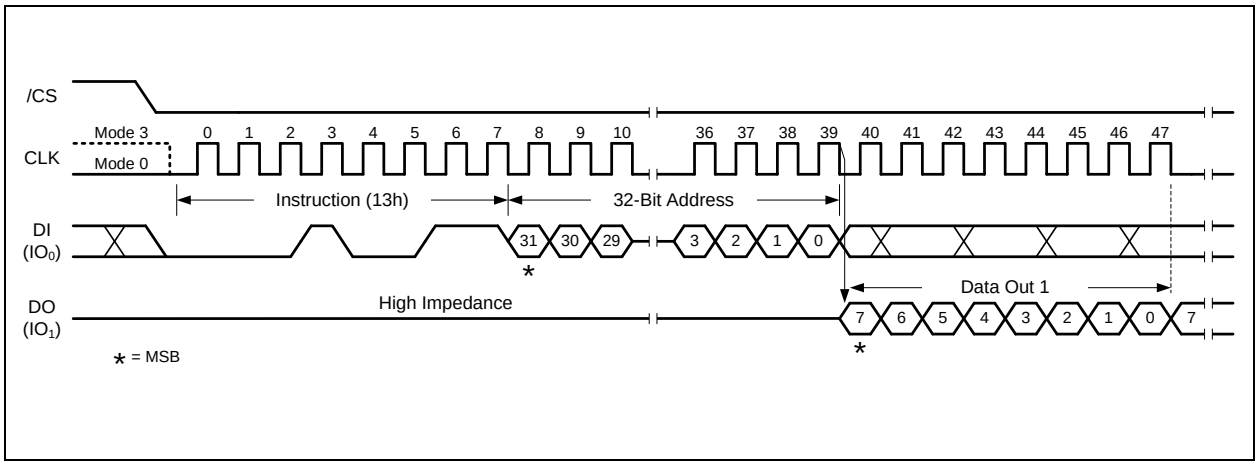


Figure 15. Read Data with 4-Byte Address Instruction (SPI Mode only)

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8.5.10 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24/32-bit address as shown in Figure 16. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a "don't care".

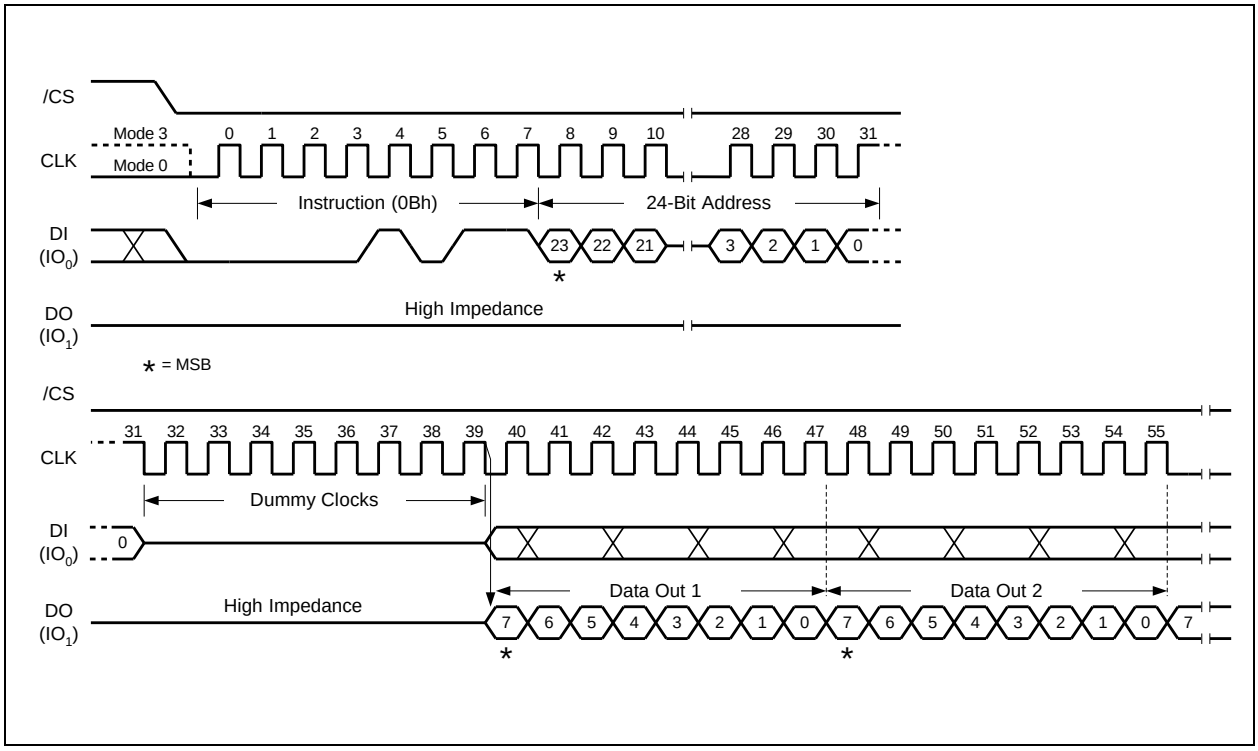


Figure 16a. Fast Read Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2.

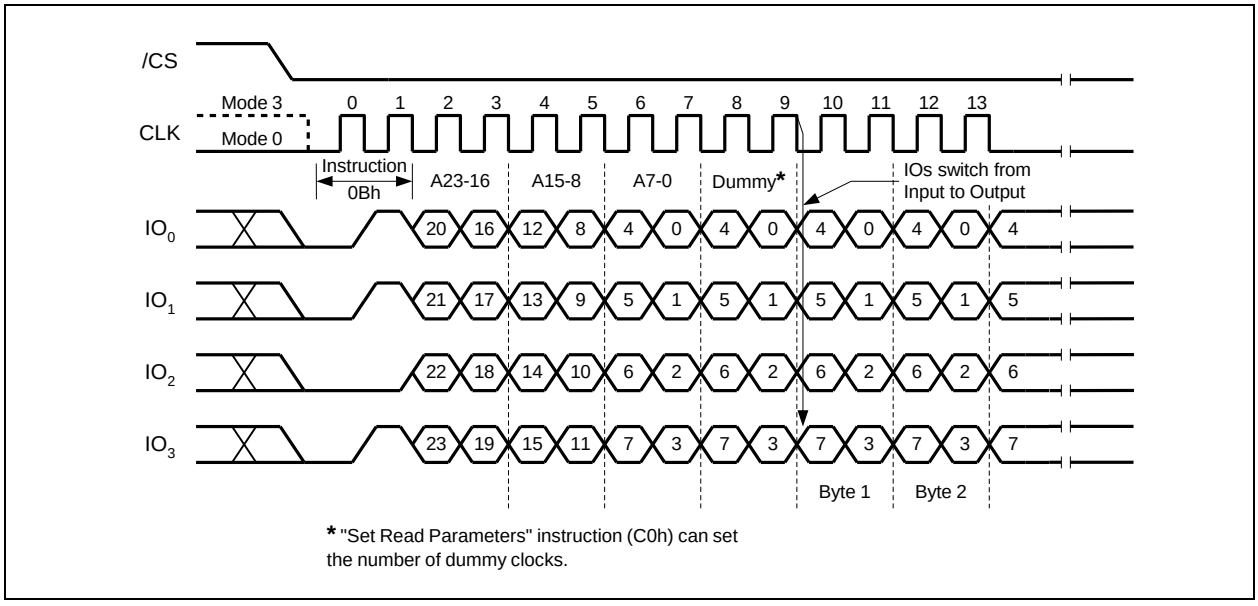


Figure 16b. Fast Read Instruction (QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.5.11 DTR Fast Read (0Dh)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24/32-bit address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding six “dummy” clocks after the 24/32-bit address as shown in Figure 17. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

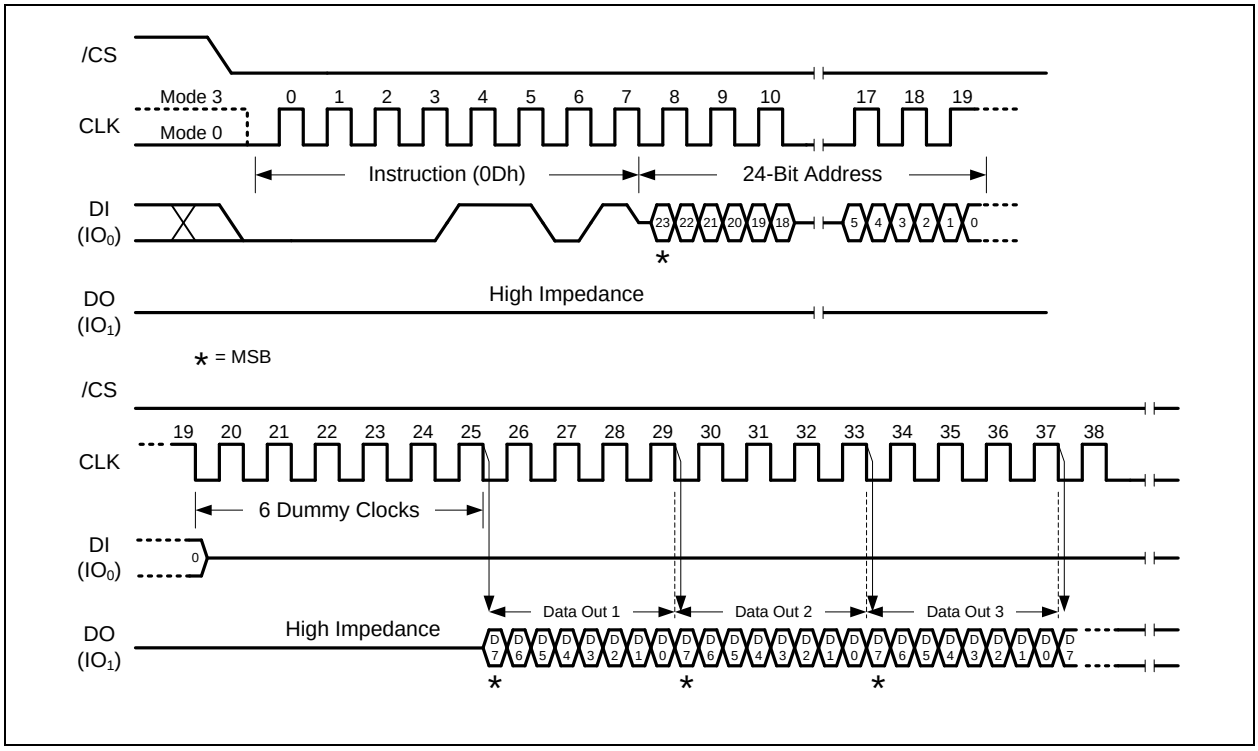


Figure 17a. DTR Fast Read Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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DTR Fast Read (0Dh) in QPI Mode

The DTR Fast Read (0Dh) instruction is also supported in QPI mode, as shown in Figure 23b. In QPI mode, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured as either 8, 10, 12, 14, or 16. The default number of dummy clocks upon power up or after a Reset instruction is 8.
“Wrap Around” feature is not available in QPI mode for DTR Fast Read (0Dh) instruction. To perform a read operation with fixed data length wrap around in QPI DTR mode, a dedicated “DTR Burst Read with Wrap (0Eh)” instruction must be used. Please refer to Section 8.2.34 for details.

The DTR Fast Read instruction is also supported in QPI mode.

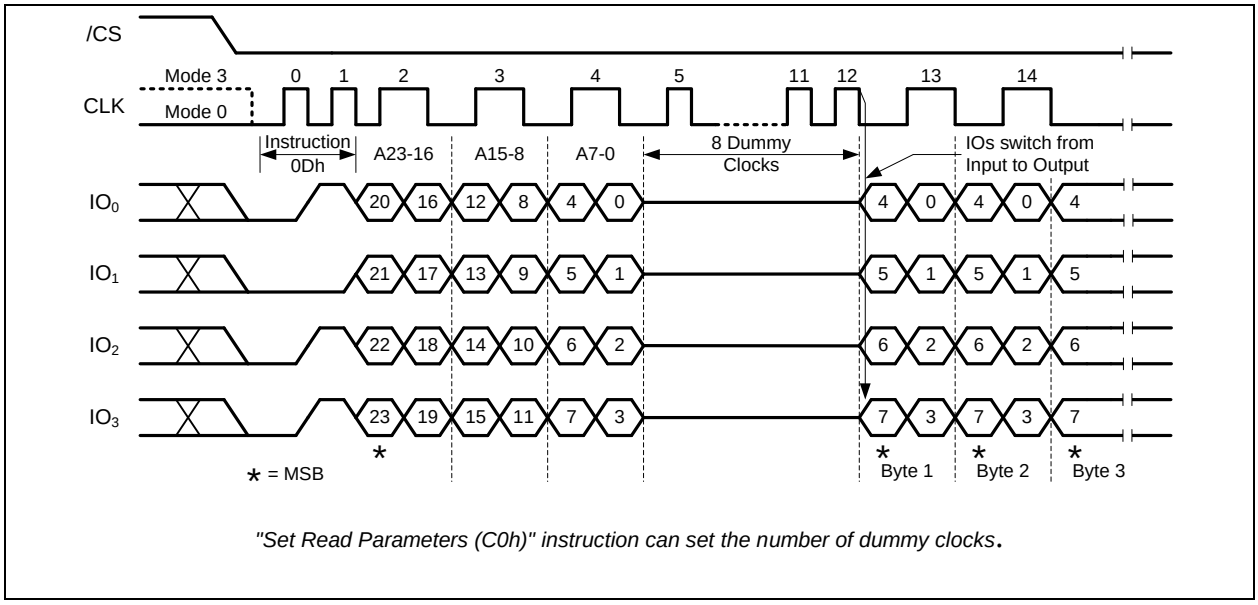


Figure 17b. DTR Fast Read Instruction (QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.5.12 Fast Read with 4-Byte Address (0Ch)

The Fast Read with 4-Byte Address instruction is similar to the Fast Read instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

The Fast Read with 4-Byte Address (0Ch) instruction is only supported in Standard SPI mode. In QPI mode, the instruction code 0Ch is used for the “Burst Read with Wrap” instruction.

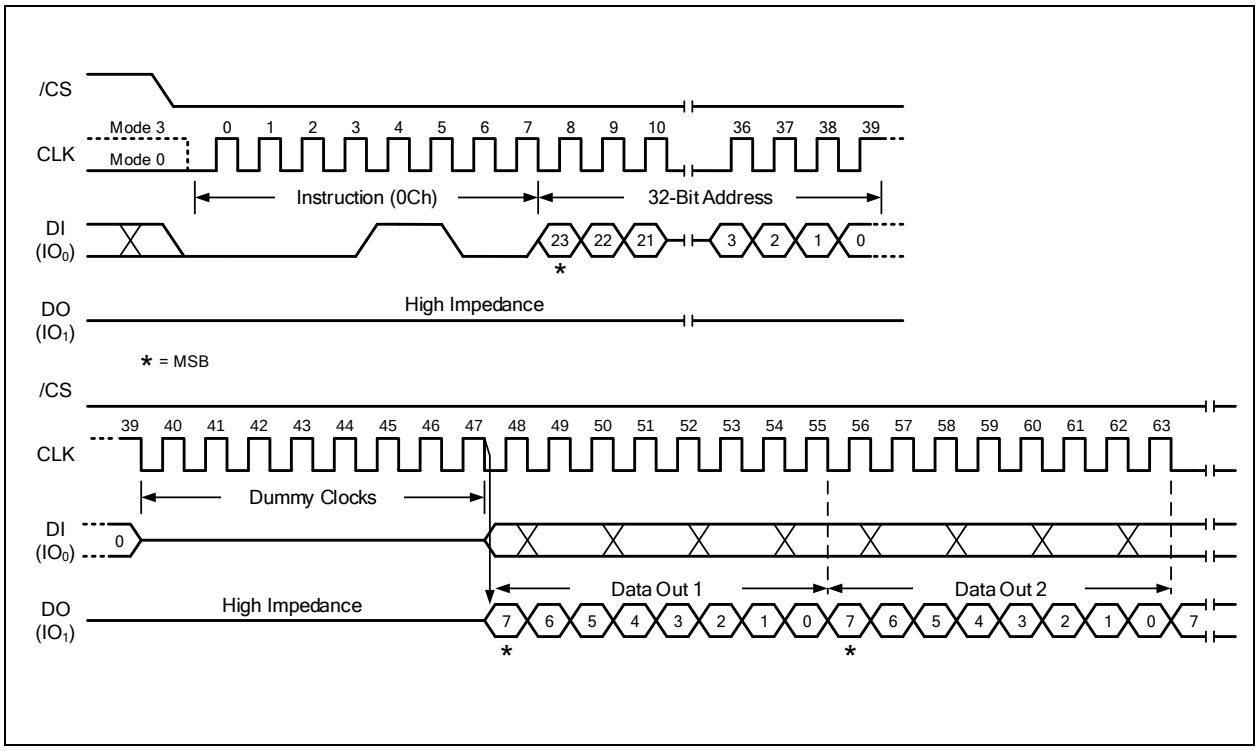


Figure 18. Fast Read with 4-Byte Address Instruction (SPI Mode only)

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8.5.13 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24/32-bit address as shown in Figure 19. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

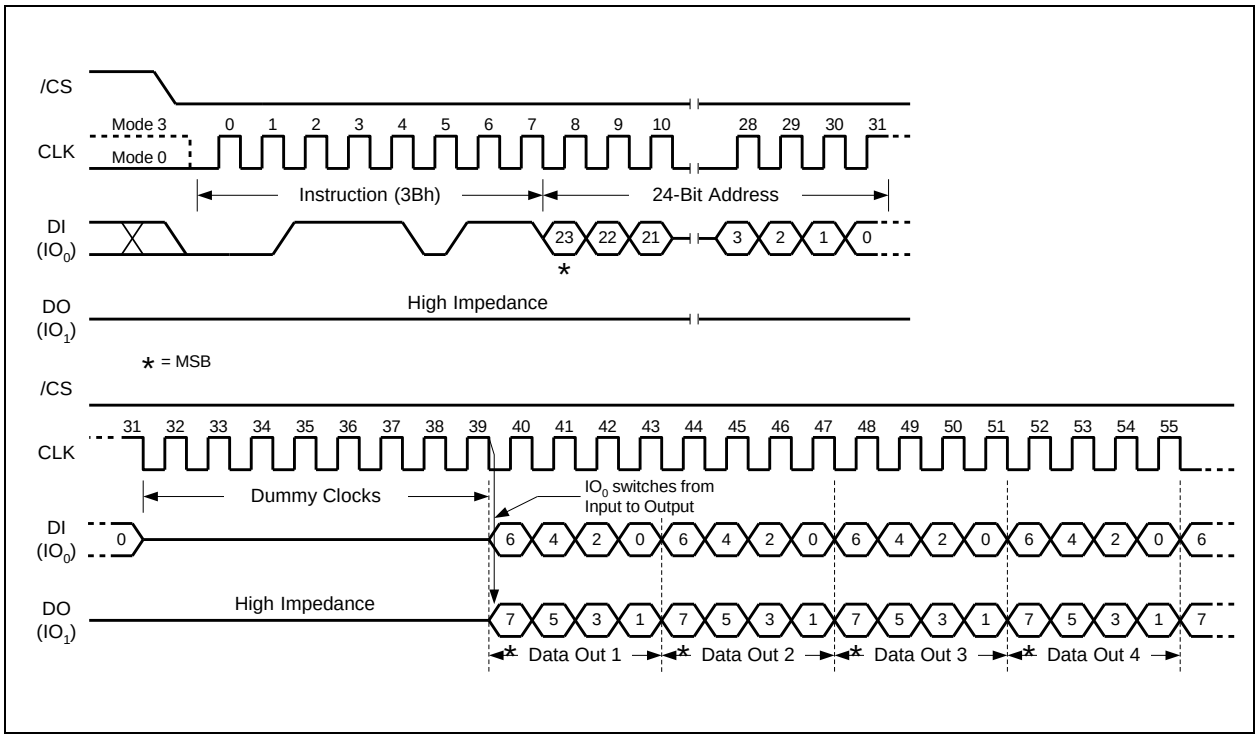


Figure 19. Fast Read Dual Output Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.5.14 Fast Read Dual Output with 4-Byte Address (3Ch)

The Fast Read Dual Output with 4-Byte Address instruction is similar to the Fast Read Dual Output instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Dual Output with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

The Fast Read Dual Output with 4-Byte Address (3Ch) instruction is only supported in Standard SPI mode.

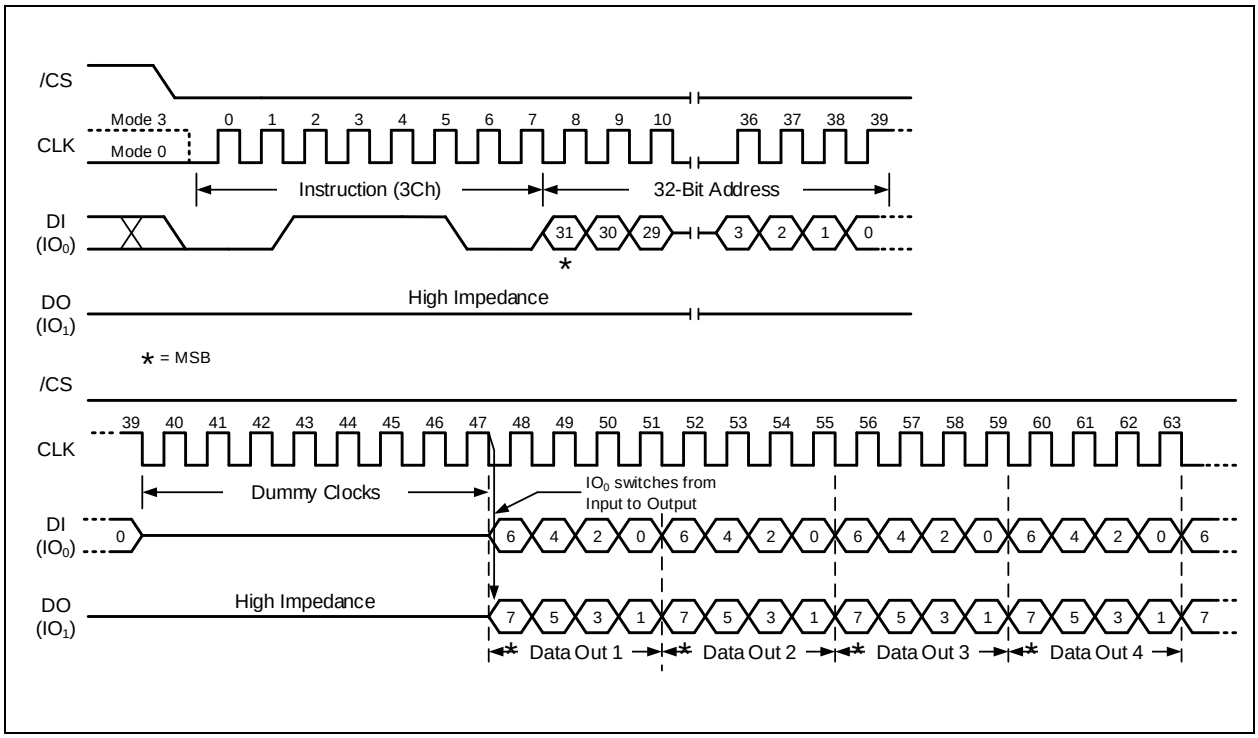


Figure 20. Fast Read Dual Output with 4-Byte Address Instruction (SPI Mode only)

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8.5.15 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24/32-bit address as shown in Figure 21. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

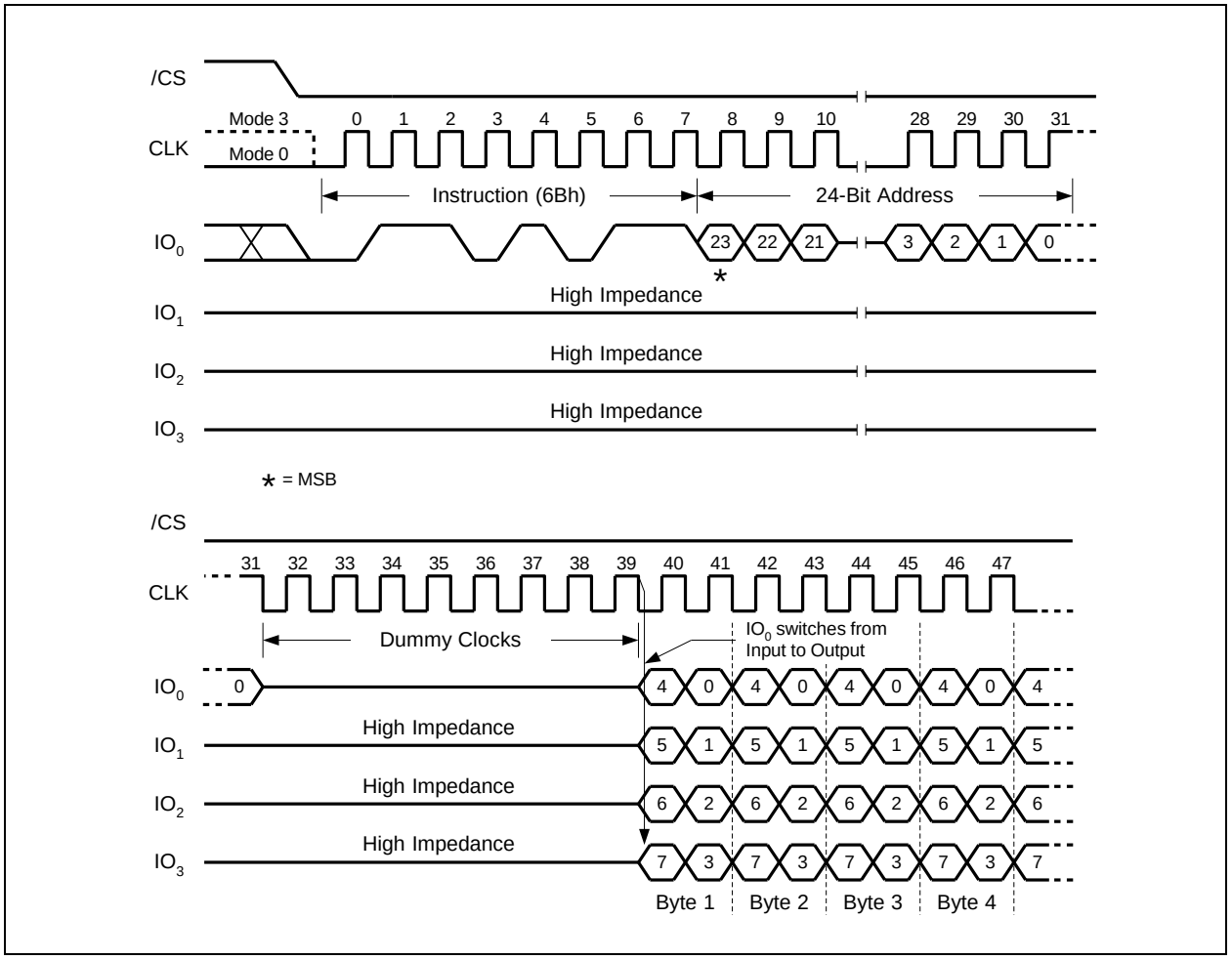


Figure 21. Fast Read Quad Output Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.5.16 Fast Read Quad Output with 4-Byte Address (6Ch)

The Fast Read Quad Output with 4-Byte Address instruction is similar to the Fast Read Quad Output instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad Output with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

The Fast Read Quad Output with 4-Byte Address (6Ch) instruction is only supported in Standard SPI mode.

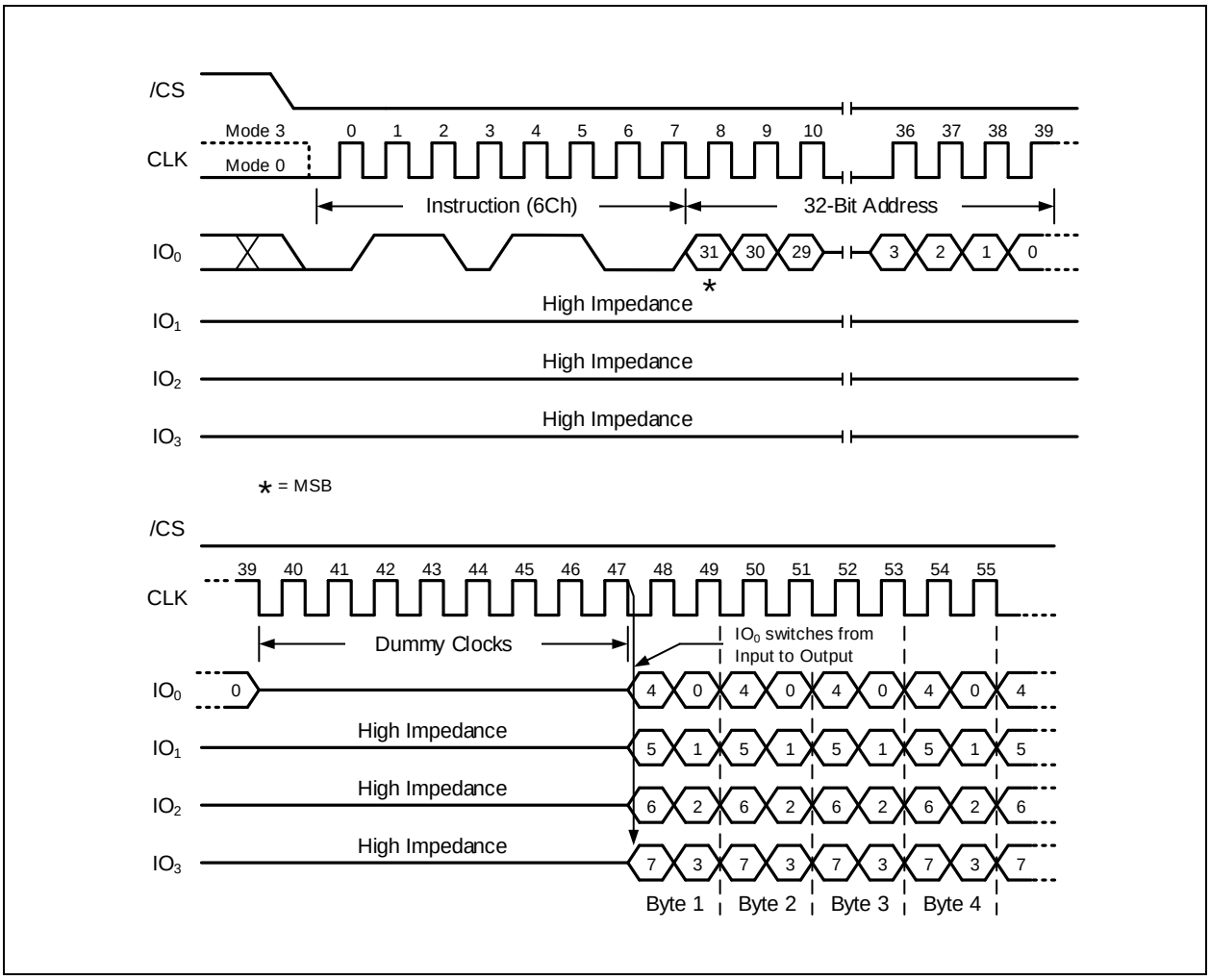


Figure 22. Fast Read Quad Output with 4-Byte Address Instruction (SPI Mode only)

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8.5.17 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23/A31-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Similar to the Fast Read Dual Output (3Bh) instruction, the Fast Read Dual I/O instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding four “dummy” clocks after the 24/32-bit address as shown in Figure 23. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

Fast Read Dual I/O with “Read Command Bypass Mode”

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the Read Command Bypass Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 22a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don’t care (“x”). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Read Command Bypass Mode bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 22b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the Read Command Bypass Mode bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

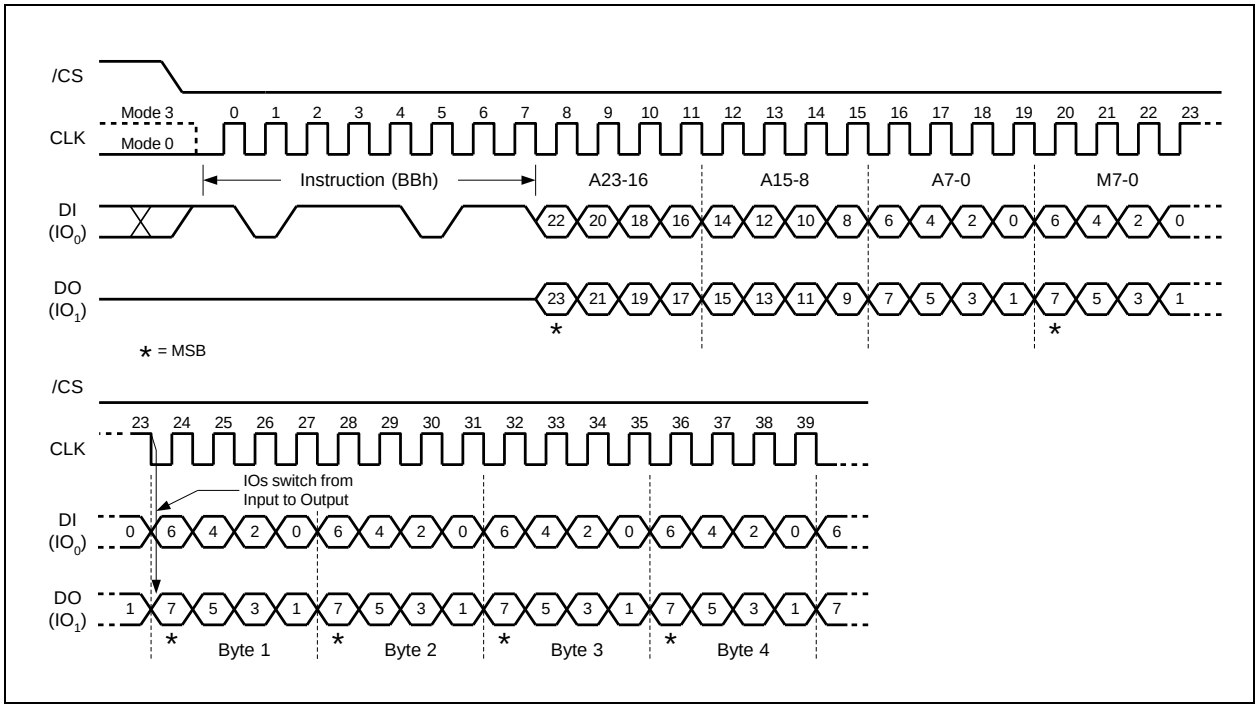


Figure 23a. Fast Read Dual I/O (Initial instruction or previous M5-4≠10, SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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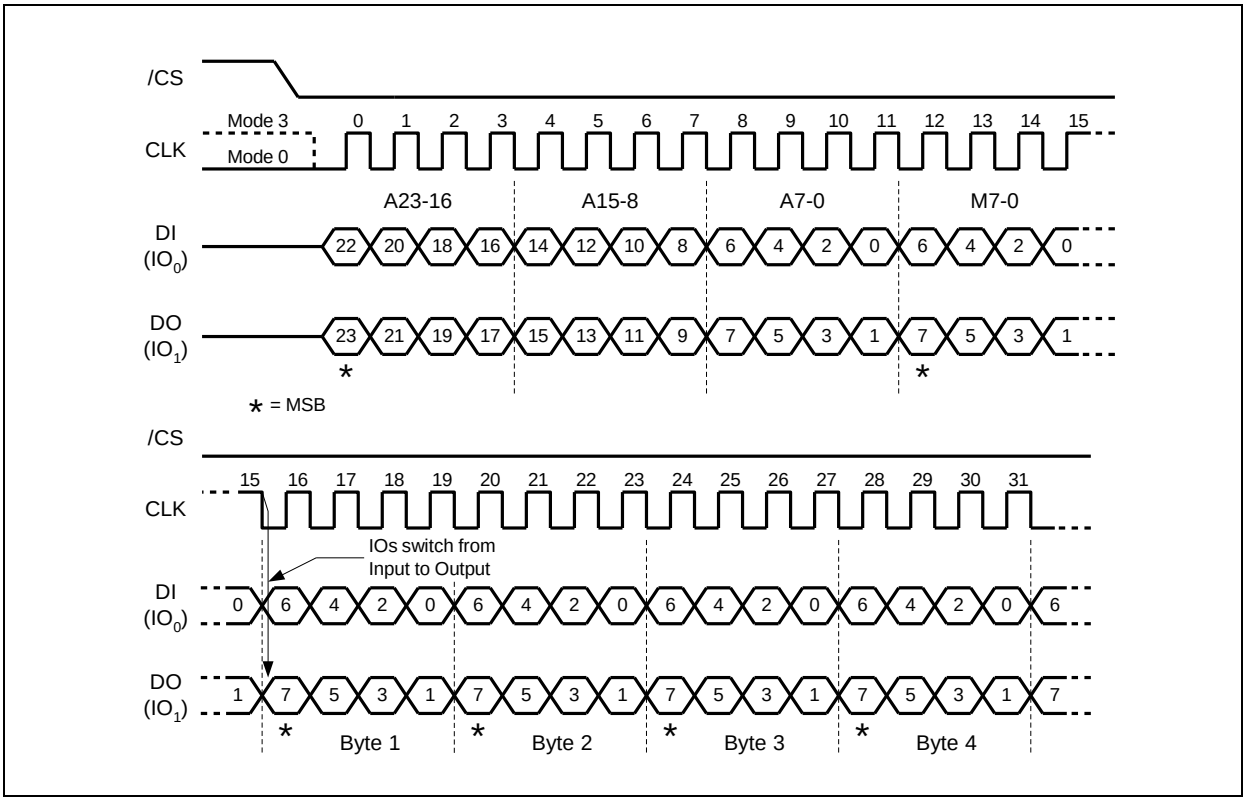


Figure 23b. Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.5.18 DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/O (BDh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23/A31-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

DTR Fast Read Dual I/O with (Read Command Bypass Mode)

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the Read Command Bypass Mode)bits (M7-0) after the input Address bits (A23-0), as shown in Figure 23a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Read Command Bypass Mode bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 23b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the Read Command Bypass Mode bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh/FFFFFh on IO0 for the next instruction (16/20 clocks), to ensure M4 = 1 and return the device to normal operation.

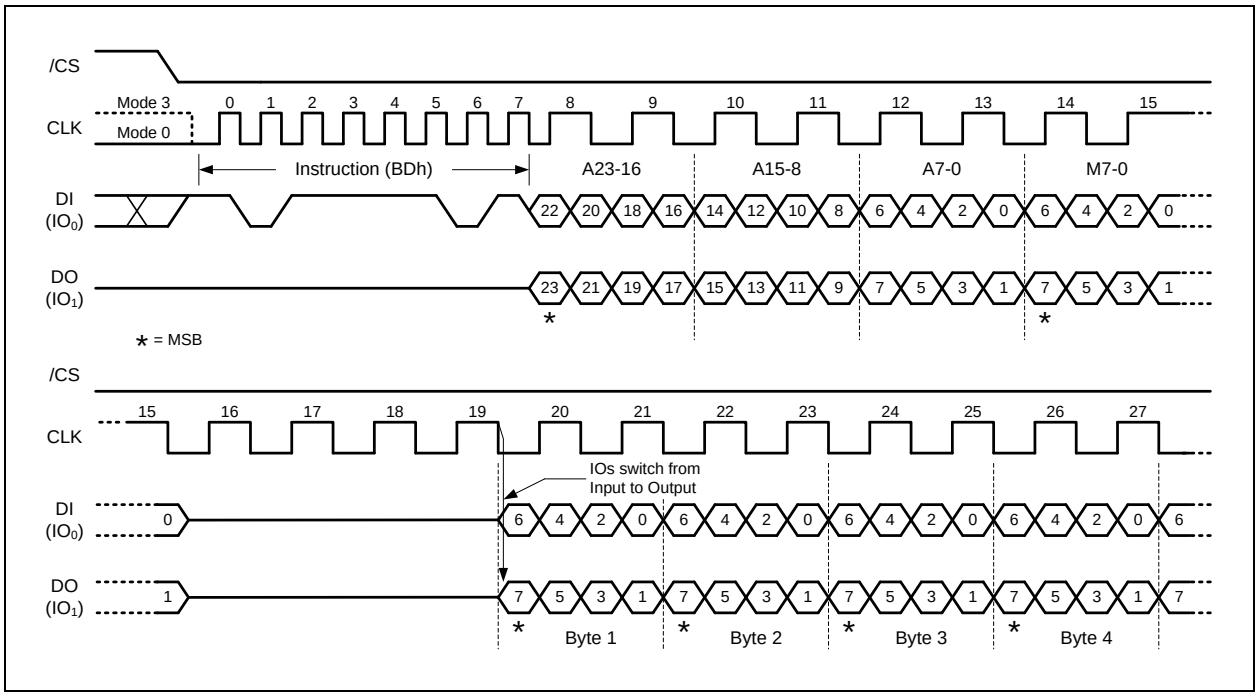


Figure 24a. DTR Fast Read Dual I/O (Initial instruction or previous M5-4≠10, SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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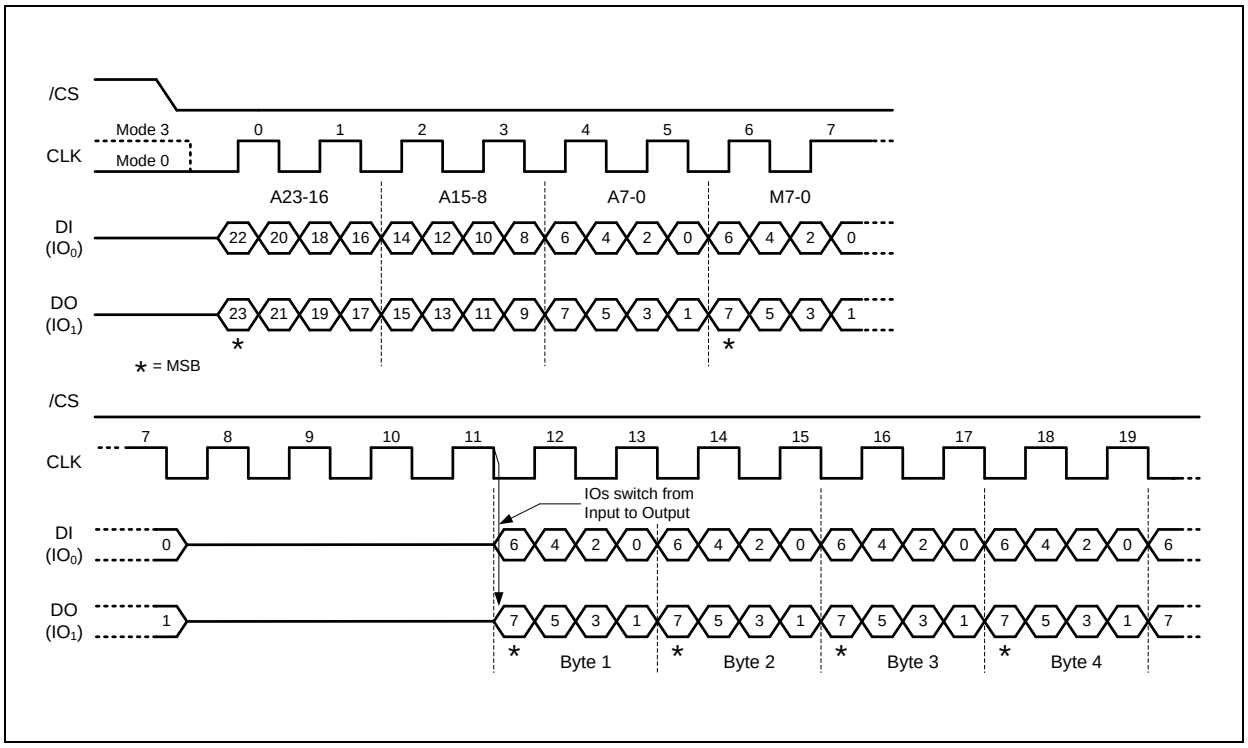


Figure 23b. DTR Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)

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8.5.19 Fast Read Dual I/O with 4-Byte Address (BCh)

The Fast Read Dual I/O with 4-Byte Address instruction is similar to the Fast Read Dual I/O instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Dual I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

The Fast Read Dual I/O with 4-Byte Address (BCh) instruction is only supported in Standard SPI mode.

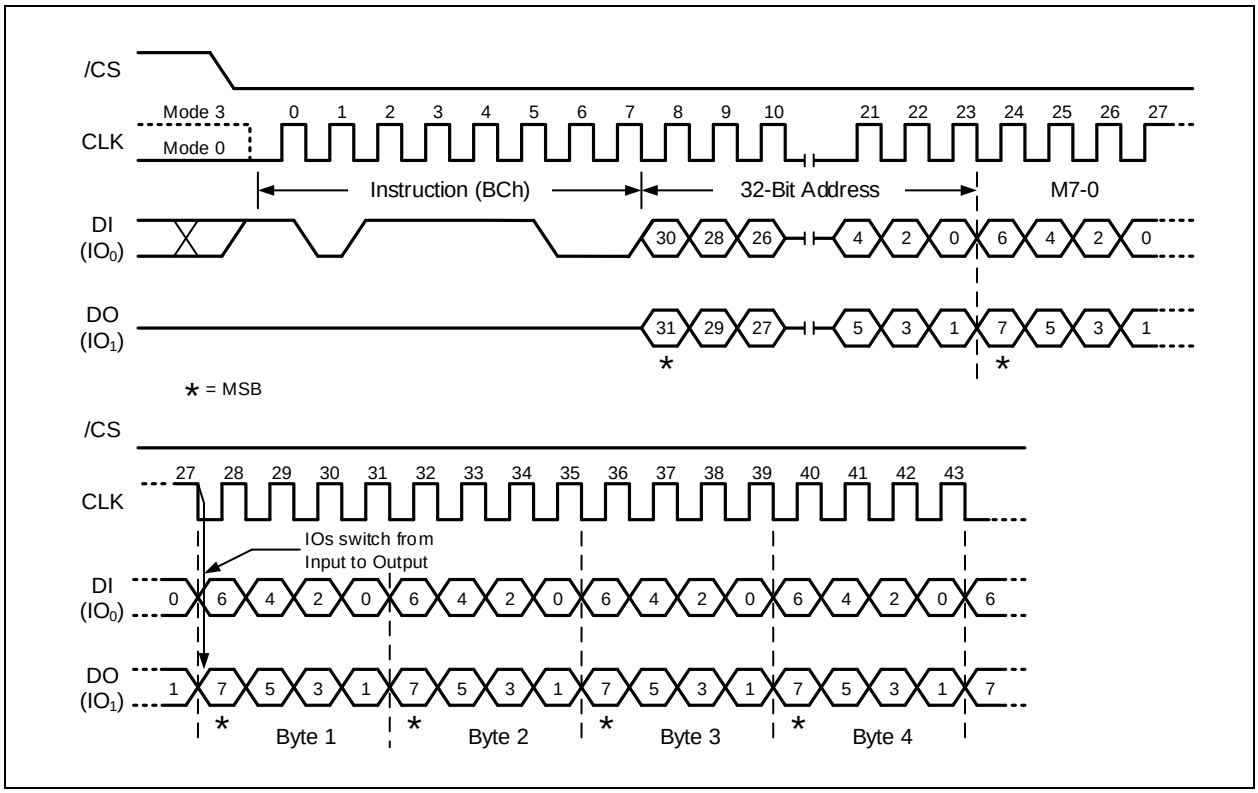


Figure 25a. Fast Read Dual I/O w/ 4-Byte Addr. (Initial instruction or previous M5-4≠10, SPI Mode only)

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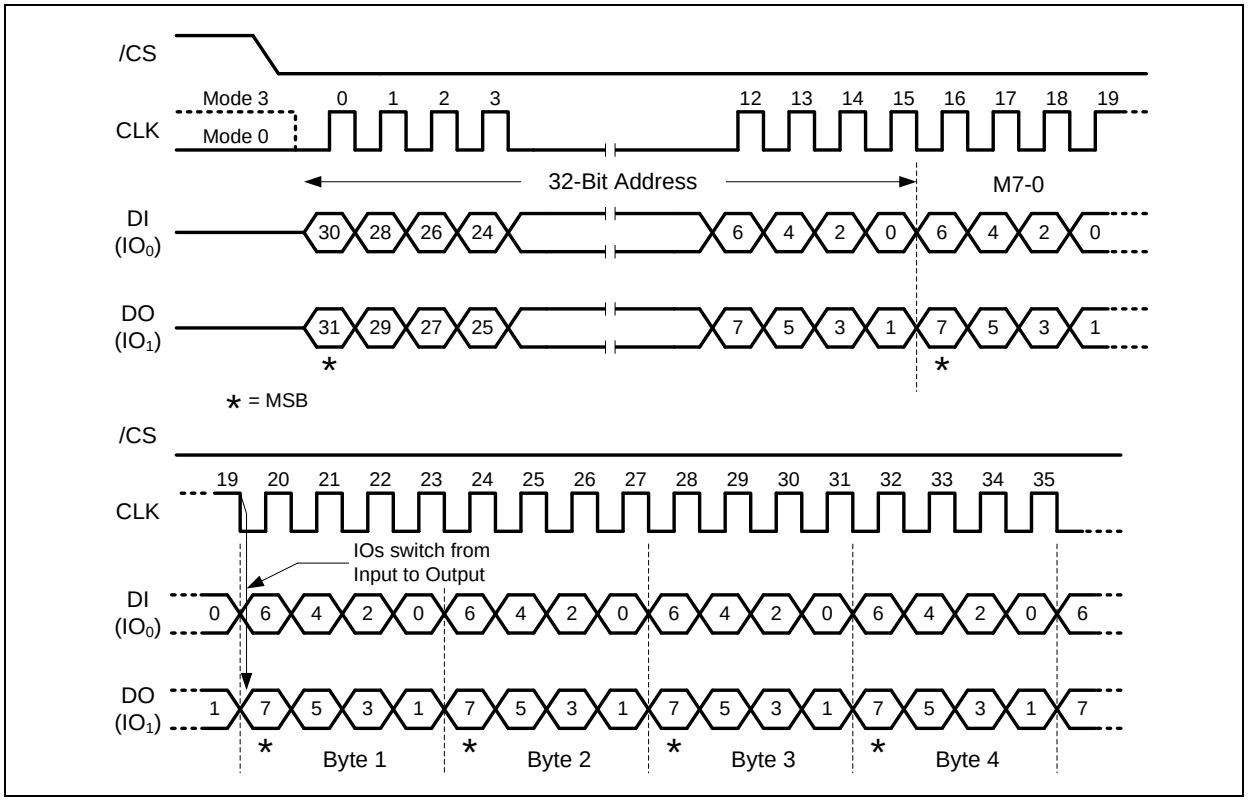


Figure 25b. Fast Read Dual I/O w/ 4-Byte Addr. (Previous instruction set M5-4=10, SPI Mode only)

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8.5.20 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Fast Read Quad I/O with "Read Command Bypass Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the Read Command Bypass Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 24a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Read Command Bypass Mode bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 24b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the Read Command Bypass Mode bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

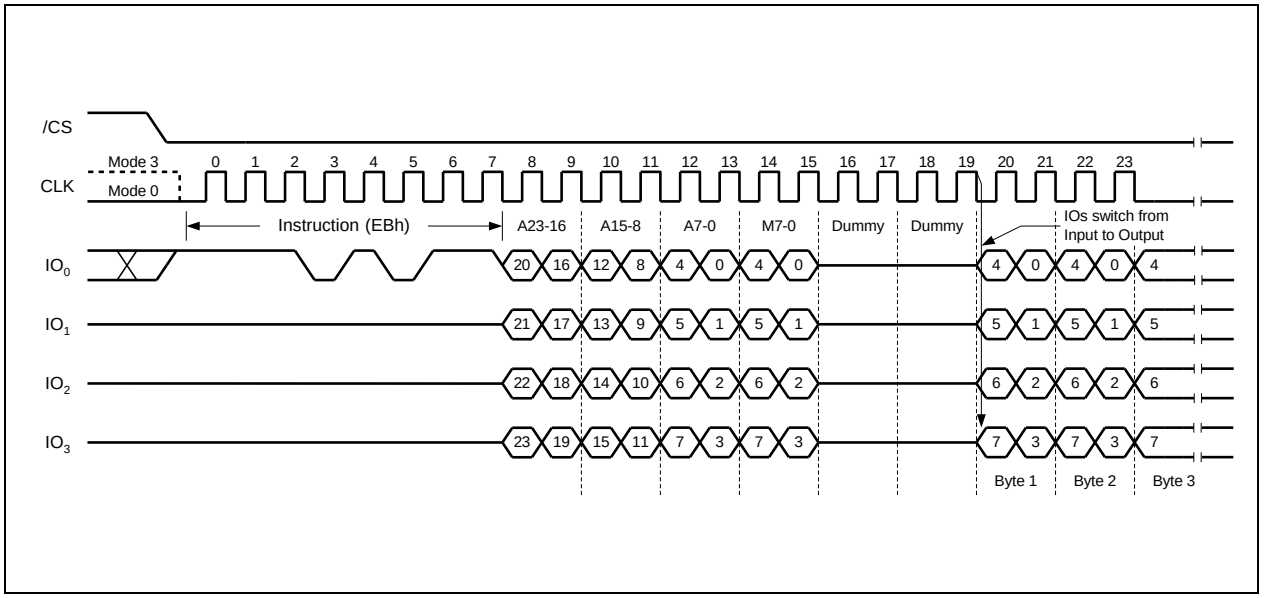


Figure 26a. Fast Read Quad I/O (Initial instruction or previous M5-4≠10, SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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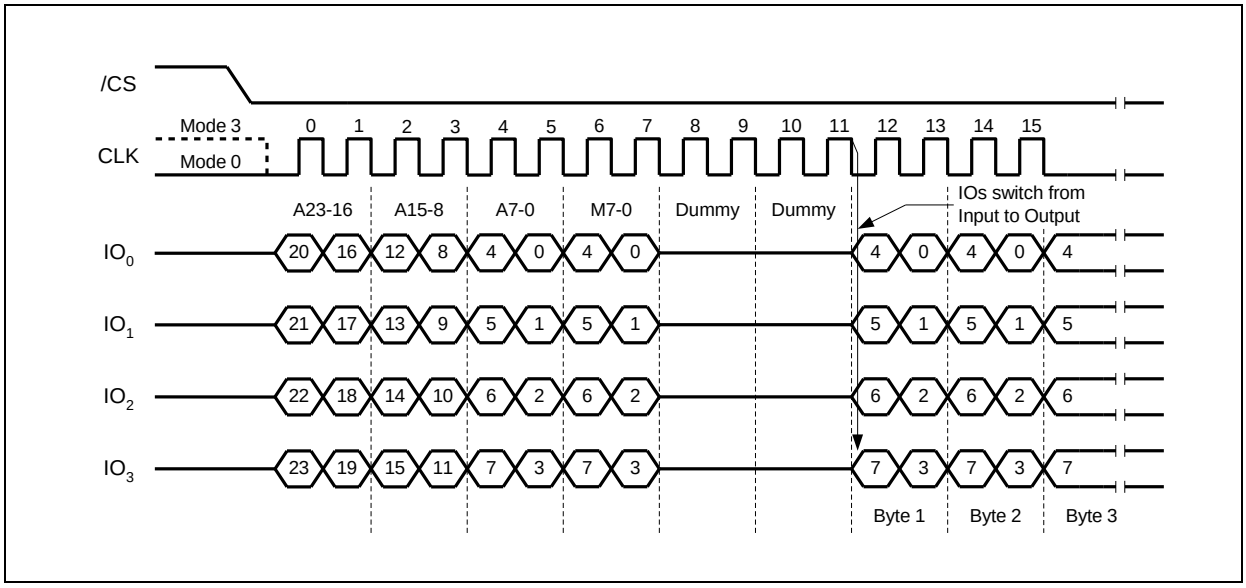


Figure 24b. Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section 8.2.25 for detail descriptions.

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Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 26c. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2.

“Wrap Around” feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be used. Please refer to 8.2.50 for details.

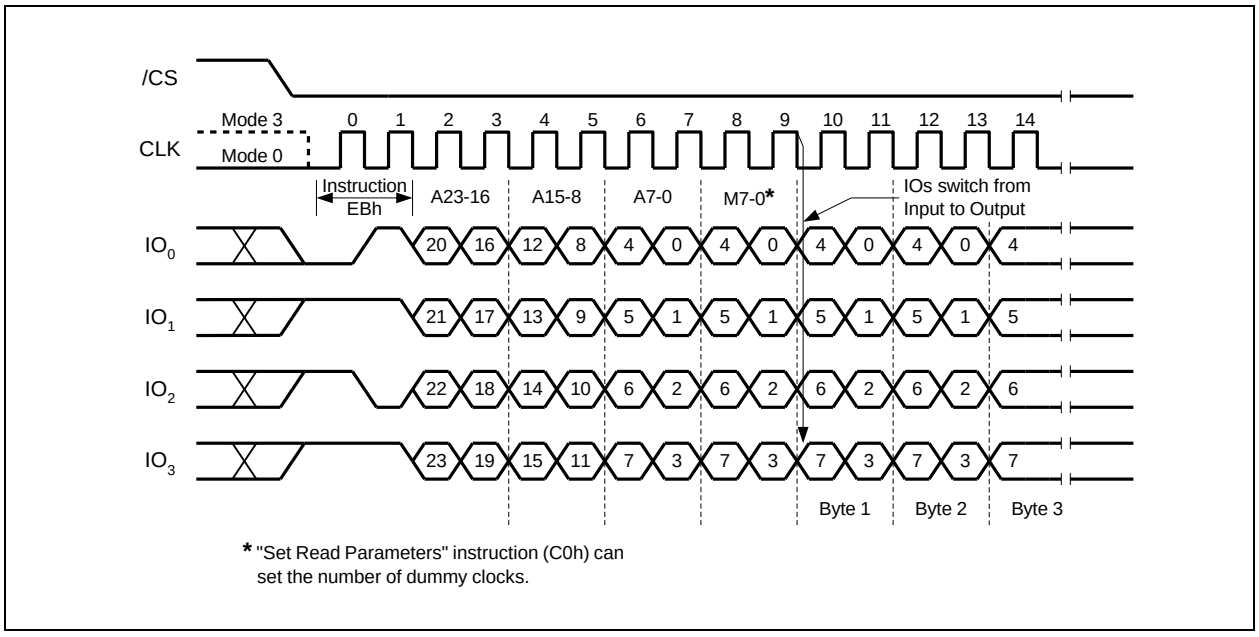


Figure 26c. Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.5.21 DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

DTR Fast Read Quad I/O with "Read Command Bypass Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the Read Command Bypass Mode bits (M7-0) after the input Address bits (A23/A31-0), as shown in Figure 27a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Read Command Bypass Mode bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 27b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the Read Command Bypass Mode bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh/3FFh on IO0 for the next instruction (8/10 clocks), to ensure M4 = 1 and return the device to normal operation.

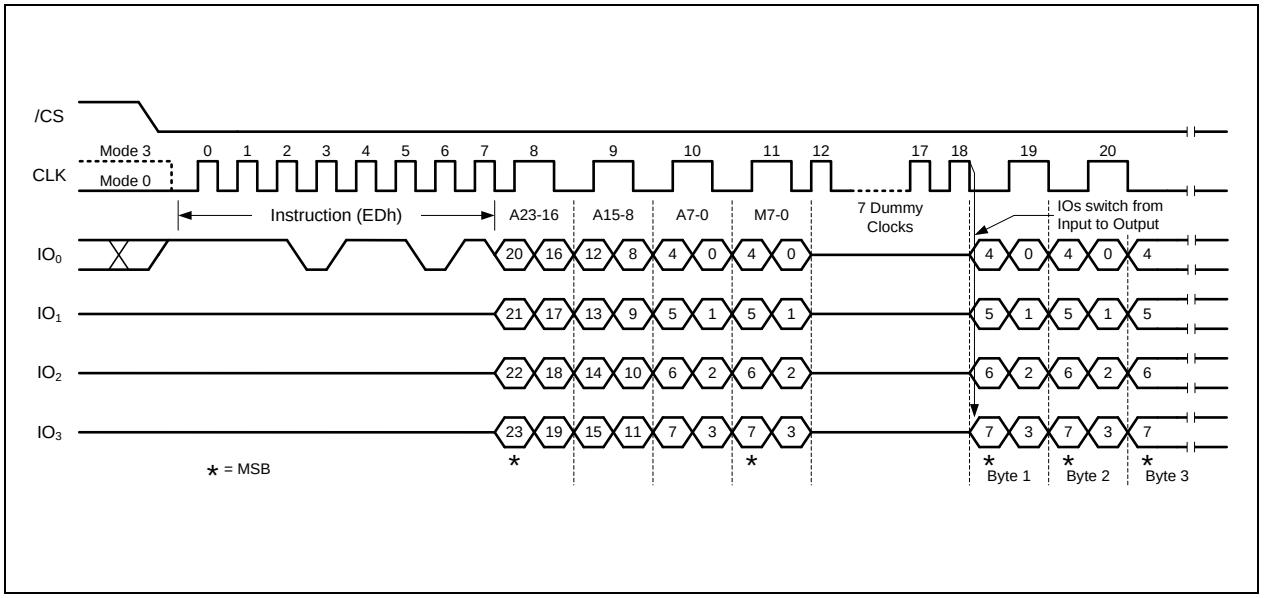


Figure 27a. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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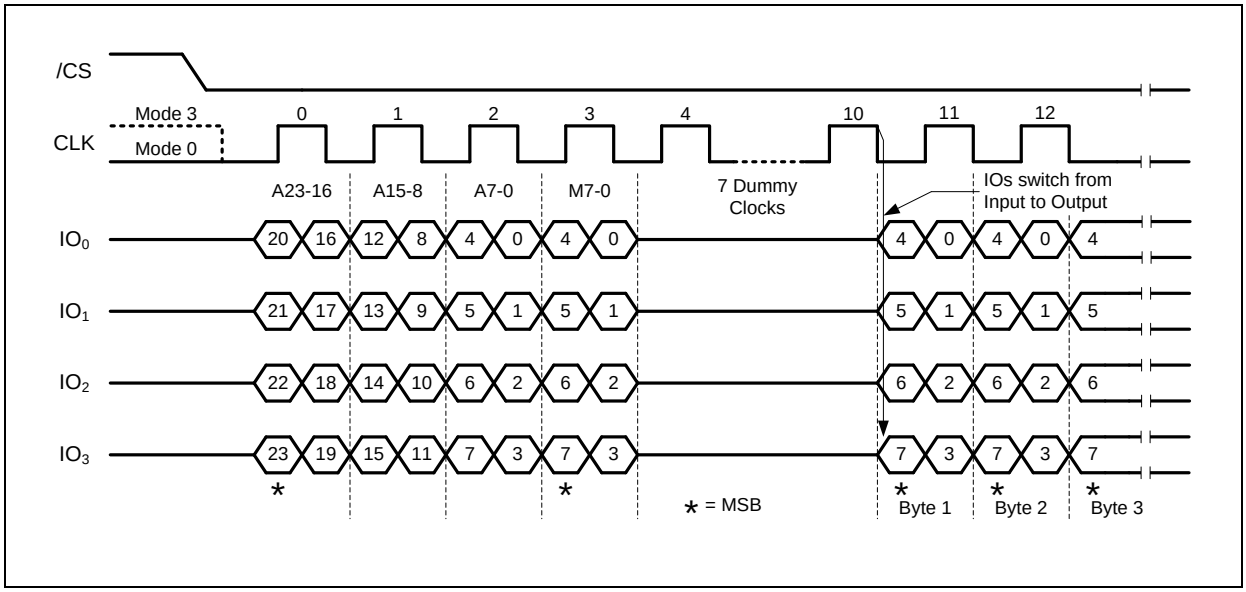


Figure 27b. Fast Read Quad I/O (Previous instruction set M5-4=10, SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

DTR Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EDh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EDh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section 8.2.49 for detail descriptions.

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DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 27c

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used. Please refer to 8.2.50 for details.

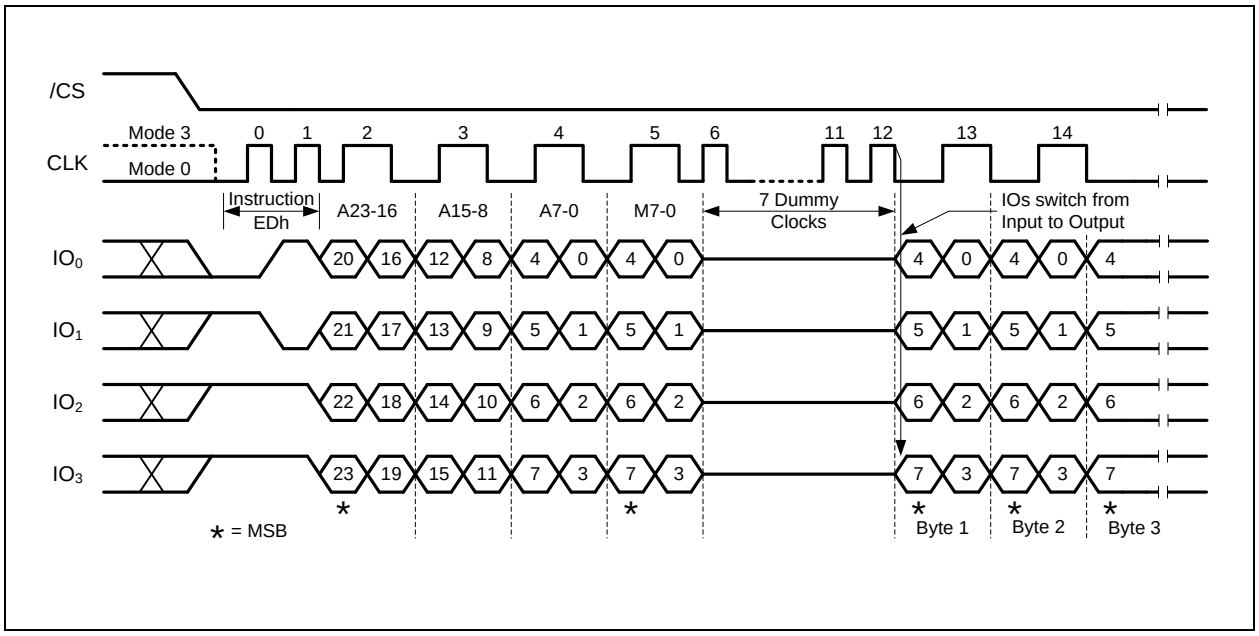


Figure 27c. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.5.22 Fast Read Quad I/O with 4-Byte Address (ECh)

The Fast Read Quad I/O with 4-Byte Address instruction is similar to the Fast Read Quad I/O instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

The Fast Read Quad I/O with 4-Byte Address (ECh) instruction is only supported in Standard SPI mode.

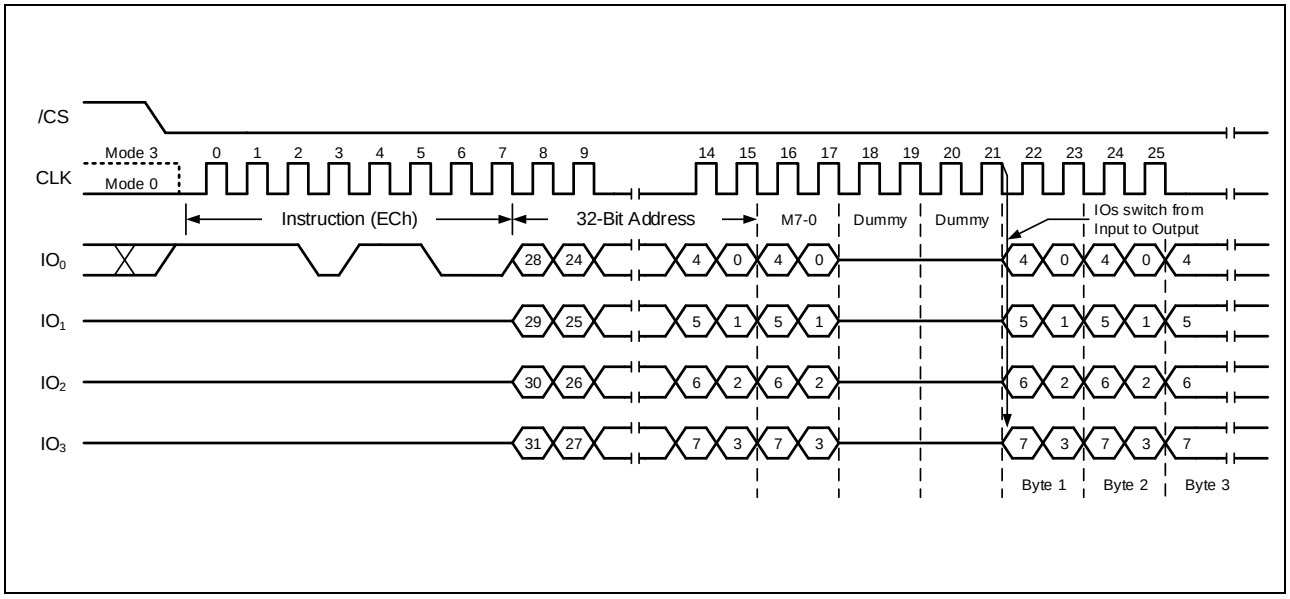


Figure 28a. Fast Read Quad I/O w/ 4-Byte Addr. (Initial instruction or previous M5-4=Fxh, SPI Mode only)

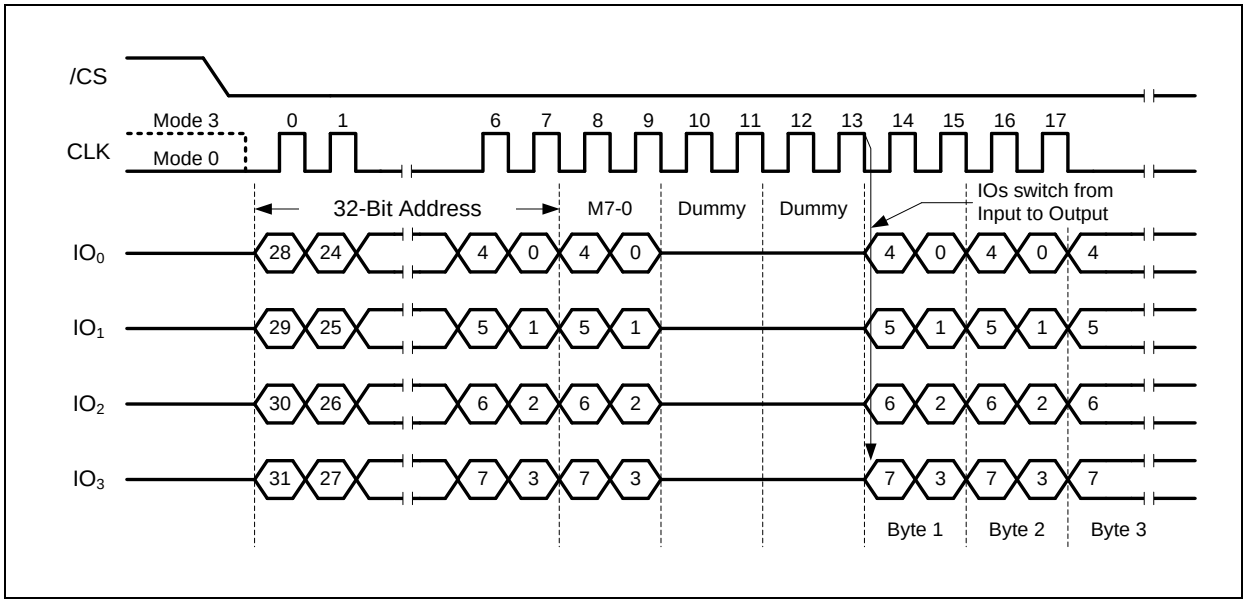


Figure 28b. Fast Read Quad I/O w/ 4-Byte Addr. (Previous instruction set M5-4=10, SPI Mode only)

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Fast Read Quad I/O with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a “Set Burst with Wrap” (77h) command prior to ECh. The “Set Burst with Wrap” (77h) command can either enable or disable the “Wrap Around” feature for the following ECh commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section 8.2.24 for detail descriptions.

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8.5.23 Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O (EBh)”, “Fast Read Quad I/O with 4-Byte Address (ECh)”, and “DTR Fast Read Quad I/O (EDh)” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24/32 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 35. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following “Fast Read Quad I/O (EBh)”, “Fast Read Quad I/O with 4-Byte Address (ECh)”, and “DTR Fast Read Quad I/O (EDh)” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

In QPI mode, the “Burst Read with Wrap (0Ch)” and “DTR Burst Read with Wrap (0Eh) instructions should be used to perform the Read operation with “Wrap Around” feature. The Wrap Length set by W6-4 in Standard SPI mode is only applicable in SPI mode and not in QPI mode. The Wrap Length in QPI mode is configured by “Set Read Parameters (C0h)” instruction. Refer to Sections 8.2.23, 8.2.24, and 8.2.25 for details.

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8.6 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24/32-bit address (A23/A31-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 32.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

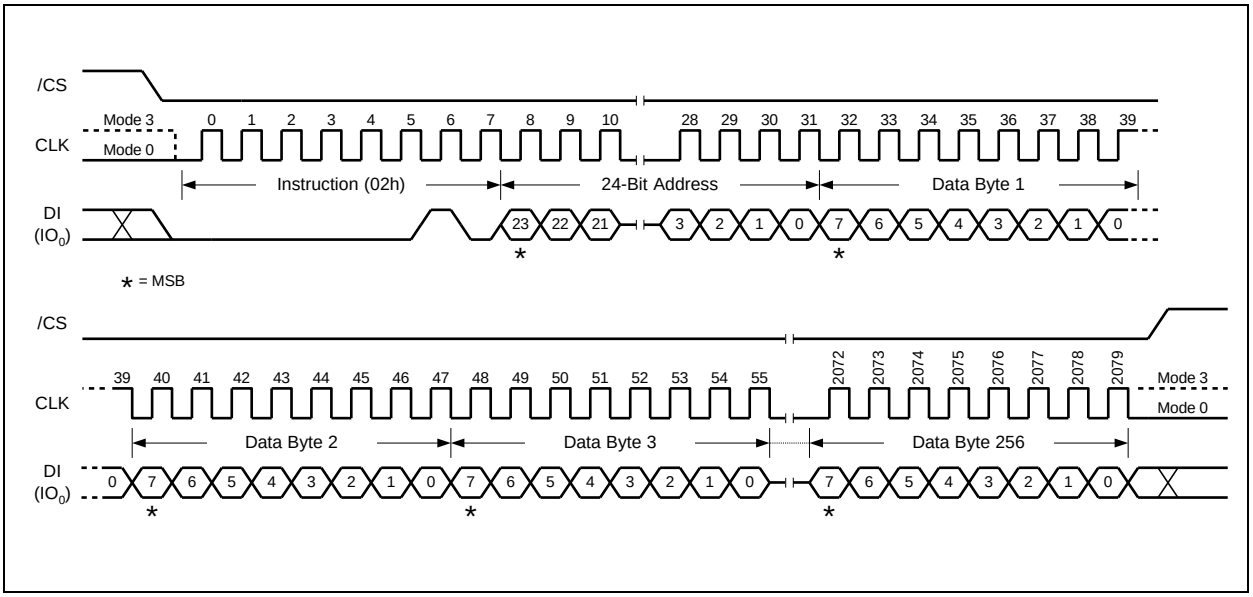


Figure 32a. Page Program Instruction (SPI Mode)

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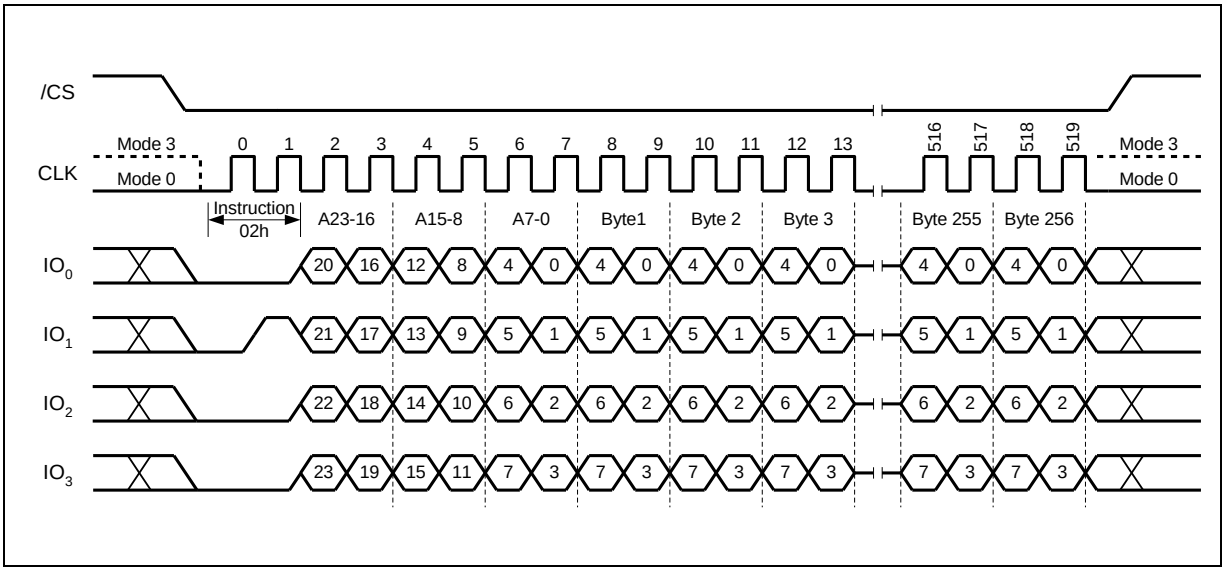


Figure 32b. Page Program Instruction (QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.1 Page Program with 4-Byte Address (12h)

The Page Program with 4-Byte Address instruction is similar to the Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Page Program with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

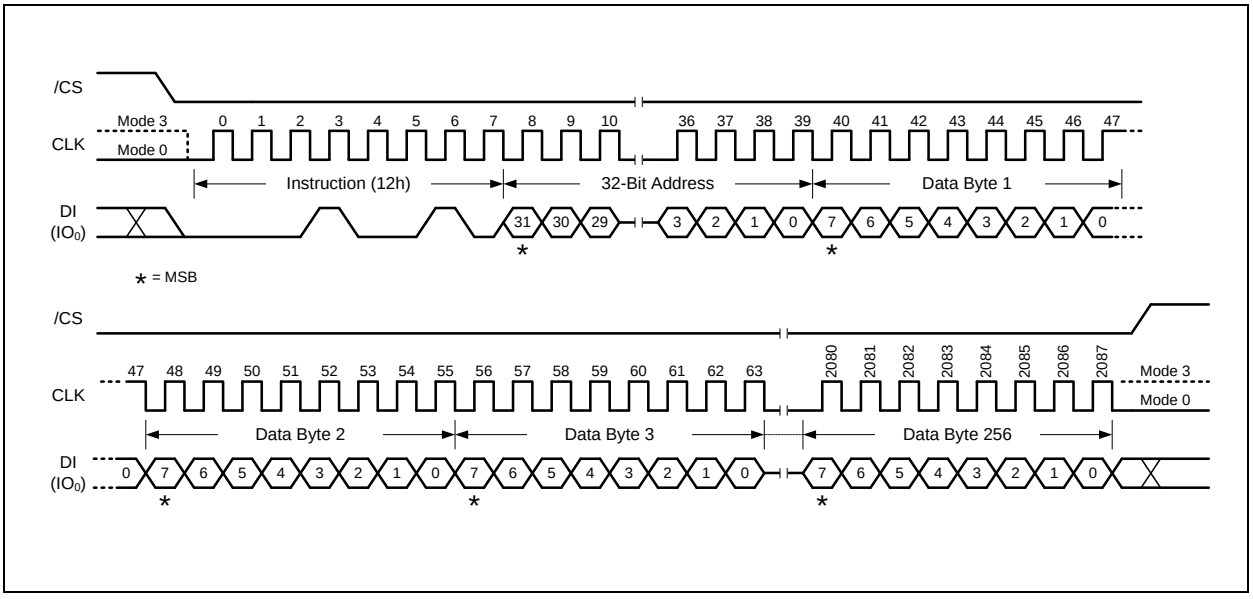


Figure 33. Page Program with 4-Byte Addr. (SPI Mode Only)

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8.6.2 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO_0, IO_1, IO_2, and IO_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "32h" followed by a 24/32-bit address (A23/A31-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 34.

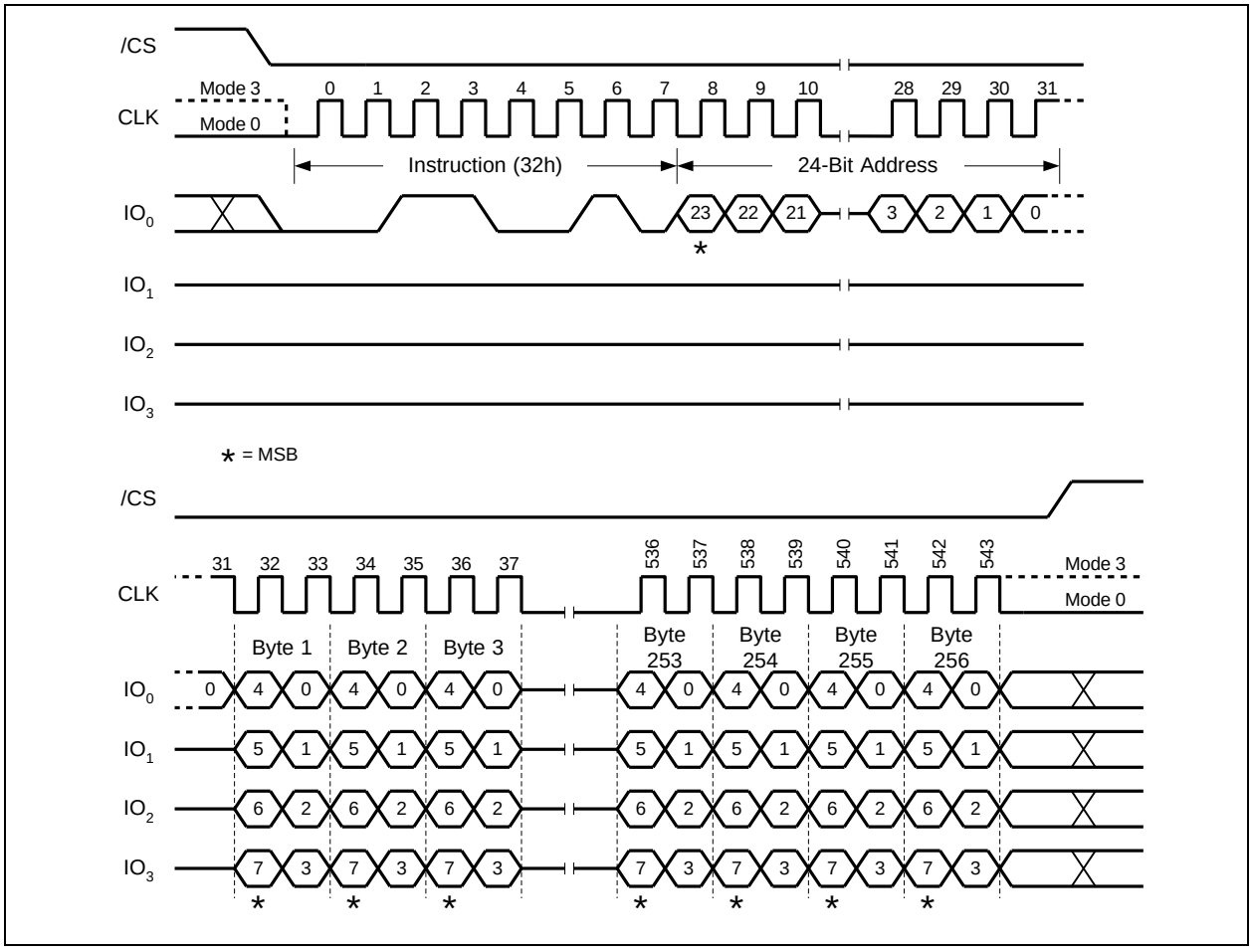


Figure 34. Quad Input Page Program Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.3 Quad Input Page Program with 4-Byte Address (34h)

The Quad Input Page Program with 4-Byte Address instruction is similar to the Quad Input Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Quad Input Page Program with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

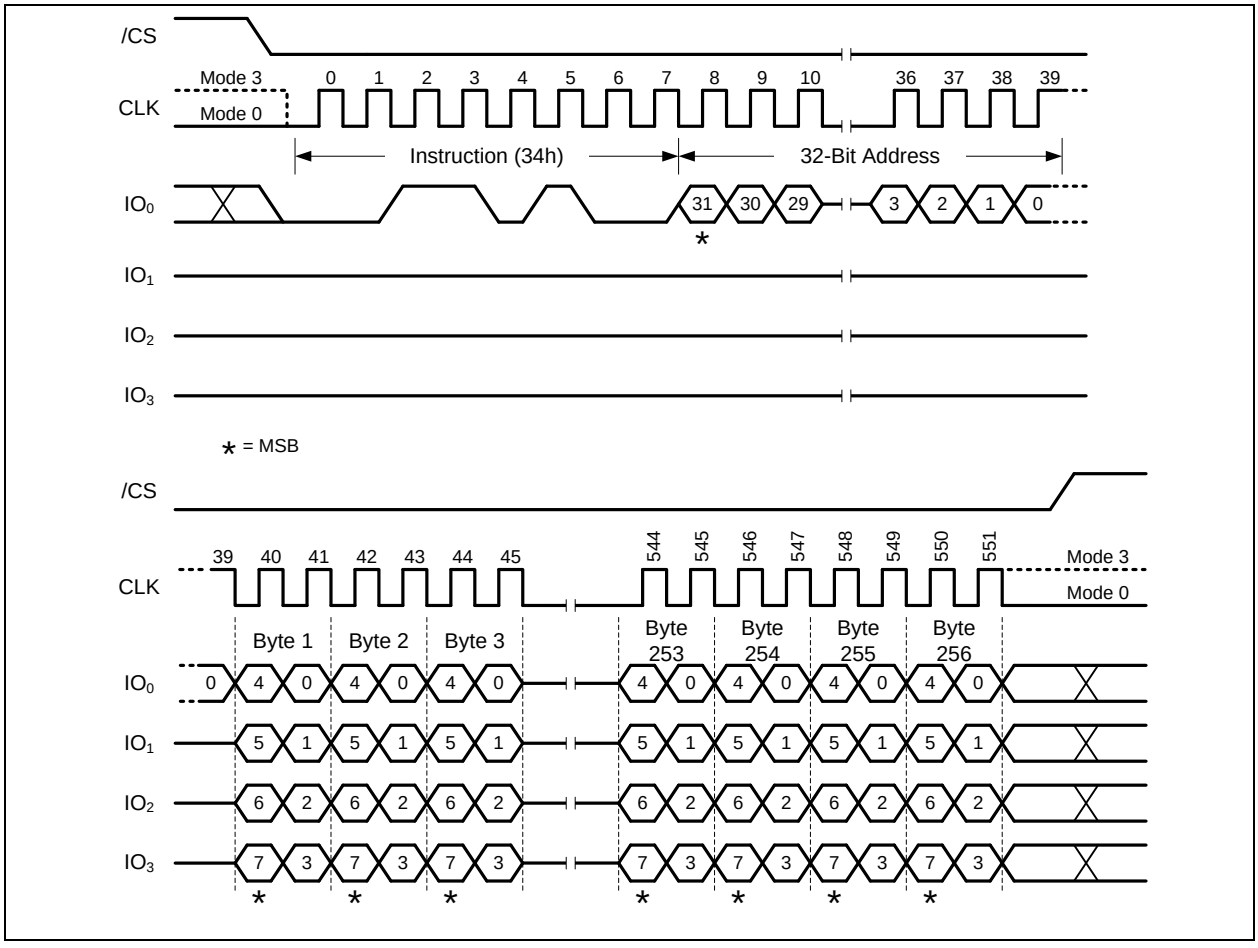


Figure 35. Quad Input Page Program with 4-Byte Addr. (SPI Mode only)

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8.6.4 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24/32-bit sector address (A23/A31-A0). The Sector Erase instruction sequence is shown in Figure 36a & 36b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

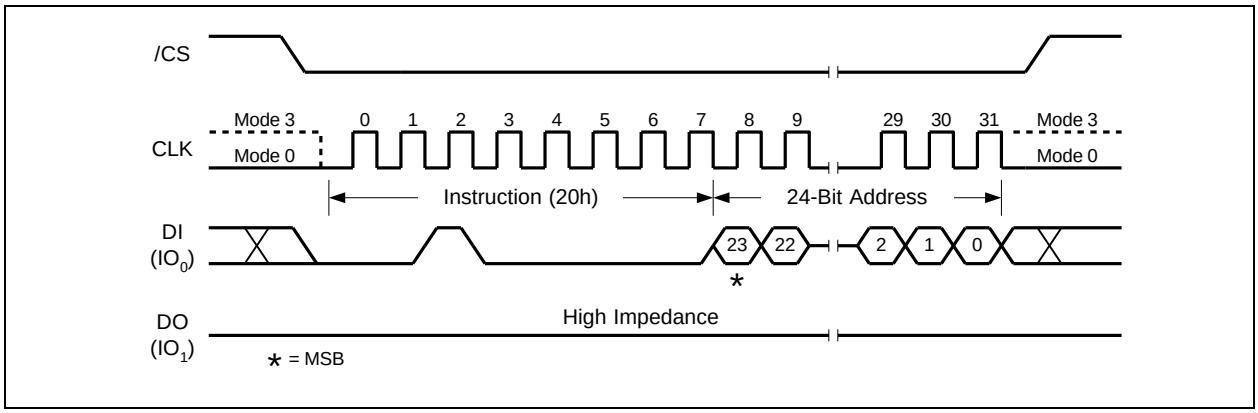


Figure 36a. Sector Erase Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

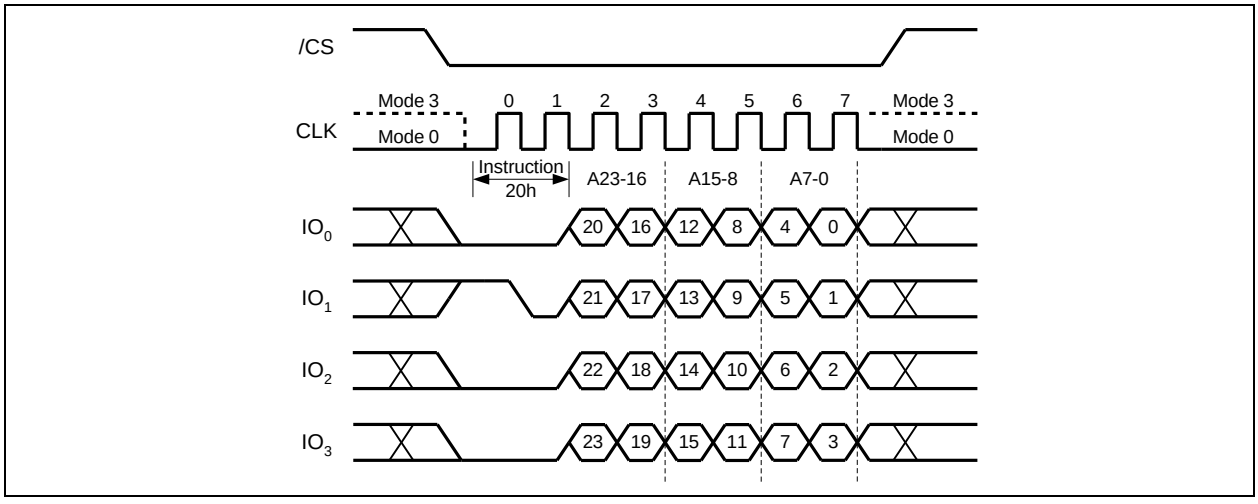


Figure 36b. Sector Erase Instruction (QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.5 Sector Erase with 4-Byte Address (21h)

The Sector Erase with 4-Byte Address instruction is similar to the Sector Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Sector Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

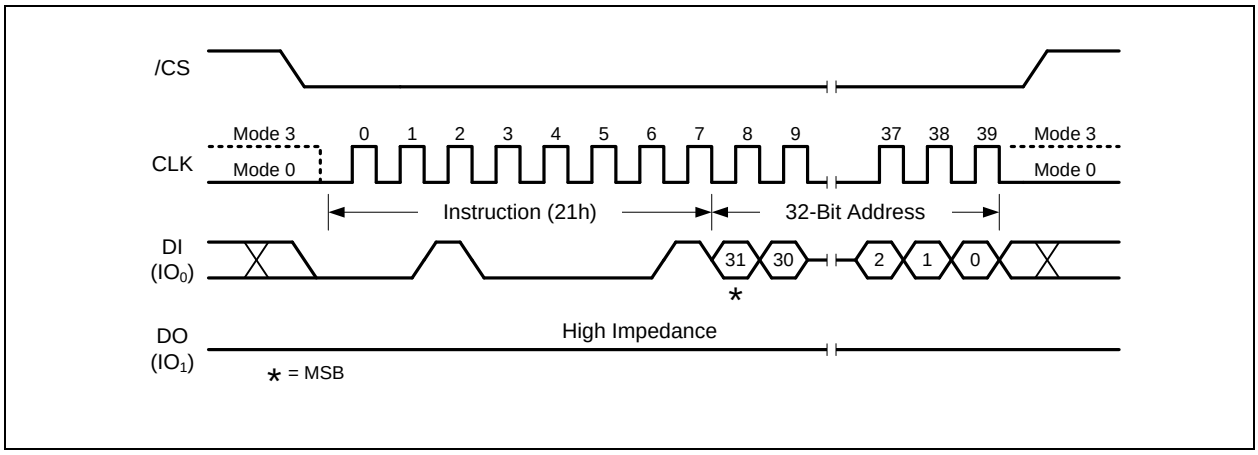


Figure 37. Sector Erase with 4-Byte Address Instruction (SPI Mode Only)

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8.6.6 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "52h" followed a 24/32-bit block address (A23/A31-A0). The Block Erase instruction sequence is shown in Figure 38a & 38b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE1} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

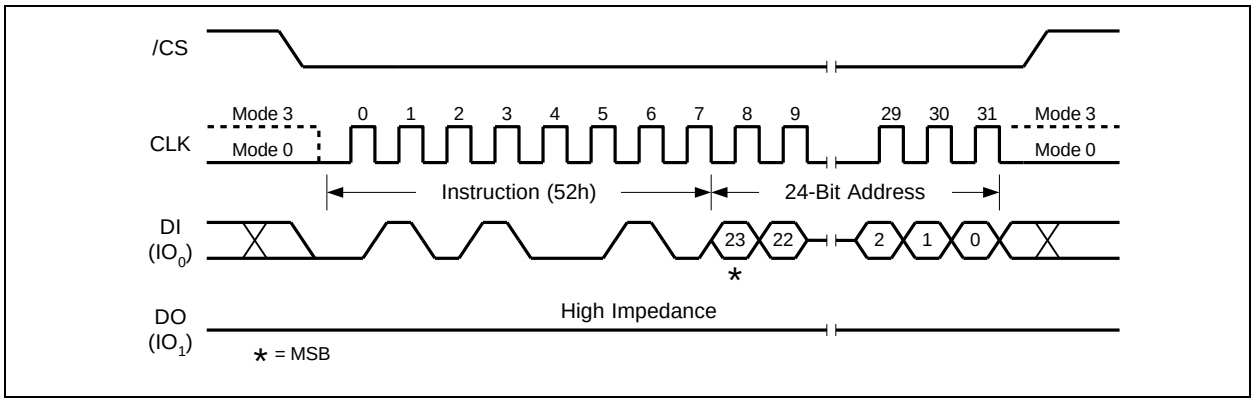


Figure 38a. 32KB Block Erase Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

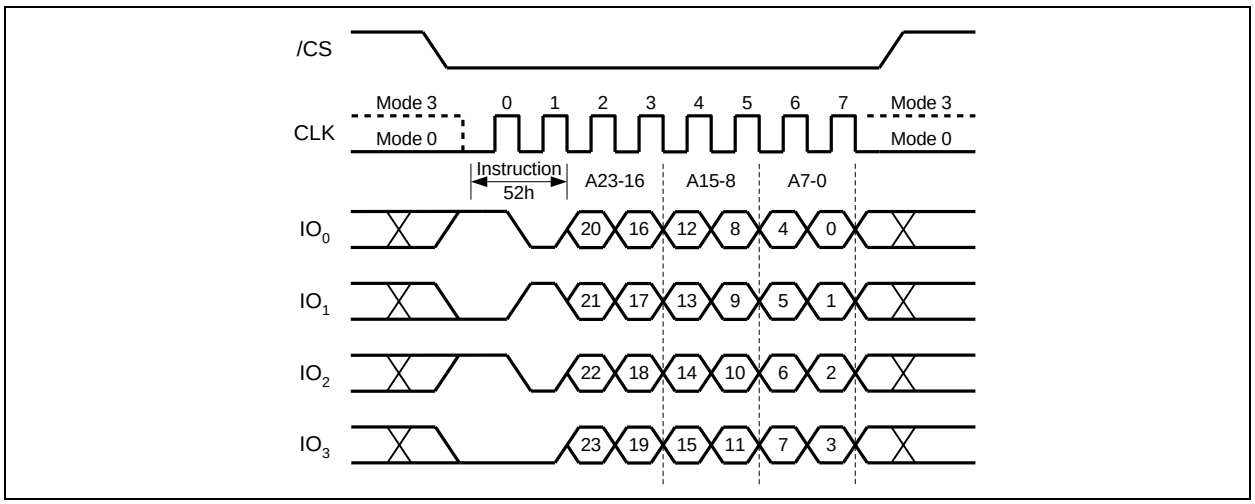


Figure 38b. 32KB Block Erase Instruction (QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.7 64KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24/32-bit block address (A23/A31-A0). The Block Erase instruction sequence is shown in Figure 39a & 39b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

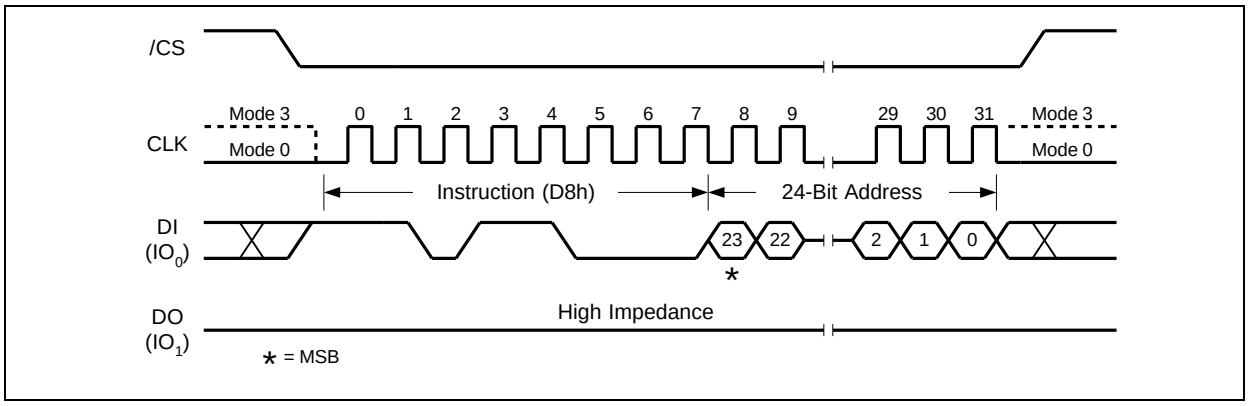


Figure 39a. 64KB Block Erase Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

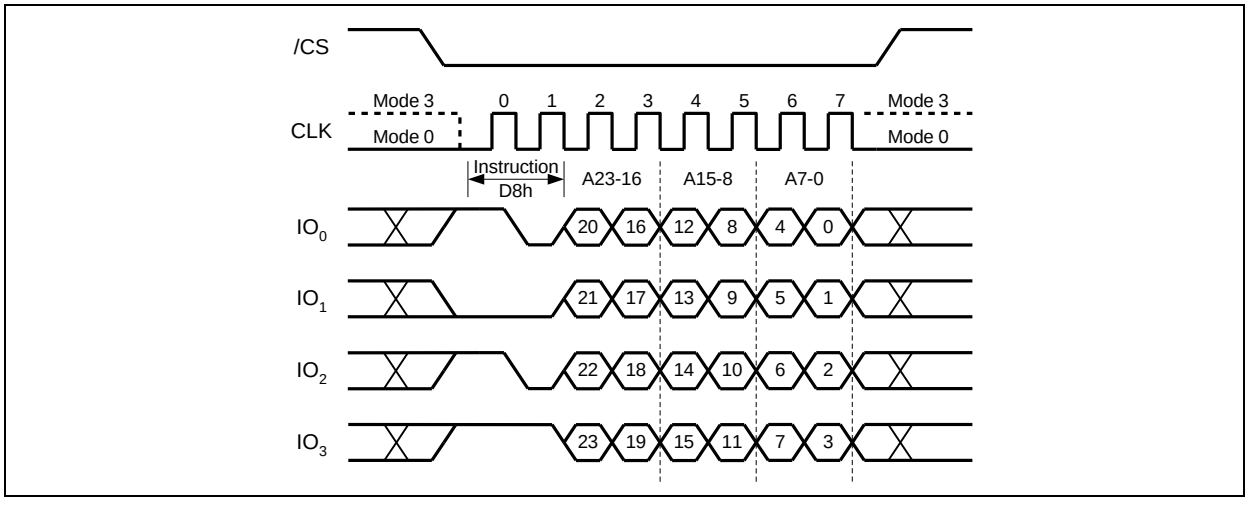


Figure 39b. 64KB Block Erase Instruction (QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.8 64KB Block Erase with 4-Byte Address (DCh)

The 64KB Block Erase with 4-Byte Address instruction is similar to the 64KB Block Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the 64KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 1Gb memory.

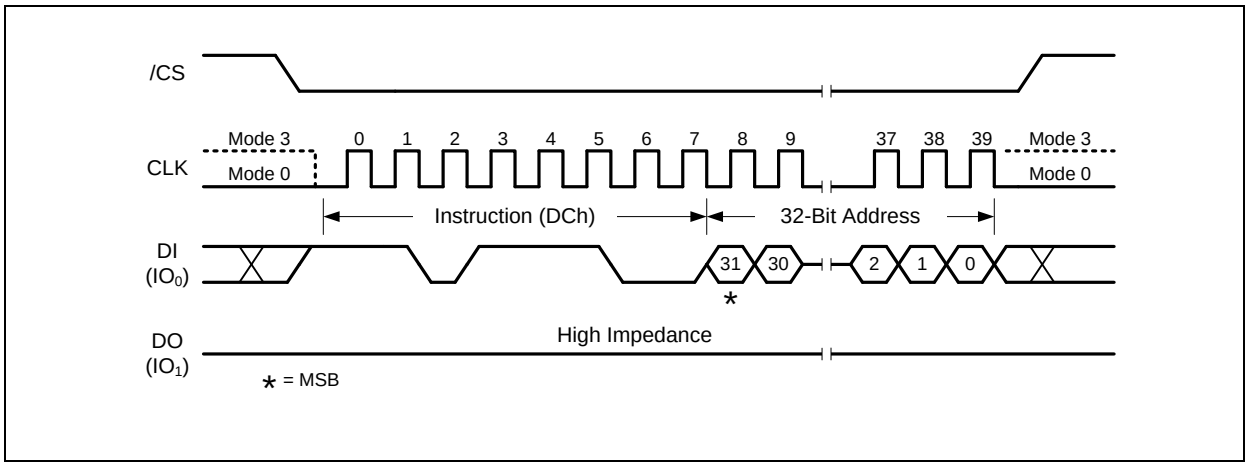


Figure 40. 64KB Block Erase with 4-Byte Address Instruction (SPI Mode Only)

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8.6.9 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 41.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

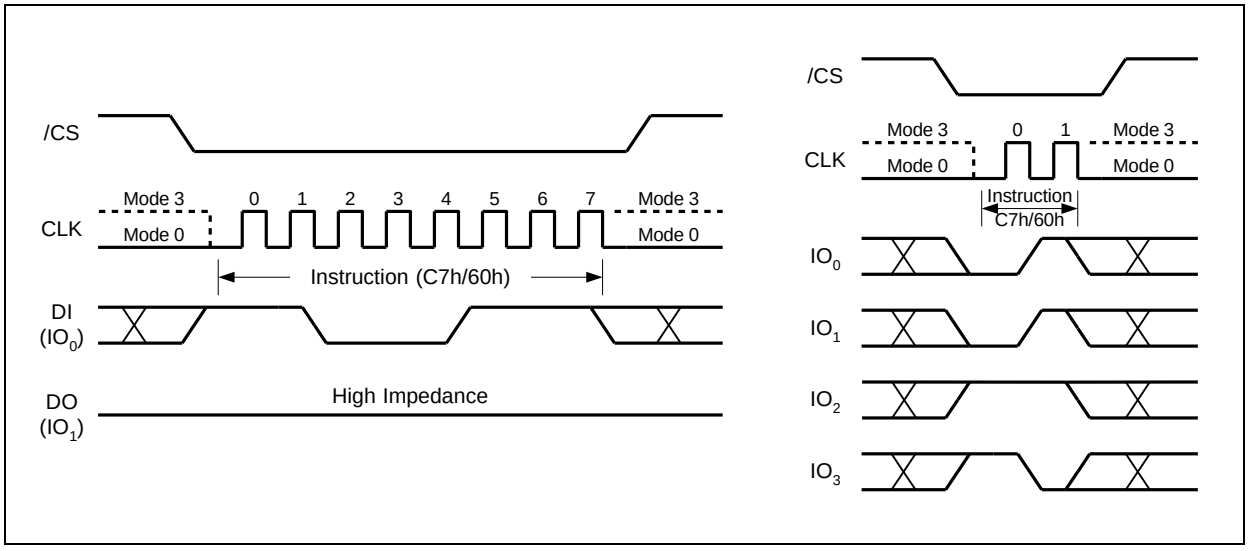


Figure 41. Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)

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8.6.10 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 42a & 42b.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “t_{SUS}” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “t_{SUS}” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “t_{SUS}” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

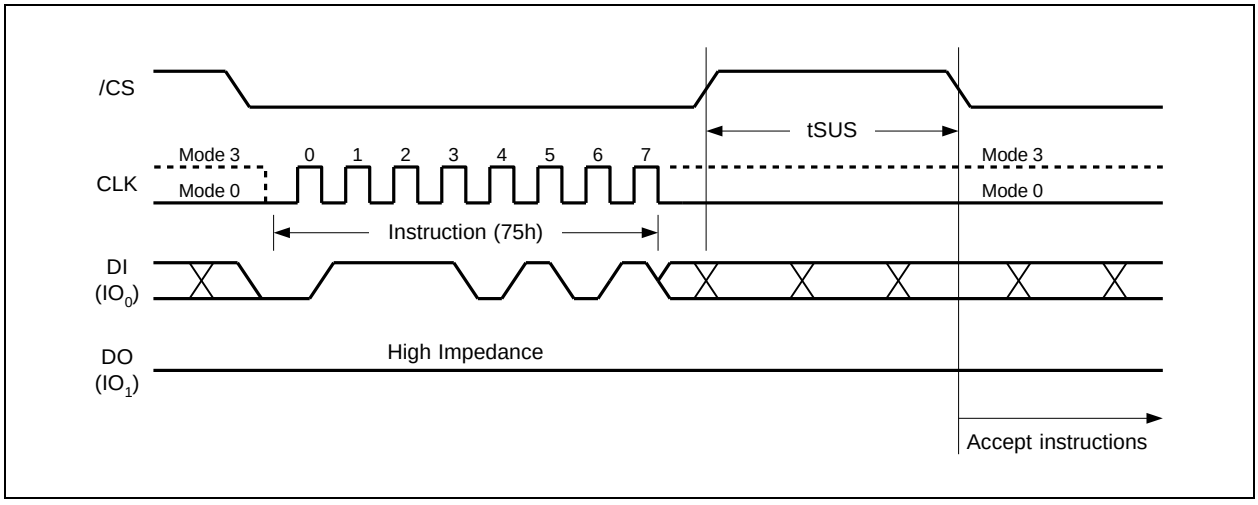


Figure 42a. Erase/Program Suspend Instruction (SPI Mode)

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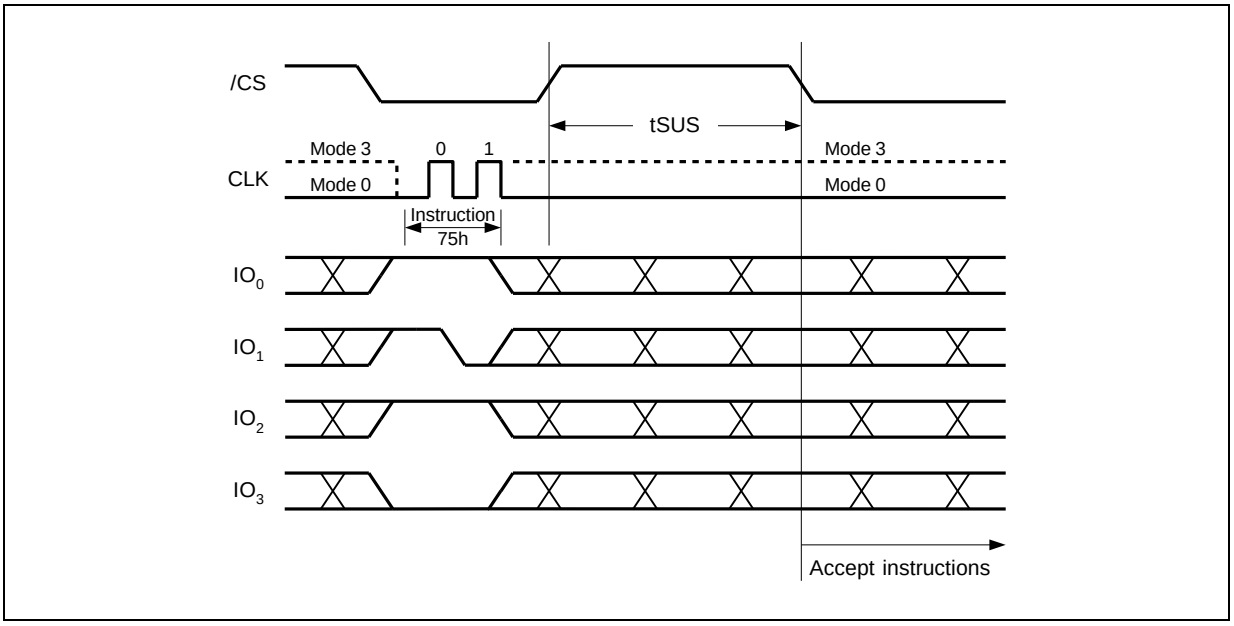


Figure 42b. Erase/Program Suspend Instruction (QPI Mode)

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8.6.11 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 43a & 43b.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “t_{SUS}” following a previous Resume instruction.

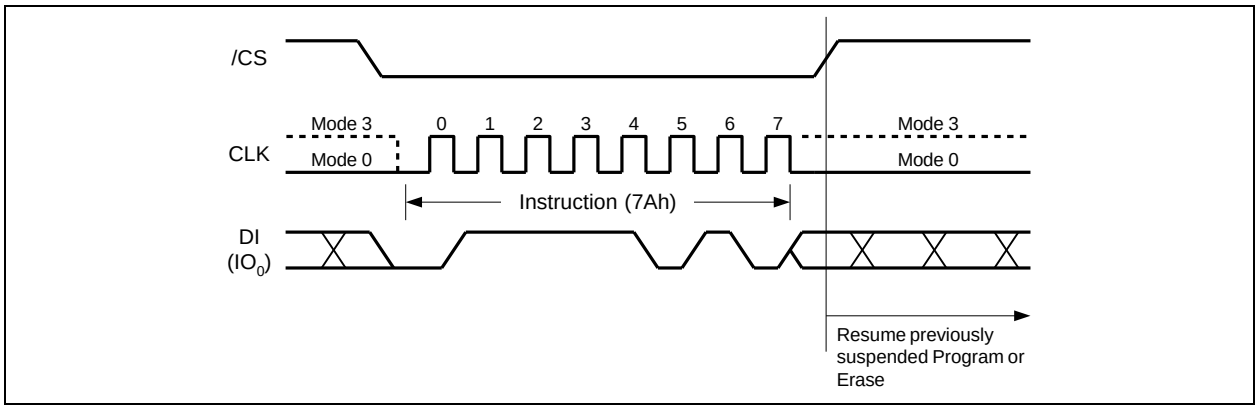


Figure 43a. Erase/Program Resume Instruction (SPI Mode)

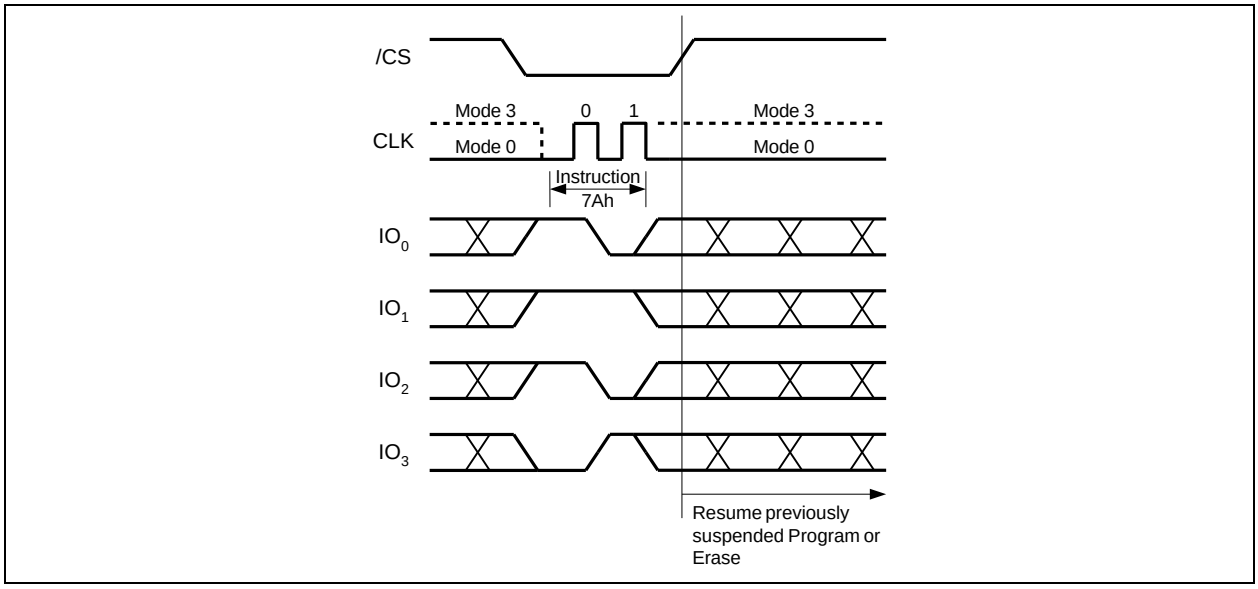


Figure 43b. Erase/Program Resume Instruction (QPI Mode)

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8.6.12 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 44a & 44b.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release Power-down (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

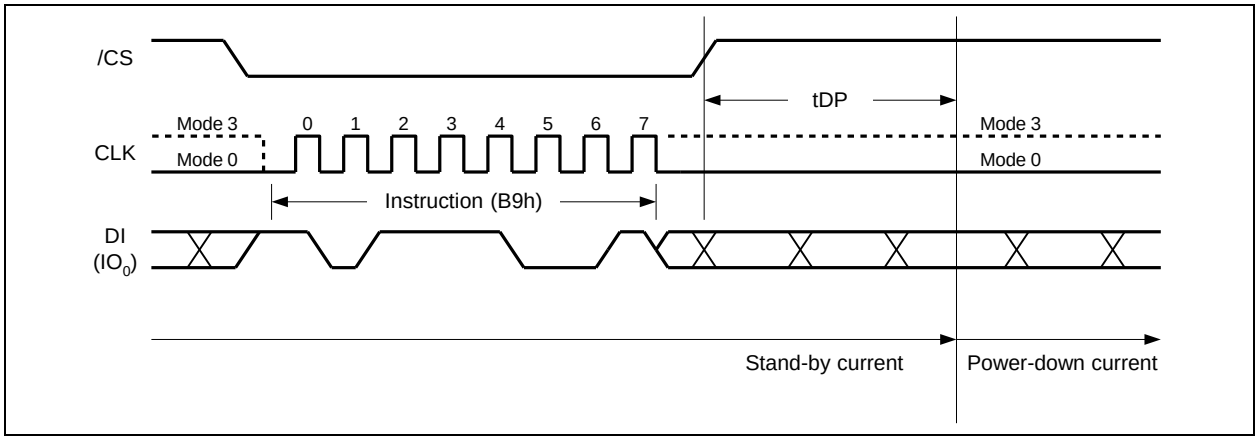


Figure 44a. Deep Power-down Instruction (SPI Mode)

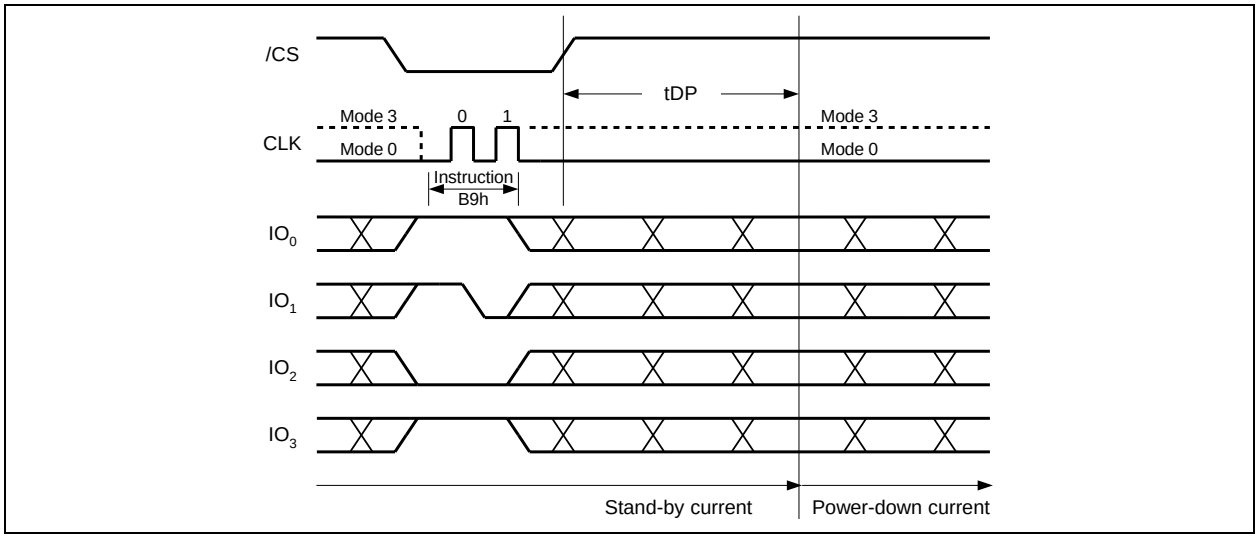


Figure 44b. Deep Power-down Instruction (QPI Mode)

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8.6.13 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in Figure 45a & 45b. Release from power-down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID values for the W25Q01JV is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 45, except that after /CS is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

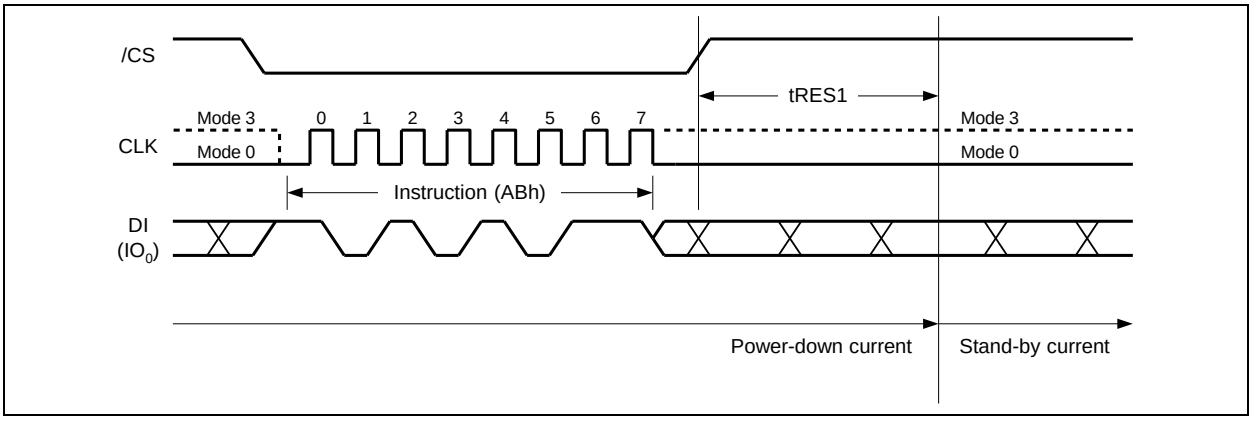


Figure 45a. Release Power-down Instruction (SPI Mode)

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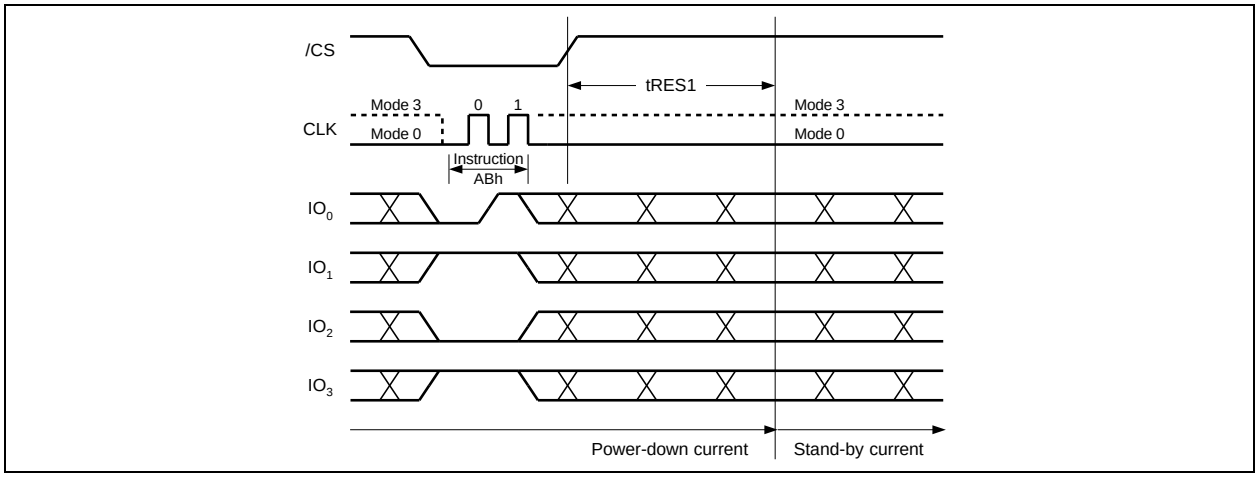


Figure 45b. Release Power-down Instruction (QPI Mode)

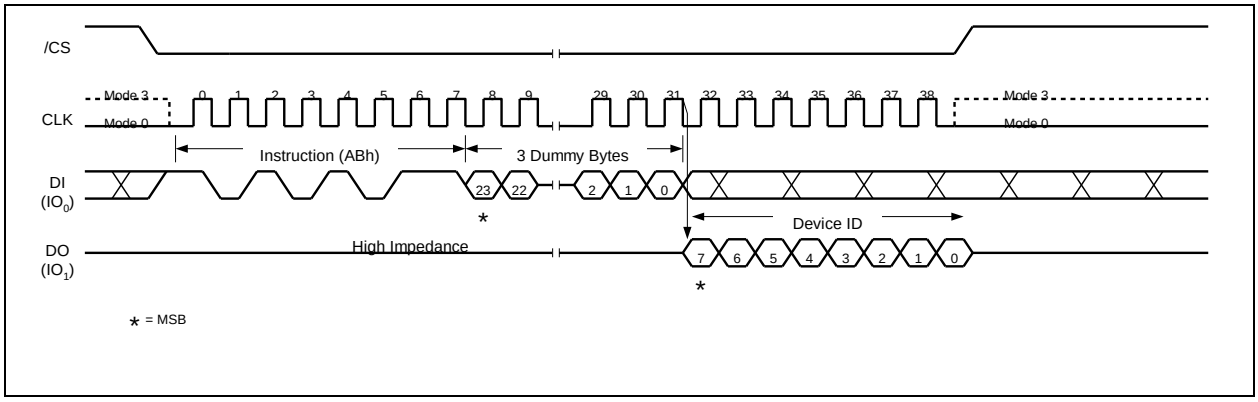


Figure 45c Device ID Instruction (SPI Mode)

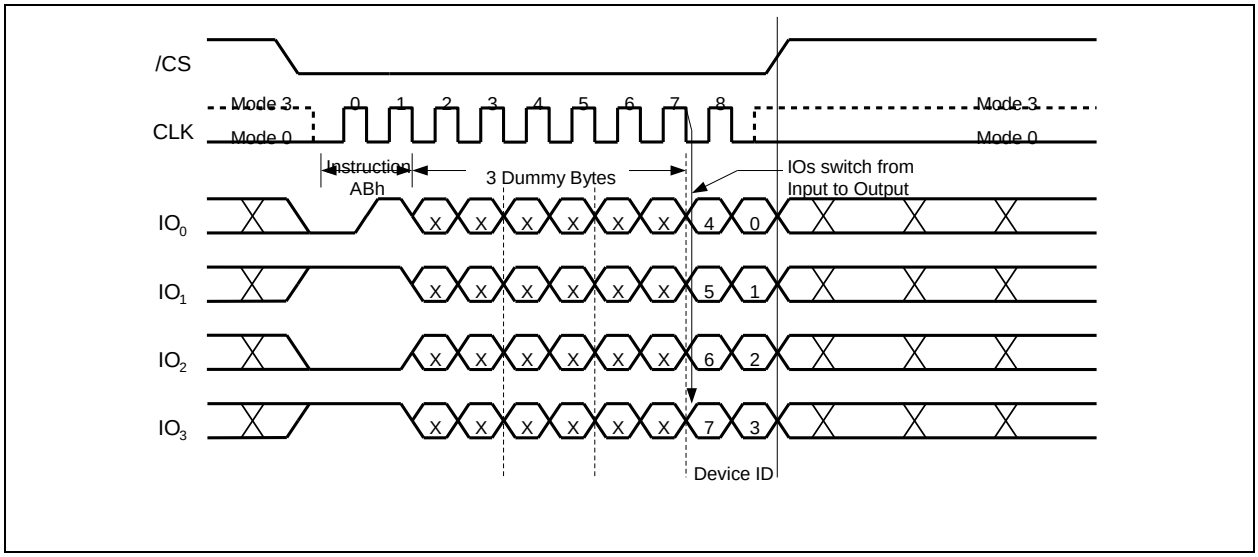


Figure 45d. Device ID Instruction (QPI Mode)

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8.6.14 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 46. The Device ID values for the W25Q01JV are listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

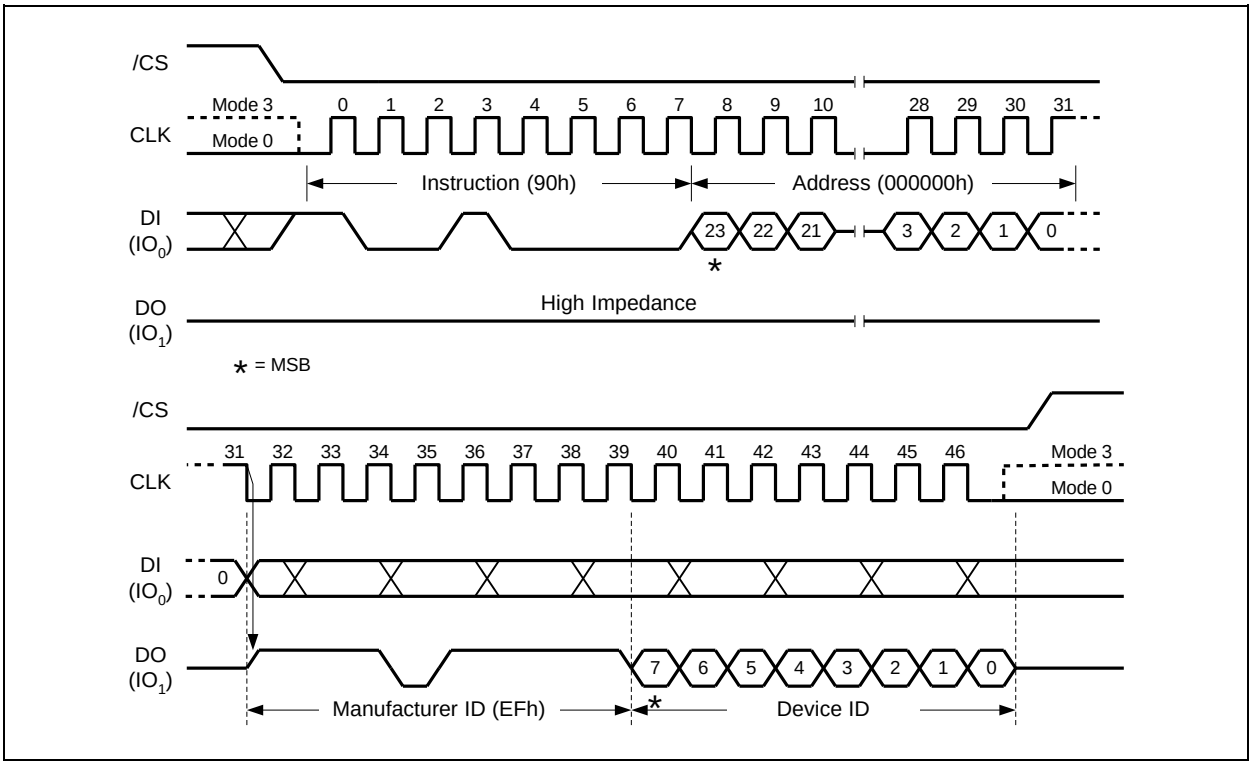


Figure 46. Read Manufacturer / Device ID Instruction (SPI Mode)

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8.6.15 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24/32-bit address (A23/A31-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 47. The Device ID values for the W25Q01JV are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

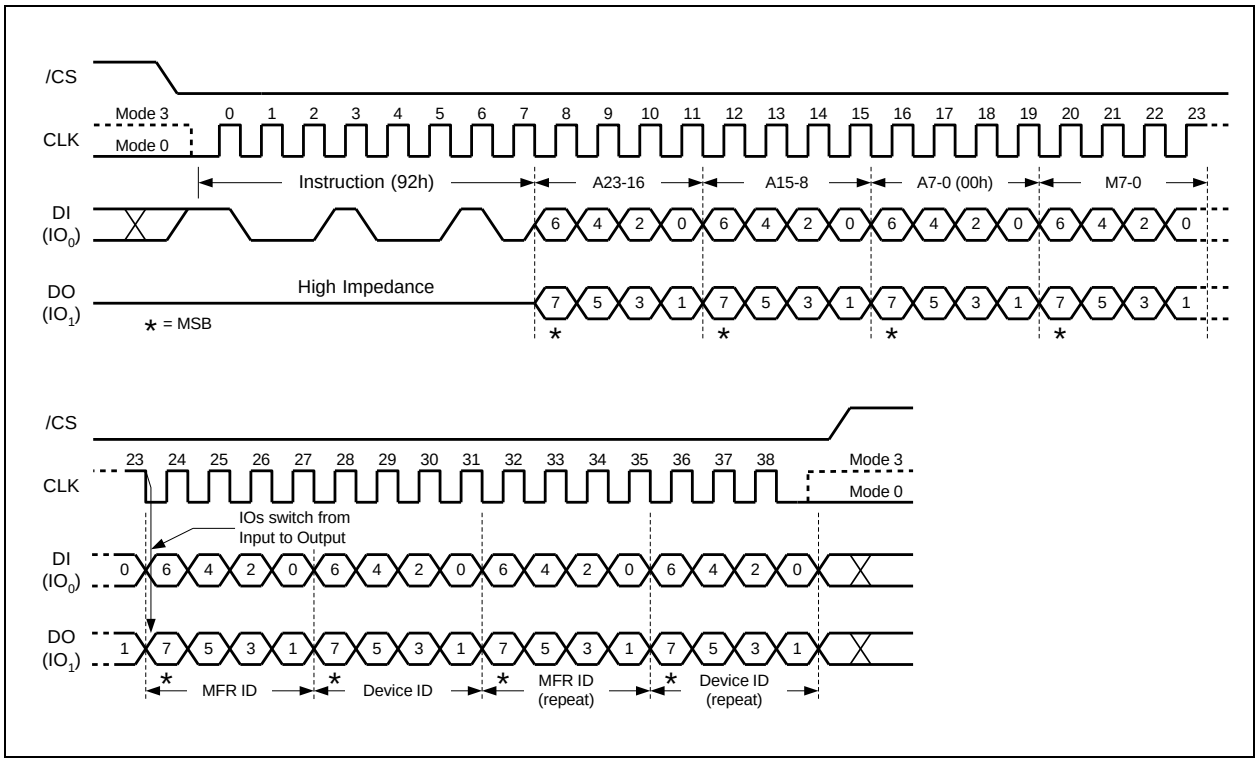


Figure 47. Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

Note:

The Read Command Bypass Mode bits M(7-0) must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

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8.6.16 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “94h” followed by a four clock dummy cycles and then a 24/32-bit address (A23/A31-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 48. The Device ID values for the W25Q01JV are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

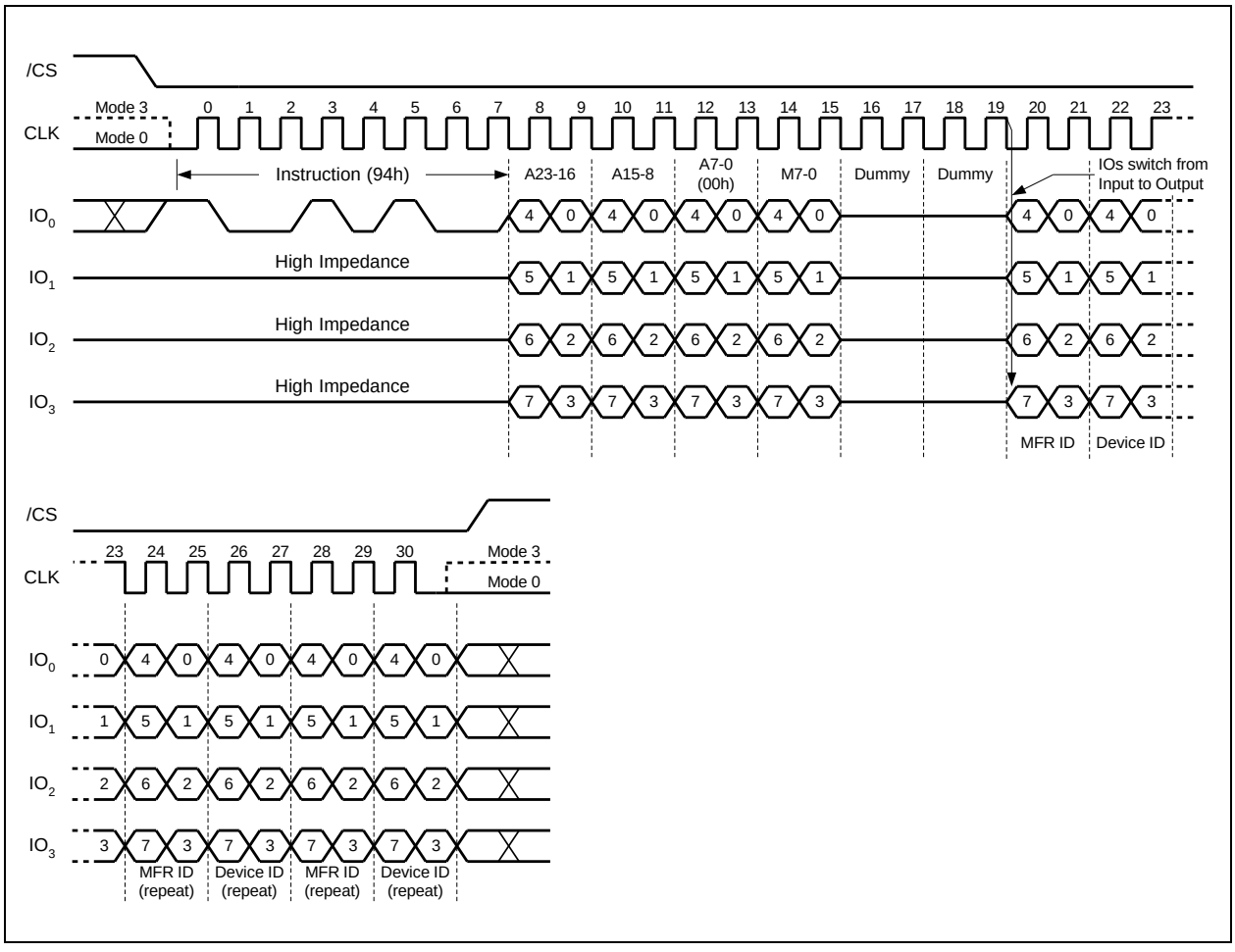


Figure 48. Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

Note:

The Read Command Bypass Mode bits M(7-0) must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

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8.6.17 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each W25Q01JV device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 49.

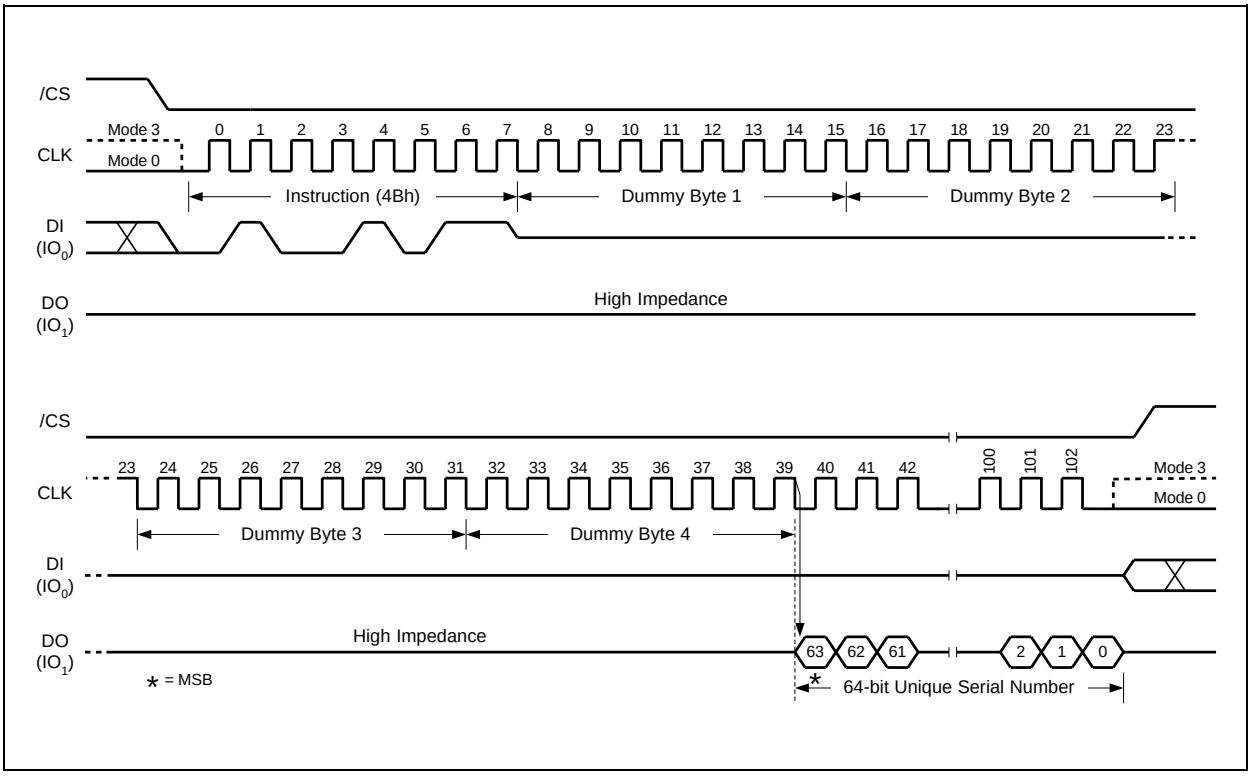


Figure 49. Read Unique ID Number Instruction (SPI Mode only)

5 Dummy Bytes are required when the device is operating in 4-Byte Address Mode

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8.6.18 Read JEDEC ID (9Fh)

For compatibility reasons, the W25Q01JV provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 50a & 50b. For memory type and capacity values refer to Manufacturer and Device Identification table.

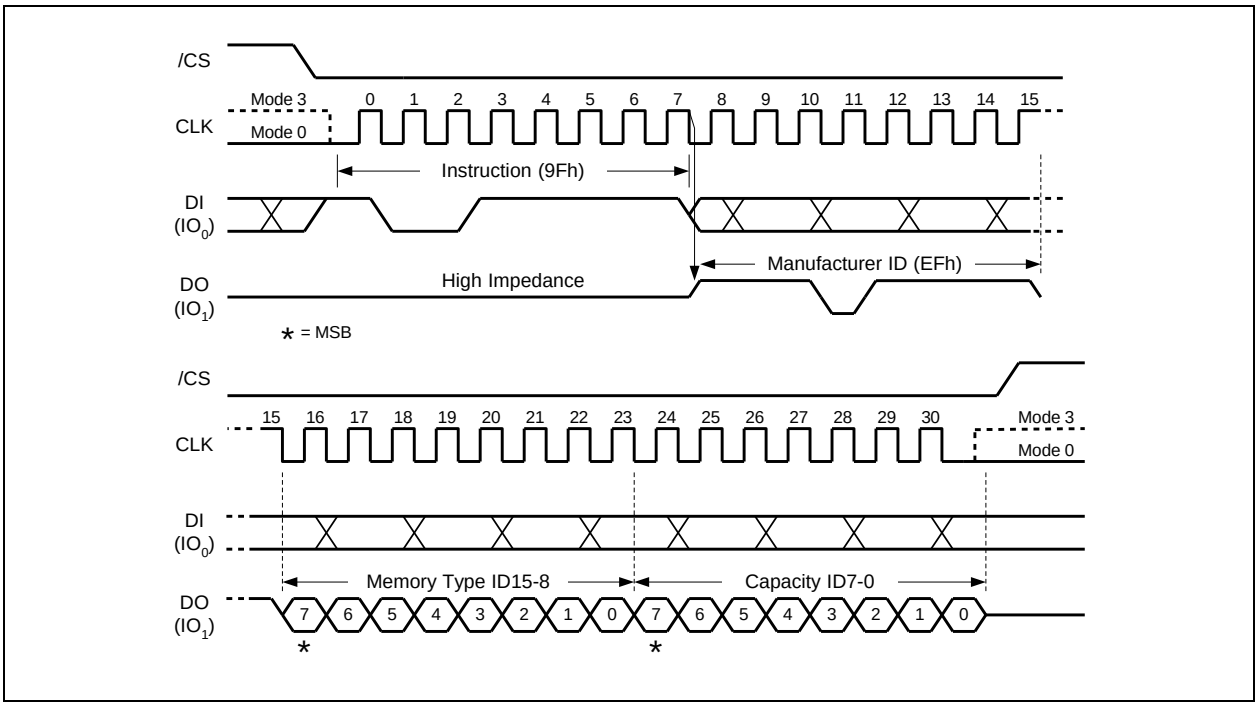


Figure 50a. Read JEDEC ID Instruction (SPI Mode)

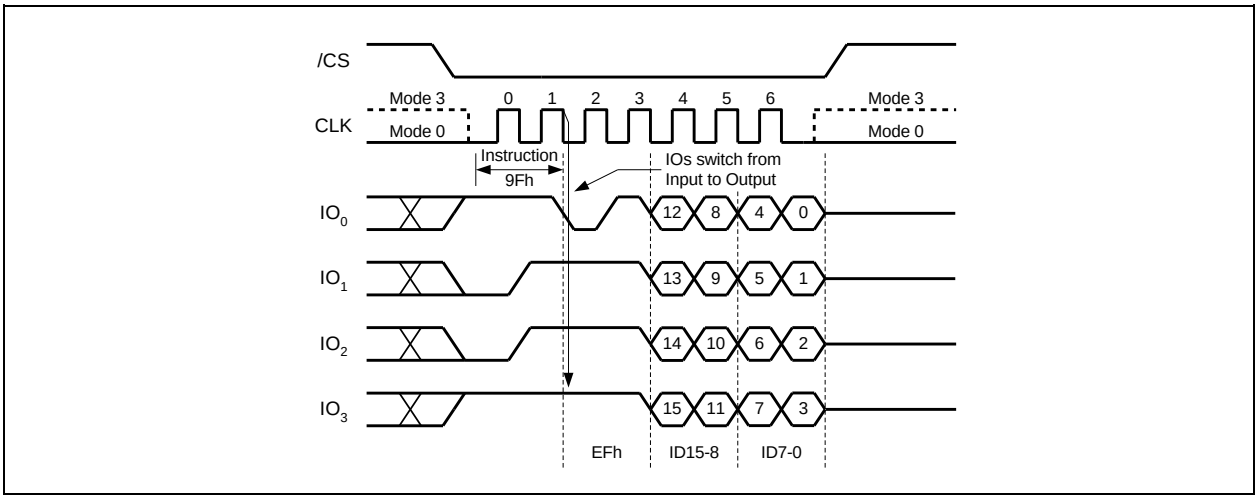


Figure 50b. Read JEDEC ID Instruction (QPI Mode)

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8.6.19 Read SFDP Register (5Ah)

The W25Q01JV features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216-Serials that is published in 2011. Most Winbond SpiFlash Memories shipped after June 2011 (date code 1124 and beyond) support the SFDP feature as specified in the applicable datasheet.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 51. For SFDP register values and descriptions, please refer to the Winbond Application Note for SFDP Definition Table.

Note: 1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

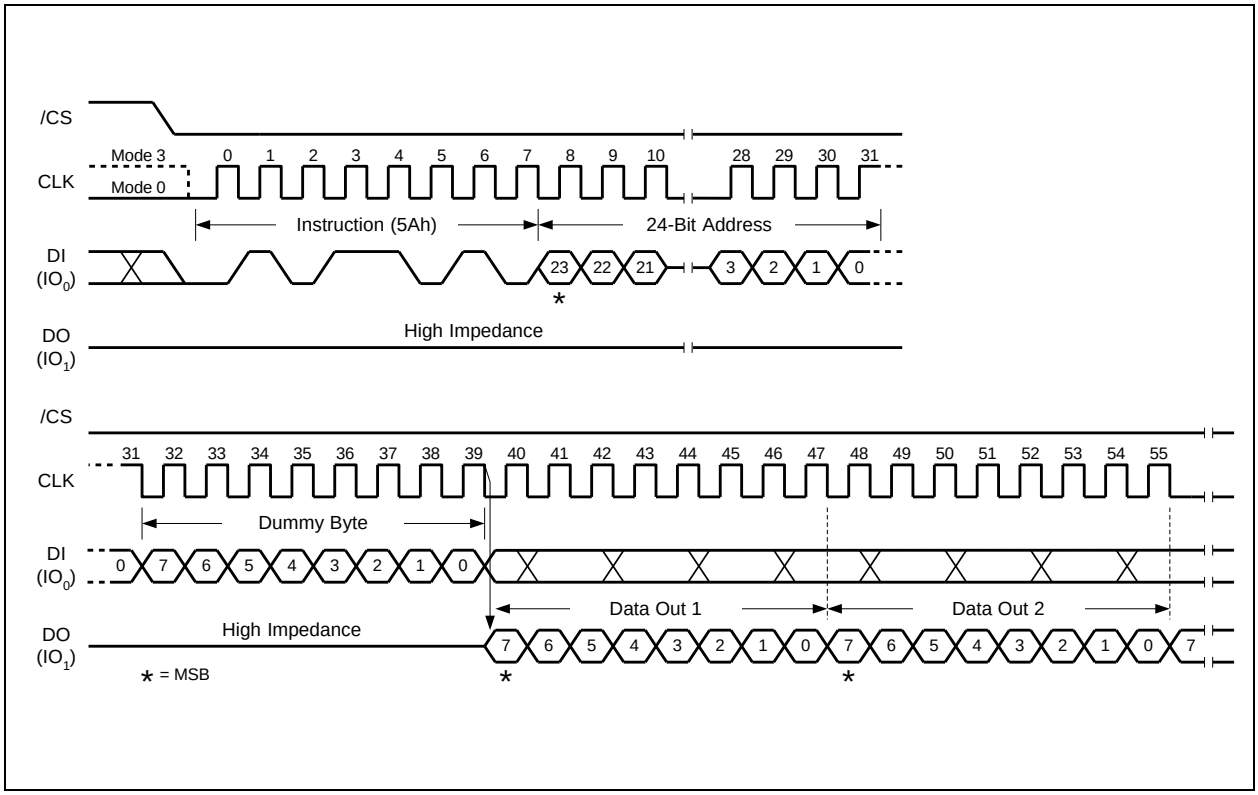


Figure 51. Read SFDP Register Instruction Sequence Diagram

Only 24-Bit Address is required when the device is operating in either 3-Byte or 4-Byte Address Mode

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8.6.20 Erase Security Registers (44h)

The W25Q01JV offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “44h” followed by a 24/32-bit address (A23/A31-A0) to erase one of the three security registers.

ADDRESS	{A23/A31}-16	A15-12	A11-8	A7-0
Security Register #1	00h/0000h	0 0 0 1	0 0 0 0	Don’t Care
Security Register #2	00h/0000h	0 0 1 0	0 0 0 0	Don’t Care
Security Register #3	00h/0000h	0 0 1 1	0 0 0 0	Don’t Care

The Erase Security Register instruction sequence is shown in Figure 52. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of t_{SE} (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB[3:1]) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored (Refer to section 7.1.8 for detail descriptions).

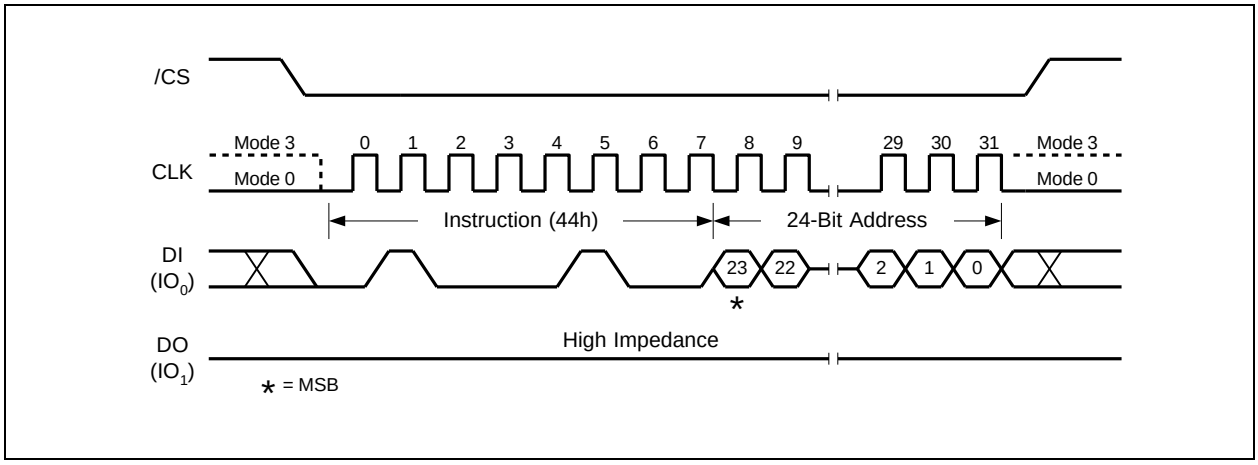


Figure 52. Erase Security Registers Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.21 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24/32-bit address (A23/A31-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	{A23/A31}-16	A15-12	A11-8	A7-0
Security Register #1	00h/0000h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h/0000h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h/0000h	0 0 1 1	0 0 0 0	Byte Address

The Program Security Register instruction sequence is shown in Figure 52. The Security Register Lock Bits (LB[3:1]) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See 7.1.8 for detail descriptions).

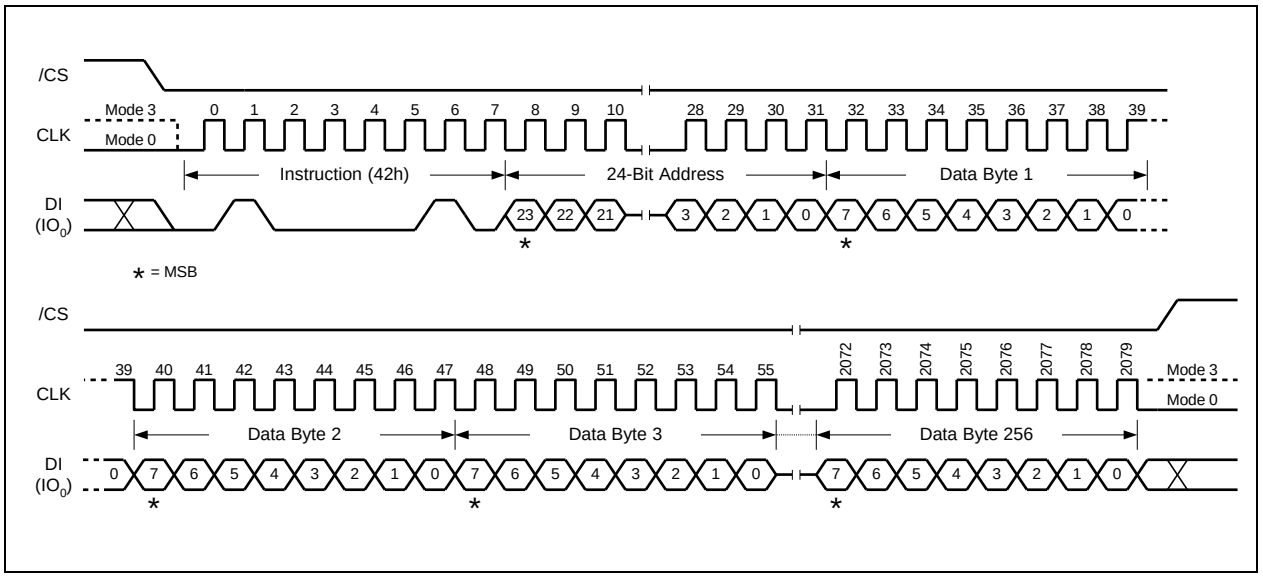


Figure 52. Program Security Registers Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.22 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the three security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24/32-bit address (A23/A31-A0) and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 53. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

ADDRESS	{A23/A31}-16	A15-12	A11-8	A7-0
Security Register #1	00h/0000h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h/0000h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h/0000h	0 0 1 1	0 0 0 0	Byte Address

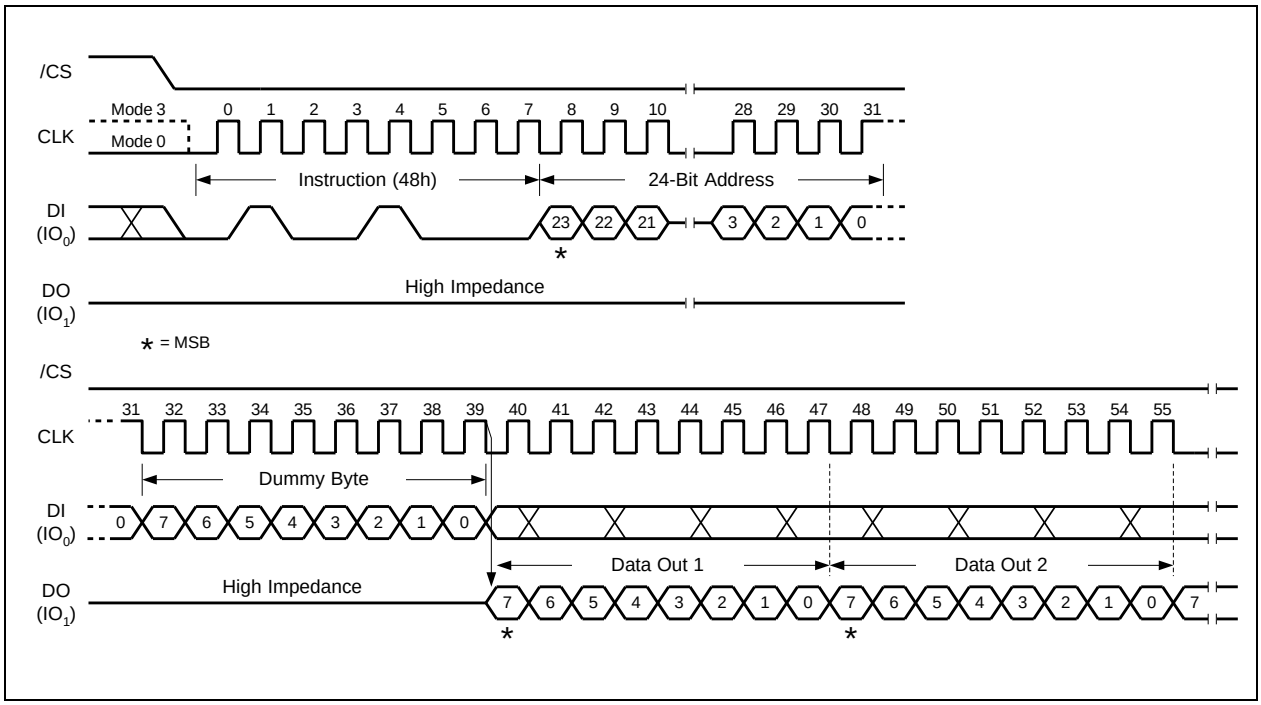


Figure 53. Read Security Registers Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.23 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of dummy clocks for “Fast Read (0Bh)”, “Fast Read Quad I/O (EBh)” & “Burst Read with Wrap (0Ch)” instructions, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0Ch)” instruction.

In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, please refer to the Instruction Table 1-4 & 7-8 for details. The “Wrap Length” is set by W5-4 bit in the “Set Burst with Wrap (77h)” instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 4. The number of dummy clocks is only programmable for “Fast Read (0Bh)”, “Fast Read Quad I/O (EBh)” & “Burst Read with Wrap (0Ch)” instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again, prior to any 0Bh, EBh or 0Ch instructions.

QPI P6-P4	DUMMY CLOCKS	MAXIMUM READ FREQ. 2.7~3.0 /3.0~3.6
0 0 0	2	33/33MHz
0 0 1	4	50/50MHz
0 1 0	6	80/104MHz
0 1 1	8	104/133MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

Note:4-bytes address alignment for Read: read address start from A1,A0=0,0

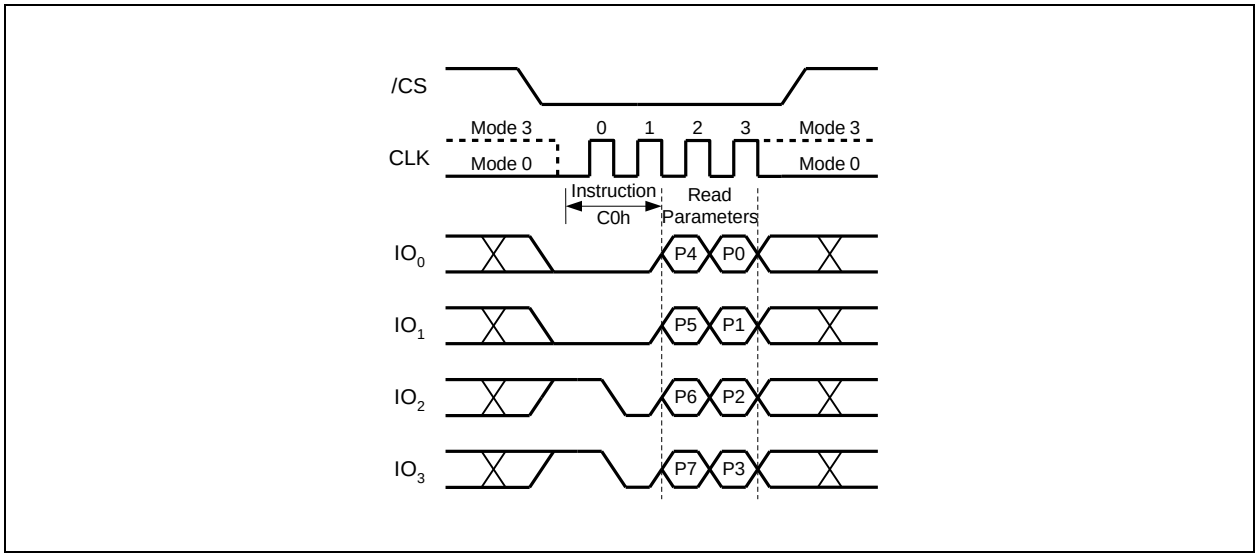


Figure 54. Set Read Parameters Instruction (QPI Mode only)

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8.6.24 Burst Read with Wrap (0Ch)

The “Burst Read with Wrap (0Ch)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” instruction.

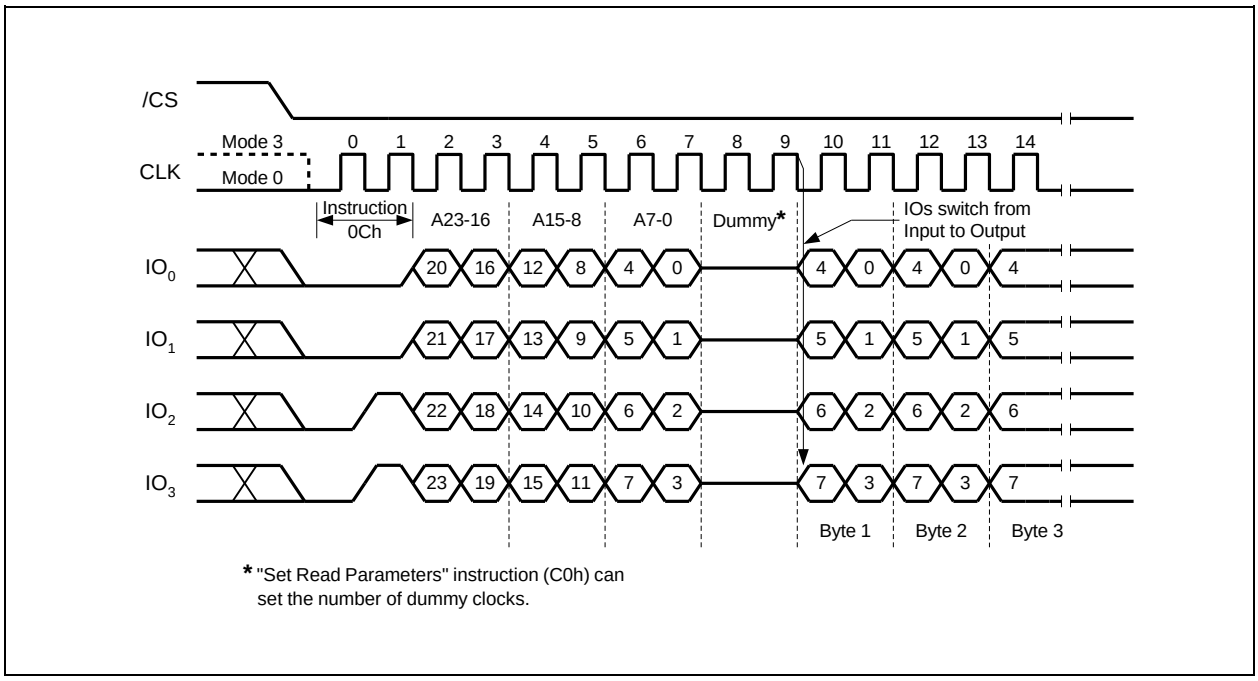


Figure 55. Burst Read with Wrap Instruction (QPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.25 DTR Burst Read with Wrap (0Eh)

The “DTR Burst Read with Wrap (0Eh)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” can be configured by the “Set Read Parameters (C0h)” instruction.

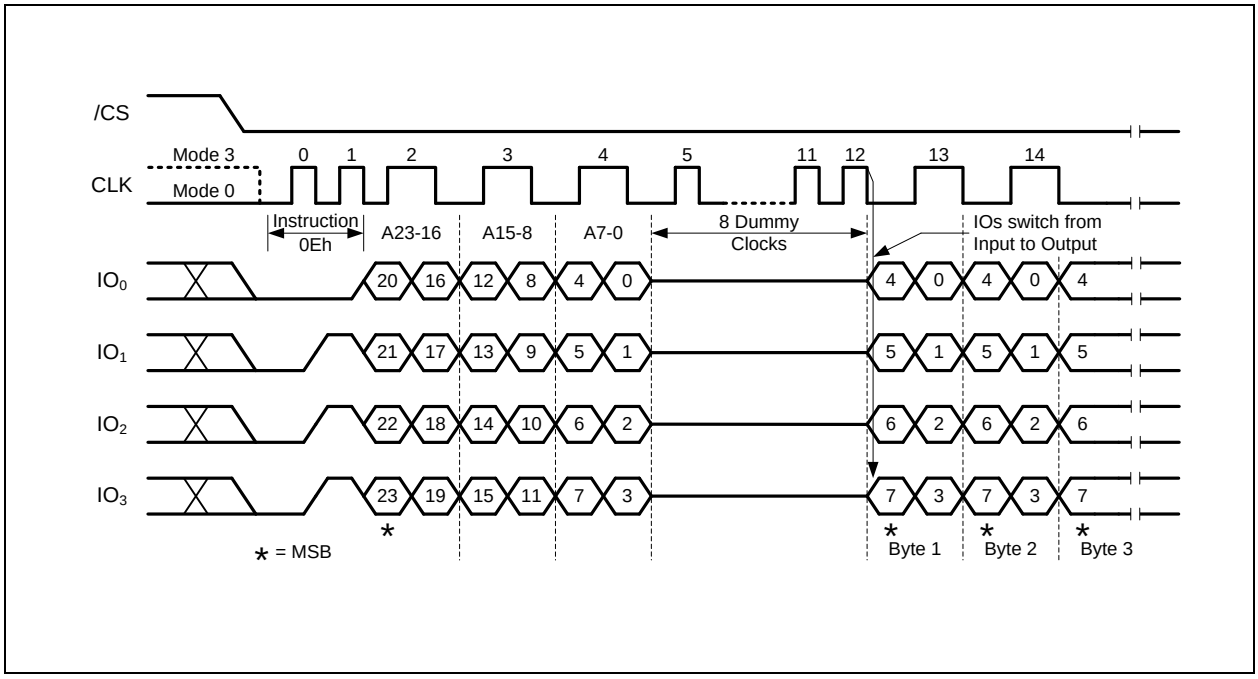


Figure 56. DTR Burst Read with Wrap Instruction (QPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.26 Enter QPI Mode (38h)

The W25Q01JV support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of Winbond serial flash memories. See Instruction Set Table 1-4 & 7-8 for all supported SPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored and the device will remain in SPI mode.

See Instruction Set Table 5-6 & 9-10 for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

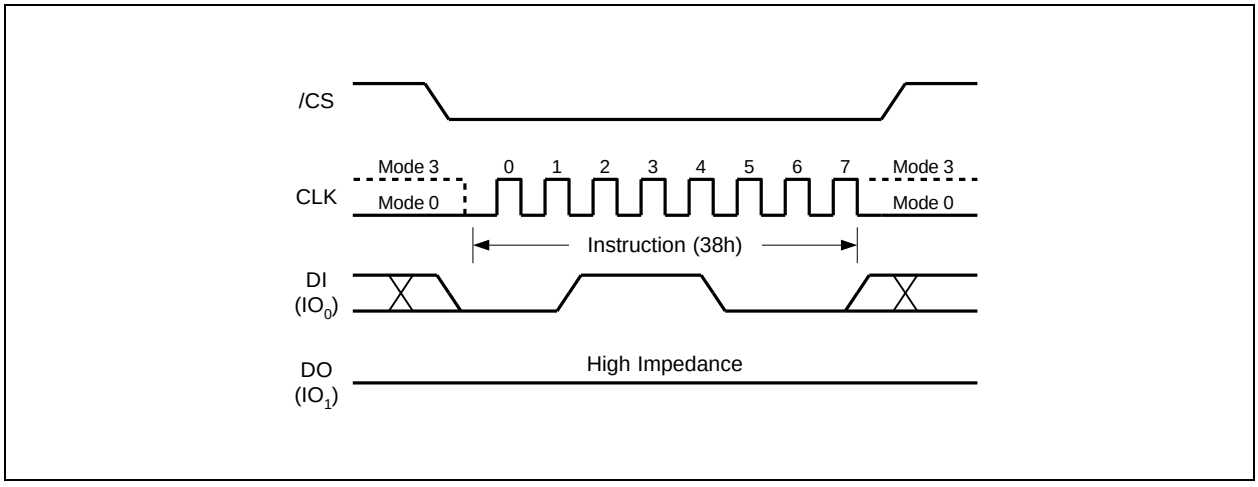


Figure 57. Enter QPI Instruction (SPI Mode only)

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8.6.27 Exit QPI Mode (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

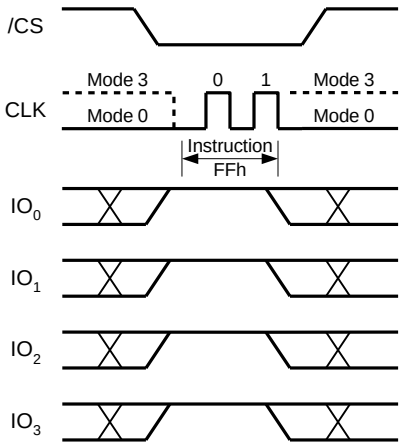


Figure 58. Exit QPI Instruction (QPI Mode only)

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8.6.28 Individual Block/Sector Lock (36h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, TB, BP[3:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

To lock a specific block or sector as illustrated in Figure 4d, an Individual Block/Sector Lock command must be issued by driving /CS low, shifting the instruction code “36h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24/32-bit address and then driving /CS high.

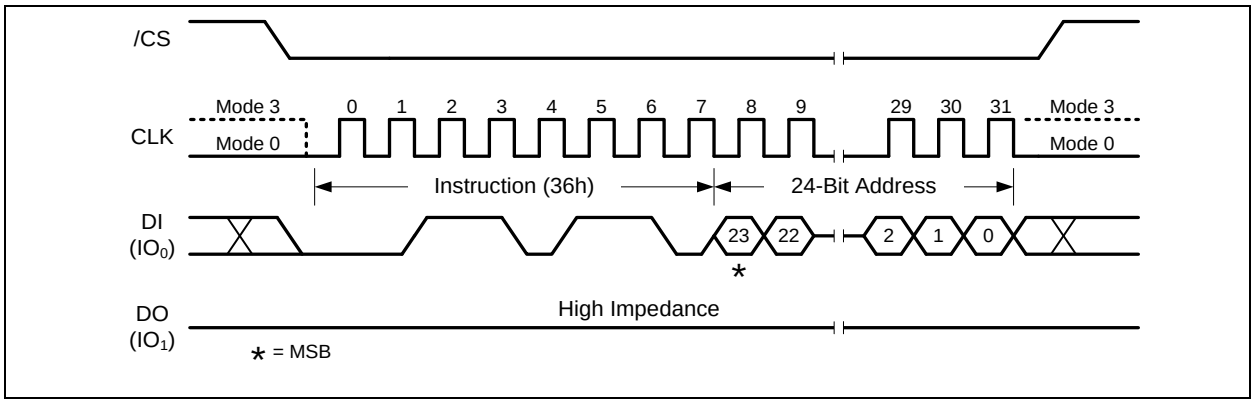


Figure 59a. Individual Block/Sector Lock Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

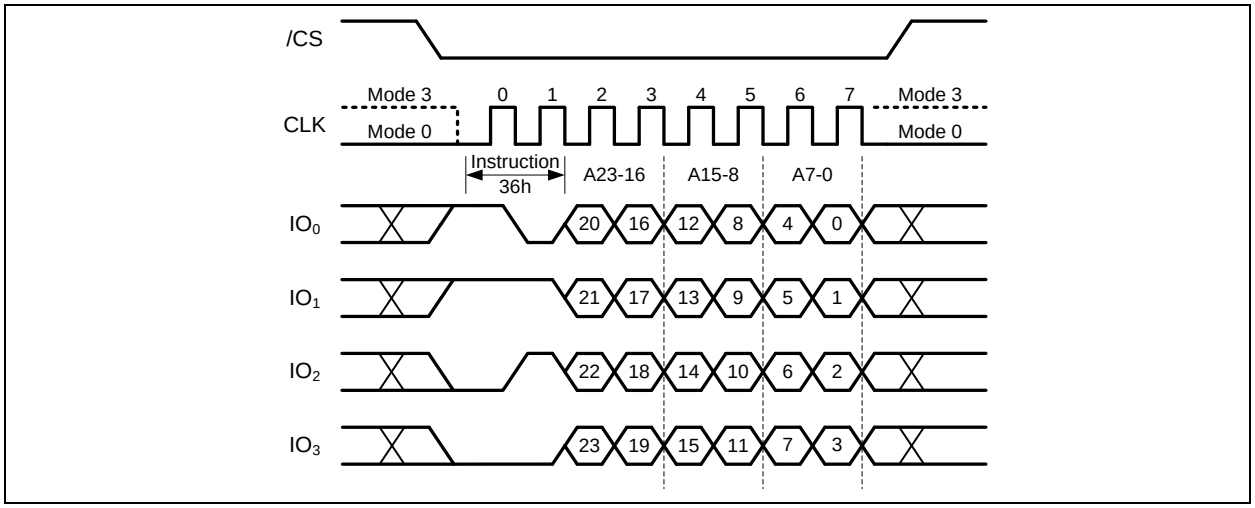


Figure 59b. Individual Block/Sector Lock Instruction (QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.29 Individual Block/Sector Unlock (39h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, TB, BP[3:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

To unlock a specific block or sector as illustrated in Figure 4d, an Individual Block/Sector Unlock command must be issued by driving /CS low, shifting the instruction code “39h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24/32-bit address and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Individual Block/Sector Unlock Instruction (Status Register bit WEL= 1).

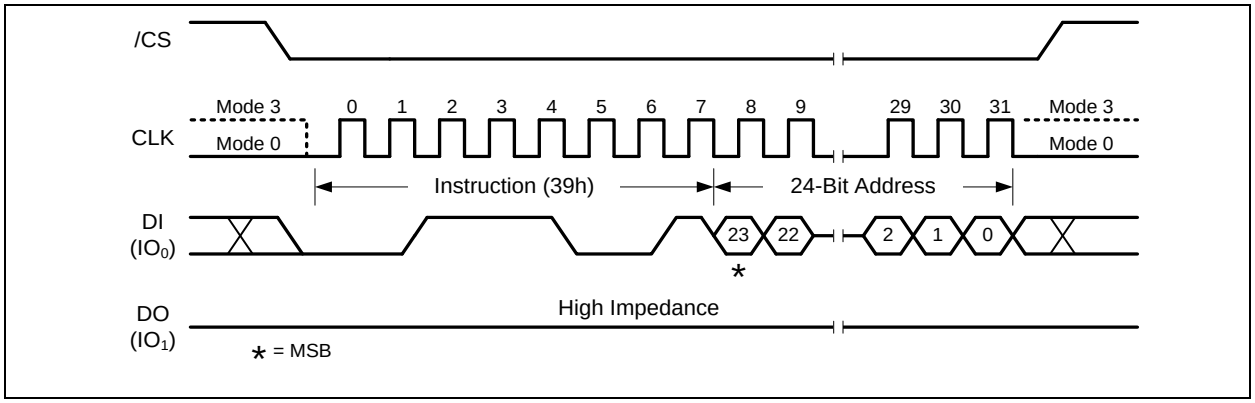


Figure 60a. Individual Block Unlock Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

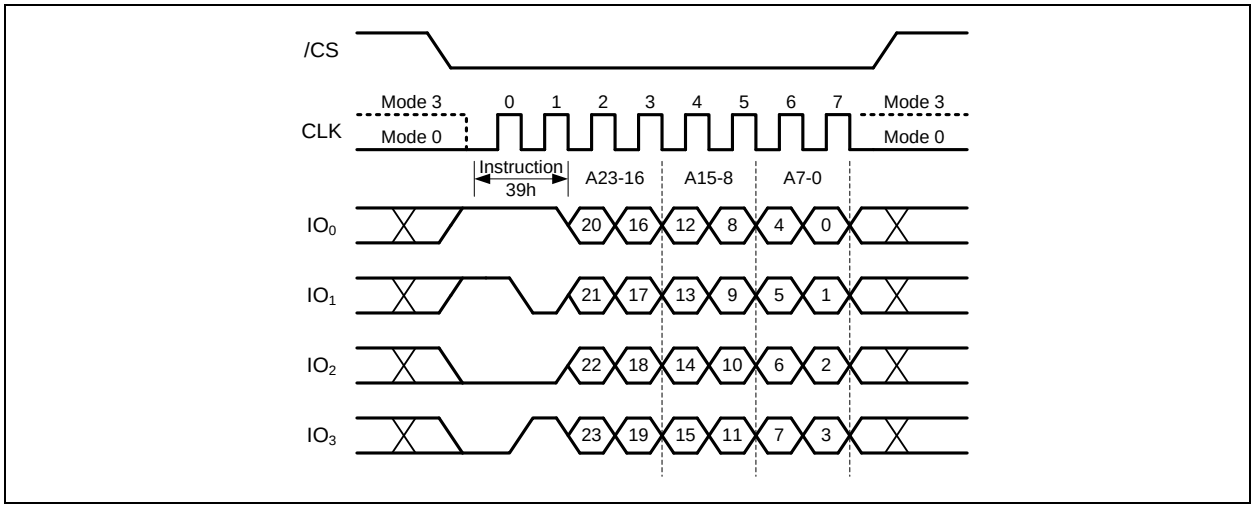


Figure 60b. Individual Block Unlock Instruction (QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.30 Read Block/Sector Lock (3Dh)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, TB, BP[3:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

To read out the lock bit value of a specific block or sector as illustrated in Figure 4d, a Read Block/Sector Lock command must be issued by driving /CS low, shifting the instruction code “3Dh” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24/32-bit address. The Block/Sector Lock bit value will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 54. If the least significant bit (LSB) is 1, the corresponding block/sector is locked; if LSB=0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.

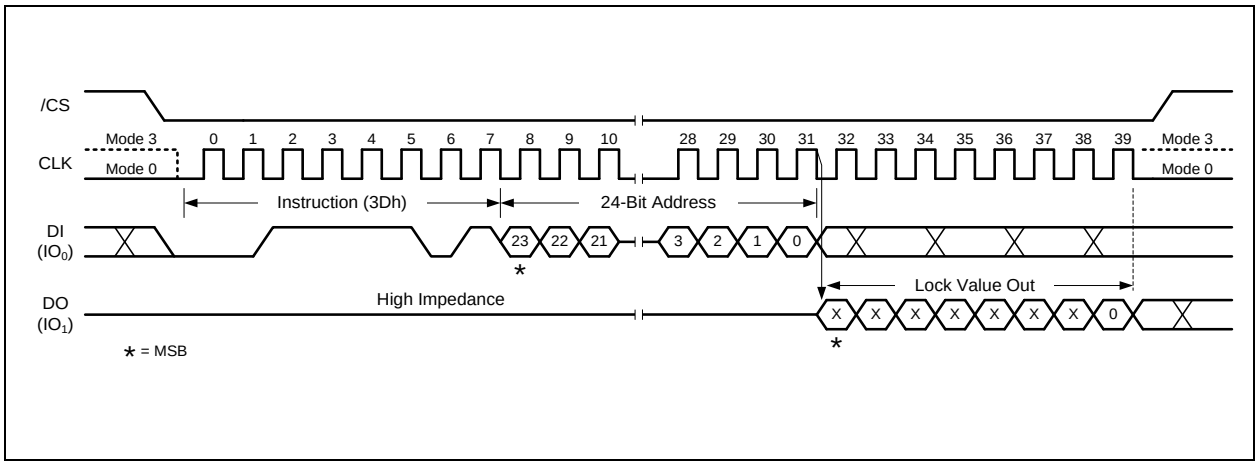


Figure 61a. Read Block Lock Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

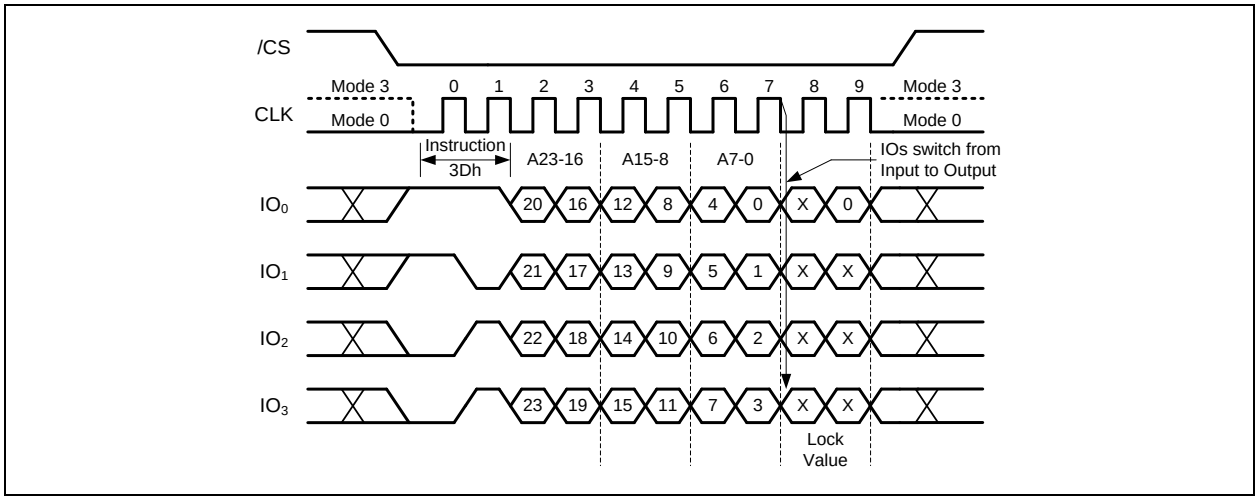


Figure 61b. Read Block Lock Instruction (QPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

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8.6.31 Global Block/Sector Lock (7Eh)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock instruction. The command must be issued by driving /CS low, shifting the instruction code “7Eh” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Global Block/Sector Lock Instruction (Status Register bit WEL= 1).

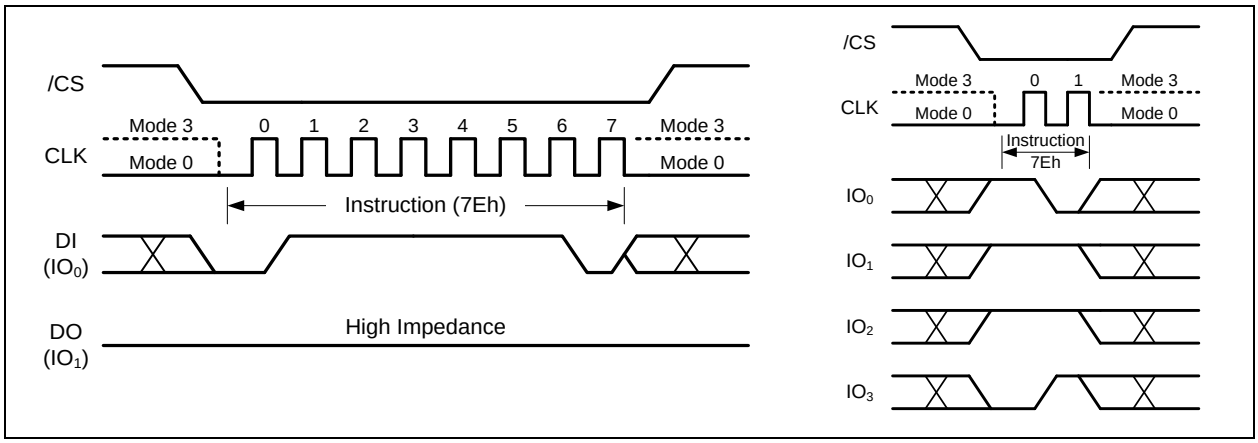


Figure 62. Global Block Lock Instruction for SPI Mode (left) or QPI Mode (right)

8.6.32 Global Block/Sector Unlock (98h)

All Block/Sector Lock bits can be set to 0 by the Global Block/Sector Unlock instruction. The command must be issued by driving /CS low, shifting the instruction code “98h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Global Block/Sector Unlock Instruction (Status Register bit WEL= 1).

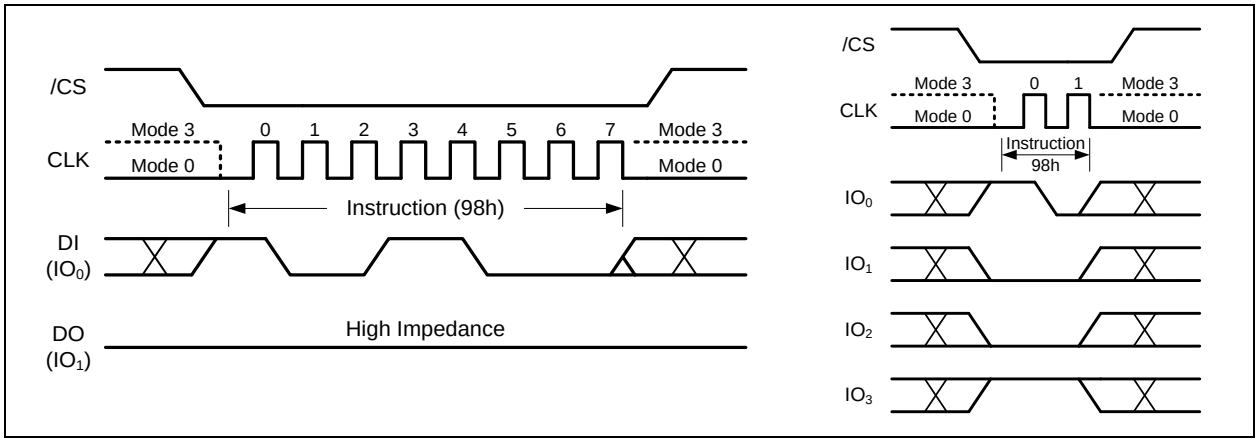


Figure 63. Global Block Unlock Instruction for SPI Mode (left) or QPI Mode (right)

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8.6.33 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the W25Q01JV provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), setting (M7-M0) and Wrap Bit setting (W6-W4).

“Enable Reset (66h)” and “Reset (99h)” instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

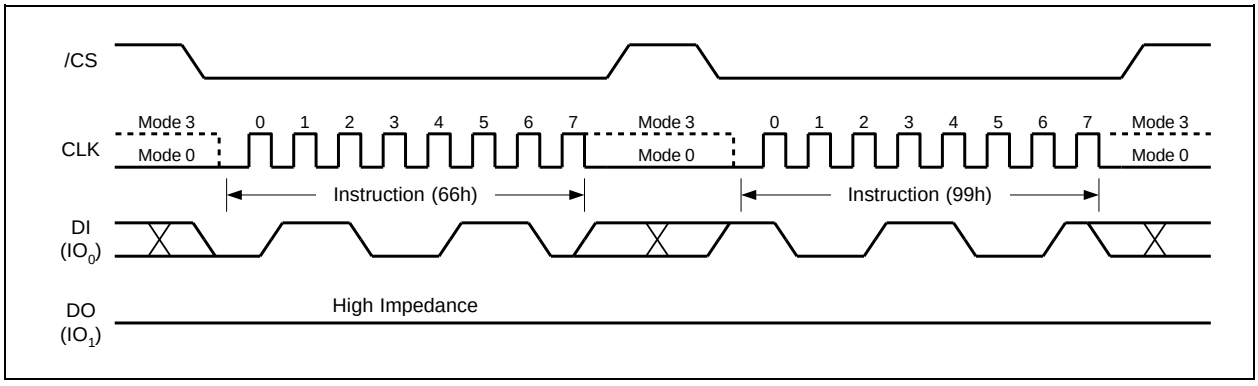


Figure 64a. Enable Reset and Reset Instruction Sequence (SPI Mode)

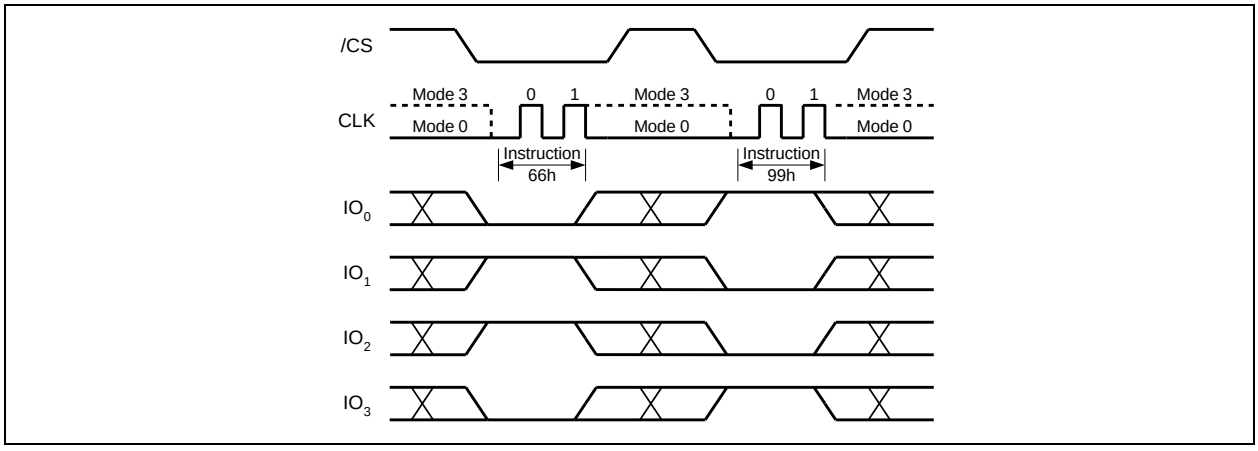


Figure 64b. Enable Reset and Reset Instruction Sequence (QPI Mode)

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9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings (1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +4.6V	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0 to VCC+2.0	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	F_R = 133MHz, f_R = 50MHz	3.0	3.6	V
		F_R = 104MHz, f_R = 50MHz	2.7	3.0	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C

Note:

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

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9.3 Power-up Power-down Timing and Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}(1)	20		µs
Time Delay Before Write Instruction	t_{PUW}(1)	5		ms
Write Inhibit Threshold Voltage	V_{WI}(1)	1.0	1.4	V

Note:

1. These parameters are characterized only.

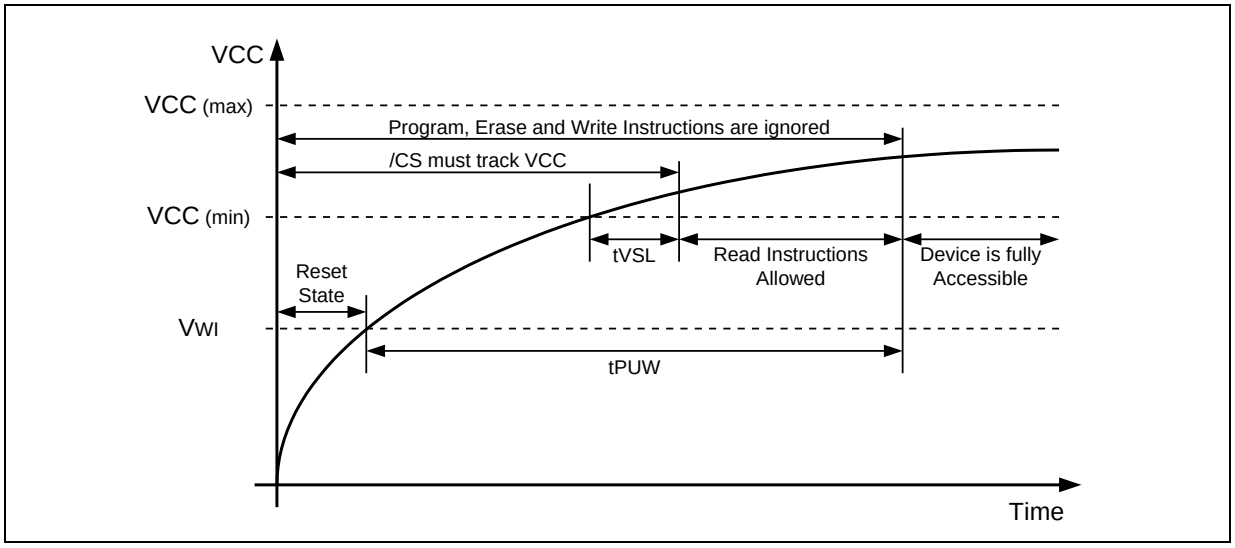


Figure 65a. Power-up Timing and Voltage Levels

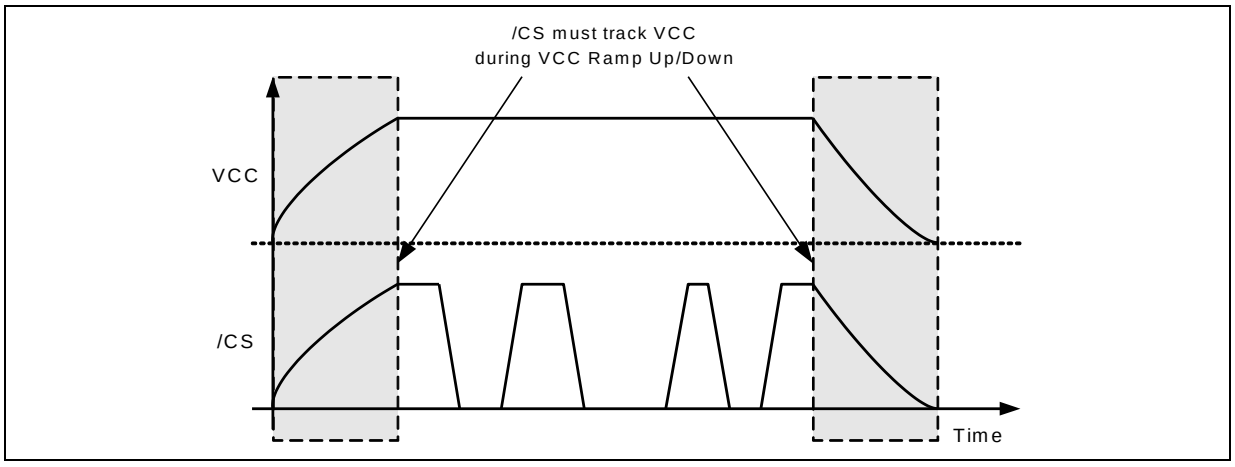


Figure 65b. Power-up, Power-Down Requirement

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9.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V			12	pF
Output Capacitance	Cout(1)	V_{OUT} = 0V			16	pF
Input Leakage	I_{LI}				±4	µA
I/O Leakage	I_{LO}				±4	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		10	170	µA
Power-down Current	I_{CC2}	/CS = VCC, VIN = GND or VCC		1	40	µA
Current Read Data / Dual /Quad 50MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open			70	mA
Current Read Data / Dual Output Read/Quad Output Read 104MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open			80	mA
Current Read Data / Dual Output Read/Quad Output Read 133MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open			100	mA
Current Write Status Register	I_{CC4}	/CS = VCC		20	25	mA
Current Page Program	I_{CC5}	/CS = VCC		20	25	mA
Current Sector/Block Erase	I_{CC6}	/CS = VCC		20	25	mA
Current Chip Erase	I_{CC7}	/CS = VCC		20	50	mA
Input Low Voltage	V_{IL}		–0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC – 0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.
2. Checker Board Pattern.

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9.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

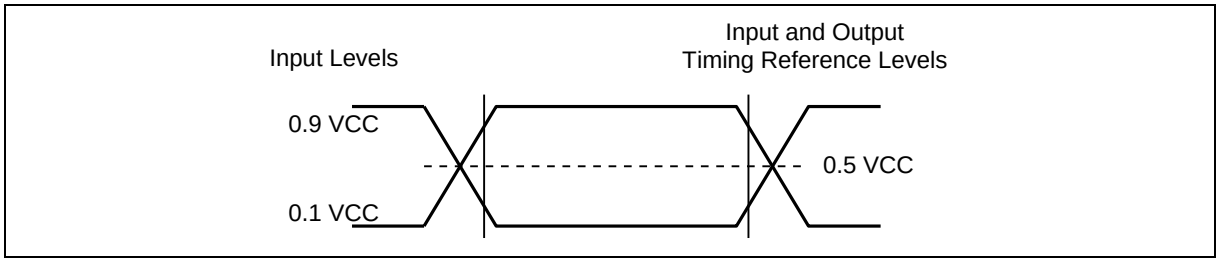


Figure 66. AC Measurement I/O Waveform

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9.6 AC Electrical Characteristics(6)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency except for BBh/BCh & DTR & Read Data (03h/13h) instructions (3.0V-3.6V)	F_R(6)	f_{C1}	D.C.		133	MHz
Clock frequency except for BBh/BCh & DTR & Read Data (03h/13h) instructions(2.7V-3.0V)	F_R	f_{C1}	D.C.		104	MHz
Clock frequency for BBh/BCh instructions (2.7V-3.6V)	F_R(6)	f_{C1}	D.C.		90	MHz
Clock frequency for DTR instructions except for BDh (3.0V-3.6V)	F_R		D.C		80	MHz
Clock frequency for DTR instructions (2.7V-3.6V)	F_R		D.C		66	MHz
Clock frequency for Read Data instruction (03h/13h)	f_R		D.C.		50	MHz
Clock High, Low Time for all instructions	t_{CLH}/ t_{CLL}(1)		45%PC			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Active Setup Time relative to CLK (DTR)	t_{SLCH1}	t_{CSS1}	10			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
/CS Deselect Time (During Read)	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (During Erase or Program or Write)	t_{SHSL2}	t_{CSH}	50			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			10	ns
Clock Low to Output Valid	t_{CLQV1}	t_{V1}			7.5	ns
Output Hold Time	t_{CLQX}	t_{HO}	1.5			ns

Continued – next page

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AC Electrical Characteristics (cont'd)

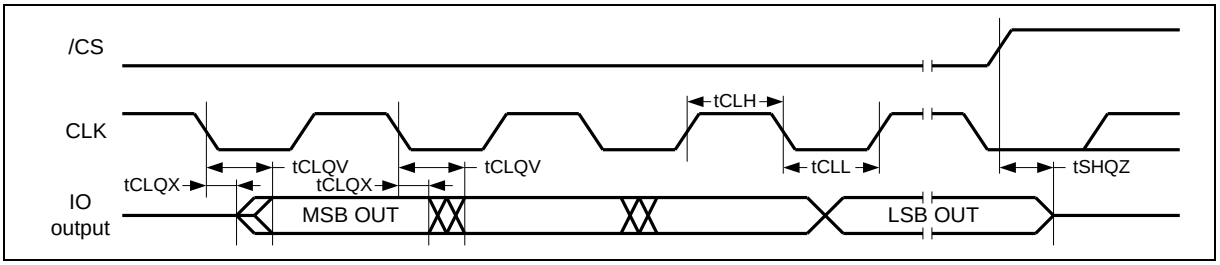
DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Active Setup Time relative to CLK	t_{HLCH}		5			ns
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	t_{HHQX}(2)	t_{LZ}			8	ns
/HOLD to Output High-Z	t_{HLQZ}(2)	t_{HZ}			12	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}(3)		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}(3)		100			ns
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without ID Read	t_{RES1}(2)				3	µs
/CS High to Standby Mode with ID Read	t_{RES2}(2)				1.8	µs
/CS High to next Instruction after Suspend	t_{SUS}(2)				20	µs
/CS High to next Instruction after Reset	t_{RST}(2)				30	µs
/RESET pin Low period to reset the device	t_{RESET}(2)		1(4)			µs
Write Status Register Time	t_W			10	15	ms
Page Program Time	t_{PP}			0.7	3.5	ms
Sector Erase Time (4KB)	t_{SE}			50	400	ms
Block Erase Time (32KB)	t_{BE1}			120	1,600	ms
Block Erase Time (64KB)	t_{BE2}			150	2,000	ms
Chip Erase Time	t_{CE}			200	1000	s

Notes:

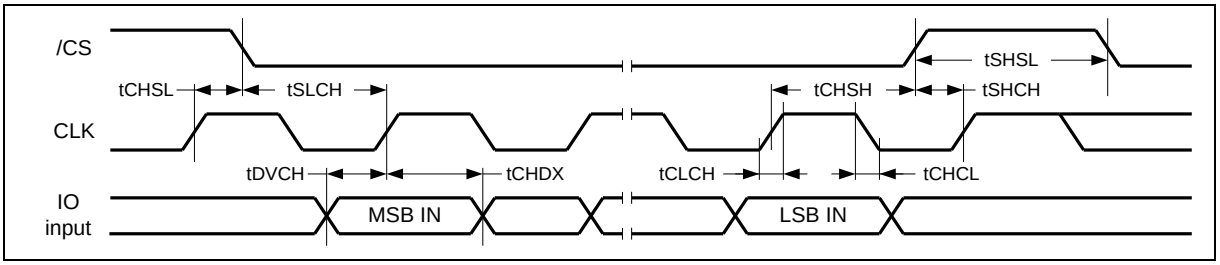
1. Clock high + Clock low must be less than or equal to Pc. Pc = 1/fc(max.)
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP=1.
4. It is possible to reset the device with shorter tRESET (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.
5. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V
6. 4-bytes address alignment for Read: read address start from A1,A0=0,0

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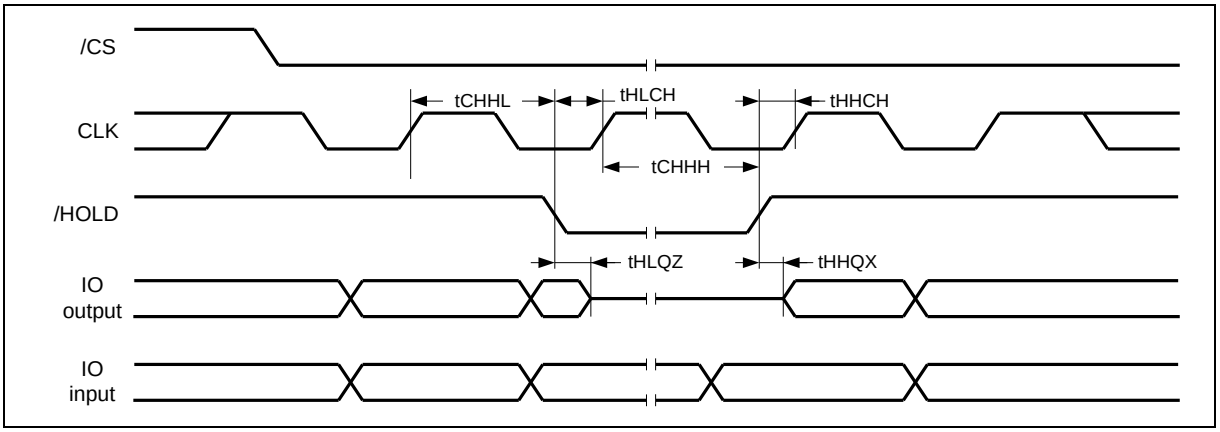
9.7 Serial Output Timing



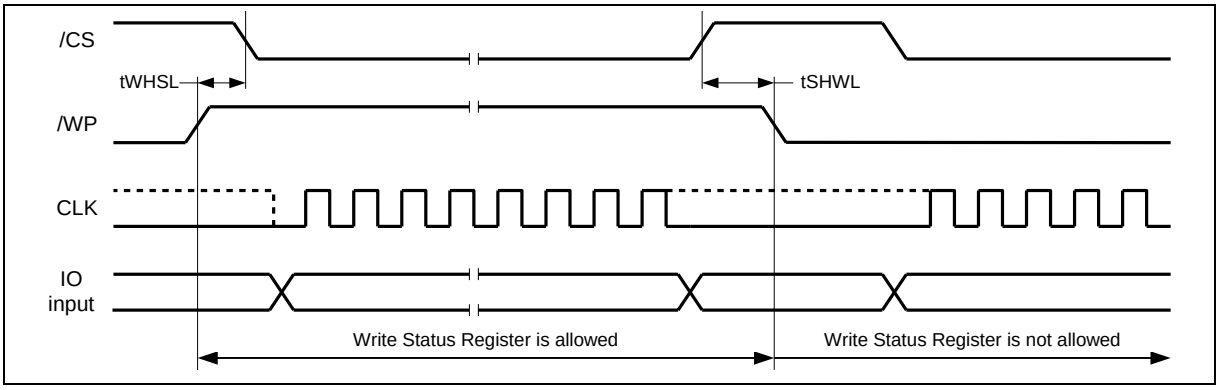
9.8 Serial Input Timing



9.9 /HOLD Timing



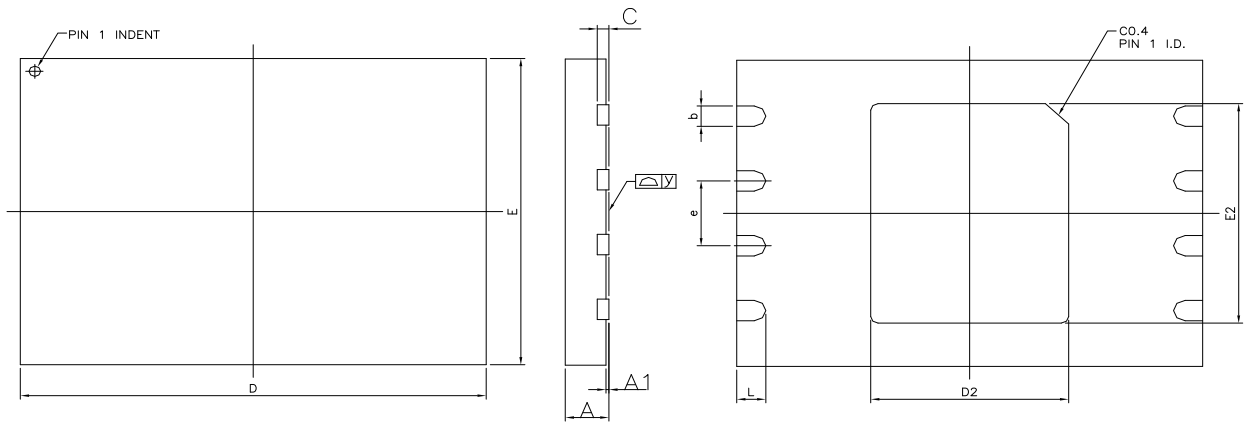
9.10 /WP Timing



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10. PACKAGE SPECIFICATIONS

10.1 8-Pad WSON 8x6-mm (Package Code ZE)



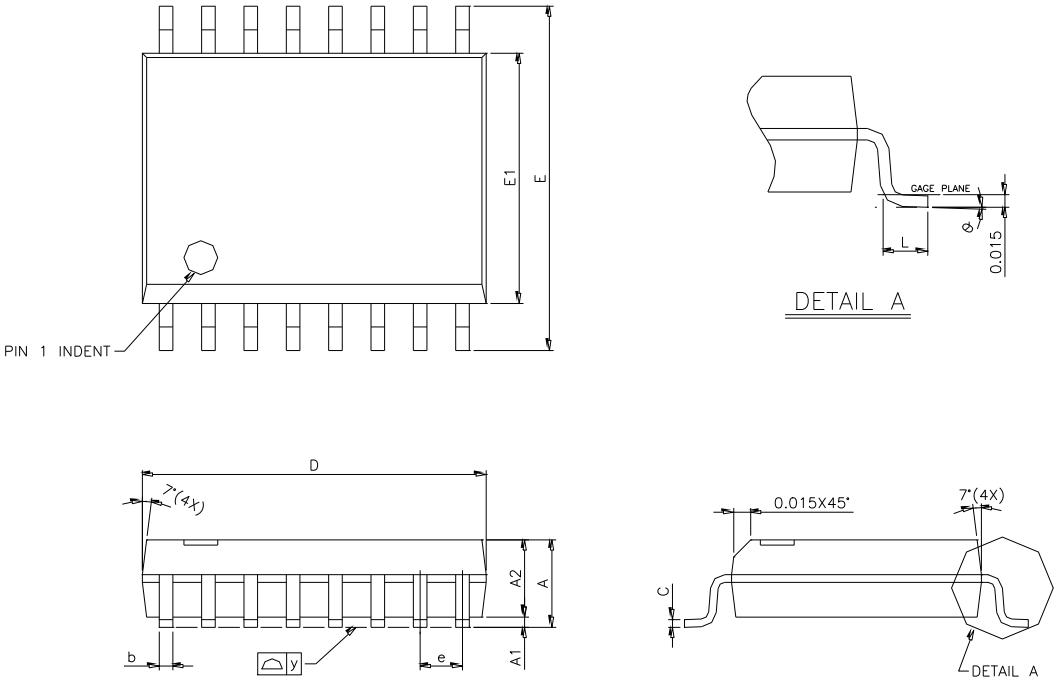
SYMBOL	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 Ref.	---	---	0.008 Ref.	---
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	5.90	6.00	6.10	0.232	0.236	0.240
E2	4.25	4.30	4.35	0.167	0.169	0.171
e	1.27 BSC			0.050 BSC		
L	0.45	0.50	0.55	0.018	0.020	0.022
y	0.00	---	0.05	0.000	---	0.002

Note:

The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.

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10.2 16-Pin SOIC 300-mil (Package Code SF)

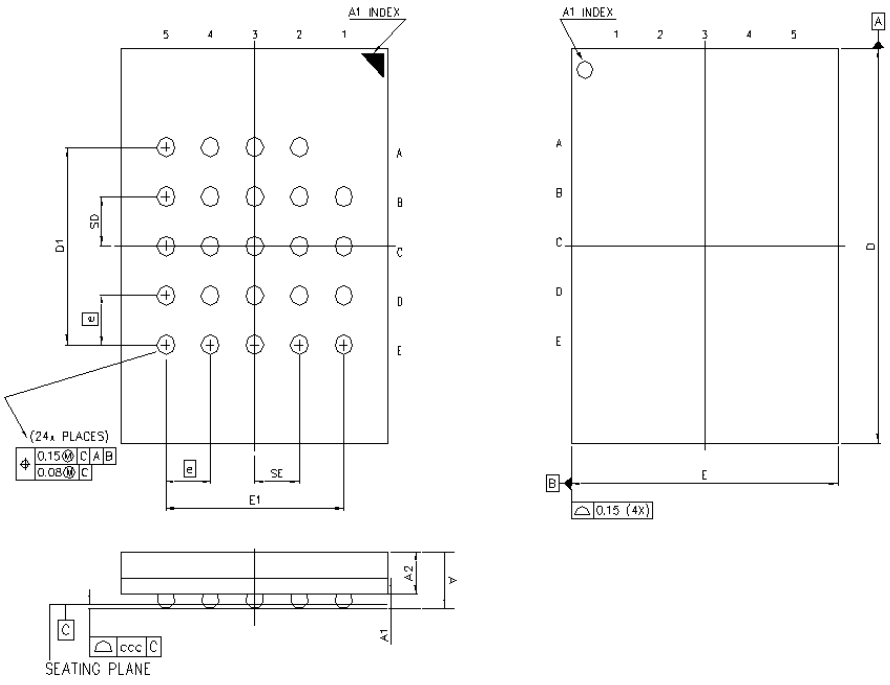


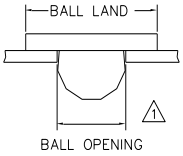
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	---	0.30	0.004	---	0.012
A2	---	2.31	---	---	0.091	---
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	10.08	10.31	10.49	0.397	0.406	0.413
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	1.27 BSC			0.050 BSC		
L	0.38	0.81	1.27	0.015	0.032	0.050
y	---	---	0.076	---	---	0.003
θ	0°	---	8°	0°	---	8°

Note: Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)

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10.3 24-Ball TFBGA 8x6-mm (Package Code TB, 5x5-1 Ball Array)





Note:

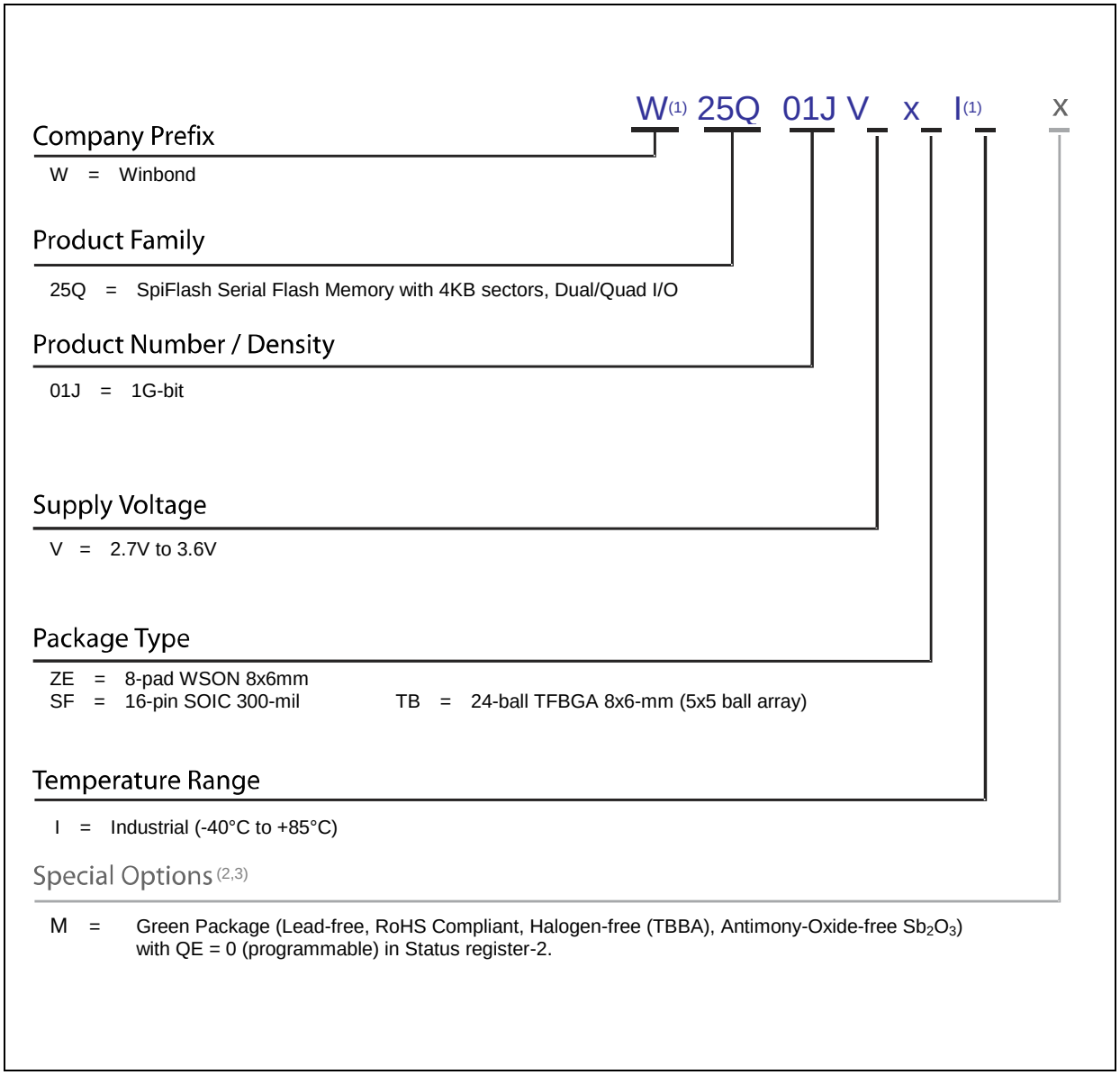
Ball land: 0.45mm. Ball Opening: 0.35mm

PCB ball land suggested <= 0.35mm

Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.20	---	---	0.047
A1	0.26	0.31	0.36	0.010	0.012	0.014
A2	---	0.85	---	---	0.033	---
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1		4.00 BSC			0.157 BSC	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1		4.00 BSC			0.157 BSC	
SE		1.00 TYP			0.039 TYP	
SD		1.00 TYP			0.039 TYP	
e		1.00 BSC			0.039 BSC	
ccc	---	---	0.10	---	---	0.0039

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10.4 Ordering Information



Notes:

1. The “W” prefix and the Temperature designator “I” are not included on the part marking.
2. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T) or Tray (shape S), when placing orders.
3. For shipments with special order options, please contact Winbond.

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10.5 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25Q01JV SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 10-digit number.

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
ZE[2] WSON-8 8x6mm	1G-bit	W25Q01JVZEIM	25Q01JVIM
SF SOIC-16 300mil	1G-bit	W25Q01JVSFIM	25Q01JVFIM
TB[1] TFBGA-24 8x6mm (5x5-1 Ball Array)	1G-bit	W25Q01JVTBIM	25Q01JVBIM

Note:

1. These package types are special order, please contact Winbond for more information.
2. For WSON packages, the package type ZE is not used in the top side marking.

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11. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	03/28/2019 10/15/2019	92 104 106 113	New Create Updated C0h Updated ICC3 SPEC Updated tCSS1 tCLQV & Tpp & Tce Updated product number
B	11/13/2019		Removed Preliminary & EAR
C	03/31/2020	8	Updated TFBGA A4 Ball
D	11/02/2020	18	Updated LB Non-Volatile
E1	03/04/2024	7 16,17,19,31	Updated SOIC-16 DNU/NC Updated Stacked die operation application note no.
F	10/04/2024	96,98 108	Added write enable for 39h, 7Eh and 98h Added Notice for SPIC-16 300mil

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