1.8V 1G-BIT
SLC QSPINAND FLASH MEMORY WITH DUAL/QUAD SPI
BUFFER READ & SEQUENTIAL READ

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1. GENERAL DESCRIPTIONS

The W25N01KW (1G-bit) SLC QspiNAND Flash Memory provides a storage solution for systems with limited space, pins and power. The W25N QspiNAND family incorporates the popular SPI interface and the traditional large NAND non-volatile memory space. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 1.7V to 1.95V power supply with current consumption as low as 25mA active and10µA for standby. All W25N QspiNAND family devices are offered in space-saving packages which were impossible to use in the past for the typical NAND flash memory.

The W25N01KW 1G-bit memory array is organized into 65,536 programmable pages of 2,048-bytes each. The entire page can be programmed at one time using the data from the 2,048-Byte internal buffer. Pages can be erased in groups of 64 (128KB block erase). The W25N01KW has 1,024 erasable blocks.

The W25N01KW supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions.

The W25N01KW provides Sequential Read Mode that allows for efficient access to the entire memory array with a single Read instruction. These features are ideal for code shadowing applications.

A Hold pin, Write Protect pin and programmable write protection, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID, one Unique ID page, one parameter page and ten 2,048-Byte OTP pages. To provide better NAND flash memory manageability, user configurable internal ECC is also available in W25N01KW.

2. FEATURES

- **New W25N Family of QspiNAND Memories**
  - W25N01KW: 1G-bit / 128M-Byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Compatible SPI serial flash instructions
- **Organization**
  - Page size: 2,112 Byte (2048+64 Byte) + 32 Byte controlled by Flash for ECC parity bits.
  - Block size: 64 Pages (128K+4K Byte) + 2K Byte controlled by Flash for ECC parity bits.
- **Highest Performance Serial NAND Flash**
  - 104MHz Standard/Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - Fast Program/Erase performance
  - 100,000 erase/program cycles(1)
  - 10-year data retention
- **Low Power, Wide Temperature Range**
  - Single 1.70 to 1.95V supply
  - 25mA active, 10µA standby, 1µA DPD(2)
  - -40°C to +85°C/105°C(3) operating range
- **Flexible Architecture with 128KB blocks**
  - Uniform 128K-Byte Block Erase
  - Flexible page data load methods
- **Advanced Features(4)**
  - On chip 4-Bit ECC for memory array
  - Block 0 to Block 7 and Block 1020 to Block 1023 are valid blocks when shipped from factory with on chip ECC enabled
  - ECC status bits indicate ECC results
  - Bad Block Management and LUT access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Unique ID and parameter pages(5)
  - Ten 2KB OTP pages(6)
- **Space Efficient Packaging**
  - 8-pad WSON 6x5-mm and 8x6-mm
  - Contact Winbond for other package options

Notes:
1. Endurance specification is based on the on-chip ECC or 4bits/528bytes ECC (Error Correcting Code), industrial grade only. Contact Winbond for detail information.
2. Industrial grade only. DPD stands for Deep Power Down.
3. 105°C is supported in Industrial Plus Grade
4. Please refer to chapter 7 for detail information
5. Please refer to chapter 8.2.23 & 24 for detail information
6. OTP pages can only be programmed.

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3. PACKAGE TYPES AND PIN CONFIGURATIONS

W25N01KW is offered in an 8-pad WSON 6x5-mm (package code ZP) and an 8-pad WSON 8x6-mm (package code ZE), packages as shown in Figure 1. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pad Configuration WSON 6x5-mm, WSON 8x6-mm

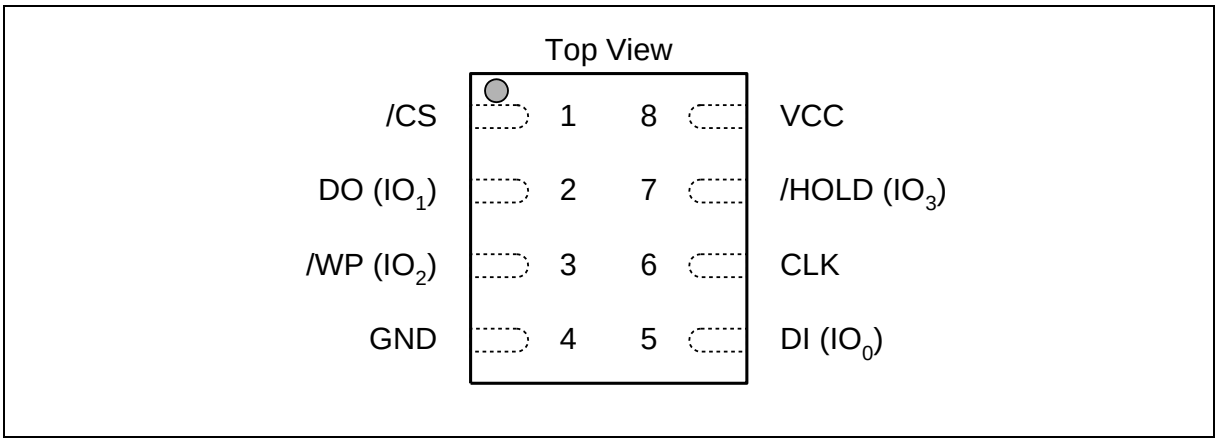


Figure 1. W25N01KW Pad Assignments, 8-pad WSON 6x5mm and 8x6-mm (Package Code ZP, ZE)

3.2 Pad Description WSON 6x5-mm, WSON 8x6-mm

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

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3.3 pin descriptions

3.4 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal page read, erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 33b). If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

3.5 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25N01KW supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

3.6 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect bits BP[3:0] and Status Register Protect SRP bits SRP[1:0], a portion as small as one 256KB Block or up to the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the /WP pin.

When WP-E=0, the device is in the Software Protection mode that only SR-1 can be protected. The /WP pin functions as a data I/O pin for the Quad SPI operations, as well as an active low input pin for the Write Protection function for SR-1. Refer to section 7.1.3 for detail information.

When WP-E=1, the device is in the Hardware Protection mode that /WP becomes a dedicated active low input pin for the Write Protection of the entire device. If /WP is tied to GND, all “Write/Program/Erase” functions are disabled. The entire device (including all registers, memory array, OTP pages) will become read-only. Quad SPI read operations are also disabled when WP-E is set to 1.

3.7 HOLD (/HOLD)

During Standard and Dual SPI operations, the /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low.

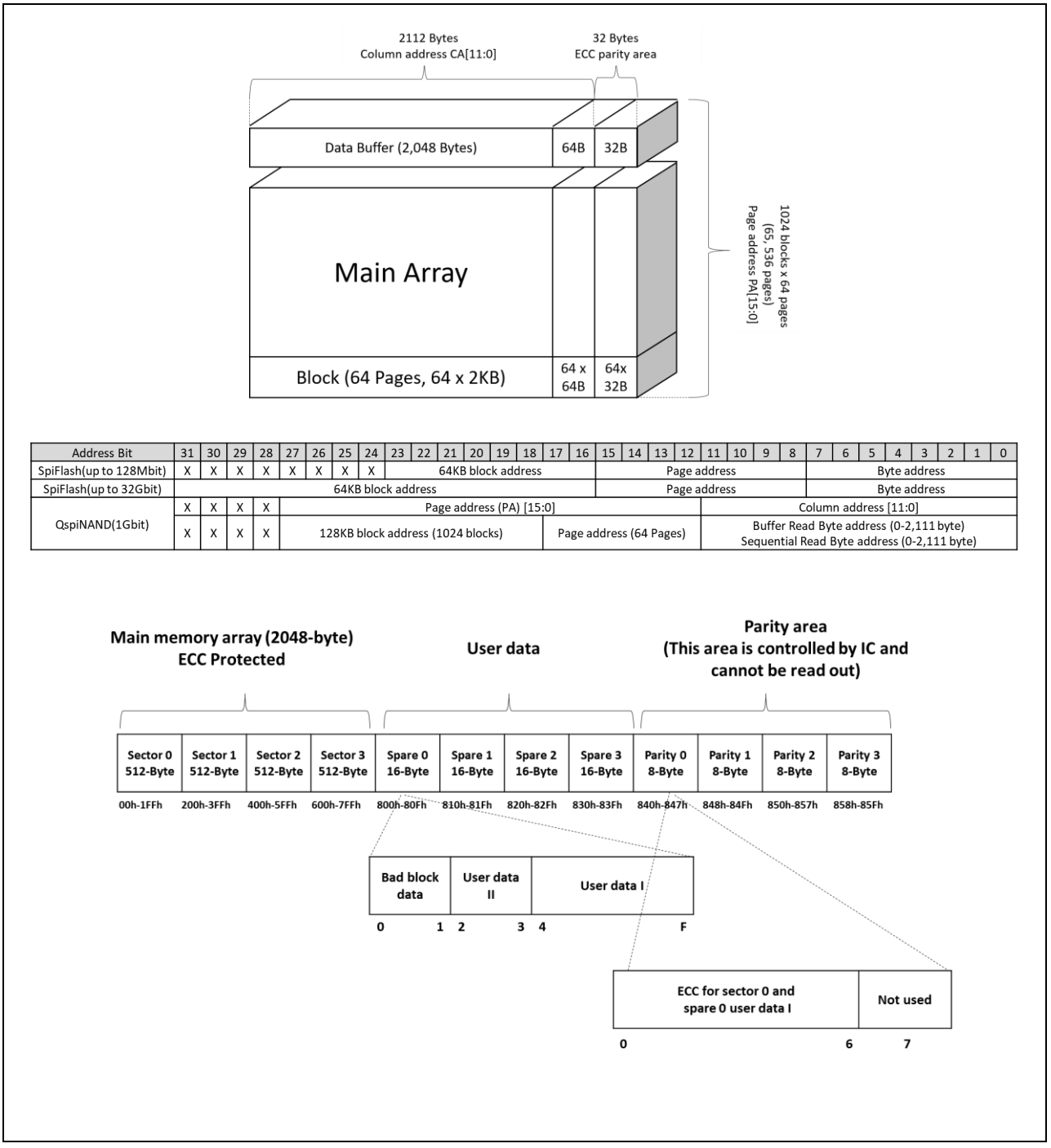
When a Quad SPI Read/Buffer Load instruction is issued, /HOLD pin will become a data I/O pin for the Quad operations and no HOLD function is available until the current Quad operation finishes. /HOLD (IO3) must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the /HOLD input to float.

3.8 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

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4. BLOCK DIAGRAM



Address Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SpiFlash(up to 128Mbit)	X	X	X	X	X	X	X	X	64KB block address								Page address								Byte address							
SpiFlash(up to 32Gbit)	64KB block address																Page address								Byte address							
QspiNAND(1Gbit)	X	X	X	X	Page address (PA) [15:0]												Column address [11:0]															
	X	X	X	X	128KB block address (1024 blocks)												Page address (64 Pages)				Buffer Read Byte address (0-2,111 byte) Sequential Read Byte address (0-2,111 byte)											

Figure 2. W25N01KW Flash Memory Architecture and Addressing

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5. FUNCTIONAL DESCRIPTIONS

5.1 Device Operation Flow

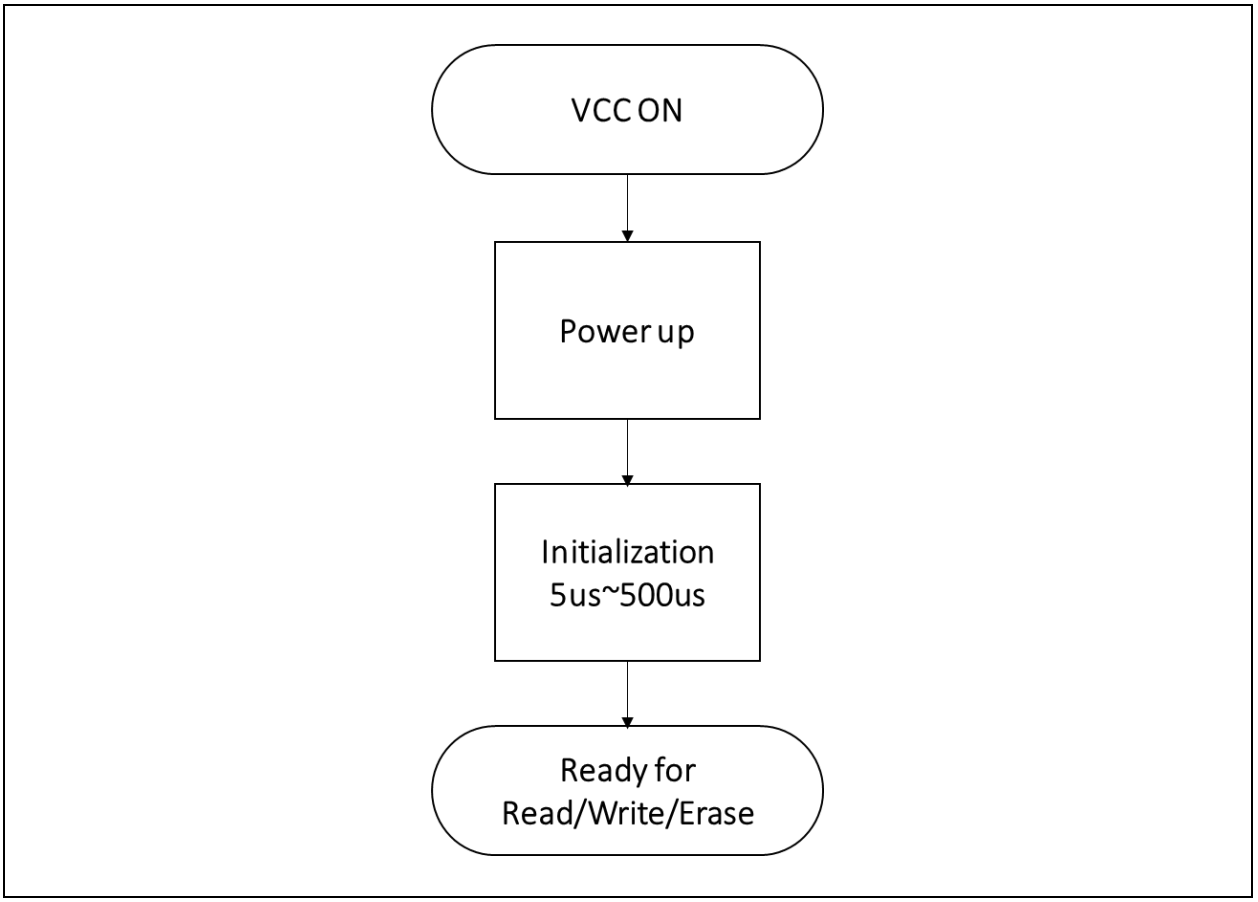


Figure 3. W25N01KW Flash Memory Operation Diagram

5.1.1 Standard SPI Instructions

The W25N01KW is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the SpiNAND. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

5.1.2 Dual SPI Instructions

The W25N01KW supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary QspiNAND devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical

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code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

5.1.3 Quad SPI Instructions

The W25N01KW supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)” and “Quad Program Data Load (32h/34h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary SpiNAND. The Quad Read instructions offer a significant improvement in random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instruction, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively.

5.1.4 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25N01KW operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. When a Quad SPI command is issued, /HOLD pin will act as a dedicated IO pin (IO3).

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

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5.1.5 Reset Signaling Protocol

The W25N01KW provides additional Hardware Reset by a signaling protocol

The key points for the Reset Signaling Protocol are:

- CLK remains stable in either High or Low state. Toggle /CS instead of CLK. This prevents any confusion with a command, as no command bits are transferred (clocked).
- W25N01KW captures the state of DI(IO0) on the rising edge of /CS.
- DI(IO0) have to be low on the first /CS, high on the second, low on the third, high on the fourth. This 5h pattern (=0b0101) is for differentiate from random noise.
- The hardware reset by signaling protocol release the deep power down state.

Once the Reset Signaling Protocol is accepted, any on-going internal operations will be terminated and will reset the device to its initial power-on state. It takes same busy time with power-on (tVSL and tPUW) because Hardware Reset goes into the same state of after power-on. No command will be accepted during the tVSL period. Please refer to “7.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detail information about the value of each Status Registers after reset. If there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device, data corruption may happen at only the address that is the target of the on-going operation. It is recommended to check the BUSY bit in Status Register before issuing the Reset command.

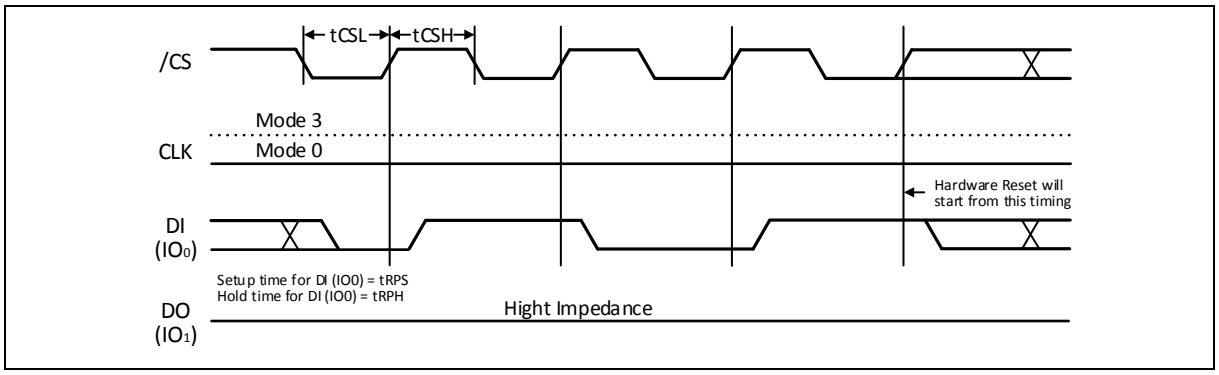


Figure 4. Reset Signaling Protocol

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5.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25N01KW provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Protection Register (SR-1)
- Lock Down write protection for Protection Register (SR-1) until the next power-up
- One Time Program (OTP) write protection for memory array using Protection Register (SR-1)
- Hardware write protection using /WP pin when WP-E is set to 1

Upon power-up or at power-down, while VCC is below VCC(min), (see “Power-up Power-down Timing Requirements”), all operations are disabled and no instructions are recognized. During power-up, after the VCC voltage exceeds VCC(min) and tVSL has elapsed, all program and erase related instructions are further disabled for a time delay of tPUW. This includes the Write Enable, Program Execute, Block Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and tVSL time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Program Execute and Block Erase instruction will be accepted. After completing a program or erase instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Protection Register section for further information.

The WP-E bit in Protection Register (SR-1) is used to enable the hardware protection. When WP-E is set to 1, bringing /WP low in the system will block any Write/Program/Erase command to the W25N01KW, the device will become read-only. The Quad SPI operations are also disabled when WP-E is set to 1.

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6. PROTECTION, CONFIGURATION AND STATUS REGISTERS

Three Status Registers are provided for W25N01KW: Protection Register (SR-1), Configuration Register (SR-2) & Status Register (SR-3). Each register is accessed by Read Status Register and Write Status Register commands combined with 1-Byte Register Address respectively.

The Read Status Register instruction (05h / 0Fh) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Read modes, Protection Register/OTP area lock status, Erase/Program results, ECC usage/status. The Write Status Register instruction can be used to configure the device write protection features, Software/Hardware write protection, Read modes, enable/disable ECC, Protection Register/OTP area lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and when WP-E is set to 1, the /WP pin.

6.1 Protection Register / Status Register-1 (Volatile Writable, OTP lockable)

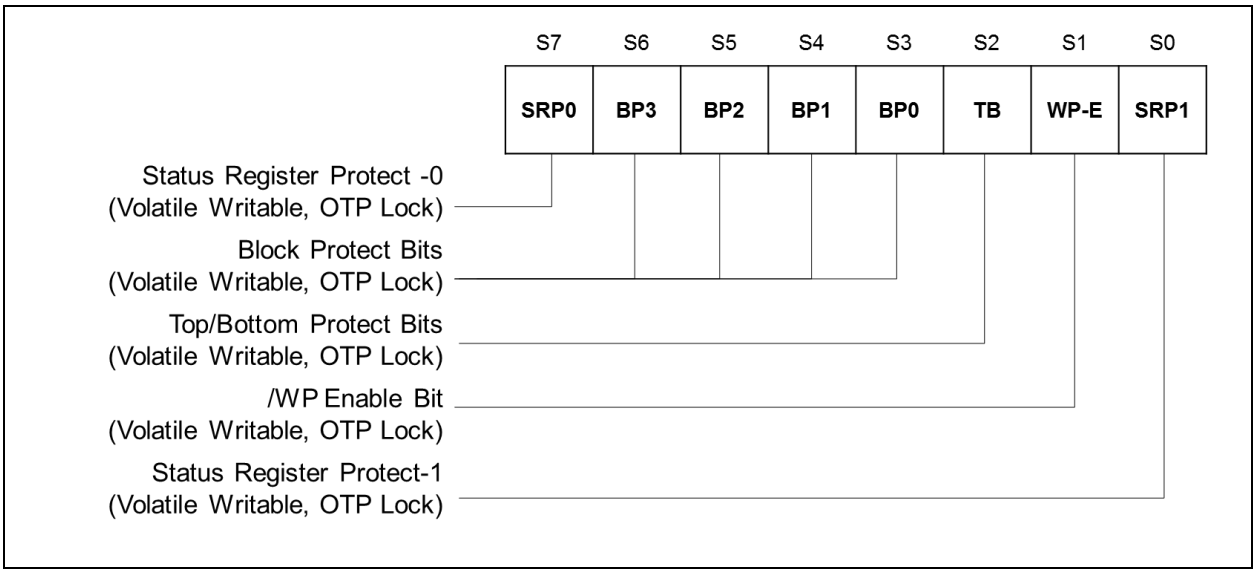


Figure 5. Protection Register / Status Register-1 (Address Axh)

6.1.1 Block Protect Bits (BP3, BP2, BP1, BP0, TB) – *Volatile Writable, OTP lockable*

The Block Protect bits (BP3, BP2, BP1, BP0 & TB) are volatile read/write bits in the status register-1 (S6, S5, S4, S3 & S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The default values for the Block Protection bits are 1 after power up to protect the entire array. If the SR1-L bit in the Configuration Register (SR-2) is set to 1, the default values will the values that are OTP locked.

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6.1.2 Write Protection Enable Bit (WP-E) – *Volatile Writable, OTP lockable*

The Write Protection Enable bit (WP-E) is a volatile read/write bits in the status register-1 (S1). The WP-E bit, in conjunction with SRP1 & SRP0, controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection, /WP pin functionality, and Quad SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, /WP & /HOLD pins are multiplexed as IO pins, and Quad program/read functions are enabled all the time. When WP-E is set to 1, the device is in Hardware Protection mode, all Quad functions are disabled and /WP & /HOLD pins become dedicated control input pins.

6.1.3 Status Register Protect Bits (SRP1, SRP0) – *Volatile Writable, OTP lockable*

The Status Register Protect bits (SRP1 and SRP0) are volatile read/write bits in the status register (S0 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Software Protection (Driven by Controller, Quad Program/Read is enabled)				
SRP1	**SRP0**	**WP-E**	**/WP / IO2**	**Descriptions**
0	0	0	X	No /WP functionality */WP pin will always function as IO2*
0	1	0	0	SR-1 cannot be changed (/WP = 0 during Write Status) */WP pin will function as IO2 for Quad operations*
0	1	0	1	SR-1 can be changed (/WP = 1 during Write Status) */WP pin will function as IO2 for Quad operations*
1	0	0	X	Power Lock Down(1) SR-1 */WP pin will always function as IO2*
1	1	0	X	Enter OTP mode to protect SR-1 (allow SR1-L=1) */WP pin will always function as IO2*

Hardware Protection (System Circuit / PCB layout, Quad Program/Read is disabled)				
SRP1	**SRP0**	**WP-E**	**/WP only**	**Descriptions**
0	X	1	VCC	SR-1 can be changed
1	0	1	VCC	Power Lock-Down(1) SR-1
1	1	1	VCC	Enter OTP mode to protect SR-1 (allow SR1-L=1)
X	X	1	GND	All “Write/Program/Erase” commands are blocked Entire device (SRs, Array, OTP area) is read-only

Notes:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

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6.2 Configuration Register / Status Register-2 (Volatile Writable)

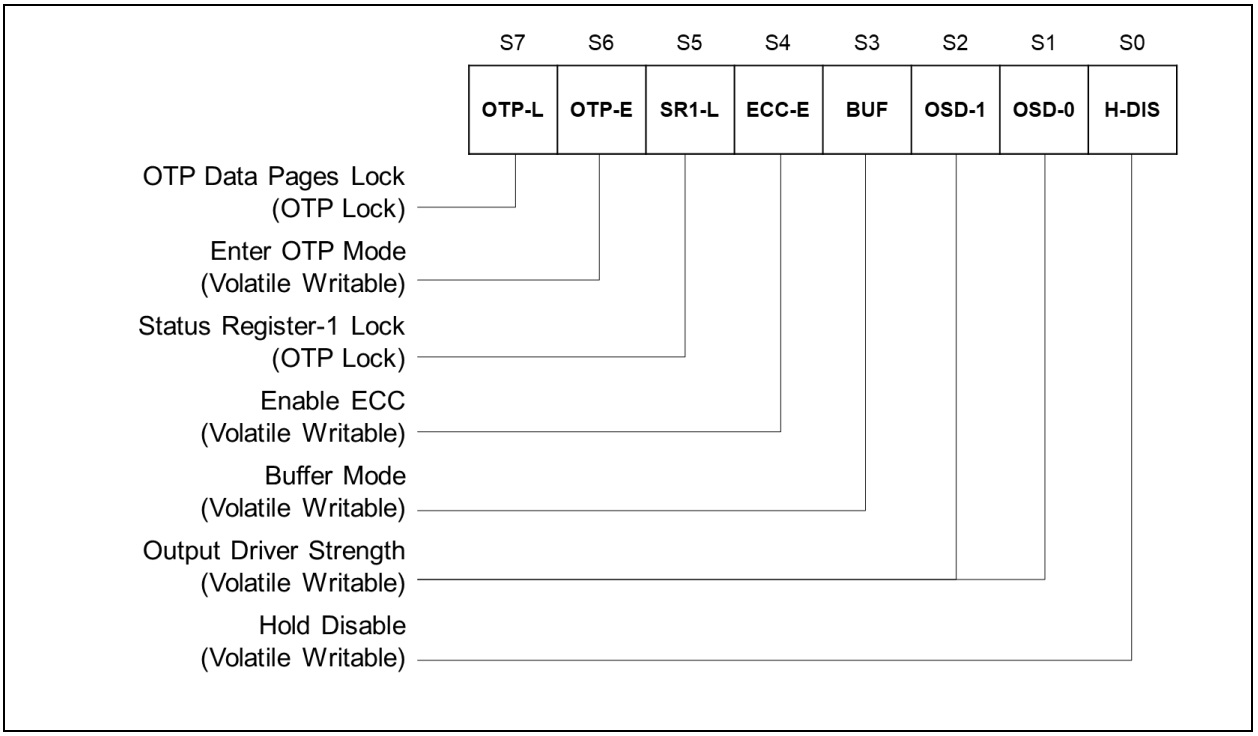


Figure 6. Configuration Register / Status Register-2 (Address Bxh)

6.2.1 One Time Program Lock Bit (OTP-L) – *OTP lockable*

In addition to the main memory array, W25N01KW also provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 10 pages of 2,112-Byte each. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from "1" to "0", and data is not reversible ("0" to "1") by the Erase command. Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

6.2.2 Enter OTP Access Mode Bit (OTP-E) – *Volatile Writable*

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up or a RESET command is 0.

6.2.3 Status Register-1 Lock Bit (SR1-L) – *OTP lockable*

The SR1-L lock bit is used to OTP lock the values in the Protection Register (SR-1). Depending on the settings in the SR-1, the device can be configured to have a portion of or up to the entire array to be write-protected, and the setting can be OTP locked by setting SR1-L bit to 1. SR1-L bit can only be set to 1 permanently when SRP1 & SRP0 are set to (1,1), and OTP Access Mode must be entered (OTP-E=1) to execute the programming. Please refer to 8.2.18 for detailed information.

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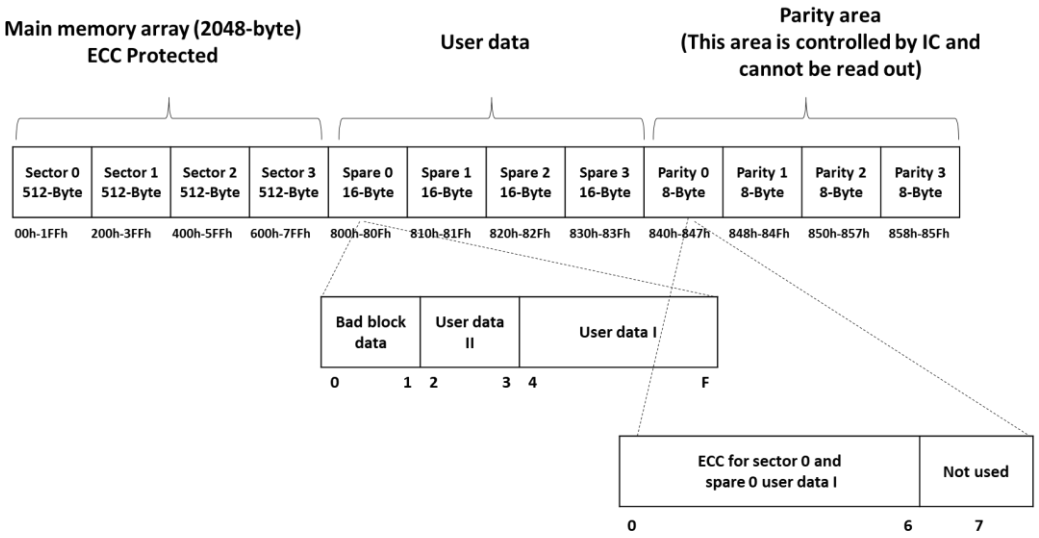
6.2.4 ECC Enable Bit (ECC-E) – *Volatile Writable*

W25N01KW has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 32-Byte area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bits. ECC function is enabled by default when power on (ECC-E=1), and it will not be reset to 0 by the Device Reset command.

The constraint when ECC-E=1 are as follows:

- The areas protected by ECC is shown in the table below. User Data I is protected by ECC, but User Data II is out of protected by ECC.
- The Number of Partial Page Program (NoP) is 4 for the entire page, including the spare area and parity area. Therefore the user needs to program one sector and User Data I of paired spare area (example, main area-sector 0 and spare area-spare 0) at one time program to properly and automatically program the ECC parity area.

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Area	Main area			
	Sector 0	Sector 1	Sector 2	Sector 3
Address (Start)	000h	200h	400h	600h
Address (End)	1FFh	3FFh	5FFh	7FFh
Size	512B	512B	512B	512B

Area	Spare area							
	Spare 0		Spare 1		Spare 2		Spare 3	
	UD2	UD1	UD2	UD1	UD2	UD1	UD2	UD1
Address (Start)	800h	804h	810h	814h	820h	824h	830h	834h
Address (End)	803h	80Fh	813h	81Fh	823h	82Fh	833h	83Fh
Size	4B	12B	4B	12B	4B	12B	4B	12B

Area	Parity area							
	Parity 0		Parity 1		Parity 2		Parity 3	
	EPC	NU	EPC	NU	EPC	NU	EPC	NU
Address (Start)	840h	847h	848h	84Fh	850h	857h	858h	85Fh
Address (End)	846h	847h	84Eh	84Fh	856h	857h	85Eh	85Fh
Size	7B	1B	7B	1B	7B	1B	7B	1B

Notes:

1. UD2: User Data II
2. UD1: User Data I
3. EPC: ECC Parity Code
4. NU: Not Use

The gray area of the above table is protected by ECC. From each 7 bytes. Bit [51:0] is used for ECC Parity bits. Address 840h - 85Fh is controlled by IC.

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6.2.5 Output Driver Strength (ODS-1, ODS-0) – *Volatile Writable*

ODS-1, ODS-0	Output driver strength	Ron
0, 0	Set 1	25 Ω
0, 1	Set 2	33 Ω
1, 0	Set 3 (default)	50 Ω
1, 1	Set 4	75 Ω

6.2.6 Hold Disable (H-DIS) – *Volatile Writable*

When the Hold Disable (H-DIS) bit set to 1, the hold function would be disabled.

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6.2.7 Buffer Read / Sequential Read Mode Bit (BUF) – *Volatile Writable*

W25N01KW provides two different modes for read operations, Buffer Read Mode (BUF=1) and Sequential Read Mode (BUF=0). Prior to any Read operation, a Page Data Read command is needed to initiate the data transfer from a specified page in the memory array to the Data Buffer. By default, after power up, the data in page 0 will be automatically loaded into the Data Buffer and the device is ready to accept any read commands.

The Buffer Read Mode (BUF=1) requires a Column Address to start outputting the existing data inside the Data Buffer, and once it reaches the end of the data buffer (Byte 2,111), DO (IO1) pin will become high-Z state.

The Sequential Read Mode (BUF=0) doesn't require the starting Column Address. The device will always start output the data from the first column (Byte 0) of the Data buffer, and once the end of the data buffer (Byte 2,111) is reached, the data output will continue through the next memory page. With Sequential Read Mode, it is possible to read out the entire memory array using a single read command. Please refer to respective command descriptions for the dummy cycle requirements for each read commands under different read modes.

In Sequential Read Mode, for each read instruction: 03h, 0Bh, 3Bh, 6Bh, BBh and EBh, the CA [15:0] address input becomes dummy input. The read must start from the beginning of the page. During this read mode, there is no built-in ECC algorithm that can be used to preserve the data integrity.

For W25N01KWxxxU part number, the default value of BUF bit after power up is 0. BUF bit can be written to 1 in the Status Register-2 to perform the Buffer Read operation.

For W25N01KWxxxE part number, the default value of BUF bit after power up is 1. BUF bit can be written to 0 in the Status Register-2 to perform the Sequential Read operation.

BUF	ECC-E	Read Mode (Starting from Buffer)	ECC Status	Data Output Structure
1	0	Buffer Read	N/A	2,048 + 64
1	1	Buffer Read	Page based	2,048 + 64
0	X	Sequential Read	N/A	2,048 + 64

*note: Bit flip count > BFD setting

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6.3 Status Register-3 (Status Only)

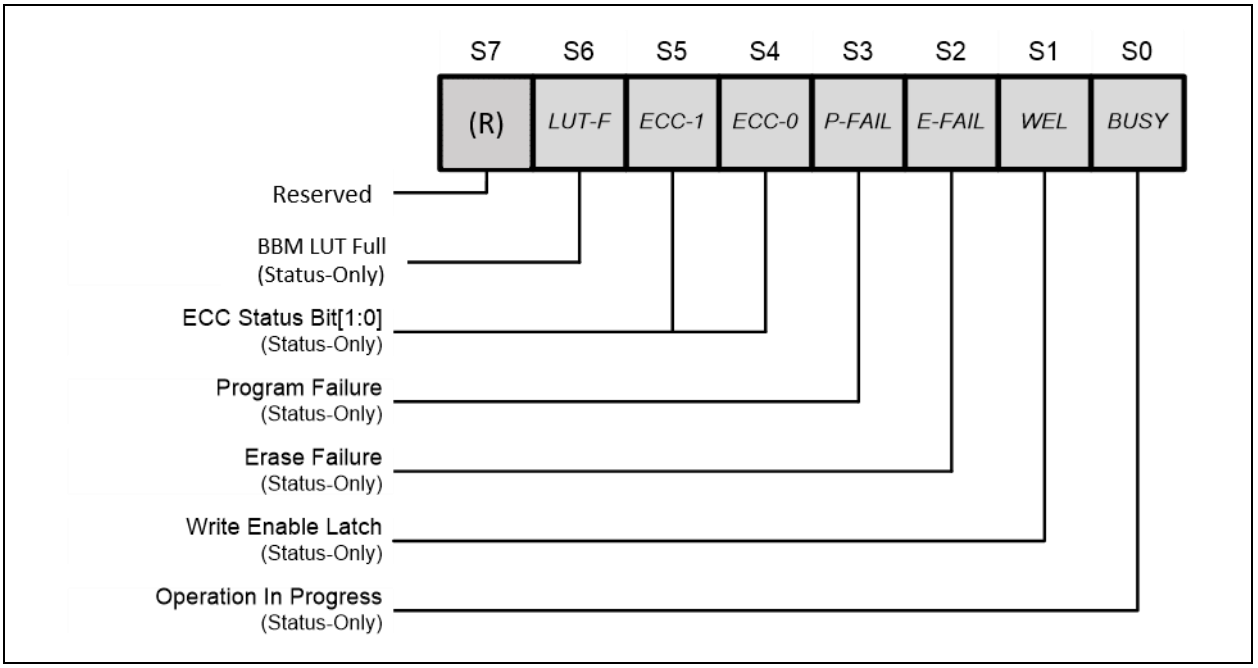


Figure 7. Status Register-3 (Address Cxh)

6.3.1 Look-Up Table Full (LUT-F) – Status Only

To facilitate the NAND flash memory bad block management, the W25N01KW is equipped with an internal Bad Block Management Look-Up-Table (BBM LUT). Up to 20 bad memory blocks may be replaced by a good memory block respectively. The addresses of the blocks are stored in the internal Look-Up Table as Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 20 memory block links have been fully utilized or not. The default value of LUT-F is 0, once all 20 links are used, LUT-F will become 1, and no more memory block links may be established.

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6.3.2 Cumulative ECC Status (ECC-1, ECC-0) – *Status Only*

ECC function is used in NAND flash memory to correct limited memory errors during read operations. Bit flips count in a sector equal to or less than 4bits would be detected and corrected. The ECC Status Bits (ECC-1, ECC-0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-E=0. These bits will be cleared to 0 after a power cycle or a RESET command or a Page Data Read Command.

ECC Status		Descriptions
ECC-1	ECC-0	
0	0	Entire data output is **successful**. No bit flips were detected in previous page read.
0	1	Entire data output is **successful**. Bit flips were detected and corrected. Bit flip count did not exceed the bit flip detection threshold. The threshold is set by bits [7:4] in address 10h in the feature table.
1	0	Multiple bit flips were detected and not corrected.
1	1	Bit flips were detected and corrected. Bit flip count *exceeded the bit flip detection threshold. Page data refreshment or remove must be taken to hold data retention.

*note: Bit flip count > BFD setting

6.3.3 Program Failure (P-FAIL) – *Status Only*

The Program Failure Bit is used to indicate whether the internally-controlled Program operation was executed successfully (P-FAIL=0) or timed out (P-FAIL=1). The P-FAIL bit is also set when the Program command is issued to a locked or protected memory array or OTP area. This bit is cleared at the beginning of the Program Execute instruction on an unprotected memory array or OTP area. Device Reset instruction can also clear the P-FAIL bit.

6.3.4 Erase Failure (E-FAIL) – *Status Only*

The Erase Failure Bit is used to indicate whether the internally-controlled Erase operation was executed successfully (E-FAIL=0) or timed out (E-FAIL=1). The E-FAIL bit is also set when the Erase command is issued to a locked or protected memory array. This bit is cleared at the beginning of the Block Erase instruction on an unprotected memory array. Device Reset instruction can also clear the E-FAIL bit.

6.3.5 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read and Program Execute for OTP pages.

6.3.6 Erase/Program In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is powering up or executing a Page Data Read, Program Execute, Block Erase. During this time the device will ignore further instructions except for the Read Status Register and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

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6.4 Extended internal ECC feature registers

Address	Bit							
	S7	S6	S5	S4	S3	S2	S1	S0
10h	I	BFD2	BFD1	BFD0	I	I	I	I
20h	I	I	I	I	BFS3	BFS2	BFS1	BFS0
30h	I	MBF2	MBF1	MBF0	I	MFS2	MFS1	MFS0
40h	I	BFR6	BFR5	BFR4	I	BFR2	BFR1	BFR0
50h	I	BFR14	BFR13	BFR12	I	BFR10	BFR9	BFR8

* I = Reserved Bit

Figure 8. Extended Internal ECC feature registers

6.4.1 ECC Bit Flip Count Detection (BFD) – *Volatile Writable*

The ECC Bit Flip Count Detection function detects the bit flip count in a page. The users set the threshold bit count using the Write Extended Internal ECC feature registers command. The threshold bit count is decided by the bit flip detection setting bit (BFD) in address 10h in the feature table as shown in Figure 9. The detected results will be indicated in the BFS bits (bits [7:0]) in address 20h. When bit flips exceed the threshold in a sector, the BFS bits are set after the Page Data Read (13h) command with ECC-E = 1.

BFD2	BFD1	BFD0	Description
0	0	0	Reserved
0	0	1	Detect 1 bit flip in a sector.
0	1	0	Detect 2 bits flip in a sector.
0	1	1	Detect 3 bits flip in a sector. (default)
1	X	X	Reserved

*Note: change by test trimming

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6.4.2 ECC Bit Flip Count Detection Status (BFS) – *Status Only*

Symbol	Parameter	Status	Description
BFS3	Bit flip count detection status in sector 3	1	Bit flips count is equal to or more than threshold bit count
		0	Bit flips count is less than threshold bit count
BFS2	Bit flip count detection status in sector 2	1	Bit flips count is equal to or more than threshold bit count
		0	Bit flips count is less than threshold bit count
BFS1	Bit flip count detection status in sector 1	1	Bit flips count is equal to or more than threshold bit count
		0	Bit flips count is less than threshold bit count
BFS0	Bit flip count detection status in sector 0	1	Bit flips count is equal to or more than threshold bit count
		0	Bit flips count is less than threshold bit count

6.4.3 ECC Bit Flip Count Report (BFR) – *Status Only*

The ECC Bit Flip Count Report function reports the bit flip count of each sector in a page. The users can read the bit flip count using the Read Extended Internal ECC status register command with address 40h and 50h.

BFR14/10/6/2	BFR13/9/5/1	BFR12/8/4/0	Description
0	0	0	No bit flip in a sector
0	0	1	Detect 1 bit flips in a sector and corrected.
0	1	0	Detect 2 bits flip in a sector and corrected.
0	1	1	Detect 3 bits flip in a sector and corrected.
1	0	0	Detect 4 bits flip in a sector and corrected.
1	1	1	Bit flips over 4 bits in a sector and were not corrected.

BFR set	Parameter
BFR[14:12]	Bit flip count detection report for sector 3
BFR[10:8]	Bit flip count detection report for sector 2
BFR[6:4]	Bit flip count detection report for sector 1
BFR[2:0]	Bit flip count detection report for sector 0

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6.4.4 ECC Maximum Bit Flip Count Report (MBF, MFS) – *Status Only*

The ECC Maximum Bit Flip Count Report function provides the maximum bit flip count in a page. The maximum count is indicated in address 30h of the feature table shown in follow table. The sector number in which the maximum bit flip occurred in a page is indicated in the MFS bit (bits [2:0]) in address 30h as shown in follow table. When several sector's maximum bit flip count is the same, the lowest sector number is indicated in these bits. The users get the report using the Read Extended Internal ECC status register command.

MBF2	MBF1	MBF0	Description
0	0	0	No bit error is detected in the page.
0	0	1	Maximum bit flip count is 1 bit in a sector. Bit flip was corrected.
0	1	0	Maximum bit flip count is 2 bits in a sector. Bit flips were corrected.
0	1	1	Maximum bit flip count is 3 bits in a sector. Bit flips were corrected.
1	0	0	Maximum bit flip count is 4 bits in a sector. Bit flips were corrected.
1	1	1	Maximum bit flip count exceeds 4 bits in a sector. Bit flips were not corrected.

MFS2	MFS1	MFS0	Description
0	0	0	Maximum bit flips occurred in sector 0.
0	0	1	Maximum bit flips occurred in sector 1.
0	1	0	Maximum bit flips occurred in sector 2.
0	1	1	Maximum bit flips occurred in sector 3.

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6.5 W25N01KW Status Register Memory Protection

STATUS REGISTER[1]					W25N01KW (1G-BIT /128M-BYTE) MEMORY PROTECTION[2]			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED PAGE ADDRESS PA[23:0]	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	1022 thru 1023	FF80h – FFFFh	256KB	Upper 1/512
0	0	0	1	0	1020 thru 1023	FF00h – FFFFh	512KB	Upper 1/256
0	0	0	1	1	1016 thru 1023	FE00h – FFFFh	1MB	Upper 1/128
0	0	1	0	0	1008 thru 1023	FC00h – FFFFh	2MB	Upper 1/64
0	0	1	0	1	992 thru 1023	F800h – FFFFh	4MB	Upper 1/32
0	0	1	1	0	960 thru 1023	F000h – FFFFh	8MB	Upper 1/16
0	0	1	1	1	896 thru 1023	E000h – FFFFh	16MB	Upper 1/8
0	1	0	0	0	768 thru 1023	C000h – FFFFh	32MB	Upper 1/4
0	1	0	0	1	512 thru 1023	8000h – FFFFh	64MB	Upper 1/2
1	0	0	0	1	0 thru 1	0000h – 007Fh	256KB	Lower 1/512
1	0	0	1	0	0 thru 3	0000h – 00FFh	512KB	Lower 1/256
1	0	0	1	1	0 thru 7	0000h – 01FFh	1MB	Lower 1/128
1	0	1	0	0	0 thru 15	0000h – 03FFh	2MB	Lower 1/64
1	0	1	0	1	0 thru 31	0000h – 07FFh	4MB	Lower 1/32
1	0	1	1	0	0 thru 63	0000h – 0FFFh	8MB	Lower 1/16
1	0	1	1	1	0 thru 127	0000h – 1FFFh	16MB	Lower 1/8
1	1	0	0	0	0 thru 255	0000h – 3FFFh	32MB	Lower 1/4
1	1	0	0	1	0 thru 511	0000h – 7FFFh	64MB	Lower 1/2
X	1	0	1	X	0 thru 1023	0000h – FFFFh	128MB	ALL
X	1	1	X	X	0 thru 1023	0000h – FFFFh	128MB	ALL

Notes:

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

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7. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25N01KW consists of 26 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1, 2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 10 through 37. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the device is performing Program or Erase operation, Page Data Read or OTP locking operations, BUSY bit will be high, and all instructions except for Read Status Register or Read JEDEC ID will be ignored until the current operation cycle has completed.

7.1 Device ID and Instruction Set Tables

7.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 – MF0)**
Winbond SpiNAND	EFh
Device ID	**(ID15 – ID0)**
W25N01KW	BE21h

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7.1.2 Instruction Set Table 1 (Buffer Read, BUF =1)

Instructions	OpCode	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
Device RESET	**FFh**								
JEDEC ID	**9Fh**	Dummy	***EFh***	***BEh***	***21h***				
Read Status Register 1	**0Fh / 05h**	Axh	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Read Status Register 2	**0Fh / 05h**	Bxh	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Read Status Register 3	**0Fh / 05h**	Cxh	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Read Extended Internal ECC feature registers	**0Fh / 05h**	10h/20h/30h/40h/50h	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Write Status Register 1	**1Fh / 01h**	Axh	S7-0						
Write Status Register 2	**1Fh / 01h**	Bxh	S7-0						
Write Extended Internal ECC feature registers	**1Fh / 01h**	10h	S7-0						
BB Management (Swap Blocks)	**A1h**	LBA	LBA	PBA	PBA				
Read BBM LUT	**A5h**	Dummy	*LBA0*	*LBA0*	*PBA0*	*PBA0*	*LBA1*	*LBA1*	*PBA1*
Last ECC failure page address	**A9h**	Dummy	**PA15-8**	**PA7-0**					
Write Enable	**06h**								
Write Disable	**04h**								
Block Erase	**D8h**	**PA23-16*[1]**	**PA15-8**	**PA7-0**					
Program Data Load (Reset Buffer)	**02h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Random Program Data Load	**84h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Quad Program Data Load (Reset Buffer)	**32h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Random Quad Program Data Load	**34h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Program Execute	**10h**	*Dummy	**PA15-8**	**PA7-0**					
Page Data Read	**13h**	*Dummy	**PA15-8**	**PA7-0**					
Read	**03h**	**CA15-8**	**CA7-0**	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read	**0Bh**	**CA15-8**	**CA7-0**	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read Dual Output	**3Bh**	**CA15-8**	**CA7-0**	Dummy	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad Output	**6Bh**	**CA15-8**	**CA7-0**	Dummy	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Fast Read Dual I/O	**BBh**	**CA15-8 / 2**	**CA7-0 / 2**	Dummy / 2	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad I/O	**EBh**	**CA15-8 / 4**	**CA7-0 / 4**	Dummy / 4	Dummy / 4	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Deep Power-Down	**B9h**								
Release Power-Down	**ABh**								
Enable Reset	**66h**								
Reset Device	**99h**								

*__note__: PA[23:16] input would be ignored.

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7.1.3 Instruction Set Table 2 (Sequential Read, BUF = 0)

Instructions	OpCode	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
Device RESET	**FFh**								
JEDEC ID	**9Fh**	Dummy	***EFh***	***BEh***	***21h***				
Read Status Register 1	**0Fh / 05h**	Axh	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Read Status Register 2	**0Fh / 05h**	Bxh	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Read Status Register 3	**0Fh / 05h**	Cxh	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Read Extended Internal ECC feature registers	**0Fh / 05h**	10h/20h/30h/40h/50h	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***	***S7-0***
Write Status Register 1	**1Fh / 01h**	Axh	S7-0						
Write Status Register 2	**1Fh / 01h**	Bxh	S7-0						
Write Extended Internal ECC feature registers	**1Fh / 01h**	10h	S7-0						
BB Management (Swap Blocks)	**A1h**	LBA	LBA	PBA	PBA				
Read BBM LUT	**A5h**	Dummy	*LBA0*	*LBA0*	*PBA0*	*PBA0*	*LBA1*	*LBA1*	*PBA1*
Last ECC failure page address	**A9h**	Dummy	**PA15-8**	**PA7-0**					
Write Enable	**06h**								
Write Disable	**04h**								
Block Erase	**D8h**	**PA23-16*[1]**	**PA15-8**	**PA7-0**					
Program Data Load (Reset Buffer)	**02h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Random Program Data Load	**84h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Quad Program Data Load (Reset Buffer)	**32h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Random Quad Program Data Load	**34h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Program Execute	**10h**	Dummy	**PA15-8**	**PA7-0**					
Page Data Read	**13h**	Dummy	**PA15-8**	**PA7-0**					
Read	**03h**	Dummy	Dummy	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read	**0Bh**	Dummy	Dummy	Dummy	Dummy	***D7-0***	***D7-0***	***D7-0***	***D7-0***
Fast Read Dual Output	**3Bh**	Dummy	Dummy	Dummy	Dummy	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad Output	**6Bh**	Dummy	Dummy	Dummy	Dummy	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***	***D7-0 / 4***
Fast Read Dual I/O	**BBh**	Dummy / 2	Dummy / 2	Dummy / 2	Dummy / 2	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***	***D7-0 / 2***
Fast Read Quad I/O	**EBh**	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	***D7-0 / 4***	***D7-0 / 4***
Deep Power-Down	**B9h**								
Release Power-Down	**ABh**								
Enable Reset	**66h**								
Reset Device	**99h**								

***note**: PA[23:16] input would be ignored.

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Notes:

1. ***D7-0*** designates data output from the device.

2. Column Address (CA) only requires CA[11:0], CA[15:12] are considered as dummy bits.

3. Page Address (PA) requires 16 bits. PA[15:6] is the address for 128KB blocks (total 1024 blocks), PA[5:0] is the address for 2KB pages (total 64 pages for each block).

4. Status Register Addresses:
   Status Register 1 / Protection Register: Addr = Axh
   Status Register 2 / Configuration Register: Addr = Bxh
   Status Register 3 / Status Register: Addr = Cxh

5. Dual SPI Address Input (**CA15-8 / 2** and **CA7-0 / 2**) format:
   IO0 = x, x, CA10, CA8, CA6, CA4, CA2, CA0
   IO1 = x, x, CA11, CA9, CA7, CA5, CA3, CA1

6. Dual SPI Data Output (***D7-0 / 2***) format:
   IO0 = D6, D4, D2, D0, ……
   IO1 = D7, D5, D3, D1, ……

7. Quad SPI Address Input (**CA15-8 / 4** and **CA7-0 / 4**) format:
   IO0 = x, CA8, CA4, CA0
   IO1 = x, CA9, CA5, CA1
   IO2 = x, CA10, CA6, CA2
   IO3 = x, CA11, CA7, CA3

8. Quad SPI Data Input/Output (***D7-0 / 4***) format:
   IO0 = D4, D0, ……
   IO1 = D5, D1, ……
   IO2 = D6, D2, ……
   IO3 = D7, D3, ……

9. All Quad Program/Read commands are disabled when WP-E bit is set to 1 in the Protection Register.

10. For all Read operations, as soon as /CS signal is brought to high to terminate the read operation, the device will be ready to accept new instructions and all the data inside the Data Buffer will remain unchanged from the previous Page Data Read instruction.

11. For all Read operations in the Sequential Read Mode, once the /CS signal is brought to high to terminate the read operation, the device will still remain busy for tRD3 (BUSY=1), and all the data inside the Data buffer will be lost and un-reliable to use. A new Page Data Read instruction must be issued to reload the correct page data into the Data Buffer.

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7.2 Instruction Descriptions

7.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the W25N01KW provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device state bits will follow the below table. Once the Reset command is accepted by the device, the device will take approximately tRST to reset, depending on the current operation the device is performing, tRST can be 5us~500us. During this period, no command will be accepted.

Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit in Status Register before issuing the Reset command.

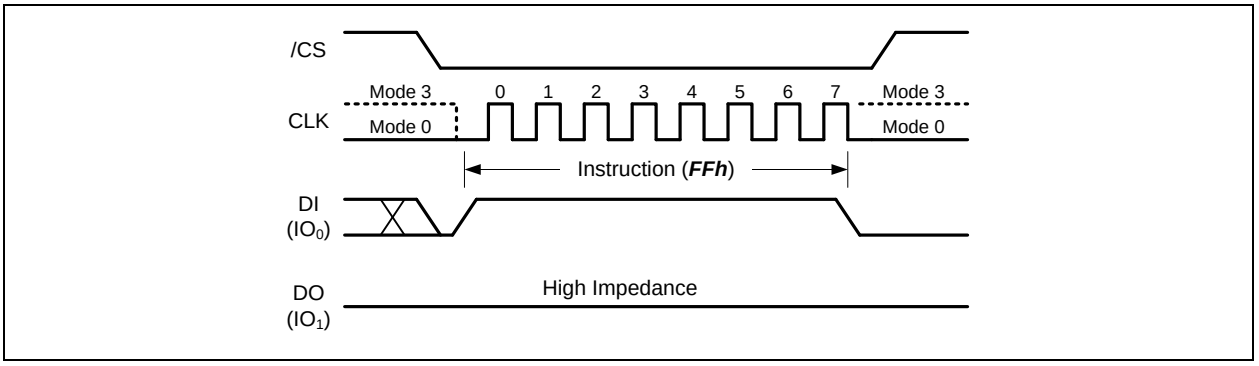


Figure 9. Device Reset Instruction

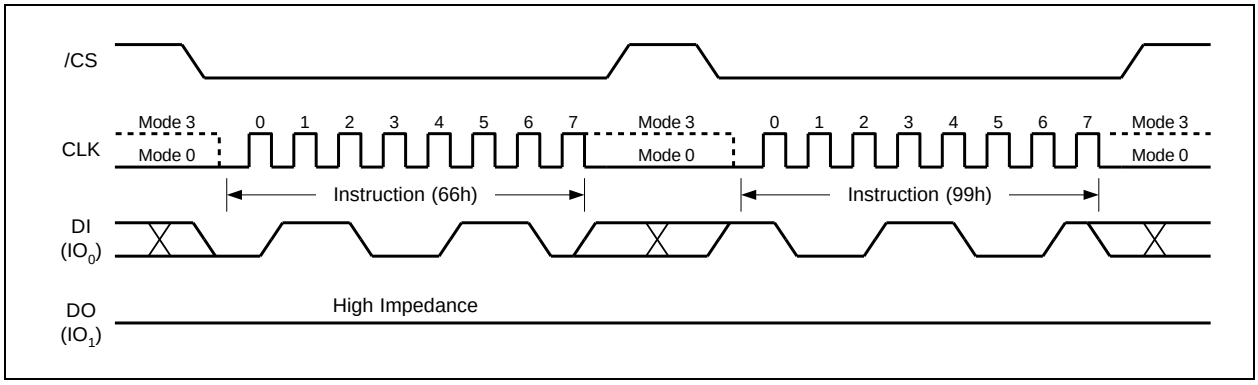


Figure 10. Enable Reset and Reset Instruction Sequence

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Register	Address		Bits	Shipment default	Power up after LUT is full	Power up after OTP area locked	Power up after SR-1 locked	After Reset (FFh) command	After Reset (66h+99h) command or reset signaling protocol
Status register-1	Axh	S7	SRP0	0	0	0	1(locked)	No change	0
		S6	BP3	1	1	1	x(locked)	No change	1
		S5	BP2	1	1	1	x(locked)	No change	1
		S4	BP1	1	1	1	x(locked)	No change	1
		S3	BP0	1	1	1	x(locked)	No change	1
		S2	TB	1	1	1	x(locked)	No change	1
		S1	WP-E	0	0	0	x(locked)	No change	0
		S0	SRP1	0	0	0	1(locked)	No change	0
Status register-2	Bxh	S7	OTP-L	0	1	1	0	Clear to 0 before OTP set	Clear to 0 before OTP set
		S6	OTP-E	0	0	0	0	0	0
		S5	SR1-L	0	0	0	1	Clear to 0 before OTP set	Clear to 0 before OTP set
		S4	ECC-E	1	1	1	1	No change	1
		S3	BUF	Based on special options	Based on special options	Based on special options	Based on special options	No change	Based on speical options
		S2	ODS-1	1	1	1	1	No change	1
		S1	ODS-0	0	0	0	0	No change	0
		S0	H-DIS	1	1	1	1	No change	1
Status register-3	Cxh	S7	Reserved	0	0	0	0	0	0
		S6	LUF-F	0	1	0	0	No change	Depends on LUT status after reset
		S5	ECC-1	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S4	ECC-0	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S3	P-FAIL	0	0	0	0	0	0
		S2	E-FAIL	0	0	0	0	0	0
		S1	WEL	0	0	0	0	0	0
		S0	BUSY	0	0	0	0	0	0

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Register	Address		Bits	Shipment default	Power up after LUT is full	Power up after OTP area locked	Power up after SR-1 locked	After Reset (FFh) command	After Reset (66h+99h) command or reset signaling protocol
Extended Cumulative ECC feature register-1	10h	S7	Reserved	0	0	0	0	0	0
		S6	BFD2	0	0	0	0	No change	0
		S5	BFD1	1	1	1	1	No change	1
		S4	BFD0	1	1	1	1	No change	1
		S3	Reserved	0	0	0	0	0	0
		S2	Reserved	0	0	0	0	0	0
		S1	Reserved	0	0	0	0	0	0
		S0	Reserved	0	0	0	0	0	0
Extended Cumulative ECC feature register-2	20h	S7	Reserved	0	0	0	0	0	0
		S6	Reserved	0	0	0	0	0	0
		S5	Reserved	0	0	0	0	0	0
		S4	Reserved	0	0	0	0	0	0
		S3	BFS3	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S2	BFS2	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S1	BFS1	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S0	BFS0	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
Extended Cumulative ECC feature register-3	30h	S7	Reserved	0	0	0	0	0	0
		S6	MBF2	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S5	MBF1	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S4	MBF0	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S3	Reserved	0	0	0	0	0	0
		S2	MFS2	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S1	MFS1	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S0	MFS0	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
Extended Cumulative ECC feature register-4	40h	S7	Reserved	0	0	0	0	0	0
		S6	BFR6	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S5	BFR5	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S4	BFR4	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S3	Reserved	0	0	0	0	0	0
		S2	BFR2	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S1	BFR1	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S0	BFR0	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
Extended Cumulative ECC feature register-5	50h	S7	Reserved	0	0	0	0	0	0
		S6	BFR14	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S5	BFR13	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S4	BFR12	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S3	Reserved	0	0	0	0	0	0
		S2	BFR10	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S1	BFR9	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
		S0	BFR8	Depends on page load result	Depends on page load result	Depends on page load result	Depends on page load result	0	0
Page 0 Reload				Page 0 reload	Page 0 reload	Page 0 reload	Page 0 reload	No reload	No reload

Figure 11. Default values of the Status Registers after power up and Device Reset

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7.2.2 Read JEDEC ID (9Fh)

The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh” followed by 8 dummy clocks. The JEDEC assigned Manufacturer ID byte for Winbond (Efh) and two Device ID bytes are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 12. For memory type and capacity values refer to Manufacturer and Device Identification table.

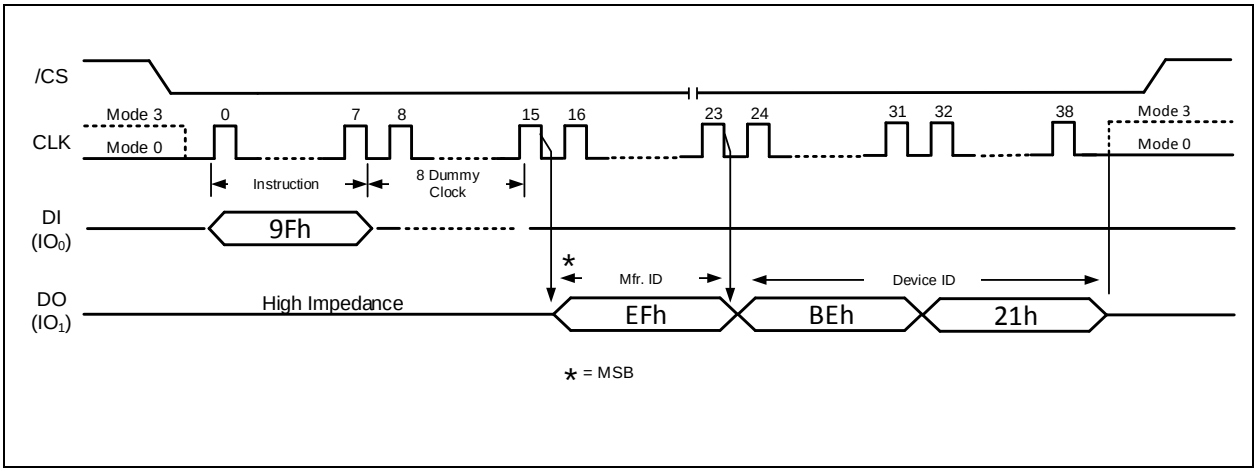


Figure 12. Read JEDEC ID Instruction

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7.2.3 Read Status Register (0Fh / 05h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “0Fh or 05h” into the DI pin on the rising edge of CLK followed by an 8-bit Status Register Address. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 13. Refer to section 7.1-3 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Page Read cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously. The instruction is completed by driving /CS high.

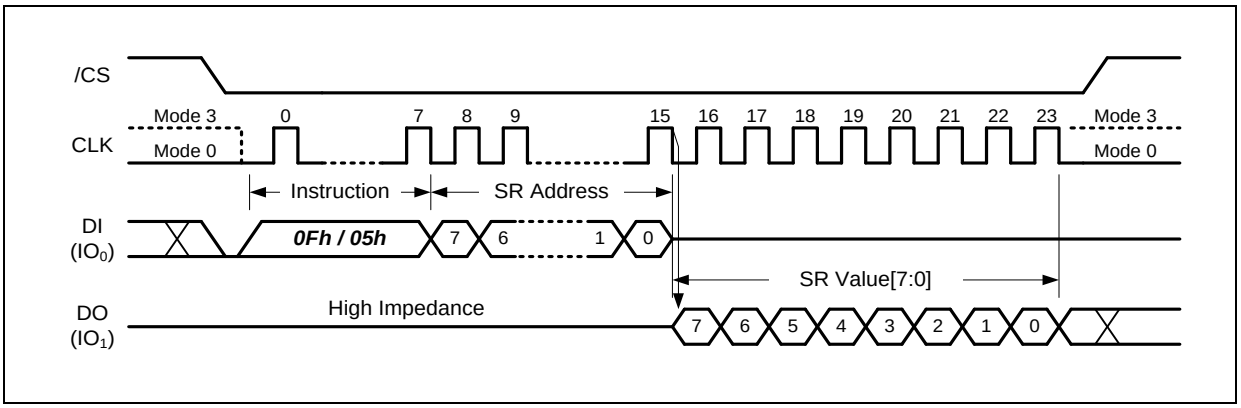


Figure 13. Read Status Register Instruction

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7.2.4 Write Status Register (1Fh / 01h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP[1:0], TB, BP[3:0] and WP-E bit in Status Register-1; OTP-L, OTP-E, SR1-L and ECC-E in Status Register-2, and feature bits in extended Internal ECC feature registers. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

To write the Status Register bits, the instruction is entered by driving /CS low, sending the instruction code "1Fh or 01h", followed by an 8-bit Status Register Address, and then writing the status register data byte as illustrated in Figure 14.

Refer to section 7.1-3 for Status Register descriptions. After power up, factory default for BP[3:0], TB, ECC-E bits are 1, while other bits are 0.

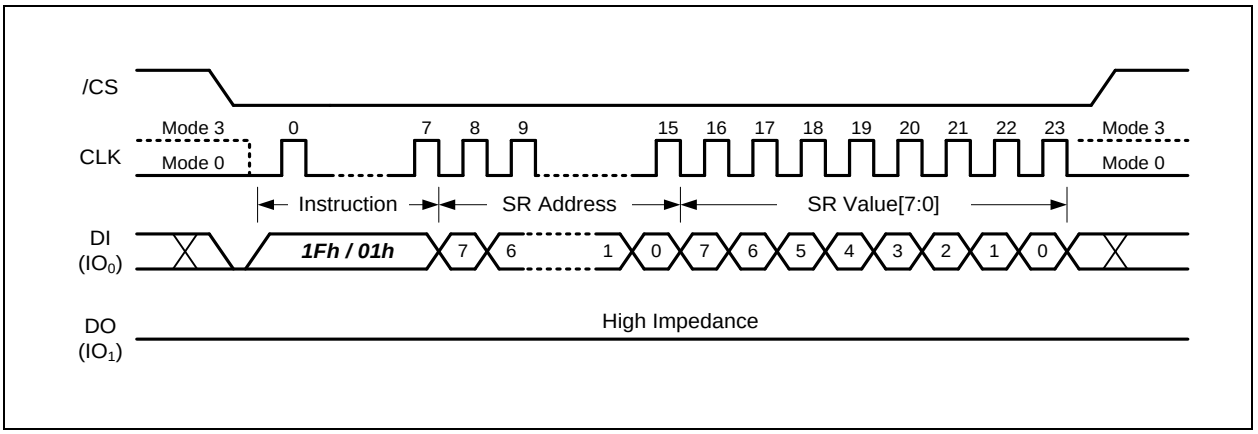


Figure 14. Write Status Register Instruction

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7.2.5 Write Enable (06h)

The Write Enable instruction (Figure 15) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Load Program Data (02h/84h/32h/34h), Program execute and Block Erase instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

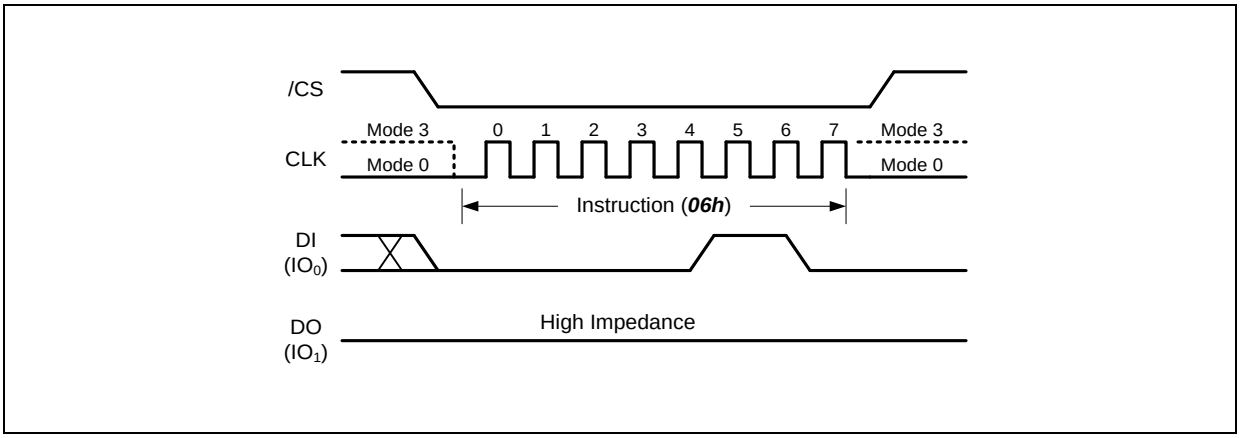


Figure 15. Write Enable Instruction

7.2.6 Write Disable (04h)

The Write Disable instruction (Figure 16) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Page Data Read, Program Execute, Block Erase and Reset instructions.

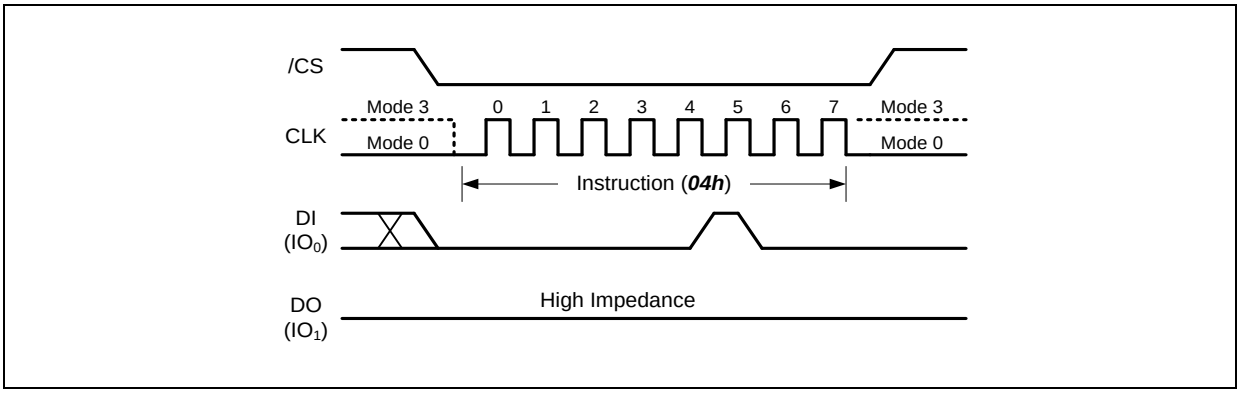


Figure 16. Write Disable Instruction

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7.2.7 Bad Block Management (A1h)

Due to large NAND memory density size and the technology limitation, NAND memory devices are allowed to be shipped to the end customers with certain amount of “Bad Blocks” found in the factory testing. Up to 2% of the memory blocks can be marked as “Bad Blocks” upon shipment, which is a maximum of 20 blocks for W25N01KW. In order to identify these bad blocks, it is recommended to scan the entire memory array for bad block markers set in the factory. A “Bad Block Marker” is a non-FFh data byte stored at Byte 0 of Page 0 for each bad block. An additional marker is also stored in the first byte of the 64-Byte spare area.

W25N01KW offers a convenient method to manage the bad blocks typically found in NAND flash memory after extensive use. The “Bad Block Management” command is initiated by shifting the instruction code “A1h” into the DI pin and followed by the 16-bits “Logical Block Address” and 16-bits “Physical Block Address”. The logical block address is the address for the “bad” block that will be replaced by the “good” block indicated by the physical block address.

A Write Enable instruction must be executed before the device will accept the Bad Block Management instruction (Status Register bit WEL=1). The Bad Block Management instruction is initiated by driving the /CS pin low and shifting the instruction code “A1h” followed by 16-bits LBA (Bad Block address) and the 16-bits PBA (Good Block address). After /CS is driven high to complete the instruction cycle, the self-timed Bad Block Management instruction will commence for a time duration of tPP (See AC Characteristics). While the Bad Block Management cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Bad Block Management cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Bad Block Management cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

Once a Bad Block Management command is successfully executed, the specified LBA-PBA link will be added to the internal Look Up Table (LUT). Up to 20 links can be established in the non-volatile LUT. If all 20 links have been written, the LUT-F bit in the Status Register will become a 1, and no more LBA-PBA links can be established. Therefore, prior to issuing the Bad Block Management command, the LUT-F bit value can be checked or a “Read BBM Look Up Table” command can be issued to confirm if spare links are still available in the LUT.

To guarantee a Sequential Read operation on the first 1,000 blocks, the manufacturer may have used some of the BBM LUT entrees. It is advisable for the user to scan all blocks and keep a table of all manufacturer bad blocks prior to first erase/program operation.

Registering the same address in multiple PBAs is prohibited. It may cause unexpected behavior.

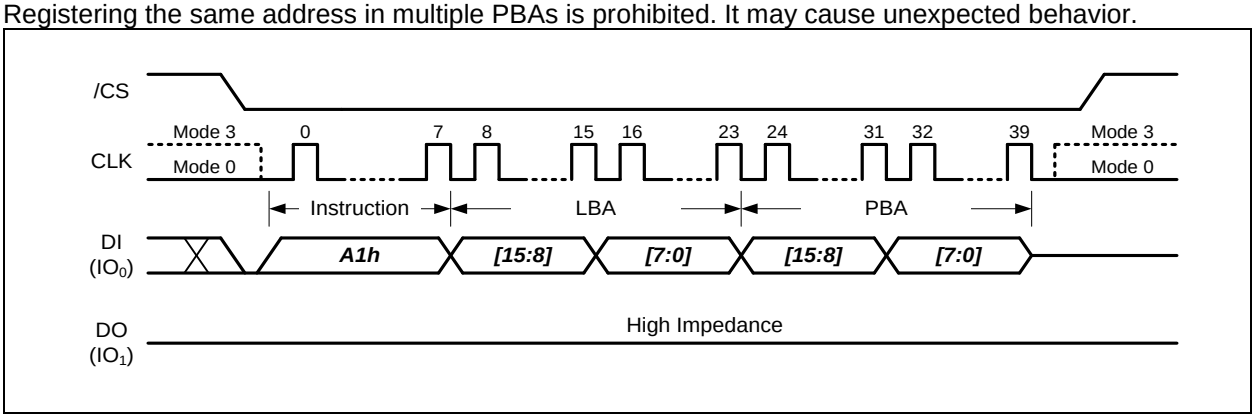


Figure 17. Bad Block Management Instruction

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7.2.8 Read BBM Look Up Table (A5h)

The internal Look Up Table (LUT) consists of 20 Logical-Physical memory block links (from LBA0/PBA0 to LBA19/PBA19). The “Read BBM Look Up Table” command can be used to check the existing address links stored inside the LUT.

The “Read BBM Look Up Table” command is initiated by shifting the instruction code “A5h” into the DI pin and followed by 8-bits dummy clocks, at the falling edge of the 16th clocks, the device will start to output the 16-bits “Logical Block Address” and the 16-bits “Physical Block Address” as illustrated in Figure 19. All block address links will be output sequentially starting from the first link (LBA0 & PBA0) in the LUT. If there are available links that are unused, the output will contain all “00h” data.

The MSB bits LBA [15:14] of each link are used to indicate the status of the link.

LBA[15] (Enable)	LBA[14] (Invalid)	Descriptions
0	0	This link is available to use.
1	0	This link is enabled, and it is a valid link.
1	1	This link was enabled, but it is not valid anymore.
0	1	Not applicable.

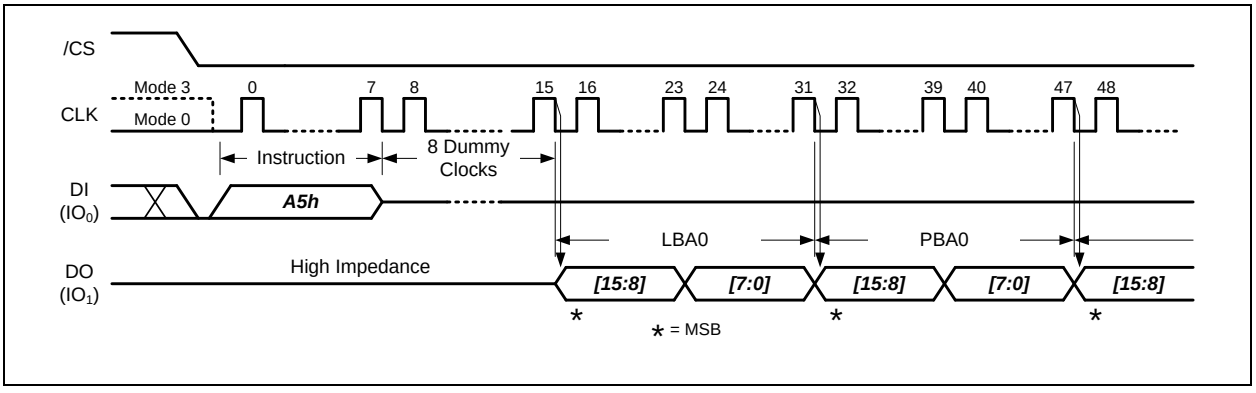


Figure 18. Read BBM Look Up Table Instruction

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7.2.9 Last ECC Failure Page Address (A9h)

To better manage the data integrity, W25N01KW implements internal ECC correction for the entire memory array. When the ECC-E bit in the Status/Configuration Register is set to 1 (also power up default), the internal ECC algorithm is enabled for all Program and Read operations. During a “Program Execute” command for a specific page, the ECC algorithm will calculate the ECC information based on the data inside the 2K-Byte data buffer and write the ECC data into the extra 32-Byte ECC area in the same physical memory page.

During the Read operations, ECC information will be used to verify the data read out from the physical memory array and possible corrections can be made to limited amount of data bits that contain errors. The ECC Status Bits (ECC-1 & ECC-0) will also be set indicating the result of ECC calculation.

The failure page address (or the last page address if it’s multiple pages) can be obtained by issuing the “Last ECC failure Page Address” command. The 16-bits Page Address that contains un-correctable ECC errors will be presented on the DO pin following the instruction code “A9h” and 8-bits dummy clocks on the DI pin.

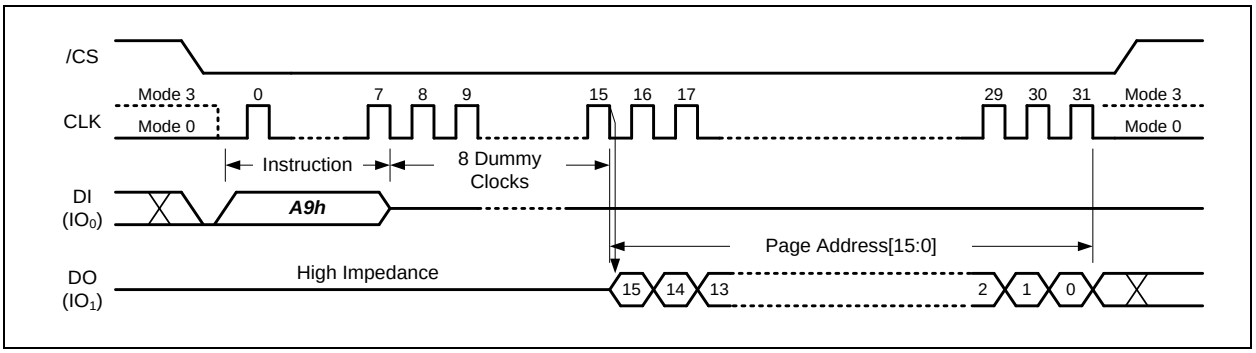


Figure 19. Last ECC Failure Page Address Instruction

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7.2.10 128KB Block Erase (D8h)

The 128KB Block Erase instruction sets all memory within a specified block (64-Pages, 128K-Bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed by the 24-bit page address. The Block Erase instruction sequence is shown in Figure 20.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed block is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits.

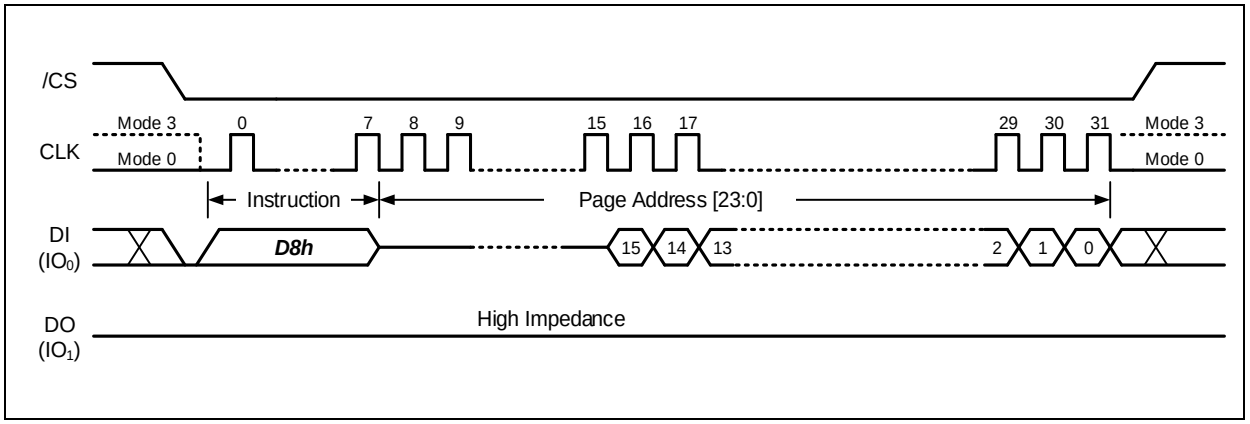


Figure 20. 128KB Block Erase Instruction

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7.2.11 Load Program Data (02h) / Random Load Program Data (84h)

The Program operation allows from one byte to 2,112 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Program operation involves two steps: 1. Load the program data into the Data Buffer. 2. Issue “Program Execute” command to transfer the data from Data Buffer to the specified memory page.

A Write Enable instruction must be executed before the device will accept the Load Program Data Instructions (Status Register bit WEL= 1). The “Load Program Data” or “Random Load Program Data” instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” or “84h” followed by a 16-bit column address (only CA[11:0] is effective) and at least one byte of data into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device. The Load Program Data instruction sequence is shown in Figure 21.

Both “Load Program Data” and “Random Load Program Data” instructions share the same command sequence. The difference is that “Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

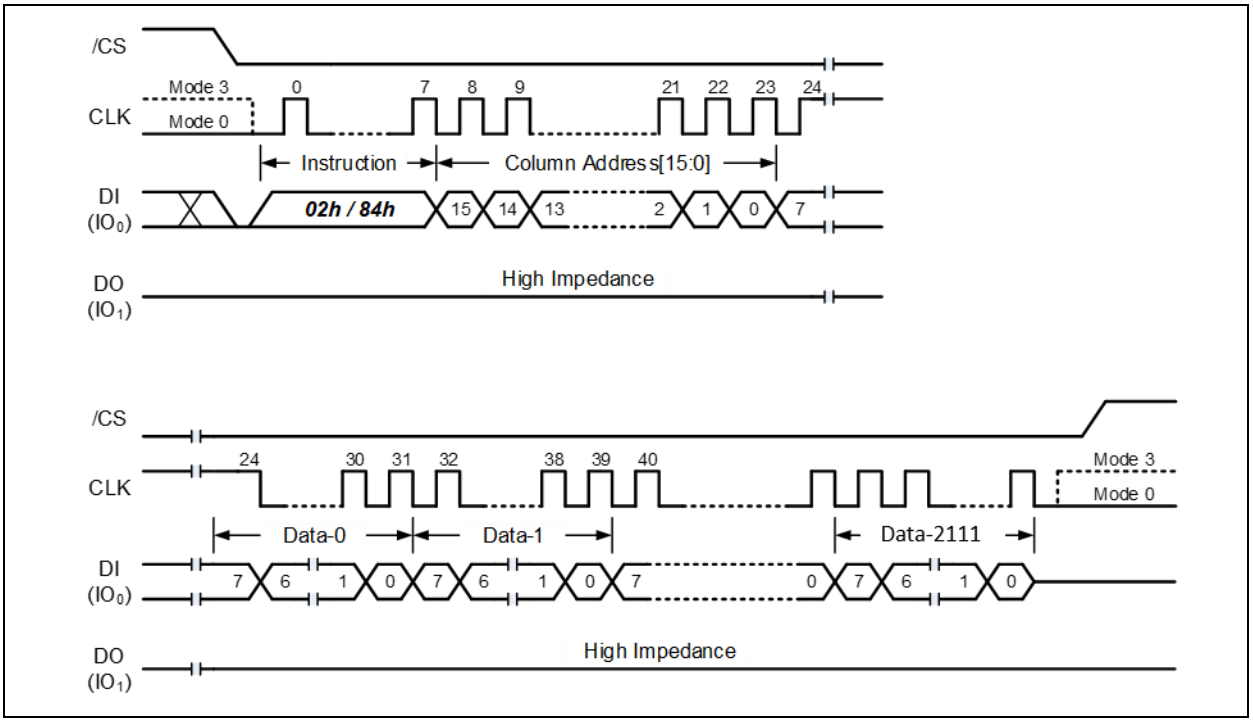


Figure 21. Load / Random Load Program Data Instruction

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7.2.12 Quad Load Program Data (32h) / Quad Random Load Program Data (34h)

The “Quad Load Program Data” and “Quad Random Load Program Data” instructions are identical to the “Load Program Data” and “Random Load Program Data” in terms of operation sequence and functionality. The only difference is that “Quad Load” instructions will input the data bytes from all four IO pins instead of the single DI pin. This method will significantly shorten the data input time when a large amount of data needs to be loaded into the Data Buffer. The instruction sequence is illustrated in Figure 22.

Both “Quad Load Program Data” and “Quad Random Load Program Data” instructions share the same command sequence. The difference is that “Quad Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Quad Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

When WP-E bit in the Status Register is set to a 1, all Quad SPI instructions are disabled.

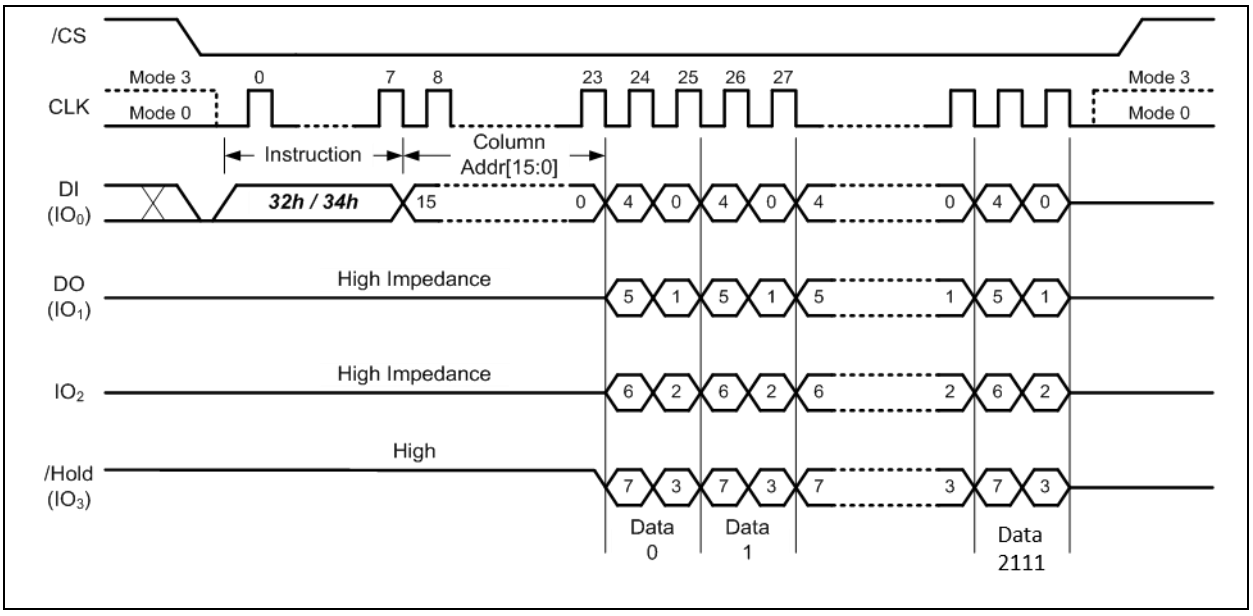


Figure 22. Quad Load / Quad Random Load Program Data Instruction

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7.2.13 Program Execute (10h)

The Program Execute instruction is the second step of the Program operation. After the program data are loaded into the 2,112-Byte Data Buffer (or 2,048 bytes when ECC is enabled), the Program Execute instruction will program the Data Buffer content into the physical memory page that is specified in the instruction. The instruction is initiated by driving the /CS pin low then shifting the instruction code “10h” followed by 24-bit Page Address into the DI pin as shown in Figure 23.

The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. Programming pages out of sequence is prohibited.

After /CS is driven high to complete the instruction cycle, the self-timed Program Execute instruction will commence for a time duration of tpp (See AC Characteristics). While the Program Execute cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Program Execute cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Execute cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits.

Do not cross plane address boundaries to apply the Program Execute operation. The page data read from one plane cannot program to different plane.

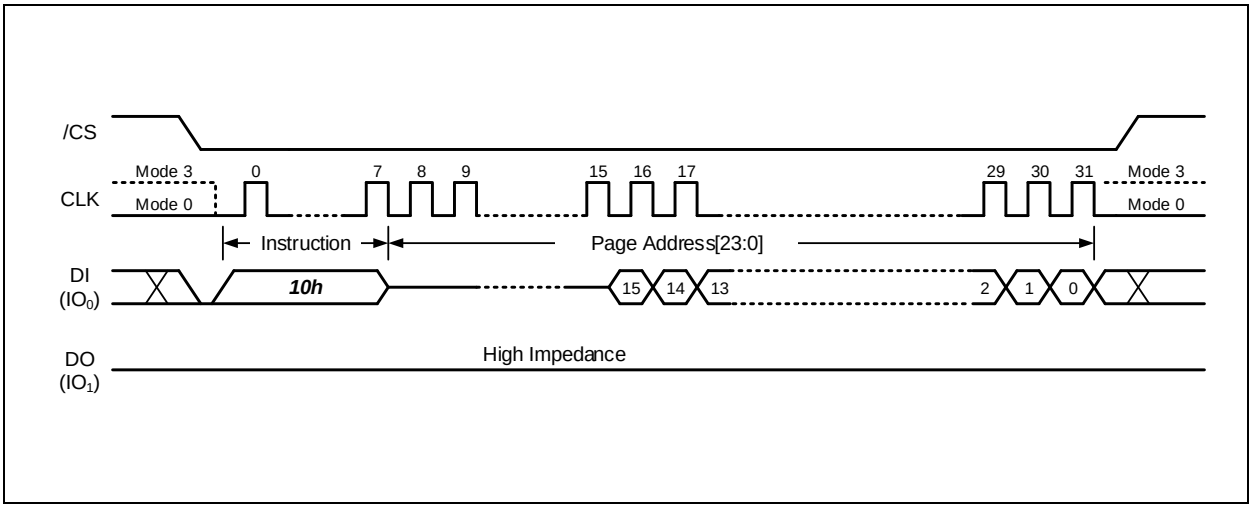


Figure 23. Program Execute Instruction

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7.2.14 Page Data Read (13h)

The Page Data Read instruction will transfer the data of the specified memory page into the 2,112-Byte Data Buffer. The instruction is initiated by driving the /CS pin low then shifting the instruction code “13h” followed by 24-bit Page Address into the DI pin as shown in Figure 24.

After /CS is driven high to complete the instruction cycle, the self-timed Page Data Read instruction will commence for a time duration of tRD (See AC Characteristics). While the Page Data Read cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Data Read cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again.

After the 2,112 bytes of page data are loaded into the Data Buffer, several Read instructions can be issued to access the Data Buffer and read out the data.

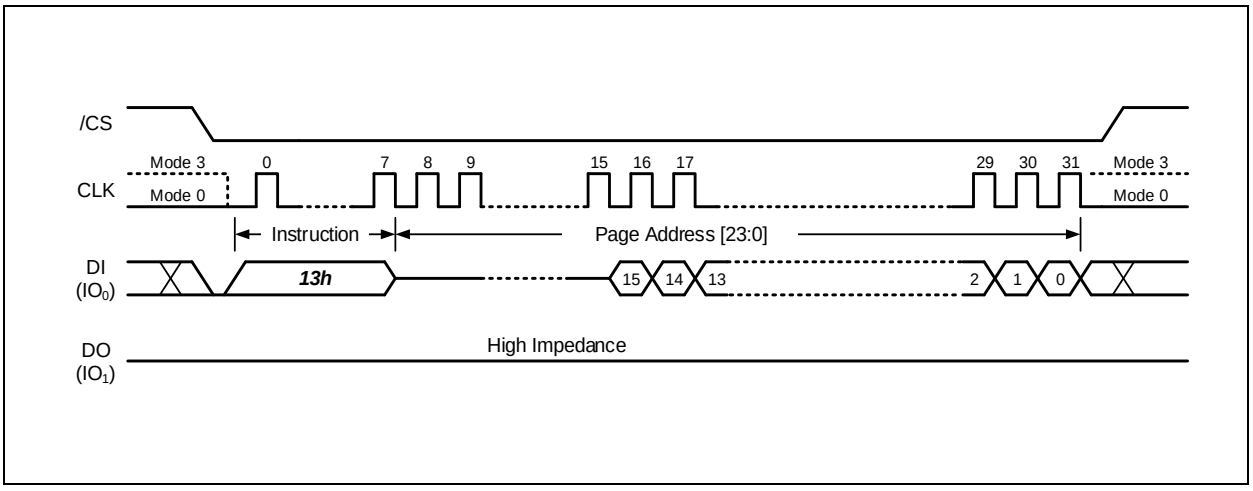


Figure 24. Page Data Read Instruction

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7.2.15 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Read Data instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by the 16-bit Column Address and 8-bit dummy clocks or a 24-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 25 & 26. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond’s NOR flash memory command sequence.

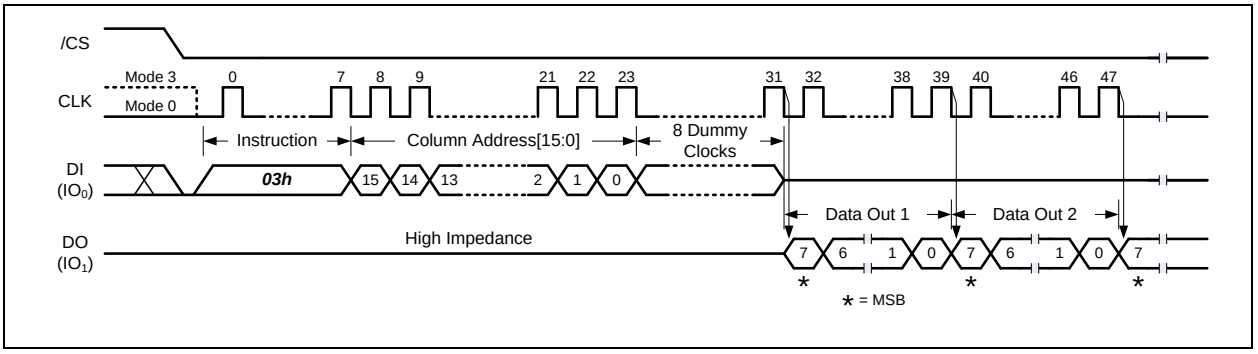


Figure 25. Read Data Instruction (Buffer Read Mode, BUF=1)

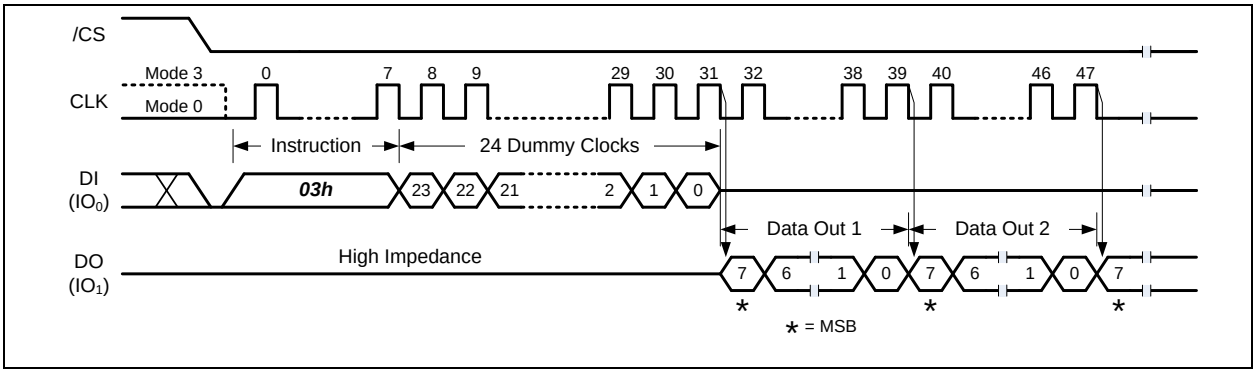


Figure 26. Read Data Instruction (Sequential Read Mode, BUF=0)

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7.2.16 Fast Read (0Bh)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Bh” followed by the 16-bit Column Address and 8-bit dummy clocks or a 32-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

The Fast Read instruction sequence is shown in Figure 27 & 28. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond’s NOR SpiFlash memory command sequence.

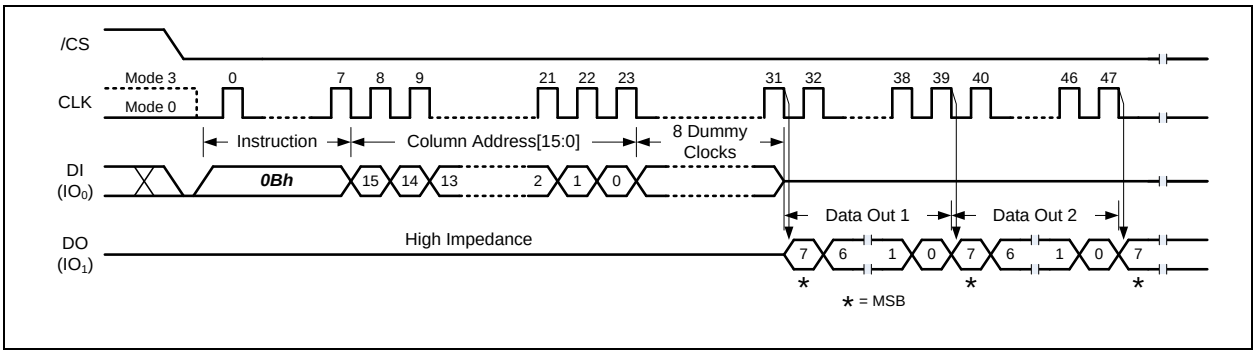


Figure 27. Fast Read Instruction (Buffer Read Mode, BUF=1)

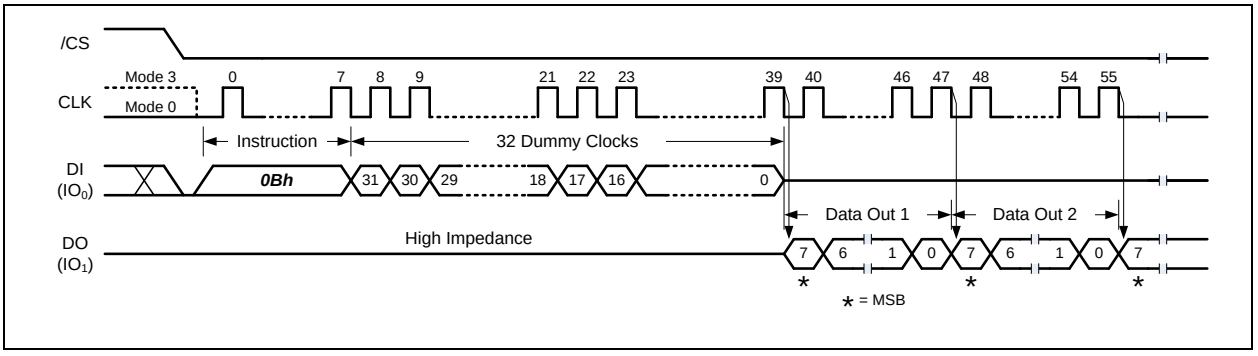


Figure 28. Fast Read Instruction (Sequential Read Mode, BUF=0)

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7.2.17 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices.

The Fast Read Dual Output instruction sequence is shown in Figure 29 & 30. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's NOR SpiFlash memory command sequence.

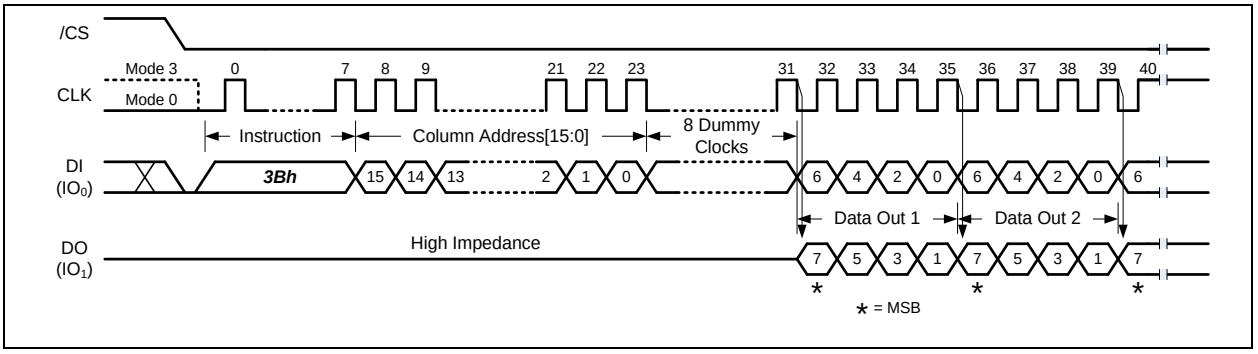


Figure 29. Fast Read Dual Output Instruction (Buffer Read Mode, BUF=1)

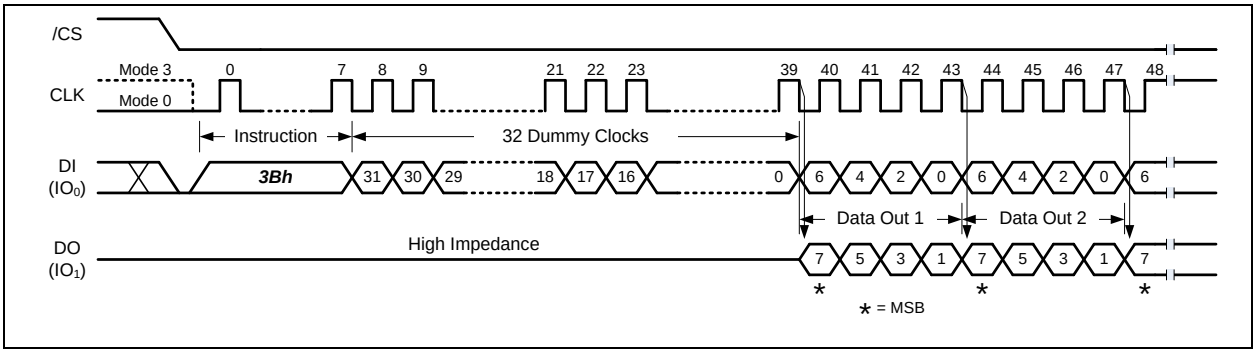


Figure 30. Fast Read Dual Output Instruction (Sequential Read Mode, BUF=0)

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7.2.18 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction sequence is shown in Figure 31 & 32. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's NOR SpiFlash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

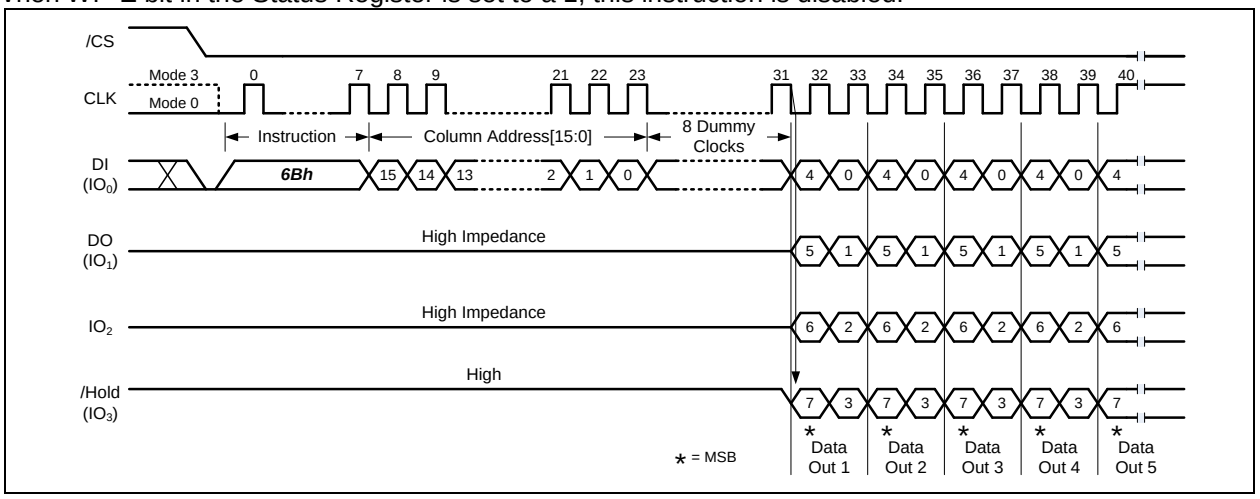


Figure 31. Fast Read Quad Output Instruction (Buffer Read Mode, BUF=1)

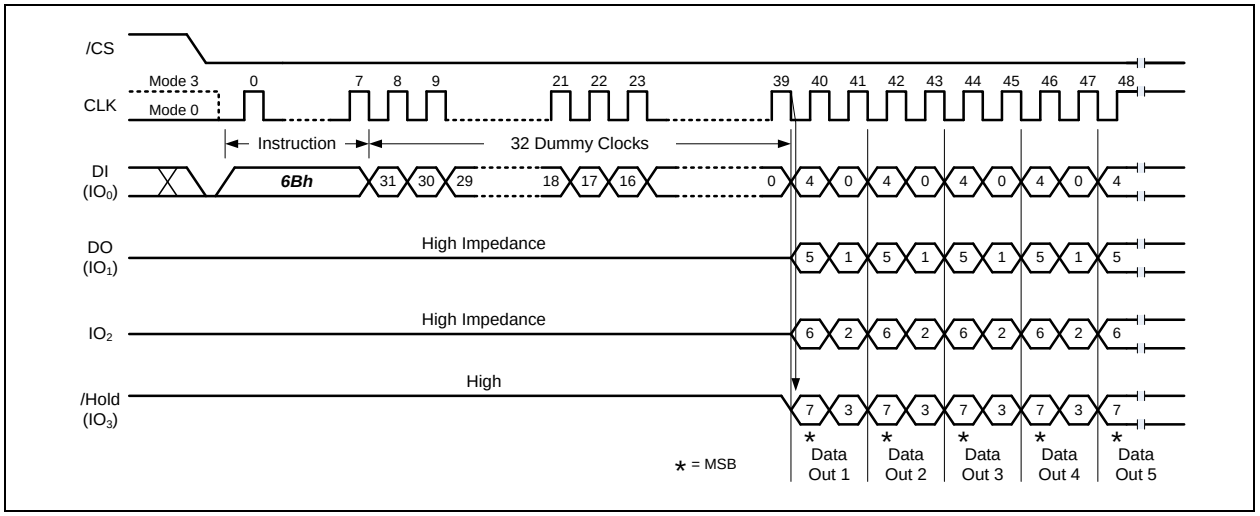


Figure 32. Fast Read Quad Output Instruction (Sequential Read Mode, BUF=0)

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7.2.19 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Fast Read Quad Output instruction sequence is shown in Figure 33 & 34. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's NOR SpiFlash memory command sequence.

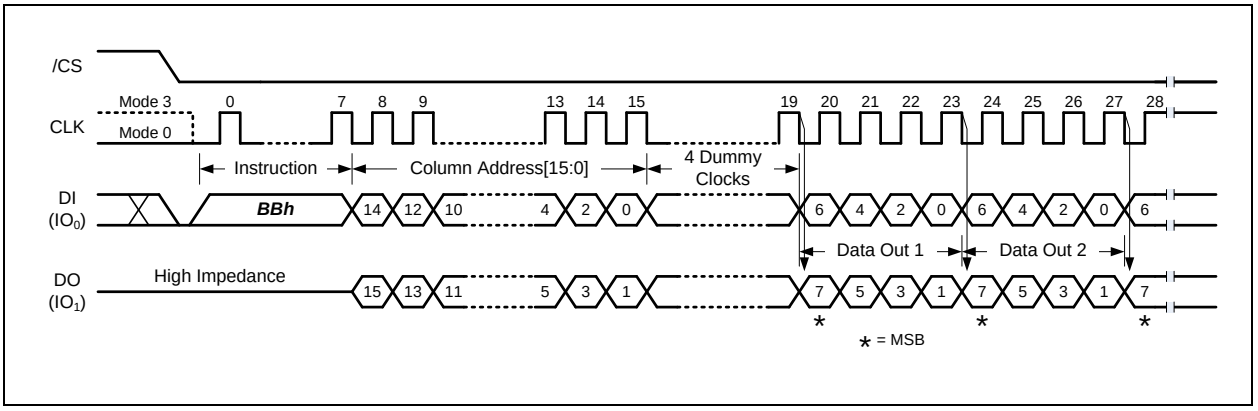


Figure 33. Fast Read Dual I/O Instruction (Buffer Read Mode, BUF=1)

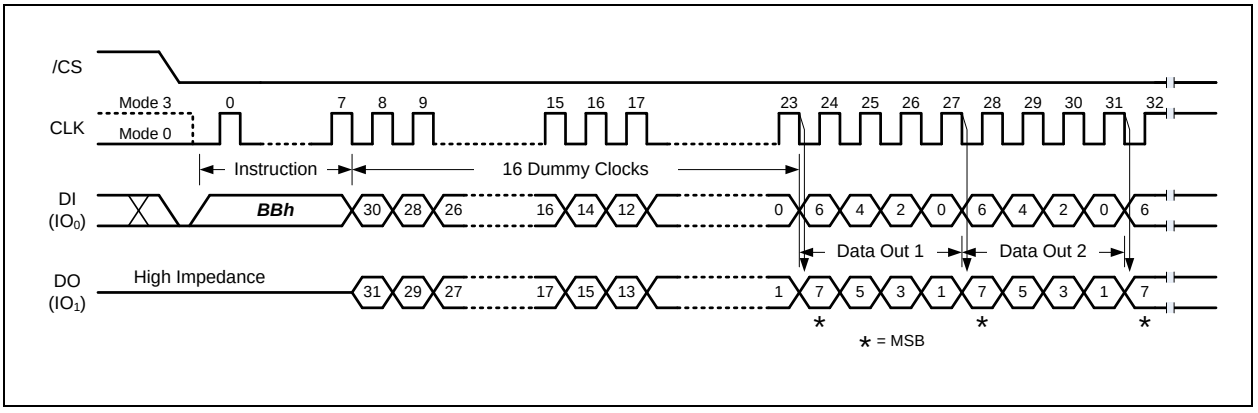


Figure 34. Fast Read Dual I/O Instruction (Sequential Read Mode, BUF=0)

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7.2.20 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Fast Read Quad Output instruction sequence is shown in Figure 35 & 36. When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state. When BUF=0, the device is in the Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's NOR SpiFlash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

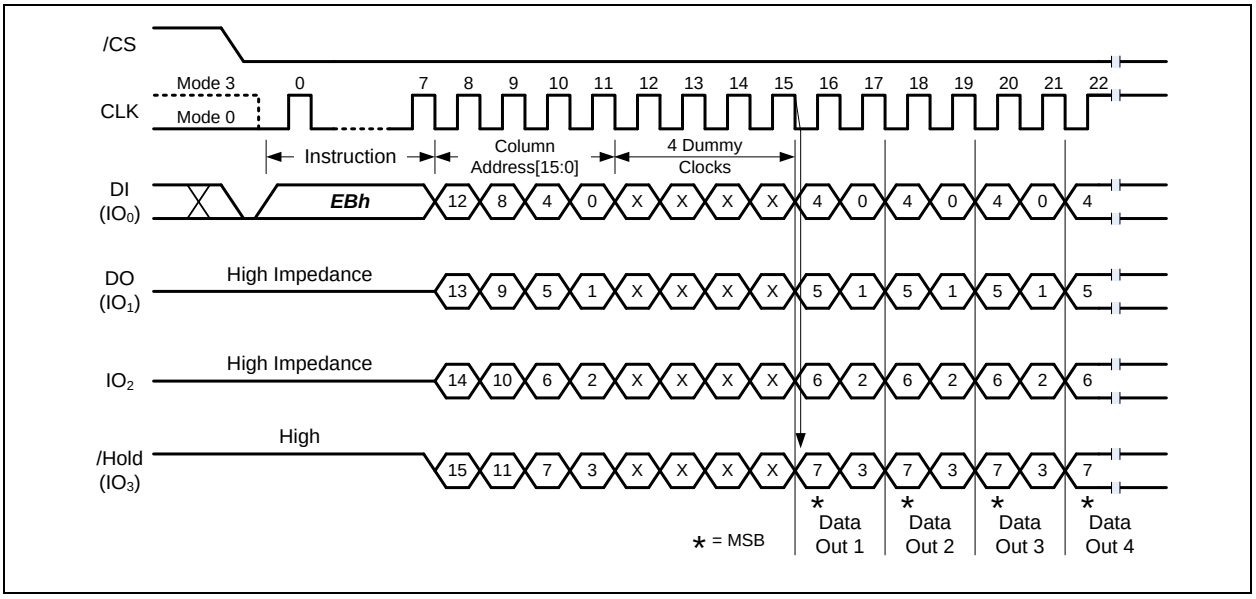


Figure 35. Fast Read Quad I/O Instruction (Buffer Read Mode, BUF=1)

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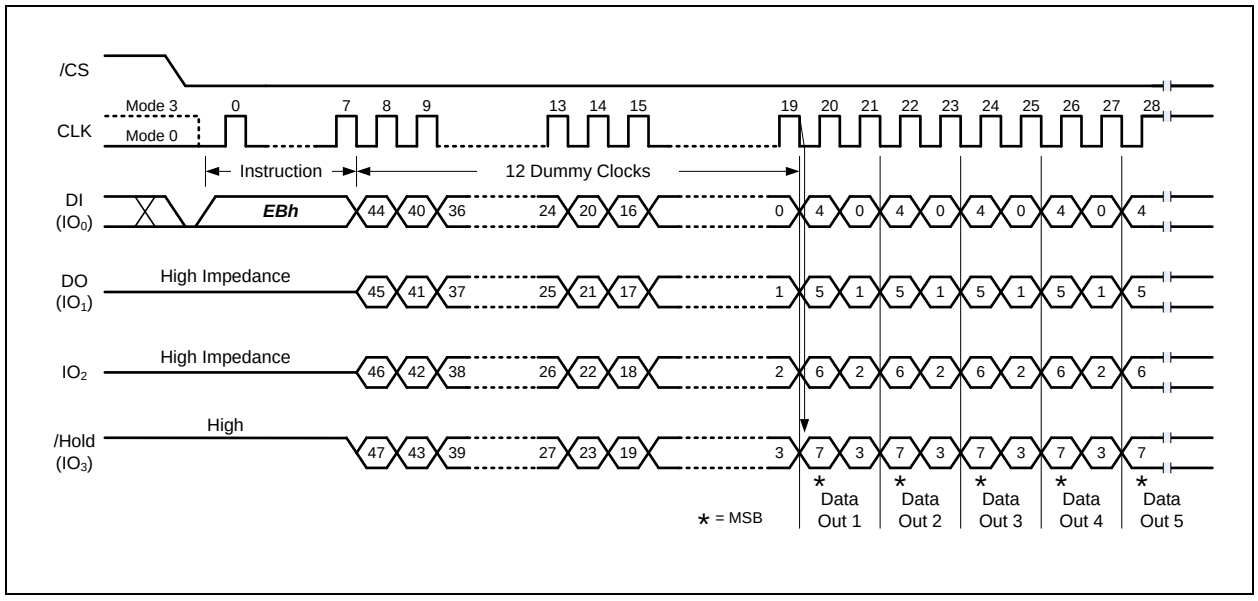


Figure 36. Fast Read Quad I/O Instruction (Sequential Read Mode, BUF=0)

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7.2.22 Accessing Unique ID / Parameter / OTP Pages (OTP-E=1)

In addition to the main memory array, the W25N01KW is also equipped with one Unique ID Page, one Parameter Page, and ten OTP Pages.

Page Address	Page Name	Descriptions	Data Length
00h	Unique ID Page	Factory programmed, Read Only	32-Byte x 16
01h	Parameter Page	Factory programmed, Read Only	256-Byte x 3
02h	OTP Page [0]	Program Only, OTP lockable	2,112-Byte
…	OTP Pages [1:8]	Program Only, OTP lockable	2,112-Byte
0Bh	OTP Page [9]	Program Only, OTP lockable	2,112-Byte

To access these additional data pages, the OTP-E bit in Status Register-2 must be set to “1” first. Then, Read operations can be performed on Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it’s not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

Read Operations

A “Page Data Read” command must be issued followed by a specific page address shown in the table above to load the page data into the main Data Buffer. After the device finishes the data loading (BUSY=0), all Read commands may be used to read the Data Buffer starting from any specified Column Address. Please note all Read commands must now follow the “Buffer Read Mode” command structure (CA[15:0], number of dummy clocks). ECC can also be enabled for the OTP page read operations to ensure the data integrity.

Program and OTP Lock Operations

OTP pages provide the additional space (2K-Byte x 10) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state set in the factory, and can only be programmed (change data from “1” to “0”) until being locked by OTP-L bit in the Configuration/Status Register-2. OTP-E must be first set to “1” to enable the access to these OTP pages, then the program data must be loaded into the main Data Buffer using any “Program Data Load” commands. The “Program Execute” command followed by a specific OTP Page Address is used to initiate the data transfer from the Data Buffer to the OTP page. When ECC is enabled, ECC calculation will be performed during “Program Execute”, and the ECC information will be stored into the 32-Byte parity area.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible. While still in the “OTP Access Mode” (OTP-E=1), user needs to set OTP-L bit in the Configuration/Status Register-2 to “1”, and issue a “Program Execute” command(Page address is “don’t care”). After the device finishes the OTP lock setting (BUSY=0), the user can set OTP-E to “0” to return to the main memory array operation.

SR1-L OTP Lock Operation

The Protection/Status Register-1 contains protection bits that can be set to protect either a portion or the entire memory array from being Programmed/Erased or set the device to either Software Write Protection (WP-E=0) or Hardware Write Protection (WP-E=1). Once the BP[3:0], TB, WP-E bits are set correctly, SRP1 and SRP0 should also be set to “1”s as well to allow SR1-L bit being set to “1” to permanently lock the protection settings in the Status Register-1 (SR1). Similar to the OTP-L setting procedure above, in order to set SR1-L lock bit, the device must enter the “OTP Access Mode” (OTP-E=1) first, and SR1-L bit should be set to “1” prior to the “Program Execute” command(Page address is “don’t care”). Once SR1-L is set to “1” (BUSY=0), the user can set OTP-E to “0” to return to the main memory array operation.

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7.2.23 Parameter Page Data Definitions

The Parameter Page contains 3 identical copies of the 256-Byte Parameter Data. The table below lists all the key data byte locations. All other unspecified byte locations have 00h data as default.

Byte	Descriptions	Values
0~3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4~5	Revision number	00h, 00h
6~7	Feature supported	00h, 00h
8~9	Optional command supported	00h, 00h
10~31	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32~43	Device manufacturer	57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44~63	Device model	57h, 32h, 35h, 4Eh, 30h, 31h, 4Bh, 57h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	EFh
65~66	Date code	00h, 00h
67~79	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80~83	Number of data bytes per page	00h, 08h, 00h, 00h
84~85	Number of spare bytes per page	40h, 00h
86~91	Reserved	00h, 00h, 00h, 00h, 00h, 00h
92~95	Number of pages per block	40h, 00h, 00h, 00h
96~99	Number of blocks per logical unit	00h, 04h, 00h, 00h
100	Number of logical units	01h
101	Number of address bytes	00h
102	Number of bits per cell	01h
103~104	Bad blocks maximum per unit	14h, 00h
105~106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108~109	Block endurance for guaranteed valid blocks	00h, 00h
110	Number of programs per page	04h
111	Reserved	00h
112	Number of ECC bits	00h
113	Number of plane address bits	00h
114	Multi-plane operation attributes	00h
115~127	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
128	I/O pin capacitance, maximum	08h
129~132	Reserved	00h, 00h, 00h, 00h
133~134	Maximum page program time (us)	BCh, 02h

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135~136	Maximum block erase time (us)	10h, 27h
137~138	Maximum page read time (us)	3Ch, 00h
139~163	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h,
164~165	Vendor specific revision number	00h, 00h
166~253	Vendor specific	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
254~255	Integrity CRC	**B5h, 26h**
256~511	Value of bytes 0~255	
512~767	Value of bytes 0~255	
768~2175	Reserved	

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7.2.24 Deep Power-Down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-Down instruction. The lower power consumption makes the Power-Down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 37.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release Power-down / Device ID (ABh) and reset (66h+99h, FFh) instruction, which restores the device to normal operation, will be recognized. The hardware reset by signaling protocol also release the power-down state. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

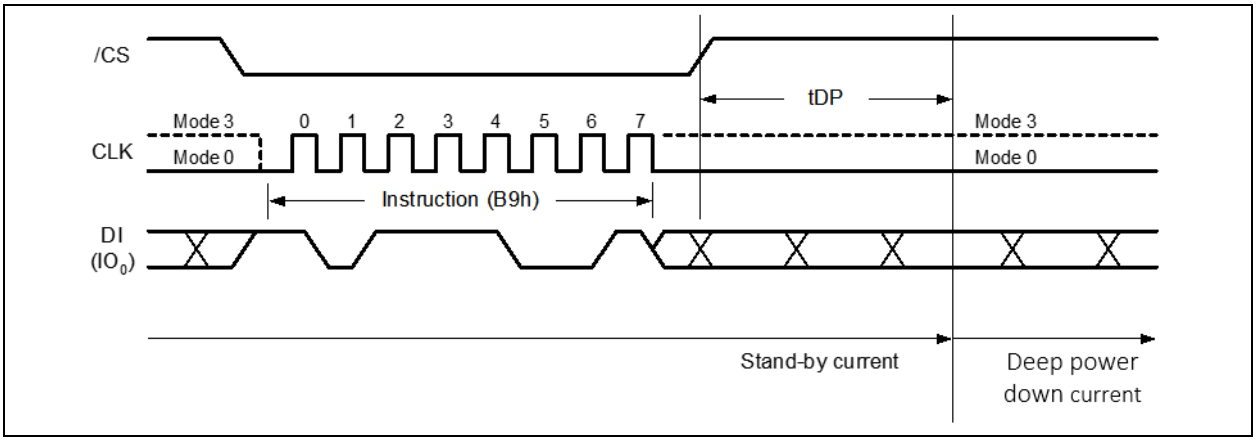


Figure 37. Deep Power-Down Instruction

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7.2.25 Release Power-Down (ABh)

The Release from Power-Down instruction is used to release the device from the power-down state.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in Figure 38. Release from power-down will take the time duration of tRES (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES time duration.

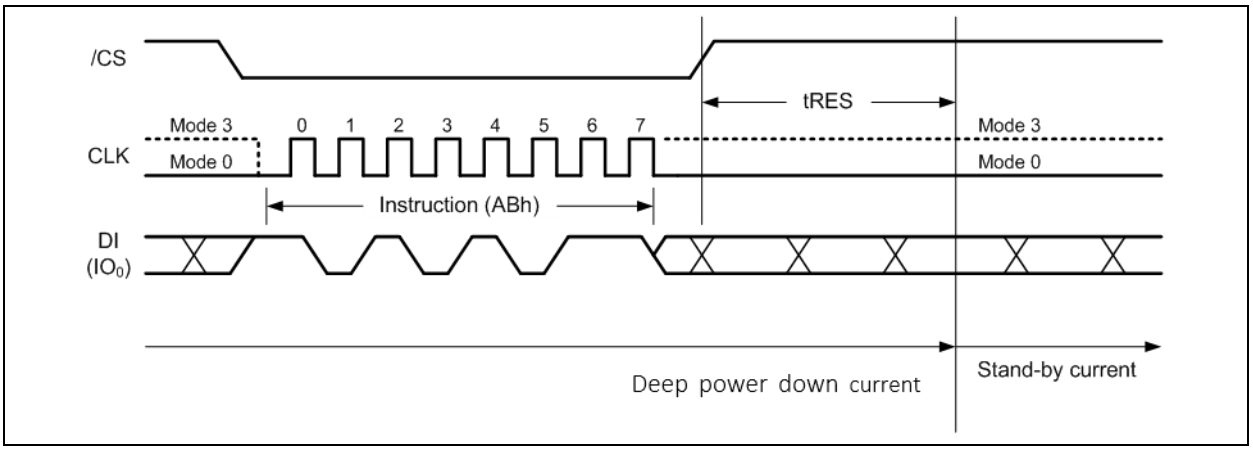


Figure 38. Release Power-down Instruction

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8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings(1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to 2.5	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0 to VCC+2.0	V
Short Circuit Output Current, Ios			5	mA
Storage Temperature	TSTG		–65 to +150	℃
Lead Temperature	TLEAD		See Note (2)	℃
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Standard JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

8.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC		1.7	1.95	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C
		Industrial Plus	-40	+105	°C

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8.3 Power-up Power-down Timing Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}(1)	200		µs
Time Delay Before Write Instruction	t_{PUW}(1)	1		ms
Minimum duration for ensuring initialization will occur	t_{PWD}(1)	1		ms
VCC voltage for ensuring initialization will occur	V_{PWD}(1)		0.7	V

Note: These parameters are characterized only.

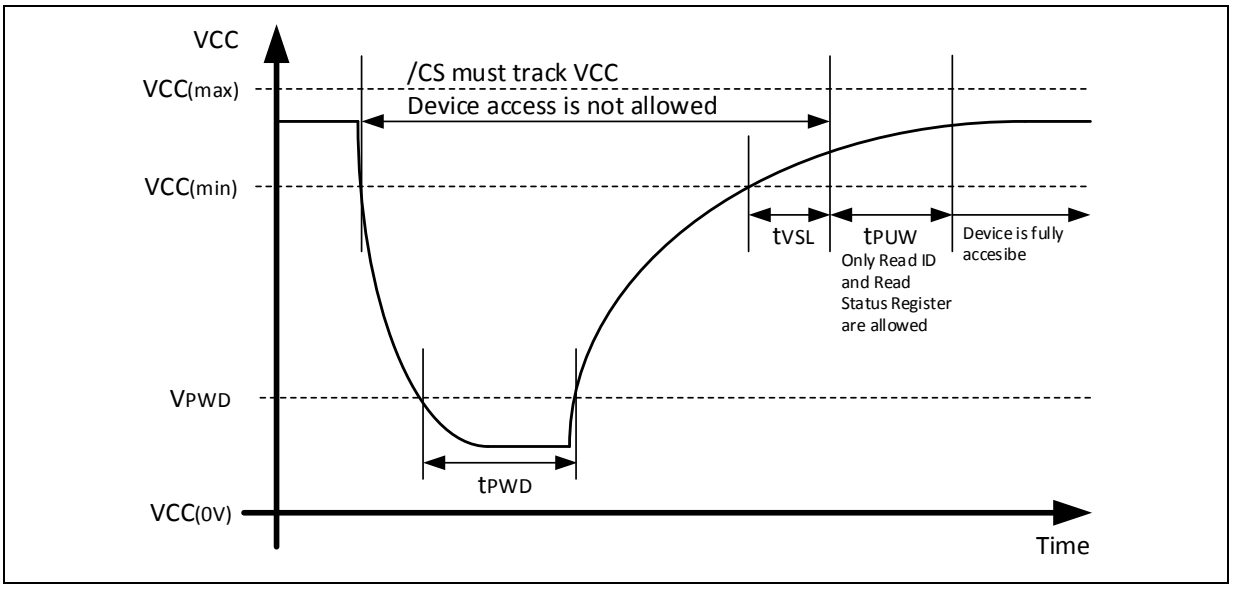


Figure 39. Power-up Timing and Voltage Levels

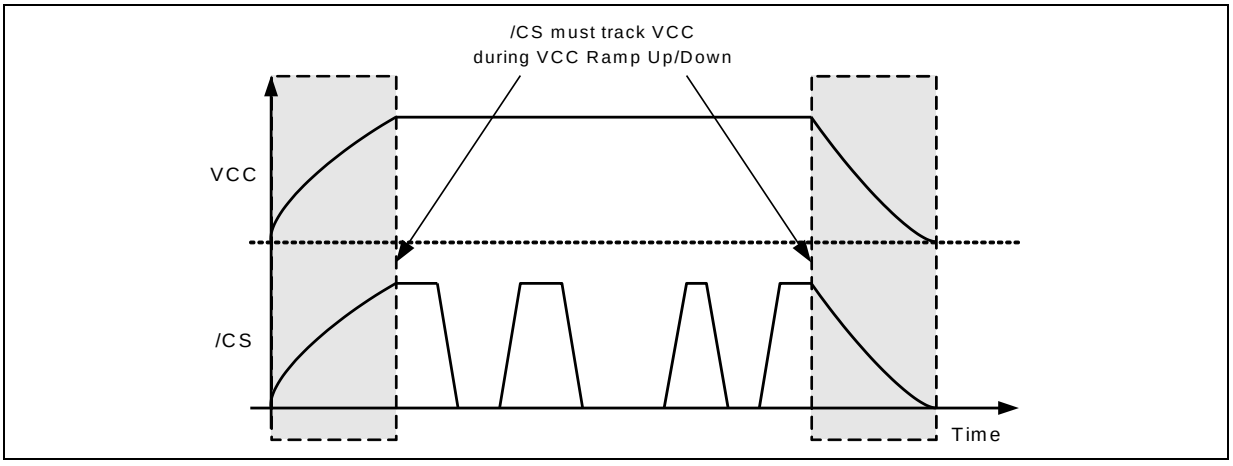


Figure 40. Power-up, Power-Down Requirement

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8.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V(1)			6	pF
Output Capacitance	C_{OUT}(1)	V_{OUT} = 0V(1)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		10	50	µA
Standby Current (105C)	I_{CC1}	/CS = VCC, VIN = GND or VCC		20	100	µA
Deep Power-Down Current	I_{CC2}	/CS = VCC, VIN = GND or VCC			1	µA
Read Current (0Bh) In buffer read mode	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		15	25	mA
Read Current (3Bh) In buffer read mode	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		20	30	mA
Read Current (6Bh) In buffer read mode	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		25	35	mA
Read Current (0Bh) In Sequential Read mode	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		35	45	mA
Read Current (3Bh) In Sequential Read mode	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		40	50	mA
Read Current (6Bh) In Sequential Read mode	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		55	70	mA
Current Page Program	I_{CC4}	/CS = VCC		25	35	mA
Current Block Erase	I_{CC5}	/CS = VCC		25	35	mA
Input Low Voltage	V_{IL}		- 0.3		VCC x 0.2	V
Input High Voltage	V_{IH}		VCC x 0.8		VCC + 0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 100uA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = –100µA	VCC – 0.2			V

Notes:

The typical (TYP) value is tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V.

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8.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC		V

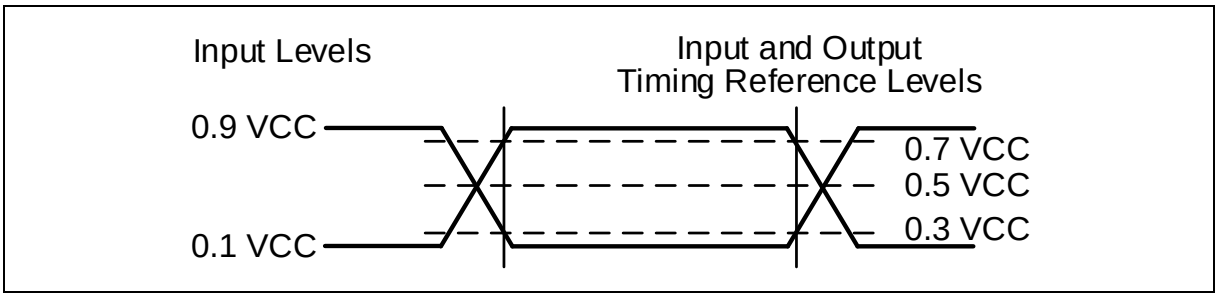


Figure 41. AC Measurement I/O Waveform

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8.6 AC Electrical Characteristics(3)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for all instructions	F_R	f_{C1}	D.C.		104	MHz
Clock High, Low Time for all instructions	t_{CLH}, t_{CLL}(1)		45%Pc			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
/CS Deselect Time (for Array Read → Array Read)	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (for Erase, Program or Read Status Registers → Read Status Registers)	t_{SHSL2}	t_{CSH}	50			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			10	ns
Clock Low to Output Valid	t_{CLQV}	t_V			7	ns
Output Hold Time	t_{CLQX}	t_{HO}	2			ns
/HOLD Active Setup Time relative to CLK	t_{HLCH}		5			ns
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns
/CS High to Deep Power-Down Mode	t_{DP}(2)				3	us
/CS High to Standby Mode (Release Deep Power-Down Mode)	t_{RES}(2)				1.5	ms

Continued – next page

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AC Electrical Characteristics (cont'd)

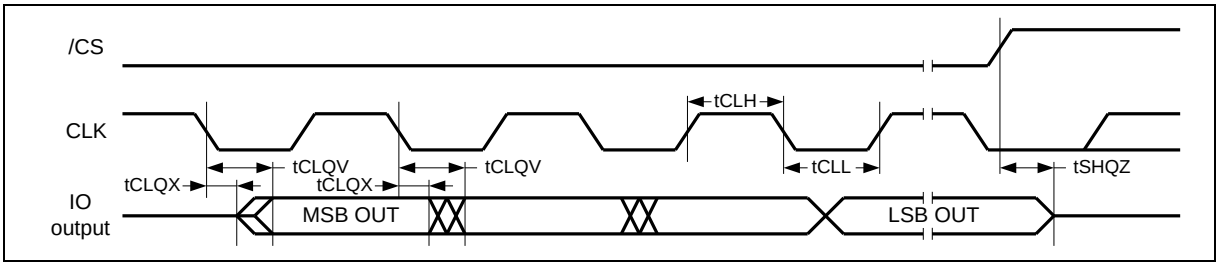
DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	t_{HHQX}(2)	t_{LZ}			7	ns
/HOLD to Output High-Z	t_{HLQZ}(2)	t_{HZ}			12	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}		100			ns
Status Register Write Time	t_W				50	ns
/CS High to next Instruction after Reset during Page Data Read / Program Execute / Block Erase	t_{RST}(2)				5/10/500	µs
/CS High to next instruction after Reset with page 0 data load option	t_{RST2}				100	us
Read Page Data Time (ECC disabled)	t_{RD1}				25	µs
Read Page Data Time (ECC enabled)	t_{RD2}			45	60	µs
Sequential Read Stop to Device Ready Time	t_{RDSR}				7	us
Page Program and OTP Lock Time	tpp			340	700	us
Block Erase Time	t_{BE}			2.5	10	ms
Number of partial page programs	NoP				4	times
Reset Signaling Protocol /CS Low Time	tCSL		500			ns
Reset Signaling Protocol /CS High Time	tCSH		500			ns
Reset Signaling Protocol data in Setup Time	tRPS		5			ns
Reset Signaling Protocol data in Hold Time	tRPH		5			ns

Notes:

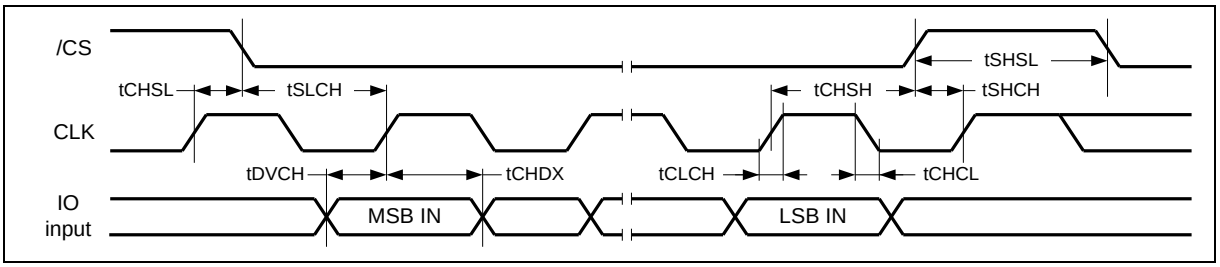
1. Clock high + Clock low must be less than or equal to Pc. PC = 1/fc1(max)
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. The typical (TYP) spec is tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V.
4. The product which re-loads page0 data after Reset takes tRST + tRD busy time.
5. AC electrical characteristics is based on default setting of ODS.

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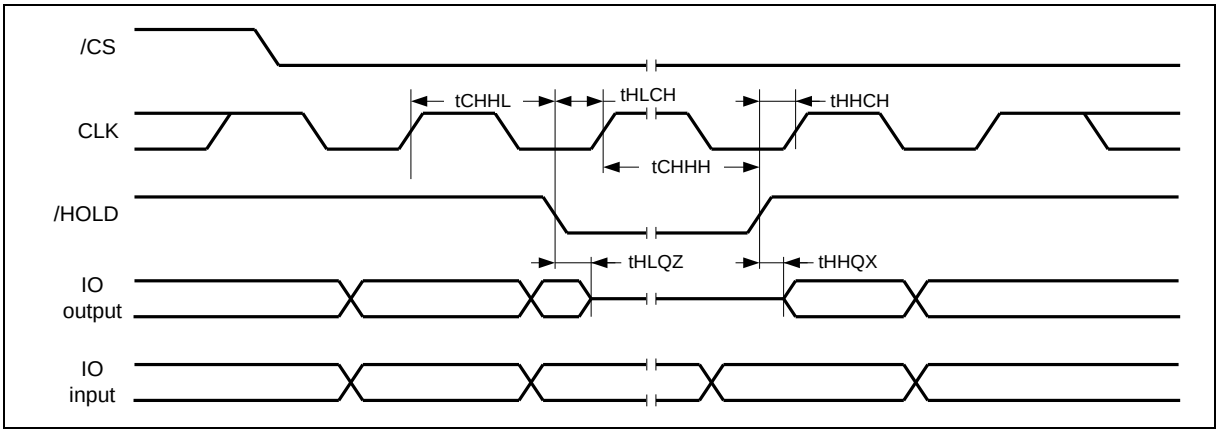
8.7 Serial Output Timing



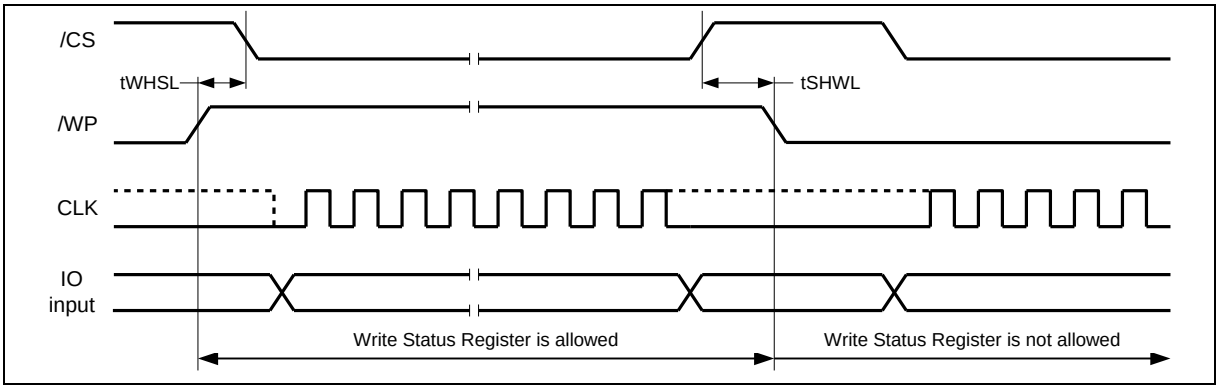
8.8 Serial Input Timing



8.9 /HOLD Timing



8.10 /WP Timing



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9. INVALID BLOCK MANAGEMENT

9.1 Invalid Blocks

The W25N01KW may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks (See Table 12.1). An invalid block is defined as blocks that contain on-chip ECC uncorrectable bad bits. The first eight blocks, block 0 to block 7 and the last four blocks, block 1020 to block 1023 are guaranteed to be valid blocks at the time of shipment with on-chip ECC enabled.

Parameter	Symbol	Min	Max	Unit
Number of valid blocks	Nvb	1004	1024	blocks

Table 9-1 Valid Block Number

9.2 Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain uncorrectable bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The W25N01KW has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased, and invalid blocks are permanently marked. The mark information cannot be erased. All initial invalid blocks are marked with non-FFh at the 1st one byte of main array and the 1st byte of spare area on the 1st page. It should be checked for invalid blocks by reading the marked locations and create a table of initial invalid blocks as following flow chart.

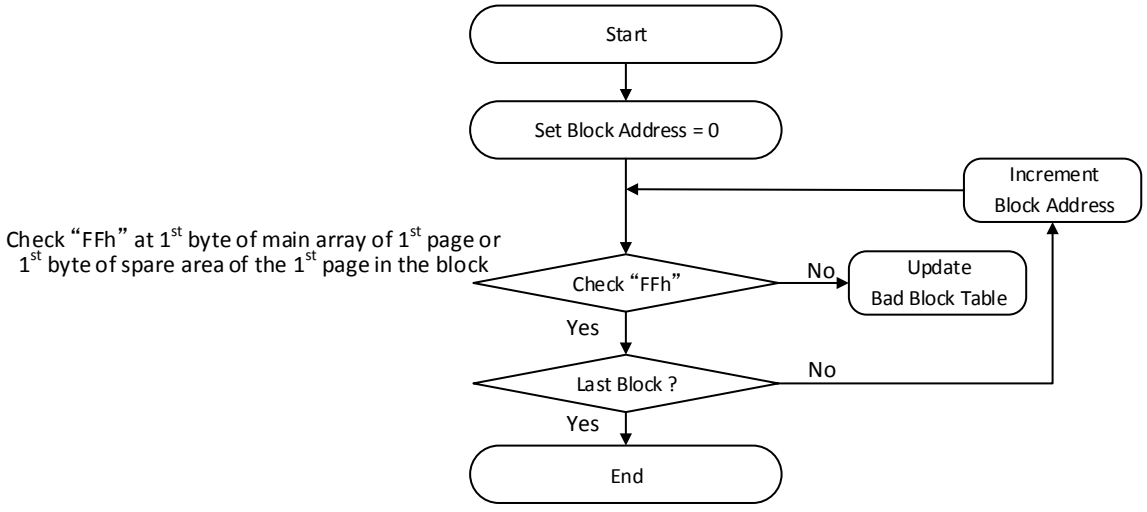


Figure 42. Flow Chart of Create Initial Invalid Block Table

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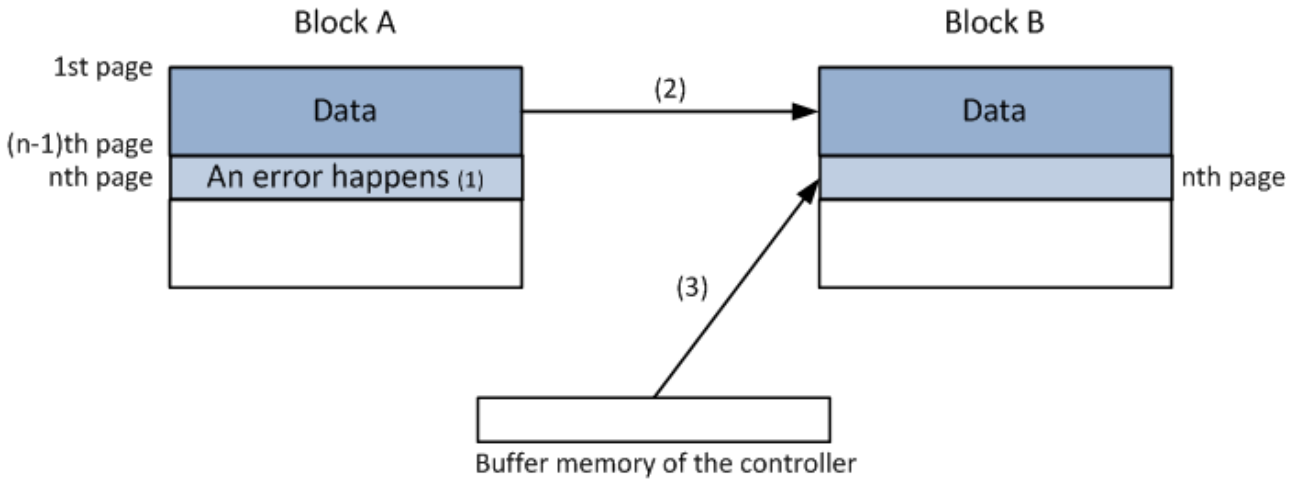
9.3 Error in Operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each read, program and erase operation, check the Cumulative ECC Status, P-FAIL and E-FAIL bit to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm.

Operation	Detection and recommended procedure
Erase	Status register read after erase, check E-FAIL bit → Block Replacement
Program	Status register read after program, check P-FAIL bit → Block Replacement
Read	Status register read, check Cumulative ECC Status → ECC correction

Table 9-2 Block Failure



Note:

1. **An error happens in the nth page of block A during program or erase operation.**
2. **Copy the data in block A to the same location of block B which is valid block.**
3. **Copy the nth page data of block A in the buffer memory to the nth page of block B**
4. **Creating or updating bad block table for preventing further program or erase to block A**

.

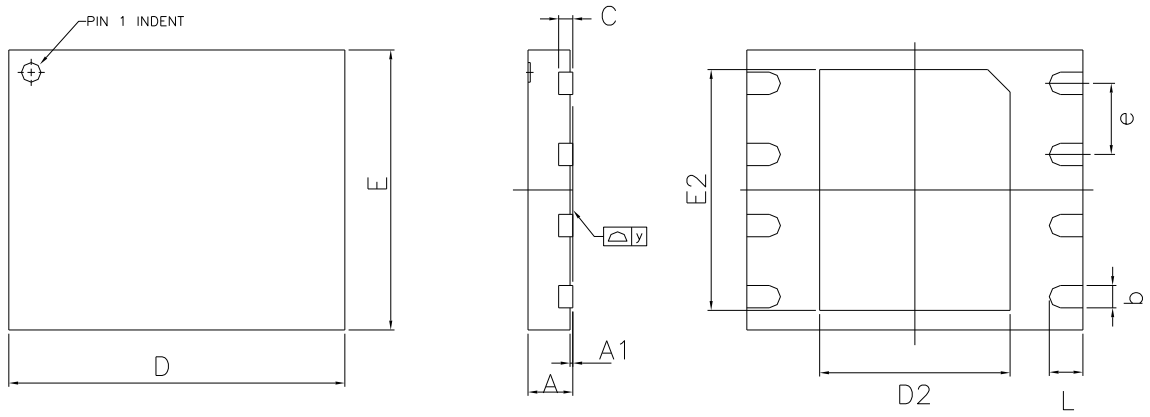
9.4 Addressing in Program Operation

The pages within the block have to be programmed sequentially from LSB (least significant bit) page to the MSB (most significant bit) within the block. The LSB is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.

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10. PACKAGE SPECIFICATIONS

10.1 8-Pad WSON 6x5-mm (Package Code ZP)



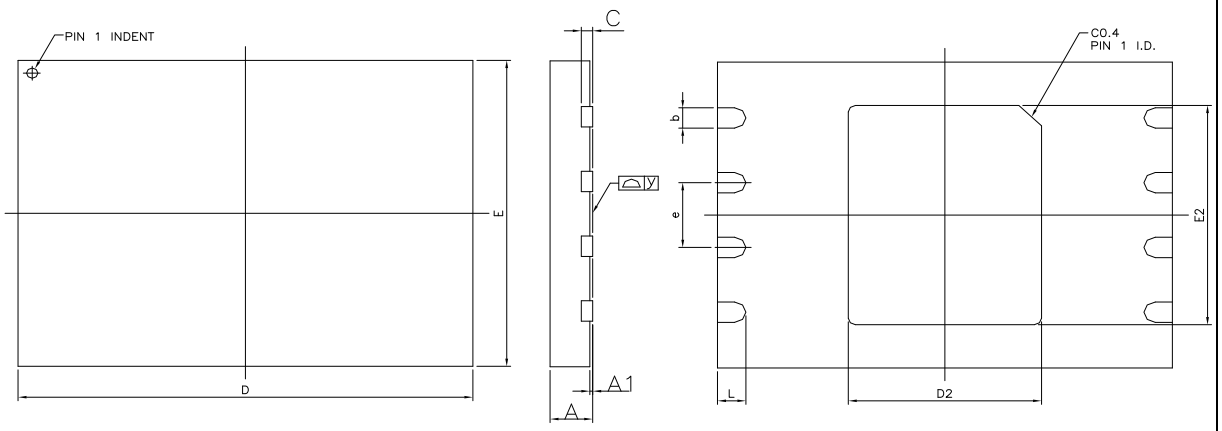
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF	---	---	0.008 REF	---
D	5.90	6.00	6.10	0.232	0.236	0.240
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	4.25	4.30	4.35	0.167	0.169	0.171
e	1.27 BSC			0.050 BSC		
L	0.55	0.60	0.65	0.022	0.024	0.026
y	0.00	---	0.075	0.000	---	0.003

Notes:

The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.

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10.2 8-Pad WSON 8x6-mm (Package Code ZE)



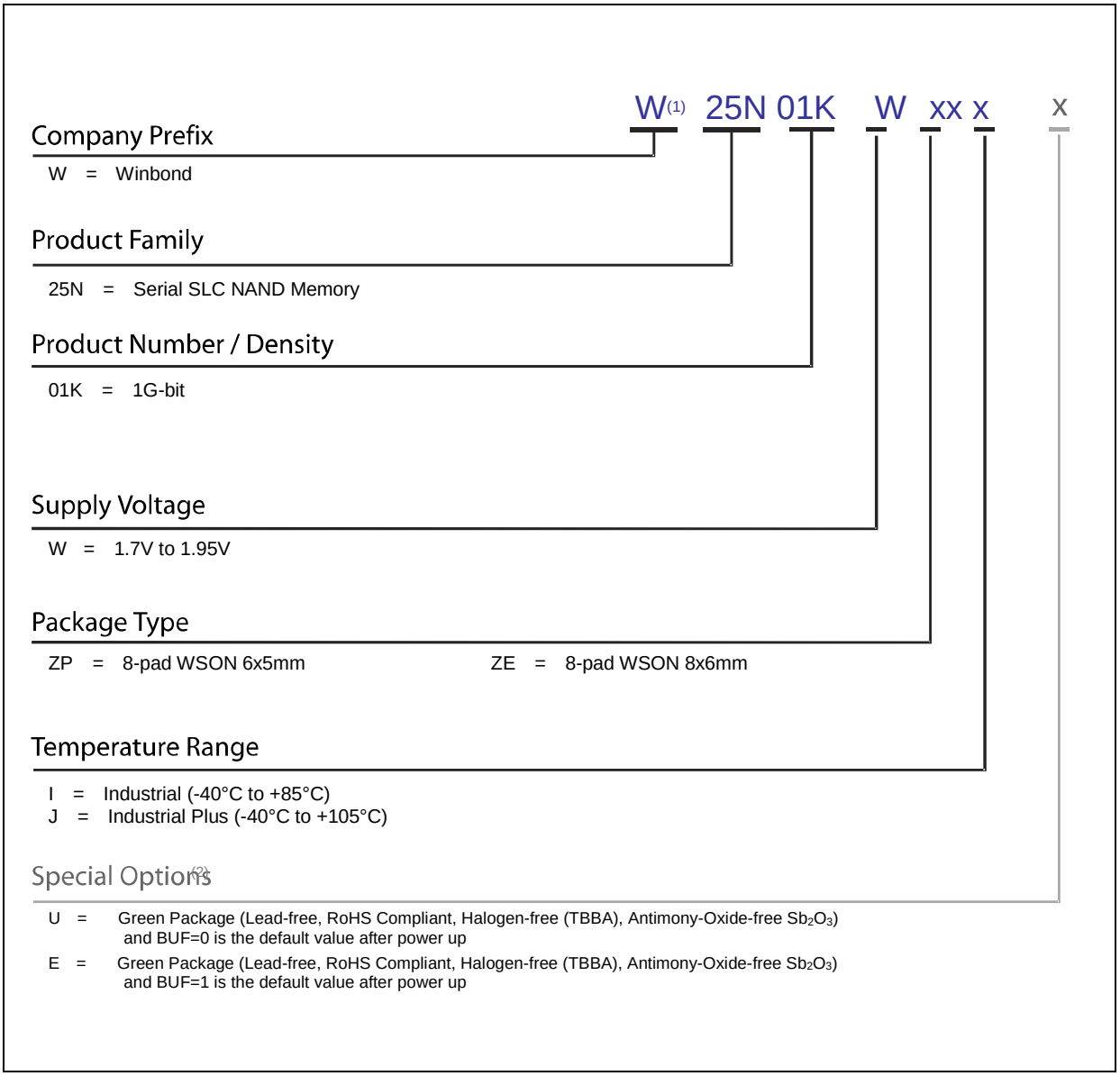
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF	---	---	0.008 REF	---
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	5.90	6.00	6.10	0.232	0.236	0.240
E2	4.25	4.30	4.35	0.167	0.169	0.171
e	---	1.27	---	---	0.050	---
L	0.45	0.50	0.55	0.018	0.020	0.022
y	0.00	---	0.050	0.000	---	0.002

Notes:

The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.

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11. ORDERING INFORMATION



Notes:

1. The “W” prefix is not included on the part marking.
2. Standard bulk shipments are in tray for WSON and TFBGA packages. For other packing options, please specify when placing orders.

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11.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25N01KW QspiNAND Memory. Please contact Winbond for specific availability by density and package type. Winbond QspiNAND memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 11-digit number.

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
ZP WSON-8 6x5mm	1G-bit	W25N01KWZPIU	25N01KWZPIU
ZE WSON-8 8x6mm	1G-bit	W25N01KWZEIU	25N01KWZEIU

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
ZP WSON-8 6x5mm	1G-bit	W25N01KWZPJU	25N01KWZPJU
ZE WSON-8 8x6mm	1G-bit	W25N01KWZEJU	25N01KWZEJU

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
ZP WSON-8 6x5mm	1G-bit	W25N01KWZPIE	25N01KWZPIE
ZE WSON-8 8x6mm	1G-bit	W25N01KWZEIE	25N01KWZEIE

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
ZP WSON-8 6x5mm	1G-bit	W25N01KWZPJE	25N01KWZPJE
ZE WSON-8 8x6mm	1G-bit	W25N01KWZEJE	25N01KWZEJE

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12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	2023/12/01	All	New create preliminary datasheet
B	2024/01/04	All	Remove the preliminary information
C	2024/01/11	21	Update the typo in chapter 6.3.1
D	2024/02/21	4	Update the typo in chapter 5.1.5
E	2024/08/09	6 12, 56 32, 33	Update the endurance spec from 60,000 to 100,000 Update the information for deep power down Update the typo in figure 11
F	2025/12/22	63	Update the tPP typical spec from 400us to 340us

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