# 1.8V 1G-BIT
# SERIAL SLC NAND FLASH MEMORY
# DUAL/QUAD SPI WITH 166MHZ STR & 80MHZ DTR
# BUFFER READ & CONTINUOUS READ

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# 1. GENERAL DESCRIPTIONS

The W25N01JW (1G-bit) Serial SLC NAND Flash Memory provides a storage solution for systems with limited space, pins and power. The W25N SpiFlash family incorporates the popular SPI interface and the traditional large NAND non-volatile memory space. The device operates on a single 1.70V to 1.95V power supply with current consumption as low as 25mA active and 10µA for standby. All W25N SpiFlash family devices are offered in space-saving packages which were impossible to use in the past for the typical NAND flash memory.

The W25N01JW 1G-bit memory array is organized into 65,536 programmable pages of 2,048-Byte each. The entire page can be programmed at one time using the data from the 2,048-Byte internal buffer. Pages can be erased in groups of 64 (128KB block erase). The W25N01JW has 1,024 erasable blocks.

The W25N01JW supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 166MHz are supported allowing equivalent clock rates of 332MHz (166MHz x 2) for Dual I/O and 664MHz (166MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. The W25N01JW adds support for DTR (Double Transfer Rate) commands that transfer addresses and read data on both edges of the clock.

The W25N01JW provides a new Continuous Read Mode that allows for efficient access to the entire memory array with a single Read command. This feature is ideal for code shadowing applications.

A Hold pin, Write Protect pin and programmable write protection, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID, Unique ID page, parameter page and ten 2,048-Byte OTP pages. To provide better NAND flash memory manageability, user configurable internal ECC, Bad block management are also available in W25N01JW.

# 2. FEATURES

- **New W25N Family of SpiFlash Memories**
  - W25N01JW: 1G-bit / 128M-Byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold,
  - Dual SPI: CLK, /CS, $IO_0$, $IO_1$, /WP, /Hold
  - Quad SPI: CLK, /CS, $IO_0$, $IO_1$, $IO_2$, $IO_3$
  - Compatible SPI Serial Flash commands
- **Highest Performance Serial NAND Flash**
  - 166MHz Standard/Dual/Quad SPI clocks
  - 332/664MHz equivalent Dual/Quad SPI
  - DTR (Dual Transfer Rate) up to 80MHz
  - 80MB/s continuous data transfer rate
  - Fast Program/Erase performance
  - 100,000 erase/program cycles
  - 10-year data retention
- **Efficient "Continuous Read Mode"(1)**
  - Alternative method to the Buffer Read Mode
  - No need to issue "Page Data Read" between Read commands
  - Allows direct read access to the entire array
- **Low Power, Wide Temperature Range**
  - Single 1.70 to 1.95V power supply
  - 25mA active, 10µA standby current
  - -40°C to +85/+105°C operating range
- **Flexible Architecture with 128KB blocks**
  - Uniform 128K-Byte Block Erase
  - Flexible page data load methods
- **Advanced Features**
  - On-chip 1-Bit ECC for memory array
  - ECC status bits indicate ECC results
  - Bad Block Management and LUT(2) access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Unique ID and Parameter page(3)
  - Ten 2KB OTP pages(4)
- **Space Efficient Packaging**
  - 8-pad WSON 8x6-mm
  - 16-pin SOIC-300mil
  - 24-ball TFBGA 8x6-mm
  - Contact Winbond for other package options

**Notes:**

1. Only the Read command structures are different between the "Continuous Read Mode (BUF=0)" and the "Buffer Read Mode (BUF=1)", all other commands are identical
   W25N01JWxxxG: Default BUF=1 after power up
   W25N01JWxxxT: Default BUF=0 after power up
2. LUT stands for Look-Up Table
3. Please refer to 8.2.38 and 8.2.39 for detail information
4. OTP pages can only be programmed
5. Endurance specification is based on the on-chip ECC or 1bit/528 byte ECC(Error Correcting Code)



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# 3. PACKAGE TYPES AND PIN CONFIGURATIONS

W25N01JW is offered in an 8-pad WSON 8x6-mm (package code ZE), 160pin SOIC-300mil (package code SF), and 24-ball 8x6-mm TFBGA (package code TB) packages as shown in Figure 3-1, 3-2 and 3-3 respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

## 3.1 Pad Configuration WSON 8x6-mm

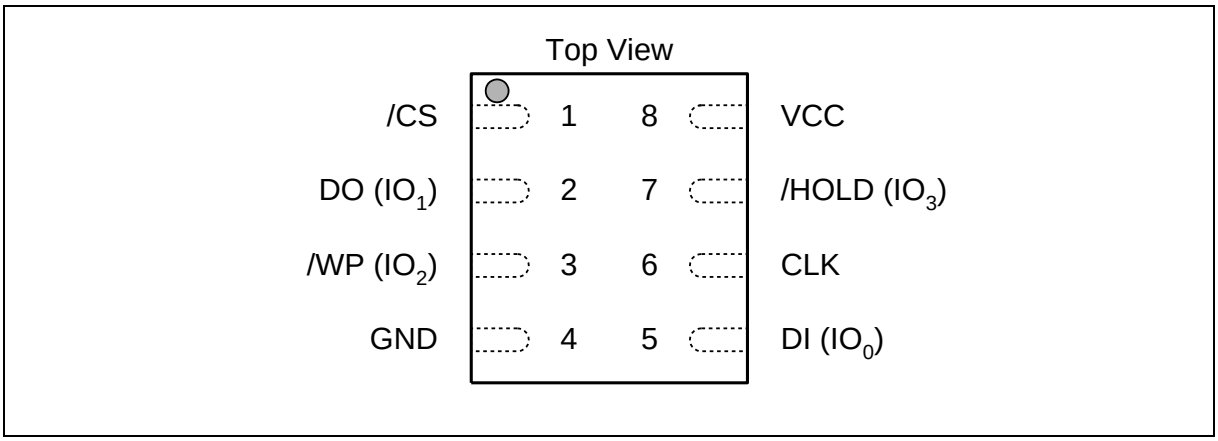



Figure 3-1 W25N01JW Pad Assignments, 8-pad WSON 8x6-mm (Package Code ZE)

## 3.2 Pad Description WSON 8x6-mm

| PAD NO. | PAD NAME | I/O | FUNCTION |
|---|---|---|---|
| 1 | /CS | I | Chip Select Input |
| 2 | DO (IO1) | I/O | Data Output (Data Input Output 1)(1) |
| 3 | /WP (IO2) | I/O | Write Protect Input ( Data Input Output 2)(2) |
| 4 | GND | | Ground |
| 5 | DI (IO0) | I/O | Data Input (Data Input Output 0)(1) |
| 6 | CLK | I | Serial Clock Input |
| 7 | /HOLD (IO3) | I/O | Hold Input (Data Input Output 3)(2) |
| 8 | VCC | | Power Supply |

**Notes:**

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.



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## 3.3 Pin Configuration SOIC 300-mil

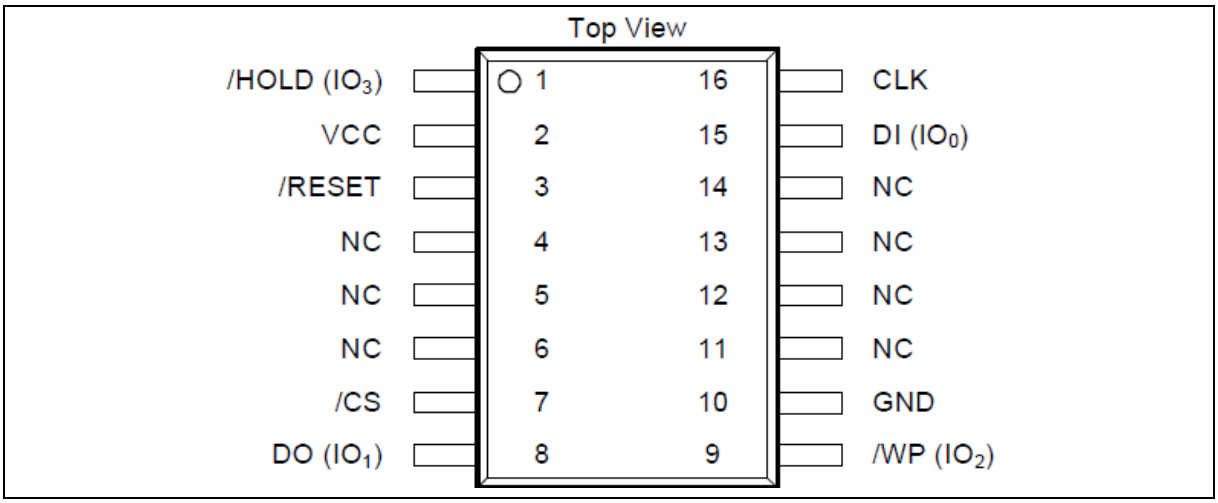



Figure 3-2 W25N01JW Pin Assignments, 16-pin SOIC 300-mil (Package Code SF)

## 3.4 Pin Description SOIC 300-mil

| PIN NO. | PIN NAME | I/O | FUNCTION |
|---|---|---|---|
| 1 | /HOLD (IO3) | I/O | Hold Input (Data Input Output 3)(2) |
| 2 | VCC | | Power Supply |
| 3 | /RESET | I | Reset Input(3) |
| 4 | N/C | | No Connect |
| 5 | N/C | | No Connect |
| 6 | N/C | | No Connect |
| 7 | /CS | I | Chip Select Input |
| 8 | DO (IO1) | I/O | Data Output (Data Input Output 1)(1) |
| 9 | /WP (IO2) | I/O | Write Protect Input ( Data Input Output 2)(2) |
| 10 | GND | | Ground |
| 11 | N/C | | No Connect |
| 12 | N/C | | No Connect |
| 13 | N/C | | No Connect |
| 14 | N/C | | No Connect |
| 15 | DI (IO0) | I/O | Data Input (Data Input Output 0)(1) |
| 16 | CLK | I | Serial Clock Input |

**Notes:**

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.
3. The /RESET pin on SOIC-16 package is a dedicated hardware reset pin.



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## 3.5 Ball Configuration TFBGA 8x6-mm (5x5-1 Ball Array)

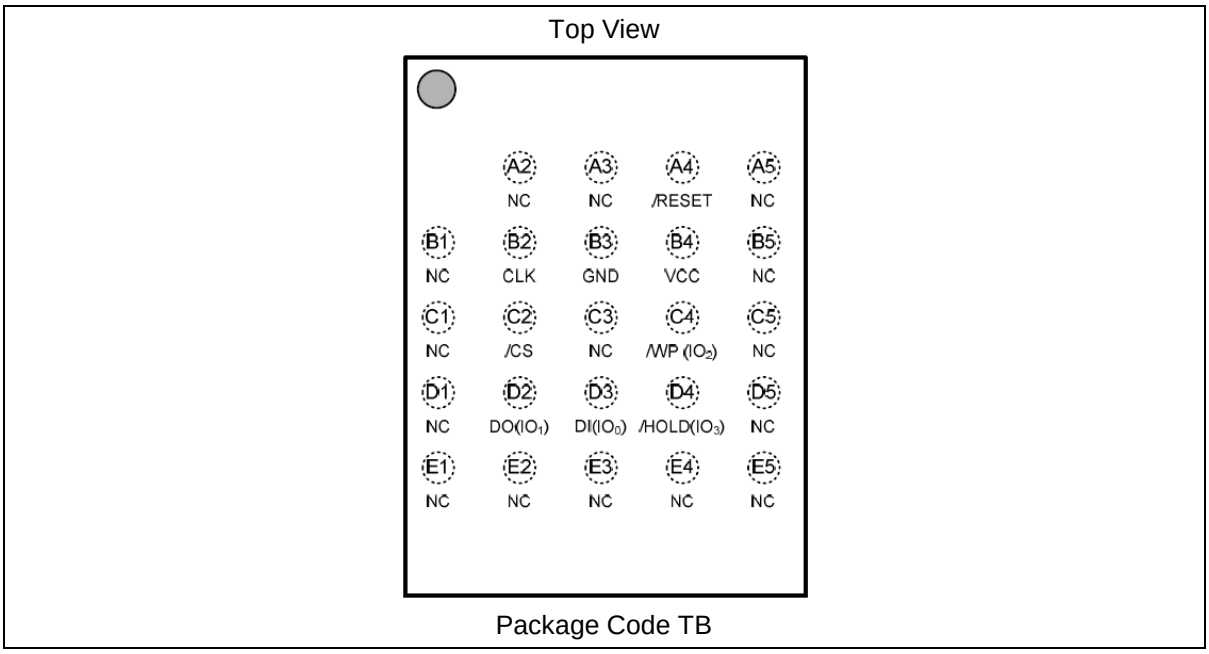



Figure 3-3 W25N01JW Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code TB)

## 3.6 Ball Description TFBGA 8x6-mm

| BALL NO. | PIN NAME | I/O | FUNCTION |
|---|---|---|---|
| A4 | /RESET | I | Reset Input |
| B2 | CLK | I | Serial Clock Input |
| B3 | GND | | Ground |
| B4 | VCC | | Power Supply |
| C2 | /CS | I | Chip Select Input |
| C4 | /WP (IO2) | I/O | Write Protect Input (Data Input Output 2)(2) |
| D2 | DO (IO1) | I/O | Data Output (Data Input Output 1)(1) |
| D3 | DI (IO0) | I/O | Data Input (Data Input Output 0)(1) |
| D4 | /HOLD (IO3) | I/O | Hold Input (Data Input Output 3)(2) |
| Multiple | NC | | No Connect |

**Notes:**

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.
3. The /RESET pin on TFBGA 24 package is a dedicated hardware reset pin.



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# 4. PIN DESCRIPTIONS

## 4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see "Write Protection" and "Power-up Power-down Timing Requirements"). If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

## 4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25N01JW supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

## 4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect bits BP[3:0] and Status Register Protect SRP bits SRP[1:0], a portion as small as 256K-Byte (2x128KB blocks) or up to the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the /WP pin. When QE=1, the /WP pin function is not available since this pin is used for IO2.

When WP-E=0, the device is in the Software Protection mode that only SR-1 can be protected. The /WP pin functions as a data I/O pin for the Quad SPI operations, as well as an active low input pin for the Write Protection function for SR-1. Refer to section 7.1.3 for detail information.

When WP-E=1, the device is in the Hardware Protection mode that /WP becomes a dedicated active low input pin for the Write Protection of the entire device. If /WP is tied to GND, all "Write/Program/Erase" functions are disabled. The entire device (including all registers, memory array and OTP pages) will become read-only. Quad SPI read operations are also disabled when WP-E is set to 1.

## 4.4 HOLD (/HOLD)

During Standard and Dual SPI operations, the /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When QE=1 or DTR operation is enabled, the /HOLD pin function is not available since this pin is used for IO3. The system has to drive high to /HOLD (IO3), or has to put an external pull-up resistor on the PCB.

## 4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

## 4.6 Reset (/RESET)

The /RESET pin allows the device to be reset by the controller, and provides hardware level resetting. This is highest priority among all the input signals. The /RESET pin is adopted on SOIC and TFBGA24 package types.



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## 5. BLOCK DIAGRAM

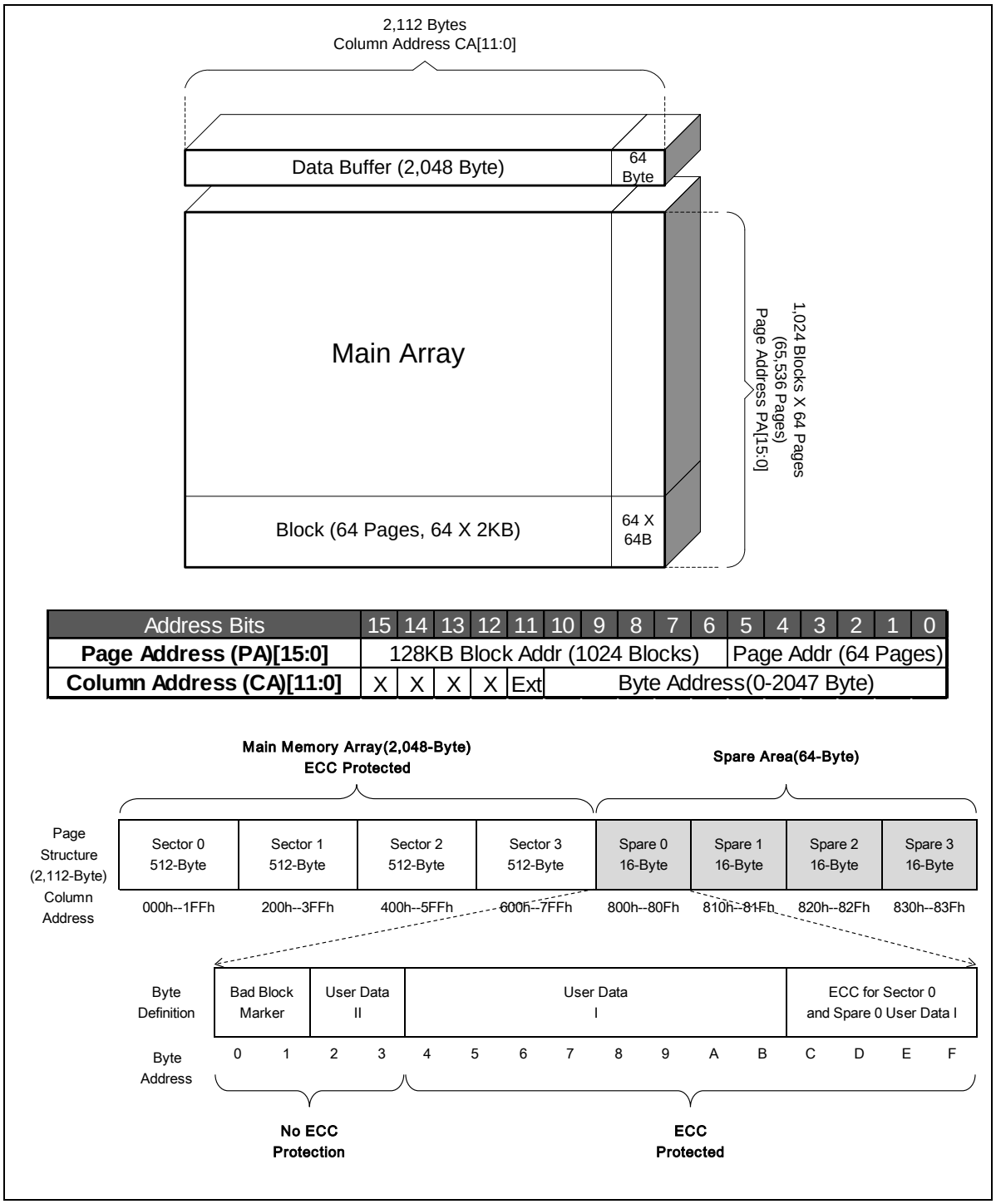


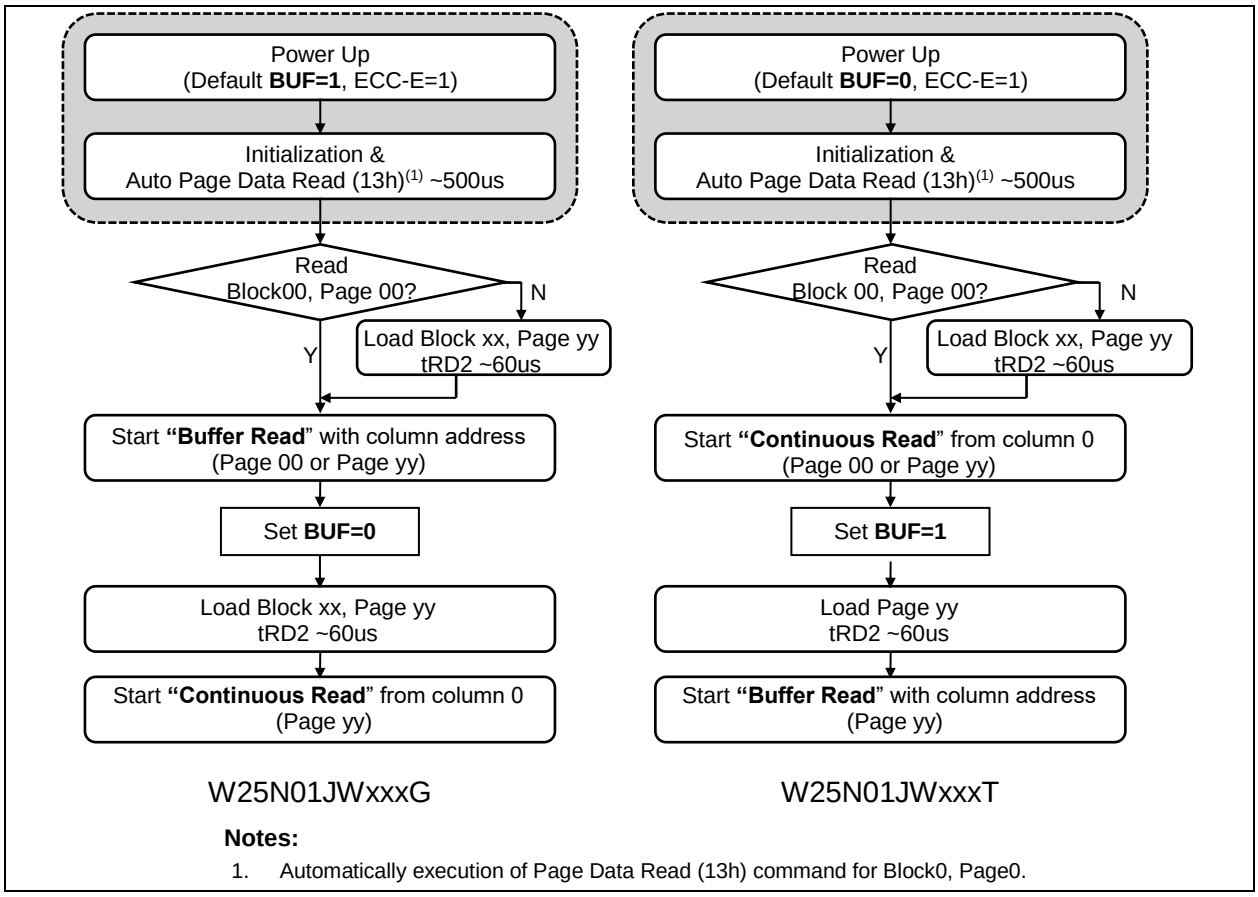

Figure 5-1 W25N01JW Flash Memory Architecture and Addressing



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# 6. FUNCTIONAL DESCRIPTIONS

## 6.1 Device Operation Flow




**Notes:**

1. Automatically execution of Page Data Read (13h) command for Block0, Page0.

Figure 6-1 W25N01JW Flash Memory Operation Diagram

### 6.1.1 Standard SPI Instructions

The W25N01JW is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

### 6.1.2 Dual SPI Instructions

The W25N01JW supports Dual SPI operation when using instructions such as "Fast Read Dual Output (3Bh)", "Fast Read Dual I/O (BBh)", "DTR Fast Read Dual Output (3Dh)" and "DTR Fast Read Dual I/O (BDh)". These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.



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### 6.1.3 Quad SPI Instructions

The W25N01JW supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)”, “DTR Fast Read Quad Output (6Dh)”, “DTR Fast Read Quad I/O (EDh)” and “Quad Program Data Load (32h/34h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively.

### 6.1.4 DTR Read Instructions

To effectively improve the read operation throughput without increasing the serial clock frequency, W25N01JW introduces DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI modes. The byte-long instruction code is latched into the device on the rising edge of the serial clock similar to all other SPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

### 6.1.5 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25N01JW operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. When QE=1 or DTR operation is enabled, the /HOLD function is not available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

### 6.1.6 Software Reset

#### 6.1.6.1 Device Reset (FFh) instruction

The Device Reset (FFh) instruction terminates any on-going internal operations without initialization for all volatile writable bits in the Status Registers. If the command sequence is successfully accepted, the device will take approximately tRST to reset. No command will be accepted during the reset period. Please refer to “8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detail information about command sequence and the value of each Status Registers after reset.

#### 6.1.6.2 Enable Reset (66h) and Reset Device (99h) instructions

The W25N01JW can be reset to the initial state by Enable Reset (66h) & Reset (99h) instructions. If the command sequence is successfully accepted, the device will take approximately tRST to reset. No command will be accepted during the reset period. Please refer to “8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detail information about command sequence and the value of each Status Registers after reset.



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### 6.1.7 Hardware Reset

#### 6.1.7.1 /RESET Pin

For the SOIC and TFBGA package types, the W25N01JW provides a dedicated /RESET pin. Drive /RESET pin low for a minimum period of 1us (tRESET) will reset the device to its initial power-on state. It takes same busy time with power-on (tVSL and tPUW) because Hardware Reset goes into the same state of after power-on. No command will be accepted during the tVSL period. Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum of 1us (tRESET) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and /HOLD). Please refer to “8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detail information about the value of each Status Registers after reset.

**Notes:**

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated /RESET pin on SOIC and TFBGA package. If the reset function is not used, this pin can be left floating in the system.

## 6.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25N01JW provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Protection Register (SR-1)
- Lock Down write protection for Protection Register (SR-1) until the next power-up
- One Time Program (OTP) write protection for memory array using Protection Register (SR-1)
- Hardware write protection using /WP pin when WP-E is set to 1

Upon power-up or at power-down, while VCC is below VCC (min), (see “Power-up Power-down Timing Requirements”), all operations are disabled and no instructions are recognized. During power-up, after the VCC voltage exceeds VCC (min) and tVSL has elapsed, all program and erase related instructions are further disabled for a time delay of tPUW. This includes the Write Enable, Program Execute, Block Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and $t_{VSL}$ time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Program Execute or Block Erase or Bad Block Management instruction will be accepted. After completing a program or erase instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Protection Register section for further information.

The WP-E bit in Protection Register (SR-1) is used to enable the hardware protection. When WP-E is set to 1, bringing /WP low in the system will block any Write/Program/Erase command to the W25N01JW, the device will become read-only. The Quad SPI operations are also disabled when WP-E is set to 1.

When QE=1, the Write Protection function is not available.



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## 6.3 DLP (Data Learning Pattern)

For Quad DTR Read commands (6Dh, EDh, EEh), a pre-defined "Data Learning Pattern" can be used by the flash memory controller to determine the flash data output timing on 4 I/O pins.

When DLP-E=1, during the last 4 dummy clocks just prior to the data output, W25N01JW will output "00110100" Data Learning Pattern sequence on each of the 4 I/O pins. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP-E=0 will disable the Data Learning Pattern output.

The Data Learning Pattern can also be defined by a "Write Data Learning Pattern (4Ah)" command followed by 8-bits user-defined pattern. The user-defined pattern is volatile. After device power cycle, the Data Learning Pattern will return to its "00110100" default value.

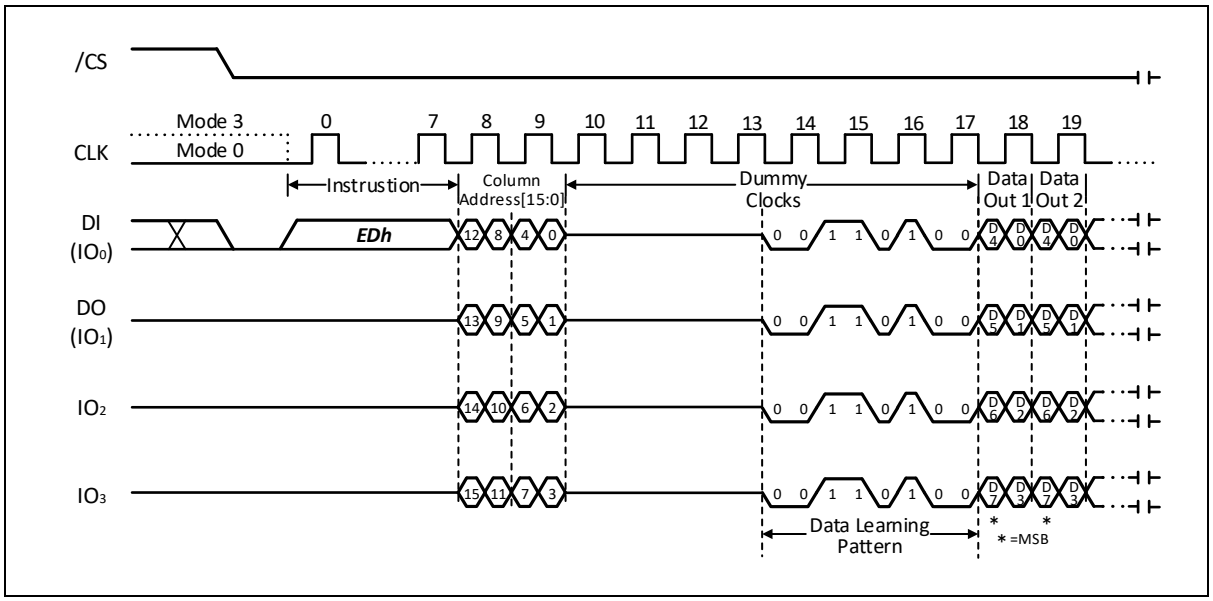



Figure 6-2 DLP (Data Learning Pattern) output example in DTR Fast Read Quad I/O (BUF=1)



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## 6.4 Interface States

This section describes the input and output signal levels.

| State | Transfer Rate | /RESET | /CS | CLK | /HOLD (IO3) | /WP (IO2) | DO (IO1) | DI (IO0) |
|---|---|---|---|---|---|---|---|---|
| Power-off | STR/DTR | X | X | X | X | X | Z | X |
| Power-on Reset | STR/DTR | *2 | *2 | X | X | X | Z | X |
| Reset (during tRST) | STR/DTR | H | X | X | X | X | Z | X |
| HW Reset | STR/DTR | L | X | X | X | X | Z | X |
| Interface Standby | STR/DTR | H | H | X | X | X | Z | X |
| Hold Cycle | STR only | H | L | L or H or T | L | X | Z *1 | X |
| Instruction Cycle | DTR | H | L | T | H | X | Z | (Input) |
| Single Input Cycle | STR | H | L | T | H | X | Z | (Input) |
| | DTR | H | L | T | X | X | Z | (Input) |
| Single Dummy Cycle | STR | H | L | T | H | X | Z | Z |
| | DTR | H | L | T | X | X | Z | Z |
| Single Output Cycle | STR | H | L | T | H | X | (Output) | X |
| | DTR | H | L | T | X | X | (Output) | X |
| Dual Input Cycle | STR | H | L | T | H | X | (Input) | (Input) |
| | DTR | H | L | T | X | X | (Input) | (Input) |
| Dual Dummy Cycle | STR | H | L | T | H | X | Z | Z |
| | DTR | H | L | T | X | X | Z | Z |
| Dual Output Cycle | STR | H | L | T | H | X | (Output) | (Output) |
| | DTR | H | L | T | X | X | (Output) | (Output) |
| Quad Input Cycle | STR | H | L | T | (Input) | (Input) | (Input) | (Input) |
| | DTR | H | L | T | (Input) | (Input) | (Input) | (Input) |
| Quad Dummy Cycle | STR | H | L | T | Z | Z | Z | Z |
| | DTR | H | L | T | Z | Z | Z | Z |
| Quad Output Cycle | STR | H | L | T | (Output) | (Output) | (Output) | (Output) |
| | DTR | H | L | T | (Output) | (Output) | (Output) | (Output) |

H= High input/output level
L= Low input/outut level
Z= Hi-Z
X= H or L level
T= Toggling between H and L

*1: During input sequence in Dual or Quad mode, this states is “X”.
*2: Refer to Fig 9.2



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# 7. PROTECTION, CONFIGURATION AND STATUS REGISTERS

Three Status Registers are provided for W25N01JW: Protection Register (SR-1), Configuration Register (SR-2) & Status Register (SR-3). Each register is accessed by Read Status Register and Write Status Register commands combined with 1-Byte Register Address respectively.

The Read Status Register instruction (05h / 0Fh) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Read modes, Protection Register/OTP area lock status, Erase/Program results and ECC usage/status.

The Write Status Register instruction can be used to configure the device write protection features, Software/Hardware write protection, Read modes and enable/disable ECC, Protection Register/OTP area lock, enable/disable Data Learning Pattern, number of dummy clocks, enable/disable Quad operation. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and when WP-E is set to 1, the /WP pin.

## 7.1 Protection Register / Status Register-1 (Volatile Writable, OTP lockable)

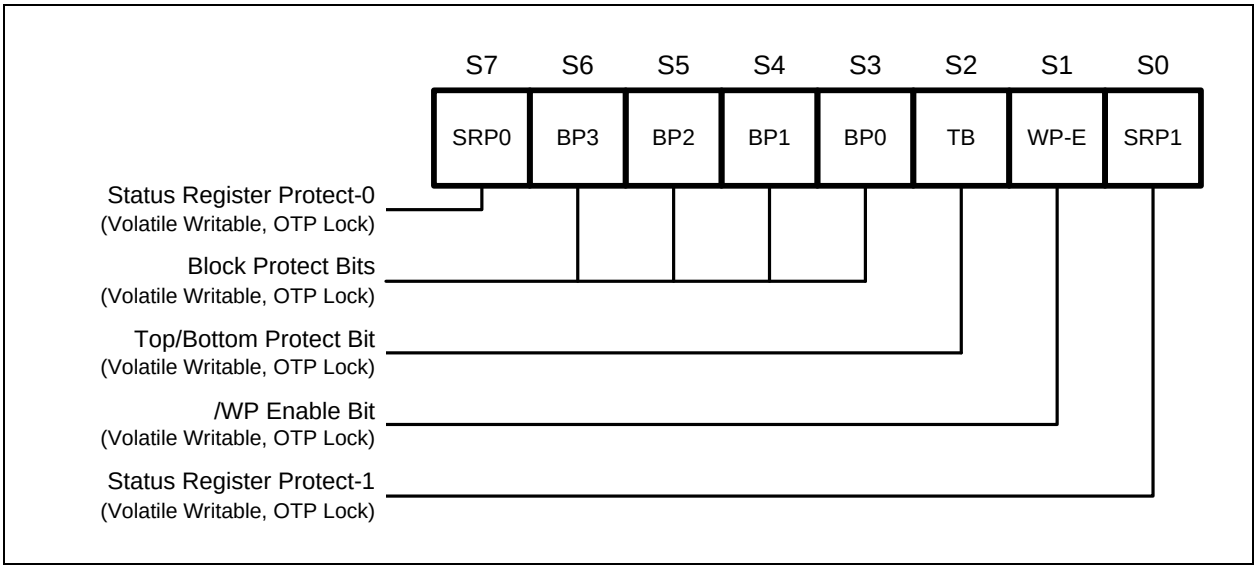



Figure 7-1 Protection Register / Status Register-1 (Address Axh)

### 7.1.1 Block Protect Bits (BP3, BP2, BP1, BP0, TB) – *Volatile Writable, OTP lockable*

The Block Protect bits (BP3, BP2, BP1, BP0 & TB) are volatile read/write bits in the status register-1 (S6, S5, S4, S3 & S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The default values for the Block Protection bits are 1 after power up to protect the entire array. If the SR1-L bit in the Configuration Register (SR-2) is set to 1, the default values will the values that are OTP locked.



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### 7.1.2 Write Protection Enable Bit (WP-E) – *Volatile Writable, OTP lockable*

The Write Protection Enable bit (WP-E) is a volatile read/write bits in the status register-1 (S1). The WP-E bit, in conjunction with SRP1 & SRP0, controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection, /WP pin functionality, and Quad SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, /WP & /HOLD pins are multiplexed as IO pins, and Quad program/read functions are enabled all the time. When WP-E is set to 1, the device is in Hardware Protection mode, all Quad functions are disabled and /WP & /HOLD pins become dedicated control input pins.

### 7.1.3 Status Register Protect Bits (SRP1, SRP0) – *Volatile Writable, OTP lockable*

The Status Register Protect bits (SRP1 and SRP0) are volatile read/write bits in the status register (S0 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

| Software Protection (Driven by Controller, WP-E is disabled) | | | | | |
|---|---|---|---|---|---|
| **SRP1** | **SRP0** | **WP-E** | **/WP/IO2** | **QE** | **Descriptions** |
| 0 | 0 | 0 | X | 0 | No /WP functionality |
| 0 | 1 | 0 | 0 | 0 | SR-1 cannot be changed (/WP = 0 during Write Status) |
| 0 | 1 | 0 | 1 | 0 | SR-1 can be changed (/WP = 1 during Write Status) |
| 1 | 0 | 0 | X | 0 | Power Lock Down(1) SR-1 |
| 1 | 1 | 0 | X | 0 | Enter OTP mode to protect SR-1 (allow SR1-L=1) |
| 0 | 0 | 0 | X | 1 | No /WP functionality<br>*/WP pin will always function as IO2* |
| 0 | 1 | 0 | X | 1 | SR-1 can be changed<br>*/WP pin will function as IO2 for Quad operations* |
| 1 | 0 | 0 | X | 1 | Power Lock Down(1) SR-1<br>*/WP pin will always function as IO2* |
| 1 | 1 | 0 | X | 1 | Enter OTP mode to protect SR-1 (allow SR1-L=1)<br>*/WP pin will always function as IO2* |

| Hardware Protection (System Circuit / PCB layout, Quad Program/Read is disabled) | | | | | |
|---|---|---|---|---|---|
| **SRP1** | **SRP0** | **WP-E** | **/WP only** | **QE** | **Descriptions** |
| 0 | X | 1 | VCC | 0 | SR-1 can be changed |
| 1 | 0 | 1 | VCC | 0 | Power Lock-Down(1) SR-1 |
| 1 | 1 | 1 | VCC | 0 | Enter OTP mode to protect SR-1 (allow SR1-L=1) |
| X | X | 1 | GND | 0 | All "Write/Program/Erase" commands are blocked<br>Entire device (SRs, Array, OTP area) is read-only |

**Notes:**

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.
2. When WP-E=1, QE bit have to be ignored.



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## 7.2 Configuration Register / Status Register-2 (Volatile Writable)

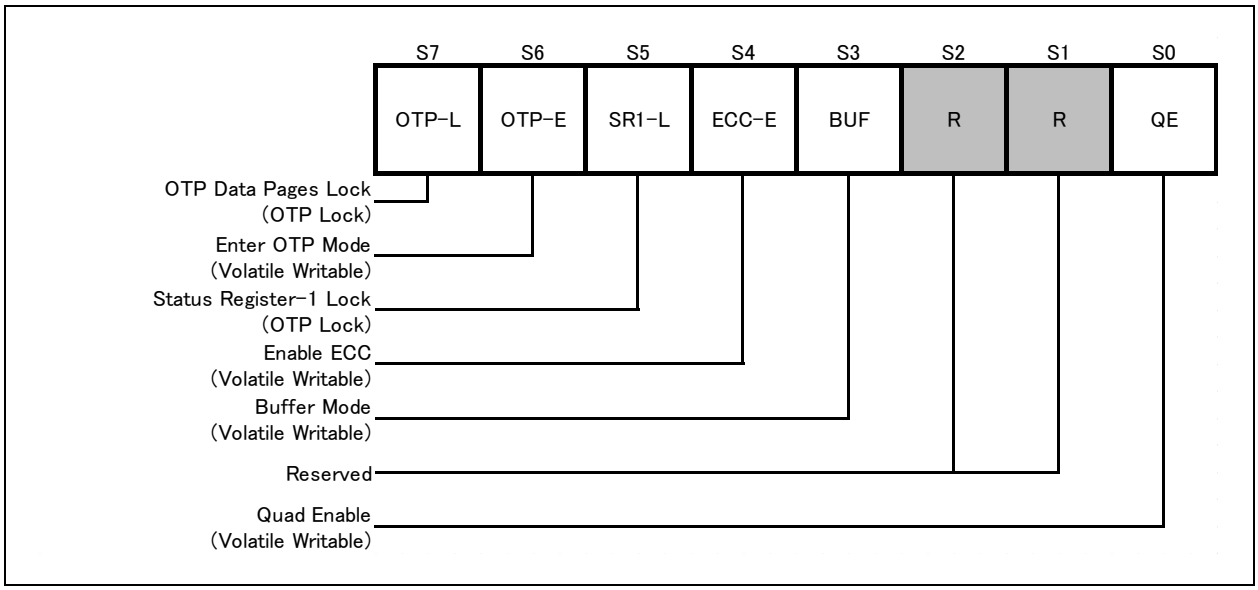



Figure 7-2 Configuration Register / Status Register-2 (Address Bxh)

### 7.2.1 One Time Program Lock Bit (OTP-L) – *OTP lockable*

In addition to the main memory array, W25N01JW also provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 10 pages of 2,112-Byte each. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from "1" to "0", and data is not reversible ("0" to "1") by the Erase command. Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

### 7.2.2 Enter OTP Access Mode Bit (OTP-E) – *Volatile Writable*

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up or a RESET command is 0.

### 7.2.3 Status Register-1 Lock Bit (SR1-L) – *OTP lockable*

The SR1-L lock bit is used to OTP lock the values in the Protection Register (SR-1). Depending on the settings in the SR-1, the device can be configured to have a portion of or up to the entire array to be write-protected, and the setting can be OTP locked by setting SR1-L bit to 1. SR1-L bit can only be set to 1 permanently when SRP1 & SRP0 are set to (1, 1), and OTP Access Mode must be entered (OTP-E=1) to execute the programming. Please refer to 8.2.38 for detailed information.



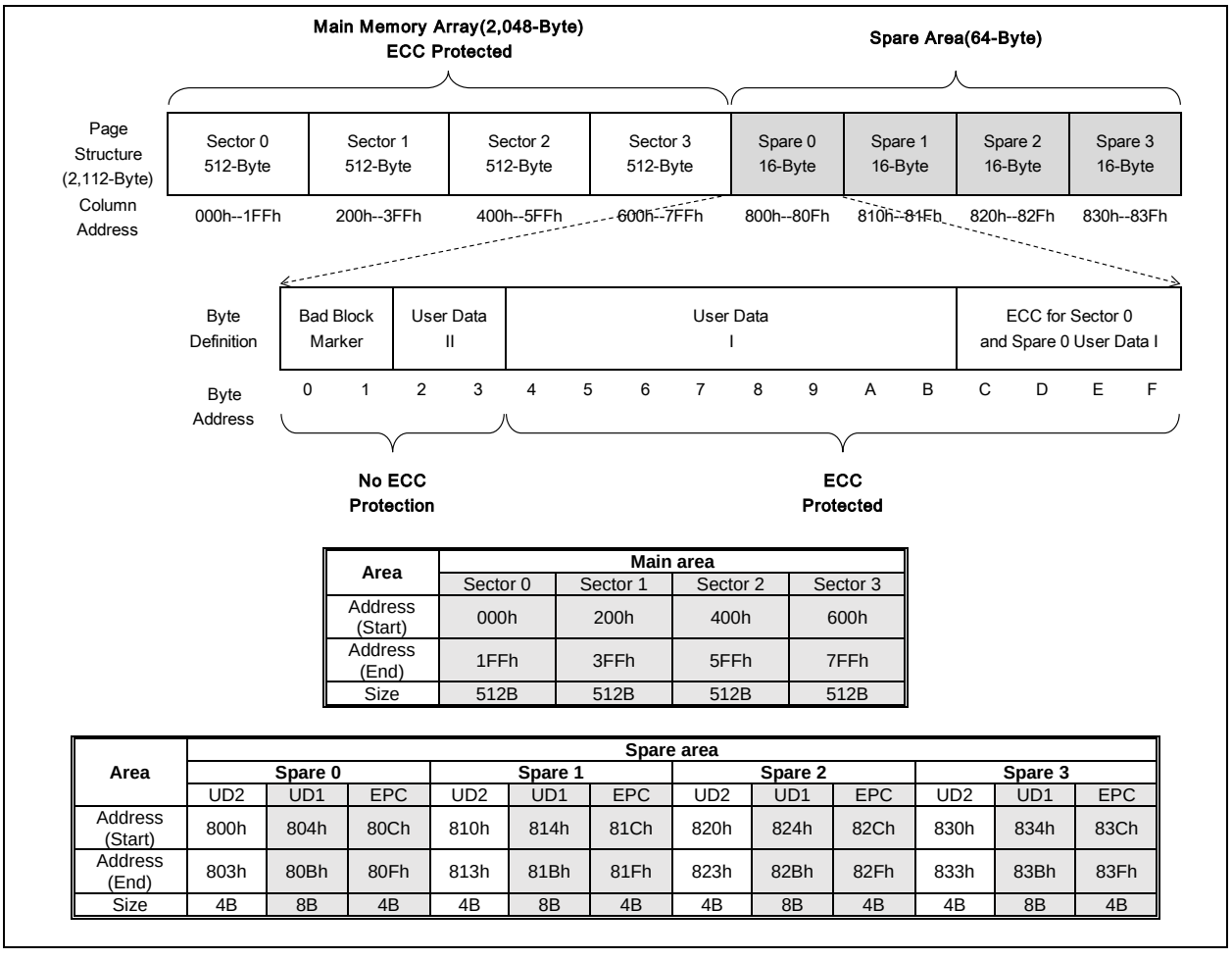
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### 7.2.4 ECC Enable Bit (ECC-E) – *Volatile Writable*

W25N01JW has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 64-Byte area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bit. ECC function is enabled by default when power on (ECC-E=1), and it will not be reset to 0 by the Device Reset command.

The constraint when ECC-E=1 are as follows:

- The areas protected by ECC is shown in the table below. User Data I is protected by ECC, but User Data II is out of protected by ECC.
- The Number of Partial Page Program (NoP) is 4 for the entire page, including the spare area. Therefore the user needs to program one sector and optionally User Data 1 of pared spare area (example, main area-sector 0 and spare area-spare 0) at one time program to properly and automatically program the ECC parity code.




| Area | Main area | | | |
|---|---|---|---|---|
| | Sector 0 | Sector 1 | Sector 2 | Sector 3 |
| Address (Start) | 000h | 200h | 400h | 600h |
| Address (End) | 1FFh | 3FFh | 5FFh | 7FFh |
| Size | 512B | 512B | 512B | 512B |

| Area | Spare area | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Spare 0 | | | Spare 1 | | | Spare 2 | | | Spare 3 | | |
| | UD2 | UD1 | EPC | UD2 | UD1 | EPC | UD2 | UD1 | EPC | UD2 | UD1 | EPC |
| Address (Start) | 800h | 804h | 80Ch | 810h | 814h | 81Ch | 820h | 824h | 82Ch | 830h | 834h | 83Ch |
| Address (End) | 803h | 80Bh | 80Fh | 813h | 81Bh | 81Fh | 823h | 82Bh | 82Fh | 833h | 83Bh | 83Fh |
| Size | 4B | 8B | 4B | 4B | 8B | 4B | 4B | 8B | 4B | 4B | 8B | 4B |

**Notes:**

1. UD2: User Data II
2. UD1: User Data I
3. EPC: ECC parity code

The gray area of the above table is protected by ECC



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### 7.2.5 Buffer Read / Continuous Read Mode Bit (BUF) – *Volatile Writable*

W25N01JW provides two different modes for read operations, Buffer Read Mode (BUF=1) and Continuous Read Mode (BUF=0). Prior to any Read operation, a Page Data Read command is needed to initiate the data transfer from a specified page in the memory array to the Data Buffer. By default, after power up, the data in page 0 will be automatically loaded into the Data Buffer and the device is ready to accept any read commands.

The Buffer Read Mode (BUF=1) requires a Column Address to start outputting the existing data inside the Data Buffer, and once it reaches the end of the data buffer (Byte 2,111), DO (IO1) pin will become high-Z state.

The Continuous Read Mode (BUF=0) doesn't require the starting Column Address. The device will always start output the data from the first column (Byte 0) of the Data buffer, and once the end of the data buffer (Byte 2,048) is reached, the data output will continue through the next memory page. With Continuous Read Mode, it is possible to read out the entire memory array using a single read command. Please refer to respective command descriptions for the dummy cycle requirements for each read commands under different read modes.

For W25N01JWxxxG part number, the default value of BUF bit after power up is 1. BUF bit can be written to 0 in the Status Register-2 to perform the Continuous Read operation.

For W25N01JWxxxT part number, the default value of BUF bit after power up is 0. BUF bit can be written to 1 in the Status Register-2 to perform the Buffer Read operation.

| BUF | ECC-E | Read Mode (Starting from Buffer) | ECC Status | Data Output Structure |
|---|---|---|---|---|
| 1 | 0 | Buffer Read | N/A | 2,048 + 64 |
| 1 | 1 | Buffer Read | Page based | 2,048 + 64 |
| 0 | 0 | Continuous Read | N/A | 2,048 |
| 0 | 1 | Continuous Read | Operation based | 2,048 |

### 7.2.6 Quad Enable (QE) – *Volatile Writable*

The Quad Enable (QE) bit is a volatile read/write bit that enables Quad SPI operation. When QE=0, the /WP and /HOLD pins are enabled, the device operates in Standard/Dual SPI modes. When QE=1 (factory default), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled, the device operates in Standard/Dual/Quad SPI modes.

If the SR1-L bit in the Configuration Register (SR-2) is set to 1, the default values will the values that are OTP locked.

**WARNING: If the /WP or /HOLD pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.**



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## 7.3 Status Register-3 (Status only)

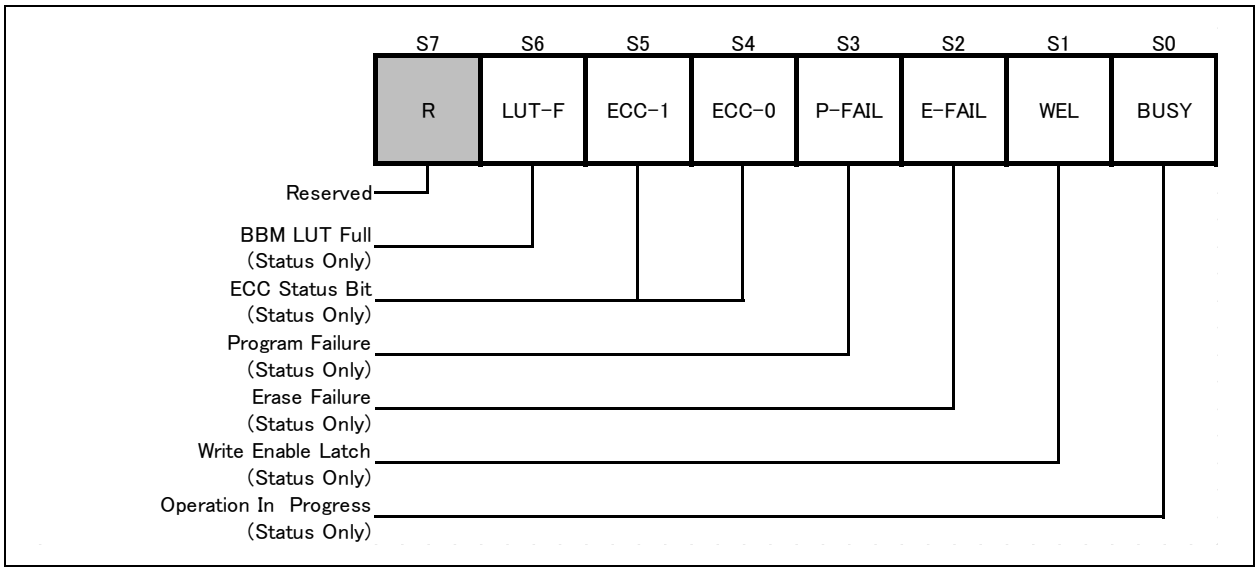



Figure 7-3 Status Register-3 (Address Cxh)

### 7.3.1 Look-Up Table Full (LUT-F) – *Status Only*

To facilitate the NAND flash memory bad block management, the W25N01JW is equipped with an internal Bad Block Management Look-Up-Table (BBM LUT). Up to 20 bad memory blocks may be replaced by a good memory block respectively. The addresses of the blocks are stored in the internal Look-Up Table as Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 20 memory block links have been fully utilized or not. The default value of LUT-F is 0, once all 20 links are used, LUT-F will become 1, and no more memory block links may be established.

### 7.3.2 Cumulative ECC Status (ECC-1, ECC-0) – *Status Only*

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECC-1, ECC-0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-E=0. These bits will be cleared to 0 after a power cycle or a RESET command or a Page Data Read command.



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| ECC Status | | Descriptions |
|---|---|---|
| ECC-1 | ECC-0 | |
| 0 | 0 | The entire data output is provided without requiring any ECC correction. |
| 0 | 1 | The entire data output experienced a 1 bit correction event after reading either single or multiple pages. |
| 1 | 0 | The entire data output experienced a 2 bit error event in a single page that cannot be corrected[2] in the Continuous Read Mode, an additional command can be used to read out the Page Address (PA) that contains the error. |
| 1 | 1 | The entire data output experienced a 2 bit error event in multiple pages. In the Continuous Read Mode, the additional command can only provide the last Page Address (PA) that contain the 2 bit error. PAs for other pages with the 2 bit error is not available. The data read is not suitable for use[2, 3]. |

**Notes:**

1. As the ECC engine is based on Hamming code, the ECC status bits are applicable for 1 bit ECC correction and 2 bit ECC detection. This Serial NAND is not expected to experience 3 or more bits of error when used within the datasheet specifications. When there is a 1 bit error correction event, user may decide to erase and reprogram the associated block, based on the user's quality policy.
2. If the read operation contains both 1 or 2 bit error event, the 2 bit error condition will be used.
3. ECC-1, ECC-0 = (1, 1) is only applicable during Continuous Read operation (BUF=0).

### 7.3.3 Program Failure (P-FAIL) – *Status Only*

The Program Failure Bit is used to indicate whether the internally-controlled Program operation was executed successfully (P-FAIL=0) or timed out (P-FAIL=1). The P-FAIL bit is also set when the Program command is issued to a locked or protected memory array or OTP area. This bit is cleared at the beginning of the Program Execute instruction on an unprotected memory array or OTP area. Device Reset instruction can also clear the P-FAIL bit.

### 7.3.4 Erase Failure (E-FAIL) – *Status Only*

The Erase Failure Bit is used to indicate whether the internally-controlled Erase operation was executed successfully (E-FAIL=0) or timed out (E-FAIL=1). The E-FAIL bit is also set when the Erase command is issued to a locked or protected memory array. This bit is cleared at the beginning of the Block Erase instruction on an unprotected memory array. Device Reset instruction can also clear the E-FAIL bit.

### 7.3.5 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read and Program Execute and Bad Block Management for OTP pages.

### 7.3.6 Read/Erase/Program in Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is powering up or executing a Page Data Read, BBM Management, Program Execute, Block Erase and Program Execute for OTP area, OTP Locking or after a Continuous Read instruction. During this time the device will ignore further instructions except for the Read Status Register, Reset and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.



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## 7.4 Status Register-4 (Writable and Status)

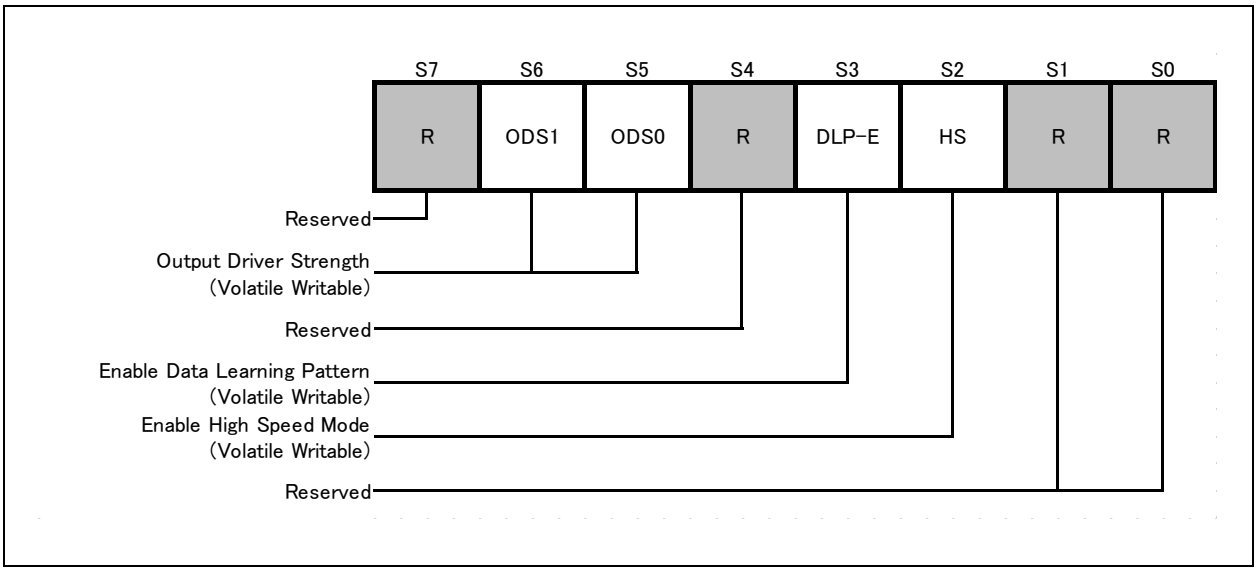



Figure 7-4 Status Register-4 (Address Dxh)

### 7.4.1 Output Driver Strength (ODS1, ODS0) – *Volatile Writable*

The ODS1 & ODS0 bits are used to determine the output driver strength for the Read operations.

| ODS1, ODS0 | Output Driver Strength |
|---|---|
| 0, 0 | 100% (Default setting) |
| 0, 1 | 75% |
| 1, 0 | 50% |
| 1, 1 | 25% |

### 7.4.2 Data Learning Pattern Enable (DLP-E) – *Volatile Writable*

For Quad DTR Read commands, a pre-defined “Data Learning Pattern” can be used by the flash memory controller to determine the flash data output timing on I/O pins. When DLP-E=1, during the last 4 dummy cycles just prior to the data output, W25N01JW will output “00110100” Data Learning Pattern sequence on each of the 4 I/O pins. During the period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP-E=0 will disable the Data Learning Pattern output. The Data Learning Pattern can also be defined by a “Write Data Learning Pattern (4Ah)” command followed by 8-bits user-defined pattern. The user defined pattern is volatile. After device power cycle, the Data Learning Pattern will return to its “00110100” default value.

### 7.4.3 High Speed Enable (HS) – *Volatile Writable*

The HS bit enables the following commands to operate at 166 MHz.

- Fast Read Dual I/O (BBh)
- Fast Read Dual I/O with 4-Byte Address (BCh)
- Fast Read Quad I/O (EBh)
- Fast Read Quad I/O with 4-Byte Address (ECh)

When HS = 1, the dummy cycles of these commands are set from 4 to 8, allowing operation at 166 MHz. When HS = 0, the dummy cycle of these commands is 4, and operation up to 104 MHz is possible.



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## 7.5 Extended Register

The Data Learning Pattern can be defined by a "Write Data Learning Pattern (4Ah)" command followed by 8-bits user-defined pattern. The user defined pattern is volatile. After device power cycle, the Data Learning Pattern will return to its "00110100" default value.

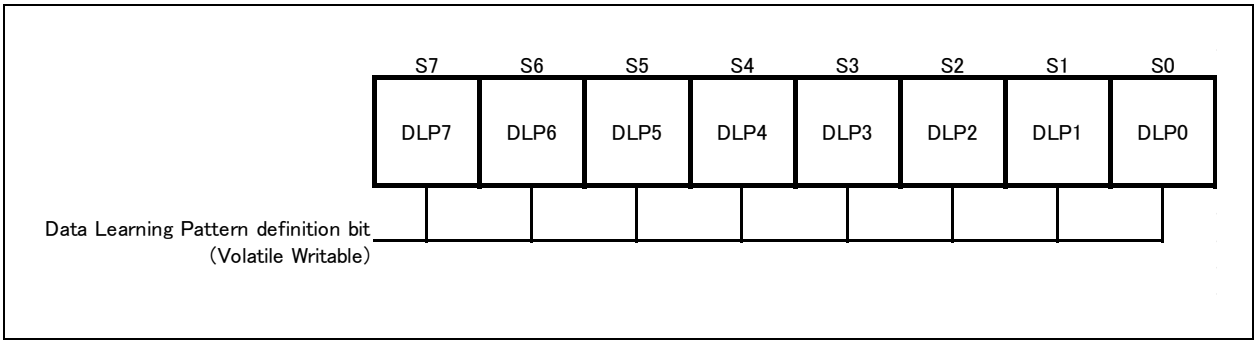



Figure 7-5 Extended Register



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## 7.6 W25N01JW Status Register Memory Protection

| STATUS REGISTER[1] | | | | | W25N01JW (1G-BIT / 128M-BYTE) MEMORY PROTECTION[2] | | | |
|---|---|---|---|---|---|---|---|---|
| TB | BP3 | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED PAGE ADDRESS PA[15:0] | PROTECTED DENSITY | PROTECTED PORTION |
| X | 0 | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 1022 & 1023 | FF80h - FFFFh | 256KB | Upper 1/512 |
| 0 | 0 | 0 | 1 | 0 | 1020 thru 1023 | FF00h - FFFFh | 512KB | Upper 1/256 |
| 0 | 0 | 0 | 1 | 1 | 1016 thru 1023 | FE00h - FFFFh | 1MB | Upper 1/128 |
| 0 | 0 | 1 | 0 | 0 | 1008 thru 1023 | FC00h - FFFFh | 2MB | Upper 1/64 |
| 0 | 0 | 1 | 0 | 1 | 992 thru 1023 | F800h - FFFFh | 4MB | Upper 1/32 |
| 0 | 0 | 1 | 1 | 0 | 960 thru 1023 | F000h - FFFFh | 8MB | Upper 1/16 |
| 0 | 0 | 1 | 1 | 1 | 896 thru 1023 | E000h - FFFFh | 16MB | Upper 1/8 |
| 0 | 1 | 0 | 0 | 0 | 768 thru 1023 | C000h - FFFFh | 32MB | Upper 1/4 |
| 0 | 1 | 0 | 0 | 1 | 512 thru 1023 | 8000h - FFFFh | 64MB | Upper 1/2 |
| 1 | 0 | 0 | 0 | 1 | 0 & 1 | 0000h – 007Fh | 256KB | Lower 1/512 |
| 1 | 0 | 0 | 1 | 0 | 0 thru 3 | 0000h - 00FFh | 512KB | Lower 1/256 |
| 1 | 0 | 0 | 1 | 1 | 0 thru 7 | 0000h - 01FFh | 1MB | Lower 1/128 |
| 1 | 0 | 1 | 0 | 0 | 0 thru 15 | 0000h - 03FFh | 2MB | Lower 1/64 |
| 1 | 0 | 1 | 0 | 1 | 0 thru 31 | 0000h - 07FFh | 4MB | Lower 1/32 |
| 1 | 0 | 1 | 1 | 0 | 0 thru 63 | 0000h - 0FFFh | 8MB | Lower 1/16 |
| 1 | 0 | 1 | 1 | 1 | 0 thru 127 | 0000h - 1FFFh | 16MB | Lower 1/8 |
| 1 | 1 | 0 | 0 | 0 | 0 thru 255 | 0000h - 3FFFh | 32MB | Lower 1/4 |
| 1 | 1 | 0 | 0 | 1 | 0 thru 511 | 0000h - 7FFFh | 64MB | Lower 1/2 |
| X | 1 | 0 | 1 | X | 0 thru 1023 | 0000h - FFFFh | 128MB | ALL |
| X | 1 | 1 | X | X | 0 thru 1023 | 0000h - FFFFh | 128MB | ALL |

**Notes:**

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.



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# 8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25N01JW are fully controlled through the SPI bus (see Instruction Set Table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures of each commands description. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the device is performing Program or Erase operation, BBM management, Page Data Read or OTP locking operations, BUSY bit will be high, and all instructions except for Read Status Register or Read JEDEC ID will be ignored until the current operation cycle has completed.

## 8.1 Device ID and Instruction Set Tables

### 8.1.1 Manufacturer and Device Identification

| **MANUFACTURER ID** | **(MF7 - MF0)** |
|---|---|
| Winbond Serial Flash | EFh |
| | |
| **Device ID** | **(ID15 - ID0)** |
| W25N01JW | BC21h |



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### 8.1.2 Instruction Set Table 1 (Continuous Read, BUF = 0, xxxT Default Power Up Mode)(11)

| Command | Op Code | Default Dummy | HS=1 Dummy | Byte2 | Byte3 | Byte4 | Byte5 | Byte6 | Byte7 |
|---|---|---|---|---|---|---|---|---|---|
| RESET Enable + RESET Memory (NOR compatible) | 66h+99h | 0 | - | | | | | | |
| Device RESET | FFh | 0 | - | | | | | | |
| Read JEDEC ID | 9Fh | 8 | - | Dummy | MF7-0 | ID15-8 | ID7-0 | | |
| Read Status Register-1 | 0Fh/05h | 0 | - | Axh | S7-0 | S7-0 | S7-0 | S7-0 | S7-0 |
| Read Status Register-2 | 0Fh/05h | 0 | - | Bxh | S7-0 | S7-0 | S7-0 | S7-0 | S7-0 |
| Read Status Register-3 | 0Fh/05h | 0 | - | Cxh | S7-0 | S7-0 | S7-0 | S7-0 | S7-0 |
| Read Status Register-4 | 0Fh/05h | 0 | - | Dxh | S7-0 | S7-0 | S7-0 | S7-0 | S7-0 |
| Write Status Register-1 | 1Fh/01h | 0 | - | Axh | S7-0 | | | | |
| Write Status Register-2 | 1Fh/01h | 0 | - | Bxh | S7-0 | | | | |
| Write Status Register-4 | 1Fh/01h | 0 | - | Dxh | S7-0 | | | | |
| Write Data Learning Pattern | 4Ah | 0 | - | P7-0 | | | | | |
| Write Enable | 06h | - | - | | | | | | |
| Write Disable | 04h | - | - | | | | | | |
| Deep Power-down | B9h | - | - | | | | | | |
| Release Deep Power-down | ABh | - | - | | | | | | |
| Bad Block Management (Swap Blocks) | A1h | 0 | - | LBA0 | LBA0 | PBA0 | PBA0 | LBA1 | LBA1 |
| Read BBM LUT | A5h | 8 | - | Dummy | LBA0 | LBA0 | PBA0 | PBA0 | LBA1 |
| Last ECC failure Page Address | A9h | 8 | - | Dummy | PA15-8 | PA7-0 | | | |
| Block Erase | D8h | 8 | - | Dummy | PA15-8 | PA7-0 | | | |
| Program Data Load | 02h | 0 | - | CA15-8 | CA7-0 | D0 | D1 | D2 | D3 |
| Random Program Data Load | 84h | 0 | - | CA15-8 | CA7-0 | D0 | D1 | D2 | D3 |
| Quad Program Data Load | 32h | 0 | - | CA15-8 | CA7-0 | D0 | D1 | D2 | D3 |
| Random Quad Program Data Load | 34h | 0 | - | CA15-8 | CA7-0 | D0 | D1 | D2 | D3 |
| Program Execute | 10h | 8 | - | Dummy | PA15-8 | PA7-0 | | | |



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(Continue instruction set table of BUF=0)

| Command | Op Code | Default Dummy | HS=1 Dummy | Byte2 | Byte3 | Byte4 | Byte5 | Byte6 | Byte7 |
|---|---|---|---|---|---|---|---|---|---|
| Page Data Read | 13h | 8 | - | PA23-16 | PA15-8 | PA7-0 | | | |
| Read | 03h | 24 | - | Dummy | | | D0 | D1 | D2 |
| Fast Read | 0Bh | 32 | - | Dummy | | | | D0 | D1 |
| Fast Read with 4-Byte Address | 0Ch | 40 | - | Dummy | | | | | D0 |
| Fast Read Dual Output | 3Bh | 32 | - | Dummy | | | | D0 | D1 | D2 | D3 |
| Fast Read Dual Output with 4-Byte Address | 3Ch | 40 | - | Dummy | | | | | D0 | D1 |
| Fast Read Quad Output | 6Bh | 32 | - | Dummy | | | | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| Fast Read Quad Output with 4-Byte Address | 6Ch | 40 | - | Dummy | | | | | D0 | D1 | D2 | D3 |
| Fast Read Dual I/O | BBh | 16 | 20 | Dummy | | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| Fast Read Dual I/O with 4-Byte Address | BCh | 20 | 24 | Dummy | | | D0 | D1 | D2 | D3 | D4 | D5 | D6 |
| Fast Read Quad I/O | EBh | 12 | 16 | Dummy | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D16 | D17 |
| Fast Read Quad I/O with 4-Byte Address | ECh | 14 | 18 | Dummy | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D16 |
| DTR Fast Read | 0Dh | 18 | - | Dummy | | D0 | D1 | D2 | D3 | D4 | D5 | D6 | … |
| DTR Fast Read with 4-Byte Address | 0Eh | 22 | - | Dummy | | | D0 | D1 | D2 | D3 | D4 | D5 | … |
| DTR Fast Read Dual Output | 3Dh | 18 | - | Dummy | | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 |
| DTR Fast Read Quad Output | 6Dh | 20 | - | Dummy | | | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D16 | D17 | D18 | D19 | D20 | D21 | D22 | D23 | D24 | D25 | D26 | D27 |
| DTR Fast Read Dual I/O | BDh | 12 | - | Dummy | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D16 | D17 |
| DTR Fast Read Dual I/O with 4-Byte Address | BEh | 14 | - | Dummy | | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D16 |
| DTR Fast Read Quad I/O | EDh | 11 | - | Dummy | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D16 | D17 | D18 | D19 | D20 | D21 | D22 | D23 | D24 | D25 | D26 | D27 | D28 | D29 | D30 | D31 | D32 | D33 | D34 | D35 | D36 |
| DTR Fast Read Quad I/O with 4-Byte Address | EEh | 12 | - | Dummy | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D16 | D17 | D18 | D19 | D20 | D21 | D22 | D23 | D24 | D25 | D26 | D27 | D28 | D29 | D30 | D31 | D32 | D33 | D34 | D35 |



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### 8.1.3 Instruction Set Table 2 (Buffer Read, BUF = 1, xxxG Default Power Up Mode)(12)

| Command | Op Code | Default Dummy | HS=1 Dummy | Byte2 | Byte3 | Byte4 | Byte5 | Byte6 | Byte7 |
|---|---|---|---|---|---|---|---|---|---|
| RESET Enable + RESET Memory (NOR compatible) | 66h+99h | 0 | - | | | | | | |
| Device RESET | FFh | 0 | - | | | | | | |
| Read JEDEC ID | 9Fh | 8 | - | Dummy | MF7-0 | ID15-8 | ID7-0 | | |
| Read Status Register-1 | 0Fh/05h | 0 | - | Axh | S7-0 | S7-0 | S7-0 | S7-0 | S7-0 |
| Read Status Register-2 | 0Fh/05h | 0 | - | Bxh | S7-0 | S7-0 | S7-0 | S7-0 | S7-0 |
| Read Status Register-3 | 0Fh/05h | 0 | - | Cxh | S7-0 | S7-0 | S7-0 | S7-0 | S7-0 |
| Read Status Register-4 | 0Fh/05h | 0 | - | Dxh | S7-0 | S7-0 | S7-0 | S7-0 | S7-0 |
| Write Status Register-1 | 1Fh/01h | 0 | - | Axh | S7-0 | | | | |
| Write Status Register-2 | 1Fh/01h | 0 | - | Bxh | S7-0 | | | | |
| Write Status Register-4 | 1Fh/01h | 0 | - | Dxh | S7-0 | | | | |
| Write Data Learning Pattern | 4Ah | 0 | - | P7-0 | | | | | |
| Write Enable | 06h | - | - | | | | | | |
| Write Disable | 04h | - | - | | | | | | |
| Deep Power-down | B9h | - | - | | | | | | |
| Release Deep Power-down | ABh | - | - | | | | | | |
| Bad Block Management (Swap Blocks) | A1h | 0 | - | LBA0 | LBA0 | PBA0 | PBA0 | LBA1 | LBA1 |
| Read BBM LUT | A5h | 8 | - | Dummy | LBA0 | LBA0 | PBA0 | PBA0 | LBA1 |
| Last ECC failure Page Address | A9h | 8 | - | Dummy | PA15-8 | PA7-0 | | | |
| Block Erase | D8h | 8 | - | Dummy | PA15-8 | PA7-0 | | | |
| Program Data Load | 02h | 0 | - | CA15-8 | CA7-0 | D0 | D1 | D2 | D3 |
| Random Program Data Load | 84h | 0 | - | CA15-8 | CA7-0 | D0 | D1 | D2 | D3 |
| Quad Program Data Load | 32h | 0 | - | CA15-8 | CA7-0 | D0 | D1 | D2 | D3 |
| Random Quad Program Data Load | 34h | 0 | - | CA15-8 | CA7-0 | D0 | D1 | D2 | D3 |
| Program Execute | 10h | 8 | - | Dummy | PA15-8 | PA7-0 | | | |



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(Continue instruction set table of BUF=1)

| Command | Op Code | Default Dummy | HS=1 Dummy | Byte2 | Byte3 | Byte4 | Byte5 | Byte6 | Byte7 |
|---|---|---|---|---|---|---|---|---|---|
| Page Data Read | 13h | 8 | - | PA23-16 | PA15-8 | PA7-0 | | | |
| Read | 03h | 8 | - | CA15-8 | CA7-0 | Dummy | D0 | D1 | D2 |
| Fast Read | 0Bh | 8 | - | CA15-8 | CA7-0 | Dummy | D0 | D1 | D2 |
| Fast Read with 4-Byte Address | 0Ch | 24 | - | CA15-8 | CA7-0 | Dummy | | | D0 |
| Fast Read Dual Output | 3Bh | 8 | - | CA15-8 | CA7-0 | Dummy | D0 D1 | D2 D3 | D4 D5 |
| Fast Read Dual Output with 4-Byte Address | 3Ch | 24 | - | CA15-8 | CA7-0 | Dummy | | | D0 D1 |
| Fast Read Quad Output | 6Bh | 8 | - | CA15-8 | CA7-0 | Dummy | D0 D1 D2 D3 | D4 D5 D6 D7 | D8 D9 D10 D11 |
| Fast Read Quad Output with 4-Byte Address | 6Ch | 24 | - | CA15-8 | CA7-0 | Dummy | | | D0 D1 D2 D3 |
| Fast Read Dual I/O | BBh | 4 | 8 | CA15-0 | Dummy D0 | D1 D2 | D3 D4 | D5 D6 | D7 D8 |
| Fast Read Dual I/O with 4-Byte Address | BCh | 12 | 8 | CA15-0 | Dummy | D0 | D1 D2 | D3 D4 | D5 D6 |
| Fast Read Quad I/O | EBh | 4 | 8 | CA15-0 Dummy | D0 D1 D2 D3 | D4 D5 D6 D7 | D8 D9 D10 D11 | D12 D13 D14 D15 | D16 D17 D18 D19 |
| Fast Read Quad I/O with 4-Byte Address | ECh | 10 | 8 | CA15-0 Dummy | D0 | D1 D2 D3 | D4 D5 D6 D7 | D8 D9 D10 D11 | D12 D13 D14 D15 D16 |
| DTR Fast Read | 0Dh | 8 | - | CA15-0 | Dummy | D0 D1 | D2 D3 | D4 D5 | D6 D7 |
| DTR Fast Read with 4-Byte Address | 0Eh | 14 | - | CA15-0 | Dummy | D0 | D1 D2 | D3 D4 | D5 … |
| DTR Fast Read Dual Output | 3Dh | 8 | - | CA15-0 | Dummy | D0 D1 D2 | D3 D4 D5 D6 | D7 D8 D9 D10 | D11 D12 D13 D14 D15 |
| DTR Fast Read Quad Output | 6Dh | 8 | - | CA15-0 | Dummy | D0 D1 D2 D3 D4 D5 | D6 D7 D8 D9 D10 D11 D12 D13 | D14 D15 D16 D17 D18 D19 D20 D21 | D22 D23 D24 D25 D26 D27 D28 D29 D30 D31 |
| DTR Fast Read Dual I/O | BDh | 8 | - | CA15-0 Dummy | D0 | D1 D2 D3 D4 | D5 D6 D7 D8 | D9 D10 D11 D12 | D13 D14 D15 D16 D17 |
| DTR Fast Read Dual I/O with 4-Byte Address | BEh | 10 | - | CA15-0 Dummy | D0 | D1 D2 D3 | D4 D5 D6 D7 | D8 D9 D10 D11 | D12 D13 D14 D15 D16 |
| DTR Fast Read Quad I/O | EDh | 8 | - | CA15-0 Dummy | D0 D1 D2 D3 D4 D5 | D6 D7 D8 D9 D10 D11 | D12 D13 D14 D15 D16 D17 D18 D19 | D20 D21 D22 D23 D24 D25 D26 D27 | D28 D29 D30 D31 D32 D33 D34 D35 D36 D37 |
| DTR Fast Read Quad I/O with 4-Byte Address | EEh | 10 | - | CA15-0 Dummy | D0 D1 D2 D3 D4 D5 | D6 D7 D8 D9 D10 D11 | D12 D13 D14 D15 D16 D17 D18 D19 | D20 D21 D22 D23 D24 D25 D26 D27 | D28 D29 D30 D31 D32 D33 D34 D35 |



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**Notes:**

1. ***Output*** designates data output from the device.

2. Column Address (CA) only requires CA[11:0], CA[15:12] are considered as dummy bits.

3. Page Address (PA) requires 16 bits. PA[15:6] is the address for 128KB blocks (total 1,024 blocks), PA[5:0] is the address for 2KB pages (total 64 pages for each block).

4. Logical and Physical Block Address (LBA & PBA) each consists of 16 bits. LBA[9:0] & PBA[9:0] are effective Block Addresses. LBA[15:14] is used for additional information.

5. Status Register Addresses:
   Status Register 1 / Protection Register: Addr = Axh
   Status Register 2 / Configuration Register: Addr = Bxh
   Status Register 3 / Status Register: Addr = Cxh

6. Dual SPI Address Input (**CA15-8** and **CA7-0**) format:
   IO0 = x, x, CA10, CA8, CA6, CA4, CA2, CA0
   IO1 = x, x, CA11, CA9, CA7, CA5, CA3, CA1

7. Dual SPI Data Output (***D7-0***) format:
   IO0 = D6, D4, D2, D0, ……
   IO1 = D7, D5, D3, D1, ……

8. Quad SPI Address Input (**CA15-8** and **CA7-0**) format:
   IO0 = x, CA8, CA4, CA0
   IO1 = x, CA9, CA5, CA1
   IO2 = x, CA10, CA6, CA2
   IO3 = x, CA11, CA7, CA3

9. Quad SPI Data Input/Output (***D7-0***) format:
   IO0 = D4, D0, ……
   IO1 = D5, D1, ……
   IO2 = D6, D2, ……
   IO3 = D7, D3, ……

10. All Quad Program/Read commands are disabled when WP-E bit is set to 1 in the Protection Register.

11. For all Read operations in the Continuous Read Mode, once the /CS signal is brought to high to terminate the read operation, the device will still remain busy for tRD3 (BUSY=1), and all the data inside the Data buffer will be lost and un-reliable to use. A new Page Data Read instruction must be issued to reload the correct page data into the Data Buffer.

12. For all Read operations in the Buffer Read Mode, as soon as /CS signal is brought to high to terminate the read operation, the device will be ready to accept new instructions and all the data inside the Data Buffer will remain unchanged from the previous Page Data Read instruction.



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## 8.2 Instruction Descriptions

### 8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)

Once the Reset instruction is accepted, any on-going internal operations will be terminated and will take approximately tRST to reset. It depending on the current operation the device is performing, tRST can be 5us~500us. During this period, no command will be accepted. After the execution of the Reset instruction is completed, the each bits of Status Register will follow the following table.

If there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device, data corruption may happen at only the address that is the target of the on-going operation. It is recommended to check the BUSY bit in Status Register before issuing the Reset command.

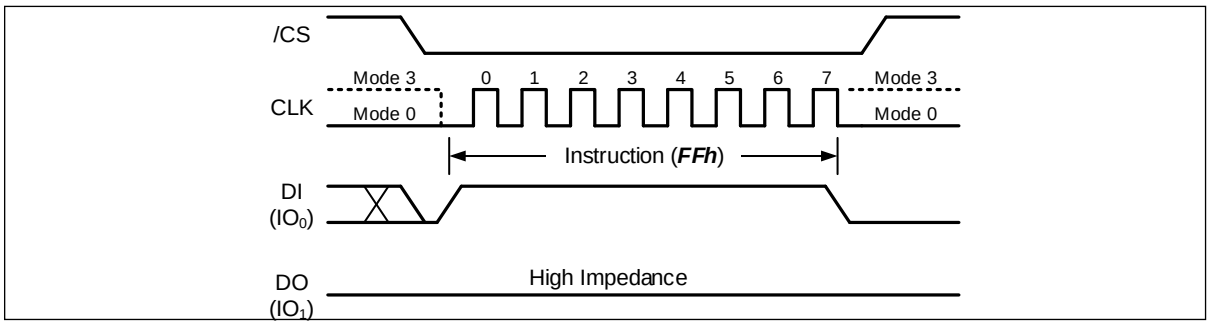



Figure 8-1 Device Reset Instruction (FFh)

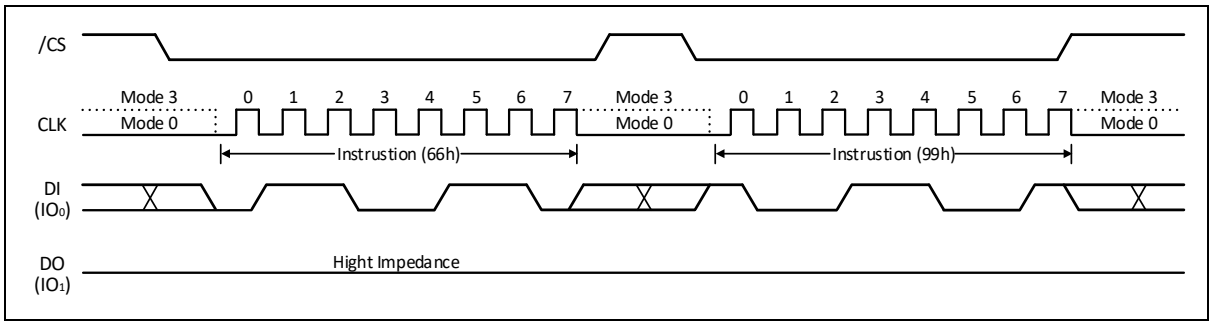



Figure 8-2 Device Reset Instruction (66h+99h)



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| Register | Address | Bits | | Shipment Default | Power Up after LUT is full | Power Up after OTP area locked | Power Up after SR-1 locked | After Reset cmd (FFh) | After Reset cmd (66h+99h) or HW RESET |
|---|---|---|---|---|---|---|---|---|---|
| Status Register-1 | Axh | S7 | SRP0 | 0 | 0 | 0 | 1 (locked) | No Change | 0 |
| | | S6 | BP3 | 1 | 1 | 1 | x (locked) | No Change | 1 |
| | | S5 | BP2 | 1 | 1 | 1 | x (locked) | No Change | 1 |
| | | S4 | BP1 | 1 | 1 | 1 | x (locked) | No Change | 1 |
| | | S3 | BP0 | 1 | 1 | 1 | x (locked) | No Change | 1 |
| | | S2 | TB | 1 | 1 | 1 | x (locked) | No Change | 1 |
| | | S1 | WP-E | 0 | 0 | 0 | x (locked) | No Change | 0 |
| | | S0 | SRP1 | 0 | 0 | 0 | 1 (locked) | No Change | 0 |
| Status Register-2 | Bxh | S7 | OTP-L | 0 | 0 | 1 | 0 | Clear to 0 befor OTP set | Clear to 0 before OTP set |
| | | S6 | OTP-E | 0 | 0 | 0 | 0 | 0 | 0 |
| | | S5 | SR1-L | 0 | 0 | 0 | 1 | Clear to 0 befor OTP set | Clear to 0 before OTP set |
| | | S4 | ECC-E | 1 | 1 | 1 | 1 | No Change | 1 |
| | | S3 | BUF W25N01JWxxxG | 1 | 1 | 1 | 1 | No Change | 1 |
| | | | BUF W25N01JWxxxT | 0 | 0 | 0 | 0 | No Change | 0 |
| | | S2 | Reserved | - | - | - | - | - | - |
| | | S1 | Reserved | - | - | - | - | - | - |
| | | S0 | QE | 1 | 1 | 1 | 1 | No Change | 1 |
| Status Register-3 | Cxh | S7 | Reserved | - | - | - | - | - | - |
| | | S6 | LUT-F | 0 | 1 | 0 | 0 | No Change | 0 (1) |
| | | S5 | ECC-1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | S4 | ECC-0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | S3 | P-FAIL | 0 | 0 | 0 | 0 | 0 | 0 |
| | | S2 | E-FAIL | 0 | 0 | 0 | 0 | 0 | 0 |
| | | S1 | WEL | 0 | 0 | 0 | 0 | 0 | 0 |
| | | S0 | BUSY | 0 | 0 | 0 | 0 | 0 | 0 |
| Status Register-4 | Dxh | S7 | Reserved | - | - | - | - | - | - |
| | | S6 | ODS1 | 0 | 0 | 0 | 0 | No Change | 0 |
| | | S5 | ODS0 | 0 | 0 | 0 | 0 | No Change | 0 |
| | | S4 | Reserved | - | - | - | - | - | - |
| | | S3 | DLP-E | 0 | 0 | 0 | 0 | No Change | 0 |
| | | S2 | HS | 0 | 0 | 0 | 0 | No Change | 0 |
| | | S1 | Reserved | - | - | - | - | - | - |
| | | S0 | Reserved | - | - | - | - | - | - |
| Extended Register | - | DLP[7:0] | | 00110100 | 00110100 | 00110100 | 00110100 | No Change | 00110100 |

Default values of the Status Registers after power up and Device Reset

**Notes:**

1. If LUT is full, the bit indicates to "1" after Reset command (66h+99h) and HW RESET.

| | During Power Up sequence | After Reset cmd (FFh) | After Reset cmd (66h+99h) or HW RESET |
|---|---|---|---|
| Auto Page Data Read (13h) (1) | Execute | Execute | Execute |

Auto Page Data Read (13h) execution during power up and after Device Reset

**Notes:**

1. Automatically execution of Page Data Read (13h) command for Block0, Page0.



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### 8.2.2 Read JEDEC ID (9Fh)

The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh” followed by 8 dummy clocks.

The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes are then shifted out on the falling edge of CLK with most significant bit (MSB) first. For memory type and capacity values refer to Manufacturer and Device Identification table.

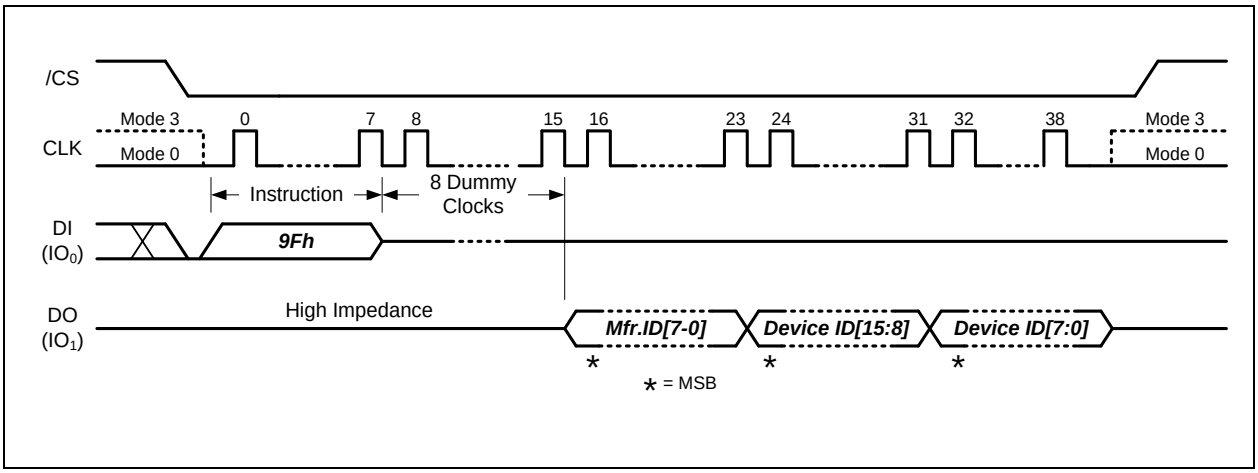



Figure 8-3 Read JEDEC ID Instruction



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### 8.2.3 Read Status Register (0Fh / 05h)

The Read Status Register instructions allow the 8-bits Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “0Fh or 05h” into the DI pin on the rising edge of CLK followed by 8-bits Status Register Address. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. Refer to section 7 for Status Register descriptions.

The read status register instruction can be used, even while a Program or Erase cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously. The instruction is completed by driving /CS high.

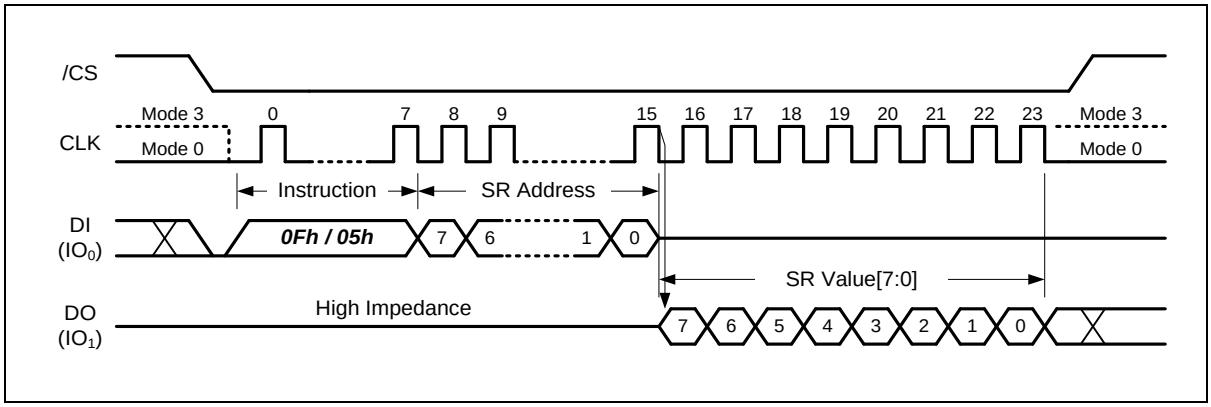



Figure 8-4 Read Status Register Instruction



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### 8.2.4 Write Status Register (1Fh / 01h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP[1:0], TB, BP[3:0] and WP-E bit in Status Register-1; OTP-L, OTP-E, SR1-L, ECC-E and BUF bit in Status Register-2. All other Status Register bits locations are read-only and will not be affected by the Write Status Register instruction.

To write the Status Register bits, the instruction is entered by driving /CS low, sending the instruction code “1Fh or 01h”, followed by 8-bits Status Register Address, and then writing the status register data byte. Refer to section 7 for Status Register descriptions. After power up, factory default for BP[3:0], TB, ECC-E bits are 1, while other bits are 0.

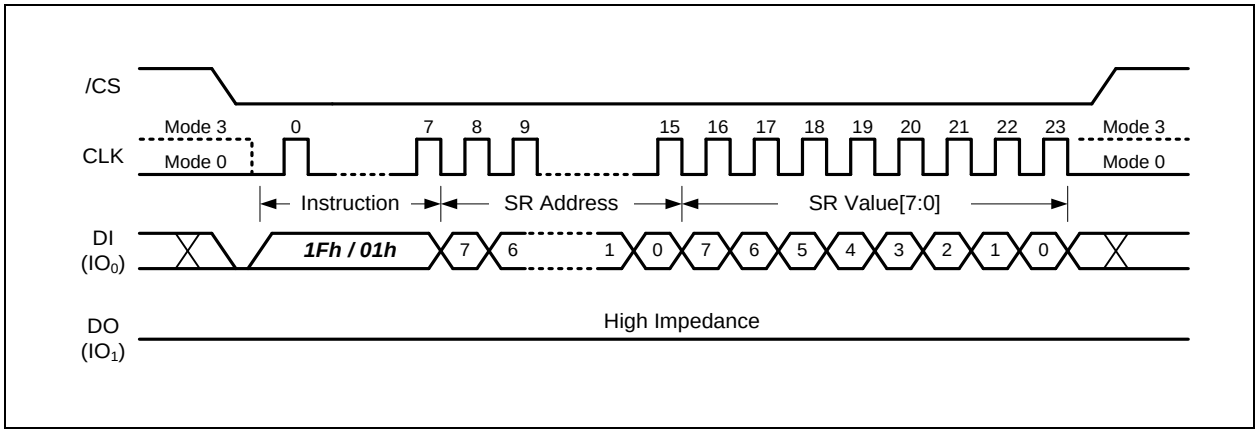



Figure 8-5 Write Status Register-1/2/3 Instruction

### 8.2.5 Write Data Learning Pattern (4Ah)

The Data Learning Pattern can be defined by a "Write Data Learning Pattern (4Ah)" command followed by 8-bits user-defined pattern. The user defined pattern is volatile. After device power cycle, the Data Learning Pattern will return to its "00110100" default value.

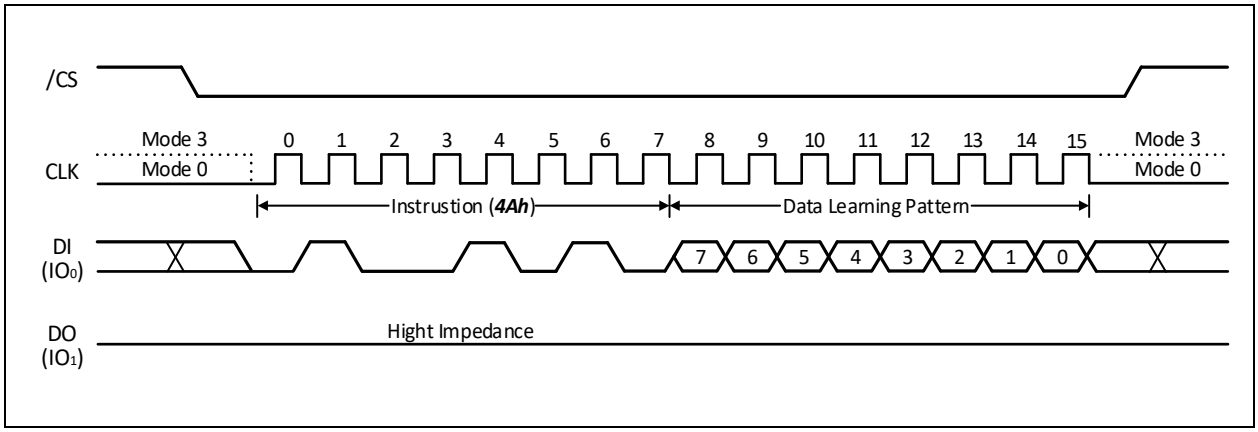



Figure 8-6 Write Data Learning Pattern



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### 8.2.6 Write Enable (06h)

The Write Enable instruction sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program and Block Erase instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

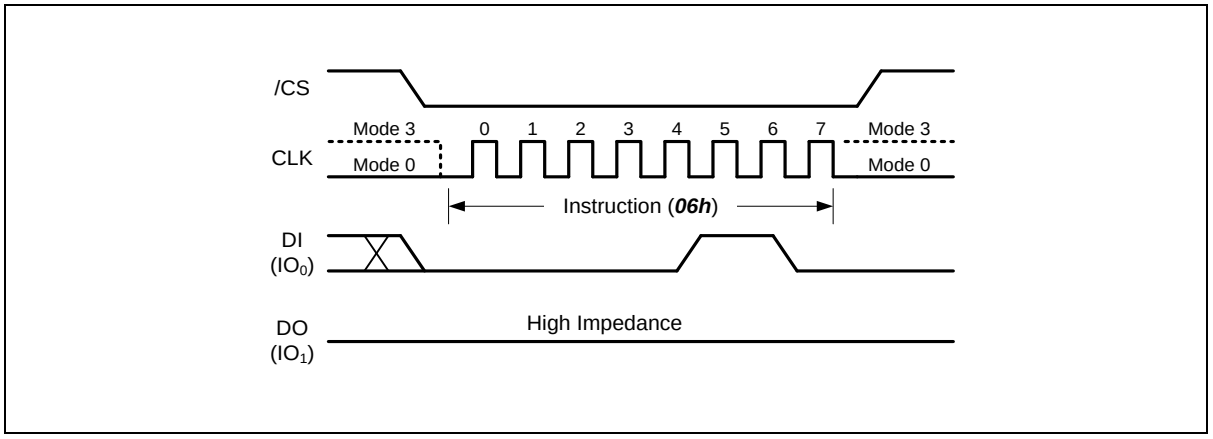



Figure 8-7 Write Enable Instruction

### 8.2.7 Write Disable (04h)

The Write Disable instruction resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Page Program, Quad Page Program, Block Erase and Reset and Bad Block Management instructions.

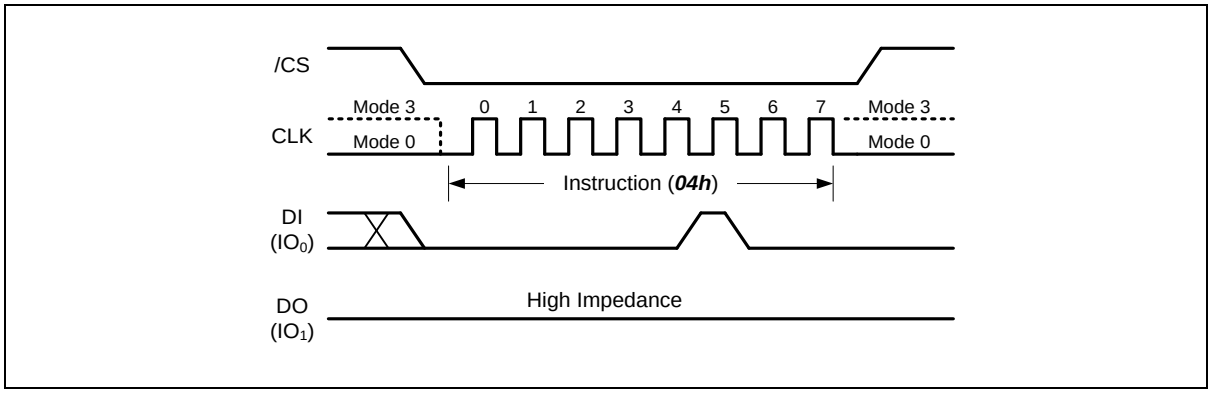



Figure 8-8 Write Disable Instruction



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### 8.2.8 Bad Block Management (A1h)

Due to large NAND memory density size and the technology limitation, NAND memory devices are allowed to be shipped to the end customers with certain amount of “Bad Blocks” found in the factory testing. Up to 2% of the memory blocks can be marked as “Bad Blocks” upon shipment, which is a maximum of 20 blocks for W25N01JW. In order to identify these bad blocks, it is recommended to scan the entire memory array for bad block markers set in the factory. A “Bad Block Marker” is a non-FFh data byte stored at Byte 0 of Page 0 for each bad block. An additional marker is also stored in the first two bytes of the 64-Byte spare area.

W25N01JW offers a convenient method to manage the bad blocks typically found in NAND flash memory after extensive use. The “Bad Block Management” command is initiated by shifting the instruction code “A1h” into the DI pin and followed by the 16-bits “Logical Block Address” and 16-bits “Physical Block Address”. The logical block address is the address for the “bad” block that will be replaced by the “good” block indicated by the physical block address.

A Write Enable instruction must be executed before the device will accept the Bad Block Management instruction (Status Register bit WEL=1). The Bad Block Management instruction is initiated by driving the /CS pin low and shifting the instruction code “A1h” followed by 16-bits LBA (Bad Block address) and the 16-bits PBA (Good Block address). After /CS is driven high to complete the instruction cycle, the self-timed Bad Block Management instruction will commence for a time duration of tPP (See AC Characteristics). While the Bad Block Management cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Bad Block Management cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Bad Block Management cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

Once a Bad Block Management command is successfully executed, the specified LBA-PBA link will be added to the internal Look Up Table (LUT). Up to 20 links can be established in the non-volatile LUT. If all 20 links have been written, the LUT-F bit in the Status Register will become a 1, and no more LBA-PBA links can be established. Therefore, prior to issuing the Bad Block Management command, the LUT-F bit value can be checked or a “Read BBM Look Up Table” command can be issued to confirm if spare links are still available in the LUT.

To guarantee a continuous read operation on the first 1,000 blocks, the manufacturer may have used some of the BBM LUT entrees. It is advisable for the user to scan all blocks and keep a table of all manufacturer bad blocks prior to first erase/program operation.

Registering the same address in multiple PBAs is prohibited. It may cause unexpected behavior.

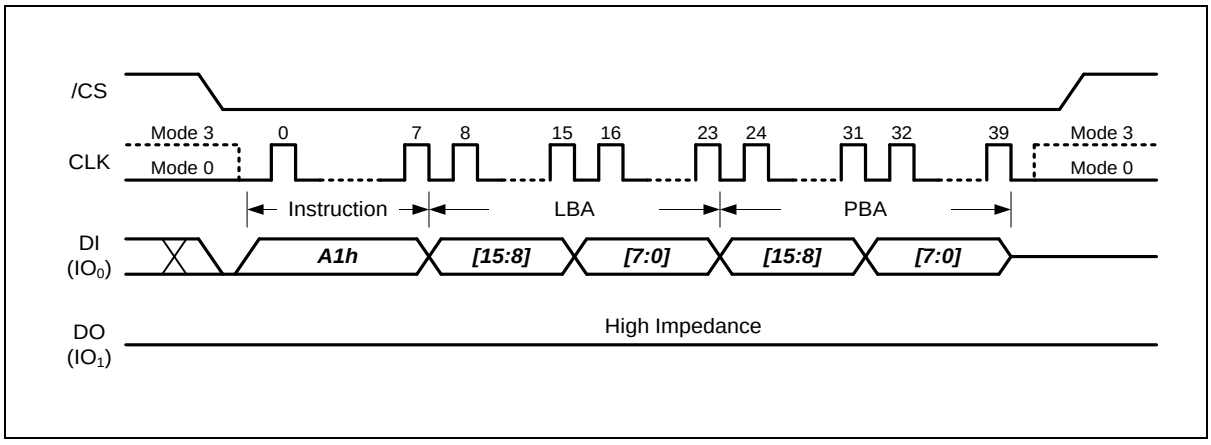



Figure 8-9 Bad Block Management Instruction



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### 8.2.9 Read BBM Look Up Table (A5h)

The internal Look Up Table (LUT) consists of 20 Logical-Physical memory block links (from LBA0/PBA0 to LBA19/PBA19). The “Read BBM Look Up Table” command can be used to check the existing address links stored inside the LUT.

The “Read BBM Look Up Table” command is initiated by shifting the instruction code “A5h” into the DI pin and followed by 8-bits dummy clocks, at the falling edge of the 16th clocks, the device will start to output the 16-bits “Logical Block Address” and the 16-bits “Physical Block Address” as illustrated in Figure 8-10. All block address links will be output sequentially starting from the first link (LBA0 & PBA0) in the LUT. If there are available links that are unused, the output will contain all “00h” data.

The MSB bits LBA[15:14] of each link are used to indicate the status of the link.

| LBA[15] (Enable) | LBA[14] (Invalid) | Descriptions |
|---|---|---|
| 0 | 0 | This link is available to use. |
| 1 | 0 | This link is enabled and it is a valid link. |
| 1 | 1 | This link was enabled, but it is not valid any more. |
| 0 | 1 | Not applicable. |

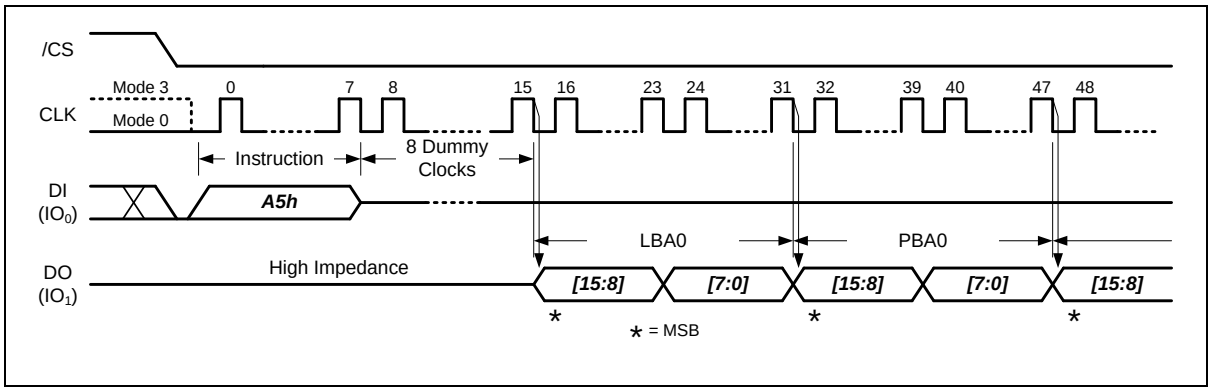



Figure 8-10 Read BBM Look Up Table Instruction



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### 8.2.10 Last ECC Failure Page Address (A9h)

To better manage the data integrity, W25N01JW implements internal ECC correction for the entire memory array. When the ECC-E bit in the Status/Configuration Register is set to 1 (also power up default), the internal ECC algorithm is enabled for all Program and Read operations. During a “Program Execute” command for a specific page, the ECC algorithm will calculate the ECC information based on the data inside the 2K-Byte data buffer and write the ECC data into the extra 64-Byte ECC area in the same physical memory page.

During the Read operations, ECC information will be used to verify the data read out from the physical memory array and possible corrections can be made to limited amount of data bits that contain errors. The ECC Status Bits (ECC-1 & ECC-0) will also be set indicating the result of ECC calculation.

For the “Continuous Read Mode (BUF=0)” operation, multiple pages of main array data can be read out continuously by issuing a single read command. Upon finishing the read operation, the ECC status bits should be check to verify if there’s any ECC correction or un-correctable errors existed in the read out data. If ECC-1 & ECC-0 equal to (1, 0) or (1, 1), the previous read out data contain one or more pages that contain ECC un-correctable errors.

The failure page address (or the last page address if it’s multiple pages) can be obtained by issuing the “Last ECC failure Page Address” command. The 16-bits Page Address that contains un-correctable ECC errors will be presented on the DO pin following the instruction code “A9h” and 8-bits dummy clocks on the DI pin.

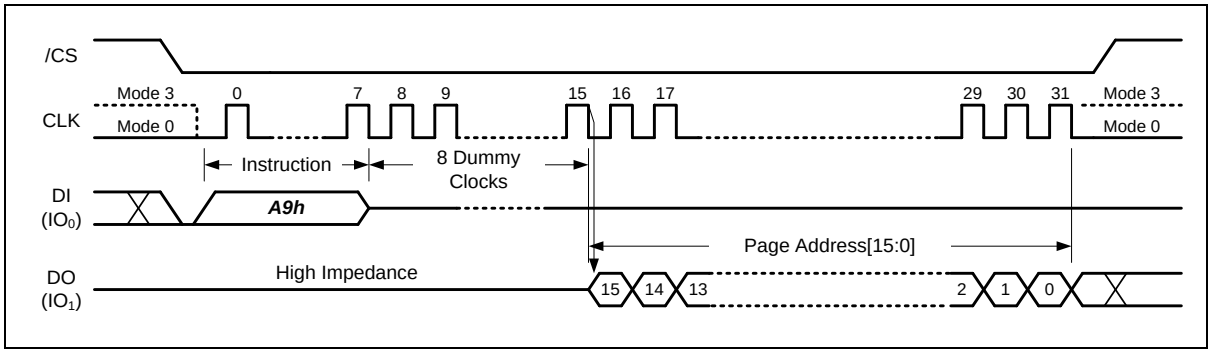



Figure 8-11 Last ECC Failure Page Address Instruction



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### 8.2.11 Deep Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h".

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power-down instruction will not be executed. After /CS is driven high, the deep power-down state will entered within the time duration of tDP (See AC Characteristics).

While in the deep power-down state only the Release Deep Power-down (ABh) and Devise Reset (FFh or 66h/99h) instructions, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring almost instructions makes the Deep Power-down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

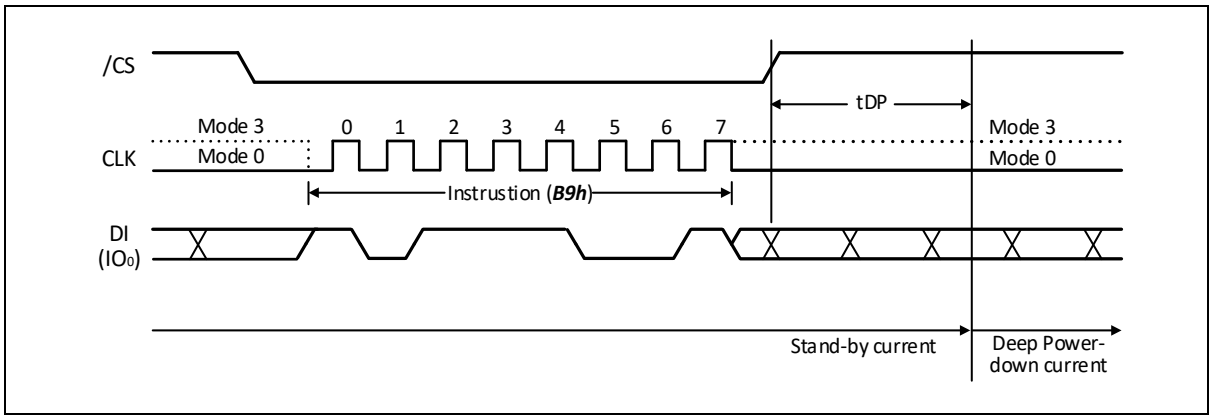



Figure 8-12 Deep Power-down Instruction



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### 8.2.12 Release Deep Power-down (ABh)

The Release Deep Power-down instruction can be used to release the device from the power-down state. To release the device from the deep power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high. Release from deep power-down state will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration.

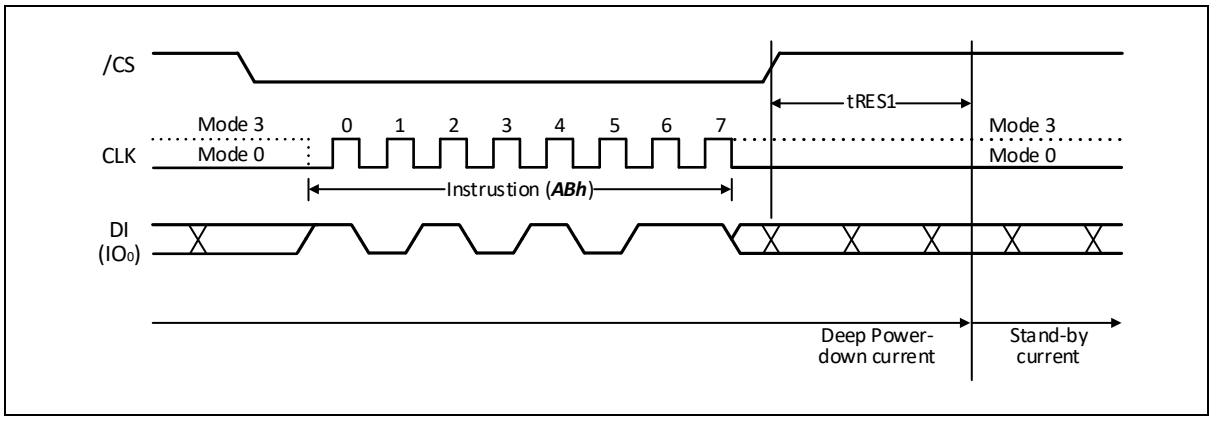



Figure 8-13 Release Deep Power-down Instruction



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### 8.2.13 128KB Block Erase (D8h)

The 128KB Block Erase instruction sets all memory within a specified block (64-Pages, 128K-Bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed by 8-bits dummy clocks and the 16-bits page address. The Block Erase instruction sequence is shown in below.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of $t_{BE}$ (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again.

After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed block is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits.

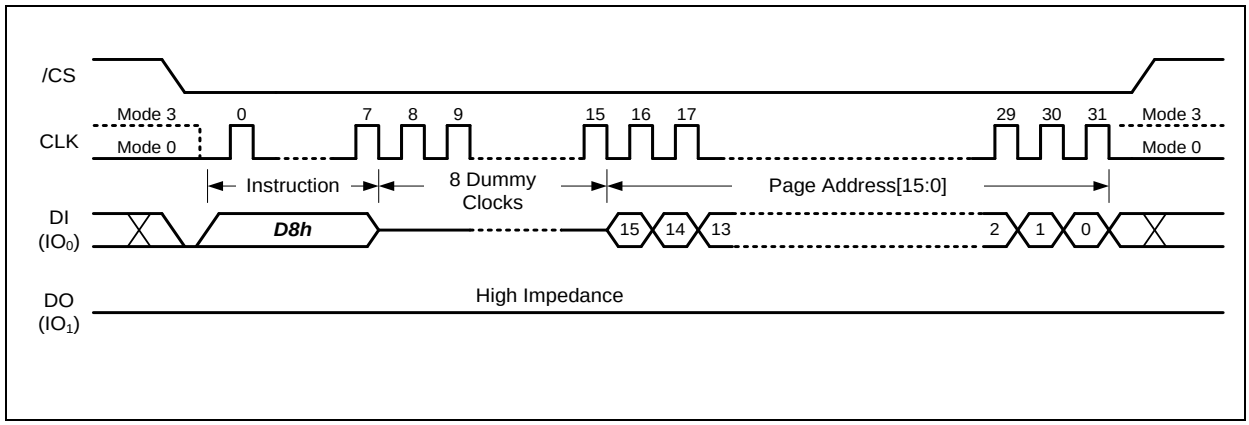



Figure 8-14 128KB Block Erase Instruction



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### 8.2.14 Load Program Data (02h) / Random Load Program Data (84h)

The Program operation allows from one byte to 2,112 bytes (a page) of data to be programmed at previously erased (FFh) memory locations.

A Program operation involves two steps:

1. Load the program data into the Data Buffer.
2. Issue “Program Execute” command to transfer the data from Data Buffer to the specified memory page.

A Write Enable instruction must be executed before the device will accept the Load Program Data Instructions (Status Register bit WEL=1). The “Load Program Data” or “Random Load Program Data” instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” or “84h” followed by a 16-bits column address (only CA[11:0] is effective). The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device. The Load Program Data instruction sequence is shown in below.

Both “Load Program Data” and “Random Load Program Data” instructions share the same command sequence. The difference is that “Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

If internal ECC algorithm is enabled, all 2,112 bytes of data will be accepted, but the bytes designated for ECC parity bits in the extra 64 bytes section will be overwritten by the ECC calculation. If the ECC-E bit is set to a 0 to disable the internal ECC, the extra 64 bytes section can be used for external ECC purpose or other usage.

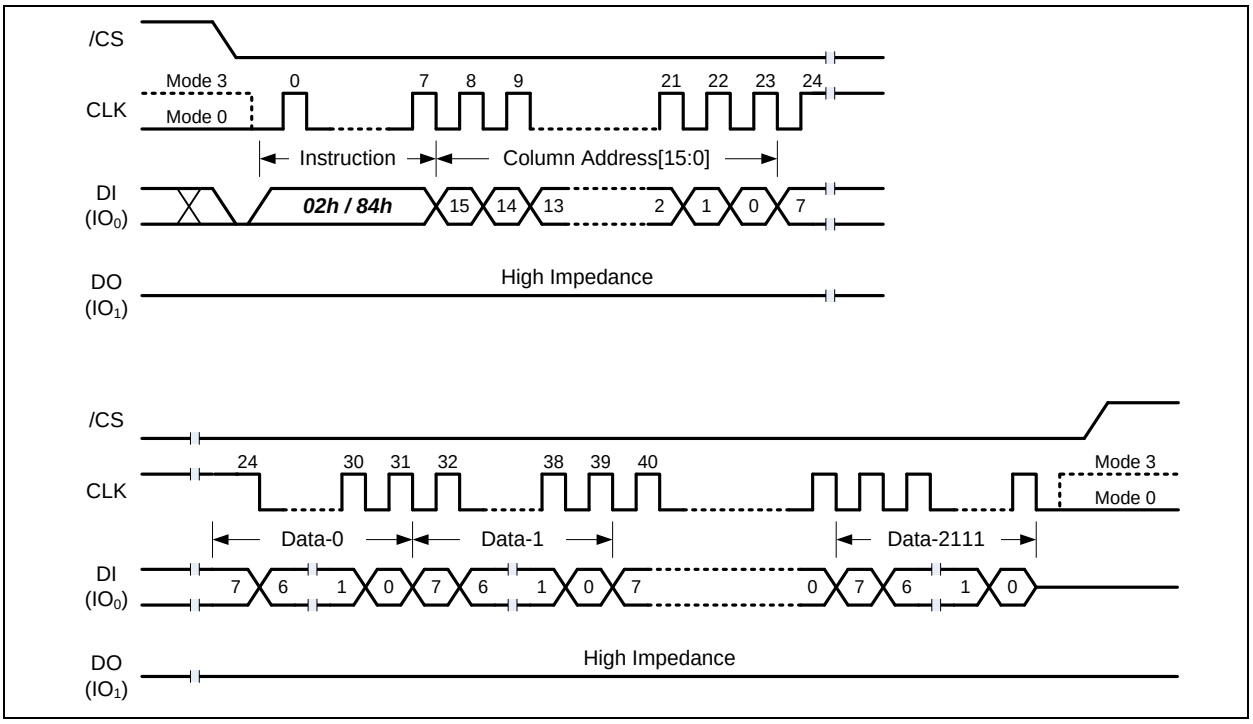



Figure 8-15 Load / Random Load Program Data Instruction



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### 8.2.15 Quad Load Program Data (32h) / Quad Random Load Program Data (34h)

The “Quad Load Program Data” and “Quad Random Load Program Data” instructions are identical to the “Load Program Data” and “Random Load Program Data” in terms of operation sequence and functionality. The only difference is that “Quad Load” instructions will input the data bytes from all four IO pins instead of the single DI pin. This method will significantly shorten the data input time when a large amount of data needs to be loaded into the Data Buffer. The instruction sequence is shown in below.

Both “Quad Load Program Data” and “Quad Random Load Program Data” instructions share the same command sequence. The difference is that “Quad Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Quad Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

When WP-E bit in the Status Register is set to a 1, all Quad SPI instructions are disabled.

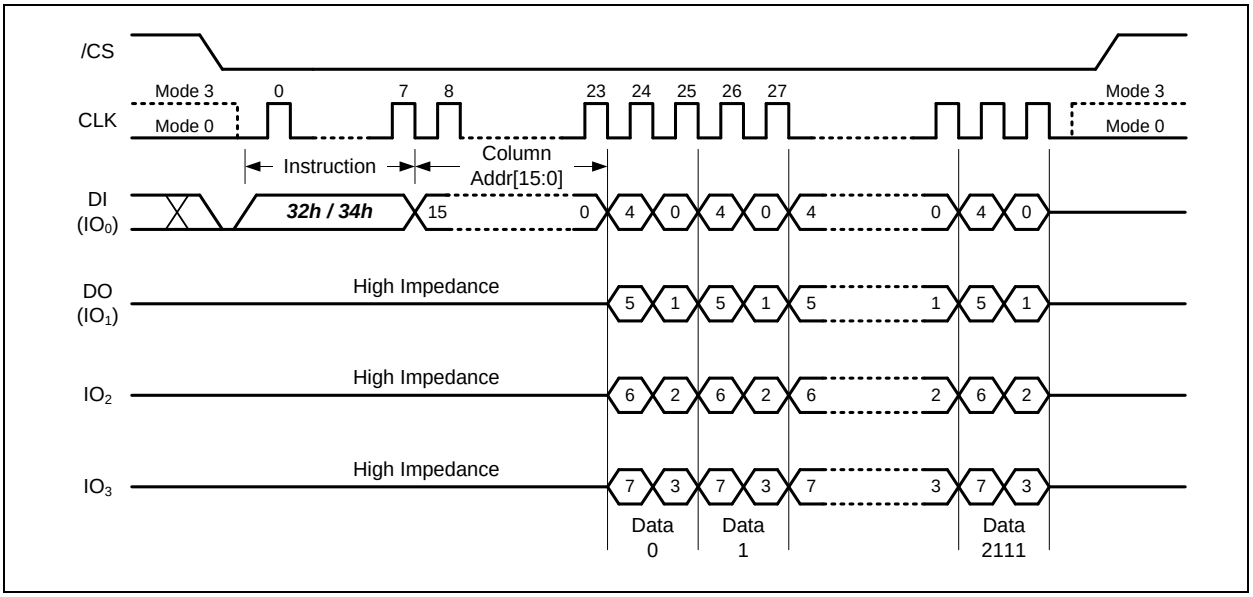



Figure 8-16 Quad Load / Quad Random Load Program Data Instruction



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### 8.2.16 Program Execute (10h)

The Program Execute instruction is the second step of the Program operation. After the program data are loaded into the 2,112-Byte Data Buffer (or 2,048 bytes when ECC is enabled), the Program Execute instruction will program the Data Buffer content into the physical memory page that is specified in the instruction. The instruction is initiated by driving the /CS pin low then shifting the instruction code “10h” followed by 8-bits dummy clocks and the 16-bits Page Address into the DI pin.

After /CS is driven high to complete the instruction cycle, the self-timed Program Execute instruction will commence for a time duration of tPP (See AC Characteristics). While the Program Execute cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Program Execute cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Execute cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits.

The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. Programming pages out of sequence is prohibited.

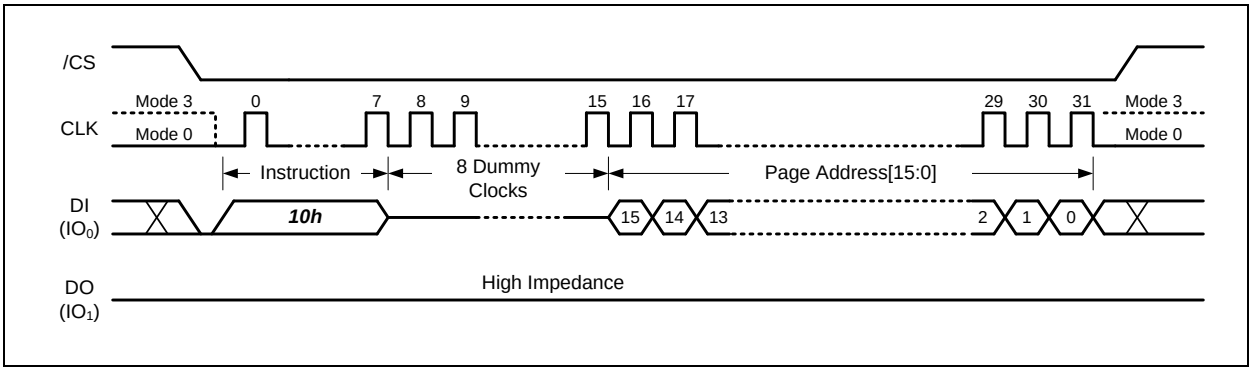



Figure 8-17 Program Execute Instruction



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### 8.2.17 Page Data Read (13h)

The Page Data Read instruction will transfer the data of the specified memory page into the 2,112-Byte Data Buffer. The instruction is initiated by driving the /CS pin low then shifting the instruction code “13h” followed by 8-bits dummy clocks and the 16-bits Page Address into the DI pin.

After /CS is driven high to complete the instruction cycle, the self-timed Read Page Data instruction will commence for a time duration of tRD1 or tRD2 (See AC Characteristics). While the Read Page Data cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Read Page Data cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again.

After the 2,112 bytes of page data are loaded into the Data Buffer, several Read instructions can be issued to access the Data Buffer and read out the data. Depending on the BUF bit setting in the Status Register, either “Buffer Read Mode” or “Continuous Read Mode” may be used to accomplish the read operations.

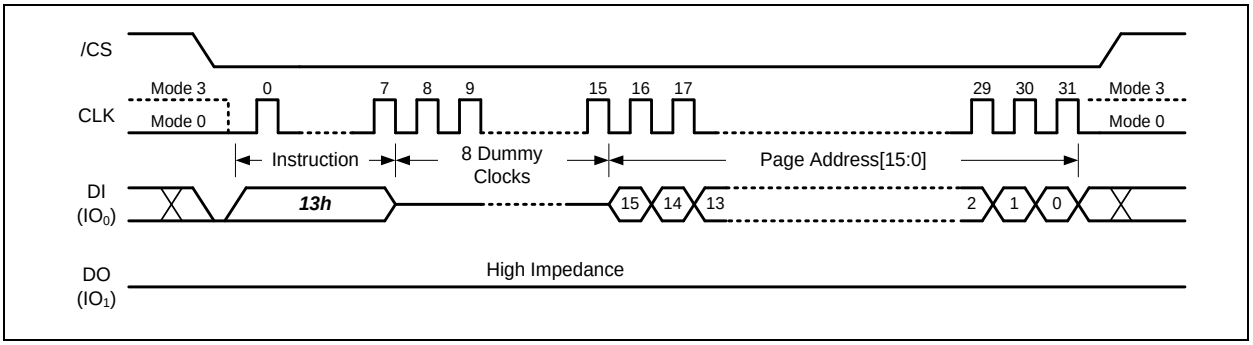



Figure 8-18 Page Data Read Instruction



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### 8.2.18 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Read Data instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by the 16-bits Column Address and 8-bits dummy clocks or a 24-bits dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond’s SpiFlash NOR flash memory command sequence.

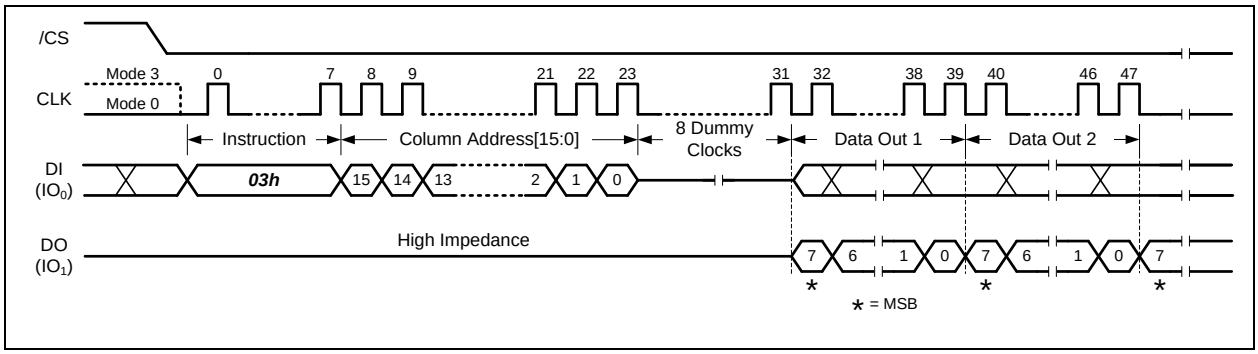



Figure 8-19 Read Data Instruction (Buffer Read Mode, BUF=1)

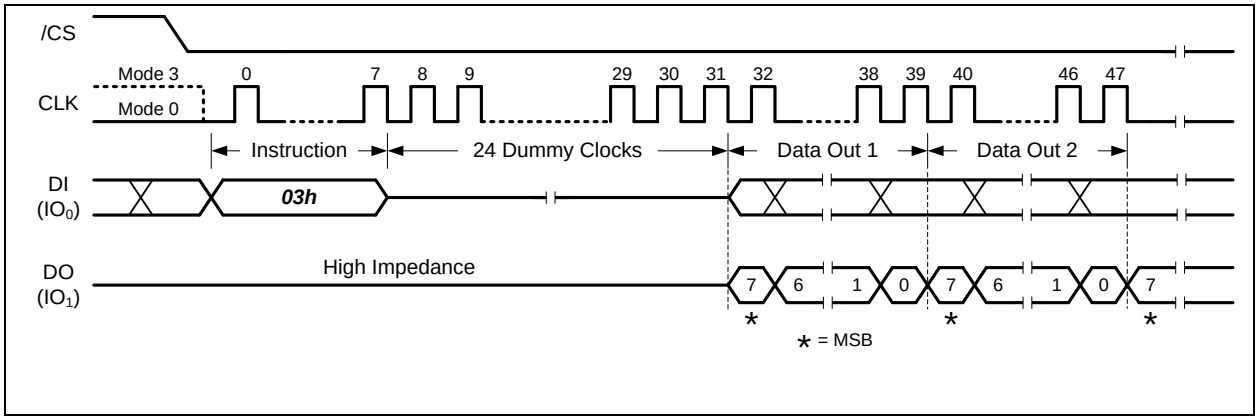



Figure 8-20 Read Data Instruction (Continuous Read Mode, BUF=0)



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### 8.2.19 Fast Read (0Bh)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Bh” followed by the 16-bits Column Address and 8-bits dummy clocks or a 32-bits dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond’s SpiFlash NOR flash memory command sequence.

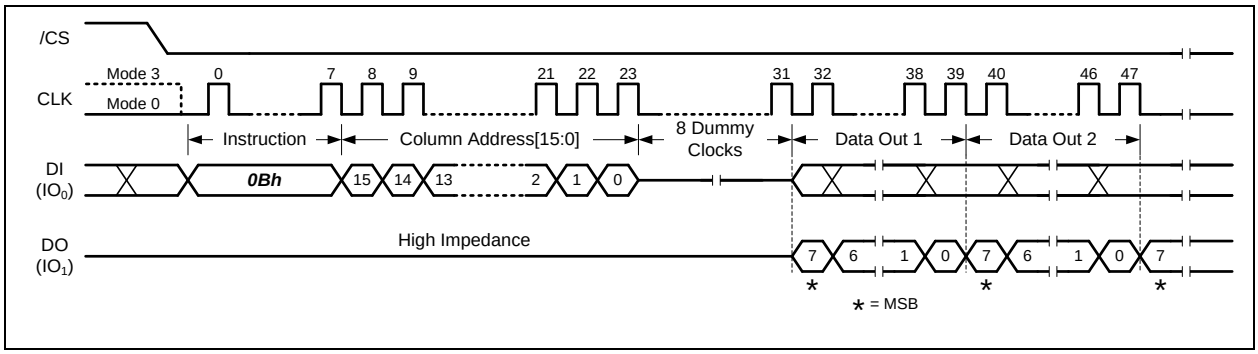



Figure 8-21 Fast Read Instruction (Buffer Read Mode, BUF=1)

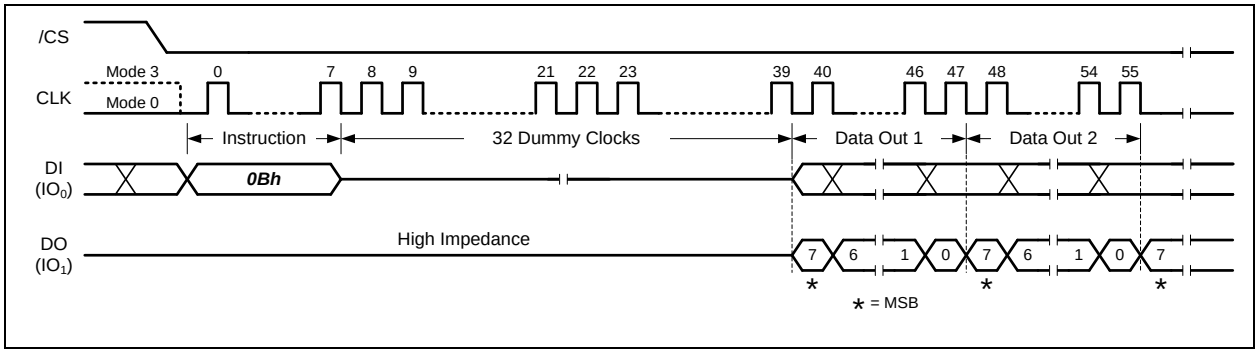



Figure 8-22 Fast Read Instruction (Continuous Read Mode, BUF=0)



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### 8.2.20 Fast Read with 4-Byte Address (0Ch)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Ch” followed by the 16-bits Column Address and 24-bits dummy clocks (when BUF=1) or 40-bits dummy clocks (when BUF=0) into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond’s SpiFlash NOR flash memory command sequence.

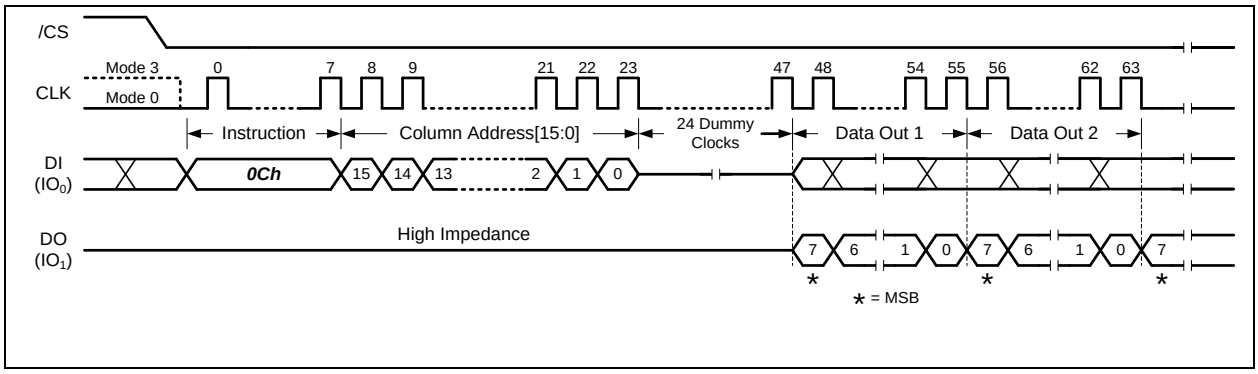



Figure 8-23 Fast Read with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

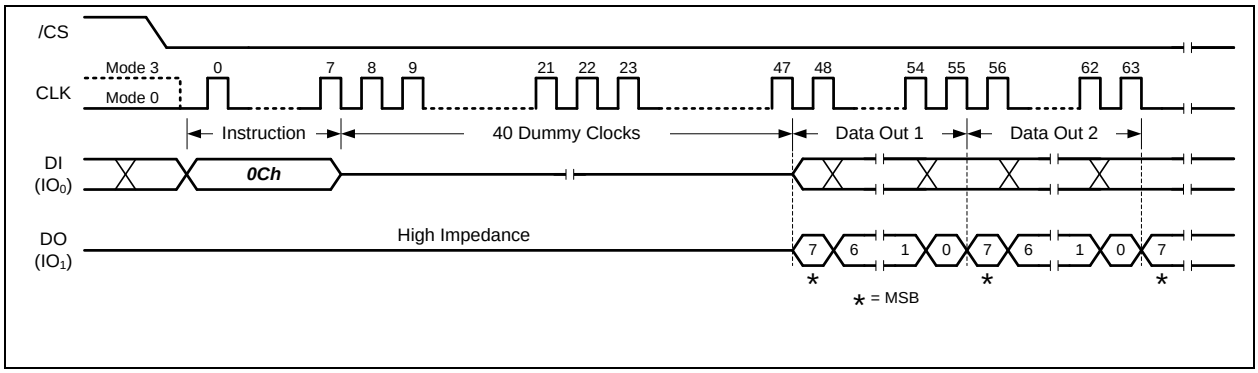



Figure 8-24 Fast Read with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)



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### 8.2.21 Fast Read Dual Output (3Bh)

The Fast Read Dual Output instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; $IO_0$ and $IO_1$. This allows data to be transferred at twice the rate of standard SPI devices.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

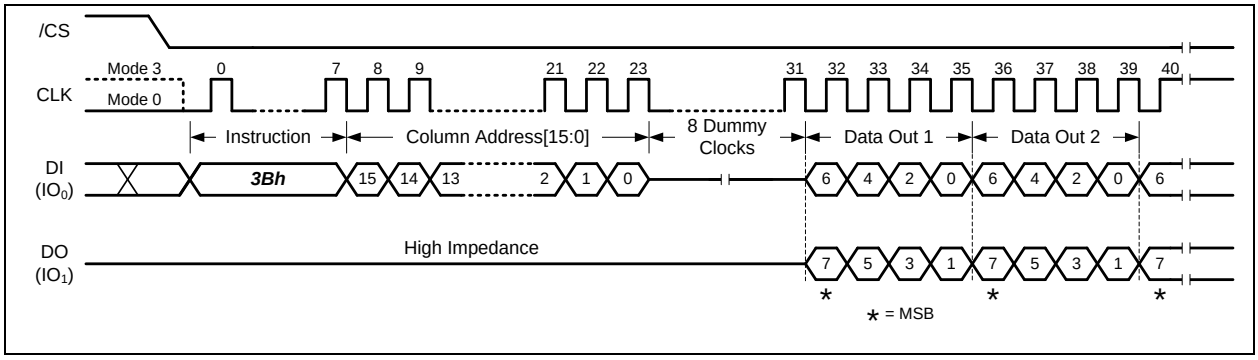



Figure 8-25 Fast Read Dual Output Instruction (Buffer Read Mode, BUF=1)

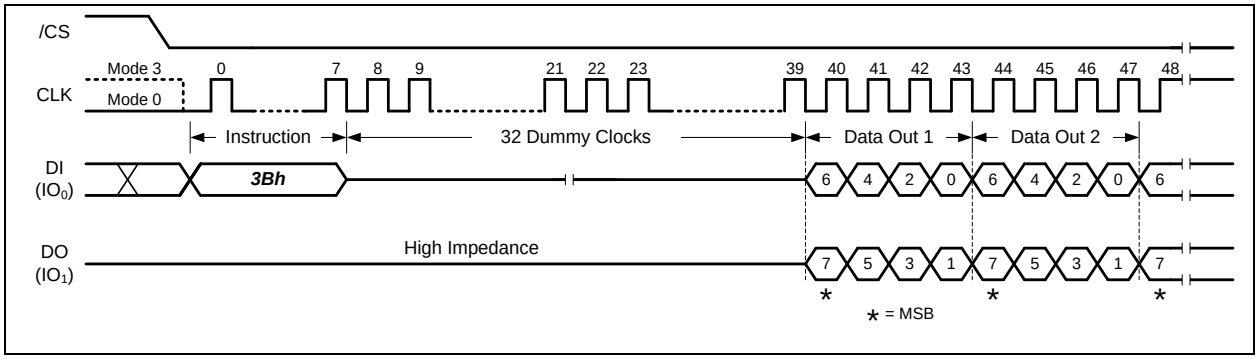



Figure 8-26 Fast Read Dual Output Instruction (Continuous Read Mode, BUF=0)



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### 8.2.22 Fast Read Dual Output with 4-Byte Address (3Ch)

The Fast Read Dual Output instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; $IO_0$ and $IO_1$. This allows data to be transferred at twice the rate of standard SPI devices.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

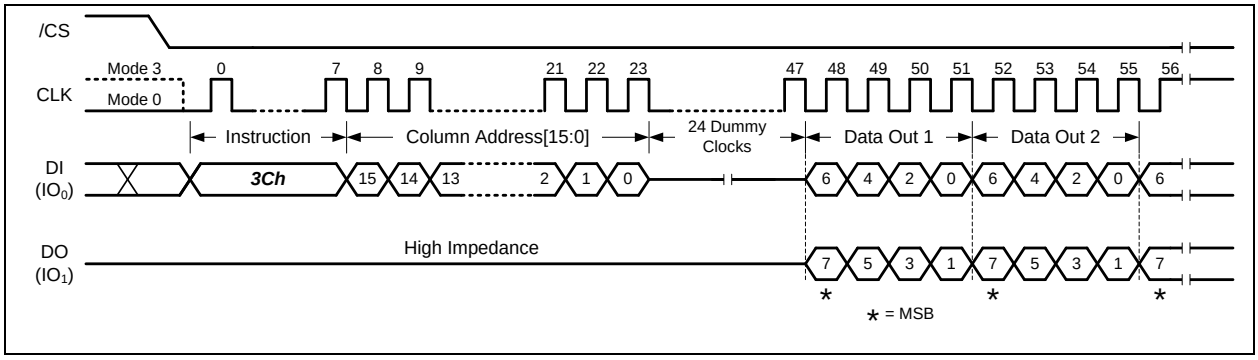



Figure 8-27 Fast Read Dual Output with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

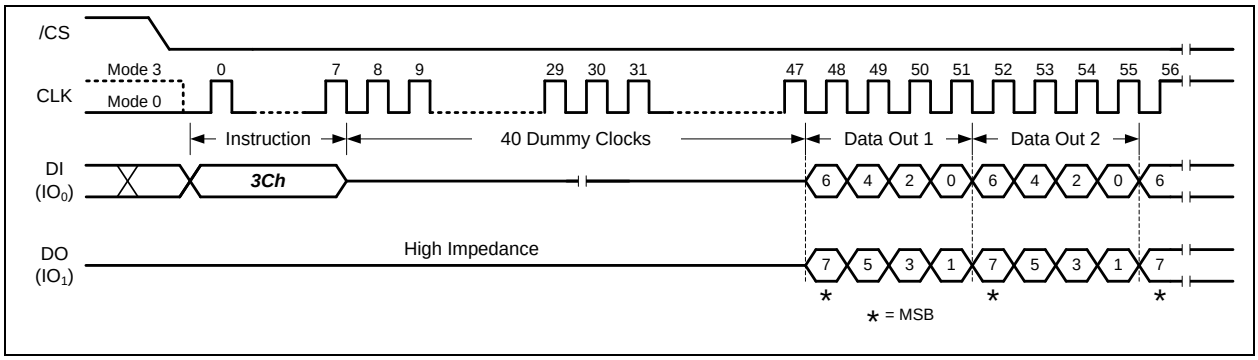



Figure 8-28 Fast Read Dual Output with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)



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### 8.2.23 Fast Read Quad Output (6Bh)

The Fast Read Quad Output instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, $IO_0$, $IO_1$, $IO_2$, and $IO_3$. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

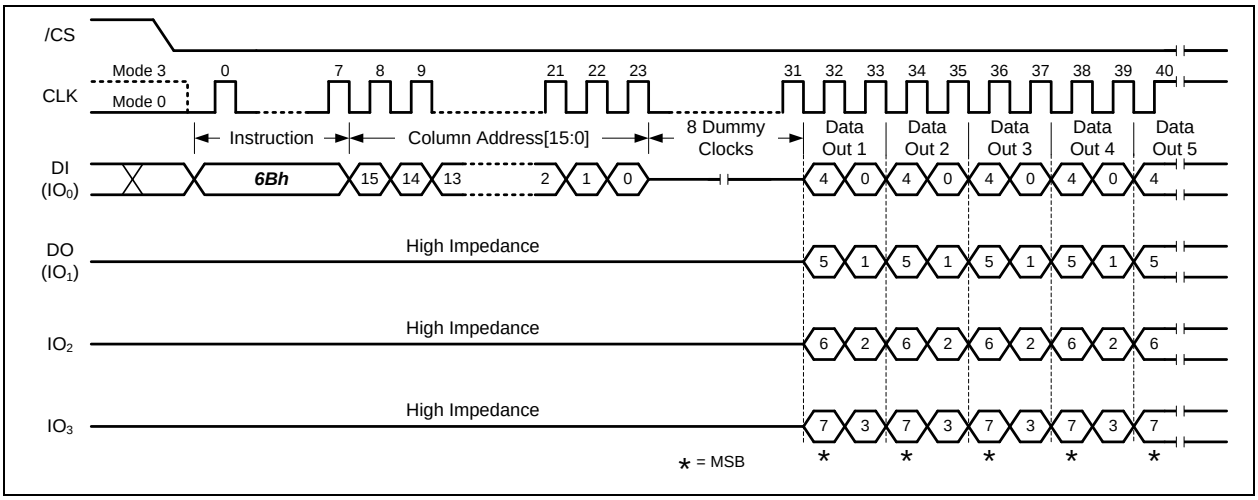



Figure 8-29 Fast Read Quad Output Instruction (Buffer Read Mode, BUF=1)

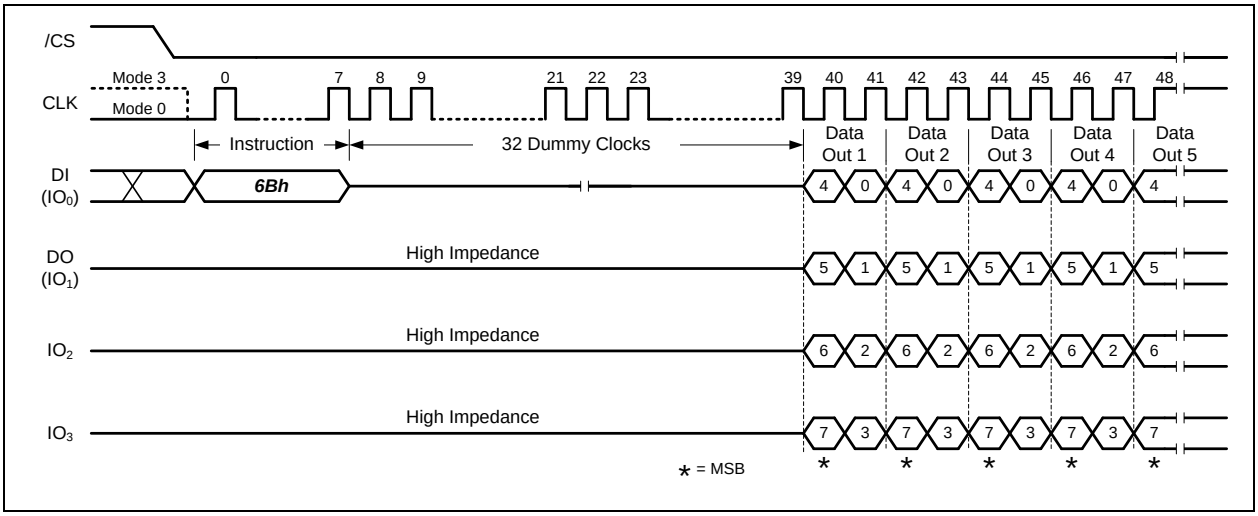



Figure 8-30 Fast Read Quad Output Instruction (Continuous Read Mode, BUF=0)



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### 8.2.24 Fast Read Quad Output with 4-Byte Address (6Ch)

The Fast Read Quad Output instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, $IO_0$, $IO_1$, $IO_2$, and $IO_3$. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

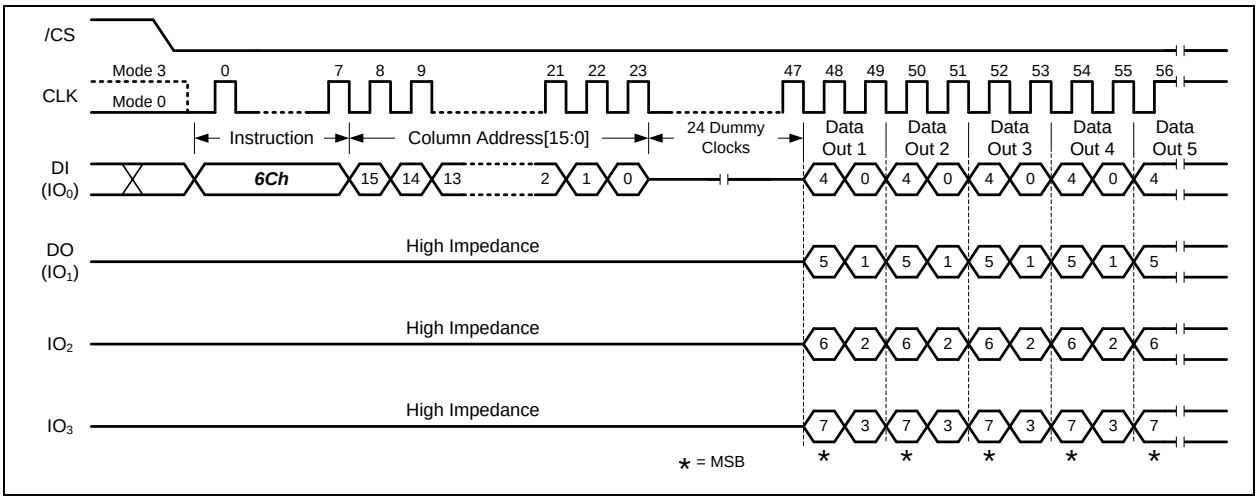



Figure 8-31 Fast Read Quad Output with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

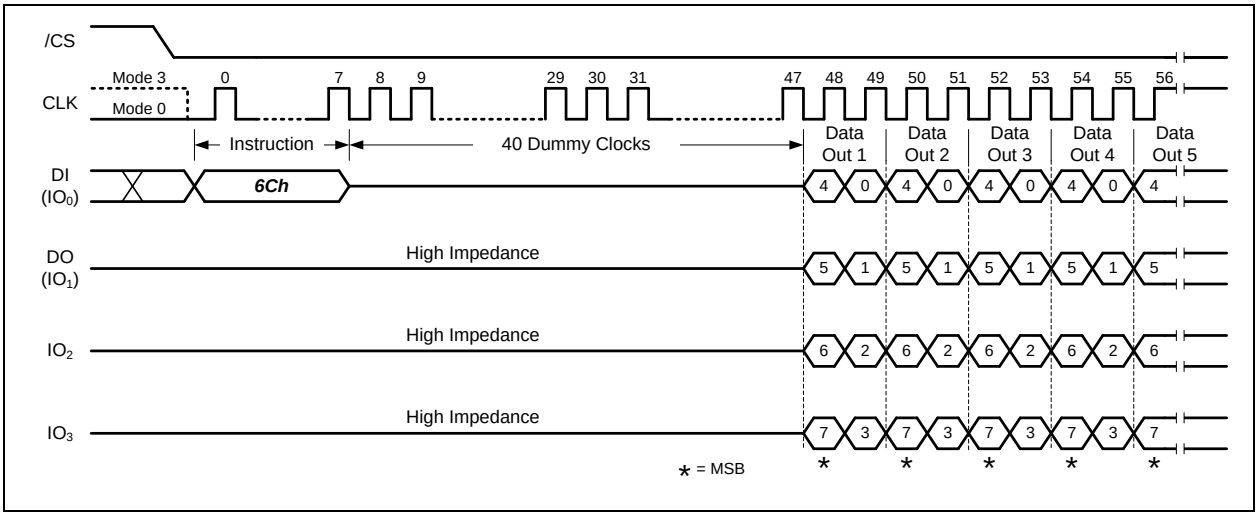



Figure 8-32 Fast Read Quad Output with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)



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### 8.2.25 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, $IO_0$ and $IO_1$. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

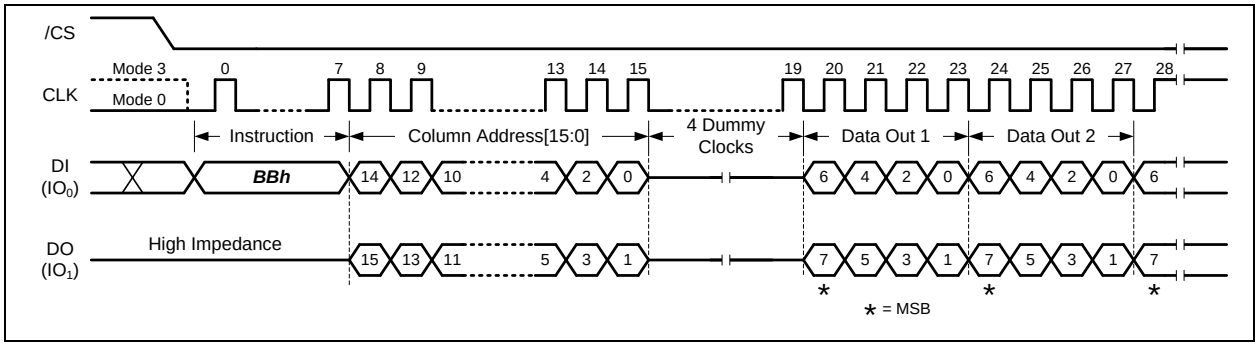



Figure 8-33 Fast Read Dual I/O Instruction (Buffer Read Mode, BUF=1)

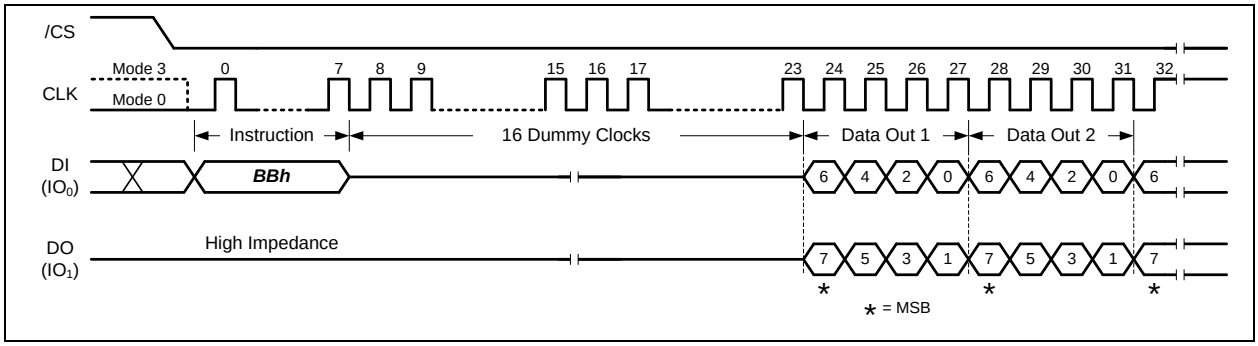



Figure 8-34 Fast Read Dual I/O Instruction (Continuous Read Mode, BUF=0)



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### 8.2.26 Fast Read Dual I/O with 4-Byte Address (BCh)

The Fast Read Dual I/O instruction allows for improved random access while maintaining two IO pins, $IO_0$ and $IO_1$. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

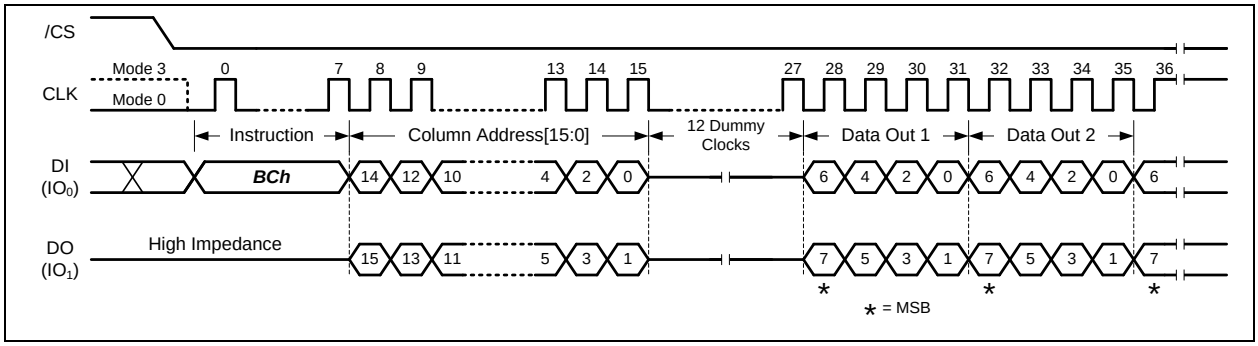



Figure 8-35 Fast Read Dual I/O with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

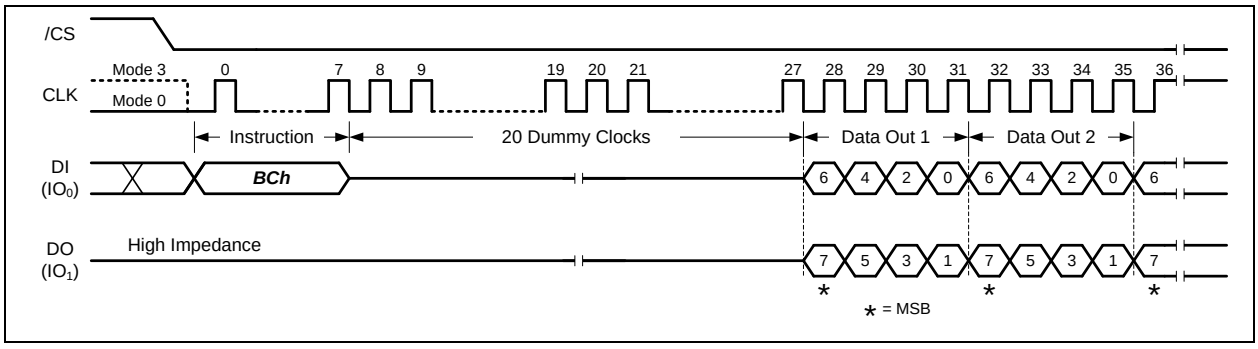



Figure 8-36 Fast Read Dual I/O with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)



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### 8.2.27 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins $IO_0$, $IO_1$, $IO_2$ and $IO_3$ prior to the data output. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad I/O Instruction. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

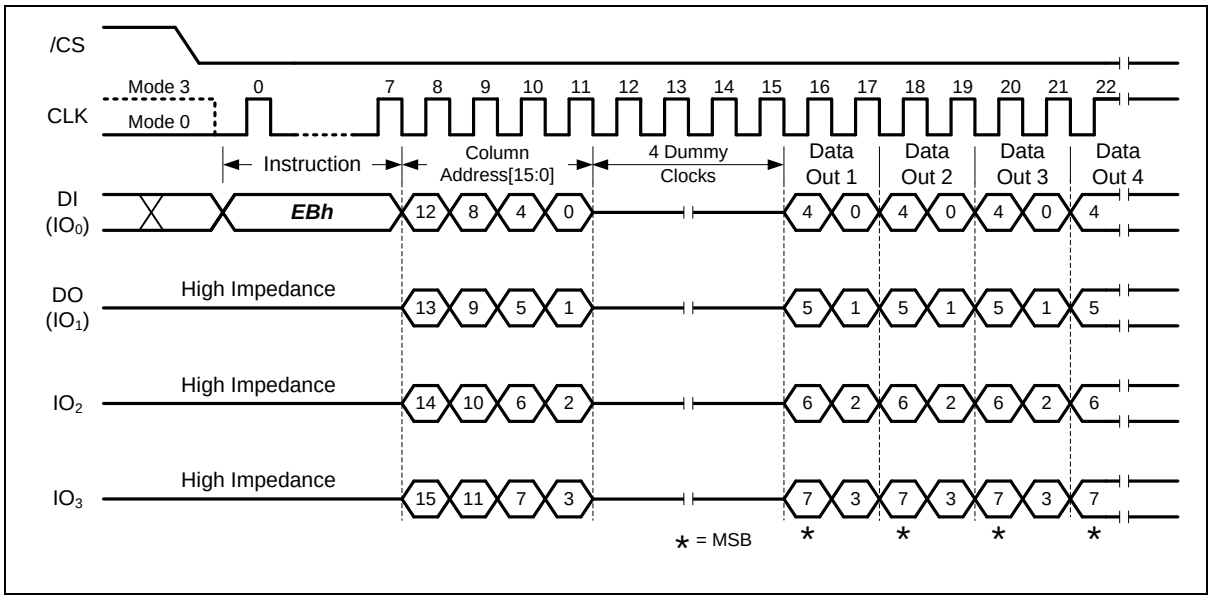



Figure 8-37 Fast Read Quad I/O Instruction (Buffer Read Mode, BUF=1)



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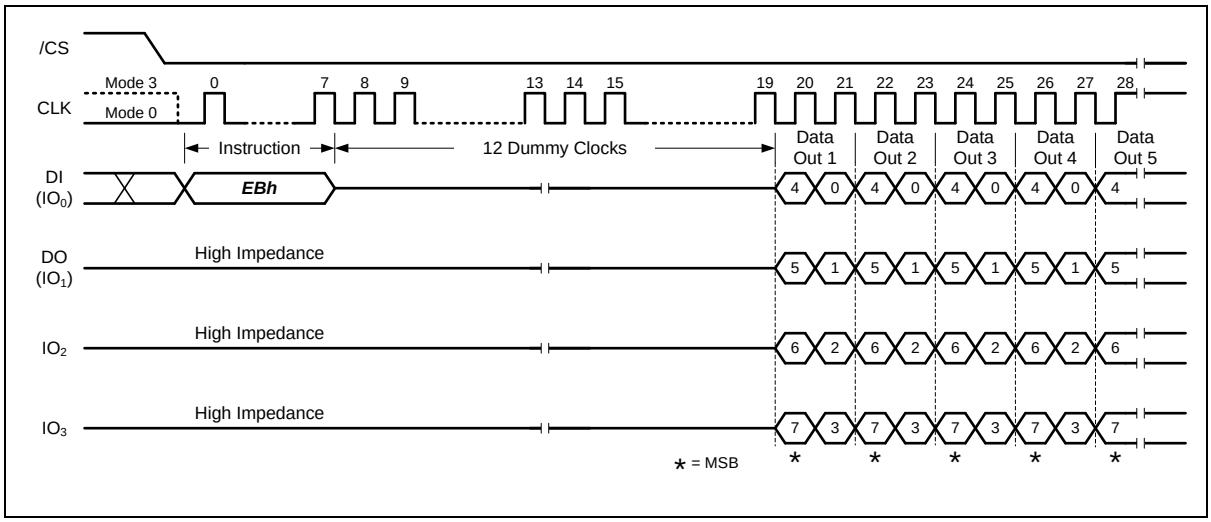



Figure 8-38 Fast Read Quad I/O Instruction (Continuous Read Mode, BUF=0)



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### 8.2.28 Fast Read Quad I/O with 4-Byte Address (ECh)

The Fast Read Quad I/O instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins $IO_0$, $IO_1$, $IO_2$ and $IO_3$ prior to the data output. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad I/O Instruction. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

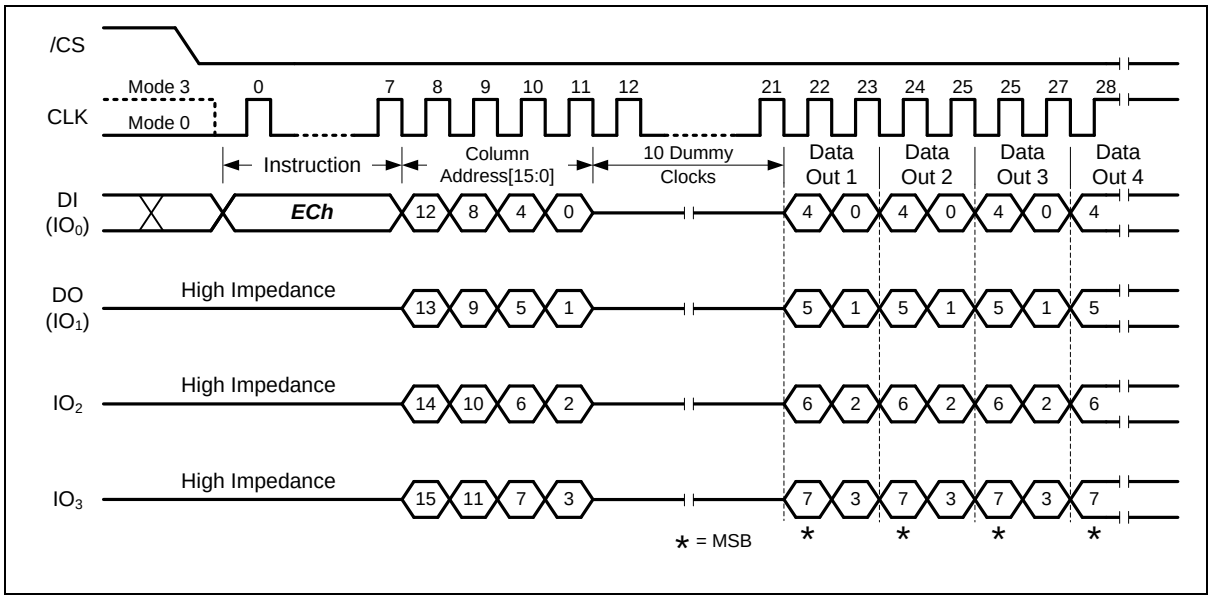



Figure 8-39 Fast Read Quad I/O with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)



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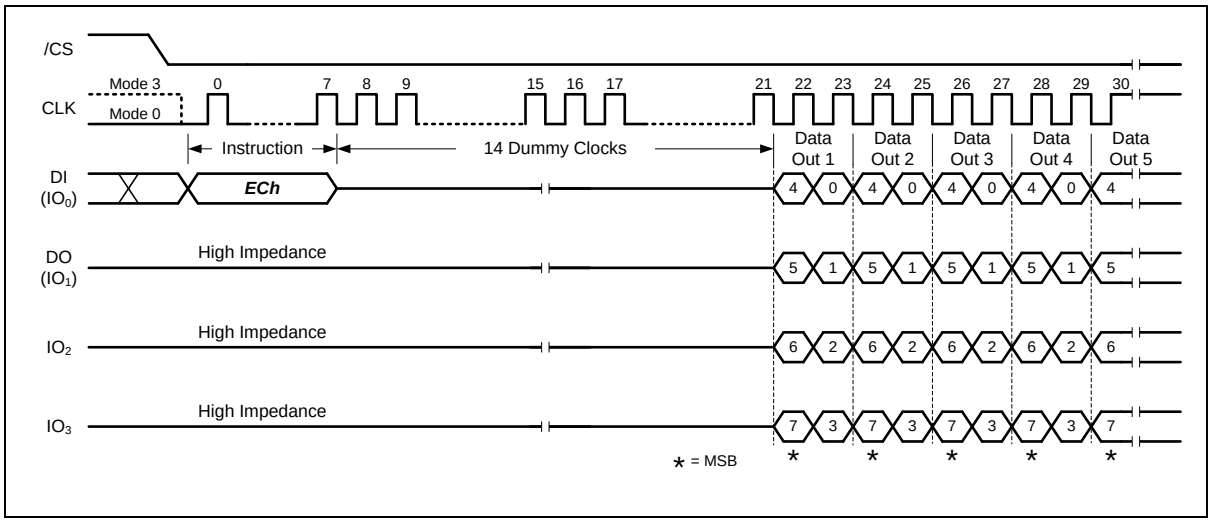



Figure 8-40 Fast Read Quad I/O with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)



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### 8.2.29 DTR Fast Read (0Dh)

The DTR Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The DTR Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Dh” followed by the 16-bits Column Address and 8-bits dummy clocks or 16-bits dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the both edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond’s SpiFlash NOR flash memory command sequence.

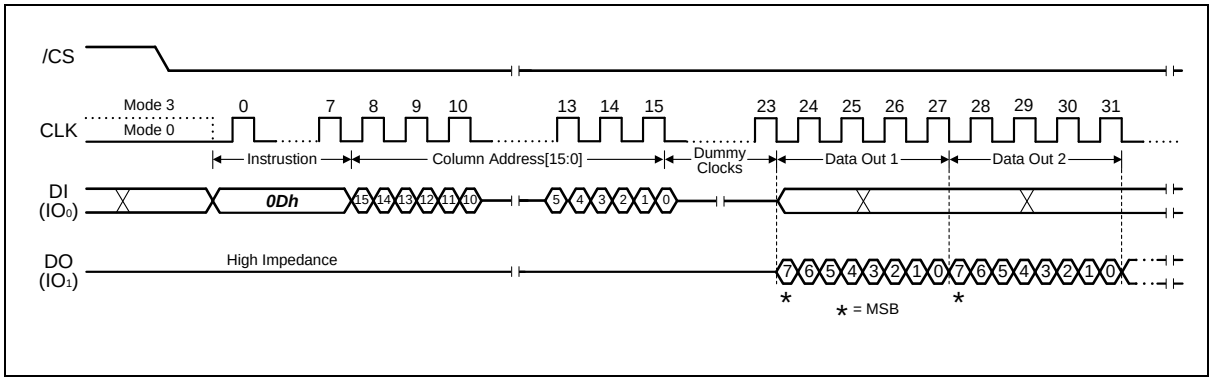



Figure 8-41 DTR Fast Read Instruction (Buffer Read Mode, BUF=1)

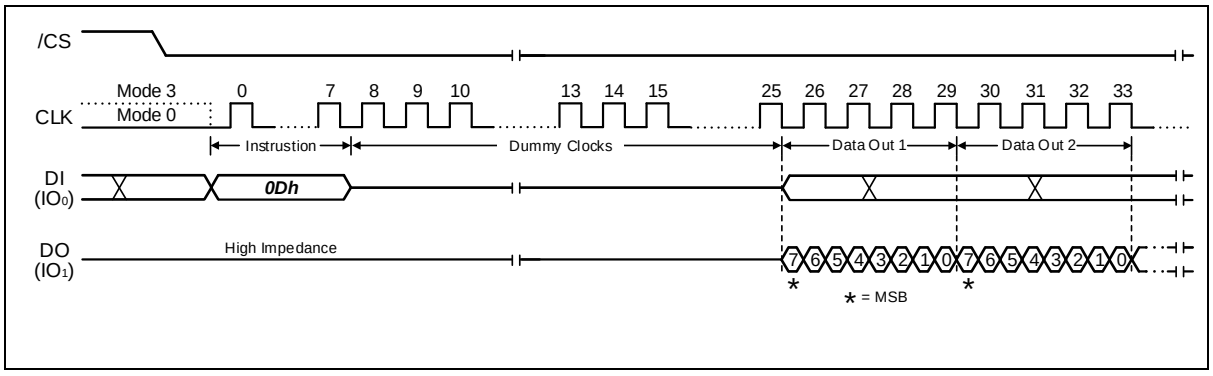



Figure 8-42 DTR Fast Read Instruction (Continuous Read Mode, BUF=0)



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### 8.2.30 DTR Fast Read with 4-Byte Address (0Eh)

The DTR Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The DTR Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Eh” followed by the 16-bits Column Address and 24-bits dummy clocks or 40-bits dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the both edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond’s SpiFlash NOR flash memory command sequence.

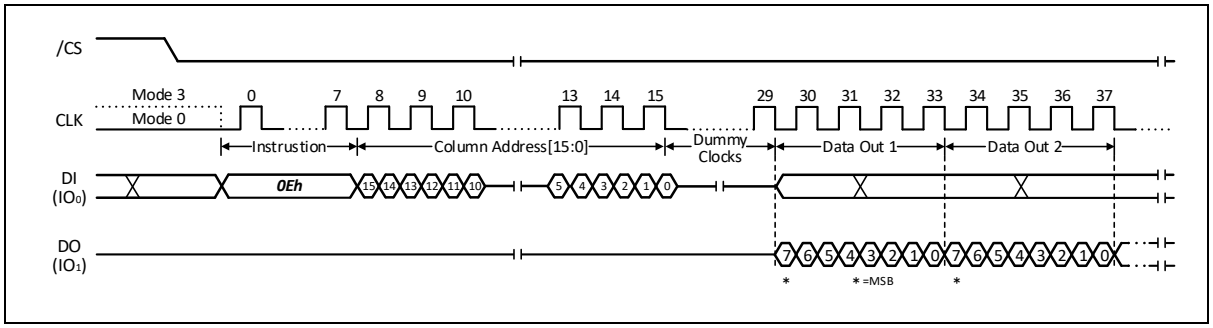



Figure 8-43 DTR Fast Read with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

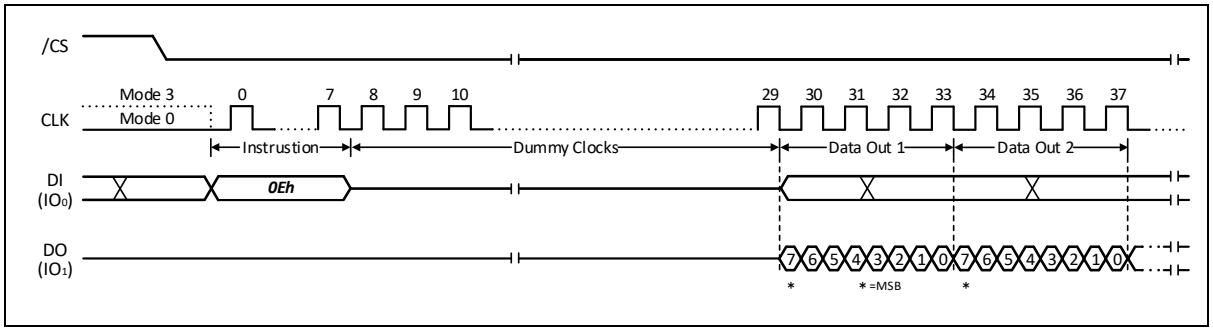



Figure 8-44 DTR Fast Read with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)



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### 8.2.31 DTR Fast Read Dual Output (3Dh)

The DTR Fast Read Dual Output instruction is similar to the DTR Fast Read (0Dh) instruction except that data is output on two pins; $IO_0$ and $IO_1$. This allows data to be transferred at twice the rate of the DTR Fast Read (0Dh) instruction.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

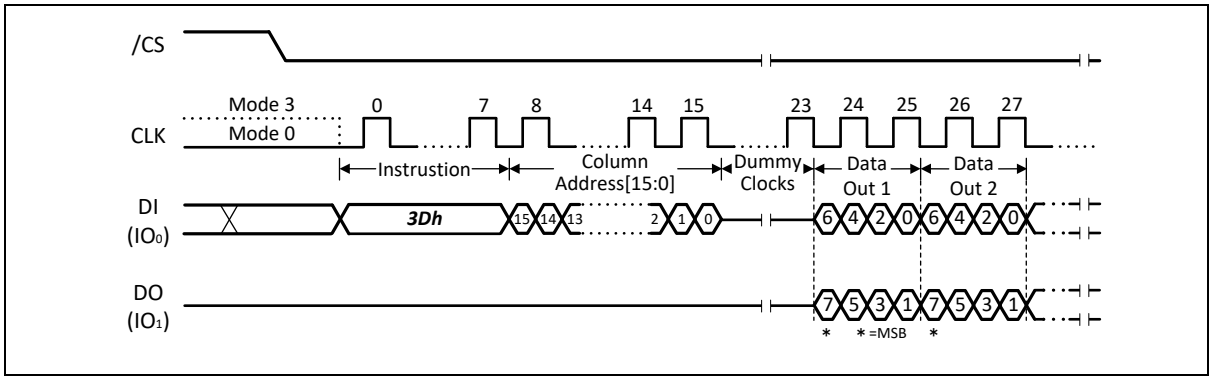



Figure 8-45 DTR Fast Read Dual Output Instruction (Buffer Read Mode, BUF=1)

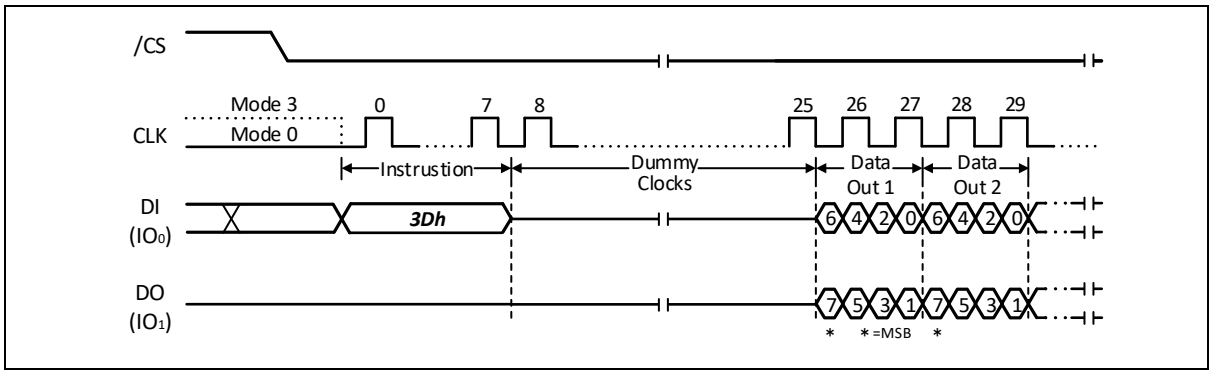



Figure 8-46 DTR Fast Read Dual Output Instruction (Continuous Read Mode, BUF=0)



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### 8.2.32 DTR Fast Read Quad Output (6Dh)

The DTR Fast Read Quad Output instruction is similar to the DTR Fast Read Dual Output (3Dh) instruction except that data is output on four pins, $IO_0$, $IO_1$, $IO_2$, and $IO_3$. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the DTR Fast Read Quad Output Instruction. The DTR Fast Read Quad Output Instruction allows data to be transferred at four times the rate of the DTR Fast Read (0Dh) instruction.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

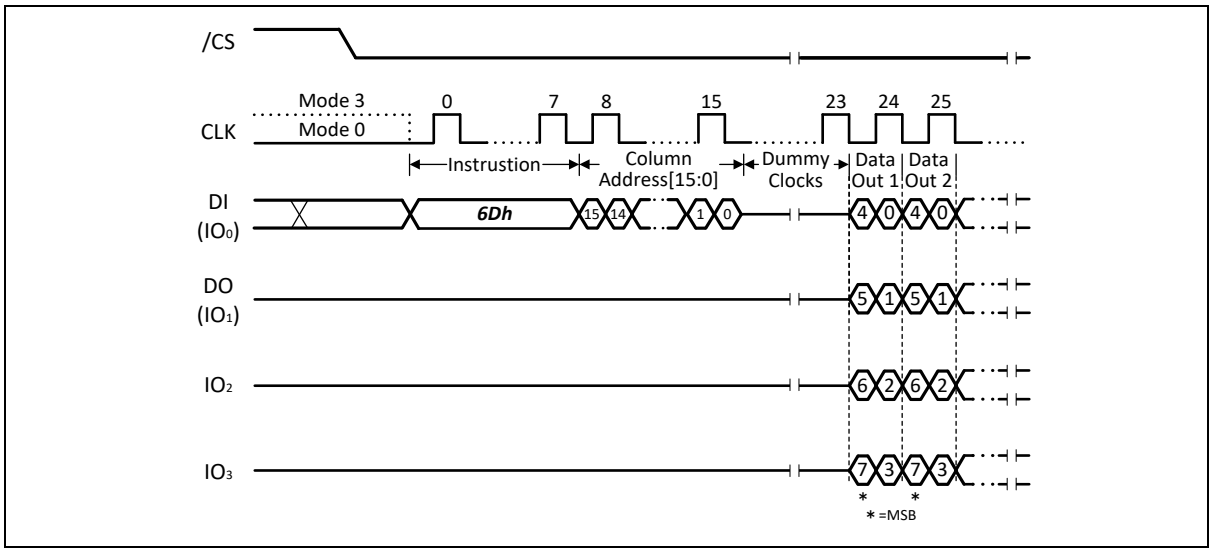



Figure 8-47 DTR Fast Read Quad Output Instruction (Buffer Read Mode, BUF=1)



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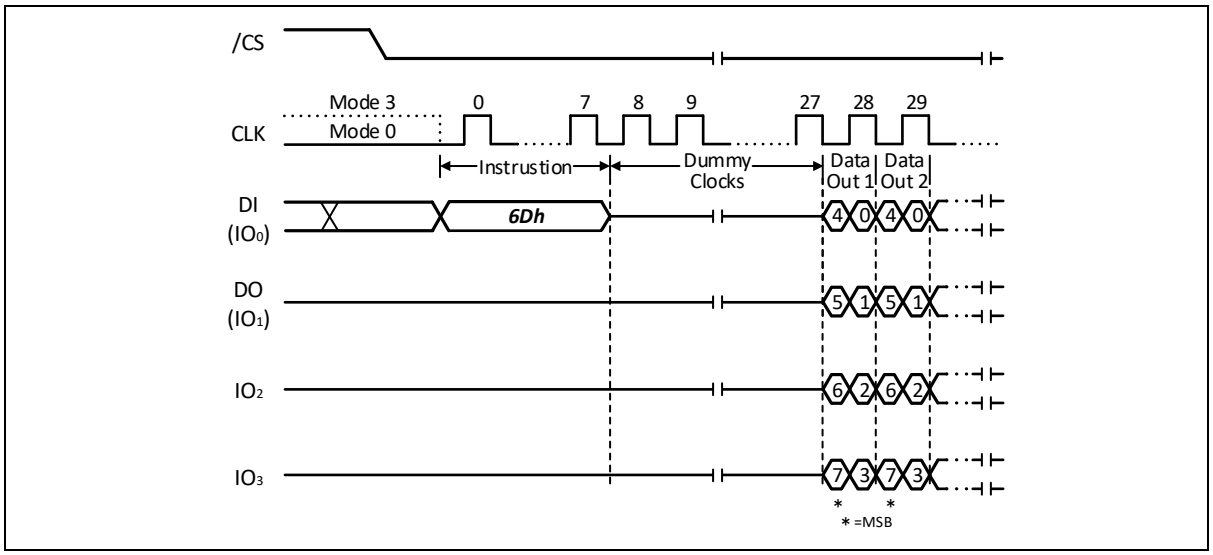



Figure 8-48 DTR Fast Read Quad Output Instruction (Continuous Read Mode, BUF=0)



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### 8.2.33 DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/O (BDh) instruction allows for improved random access while maintaining two IO pins, $IO_0$ and $IO_1$. It is similar to the DTR Fast Read Dual Output (3Dh) instruction but with the capability to input the Column Address or the dummy clocks four bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

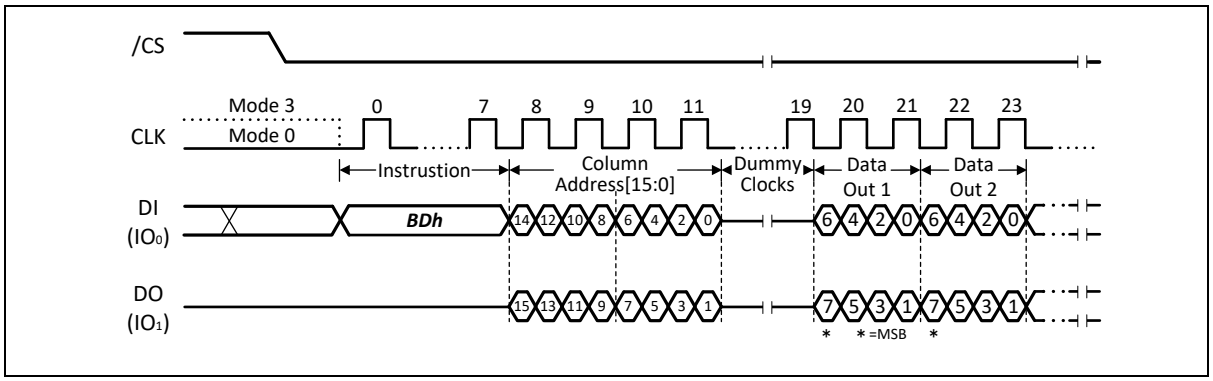



Figure 8-49 DTR Fast Read Dual I/O Instruction (Buffer Read Mode, BUF=1)

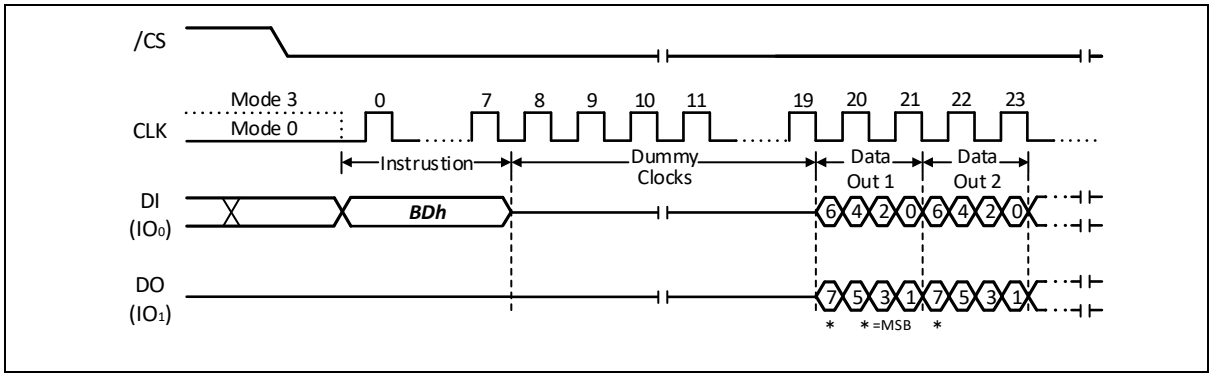



Figure 8-50 DTR Fast Read Dual I/O Instruction (Continuous Read Mode, BUF=0)



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### 8.2.34 DTR Fast Read Dual I/O with 4-Byte Address (BEh)

The DTR Fast Read Dual I/O instruction allows for improved random access while maintaining two IO pins, $IO_0$ and $IO_1$. It is similar to the DTR Fast Read Dual Output (3Dh) instruction but with the capability to input the Column Address or the dummy clocks four bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

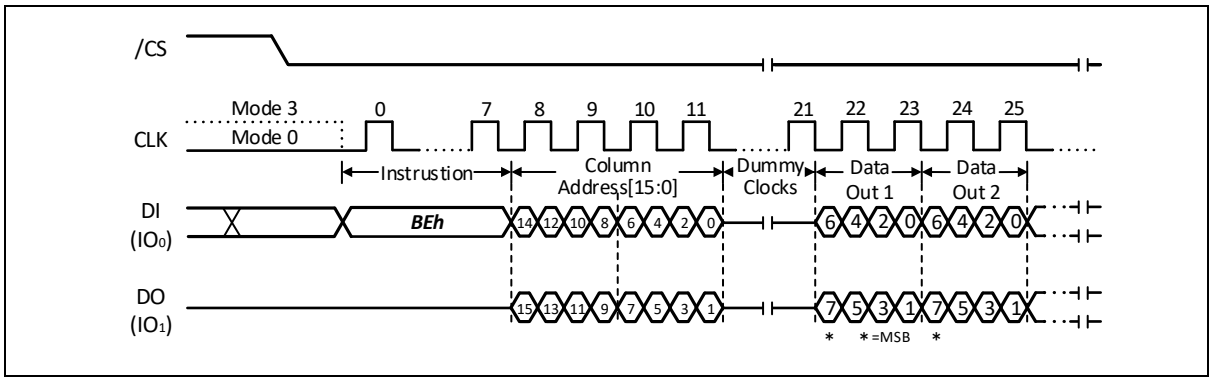



Figure 8-51 DTR Fast Read Dual I/O with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)

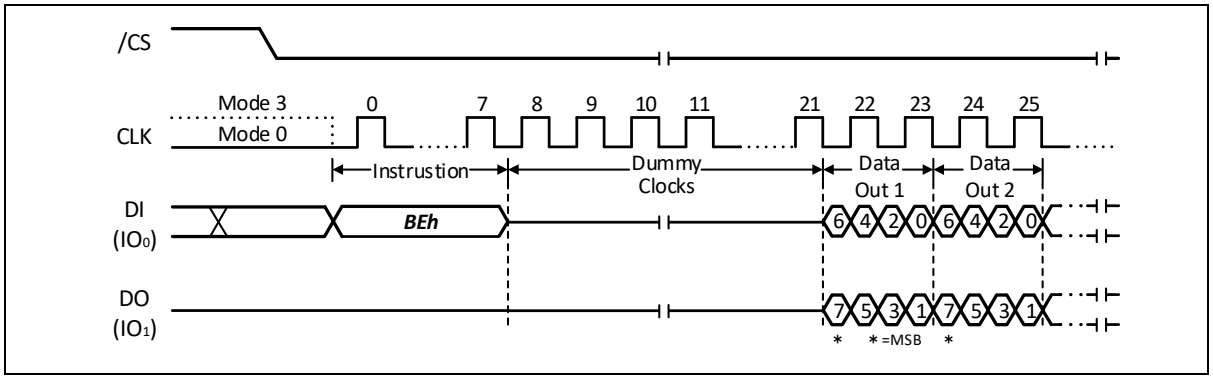



Figure 8-52 DTR Fast Read Dual I/O with 4-Byte Address Instruction (Continuous Read Mode, BUF=0)



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### 8.2.35 DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O instruction is similar to the DTR Fast Read Dual I/O (BDh) instruction except that address and data bits are input and output through four pins $IO_0$, $IO_1$, $IO_2$ and $IO_3$ prior to the data output. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the DTR Fast Read Quad I/O Instruction. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

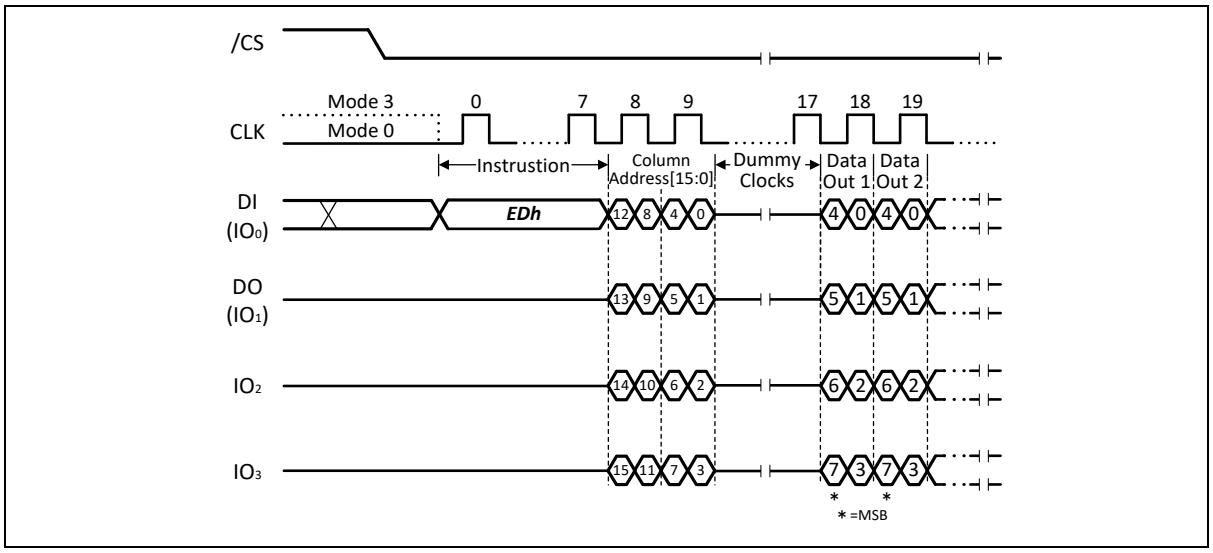



Figure 8-53 DTR Fast Read Quad I/O Instruction (Buffer Read Mode, BUF=1)

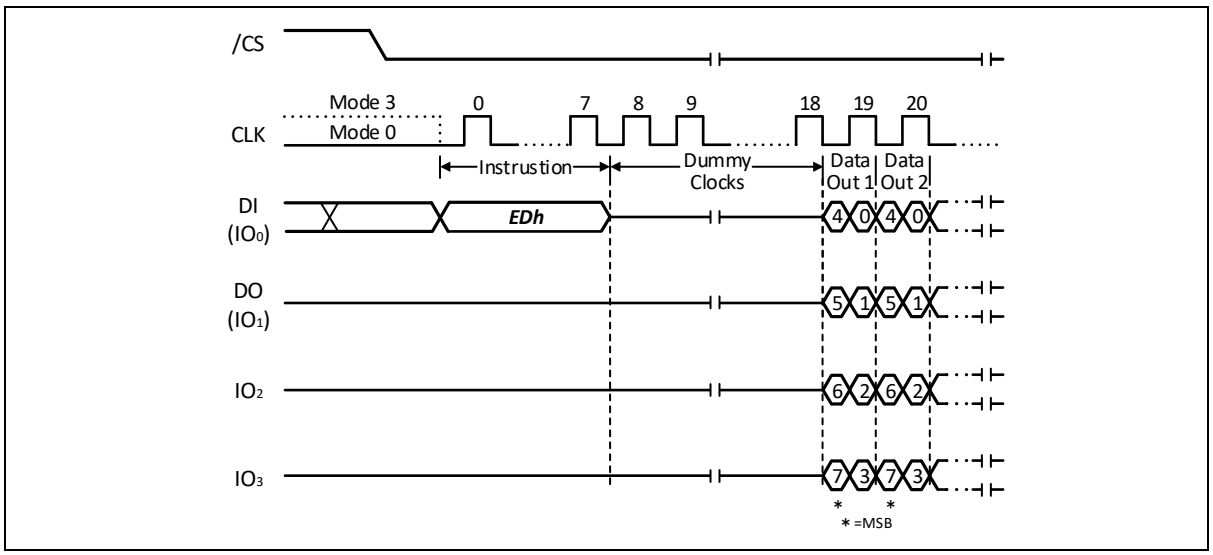



Figure 8-54 DTR Fast Read Quad I/O Instruction (Continuous Read Mode, BUF=0)



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### 8.2.36 DTR Fast Read Quad I/O with 4-Byte Address (EEh)

The DTR Fast Read Quad I/O instruction is similar to the DTR Fast Read Dual I/O (BDh) instruction except that address and data bits are input and output through four pins $IO_0$, $IO_1$, $IO_2$ and $IO_3$ prior to the data output. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the DTR Fast Read Quad I/O Instruction. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory command sequence.
When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

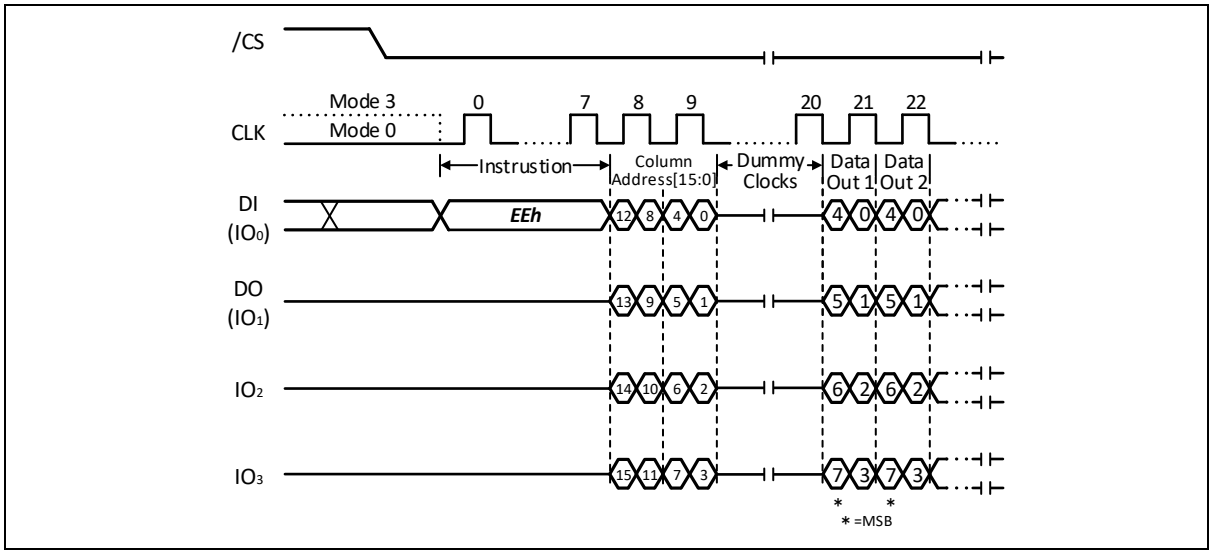



Figure 8-55 DTR Fast Read Quad I/O with 4-Byte Address Instruction (Buffer Read Mode, BUF=1)



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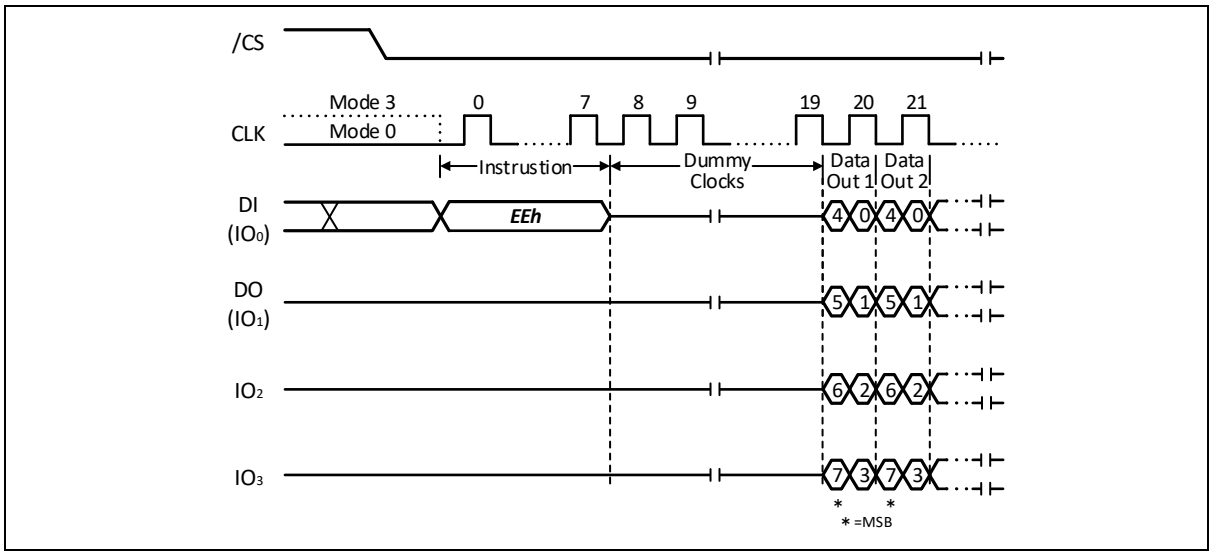



Figure 8-56 DTR Fast Read Quad I/O Instruction (Continuous Read Mode, BUF=0)



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### 8.2.37 Accessing Unique ID / Parameter / OTP Pages (OTP-E=1)

In addition to the main memory array, the W25N01JW is also equipped with one Unique ID Page, one Parameter Page, and ten OTP Pages.

| Page Address | Page Name | Descriptions | Data Length |
|---|---|---|---|
| 00h | Unique ID Page | Factory programmed, Read Only | 32-Byte x 16 |
| 01h | Parameter Page | Factory programmed, Read Only | 256-Byte x 3 |
| 02h | OTP Page [0] | Program Only, OTP lockable | 2,112-Byte |
| … | OTP Pages [1:8] | Program Only, OTP lockable | 2,112-Byte |
| 0Bh | OTP Page [9] | Program Only, OTP lockable | 2,112-Byte |

To access these additional data pages, the OTP-E bit in Status Register-2 must be set to "1" first. Then, Read operations can be performed on Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it's not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

**Read Operations**

A "Page Data Read" command must be issued followed by a specific page address shown in the table above to load the page data into the main Data Buffer. After the device finishes the data loading (BUSY=0), all Read commands may be used to read the Data Buffer starting from any specified Column Address. Please note all Read commands must now follow the "Buffer Read Mode" command structure (CA[15:0], number of dummy clocks) regardless the previous BUF bit setting. ECC can also be enabled for the OTP page read operations to ensure the data integrity.

**Program and OTP Lock Operations**

OTP pages provide the additional space (2K-Byte x 10) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state set in the factory, and can only be programmed (change data from "1" to "0") until being locked by OTP-L bit in the Configuration/Status Register-2. OTP-E must be first set to "1" to enable the access to these OTP pages, then the program data must be loaded into the main Data Buffer using any "Program Data Load" commands. The "Program Execute" command followed by a specific OTP Page Address is used to initiate the data transfer from the Data Buffer to the OTP page. When ECC is enabled, ECC calculation will be performed during "Program Execute", and the ECC information will be stored into the 64-Byte spare area.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible. While still in the "OTP Access Mode" (OTP-E=1), user needs to set OTP-L bit in the Configuration/Status Register-2 to "1", and issue a "Program Execute" command (Page Address is "don't care"). After the device finishes the OTP lock setting (BUSY=0), the user can set OTP-E to "0" to return to the main memory array operation.

**SR1-L OTP Lock Operation**

The Protection/Status Register-1 contains protection bits that can be set to protect either a portion or the entire memory array from being Programmed/Erased or set the device to either Software Write Protection (WP-E=0) or Hardware Write Protection (WP-E=1). Once the BP[3:0], TB, WP-E bits are set correctly, SRP1 and SRP0 should also be set to "1"s as well to allow SR1-L bit being set to "1" to permanently lock the protection settings in the Status Register-1 (SR1). Similar to the OTP-L setting procedure above, in order to set SR1-L lock bit, the device must enter the "OTP Access Mode" (OTP-E=1) first, and SR1-L bit should be set to "1" prior to the "Program Execute" command (Page Address is "don't care"). Once SR1-L is set to "1" (BUSY=0), the user can set OTP-E to "0" to return to the main memory array operation.



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### 8.2.38 Parameter Page Data Definitions

The Parameter Page contains 3 identical copies of the 256-Byte Parameter Data. The table below lists all the key data byte locations. All other unspecified byte locations have 00h data as default.

| Byte Number | Descriptions | Values |
|---|---|---|
| 0~3 | Parameter page signature | 4Fh, 4Eh, 46h, 49h |
| 4~5 | Revision number | 00h, 00h |
| 6~7 | Feature supported | 00h, 00h |
| 8~9 | Optional command supported | 00h, 00h |
| 10~31 | Reserved | All 00h |
| 32~43 | Device manufacturer | 57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h |
| 44~63 | Device model | 57h, 32h, 35h, 4Eh, 30h, 31h, 4Ah, 57h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h |
| 64 | JEDEC manufacturer ID | EFh |
| 65~66 | Date code | 00h, 00h |
| 67~79 | Reserved | All 00h |
| 80~83 | Number of data bytes per page | 00h, 08h, 00h, 00h |
| 84~85 | Number of spare bytes per page | 40h, 00h |
| 86~91 | Reserved | All 00h |
| 92~95 | Number of pages per block | 40h, 00h, 00h, 00h |
| 96~99 | Number of blocks per logical unit | 00h, 04h, 00h, 00h |
| 100 | Number of logical units | 01h |
| 101 | Number of address bytes | 00h |
| 102 | Number of bits per cell | 01h |
| 103~104 | Bad blocks maximum per unit | 14h, 00h |
| 105~106 | Block endurance | 01h, 05h |
| 107 | Guaranteed valid blocks at beginning of target | 01h |
| 108~109 | Block endurance for guaranteed valid blocks | 00h, 00h |
| 110 | Number of programs per page | 04h |
| 111 | Reserved | 00h |
| 112 | Number of ECC bits | 00h |
| 113 | Number of plane address bits | 00h |
| 114 | Multi-plane operation attributes | 00h |
| 115~127 | Reserved | All 00h |
| 128 | I/O pin capacitance, maximum | 08h |
| 129~132 | Reserved | All 00h |
| 133~134 | Maximum page program time (us) | BCh, 02h |
| 135~136 | Maximum block erase time (us) | 10h, 27h |
| 137~138 | Maximum page read time (us) | 3Ch, 00h |
| 139~163 | Reserved | All 00h |
| 164~165 | Vendor specific revision number | 00h, 00h |
| 166~253 | Vendor specific | All 00h |
| 254~255 | Integrity CRC | 46h, 44h |
| 256~511 | Value of bytes 0~255 | |
| 512~767 | Value of bytes 0~255 | |
| 768~2111 | Reserved | |



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# 9. ELECTRICAL CHARACTERISTICS

## 9.1 Absolute Maximum Ratings (1)

| PARAMETERS | SYMBOL | CONDITIONS | RANGE | UNIT |
|---|---|---|---|---|
| Supply Voltage | VCC | | –0.6 to +2.5 | V |
| Voltage Applied to Any Pin | VIO | Relative to Ground | –0.6 to VCC+0.4 | V |
| Transient Voltage on any Pin | VIOT | <20nS Transient Relative to Ground | –2.0 to VCC+2.0 | V |
| Storage Temperature | TSTG | | –65 to +150 | °C |
| Lead Temperature | TLEAD | | See Note (2) | °C |
| Electrostatic Discharge Voltage | VESD | Human Body Model(3) | –2000 to +2000 | V |

**Notes:**

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Standard JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

## 9.2 Operating Ranges

| PARAMETER | SYMBOL | CONDITIONS | SPEC | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| Supply Voltage | VCC | | 1.70 | 1.95 | V |
| Ambient Temperature, Operating | TA | Industrial | –40 | +85 | °C |
| | | Industrial Plus | | +105 | |



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## 9.3 Power-up Power-down Timing Requirements

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| VCC (min) to /CS low | $t_{VSL}$(1) | 200 | | µs |
| Time Delay Before Write Instruction | $t_{PUW}$(1) | 1 | | ms |
| Minimum duration for ensuring initialization will occur | $t_{PWD}$(1) | 1 | | ms |
| VCC voltage for ensuring initialization will occur | $V_{PWD}$(1) | | 0.7 | V |

**Notes:**

1. These parameters are characterized only.

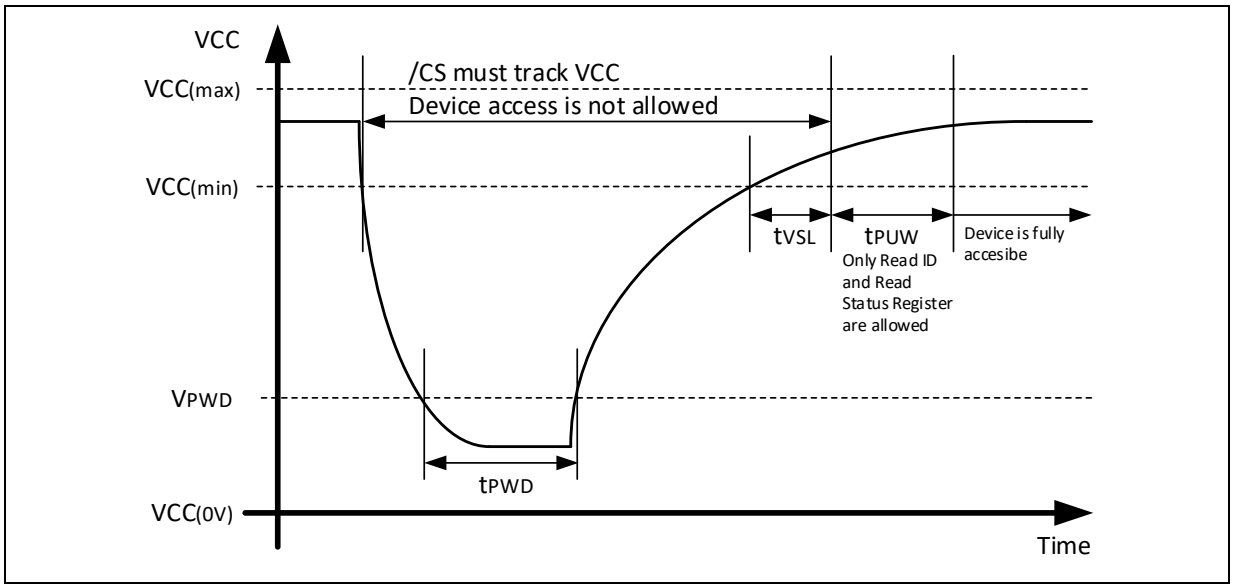



Figure 9-1 Power-up Power-down Timing and Voltage Levels

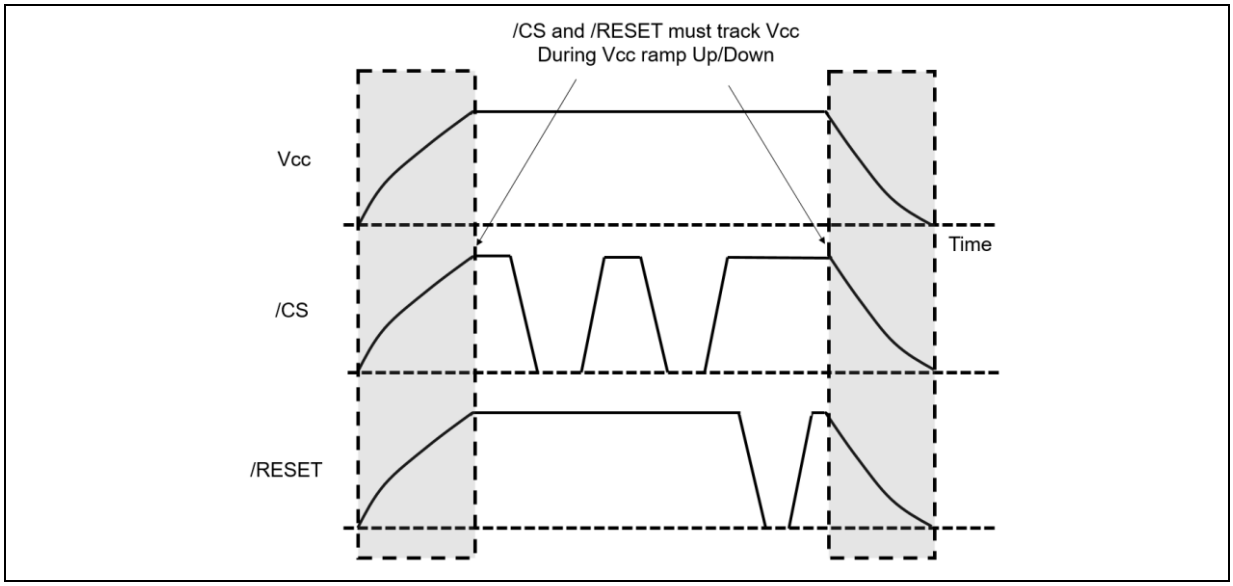



Figure 9-2 Power-up, Power-Down Requirement



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## 9.4 DC Electrical Characteristics

| PARAMETER | SYMBOL | CONDITIONS | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Input Capacitance | $C_{IN}$(1) | $V_{IN}$ = 0V(1) | | | 6 | pF |
| Output Capacitance | $C_{OUT}$(1) | $V_{OUT}$ = 0V(1) | | | 8 | pF |
| Input Leakage | $I_{LI}$ | | | | ±2 | µA |
| I/O Leakage | $I_{LO}$ | | | | ±2 | µA |
| Standby Current | $I_{CC1}$ | /CS = VCC, VIN = GND or VCC (<85°C) | | 10 | 150 | µA |
| | | /CS = VCC, VIN = GND or VCC (105°C) | | | 400 | |
| Deep Power-down Current | $I_{CC2}$ | /CS = VCC, VIN = GND or VCC (<85°C) | | 1 | 150 | µA |
| | | /CS = VCC, VIN = GND or VCC (105°C) | | | 400 | |
| Read Current (Fast Read) | $I_{CC3}$ | C = 0.1 VCC / 0.9 VCC at 166MHz STR, DO = Open | | 15 | 25 | mA |
| Read Current (Fast Read Dual I/O) | $I_{CC3}$ | C = 0.1 VCC / 0.9 VCC at 166MHz STR, DO = Open | | 20 | 30 | mA |
| Read Current (Fast Read Quad I/O) | $I_{CC3}$ | C = 0.1 VCC / 0.9 VCC at 166MHz STR or 80MHz DTR, DO = Open | | 25 | 35 | mA |
| Current Page Program | $I_{CC4}$ | /CS = VCC | | 25 | 35 | mA |
| Current Block Erase | $I_{CC5}$ | /CS = VCC | | 25 | 35 | mA |
| Input Low Voltage | $V_{IL}$ | | –0.3 | | VCC x 0.2 | V |
| Input High Voltage | $V_{IH}$ | | VCC x 0.8 | | VCC + 0.3 | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 100uA | | | 0.2 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = –100 µA | VCC-0.2 | | | V |

**Notes:**

1. The typical (TYP) value is tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V.



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## 9.5 AC Measurement Conditions

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Load Capacitance | $C_L$ | | 30 | pF |
| Input Rise and Fall Times | $T_R$, $T_F$ | | 1.5 | ns |
| Input Pulse Voltages | $V_{IN}$ | 0.1 VCC to 0.9 VCC | | V |
| Input Timing Reference Voltages | IN | 0.3 VCC to 0.7 VCC | | V |
| Output Timing Reference Voltages | OUT | 0.5 VCC | | V |

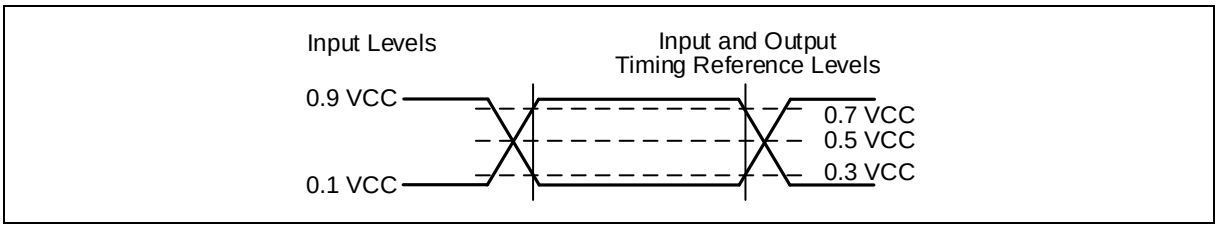



Figure 9-3 AC Measurement I/O Waveform



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## 9.6 AC Electrical Characteristics (3)

| DESCRIPTION | SYMBOL | ALT | DATA TRANSFER RATE | SPEC | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| Clock Frequency for all instruction except for:<br>1. BBh/BCh/EBh/ECh instructions (HS=0)<br>2. 03h instruction (HS=don't care)<br>3. DTR instructions (HS=don't care) | $F_R$ | $f_{C1}$ | STR only | D.C. | | 166 | MHz |
| Clock Frequency for BBh/BCh/EBh/ECh instructions with HS=1 | $F_R$ | $f_{C1}$ | STR only | D.C. | | 166 | MHz |
| Clock Frequency for BBh/BCh/EBh/ECh instructions with HS=0 | $F_R$ | $f_{C1}$ | STR only | D.C. | | 104 | MHz |
| Clock frequency for DTR instructions (HS=don't care) | $F_R$ | $f_{C1}$ | DTR only | D.C. | | 80 | MHz |
| Clock Frequency for 03h instruction (HS=don't care) | $f_R$ | | STR only | D.C. | | 54 | MHz |
| Clock High, Low Time for all instructions | $t_{CLH}$, $t_{CLL}$(1) | | STR | 0.45 × 1/ $F_R$ | | | ns |
| | | | DTR | | | | |
| Clock Rise Time peak to peak | $t_{CLCH}$(2) | | STR/DTR | 0.1 | | | V/ns |
| Clock Fall Time peak to peak | $t_{CHCL}$(2) | | STR/DTR | 0.1 | | | V/ns |
| /CS Active Setup Time relative to CLK | $t_{SLCH}$ | $t_{CSS}$ | STR/DTR | 5 | | | ns |
| /CS Not Active Hold Time relative to CLK | $t_{CHSL}$ | | STR/DTR | 5 | | | ns |
| Data In Setup Time | $t_{DVCH}$ | $t_{DSU}$ | STR/DTR | 2 | | | ns |
| | $t_{DVCL}$ | | DTR only | 2 | | | |
| Data In Hold Time | $t_{CHDX}$ | $t_{DH}$ | STR/DTR | 2 | | | ns |
| | $t_{CLDX}$ | | DTR only | 2 | | | |
| /CS Active Hold Time relative to CLK | $t_{CHSH}$ | | STR | 3 | | | ns |
| | | | DTR | 6 | | | |
| /CS Active Hold Time relative to CLK LOW | $t_{CLSH}$ | | DTR only | 3 | | | ns |
| /CS Not Active Setup Time relative to CLK | $t_{SHCH}$ | | STR | 3 | | | ns |
| | | | DTR | 6 | | | |
| /CS Deselect Time (for Array Read → Array Read) | $t_{SHSL1}$ | $t_{CSH}$ | STR/DTR | 10 | | | ns |
| /CS Deselect Time (for Erase, Program or Read Status Registers → Read Status Registers) | $t_{SHSL2}$ | $t_{CSH}$ | STR/DTR | 50 | | | ns |
| Output Disable Time | $t_{SHQZ}$(2) | $t_{DIS}$ | STR/DTR | | | 7 | ns |



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**AC Electrical Characteristics (cont'd)**

| DESCRIPTION | SYMBOL | ALT | DATA TRANSFER RATE | SPEC | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| Clock Low to Output Valid | $t_{CLQV}$ | $t_V$ | STR/DTR | | | 6 | ns |
| Clock High to Output Valid | $t_{CHQV}$ | | DTR only | | | 6 | ns |
| Output Hold Time | $t_{CLQX}$ | $t_{HO}$ | STR/DTR | 1 | | | ns |
| Output Hold Time | $t_{CHQX}$ | | DTR only | 1 | | | ns |
| /HOLD Active Setup Time relative to CLK | $t_{HLCH}$ | | STR | 2.7 | | | ns |
| /HOLD Active Hold Time relative to CLK | $t_{CHHH}$ | | STR | 2.7 | | | ns |
| /HOLD Not Active Setup Time relative to CLK | $t_{HHCH}$ | | STR | 2.7 | | | ns |
| /HOLD Not Active Hold Time relative to CLK | $t_{CHHL}$ | | STR | 2.7 | | | ns |
| /HOLD to Output Low-Z | $t_{HHQX}$(2) | $t_{LZ}$ | STR | | | 7 | ns |
| /HOLD to Output High-Z | $t_{HLQZ}$(2) | $t_{HZ}$ | STR | | | 12 | ns |
| Write Protect Setup Time Before /CS Low | $t_{WHSL}$ | | STR/DTR | 20 | | | ns |
| Write Protect Hold Time After /CS High | $t_{SHWL}$ | | STR/DTR | 100 | | | ns |
| Status Register Write Time | $t_W$ | | STR/DTR | | | 50 | ns |
| Clock High to Deep Power-down | $t_{DP}$ | | STR/DTR | | | 10 | µs |
| Clock High to Release Deep Power-down | $t_{RES1}$ | | STR/DTR | | | 80 | µs |
| /CS High to next Instruction after Reset during Page Data Read / Program Execute / Block Erase | $t_{RST}$(2) (3) | | STR/DTR | | | 5/10/ 500 | µs |
| /RESET pin Low period to reset the device | tRESET(2) | | STR/DTR | 1 | | | us |
| Read Page Data Time (ECC disabled) | $t_{RD1}$ | | STR/DTR | | | 25 | µs |
| Read Page Data Time (ECC enabled) | $t_{RD2}$ | | STR/DTR | | | 60 | µs |
| Continuous Read Stop to Device Ready Time | $t_{RD3}$ | | STR/DTR | | | 5 | µs |
| Page Program, OTP Lock, BBM Management Time | $t_{PP}$ | | STR/DTR | | 250 | 700 | us |
| Block Erase Time | $t_{BE}$ | | STR/DTR | | 2 | 10 | ms |
| Number of partial page programs | NoP | | STR/DTR | | | 4 | times |

**Notes:**

1. Clock high + Clock low must be less than or equal to 1/fC.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. The product which re-loads page0 data after Reset takes tRST + tRD busy time.
4. The typical (TYP) value is tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V.
5. AC electrical characteristics is based on default setting of ODS.



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## 9.7 Serial Output Timing

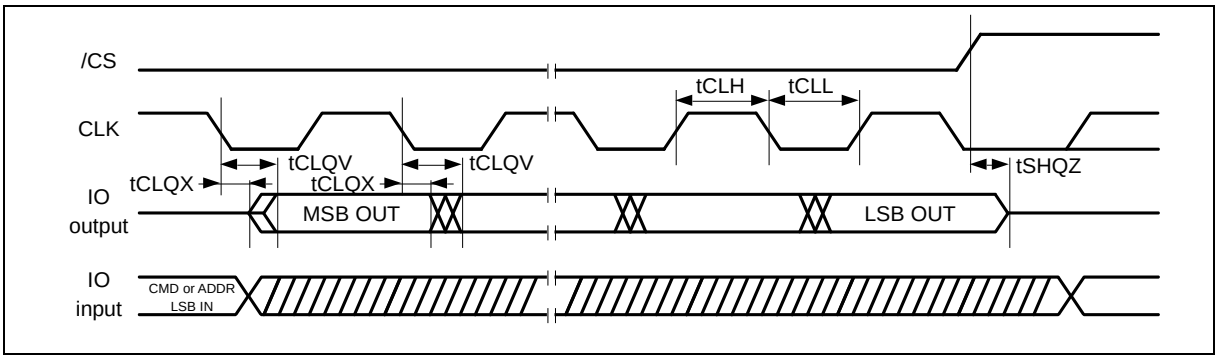



Figure 9-4 Serial Output Timing (STR)

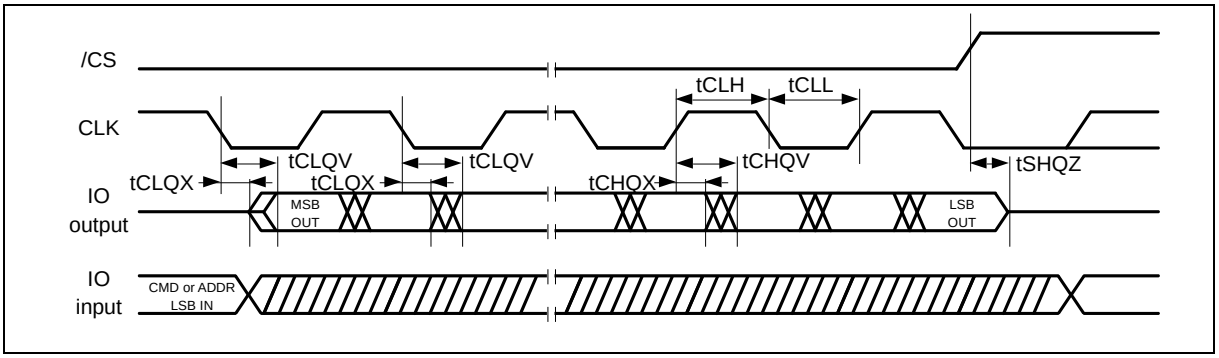



Figure 9-5 Serial Output Timing (DTR)

## 9.8 Serial Input Timing

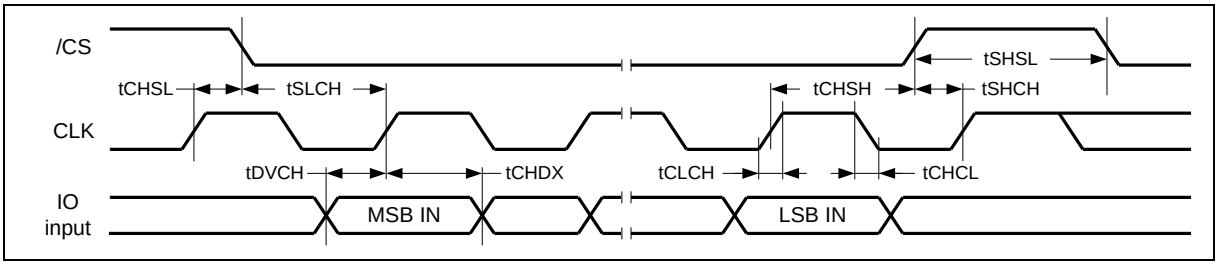



Figure 9-6 Serial Input Timing (STR)

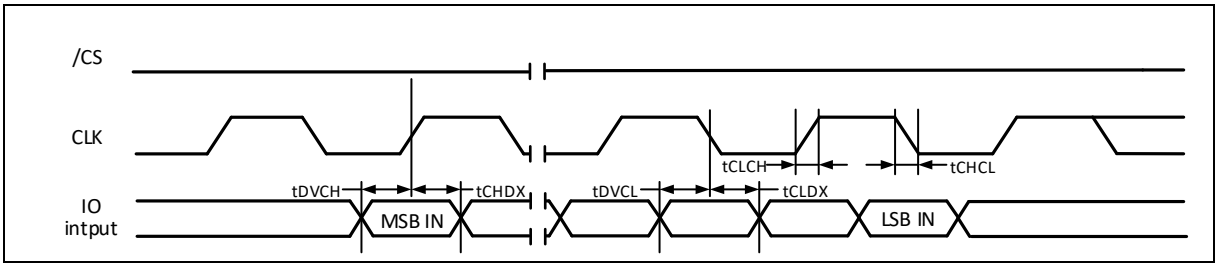



Figure 9-7 Serial Input Timing (DTR)



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## 9.9 /HOLD Timing

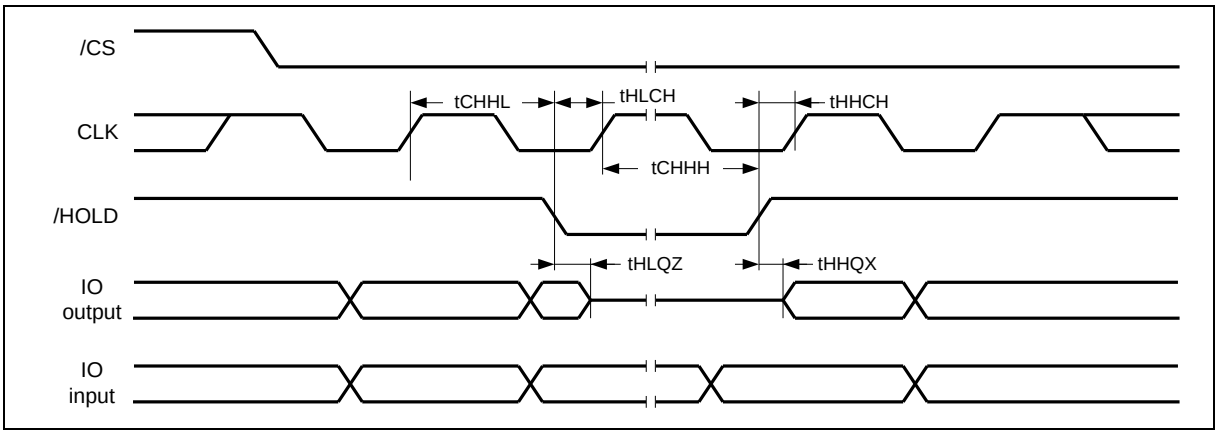



Figure 9-8 /HOLD Timing

## 9.10 /WP Timing

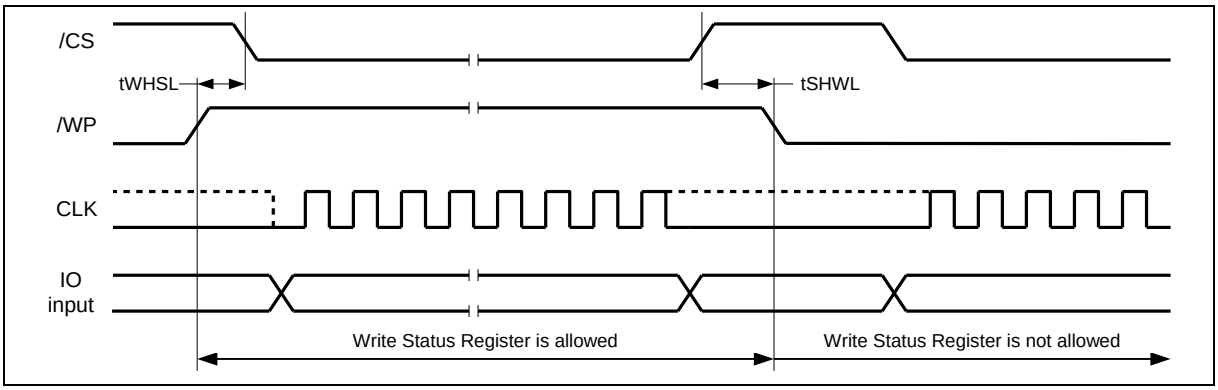



Figure 9-9 /WP Timing



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# 10. INVALID BLOCK MANAGEMENT

## 10.1 Invalid Blocks

The W25N01JW may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks. An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Valid block number | Nvb | 1004 | 1024 | blocks |

## 10.2 Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The W25N01JW has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are permanently marked. The mark information cannot be erased. All initial invalid blocks are marked with non-FFh at the 1st byte of main array and the 1st two bytes of spare area on the 1st page. It should be checked for invalid blocks by reading the marked locations, and create a table of initial invalid blocks as following flow chart.

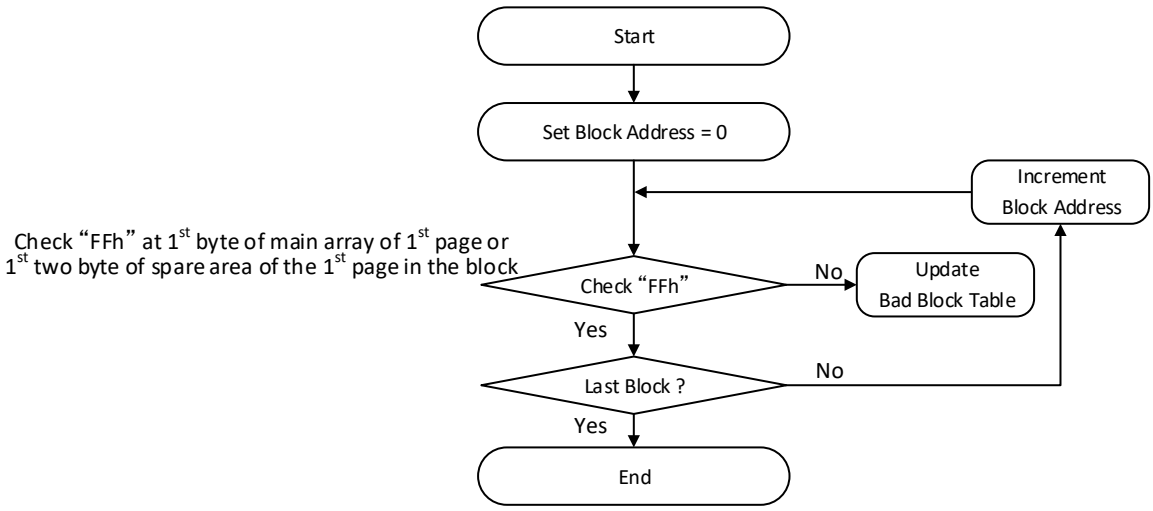



Figure 10-1 Flow Chart of Create Initial Invalid Block Table



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## 10.3 Error in Operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each program and erase operation, check the P-FAIL and E-FAIL bit to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 1-bit ECC per 528 bytes of data to ensure data recovery.

| Operation | Detection and recommended procedure |
|---|---|
| Erase | Status read after erase → Block Replacement |
| Program | Status read after program → Block Replacement |
| Read | Verify ECC → ECC correction |

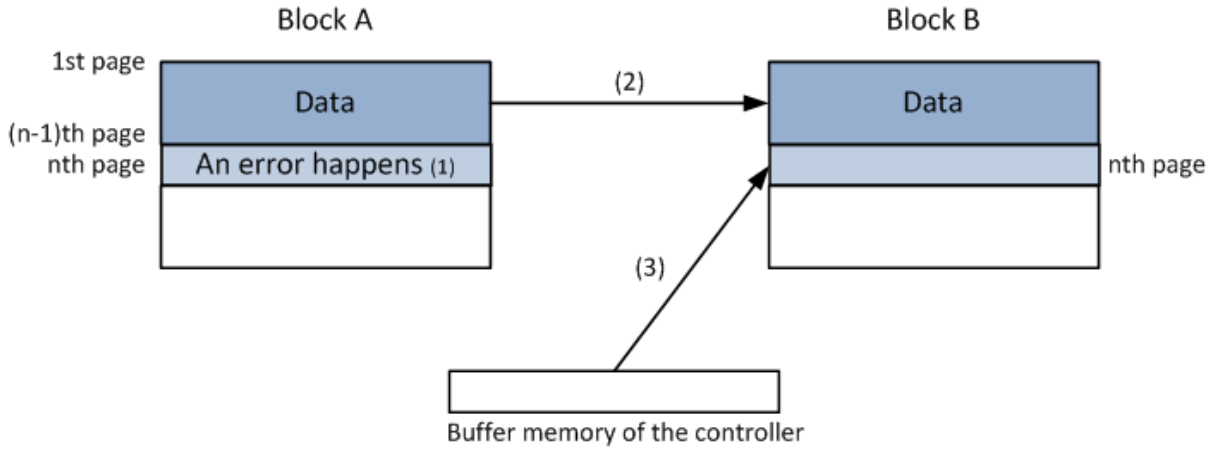



Figure 10-2 Bad Block Replacement

**Notes:**

1. An error happens in the nth page of block A during program or erase operation.
2. Copy the data in block A to the same location of block B which is valid block.
3. Copy the nth page data of block A in the buffer memory to the nth page of block B.
4. Creating or updating bad block table for preventing further program or erase to block A.

## 10.4 Addressing in Program Operation

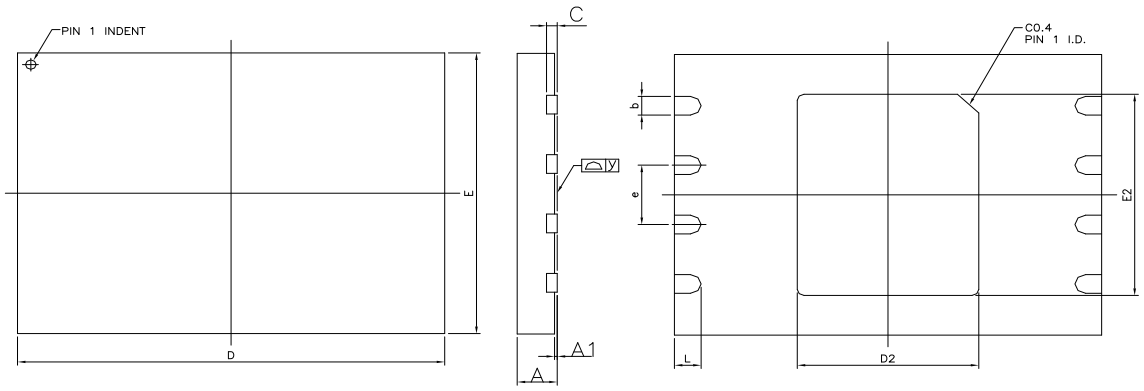
The pages within the block have to be programmed sequentially from LSB (least significant bit) page to the MSB (most significant bit) within the block. The LSB is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.



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# 11. PACKAGE SPECIFICATIONS

## 11.1 8-Pad WSON 8x6-mm (Package Code ZE)




| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| B | 0.35 | 0.40 | 0.48 | 0.014 | 0.016 | 0.019 |
| C | --- | 0.20 REF | --- | --- | 0.008 REF | --- |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D2 | 3.35 | 3.40 | 3.45 | 0.132 | 0.134 | 0.136 |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E2 | 4.25 | 4.30 | 4.35 | 0.167 | 0.169 | 0.171 |
| E | --- | 1.27 | --- | --- | 0.050 | --- |
| L | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| Y | 0.00 | --- | 0.050 | 0.000 | --- | 0.002 |

Figure 11-1 8-Pad WSON 8x6-mm (Package Code ZE)

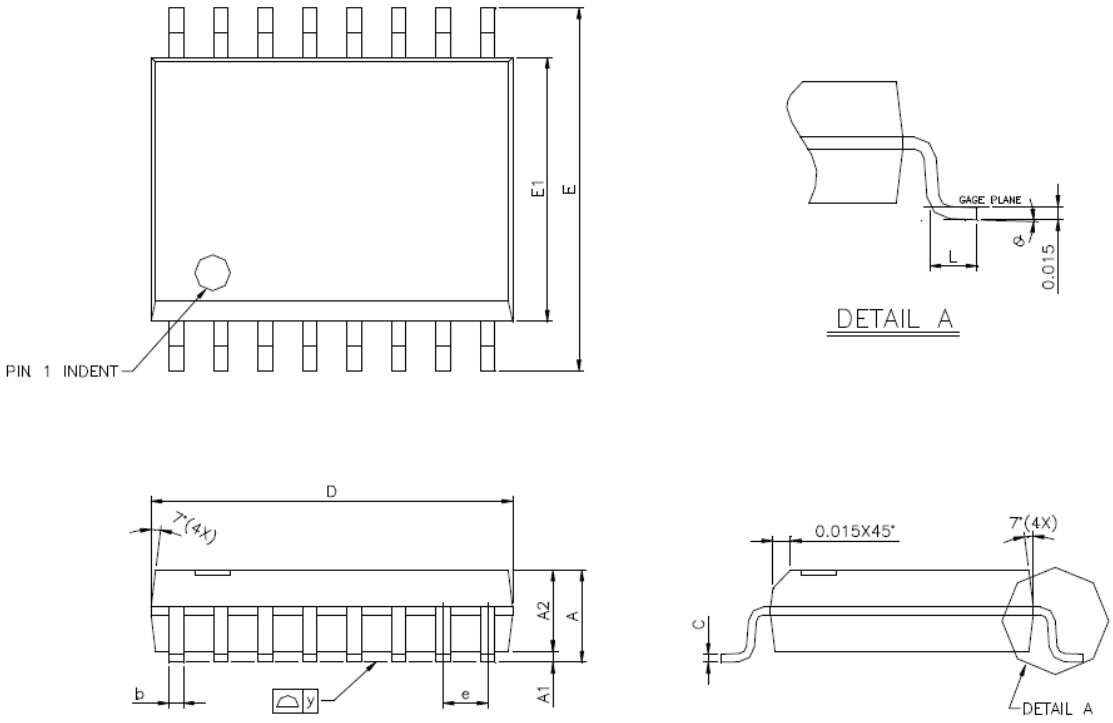
**Notes:**

1. The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.



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## 11.2 16-Pin SOIC 300mil (Package Code SF)



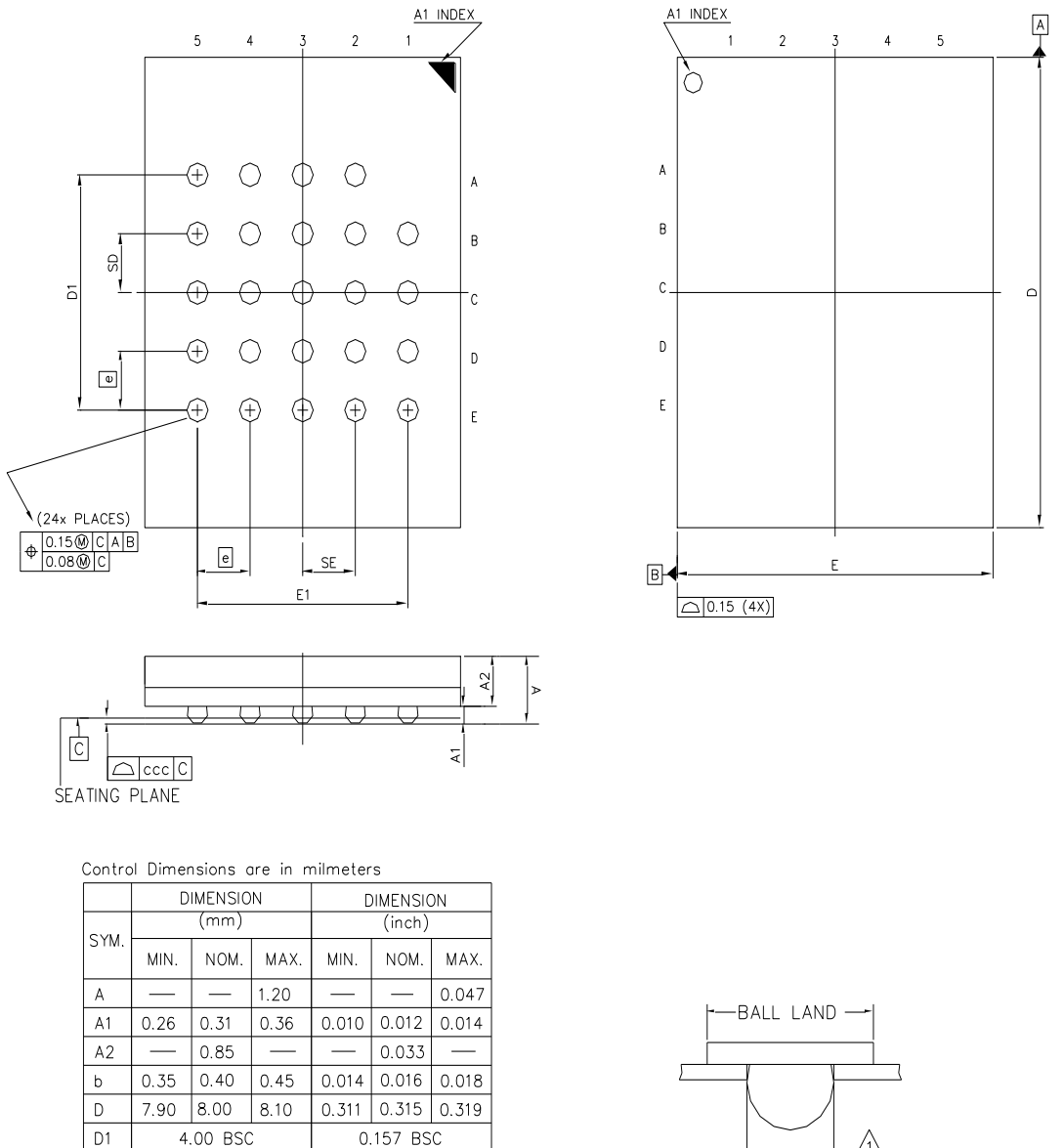

| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 2.36 | 2.49 | 2.64 | 0.093 | 0.098 | 0.104 |
| A1 | 0.10 | --- | 0.30 | 0.004 | --- | 0.012 |
| A2 | --- | 2.31 | --- | --- | 0.091 | --- |
| b | 0.33 | 0.41 | 0.51 | 0.013 | 0.016 | 0.020 |
| C | 0.18 | 0.23 | 0.28 | 0.007 | 0.009 | 0.011 |
| D | 10.08 | 10.31 | 10.49 | 0.397 | 0.406 | 0.413 |
| E | 10.01 | 10.31 | 10.64 | 0.394 | 0.406 | 0.419 |
| E1 | 7.39 | 7.49 | 7.59 | 0.291 | 0.295 | 0.299 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| L | 0.38 | 0.81 | 1.27 | 0.015 | 0.032 | 0.050 |
| y | --- | --- | 0.10 | --- | --- | 0.004 |
| θ | 0° | --- | 8° | 0° | --- | 8° |

Figure 11-2 16-Pin SOIC 300mil (Package Code SF)



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## 11.3 24-Ball TFBGA 8x6-mm (Package Code TB, 5x5-1 Ball Array)




Control Dimensions are in milmeters

| SYM. | DIMENSION (mm) | | | DIMENSION (inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.26 | 0.31 | 0.36 | 0.010 | 0.012 | 0.014 |
| A2 | — | 0.85 | — | — | 0.033 | — |
| b | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D1 | 4.00 BSC | | | 0.157 BSC | | |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E1 | 4.00 BSC | | | 0.157 BSC | | |
| SE | 1.00 TYP | | | 0.039 TYP | | |
| SD | 1.00 TYP | | | 0.039 TYP | | |
| e | 1.00 BSC | | | 0.039 BSC | | |
| ccc | – | – | 0.10 | – | – | 0.0039 |



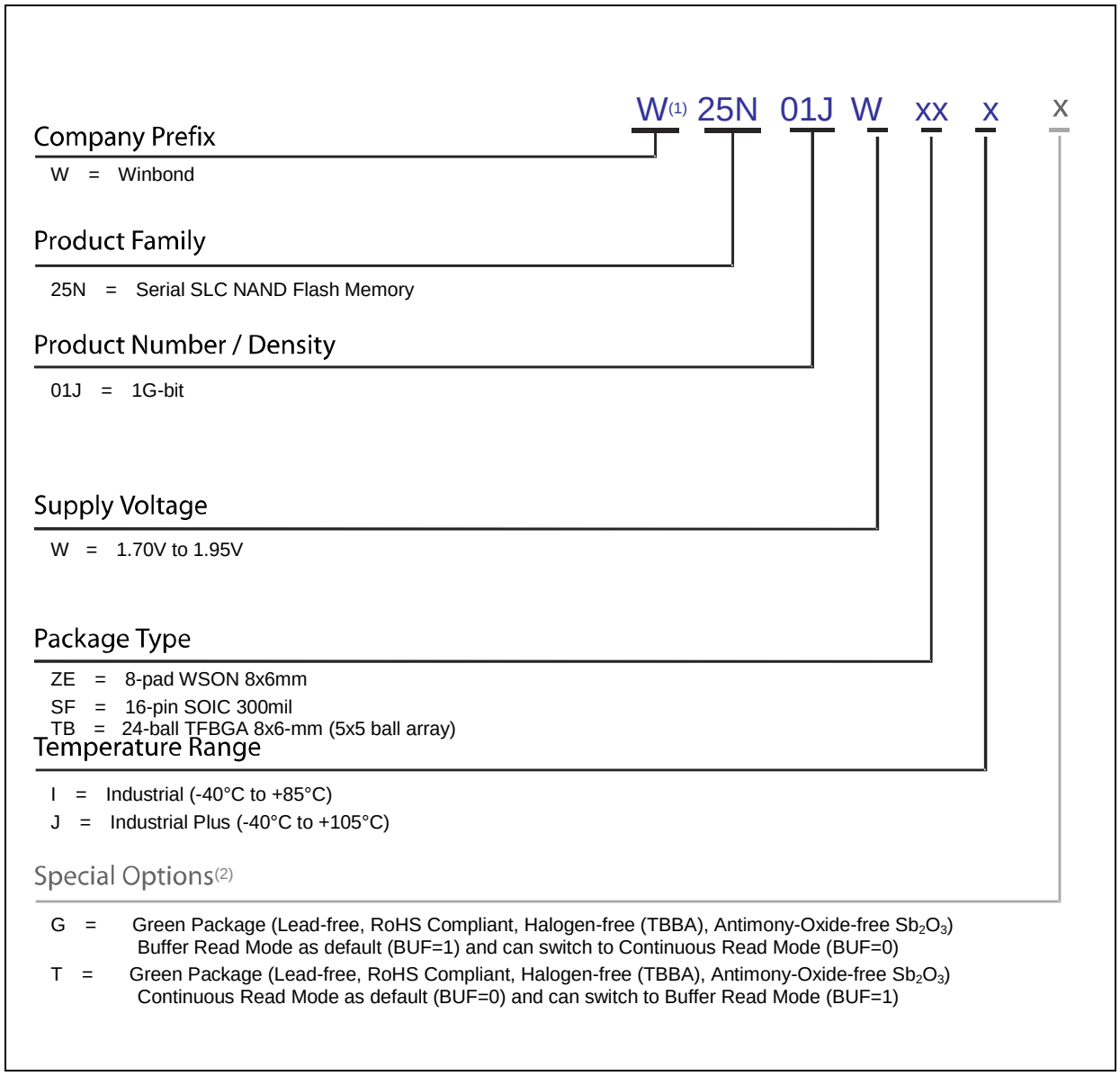

Note:
1. Ball land:0.45mm. Ball opening:0.35mm.
PCB ball land suggested <=0. 35 mm

Figure 11-3 24-Ball TFBGA 8x6-mm (Package Code TB, 5x5-1 Ball Array)



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## 12. ORDERING INFORMATION




**Notes:**

1. The "W" prefix is not included on the part marking.
2. Standard bulk shipments are in tray for WSON and TFBGA packages. For other packing options, please specify when placing orders.



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## 12.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25N01JW SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 11-digit number.

**Industrial Grade:**

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **ZE**<br>WSON-8 8x6mm | 1G-bit | W25N01JWZEIG<br>W25N01JWZEIT | 25N01JWZEIG<br>25N01JWZEIT |
| **SF**<br>SOIC-16 300mil | 1G-bit | W25N01JWSFIG<br>W25N01JWSFIT | 25N01JWSFIG<br>25N01JWSFIT |
| **TB**<br>TFBGA-24 8x6mm<br>(5x5-1 Ball Array) | 1G-bit | W25N01JWTBIG<br>W25N01JWTBIT | 25N01JWTBIG<br>25N01JWTBIT |

**Industrial Plus Grade:**

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **ZE**<br>WSON-8 8x6mm | 1G-bit | W25N01JWZEJG<br>W25N01JWZEJT | 25N01JWZEJG<br>25N01JWZEJT |
| **SF**<br>SOIC-16 300mil | 1G-bit | W25N01JWSFJG<br>W25N01JWSFJT | 25N01JWSFJG<br>25N01JWSFJT |
| **TB**<br>TFBGA-24 8x6mm<br>(5x5-1 Ball Array) | 1G-bit | W25N01JWTBJG<br>W25N01JWTBJT | 25N01JWTBJG<br>25N01JWTBJT |

**Notes:**

1. W25N01JWxxxG: BUF=1 (Buffer Read Mode) is the default value after power up. BUF bit can be written to 0.
2. W25N01JWxxxT: BUF=0 (Continuous Read Mode) is the default value after power up. BUF bit can be written to 1.



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## 13. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| 0.1 | 12/15/2016 | | New Create as Advanced Information |
| 0.2 | 5/19/2017 | | Add HW RESET, SR4 and SOIC-16<br>Update Command table |
| 0.3 | 8/27/2018 | 14, 22, 37, 38<br>11<br>16<br>18<br>47<br>76<br>76<br>80<br>81<br>83 | Update about Bad Block Management<br>Update Figure 5-1, ECC protected spare area<br>Update Interface Status table<br>Add QE bit in Software Protection table<br>Add description for page program sequence<br>tVSL change to 700us<br>Update Figure9-2<br>Remove “DTR” from /HOLD related parameters<br>Update Figure9-4 and 9-5<br>Add Invalid Block Management |
| 0.4 | 5/20/2019 | 19, 32<br>72<br>-, 78 | Change default value of SR-2 QE bit from 0 to 1<br>Add Integrity CRC value<br>Remove Chip Erase instruction |
| 0.5 | 7/1/2019 | 12<br>32<br><br>33 | Update Figure 6-1 for Auto Page Data Read operation<br>Update Default values of the Status Registers after power up and Device Reset table<br>Add Auto Page Data Read (13h) execution during power up and after Device Reset table |
| A | 10/9/2019 | <br>6<br>6, 73, 75, 85, 86<br>22<br>22<br>32<br>62<br>67<br>74 | Remove Preliminary<br>Added note 4. Endurance specification<br>Added Industrial Plus Grade<br>Updated P-FAIL & E-FAIL bits description<br>Revised ECC Status description table<br>Updated Note 1<br>Updated Figure 8-43<br>Updated Figure 8-51<br>Updated tVSL, tPUW and Figure 9-1 |
| B | 3/13/2020 | 19<br>71 | Corrected reference section number (8.2.26 to 8.2.38)<br>Corrected SR1-L OTP Lock Operation description |



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| | | | |
|---|---|---|---|
| C | 5/24/2021 | - | Corrected typos |
| | | 6 | Updated descriptions for endurance and data retention |
| | | 6 | Added Notes. 3 |
| | | 11 | Updated Figure 5-1 |
| | | 12 | Updated Figure 6-1 |
| | | 13, 14 | Updated 6.1.6 Software Reset and 6.1.7 Hardware Reset |
| | | 14 | Updated explanation about power-up and power-down sequence |
| | | 20 | Added ECC protected area and constraint when ECC-E=1 |
| | | 22 | Added a Page Data Read command as ECC status bit clear timing |
| | | 23 | Updated Notes. 1 |
| | | 23 | Removed Chip Erase |
| | | 28, 29, 30, 31 | Updated Instruction Set Table format |
| | | 32 | Updated Notes.11 |
| | | 33, 34 | Updated 8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h) |
| | | 34 | Updated the table for Default values of the Status Registers |
| | | 39 | Added command sequence explanation sentence for Bad Block Management |
| | | 73 | Updated the last row of the table |
| | | 75 | Added tPWD and VPWD spec |
| | | 75 | Updated Figure 9-1 |
| | | 76 | Updated Notes.1 |
| | | 77 | Updated Figure 9-3 |
| | | 78 | Updated descriptions for $F_R$ and $f_R$ specs |
| | | 79 | Added tRD3 spec |
| | | 79 | Updated Notes.4 |
| | | 82 | Updated description for the Initial Invalid Block mark |
| | | 83 | Added section for “Error in Operation” |
| | | 83 | Added section for “Addressing in Program Operation” |
| | | 84 | Added Notes.1 |
| | | 86 | Updated the 5x5 ball BGA package information |
| | | 87 | Updated description for special options |

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