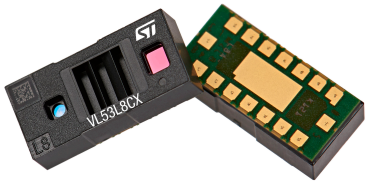
VL53L8CX

Datasheet

Low-power high-performance 8x8 multizone Time-of-Flight (ToF) sensor



Product status link
VL53L8CX

Features

- New generation, multizone Time-of-Flight (ToF) sensor with low-power and enhanced distance ranging performance
  - Multizone distance measurement capability with either 4x4 or 8x8 separate zones
  - Autonomous low-power mode with interrupt programmable threshold to wake up the host
  - Ranging up to 400 cm, with enhanced performance under ambient light
  - Multitarget detection and distance measurement in each zone
  - Histogram processing and algorithmic compensation to minimize or remove the impact of cover glass crosstalk
  - Motion indicator for each zone to show if targets have moved and how they have moved
  - Frame rate capability of 60 Hz
- Fully integrated miniature module with wide field of view (FoV)
  - New generation, high-power emitter: 940 nm invisible light VCSEL (vertical-cavity surface-emitting laser) and integrated analog driver
  - 65° diagonal square FoV using DOEs (diffractive optical elements) on both transmitter and receiver
  - Receiving array of SPADS (single photon avalanche diodes)
  - Low-power microcontroller running firmware
  - Size: 6.4 x 3.0 x 1.75 mm
- Easy integration
  - Single reflowable component
  - Requires 1.8 V core supply and 3.3 V AVDD supply
  - Optional 1.2 V or 1.8 V IOVDD interface voltage levels
  - I²C (up to 1 MHz) or SPI (up to 3 MHz) interface
  - Compatible with wide range of cover glass materials
  - Can be hidden behind a dark cover glass

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Application

- Robotic applications in difficult environments including SLAM, wall tracking, small object detection, cliff prediction, and floor type recognition
- System activation under ambient light for smart buildings and smart lighting. For example: user detection to wake up devices
- Content management for tanks, loads in trucks, and waste bins
- Liquid level monitoring
- Gesture recognition
- Keystone correction for video projectors
- Devices requiring better ambient light immunity
- Augmented reality/Virtual reality enhancement. Dual camera stereoscopy and 3D depth assistance thanks to multizone distance measurements
- IoT and battery powered devices for user and object detection
- LAF (laser assisted autofocus), which enhances the camera AF system speed and robustness, especially in difficult low light or low contrast scenes.

Description

The VL53L8CX is an 8x8 multizone, ToF ranging sensor, which enhances performance under ambient light with a reduced power consumption. Based on STMicroelectronics' FlightSense technology, the sensor is designed to provide accurate ranging up to 400 cm with a 65° diagonal FoV.

The VL53L8CX integrates a powerful new generation VCSEL, and two advanced metasurface lenses. The hardware is housed in an innovative "all in one" module. This enables a wider variety of high-performance usecases, such as low-power system activation, gesture recognition, SLAM for robotics, liquid level monitoring, and many more.

Thanks to STMicroelectronics' patented algorithms, the VL53L8CX can detect and track multiple targets within the FoV, with a 64-zone depth measurement. The STMicroelectronics' histograms ensure a cover glass crosstalk immunity above 60 cm.

Like all ToF sensors based on STMicroelectronics' FlightSense technology, the VL53L8CX measures an absolute distance regardless of the target color and reflectance.

The VL53L8CX supports SPI and I²C interfaces for high frequency frame rates and short-boot times.

The VCSEL of the VL53L8CX emits fully invisible 940 nm IR light. Such VCSEL has a Class 1 certification that is safe for the eyes. Scene browsing and multizone detection are possible with the VL53L8CP. This is due to a software customizable detection array. It detects human presence quickly and at low-power. Such detection is known as a minidepth map.

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1 Acronyms and abbreviations

Acronym/abbreviation	Definition
AF	autofocus
API	application programming interface
AR/VR	augmented reality/virtual reality
DOE	diffractive optical element
ESD	electrostatic discharge
FoV	field of view
FoI	field of illumination
GPIO	general-purpose input/output
HP	high power
I^2C	inter-integrated circuit (serial bus)
LAF	laser autofocus
LGA	land grid array
LP	low power
MCLK	main serial clock
MISO	main input secondary output
MOSI	main output secondary input
NCS	chip select
NVM	non-volatile memory
PCB	printed circuit board
PDAF	phase detection autofocus
PLL	phase-locked loop
PVT	process, voltage, and temperature
POR	power on reset
RAM	random-access memory
SPAD	single photon avalanche diode
SW	software
ToF	Time-of-Flight
UI	user interface
UM	user manual
VCSEL	vertical-cavity surface-emitting laser

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2 Product overview

2.1 Technical specifications

Table 1. Technical specifications

Feature	Detail
Package	Optical LGA16
Size	6.4 x 3.0 x 1.75 mm
Ranging	2 to 400 cm per zone
Operating voltage	AVDD: 3.3 V CORE_1V8: 1.8 V IOVDD: 1.2/1.8 V
Operating temperature	-30 to 85°C
Sample rate	Up to 60 Hz
Infrared emitter	940 nm
I²C and SPI interface	I²C: 1 MHz serial bus, address: 0x52 SPI: 3 MHz
Operating ranging mode	Continuous or autonomous (see UM3109 for more information)

2.2 Field of view

The Rx (or collector) exclusion zone includes all module assembly tolerances. It is used to define the cover glass dimensions. The cover glass opening must be equal to or wider than the exclusion zone.

The detection volume represents the applicative or system FoV in which a target is detected, and a distance measured. The Rx lens or the Rx aperture determines the detection volume. It is narrower than the exclusion zone.

Figure 1. System FoV and exclusion zone description (not to scale)

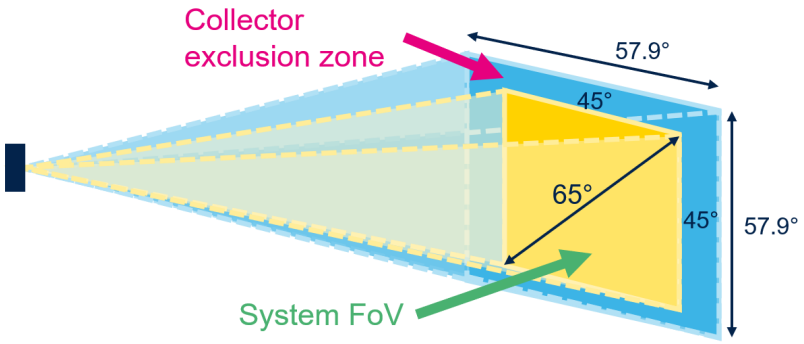


Table 2. FoV angles

	Horizontal	Vertical	Diagonal
Detection volume	45°	45°	65°
Collector exclusion zone	57.9°	57.9°	86.6°

Note: The detection volume depends on the following: environment and sensor configuration, target distance, reflectance, ambient light level, sensor resolution, sharpener, ranging mode, and integration time.

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Note: The detection volume of Table 2. FoV angles has been measured with a white 88% reflectance perpendicular target. This measurement was taken:

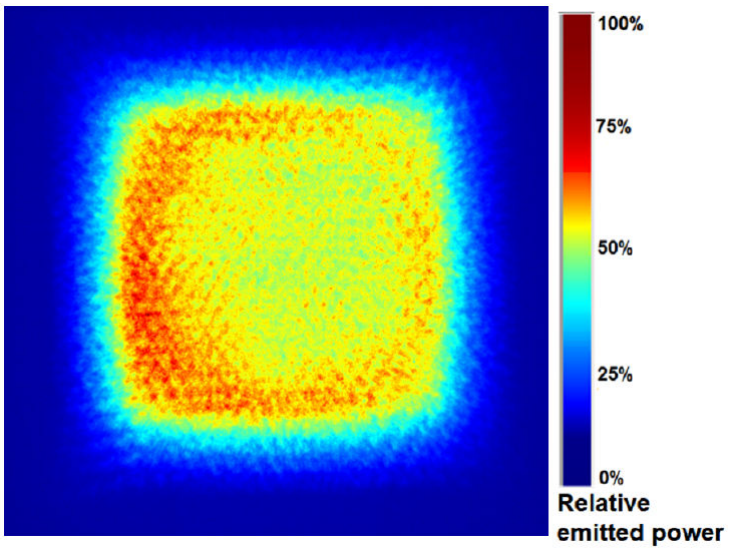
- *In full FoV*
- *Located at 1 m from the sensor*
- *Without ambient light (dark conditions)*
- *With an 8x8 resolution*
- *With a 14% sharpener (default value)*
- *In continuous mode*
- *At 15 Hz*

2.3 Field of illumination

The VCSEL field of illumination (FoI) is shown in the figure below. The relative emitted signal power depends on the FoI angle. It corresponds to:

- 43.4° x 43.4°, considering a beam with a 75% signal from the maximum.
- 57.9° x 57.9°, considering a beam with a 10% signal from the maximum.

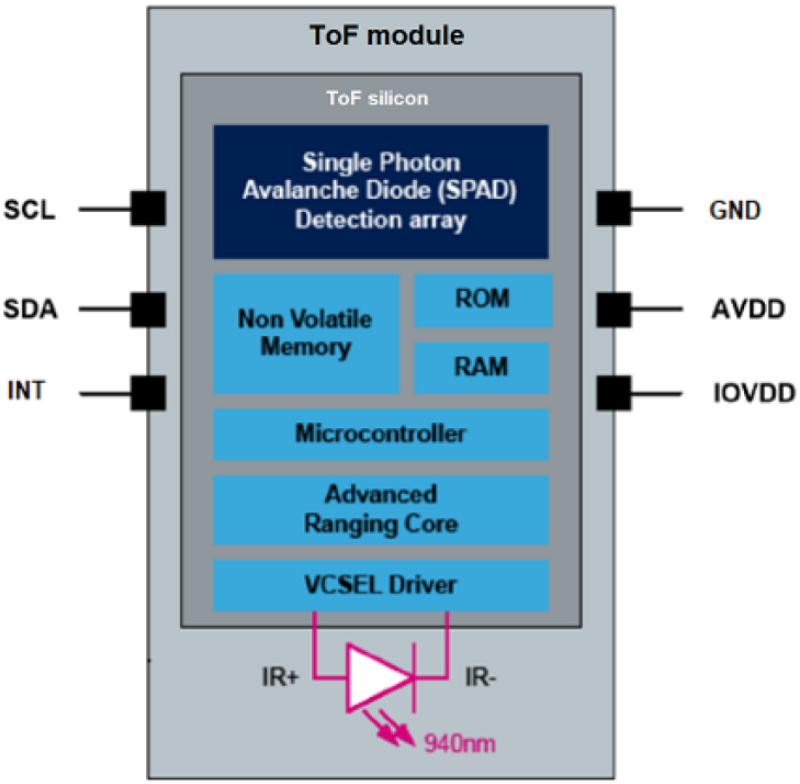
Figure 2. VL53L8CX FoI



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2.4 System block diagram

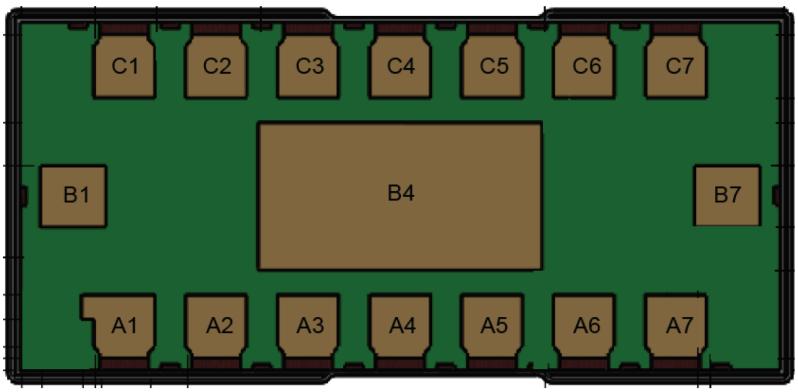
Figure 3. **VL53L8CX block diagram**



2.5 Device pinout

Figure 4. VL53L8CX pinout (bottom view) shows the pinout of the VL53L8CX.

Figure 4. **VL53L8CX pinout (bottom view)**



The VL53L8CX pin description for the I²C and SPI configuration is given in Table 3. VL53L8CX pin description for I²C and SPI configuration. For the pins that support both I²C and SPI protocol, the I²C description is listed first and the SPI second.

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Table 3. VL53L8CX pin description for I²C and SPI configuration

Pin number	Signal name	Signal type	Signal description
A1	INT	Digital input/output (I/O)	Interrupt output, defaults to open drain output (tristate), 47 kΩ pullup resistor to IOVDD required
A2	LPn	Digital input	Enables communication. Drive this pin to logic 0 to disable I²C communication when the device is in low-power mode. Drive this pin to logic 1 to enable I²C communication in low-power mode. This pin is typically used when you need to change the I²C address in multidevice systems. If it is not used, or if interfacing via the SPI, connect to IOVDD with a 47 kΩ pullup resistor.
A3	IOVDD	Power	1.2 V or 1.8 V I/O supply
A4	SDA / MOSI	Digital input/output (I/O)	**I²C**: Data (bidirectional), 2.2 kΩ pullup resistor required to IOVDD **SPI**: Main output secondary input
A5	SCL/MCLK	Digital input	**I²C**: Clock (input), 2.2 kΩ pullup resistor required to IOVDD **SPI**: Main clock
A6	RSVD1	Reserved	Connect to ground
A7	RSVD2	Reserved	Connect to ground
B1	SYNC	Digital input/output (I/O)	General purpose I/O, defaults to open drain output (tristate), 47 kΩ pullup resistor required to IOVDD
B4	THERMALPAD	Ground	Connect to a ground plane to allow good thermal conduction
B7	CORE_1V8	Power	1.8 V analog core supply
C1	SPI_I2C_N	Digital input	**I²C**: Low value selects I²C mode - Connect to GND with 47 kΩ pulldown resistor. Also used as I²C interface reset pin, active high. Toggle this pin from 0 to 1, then back to 0 to reset the I²C target. **SPI**: Connect to IOVDD with 47 kΩ pullup resistor
C2	NCS	Digital input	**I²C**: Not used - Connect to GND with 47 kΩ pulldown resistor **SPI**: Active low chip select. 47 kΩ pullup resistor required to IOVDD
C3	GND	Ground	Ground
C4	AVDD	Power	3.3 V analog and VCSEL supply
C5	MISO	Digital output	**I²C**: Do not connect **SPI**: Main input secondary output. Push-pull driven to IOVDD level
C6	RSVD3	Reserved	Connect to ground
C7	Ground	Ground	Ground

Note: The THERMALPAD pin has to be connected to ground (for more information refer to the AN5897).

Note: All digital signals must be driven to the IOVDD level.

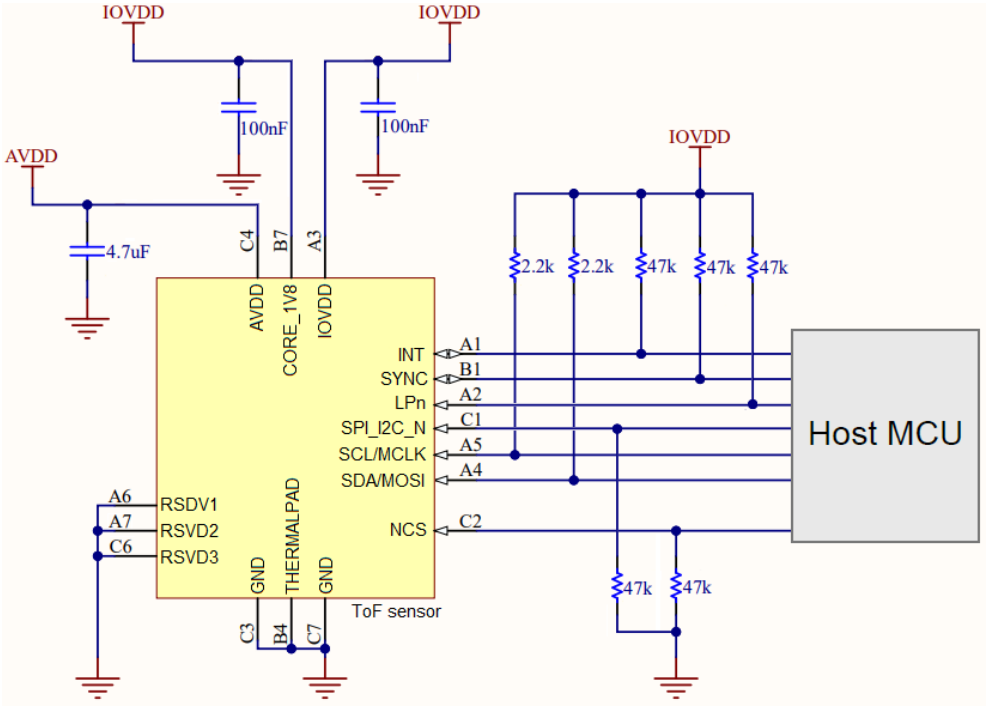
Note: Toggling the I2C_RST pin resets the sensor I²C communication only. It does not reset the sensor itself. To reset the sensor, refer to the sensor reset management procedure (UM3109).

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2.6 Application schematics

Figure 5. Typical application schematic for I²C shows the application schematic of the VL53L8CX in I²C protocol configuration.

Figure 5. Typical application schematic for I²C



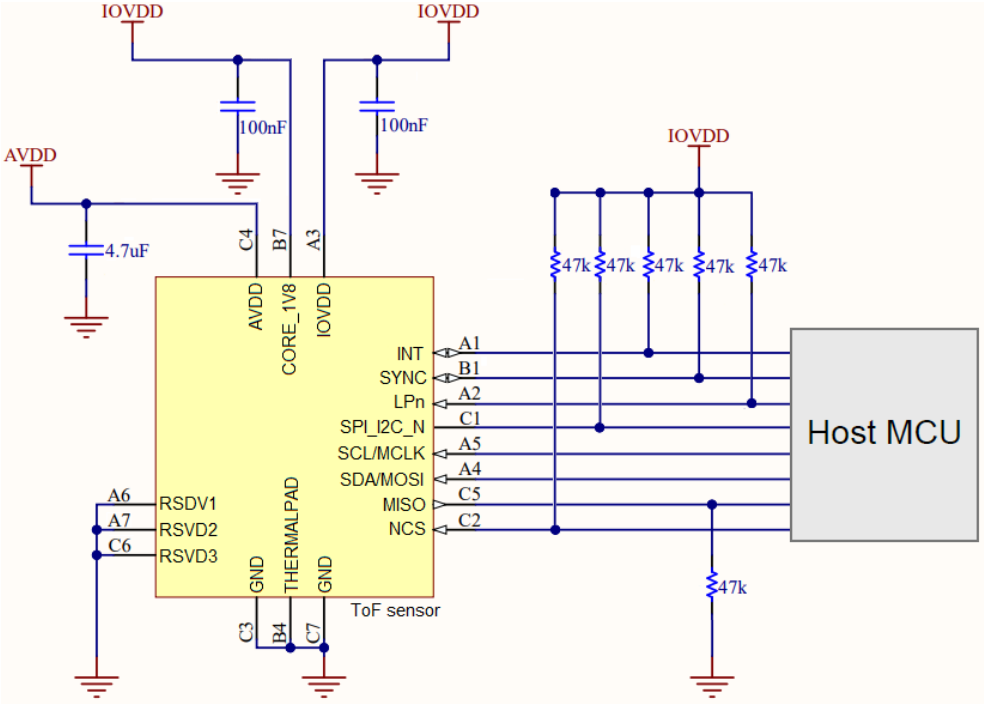
Note: Capacitors on the external supplies (AVDD, CORE_1V8, and IOVDD) should be placed as close as possible to the module pins.

Note: IOVDD must be set to ensure the host and the VL53L8CX operate at the same voltage levels for direct interfacing.

Figure 6. Typical application schematic for SPI shows the application schematic of the VL53L8CX in SPI protocol configuration.

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Figure 6. Typical application schematic for SPI



Note: Capacitors on the external supplies (AVDD, CORE_1V8, and IOVDD) should be placed as close as possible to the module pins.

Note: IOVDD must be set to ensure the host and the VL53L8CX operate at the same voltage levels for direct interfacing.

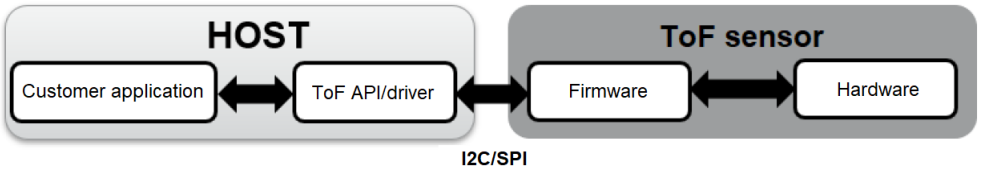
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3 Functional description

3.1 Software interface

This section describes the software interface of the device. The host customer application controls the VL53L8CX using an application programming interface (API). The API implementation is delivered to the customer as a driver (C code and reference Linux® driver). The driver provides the customer application with a set of high level functions that allow control of the VL53L8CX firmware. This includes control of items such as device initialization, ranging start/stop, and mode select.

Figure 7. VL53L8CX system functional description



3.2 Power state machine

Figure 8. Power state machine

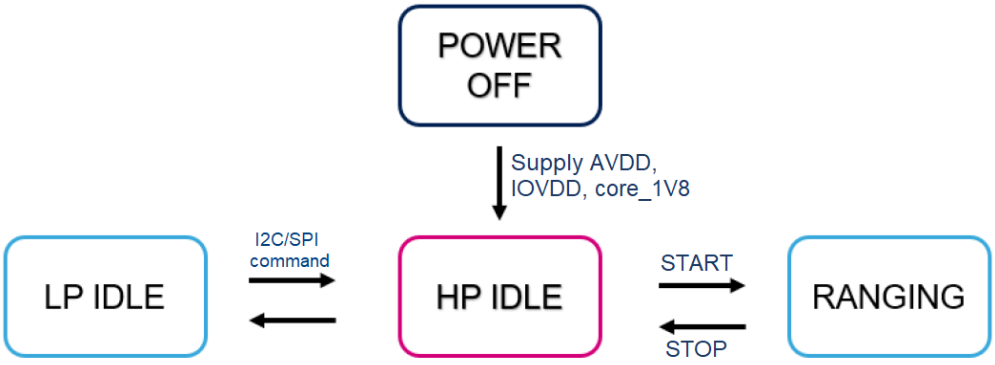


Table 4. Power state description

Device state	Description
LP idle	LP (low-power) idle state with data retention RAM and register content retained Allow fast resume to HP (high-power) I²C communication disabled if using LPn
HP idle	HP idle state Device needs to be in HP idle state to start ranging Power up state
Ranging	Full operation VCSEL is active (pulsing)

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3.3 Power up sequence

The VL53L8CX requires three power supplies:

- CORE_1V8: Analog core supply fixed at 1.8 V.
- AVDD: Analog and VCSEL supply fixed at 3.3 V.
- IOVDD: Voltage supply to the IO, which may be either 1.2 V or 1.8 V depending on the system it is integrating with. If IOVDD is 1.8 V, then the same supply may be used for both IOVDD and CORE_1V8.

When powering up the device, the three supplies should be applied at the same time.

When powering down the device, the three supplies should be removed at the same time.

To ensure proper operation of the module, the following minimum slew rates on the supplies (see Figure 9. Power up slew) must be met. This ensures correct operation of the power on the reset circuitry. The circuitry triggers at 0.9 V. However, the supplies should reach their operation levels in accordance with the slew rates listed in Table 5. Supply slew minimum limits.

Figure 9. Power up slew



Note: The minimum reset time is the minimum time required for the device RAM to load and boot up after CORE_1V8 reaches the power-on reset rising threshold. The supply must have reached the minimum operating level (1.6 V) within this time.

Note: The AVDD rise time is determined by the internal analog levels, which must be stable for correct operation.

Note: CORE_1V8 and IOVDD are assumed to be the same supply (1V8) in Figure 9. Power up slew. If using 1V2, then IOVDD should be applied at the same time as the other supplies.

Table 5. Supply slew minimum limits

Supply status	AVDD slew	CORE_1V8 slew	IOVDD slew
Start together	0.001 V/µs	0.012 V/µs	0.012 V/µs
AVDD stable followed by CORE_1V8 and IOVDD	—	0.012 V/µs	0.012 V/µs
CORE_1V8 stable followed by AVDD and IOVDD	0.001 V/µs	—	0.012 V/µs
IOVDD stable followed by AVDD and CORE_1V8	0.001 V/µs	0.012 V/µs	—

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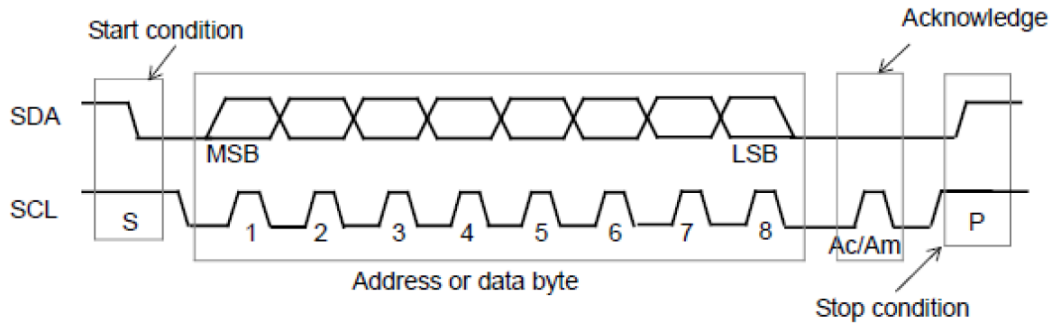
4 I²C control interface

This section specifies the control interface. The I²C interface uses two signals: serial data line (SDA) and serial clock line (SCL). Each device connected to the bus uses a unique address and a simple controller/target relationship exists.

Both SDA and SCL lines are connected to a positive supply voltage using pull-up resistors located on the host. Lines are only actively driven low. A high condition occurs when lines are floating and the pull-up resistors pull lines up. When no data is transmitted both lines are high.

The controller device performs the clock signal (SCL) generation and initiates data transfer. The I²C bus on the VL53L8CX has a maximum speed of 1 Mbits/s and uses a device 8-bit address of 0x52.

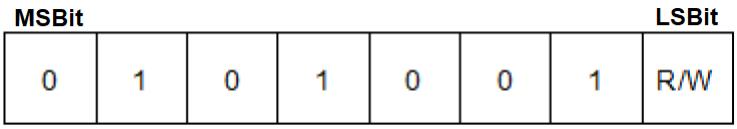
Figure 10. Data transfer protocol



Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit, Ac for VL53L8CX acknowledge and Am for controller acknowledge (host bus controller). The internal data is produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

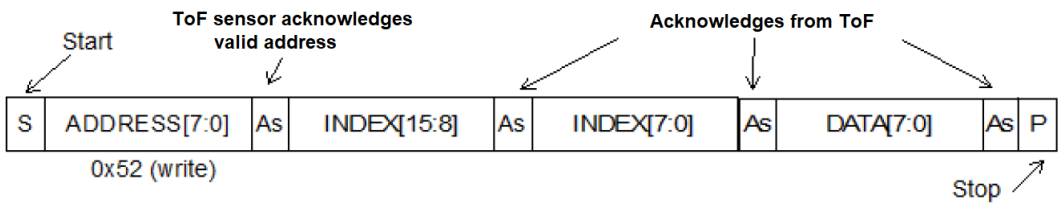
A message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition but without a preceding stop condition) followed by another message. The first byte contains the device address (0x52) and also specifies the data direction. If the least significant bit is low (that is, 0x52) the message is a controller-write-to-the-target. If the lsb is set (that is, 0x53) then the message is a controller-read-from-the-target.

Figure 11. VL53L8CX I²C device address: 0x52



All serial interface communications with the Time-of-Flight sensor must begin with a start condition. The VL53L8CX module acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/write bit (lsb of the address byte) is stored and the next byte of data, sampled from the SDA, can be interpreted. During a write sequence, the second byte received provides a 16-bit index, which points to one of the internal 8-bit registers.

Figure 12. VL53L8CX data format (write)

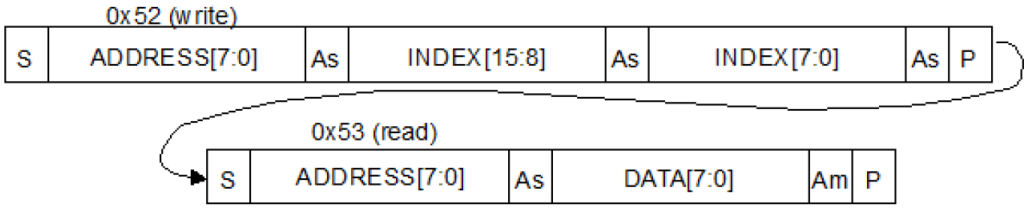


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As data are received by the target, they are written bit by bit to a serial/parallel register. After each data byte has been received by the target, an acknowledge is generated, the data are then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index is read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 13. VL53L8CX data format (read)



At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the VL53L8CX for a write and the host for a read).

A message can only be terminated by the bus controller, either by issuing a stop condition or by a negative acknowledge (that is, not pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports autoincrement indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The controller can therefore send data bytes continuously to the target until the target fails to provide an acknowledge or the controller terminates the write communication with a stop condition. If the autoincrement feature is used, the controller does **not** have to send address indexes to accompany the data bytes.

Figure 14. VL53L8CX data format (sequential write)

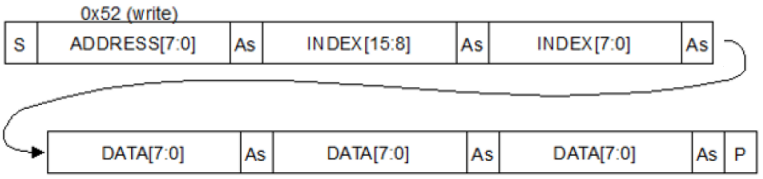
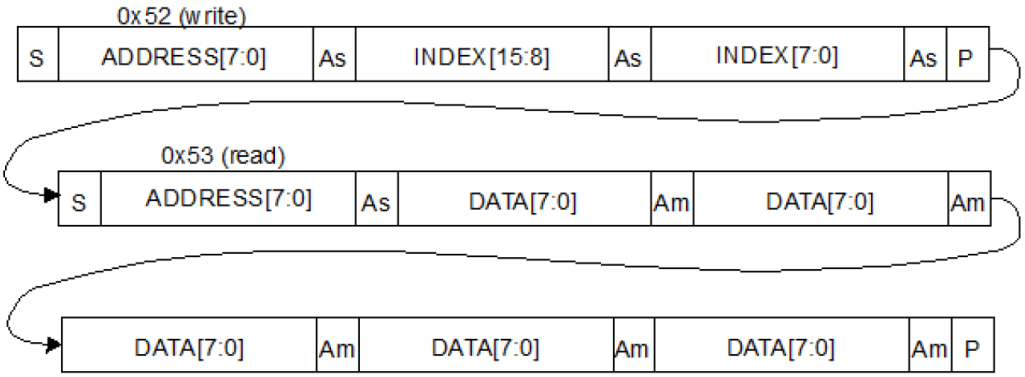


Figure 15. VL53L8CX data format (sequential read)



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4.1 I²C interface - timing characteristics

Timing characteristics are shown in Table 6. I²C interface - timing characteristics for fast mode plus (1 MHz) and Table 7. I²C interface - timing characteristics for fast mode (400 kHz). Refer to Figure 16. I²C timing characteristics for an explanation of the parameters used.

Timings are given for all process, voltage, and temperature (PVT) conditions.

Table 6. I²C interface - timing characteristics for fast mode plus (1 MHz)

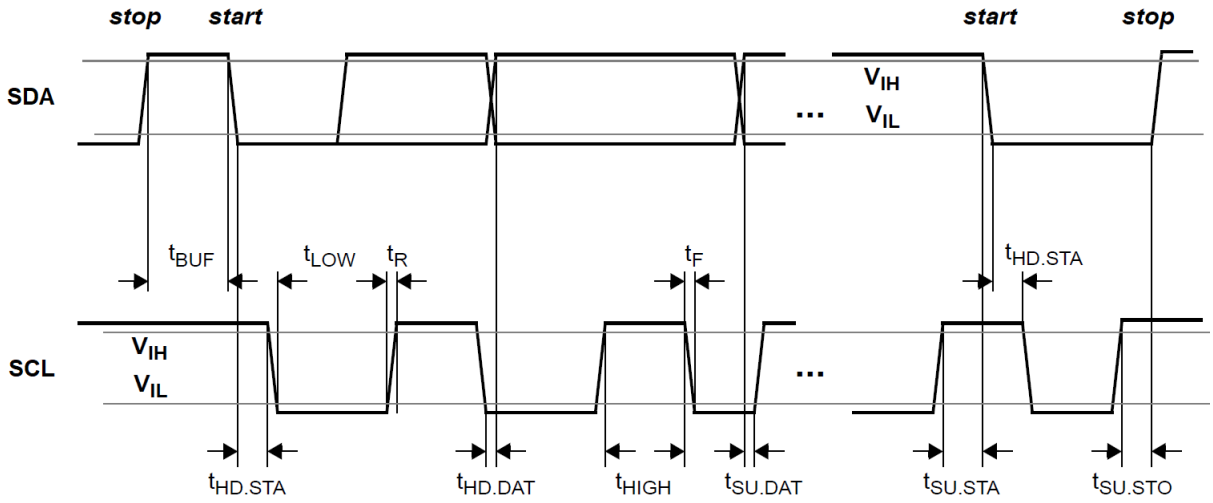
Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	—	1000	kHz
t_{LOW}	Clock pulse width low	0.5	—	—	µs
t_{HIGH}	Clock pulse width high	0.26	—	—	µs
t_{SP}	Pulse width of spikes, which are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	0.5	—	—	µs
$t_{HD.STA}$	Start hold time	0.26	—	—	µs
$t_{SU.STA}$	Start setup time	0.26	—	—	µs
$t_{HD.DAT}$	Data in hold time	0	—	0.9	µs
$t_{SU.DAT}$	Data in setup time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	120	ns
t_F	SCL/SDA fall time	—	—	120	ns
$t_{SU.STO}$	Stop setup time	0.26	—	—	µs
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
Cin	Input capacitance (SCL)	—	—	4	pF
C_L	Load capacitance (1V8)	—	140	550	pF
	Load capacitance (1V2)	—	140	150	pF

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Table 7. I²C interface - timing characteristics for fast mode (400 kHz)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I2C}	Operating frequency	0	—	400	kHz
t_{LOW}	Clock pulse width low	1.3	—	—	µs
t_{HIGH}	Clock pulse width high	0.6	—	—	µs
t_{SP}	Pulse width of spikes, which are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	1.3	—	—	µs
$t_{HD.STA}$	Start hold time	0.26	—	—	µs
$t_{SU.STA}$	Start setup time	0.26	—	—	µs
$t_{HD.DAT}$	Data in hold time	0	—	0.9	µs
$t_{SU.DAT}$	Data in setup time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	300	ns
t_F	SCL/SDA fall time	—	—	300	ns
$t_{SU.STO}$	Stop setup time	0.6	—	—	µs
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
Cin	Input capacitance (SCL)	—	—	4	pF
C_L	Load capacitance (1V8)	—	125	400	pF
	Load capacitance (1V2)	—	125	400	pF

Figure 16. I²C timing characteristics



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5 SPI timing specification

This section specifies the SPI control interface used to control data transfer.

The communication interface is based on a 4-wire, serial, synchronous interface between the host (controller) and the VL53L8CX (target device). Refer to the schematics in Section 2.6 Application schematics. The 4-wire interface comprises the following four signals:

- NCS: Chip select (active low)
- MCLK: Main serial clock
- MOSI: Main output secondary input, data output from controller
- MISO: Main input secondary output, data output from target

All signals are CMOS inputs/outputs. Their levels are in line with the IOVDD supply. The SPI modes supported are clock polarity = 1 and clock phase = 1. These modes correspond to data captured on a clock's rising edge and data propagated on a falling edge. The controller selects the target device with the NCS. The NCS enables target transmission. It is an active low signal. After the device is selected with the falling edge of the NCS, an 8-bit command can be received. If the VL53L8CX has not been activated using the NCS chip select line, the MCLK input clock and MOSI signals are disregarded.

The falling edge (high to low transition) of the NCS signal is required to initiate an action. The transmission ends with the rising edge (low-to-high transition). This causes the end of data transfer, and resets the internal counter and command registers. All this reinitializes the serial communication.

While the register address is applied on the MOSI pin, the same information is mirrored on the MISO pin.

The NCS can be reset to a noncommunication state (high) at any time, including during a transaction. Should this happen, the device resets its internal state machine. Consequently, any ongoing communications are aborted. No internal changes to the registers occur, and the interface is ready to receive a new transaction again. However, the SPI target can tolerate the MCLK being interrupted. It can resume at any point in time, without specific duration limit.

During each SPI clock cycle, a full duplex data transmission occurs. The MOSI input is the data signal, provided by the host to the device. It carries both the address and data information in write mode. Only address information is in read mode. The controller sends a bit on the MOSI line and the target reads it. Concurrently, the target sends a bit on the MISO line and the controller reads it. This sequence is maintained even when only one-directional data transfer is intended.

The MISO output is the data signal, provided by the device to the host. It carries the data in read mode only, and the mode register content during the address setup. Any internal register that can be written to, can also be read from. There are also read-only registers that contain device status information. For example, design revision details. A read instruction from an unused register location returns the value 0x00. A read instruction from the manufacturer's specific registers may return any value. A write instruction to a reserved or unused register location is illegal. The effect of such a write is ignored. Transmission may continue for any number of clock cycles. When complete, the controller stops toggling the clock signal, and typically deselects the target.

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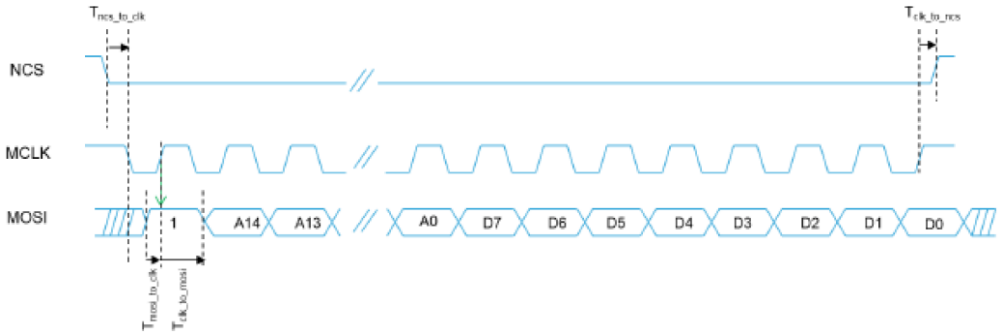
Table 8. **SPI interface timing specification**

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating frequency	F_{spi}	—	3	MHz	MCLK
Time from NCS active and MCLK falling edge	$T_{ncs_to_clk}$	0	—	ns	
Rise/Fall time on MISO	$T_{riseFallMiso}$	—	3	ns	With 20 pF load max
Duty cycle	Duty	40	60	%	
Time from MOSI stable to MCLK rising edge	$T_{mosi_to_clk}$	16	—	ns	
Time MOSI must remain stable after MCLK rising edge	$T_{clk_to_ncs}$	16	—	ns	
Time from last MCLK rising edge to NCS going inactive	$T_{clk_to_dat}$	0	—	ns	
Propagation delay from falling MCLK edge to MISO data valid		—	20	ns	With 20 pF load max

5.1 SPI write messages

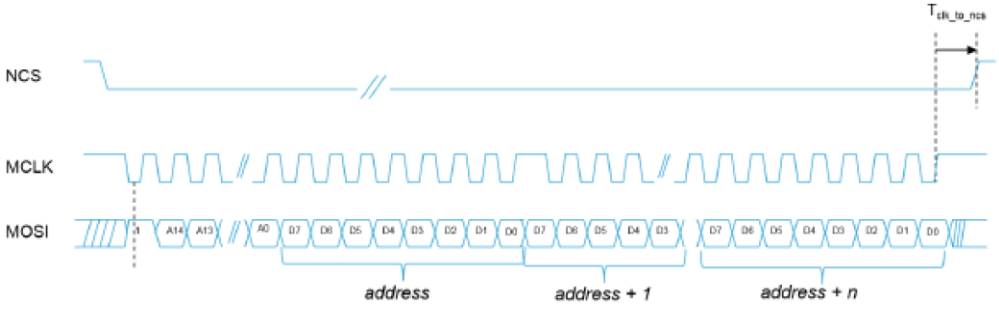
The write timing sequence is shown in Figure 17. SPI writing timing sequence. Once the NCS selects the device, the controller sends a write command to the VL53L8CX. The controller then provides a clock to output the status. The writing sequence starts with the MOSI initial value equal to 1. The address is sent first, and the data is sent afterwards. The most significant bit is sent first (big-endian format). The address length is 15 bits. Data length is 8 bits.

Figure 17. **SPI writing timing sequence**



If the host continues to transmit data beyond the first 8 data bits, then the target goes into autoincrement write mode. The autoincrement write timing sequence is shown in Figure 18. SPI autoincrement write sequence. The MOSI initial value is 1. The address is incremented automatically and internally by the target. Subsequent data bits correspond to incrementing addresses.

Figure 18. **SPI autoincrement write sequence**



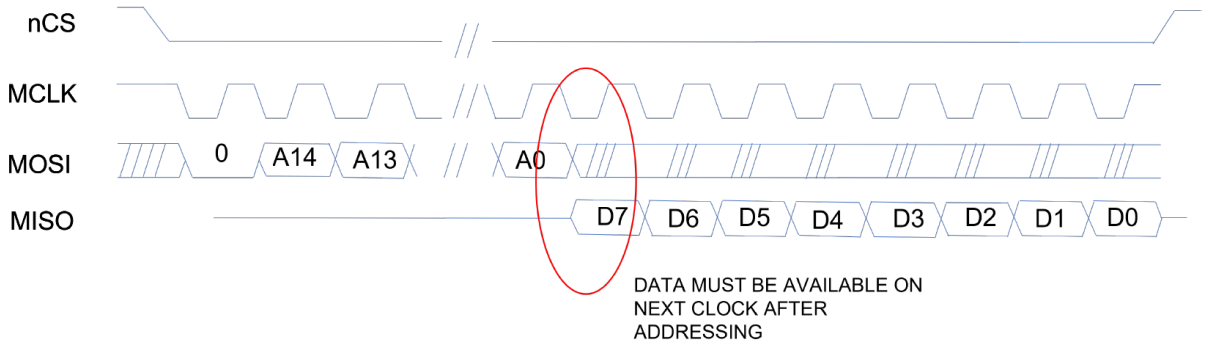
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5.2 SPI read messages

The controller sends the read command to the VL53L8CX. The controller then provides a clock to output the status.

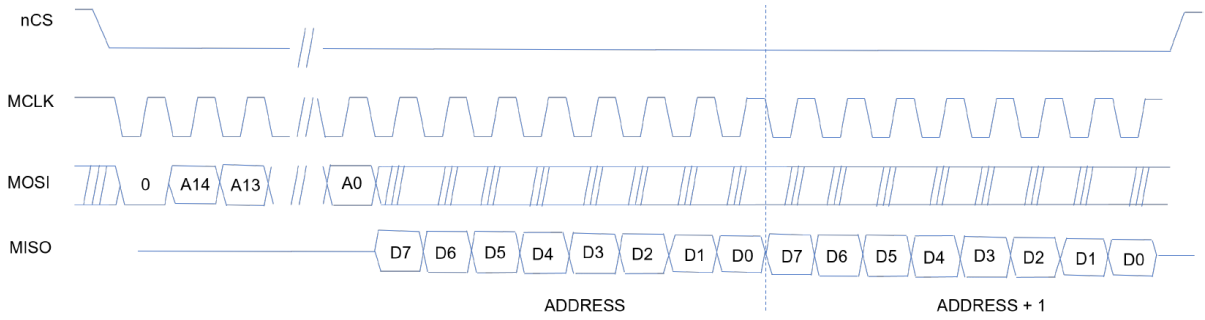
In read mode, the target writes the data to the controller. Transmission is ended by the controller. The reading sequence starts with the first value of the MOSI equal to 0. The most significant bit is sent first (big-endian format). Once the last bit of the address has been received, the device fetches the data internally. The device then presents the data onto the MOSI pin by the next falling MCLK edge (half the MCLK period). This enables the host to sample the data on the following rising edge. Once 8 bits of data have been received, the host sets the NCS high. This terminates the process. More details of the SPI read timing are shown in Figure 19. SPI read timing.

Figure 19. SPI read timing



If the host continues to toggle the MCLK after the last data bit has been read, the target goes into autoincrement read mode. In this mode, the address is automatically incremented by the target, and the read data are transmitted sequentially to the controller on the MISO line. More details of the SPI autoincrement read mode are shown in Figure 20. SPI autoincrement read sequence.

Figure 20. SPI autoincrement read sequence



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6 Electrical characteristics

6.1 Absolute maximum ratings

Table 9. Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
AVDD	-0.5	—	3.47	V
CORE_1V8	-0.5	—	1.98	
IOVDD	-0.5	—	1.98	

Note: Stresses above those listed above may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 Recommended operating conditions

Table 10. Recommended operating conditions

Parameter	Min.	Typ.	Max.	Unit
AVDD supply	3.13	3.3	3.47	V
CORE_1V8 supply	1.62	1.8	1.98	
IOVDD supply with 1.2V configuration	1.08	1.2	1.32	
IOVDD supply with 1.8V configuration	1.62	1.8	1.98	
Ambient temperature (normal operation)	-30	—	85	°C

Note: All three supplies are independent.

Note: When IOVDD is 1.8 V, it is recommended to use the same supply as CORE_1V8.

6.3 Electrostatic discharge (ESD)

The VL53L8CX is compliant with the ESD values presented in Table 11. ESD performance.

Table 11. ESD performance

Parameter	Specification	Conditions
Human body model	JEDEC JS-001-2014	± 2 kV, 1500 Ω, 100 pF
Charged body model	JEDEC JS-001-2014	± 500 V

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6.4 Current consumption

The current consumption values are given in Table 12. Current consumption.

- Typical values quoted are for nominal voltage, process, and temperature (23°C).
- Maximum values are quoted for the worst case conditions (process, voltage, and temperature), unless stated otherwise (85°C)

Table 12. Current consumption

Device state	Average current consumption						Unit
	AVDD		CORE_1V8		IOVDD		
	Typ.	Max.	Typ.	Max.	Typ.	Max.	
LP idle	55	390	0.01	0.5	0.5	2	µA
HP idle	1	1.6	3	17	0.0003	0.002	mA
Active ranging	43	50	50	80	0.003	0.006	

Note: Active ranging is when the device is actively ranging. The current consumption is not affected by a 4x4 or 8x8 zone configuration.

- *CORE_1V8 peak current is the average value +10 mA.*
- *AVDD peak current is the average current +10 mA.*
- *IOVDD peak current is the average value +10 mA.*

Table 13. Example of typical power consumption in continuous mode

Parameter	AVDD 3.3 V IOVDD/CORE_1V8 1.8V	Unit
Continuous mode (4x4 or 8x8 mode)	215	mW

Table 14. Example of typical power consumption in autonomous mode

Parameter	AVDD 3.3 V IOVDD/CORE_1V8 1.8V	Unit
4x4 mode 1 Hz frame rate with 5 ms integration time	1.6	mW
4x4 mode 5 Hz frame rate with 5 ms integration time	12.5	
8x8 mode 1 Hz frame rate with 5 ms integration time	6.7	
8x8 mode 5 Hz frame rate with 5 ms integration time	32.3	

6.5 Digital input and output

Table 15. I²C, SPI, INT, and SYNC summarize the digital I/O electrical characteristics.

Table 15. I²C, SPI, INT, and SYNC

Symbol	Parameter	IOVDD configuration	Min.	Max.	Unit
V^{IL}	Low-level input voltage	1.2/1.8V	-0.3	0.3*IOVDD	V
V^{IH}	High-level input voltage	V1.2/1.8V	0.7*IOVDD	IOVDD + 0.3	
V^{OL}	Low-level output voltage (IOUT = 4 mA)	1.2/1.8V	—	0.2*IOVDD	
V^{OH}	High-level output voltage (IOUT = 4 mA)	1.2/1.8V	0.8*IOVDD	—	

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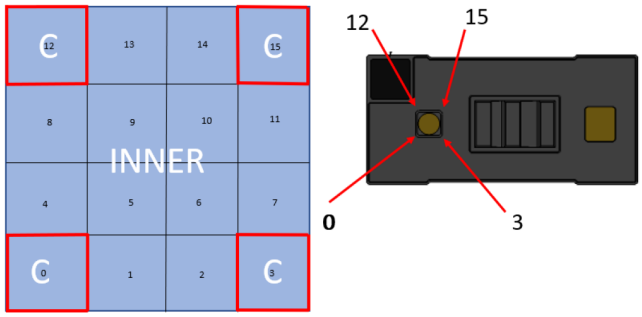
7 Ranging performances

7.1 Zone mapping

7.1.1 Zone mapping 4x4

Figure 21. Zone mapping in 4x4 mode shows the zone definition in 4x4 mode. There are 16 zones in total. They increment along a row first before starting a new row. The physical view is from the device top into the lens. The number of zones, as indicated in Figure 21. Zone mapping in 4x4 mode, corresponds to the zone IDs returned by the sensor.

Figure 21. Zone mapping in 4x4 mode

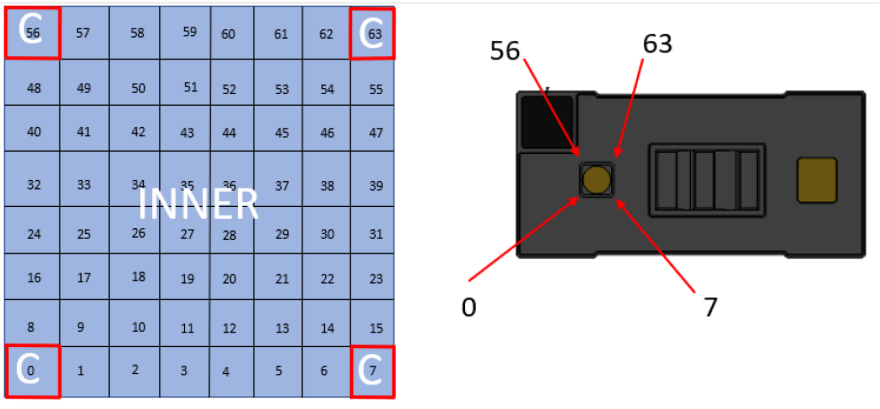


C = Corner zones
INNER = all zones not identified as the corner

7.1.2 Zone mapping 8x8

Figure 22. Zone mapping in 8x8 mode shows the zone definition in 8x8 mode. There are 64 zones in total. They increment along a row first before starting a new row. The physical view is from the device top into the lens. The number of zones, as indicated in Figure 22. Zone mapping in 8x8 mode, correspond to the zone IDs returned by the sensor to the host.

Figure 22. Zone mapping in 8x8 mode

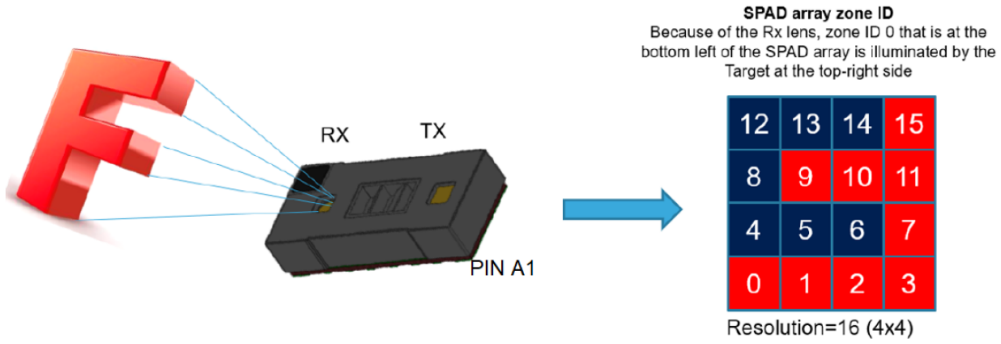


C = Corner zones
INNER = all zones not identified as the corner

7.1.3 Effective zone orientation

The VL53L8CX module includes a lens over the Rx aperture, which flips (horizontally and vertically) the captured image of the target. Consequently, the zone identified as zone 0, in the bottom left of the SPAD array (see Figure 23. Effective orientation), is illuminated by a target. This target is located at the top right-hand side of the scene.

Figure 23. Effective orientation



7.2 Continuous ranging mode

7.2.1 Measurement conditions

The following criteria and test conditions apply to all the characterization results detailed in this section unless specified otherwise:

- The specified target fills 100% of the FoV of the device (in all zones).
- Targets used are Munsell N4.75 (17%), Munsell N8.25 (54%), and Munsell N9.5 (88%).
- AVDD is 3.3 V, IOVDD is 1.8 V, and CORE_1V8 is 1.8 V.
- Nominal ambient temperature is 23°C.
- Maximum range capability is based on a 90% detection rate. (1)
- Range accuracy figures are based on 2.7 sigma. This means that 99.3% of measurements are within the specified accuracy.
- Tests are performed in the dark and at 2 W/m^2 target illumination (940 nm). A 2 W/m^2 target irradiance at 940 nm is equivalent to 5 kLux daylight.
- All tests are performed without cover glasses with a crosstalk margin set to 0 kcps.
- The sensor relies on default calibration data.
- The device is controlled through the API using the default driver settings.

1. *Detection rate is a statistical value indicating the worst case percentage of measurements that return a valid ranging. For example, taking 1000 measurements with a 90% detection rate, gives 900 valid distances. The 100 other distances may be outside the specification, or flagged with an invalid target status.*

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7.2.2 Maximum ranging distance 4x4

Table 16. Maximum ranging capabilities when ranging continuously at 30 Hz shows the maximum ranging capability of the VL53L8CX under different conditions. Refer to Section 7.2.1 Measurement conditions for the general test conditions.

Table 16. Maximum ranging capabilities when ranging continuously at 30 Hz

Target reflectance level. Full FoV (reflectance %)	Zone	Dark	Ambient light (5 kLux)
White target (88%)	Inner	Typical 4000 mm Minimum 4000 mm	Typical 2850 mm Minimum 2850 mm
	Corner	Typical 4000 mm Minimum 4000 mm	Typical 2850 mm Minimum 2700 mm
Light gray target (54%)	Inner	Typical 4000 mm Minimum 4000 mm	Typical 2600 mm Minimum 2550 mm
	Corner	Typical 4000 mm Minimum 4000 mm	Typical 2500 mm Minimum 2400 mm
Gray target (17%)	Inner	Typical 4000 mm Minimum 4000 mm	Typical 1650 mm Minimum 1600 mm
	Corner	Typical 3950 mm Minimum 3900 mm	Typical 1550 mm Minimum 1500 mm

7.2.3 Maximum ranging distance 8x8

Table 17. Maximum ranging capabilities when ranging continuously at 15 Hz shows the maximum ranging capability of the VL53L8CX under different conditions. Refer to Section 7.2.1 Measurement conditions for the general test conditions.

Table 17. Maximum ranging capabilities when ranging continuously at 15 Hz

Target reflectance level. Full FoV (reflectance %)	Zone	Dark	Ambient light (5 kLux)
White target (88%)	Inner	Typical 4000 mm Minimum 4000 mm	Typical 1550 mm Minimum 1100 mm
	Corner	Typical 3950 mm Minimum 2900 mm	Typical 1400 mm Minimum 1100 mm
Light gray target (54%)	Inner	Typical 3300 mm Minimum 2350 mm	Typical 1400 mm Minimum 1000 mm
	Corner	Typical 3100 mm Minimum 2100 mm	Typical 1250 mm Minimum 950 mm
Gray target (17%)	Inner	Typical 2450 mm Minimum 1500 mm	Typical 1150 mm Minimum 900 mm
	Corner	Typical 1950 mm Minimum 1300 mm	Typical 950 mm Minimum 700 mm

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7.2.4 Range accuracy in continuous mode

Figure 24. Range accuracy vs distance illustrates how range accuracy is defined over distance.

Figure 24. Range accuracy vs distance

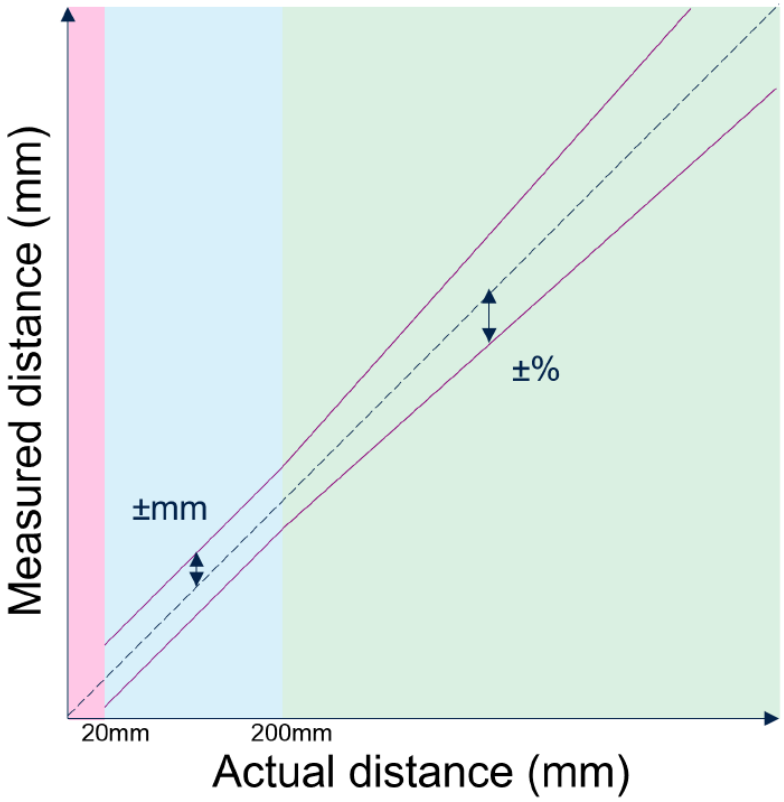


Table 18. Range accuracy in continuous mode

Mode	Distance	Target reflectance	Dark (0 kLux)	Ambient light (5 kLux)
4x4 at 30 Hz	20-200 mm	White target (88%)	±10 mm	±12 mm
		Light gray target (54%)	±9 mm	±11 mm
		Gray target (17%)	±8 mm	±10 mm
	200-4000 mm	White target (88%)	±3%	±4%
		Light gray target (54%)	±4%	±6%
		Gray target (17%)	±4%	±7%
8x8 at 15 Hz	20-200 mm	White target (88%)	±11 mm	±10 mm
		Light gray target (54%)	±12 mm	±13 mm
		Gray target (17%)	±12 mm	±14 mm
	200-4000 mm	White target (88%)	±5%	±5%
		Light gray target (54%)	±5%	±6%
		Gray target (17%)	±5%	±8%

Note: The accuracy of the corner zone data compared to the center 4 zones may degrade by up to 4%.

Note: The accuracy in Table 18. Range accuracy in continuous mode assumes a correctly mounted module. Final assemblies should include additional tolerance for PCB assembly tilt, and mounting of the PCB in a product housing. Typically an additional 1~2%.

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7.3 Autonomous ranging mode

7.3.1 Measurement conditions

The following criteria and test conditions apply to all the characterization results detailed in this section unless specified otherwise:

- The specified target fills 100% of the FoV of the device (in all zones).
- Targets used are Munsell N4.75 (17%), Munsell N8.25 (54%), and Munsell N9.5 (88%).
- AVDD is 3.3 V, IOVDD is 1.8 V, and CORE_1V8 is 1.8 V.
- Nominal ambient temperature is 23°C.
- Maximum range capability is based on a 90% detection rate. (1)
- Range accuracy figures are based on 2.7 sigma. This means that 99.3% of measurements are within the specified accuracy.
- Tests are performed in the dark and at 2 W/m^2 target illumination (940 nm). A 2 W/m^2 target irradiance at 940 nm is equivalent to 5 kLux daylight.
- All tests are performed without cover glasses with a crosstalk margin set to 0 kcps.
- The sensor relies on default calibration data.
- The device is controlled through the API using the default driver settings.

1. *Detection rate is a statistical value indicating the worst case percentage of measurements that return a valid ranging. For example, taking 1000 measurements with a 90% detection rate, gives 900 valid distances. The 100 other distances may be outside the specification, or flagged with an invalid target status.*

7.3.2 Maximum ranging distance 4x4

Table 19. Maximum ranging capabilities when ranging with autonomous mode at 1 Hz – 4x4 – integration time 5 ms shows the maximum ranging capability of the VL53L8CX under different conditions. Refer to Section 7.2.1 Measurement conditions for the general test conditions.

Table 19. Maximum ranging capabilities when ranging with autonomous mode at 1 Hz – 4x4 – integration time 5 ms

Target reflectance level. Full FoV (reflectance %)	Zone	Dark	Ambient light (5 kLux)
White target (88%)	Inner	Typical 4000 mm Minimum 4000 mm	Typical 1550 mm Minimum 1100 mm
	Corner	Typical 4000 mm Minimum 4000 mm	Typical 1400 mm Minimum 1100 mm
Light gray target (54%)	Inner	Typical 4000 mm Minimum 4000 mm	Typical 1450 mm Minimum 1100 mm
	Corner	Typical 3700 mm Minimum 3500 mm	Typical 1300 mm Minimum 1100 mm
Gray target (17%)	Inner	Typical 3000 mm Minimum 3000 mm	Typical 1350 mm Minimum 1100 mm
	Corner	Typical 2550 mm Minimum 2400 mm	Typical 1200 mm Minimum 1000 mm

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7.3.3 Maximum ranging distance 8x8

Table 20. Maximum ranging capabilities when ranging with autonomous mode at 1 Hz – 8x8 – integration time 5 ms shows the maximum ranging capability of the VL53L8CX under different conditions. Refer to Section 7.2.1 Measurement conditions for the general test conditions.

Table 20. Maximum ranging capabilities when ranging with autonomous mode at 1 Hz – 8x8 – integration time 5 ms

Target reflectance level. Full FoV (reflectance %)	Zone	Dark	Ambient light (5 kLux)
White target (88%)	Inner	Typical 3600 mm Minimum 2400 mm	Typical 1250 mm Minimum 1000 mm
	Corner	Typical 2850 mm Minimum 1700 mm	Typical 1150 mm Minimum 800 mm
Light gray target (54%)	Inner	Typical 2600 mm Minimum 1900 mm	Typical 1100 mm Minimum 900 mm
	Corner	Typical 2200 mm Minimum 1350 mm	Typical 1000 mm Minimum 750 mm
Gray target (17%)	Inner	Typical 1400 mm Minimum 1200 mm	Typical 850 mm Minimum 800 mm
	Corner	Typical 1350 mm Minimum 900 mm	Typical 700 mm Minimum 700 mm

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7.3.4 Range accuracy in autonomous mode

Figure 25. Range accuracy vs distance illustrates how range accuracy is defined over distance.

Figure 25. Range accuracy vs distance

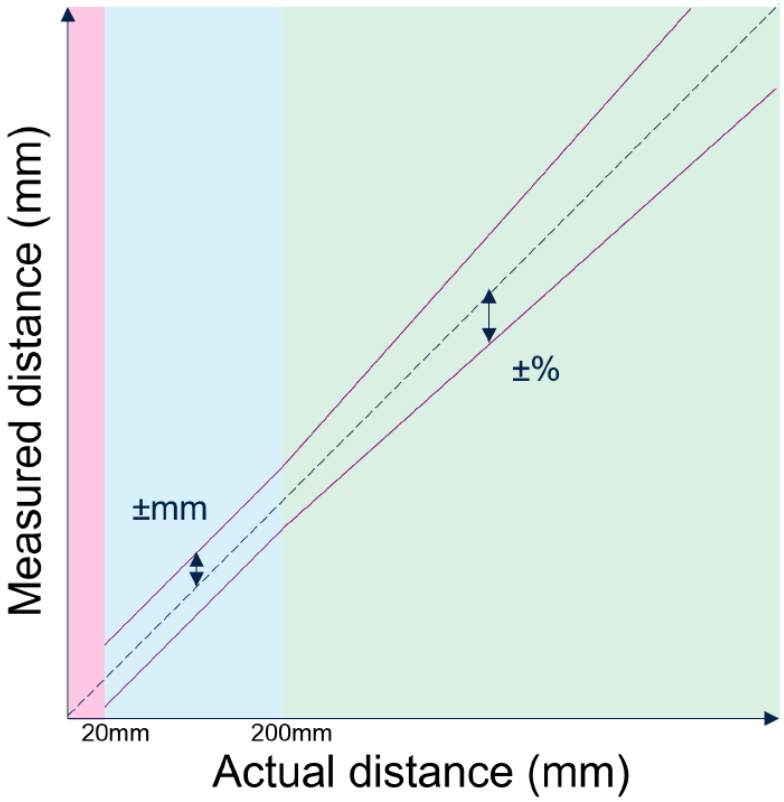


Table 21. Range accuracy in autonomous mode

Mode	Distance	Target reflectance	Dark (0 kLux)	Ambient light (5 kLux)
4x4 at 1 Hz and 5 ms integration time	20-200 mm	White target (88%)	±11 mm	±12 mm
		Light gray target (54%)	±10 mm	±12 mm
		Gray target (17%)	±10 mm	±14 mm
	200-4000 mm	White target (88%)	±3%	±5%
		Light gray target (54%)	±4%	±6%
		Gray target (17%)	±4%	±8%
8x8 at 1 Hz and 5 ms integration time	20-200 mm	White target (88%)	±10 mm	±10 mm
		Light gray target (54%)	±10 mm	±12 mm
		Gray target (17%)	±11 mm	±14 mm
	200-4000 mm	White target (88%)	±5%	±6%
		Light gray target (54%)	±6%	±8%
		Gray target (17%)	±6%	±11%

Note: The accuracy of the corner zone data compared to the center 4 zones may degrade by up to 4%.

Note: The accuracy in Table 21. Range accuracy in autonomous mode assumes a correctly mounted module. Final assemblies should include additional tolerance for a PCB assembly tilt, and mounting of the PCB in a product housing. Typically an additional 1~2%.

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7.4 Range offset drift over temperature

Self-heating or a change in ambient temperature increases silicon temperature. This results in a range offset drift. This may be minimized by performing a periodic autocalibration, resulting in a typical drift of 0.1 mm/°C.

The autocalibration is done automatically when a new ranging session is started. A stop/start of the device is required if the device is already streaming.

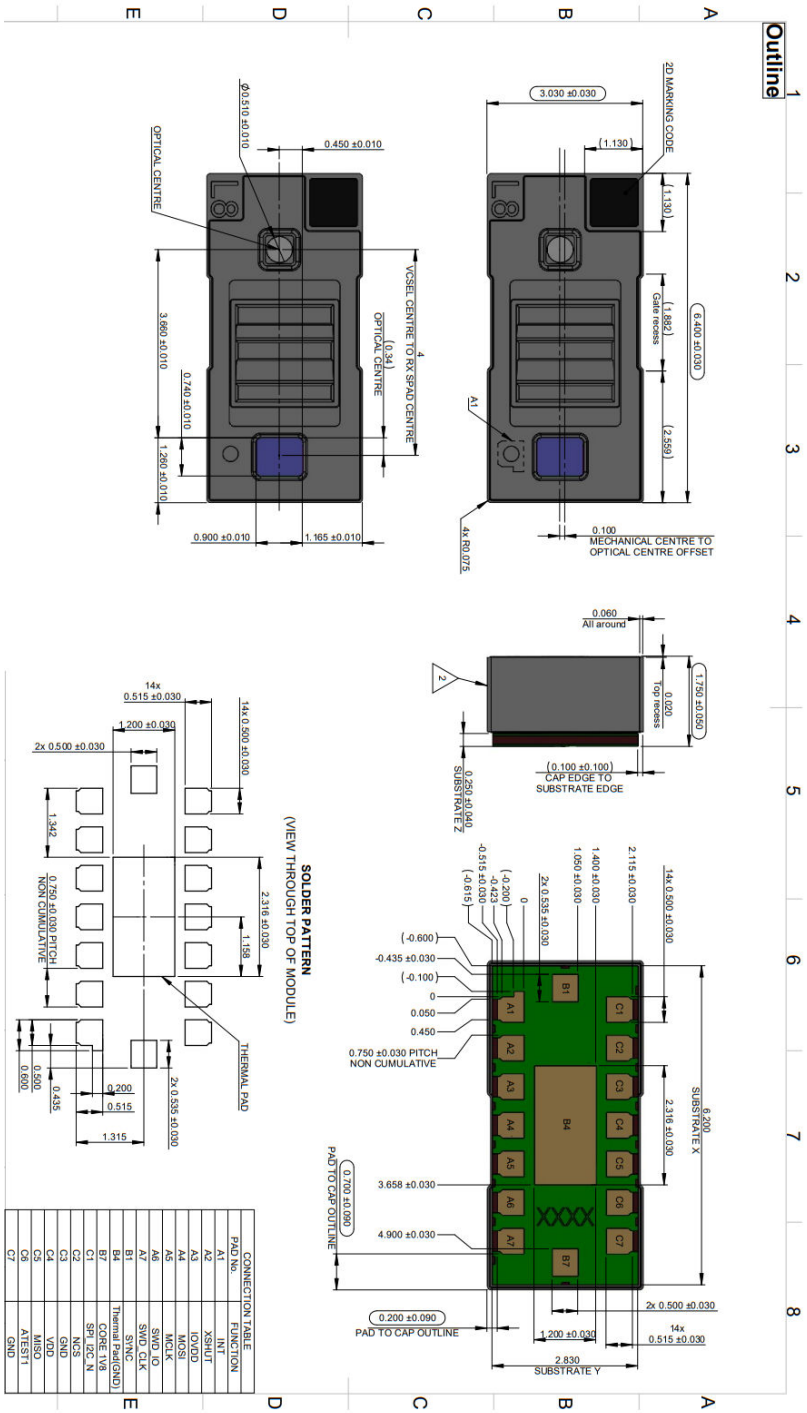
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8 Outline drawings

The figures below give details of the VL53L8CX module. All values are given in millimetres.

STMicroelectronics delivers either of these dual-source cap assemblies to the customer since the pad and substrate design are identical for both versions. This is because the pad and substrate design are identical for both versions, and have no impact on the customer PCB design. Ranging performances, reflow, and technical parameters are identical for all module designs presented below.

Figure 26. Outline drawing (1/3)



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Note: A thermal pad is required on the application board for thermal dissipation purpose. For more information, refer to AN5897.

Note: For more information, refer to the pin description in Section 2.5 Device pinout.

Figure 27. Outline drawing (2/3) - module with liner

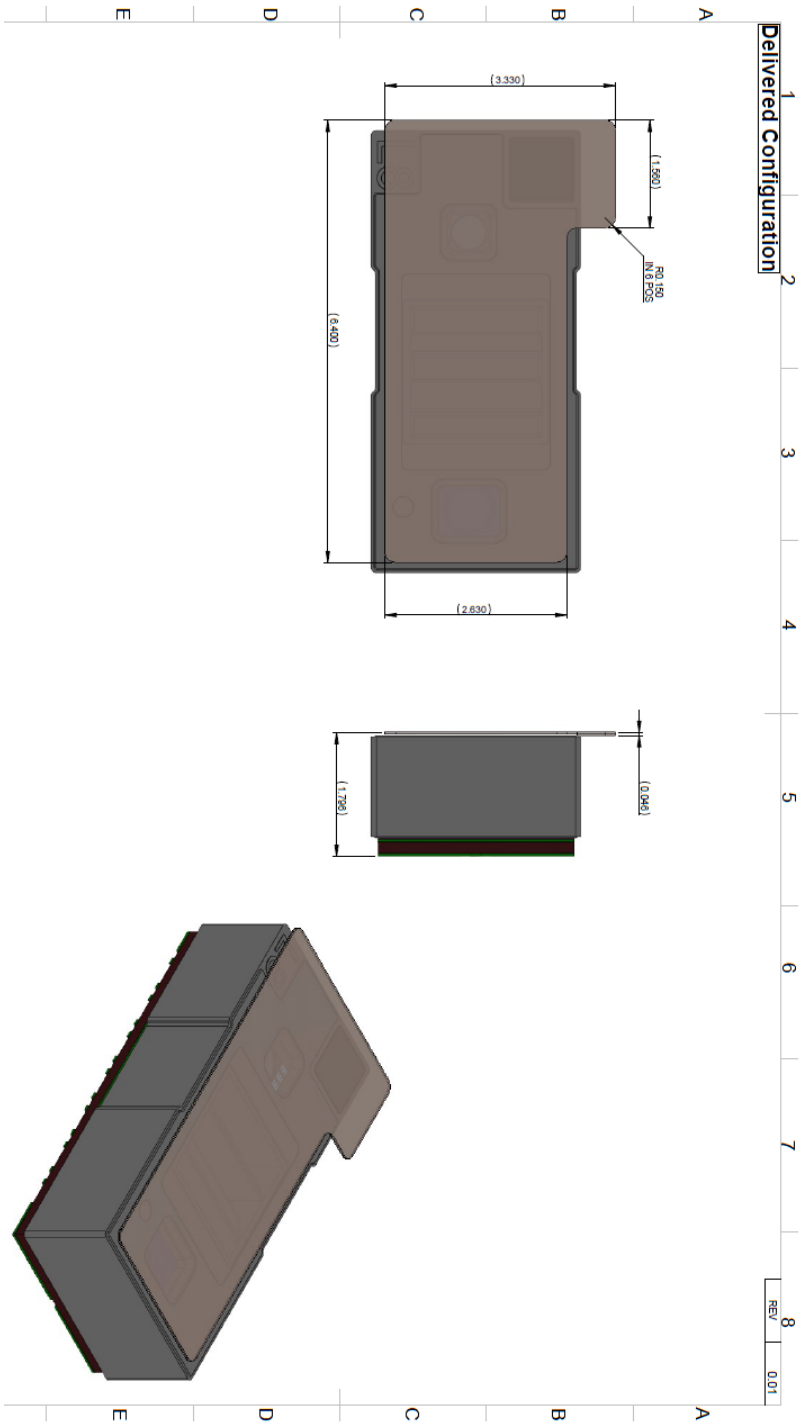
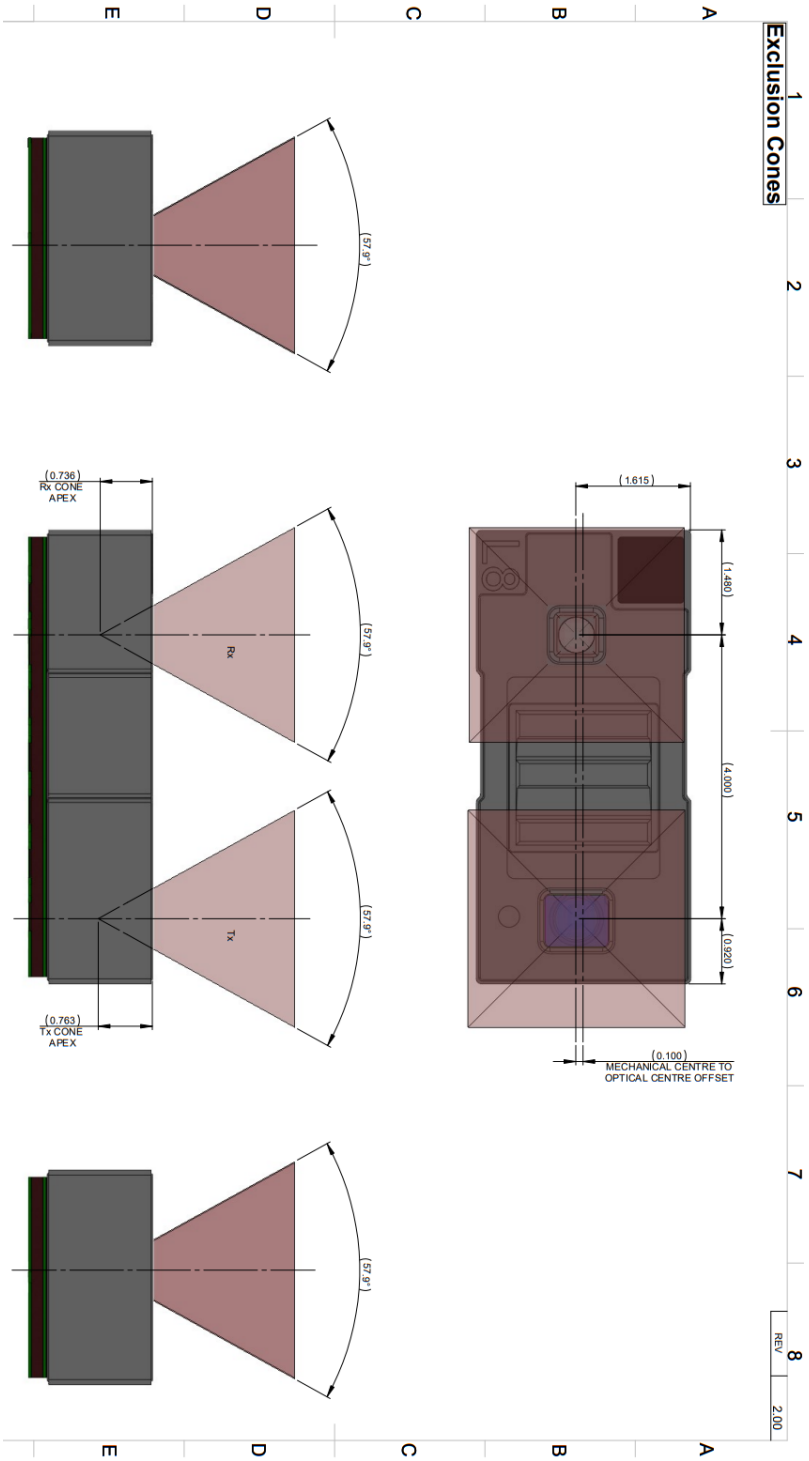


Figure 28. **Outline drawing (3/3) - optical exclusion zones**



9 Laser safety considerations

The VL53L8CX contains a laser emitter and corresponding drive circuitry. The laser output is designed to meet Class 1 laser safety limits under all reasonably foreseeable conditions including single faults in compliance with IEC 60825-1:2014.

Do not increase the laser output power by any means. Do not use any optics to focus the laser beam.

Caution: Use of controls or adjustments, or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Figure 29. Class 1 laser label



The VL53L8CX complies with:

- IEC 60825-1:2014
- 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1:2014 as described in Laser Notice No.56, dated May 8, 2019
- EN 60825-1:2014 including EN 60825-1:2014/A11:2021,
- EN 50689:2021 except for the requirement of clause 5 from EN50689 regarding Child Appealing Products. If designing a Child Appealing Product, please contact ST Technical Application Support.

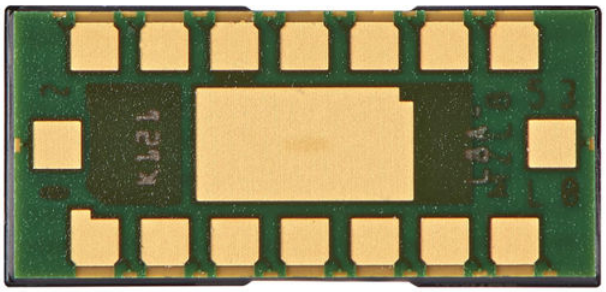
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10 Packaging and labeling

10.1 Product marking

See the figure below for the product marking area. The marking is L8A-

Figure 30. Product marking area



A 2D product marking code is applied on the corner of the module cap as shown in Figure 31. 2D marking product code.

Note: The 2D marking code aligns with pin C7 of the module and is not an indicator of pin 1.

Figure 31. 2D marking product code



10.2 Inner box labeling

The labeling follows the Microelectronics' standard packing acceptance specification. The following information is on the inner box label:

- Assembly site
- Sales type
- Quantity
- Trace code
- Marking
- Bulk ID number

10.3 Packing

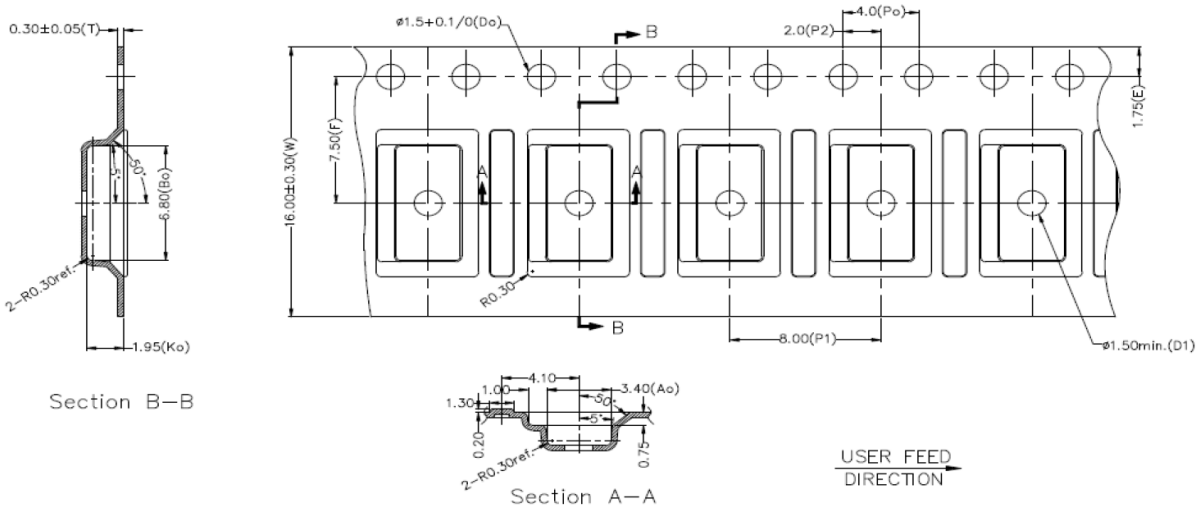
At customer/subcontractor level, it is recommended to mount the VL53L8CX in a clean environment. To help avoid any foreign material contamination at final assembly level, the modules are shipped in a tape and reel format with a protective liner. The liner is compliant with reflow at 260°C (as per JEDEC-STD-020E).

Note: The liner must be removed during assembly of the customer device, just before mounting the cover glass.

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10.4 Tape outline drawing

Figure 32. **VL53L8CX tape and reel packaging drawing**



10.5 Pb-free solder reflow process

Table 22. Recommended solder profile and Figure 33. Solder profile show the recommended and maximum values for the solder profile.

Customers have to tune the reflow profile depending on the PCB, solder paste, and material used. We expect customers to follow the “recommended” reflow profile, which is specifically tuned for the VL53L8CX package.

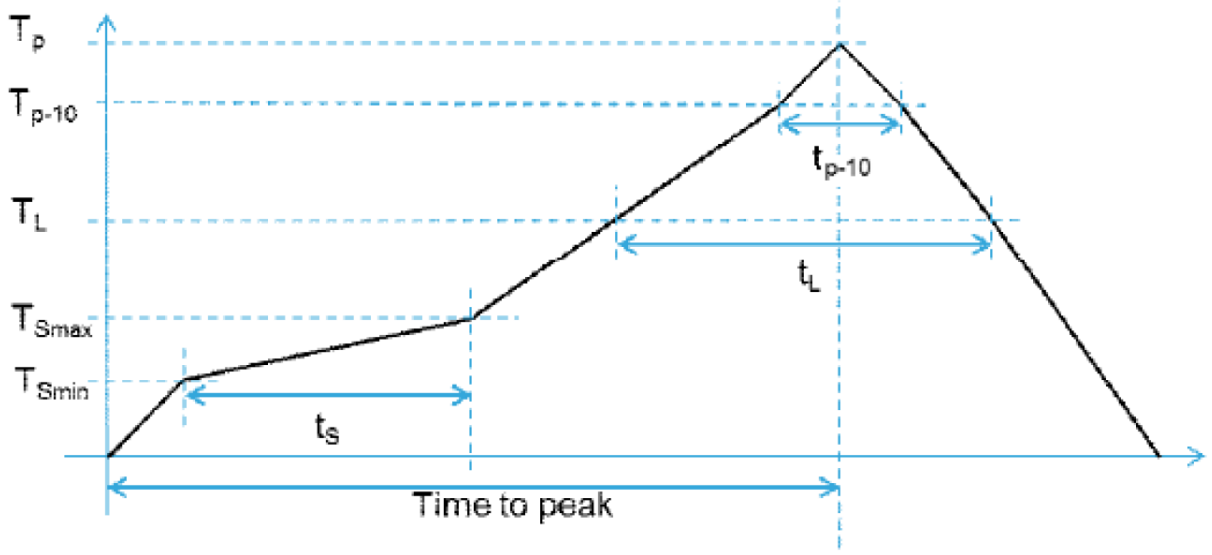
For any reason, if a customer must perform a reflow profile, which is different from the “recommended” one (especially where the peak temperature is > 240°C), the new profile must be qualified by the customer at their own risk. The profile has to be within the “maximum” profile limit described in Table 22. Recommended solder profile.

Table 22. **Recommended solder profile**

Parameters	Recommended	Maximum	Units
Minimum temperature (T_S min)	130	150	°C
Maximum temperature (T_S max)	200	200	°C
Time t_s (T_S min to T_S max)	90-110	60-120	s
Temperature (T_L)	217	217	°C
Time (t_L)	55-65	55-65	s
Ramp up	2	3	°C/s
Temperature (T_{p-10})	—	235	°C
Time (t_{p-10})	—	10	s
Ramp up	—	3	°C/s
Peak temperature (T_p)	240	260	°C
Time to peak	300	300	s
Ramp down (peak to T_L)	-4	-6	°C/s

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Figure 33. **Solder profile**



Note: The component should be limited to a maximum of three passes through this solder profile.

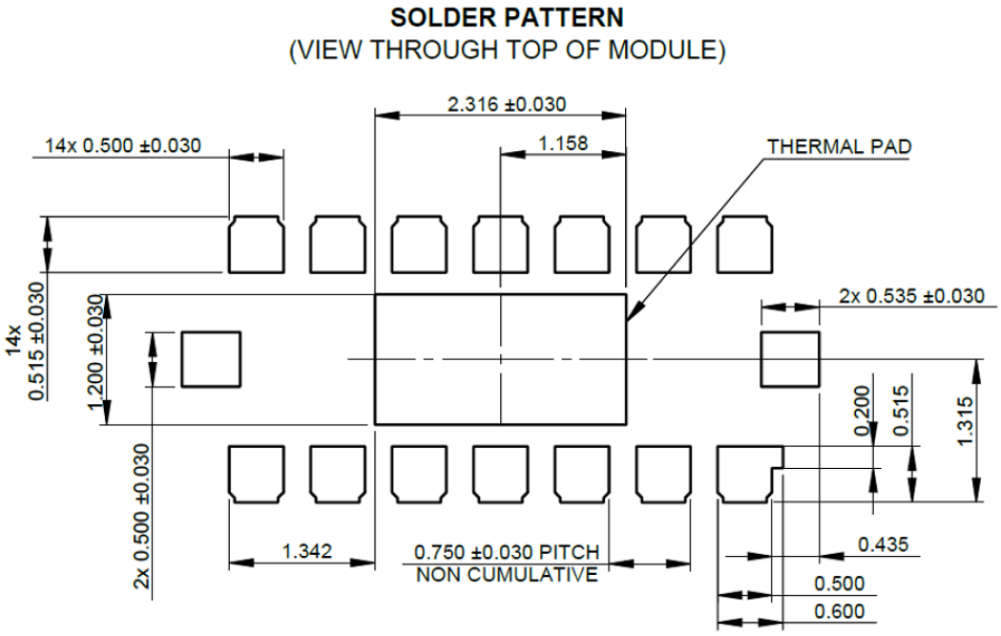
Note: As the VL53L8CX package is not sealed, only a dry reflow process should be used (such as convection reflow). Vapor phase reflow is not suitable for this type of optical component.

Note: The VL53L8CX is an optical component and as such, it should be treated carefully. This typically includes using a 'no-wash' assembly process.

10.6 Handling and storage precautions

10.6.1 Recommended solder pad dimensions

Figure 34. **Recommended solder pattern**



10.6.2 Shock precautions

Sensor modules house numerous internal components that are susceptible to shock damage. If a unit is subject to excessive shock, is dropped on the floor, or a tray/reel of units is dropped on the floor, it must be rejected, even if no apparent damage is visible.

10.6.3 Part handling

Handling must be done with nonmarring ESD safe carbon, plastic, or teflon tweezers. Ranging modules are susceptible to damage or contamination. The customer is advised to use a clean assembly process until a protective cover glass is mounted.

10.6.4 Compression force

A maximum compressive load of 25 N should be applied on the module.

10.6.5 Moisture sensitivity level

Moisture sensitivity is level 3 (MSL) as described in IPC/JEDEC JSTD-020-C.

Note: If devices are stored out of the packaging for greater than 168 h, the devices should be baked before use. The optimum bake recommended is at 90°C for a minimum of 6 hours.

10.7 Storage temperature conditions

Table 23. Recommended storage conditions

Parameter	Min.	Typ.	Max.	Unit
Temperature (storage)	-40	23	90	°C

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11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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12 Ordering information

The VL53L8CX is currently available in the format below. More detailed information is available on request.

Table 24. Order codes

Order codes	Package	Packing	Minimum order quantity
VL53L8CXV0GC/1	Optical LGA16 with liner	Tape and reel	3600 pcs

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Revision history

Table 25. **Document revision history**

Date	Version	Changes
22-Dec-2022	1	Initial release
16-Mar-2023	2	Updated Section 9 Laser safety considerations Updated Section 10.1 Product marking
27-Apr-2023	3	Modified SPI maximum value to 3 MHz in Features, Table 1. Technical specifications and Table 8. SPI interface timing specification. Updated Figure 6. Typical application schematic for SPI
05-Jun-2023	4	Modified terms master/slave to controller/target, MOSI: main output secondary input, and MISO: main input secondary output. Added a + before average value 10 mA Section 6.4 Current consumption.
21-Jun-2023	5	Table 24. Order codes: the optical package LGA16 is available with the liner (not without it).
27-Jul-2023	6	Updated Figure 6. Typical application schematic for SPI.
08-Aug-2023	7	Updated signal descriptions for C1 and C2 pins in Table 3. VL53L8CX pin description for I²C and SPI configuration.

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