MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1G BIT (128M × 8 BIT) CMOS NAND E^{2}PROM

DESCRIPTION

The TC58NVG0S3HBAI4 is a single 3.3V 1Gbit (1,140,850,688bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^{2}PROM) organized as (2048 + 128) bytes × 64 pages × 1024 blocks. The device has a 2176-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 2176-byte increments. The Erase operation is implemented in a single block unit (128 Kbytes + 8 Kbytes: 2176 bytes × 64 pages).

The TC58NVG0S3HBAI4 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed, making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization

	x8
Memory cell array	2176 × 64K × 8
Register	2176 × 8
Page size	2176 bytes
Block size	(128K + 8K) bytes

- Modes
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy

- Mode control
  Serial input/output
  Command control

- Number of valid blocks
  Min 1004 blocks
  Max 1024 blocks

- Power supply
  V_{CC} = 2.7V to 3.6V

- Access time

Cell array to register	25 μs max
Read Cycle Time	25 ns min (C_L=50pF)

- Program/Erase time

Auto Page Program	300 μs/page typ.
Auto Block Erase	2.5 ms/block typ.

- Operating current

Read (25 ns cycle)	30 mA max
Program (avg.)	30 mA max
Erase (avg.)	30 mA max
Standby	50 μA max

- Package
  P-TFBGA63-0911-0.80CZ (Weight: 0.15 g typ.)

- 8 bit ECC for each 512Byte is required.

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PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			$\overline{WP}$	ALE	V_{SS}	$\overline{CE}$	$\overline{WE}$	RY/$\overline{BY}$		
D			NC	$\overline{RE}$	CLE	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	NC	NC	NC	NC	NC		
G			NC	NC	NC	NC	NC	NC		
H			NC	I/O1	NC	NC	NC	V_{CC}		
J			NC	I/O2	NC	V_{CC}	I/O6	I/O8		
K			V_{SS}	I/O3	I/O4	I/O5	I/O7	V_{SS}		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

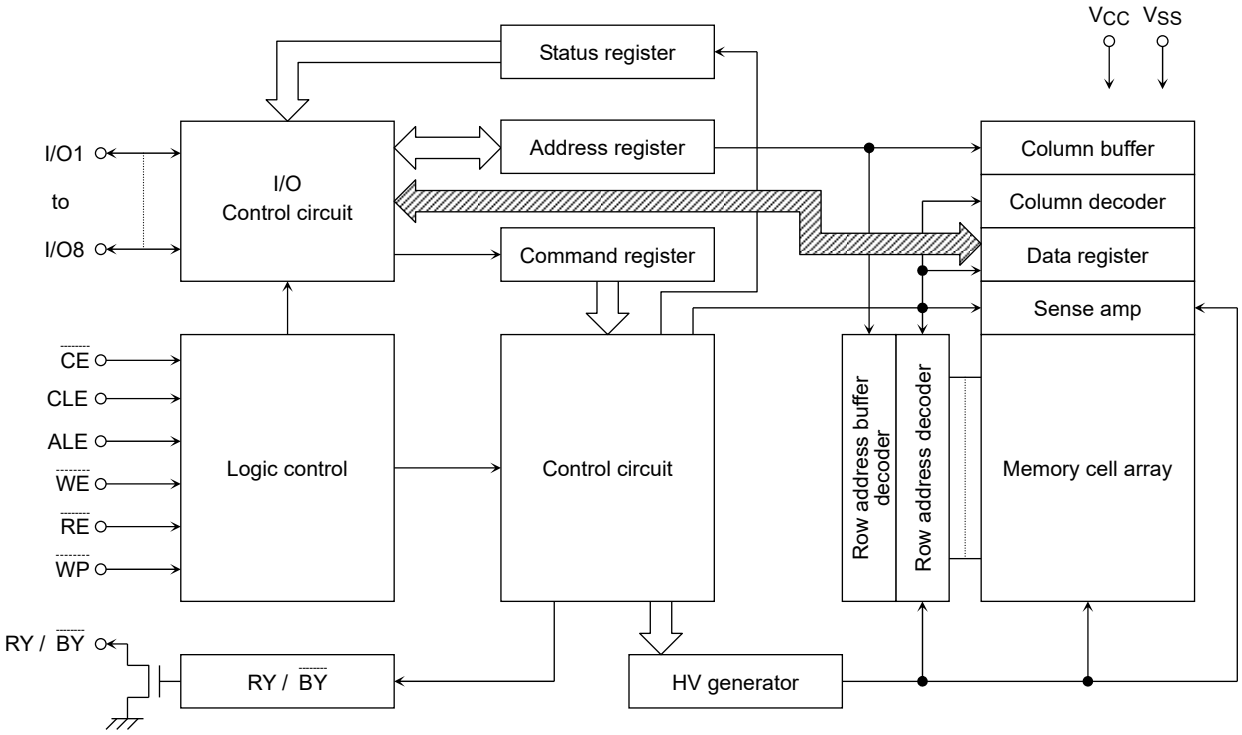
PIN NAMES

I/O1 to I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY / $\overline{BY}$	Ready/Busy
V_{CC}	Power supply
V_{SS}	Ground
NC	No Connection

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input / Output Voltage	−0.6 to V_{CC} + 0.3 (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{STG}	Storage Temperature	−55 to 125	°C
T_{OPR}	Operating Temperature	-40 to 85	°C

Note: Avoid locations where the device may be exposed to water (wet, rain, dew condensation, etc.)

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

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VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	1004	—	1024	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over lifetime.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	—	3.6	V
V_{IH}	High Level Input Voltage	V_{CC} x 0.8	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	−0.3*	—	V_{CC} x 0.2	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = -40 to 85°C, V_{CC} = 2.7 to 3.6V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO1}	Serial Read Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, t_{RC} = 25 ns	—	—	30	mA
I_{CCO2}	Programming Current	—	—	—	30	mA
I_{CCO3}	Erasing Current	—	—	—	30	mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2 V, $\overline{WP}$ = 0 V/V_{CC}	—	—	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = −0.1 mA	V_{CC} − 0.2	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1 mA	—	—	0.2	V
I_{OL} (RY / $\overline{BY}$)	Output Current of RY / $\overline{BY}$ pin	V_{OL} = 0.2 V	—	4	—	mA

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AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = -40 to 85°C, V_{CC} = 2.7 to 3.6V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CLS}	CLE Setup Time	12	—	ns
t_{CLH}	CLE Hold Time	5	—	ns
t_{CS}	$\overline{CE}$ Setup Time	20	—	ns
t_{CH}	$\overline{CE}$ Hold Time	5	—	ns
t_{WP}	Write Pulse Width	12	—	ns
t_{ALS}	ALE Setup Time	12	—	ns
t_{ALH}	ALE Hold Time	5	—	ns
t_{DS}	Data Setup Time	12	—	ns
t_{DH}	Data Hold Time	5	—	ns
t_{WC}	Write Cycle Time	25	—	ns
t_{WH}	$\overline{WE}$ High Hold Time	10	—	ns
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns
t_{RW}	Ready to $\overline{WE}$ Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	12	—	ns
t_{RC}	Read Cycle Time	25	—	ns
t_{REA}	$\overline{RE}$ Access Time	—	20	ns
t_{CEA}	$\overline{CE}$ Access Time	—	25	ns
t_{CLR}	CLE Low to $\overline{RE}$ Low	10	—	ns
t_{AR}	ALE Low to $\overline{RE}$ Low	10	—	ns
t_{RHOH}	$\overline{RE}$ High to Output Hold Time	25	—	ns
t_{RLOH}	$\overline{RE}$ Low to Output Hold Time	5	—	ns
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	60	ns
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns
t_{CSD}	$\overline{CE}$ High to ALE or CLE Don't Care	0	—	ns
t_{REH}	$\overline{RE}$ High Hold Time	10	—	ns
t_{IR}	Output-High-Impedance-to-$\overline{RE}$ Falling Edge	0	—	ns
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	60	—	ns
t_{WB}	$\overline{WE}$ High to Busy	—	100	ns
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	5/5/10/500	μs

*1: tCLS and tALS cannot be shorter than tWP

*2: tCS should be longer than tWP + 8ns

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AC TEST CONDITIONS

PARAMETER	CONDITION
	V_{CC}: 2.7 to 3.6V
Input level	V_{CC} – 0.2 V, 0.2 V
Input pulse rise and fall time	3 ns
Input comparison level	V_{CC} / 2
Output data comparison level	V_{CC} / 2
Output load	C_L (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY / $\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document)

PROGRAMMING / ERASING / READING CHARACTERISTICS
(Ta = -40 to 85°C, V_{CC} = 2.7 to 3.6V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Programming Time	—	300	700	μs	
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)	—	—	700	μs	(2)
N	Number of Partial Program Cycles in the Same Page	—	—	4		(1)
t_{BERASE}	Block Erasing Time	—	2.5	5	ms	
t_R	Memory Cell Array to Starting Address	—	—	25	μs	
$t_{DCBSYR1}$	Data Cache Busy in Read Cache (following 31h and 3Fh)	—	—	25	μs	
$t_{DCBSYR2}$	Data Cache Busy in Page Copy (following 3Ah)	—	—	30	μs	

(1) Refer to Application Note (12) toward the end of this document.

(2) $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

Data Output

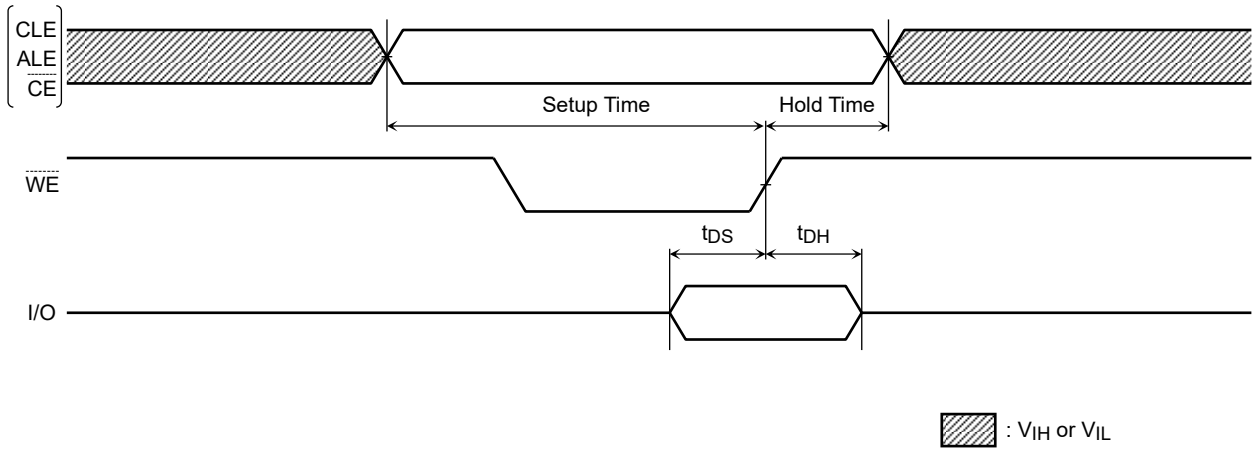
When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depends on tRHOH (25ns MIN). Under this condition, the waveforms look like Normal Serial Read Mode.
When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depends on tRLOH (5ns MIN). Under this condition, output buffers are disabled by the rising edge of CLE, ALE, /CE or the falling edge of /WE, and waveforms look like Extended Data Output Mode.

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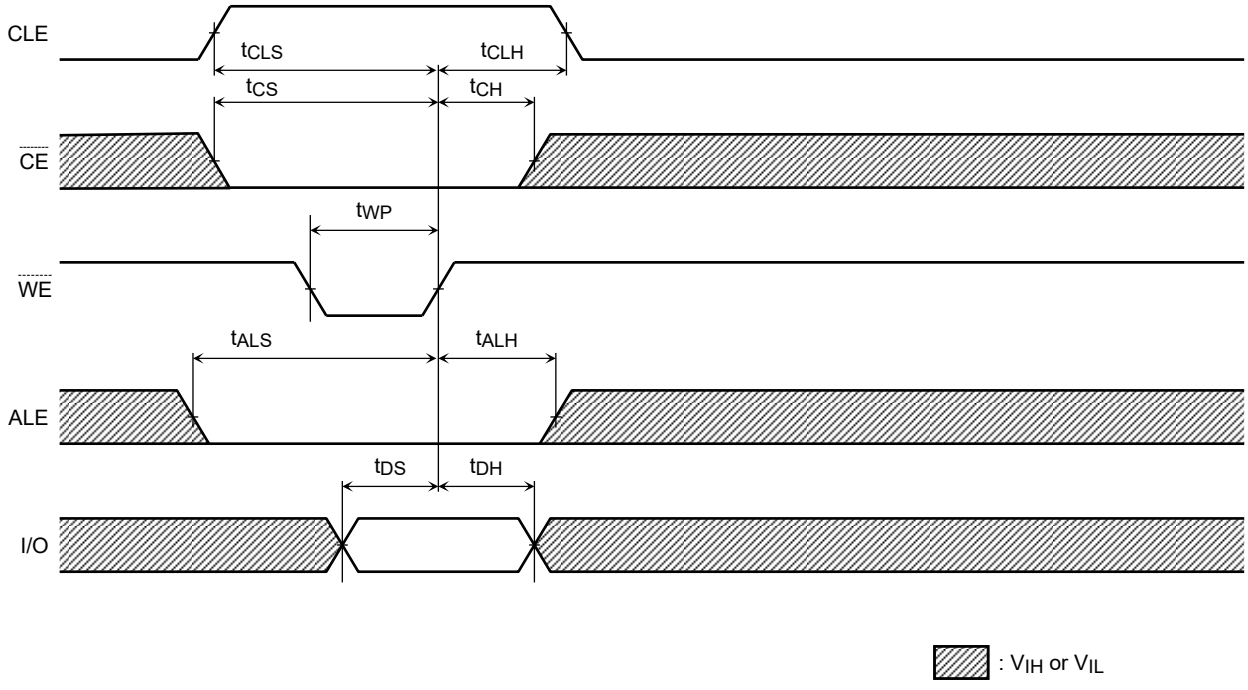
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TIMING DIAGRAMS

Latch Timing Diagram for Command/Address/Data



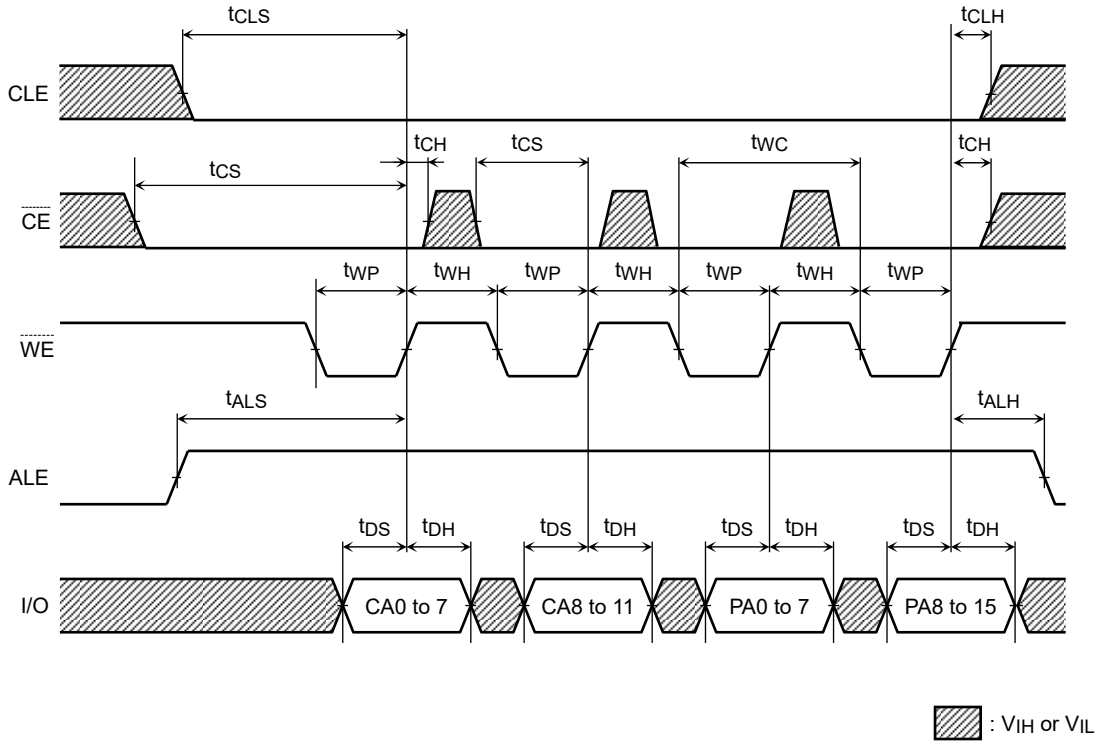
Command Input Cycle Timing Diagram



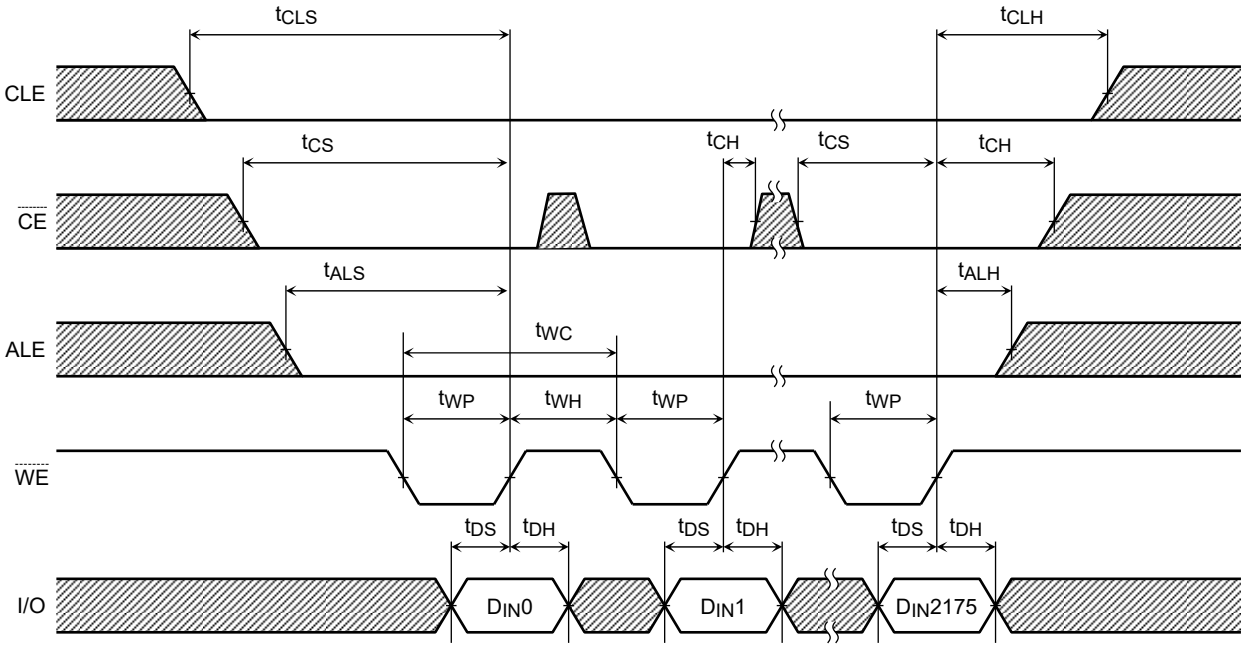
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Address Input Cycle Timing Diagram



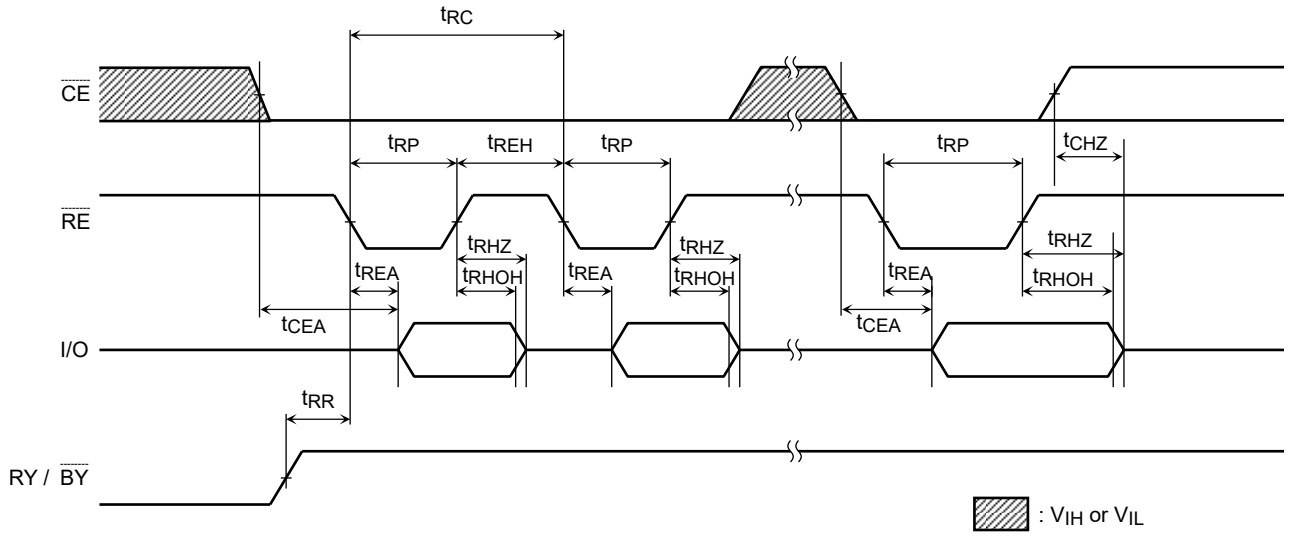
Data Input Cycle Timing Diagram



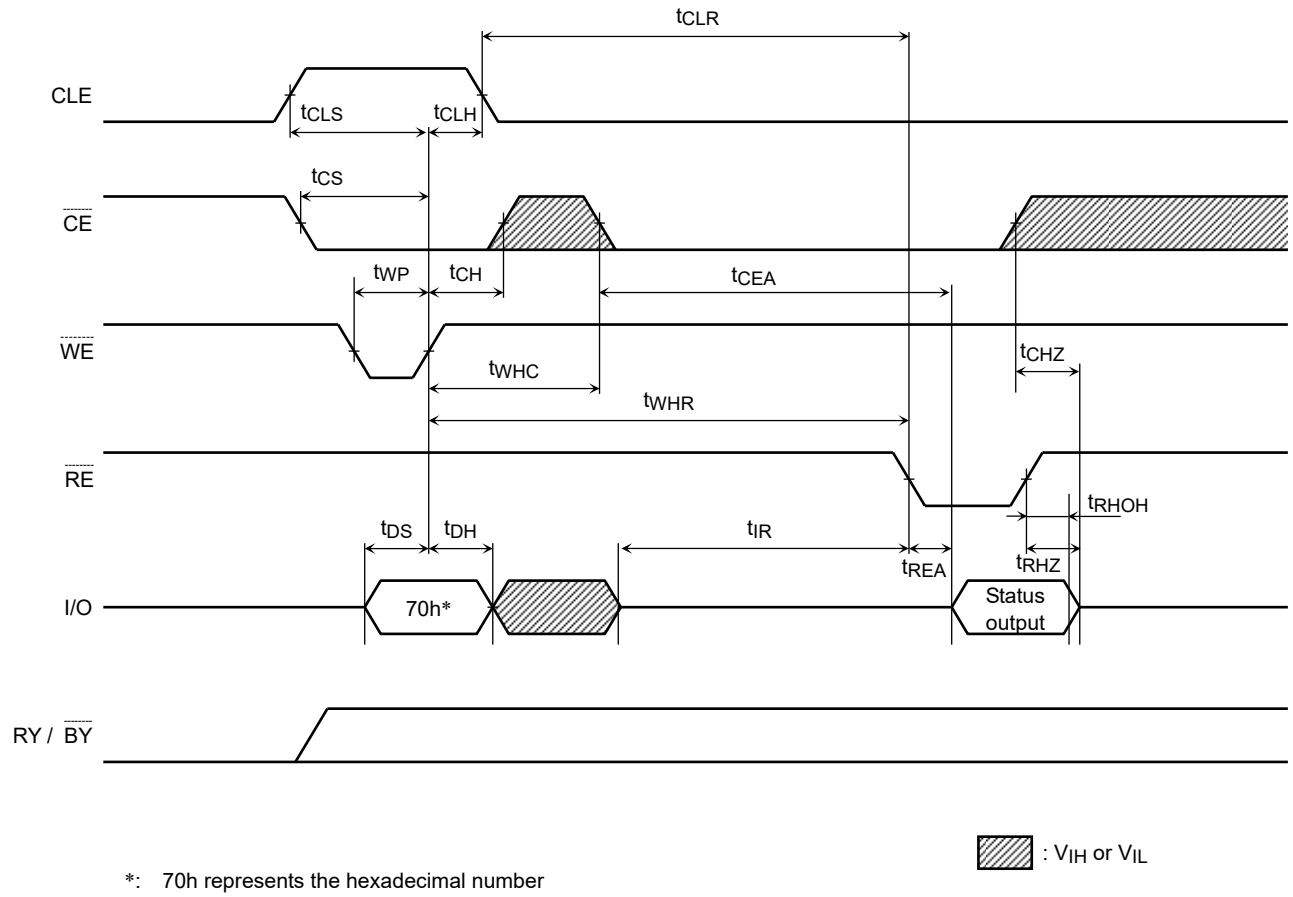
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Serial Read Cycle Timing Diagram



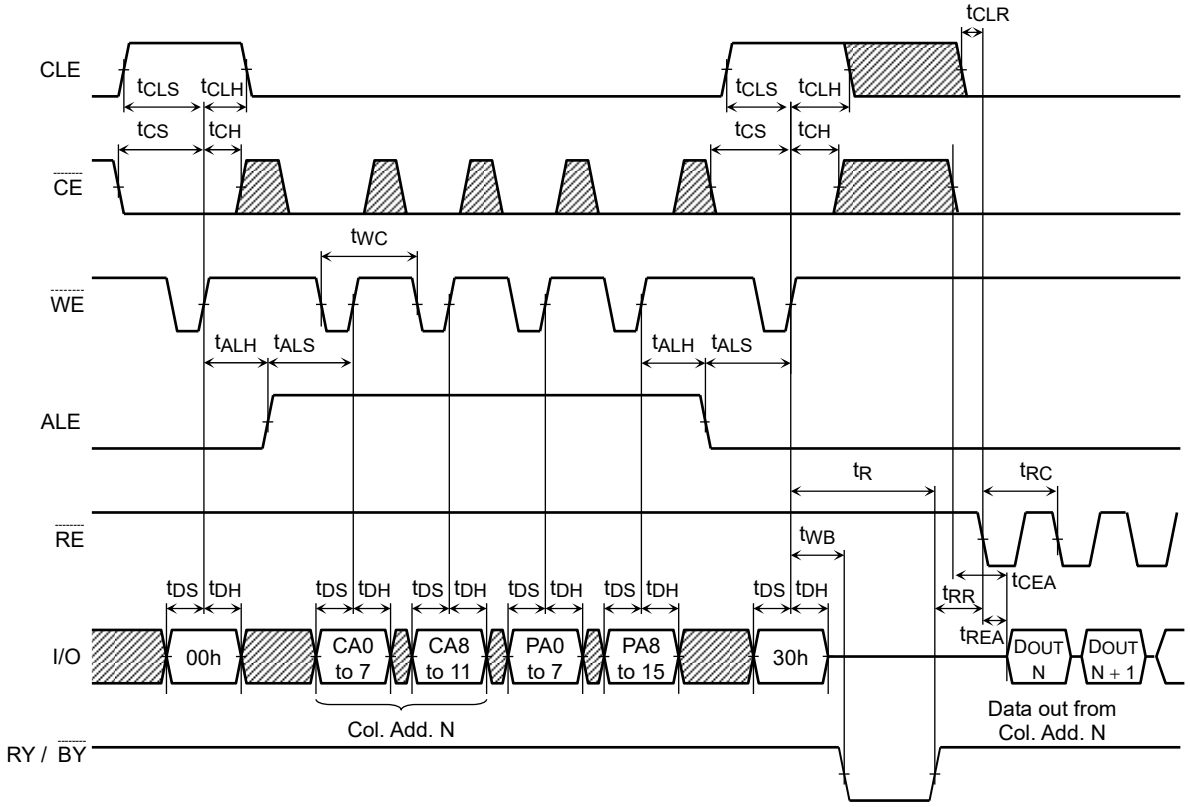
Status Read Cycle Timing Diagram



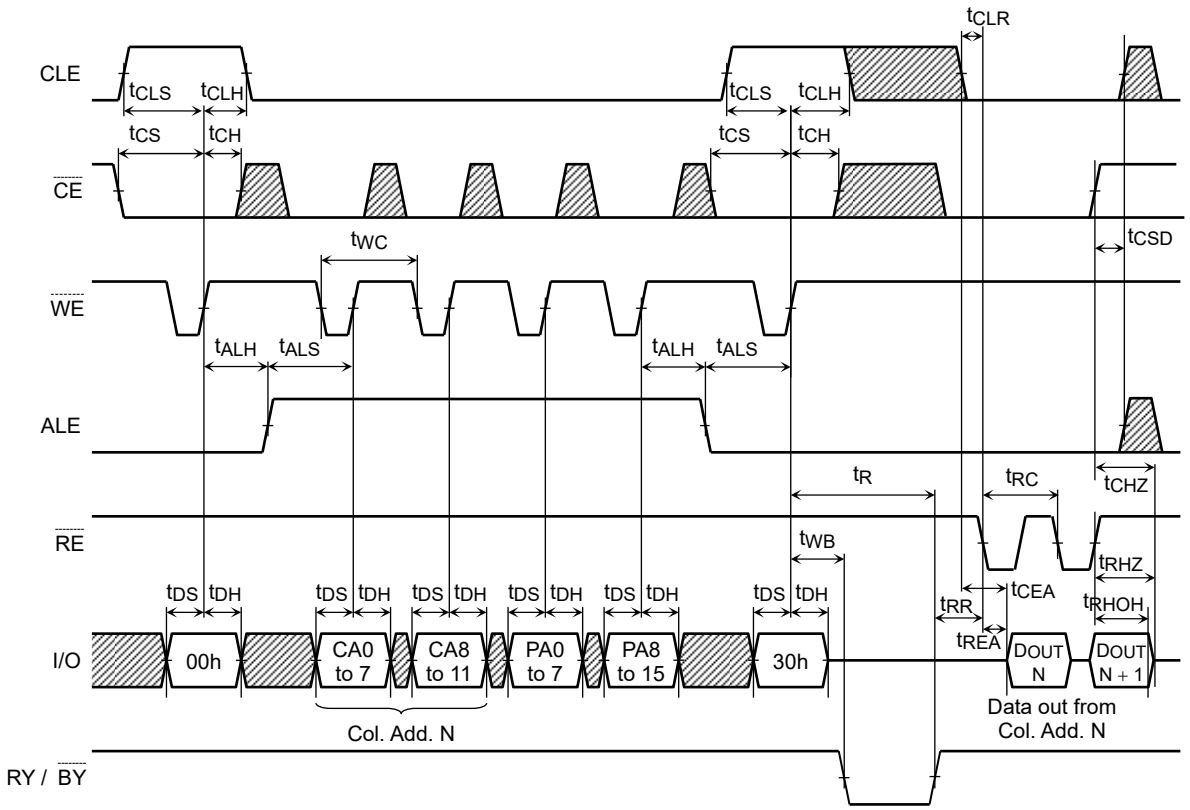
*: 70h represents the hexadecimal number

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Read Cycle Timing Diagram



Read Cycle Timing Diagram: When Interrupted by $\overline{CE}$

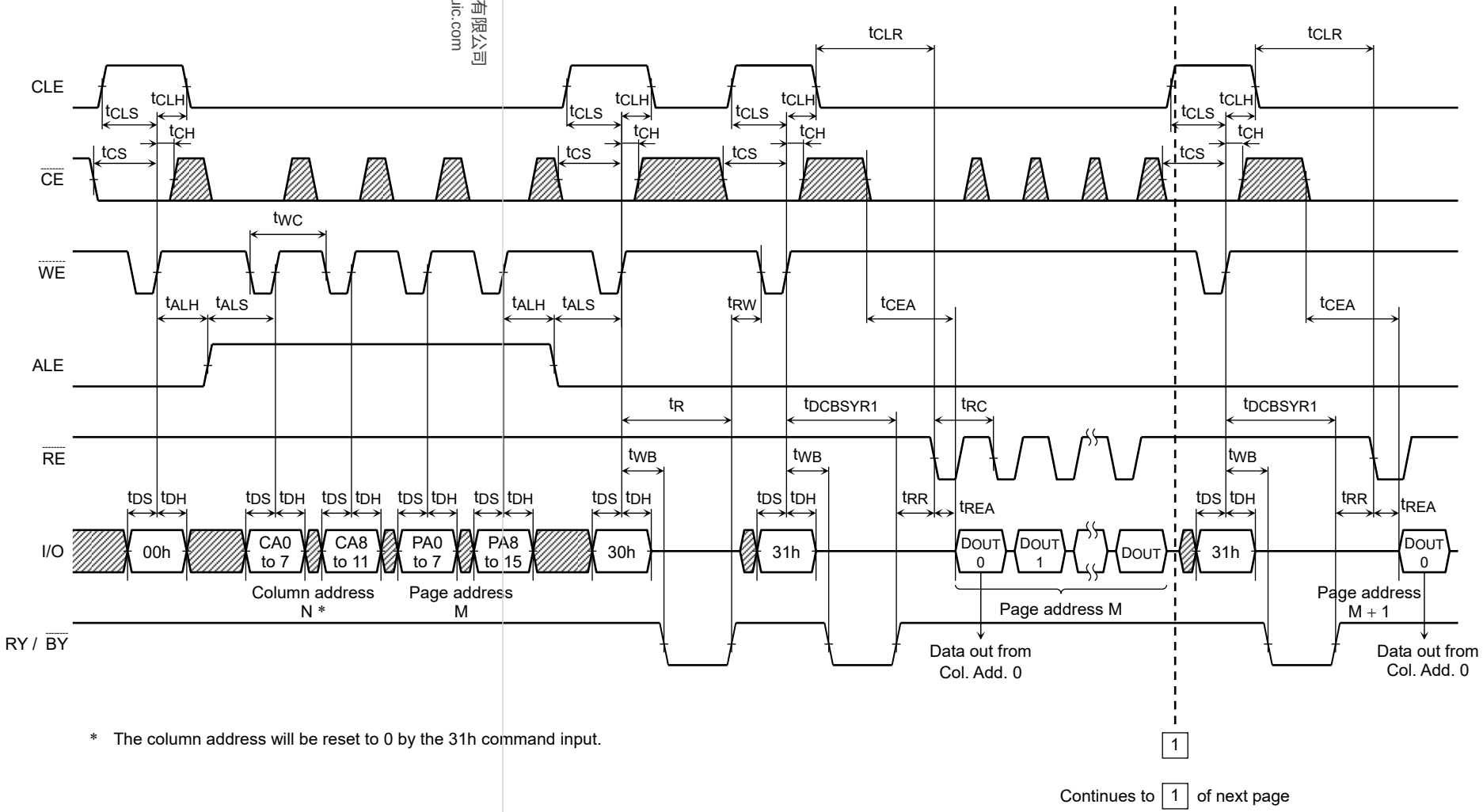


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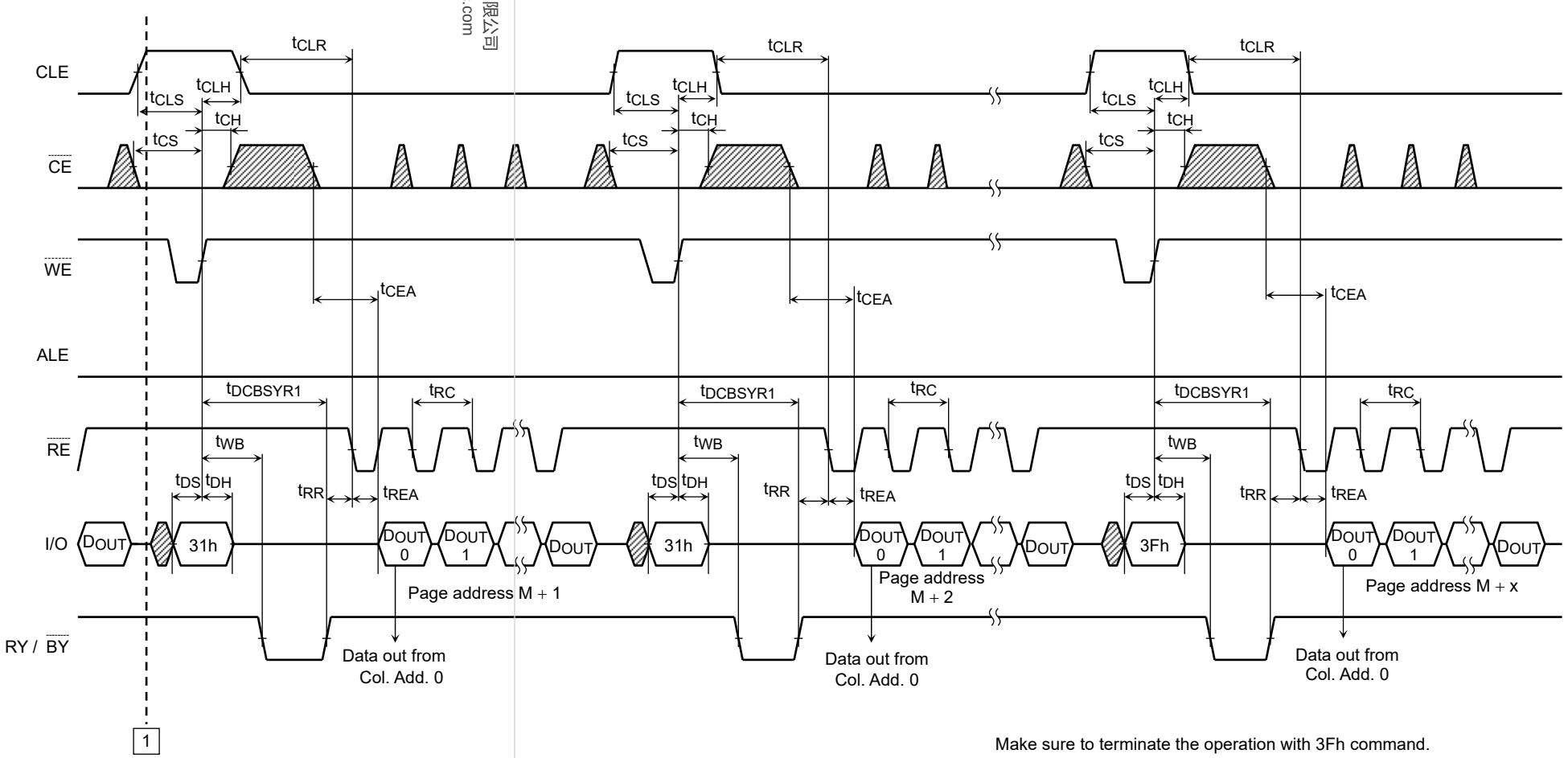
Read Cycle with Data Cache Timing Diagram (2/2)



* The column address will be reset to 0 by the 31h command input.

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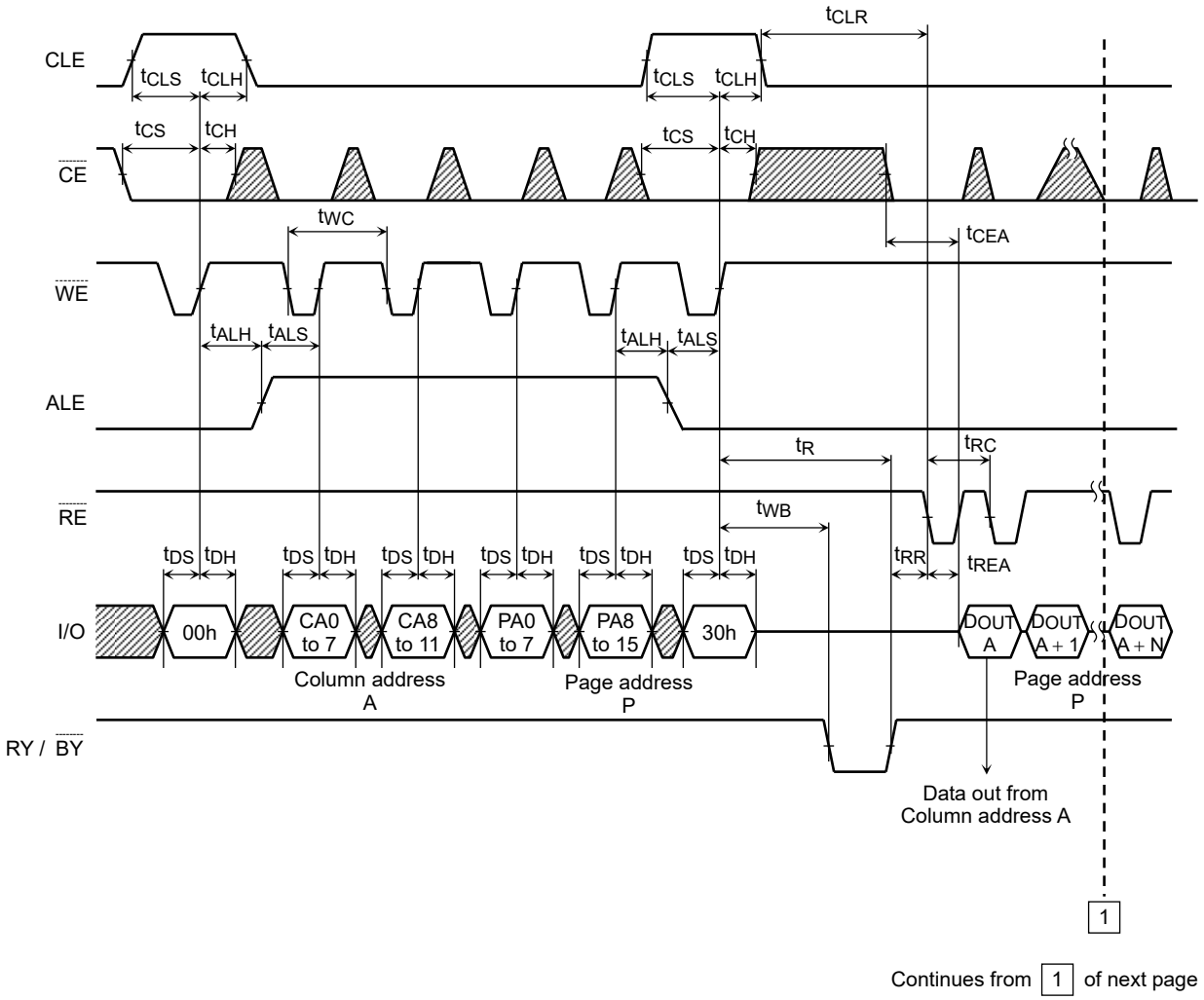
Read Cycle with Data Cache Timing Diagram (2/2)



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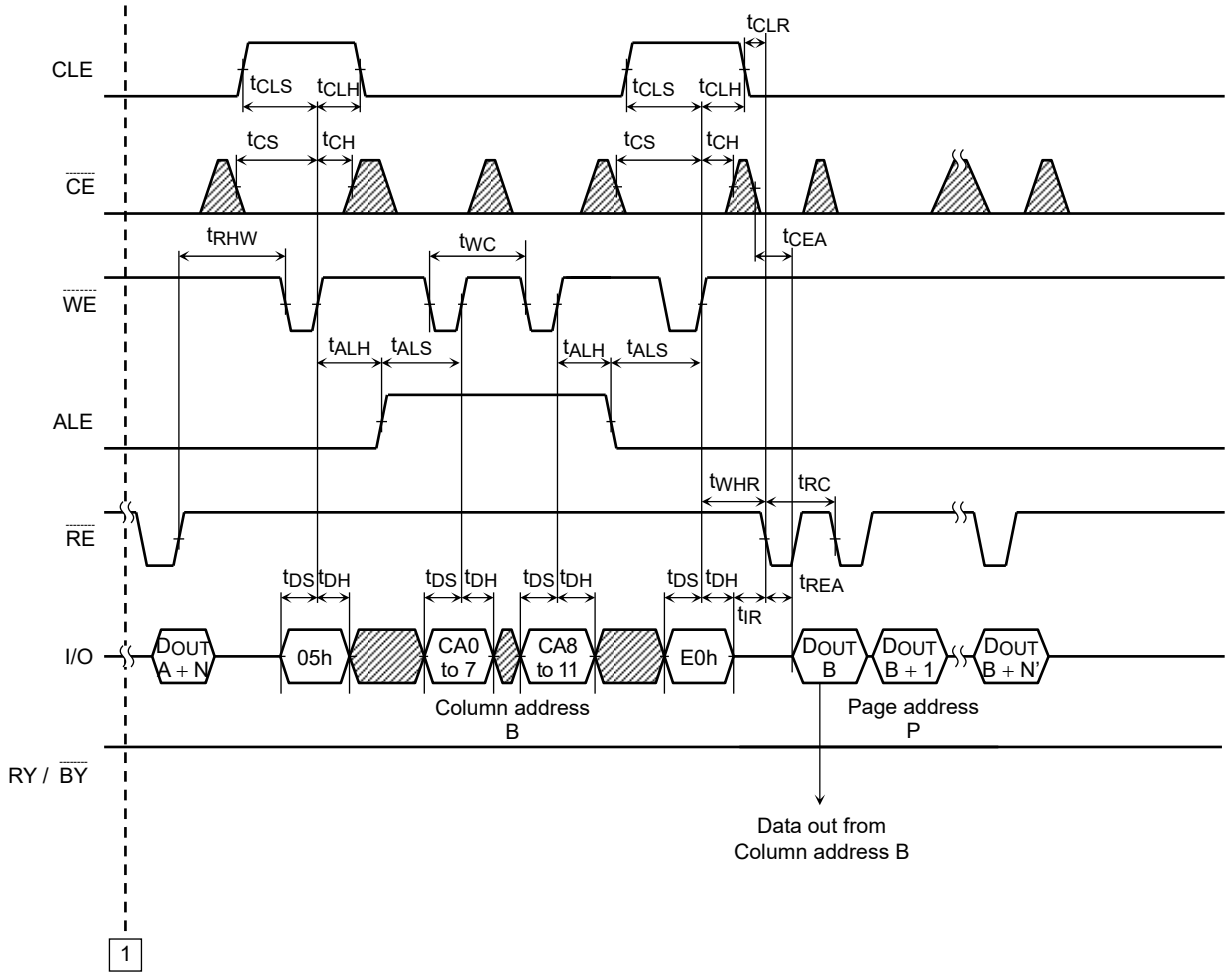
Make sure to terminate the operation with 3Fh command.

Column Address Change in Read Cycle Timing Diagram (1/2)



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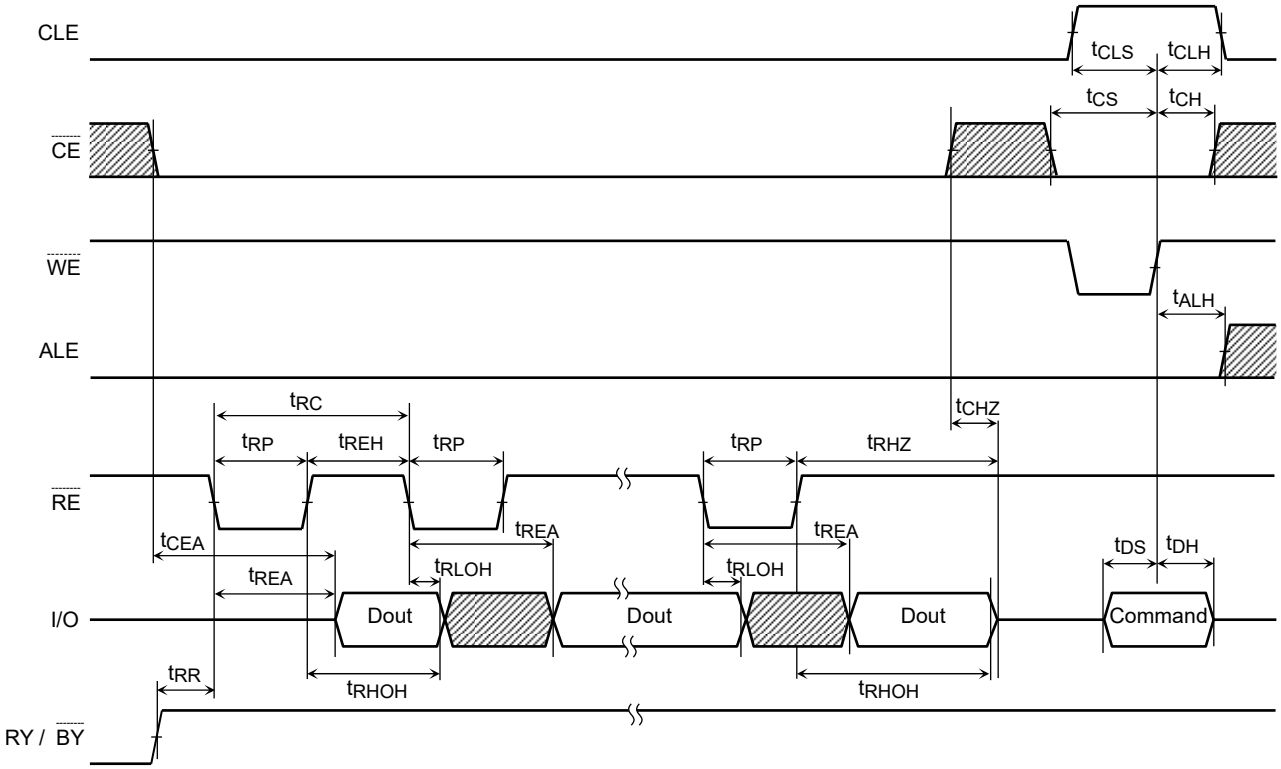
Column Address Change in Read Cycle Timing Diagram (2/2)



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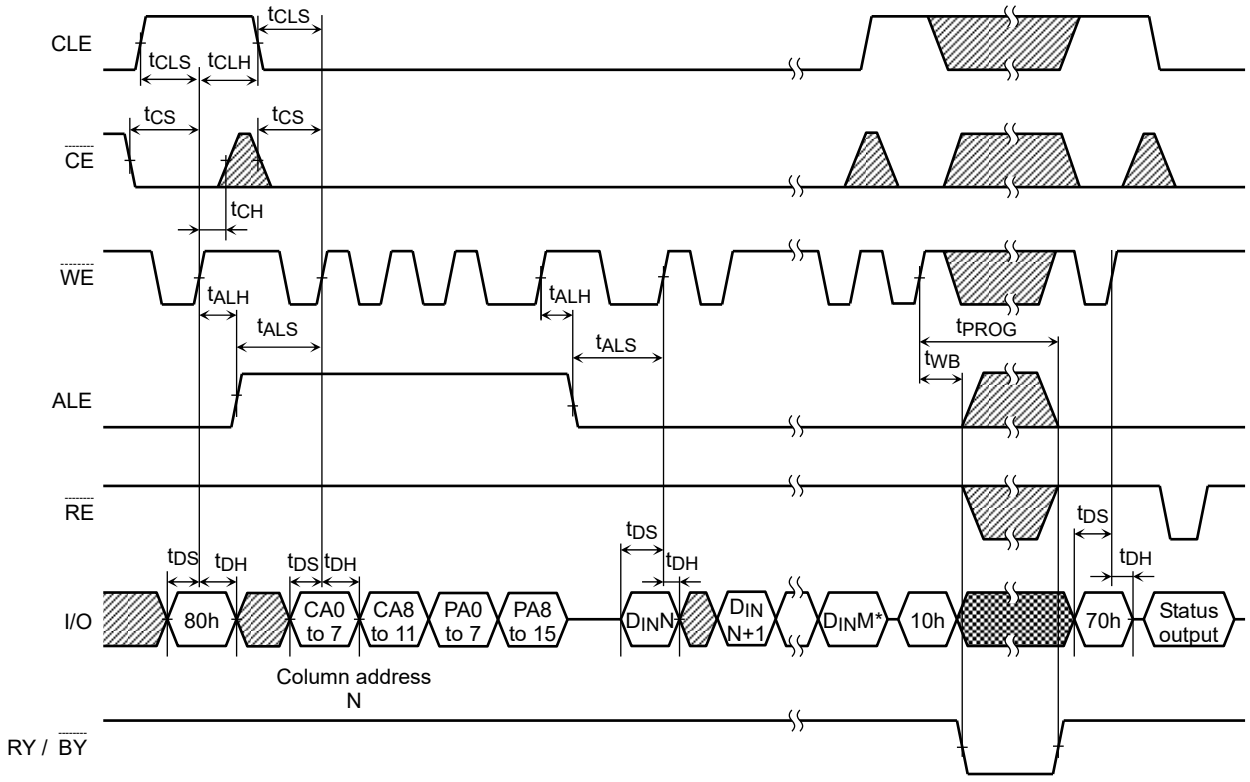
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Data Output Timing Diagram



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Auto-Program Operation Timing Diagram



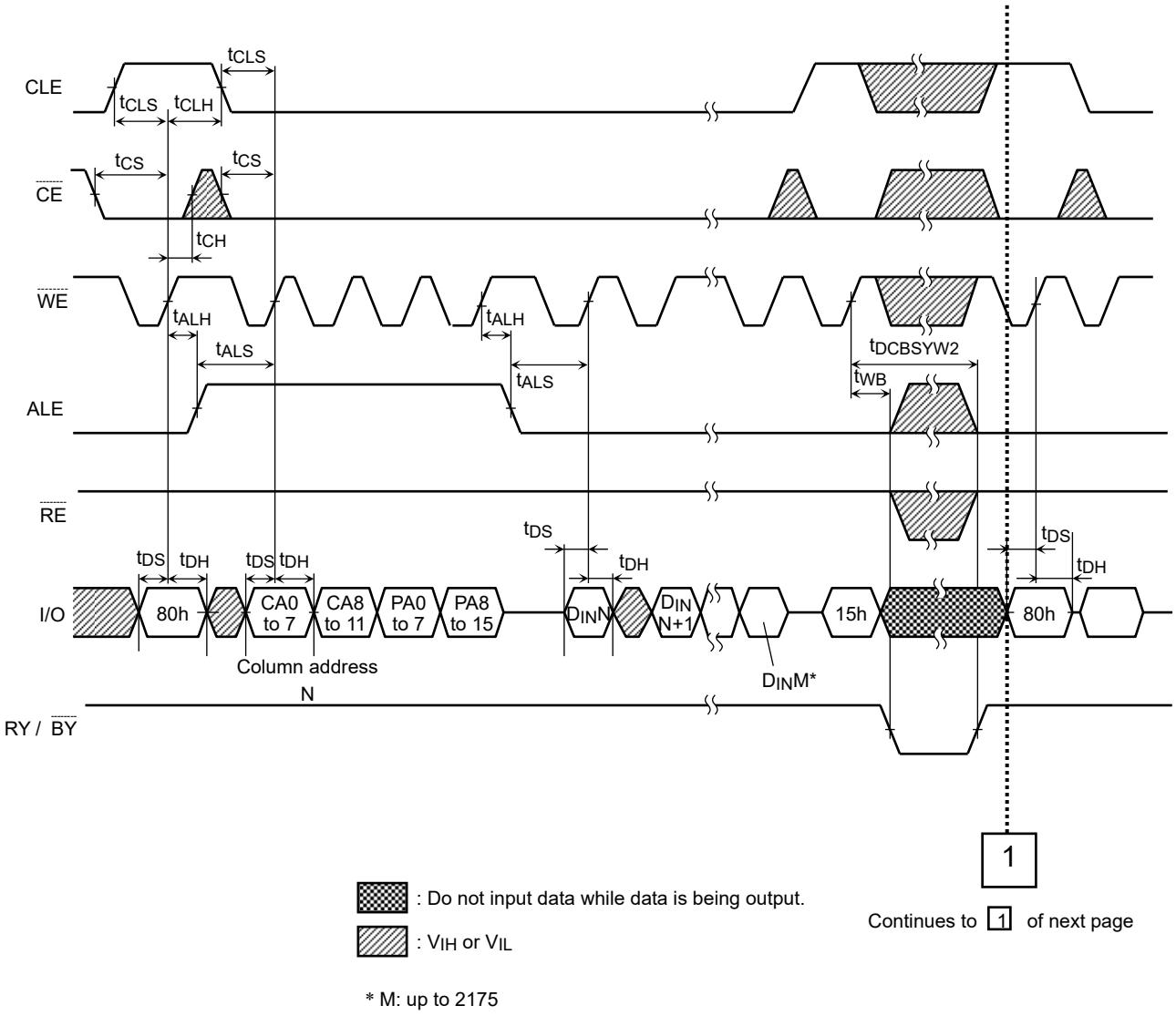
: Do not input data while data is being output.

: V_{IH} or V_{IL}

* M: up to 2175

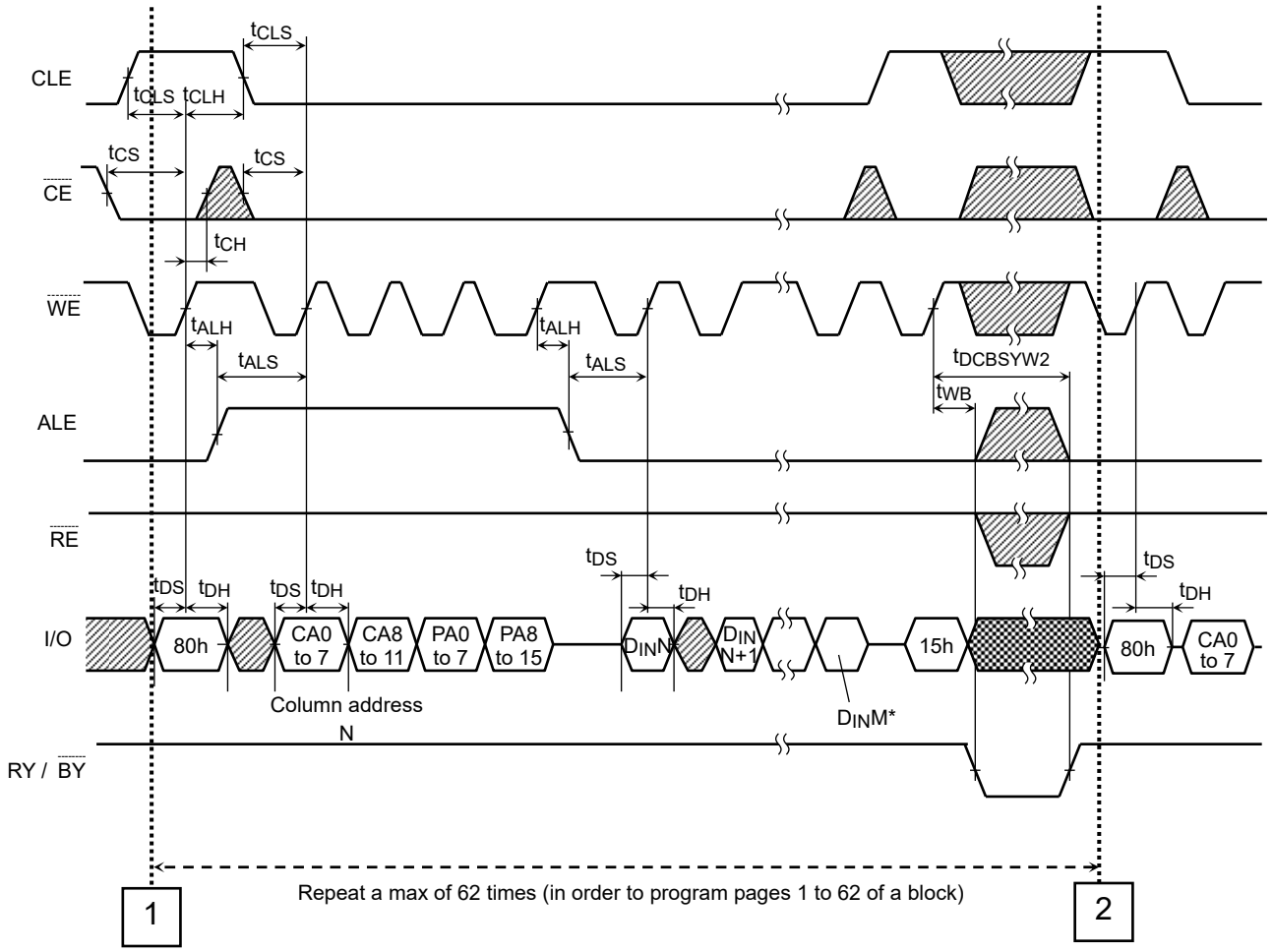
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Auto-Program Operation with Data Cache Timing Diagram (1/3)



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Auto-Program Operation with Data Cache Timing Diagram (2/3)



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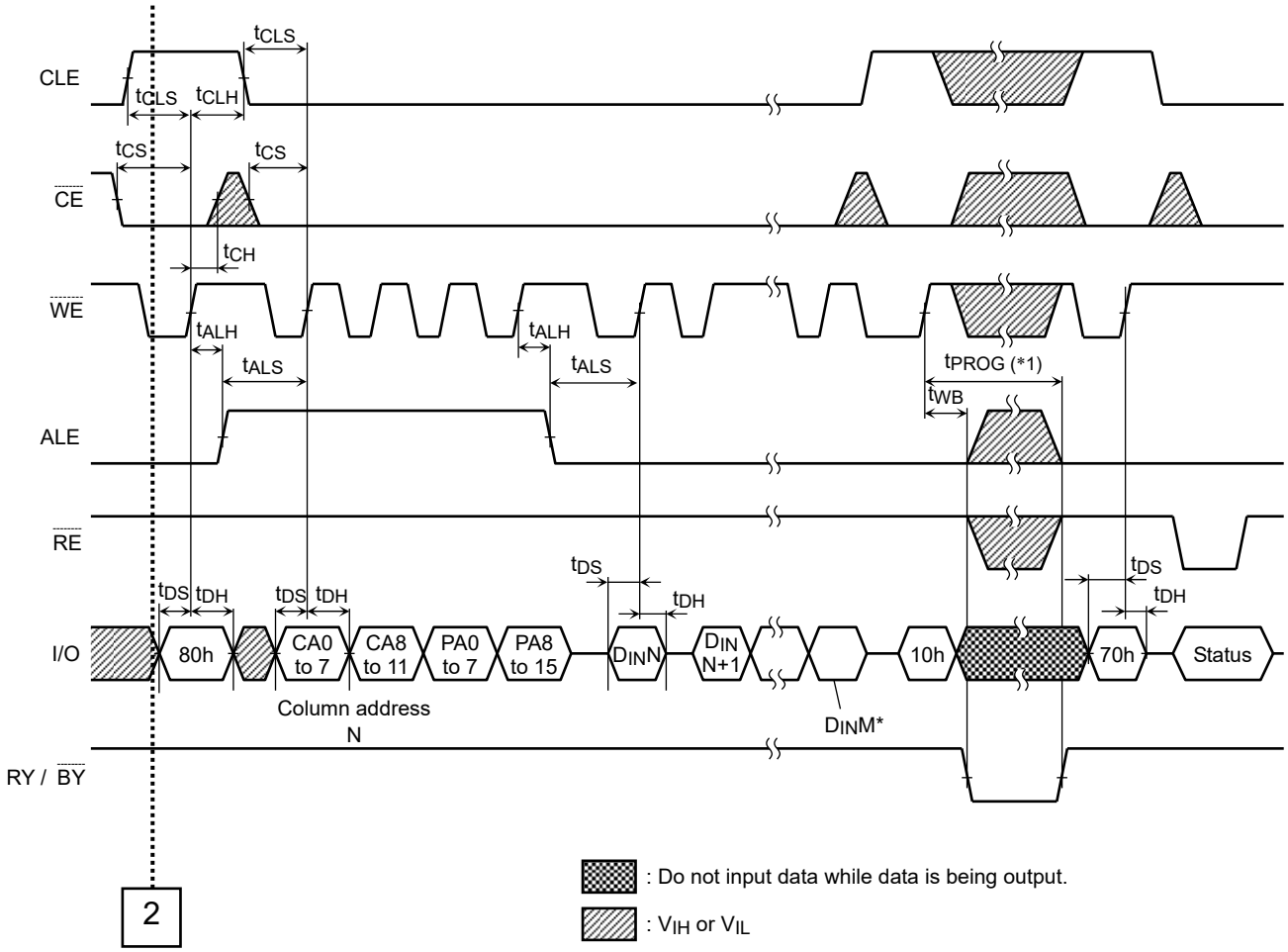
: Do not input data while data is being output.

: V_{IH} or V_{IL}

* M: up to 2175

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Auto-Program Operation with Data Cache Timing Diagram (3/3)



(*1) t_{PROG}: Since the last page's programming by 10h command is initiated after the previous cache program, the t_{PROG} during cache programming is given by the following equation.

t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page − A
A = (command input cycle + address input cycle + data input cycle time of the last page)

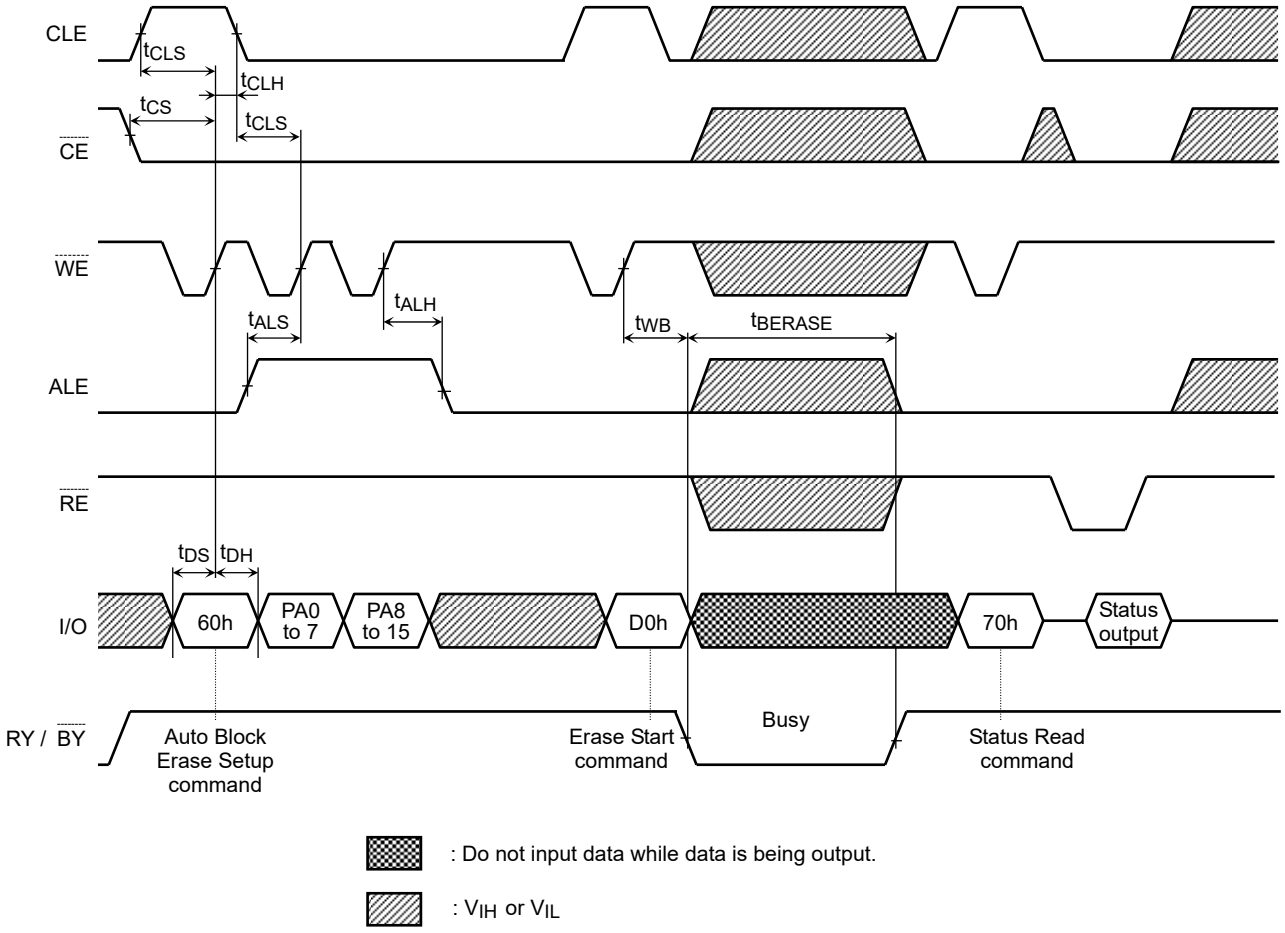
If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

(Note) Make sure to terminate the operation with 80h-10h command sequence.
If the operation is terminated by 80h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing the Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed, issue FFh reset before the next operation.

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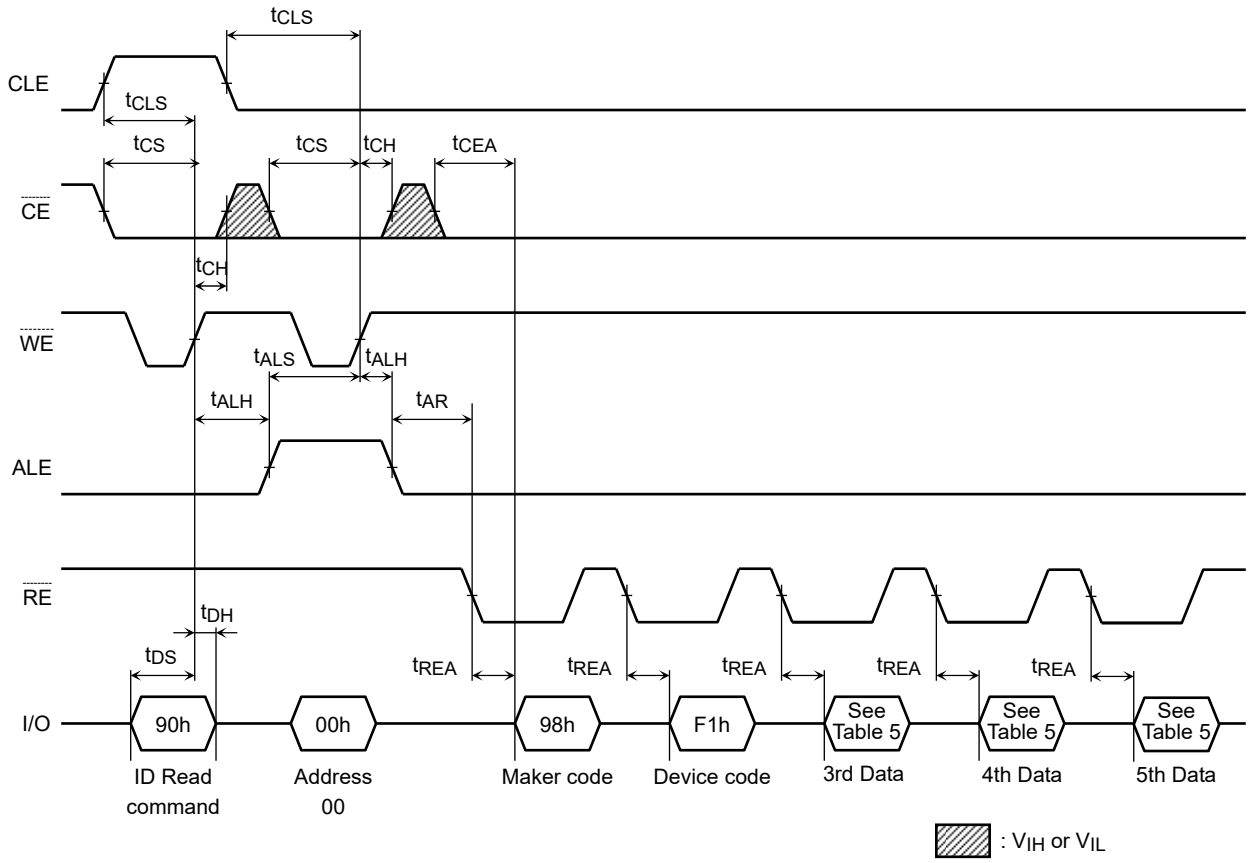
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Auto Block Erase Timing Diagram



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ID Read Operation Timing Diagram



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PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of $\overline{WE}$ while ALE is High.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High while the device is in Ready state. The $\overline{CE}$ signal is ignored when the device is in Busy state (RY / $\overline{BY}$= L), such as during a Program, Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used to protect the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: RY / $\overline{BY}$

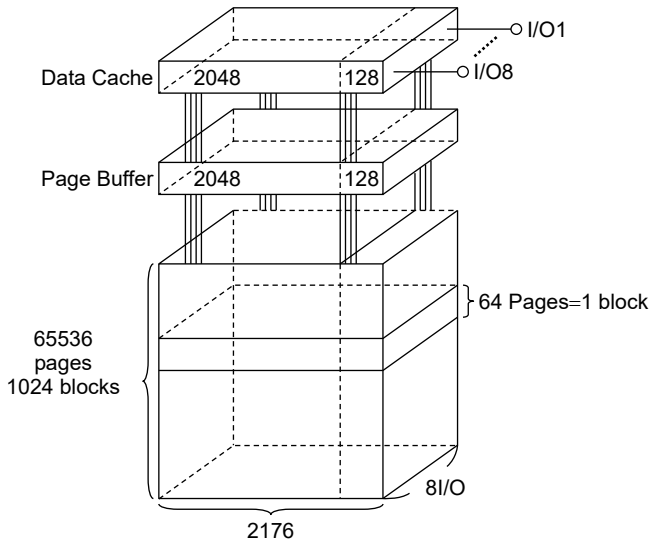
The RY / $\overline{BY}$output signal is used to indicate the operating condition of the device. The RY / $\overline{BY}$ signal is in Busy state (RY / $\overline{BY}$= L) during the Program, Erase and Read operations and will return to Ready state (RY / $\overline{BY}$= H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled up to V_{CC} with an appropriate resistor.
If RY / $\overline{BY}$ signal is not pulled up to V_{CC} (“Open” state), device operation cannot be guaranteed.

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Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.



A page consists of 2176 bytes in which 2048 bytes are used for main memory storage and 128 bytes are for redundancy or for other uses.

1 page = 2176 bytes
1 block = 2176 bytes × 64 pages = (128K + 8K) bytes
Capacity = 2176 bytes × 64 pages × 1024 blocks

An address is read in via the I/O port over four consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	L	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8

CA0 to CA11: Column address
PA0 to PA5: Page address in block
PA6 to PA15: Block address

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Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$*1
Command Input	H	L	L	⌐└↗	H	*
Data Input	L	L	L	⌐└↗	H	H
Address Input	L	H	L	⌐└↗	H	*
Serial Data Output	L	L	L	H	↘⌐	*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: When the $\overline{WP}$ signal goes Low, Program or Erase operation is inhibited (Refer to Application Note (10) toward the end of this document).

*2: If $\overline{CE}$ is Low during Read Busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to the device. Reset or Status Read command can be input during Read Busy.

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Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Read with Data Cache	31	—	
Read Start for Last Page in Read Cycle with Data Cache	3F	—	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Auto Page Program with Data Cache	80	15	
Read for Page Copy (2) with Data Out	00	3A	
Auto Program with Data Cache during Page Copy (2)	8C	15	
Auto Program for last page during Page Copy (2)	8C	10	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70	—	O
Reset	FF	—	O

HEX data bit assignment
(Example) Serial Data Input: 80h

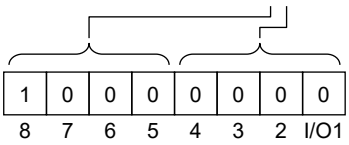


Table 4. Read mode operation states

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

H: V_{IH}, L: V_{IL}

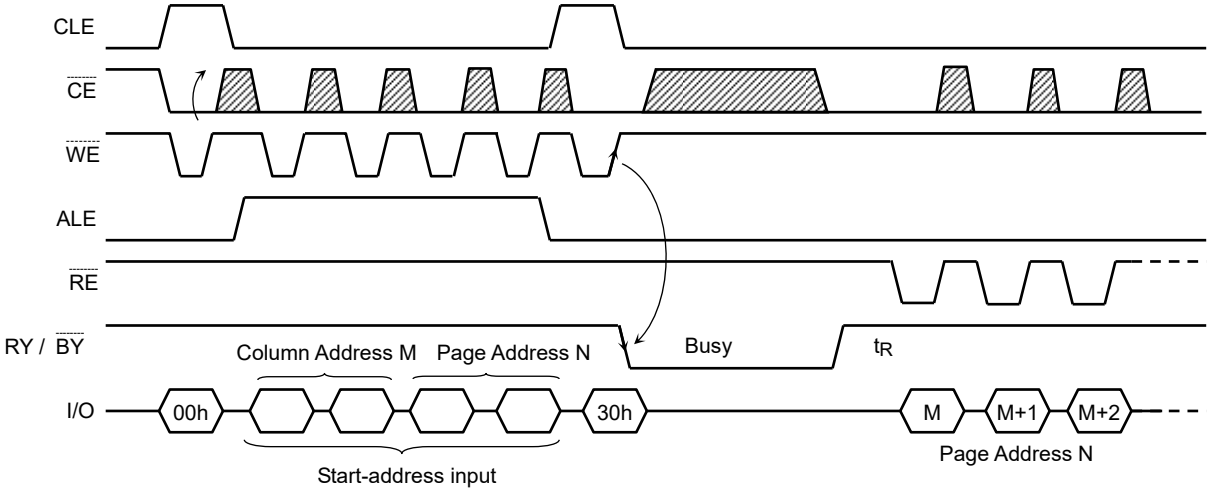
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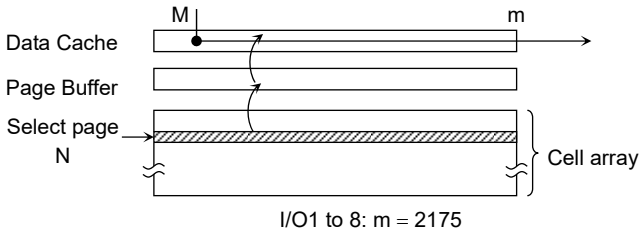
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DEVICE OPERATION

Read Mode

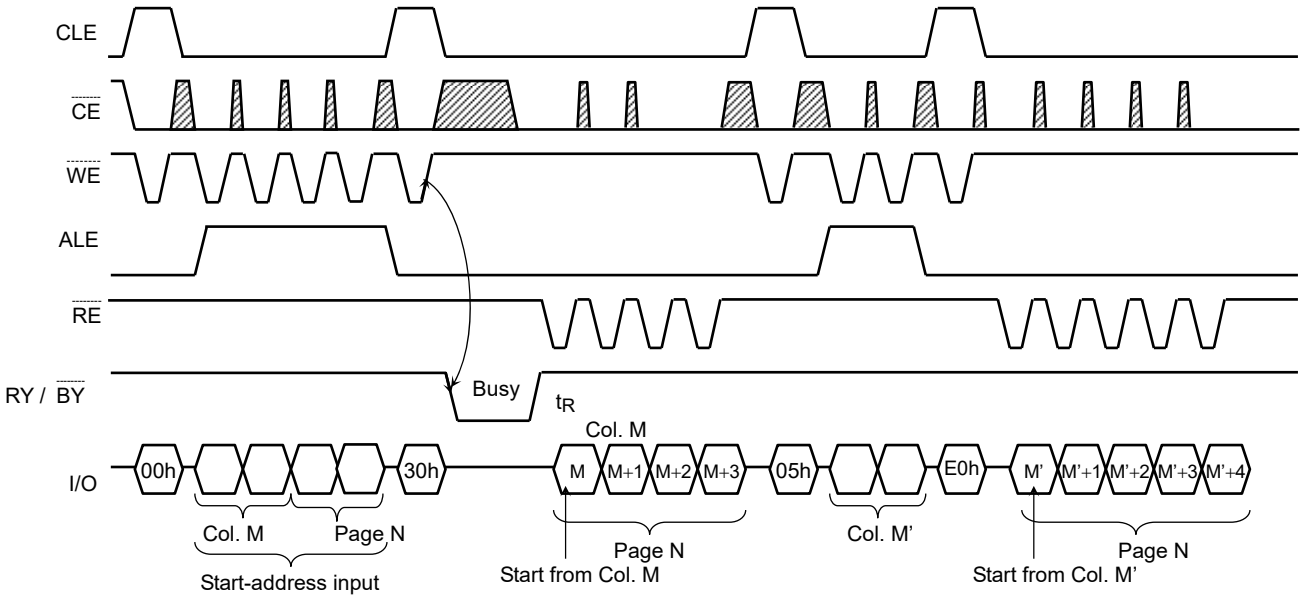
Read mode is set when the "00h" and “30h” commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. After the initial power on sequence, “00h” command is latched into the internal command register. Then the Read operation after the power on sequence is executed by the setting of only four address cycles and “30h” command. The sequence and the block diagram are shown below (Refer to the timing chart for detail).

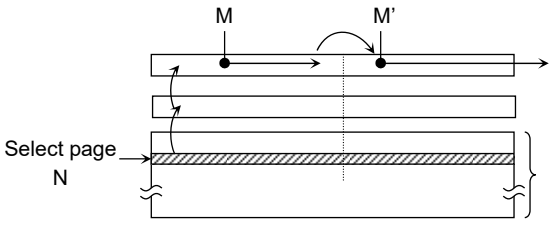




A data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.
After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

Random Column Address Change in Read Cycle





During the serial data output from the Data Cache, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serially starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.

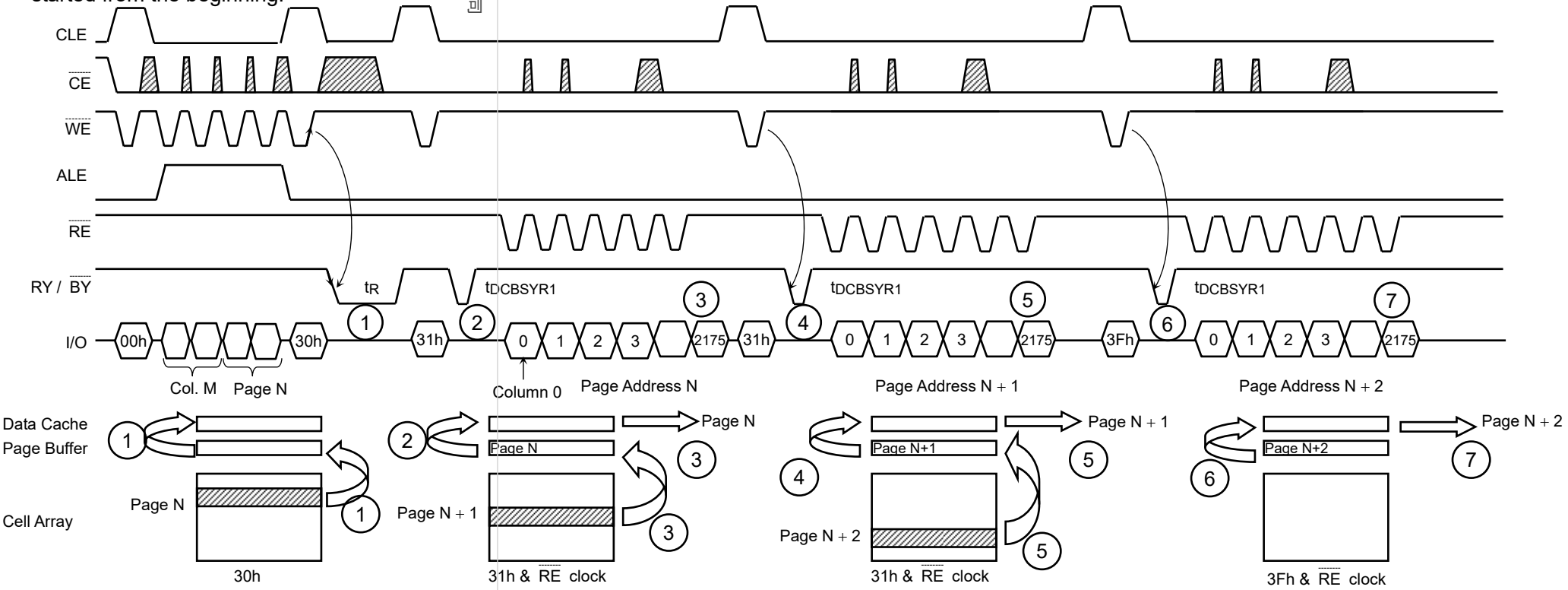
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Read with Data Cache

The device has a Read with Data Cache that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning.



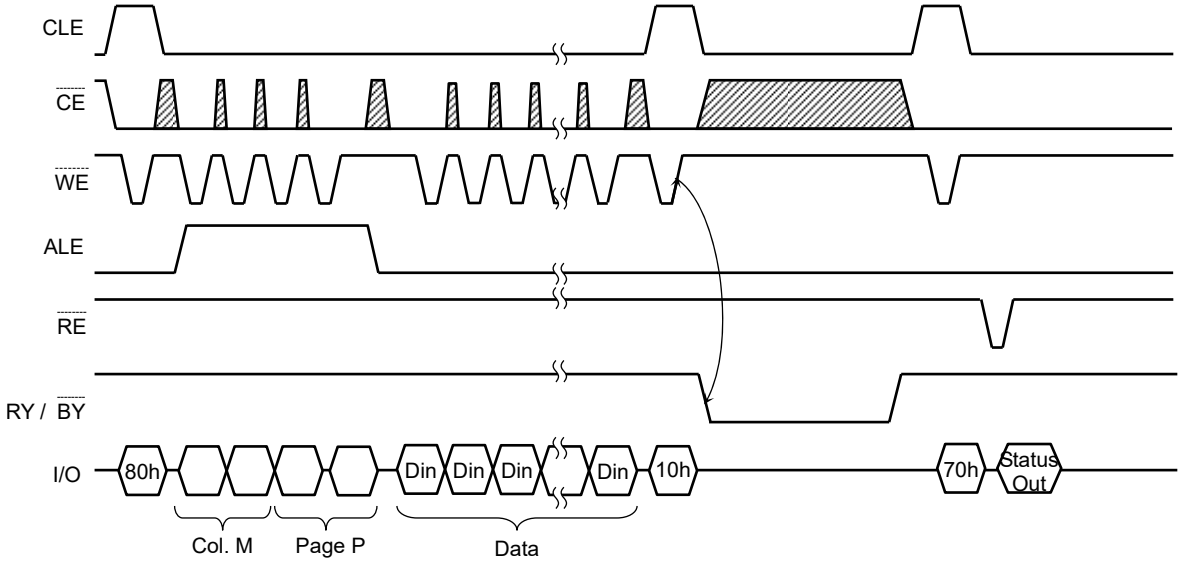
If the 31h command is issued to the device, the data content of the next page is transferred to the Page Buffer during serial data out from the Data Cache, reducing the t_R (Data transfer from memory cell to data register).

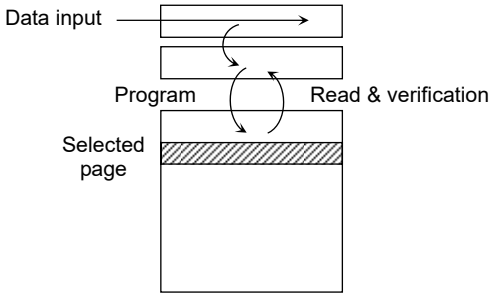
1. Normal read. Data is transferred from Page N to Data Cache through Page Buffer. During this time period, the device outputs Busy state for t_R max.
2. After the Ready/Busy signal returns to Ready, 31h command is issued and data is transferred to Data Cache from Page Buffer again. This data transfer takes $t_{DCBSYR1}$ max and the completion of this time period can be detected by Ready/Busy signal.
3. Data of Page N + 1 is transferred to Page Buffer from cell while the data of Page N in Data Cache can be read out by /RE clock simultaneously.
4. The 31h command makes data of Page N + 1 transfer to Data Cache from Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for $t_{DCBSYR1}$ max.. This Busy period depends on the combination of the internal data transfer time from cell to Page Buffer and the serial data out time.
5. Data of Page N + 2 is transferred to Page Buffer from cell while the data of Page N + 1 in Data Cache can be read out by /RE clock simultaneously.
6. The 3Fh command makes the data of Page N + 2 transfer to the Data Cache from the Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for $t_{DCBSYR1}$ max.. This Busy period depends on the combination of the internal data transfer time from cell to Page Buffer and the serial data out time.
7. Data of Page N + 2 in Data Cache can be read out, but since the 3Fh command does not transfer the data from the memory cell to Page Buffer, the device can accept new command input immediately after the completion of serial data out.

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Auto Page Program Operation

The device carries out an Auto Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below (Refer to the detailed timing chart).

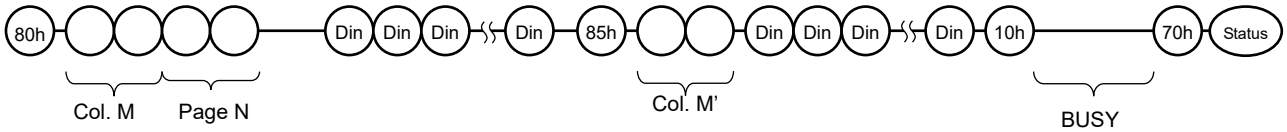


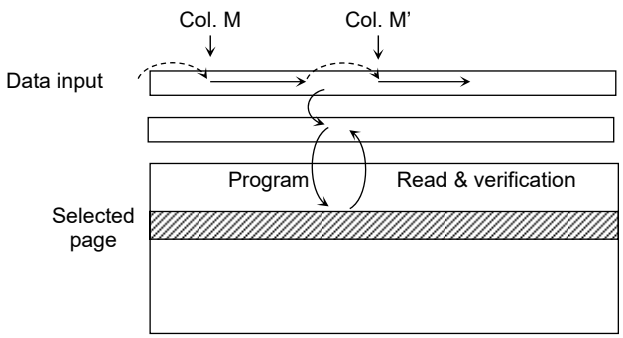


The data is transferred (programmed) from the Data Cache via the Page Buffer to the selected page on the rising edge of $\overline{WE}$ following input of the “10h” command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Random Column Address Change in Auto Page Program Operation

The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.
Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.





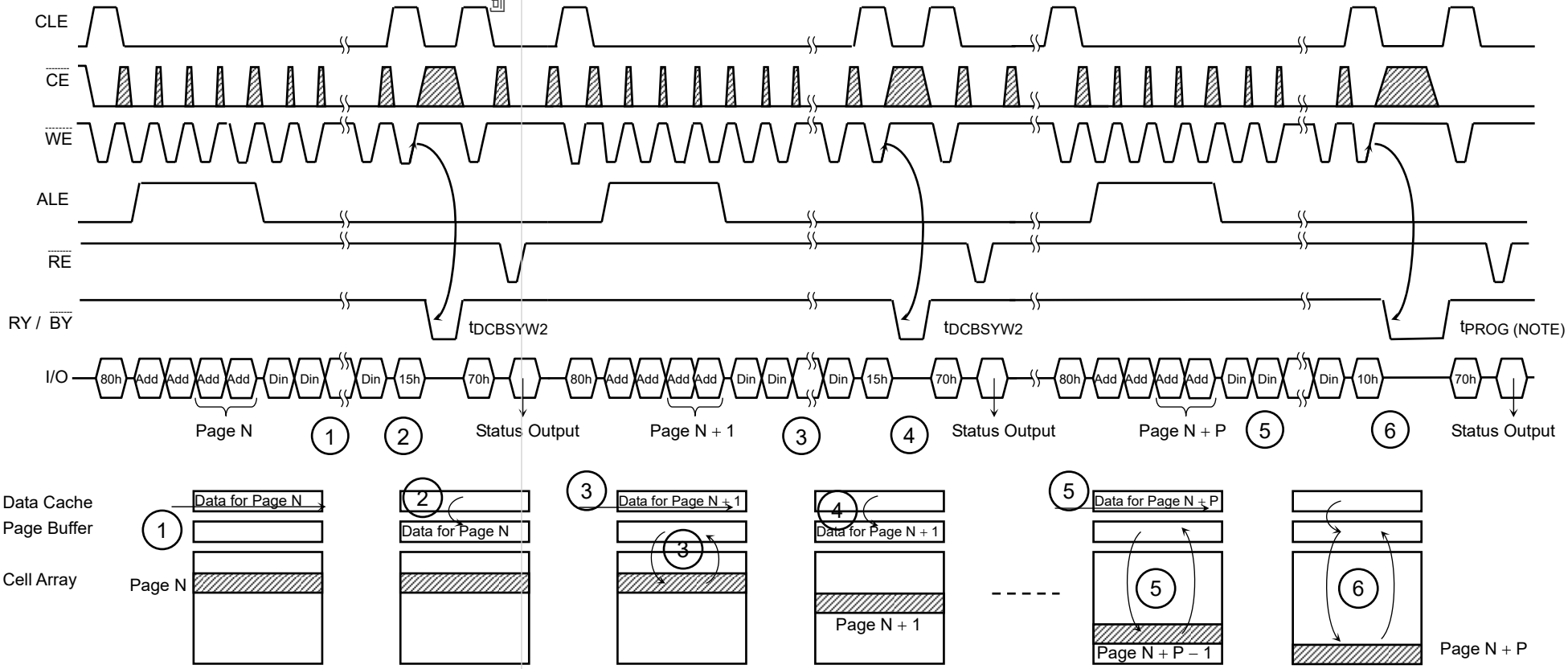
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Auto Page Program Operation with Data Cache

The device has an Auto Page Program with Data Cache operation enabling the high speed program operation shown below. When the block address changes, this sequence has to be started from the beginning.



Issuing the 15h command to the device after serial data input initiates the program operation with Data Cache

1. Data for Page N is input to Data Cache.
2. Data is transferred to the Page Buffer by the 15h command. During the transfer the Ready/Busy signal outputs Busy state ($t_{DCBSYW2}$).
3. Data is programmed to the selected page while the data for Page N + 1 is input to the Data Cache.
4. By the 15h command, the data in the Data Cache is transferred to the Page Buffer after the programming of Page N is completed. The device outputs Busy state from the 15h command until the Data Cache becomes empty. The duration of this period depends on timing between the internal programming of Page N and serial data input for Page N + 1 ($t_{DCBSYW2}$).
5. Data for Page N + P is input to the Data Cache while the data of the Page N + P – 1 is being programmed.
6. The programming with Data Cache is terminated by the 10h command. When the device becomes Ready state, it shows that the internal programming of the Page N + P is completed.

NOTE: Since the last page's programming by the 10h command is initiated after the previous cache program, the t_{PROG} during cache programming is given by the following;
t_{PROG} = t_{PROG} for the last page + t_{PROG} of the previous page – (command input cycle + address input cycle + data input cycle time of the previous page)

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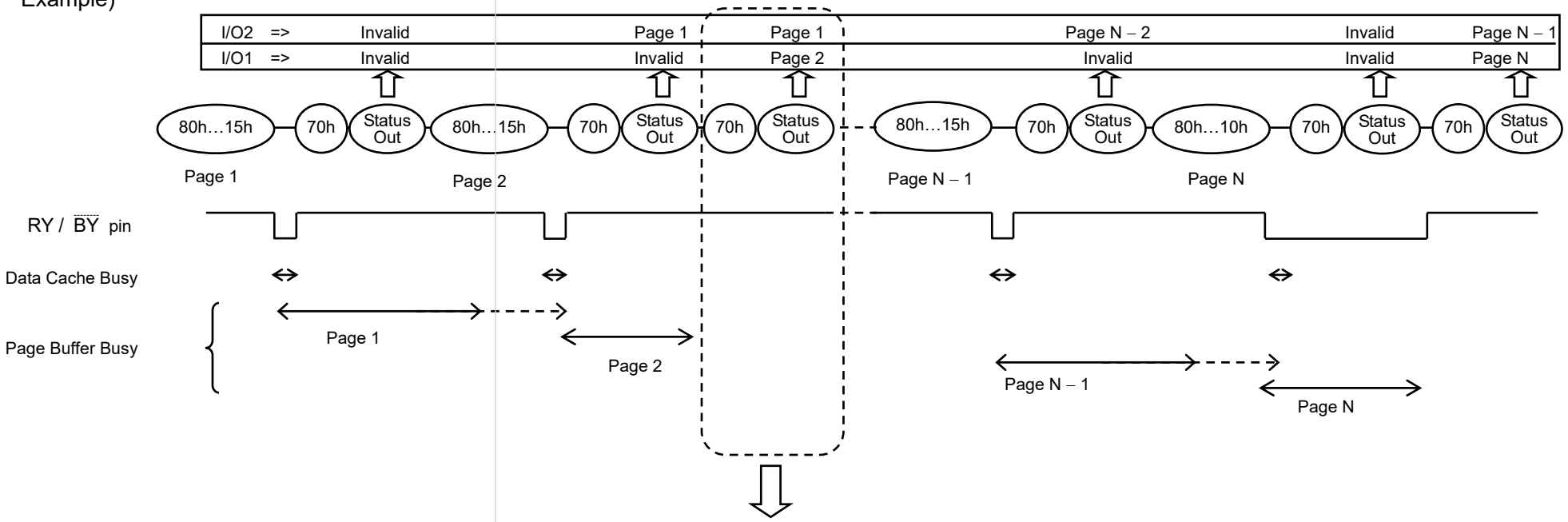
Pass/Fail status for each page programmed by the Auto Page Program with Data Cache operation can be detected by the Status Read operation.

- I/O1: Pass/Fail of the current page program operation.
- I/O2: Pass/Fail of the previous page program operation.

The Pass/Fail status on I/O1 and I/O2 are valid under the following conditions.

- Status on I/O1: Page Buffer Ready/Busy is Ready.
  The Page Buffer Ready/Busy is output on I/O6 by Status Read operation or RY / $\overline{BY}$ pin after the 10h command.
- Status on I/O2: Data Cache Read/Busy is Ready.
  The Data Cache Ready/Busy is output on I/O7 by Status Read operation or RY / $\overline{BY}$ pin after the 15h command.

Example)



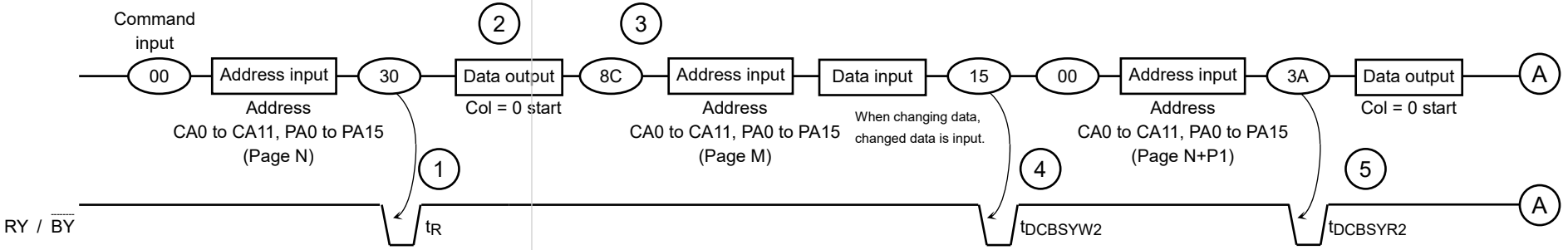
If the Page Buffer Busy returns to Ready before the next 80h command input and Status Read is done during this Ready period, the Status Read provides the Pass/Fail result for Page 2 on I/O1 and the Pass/Fail result for Page1 on I/O2.

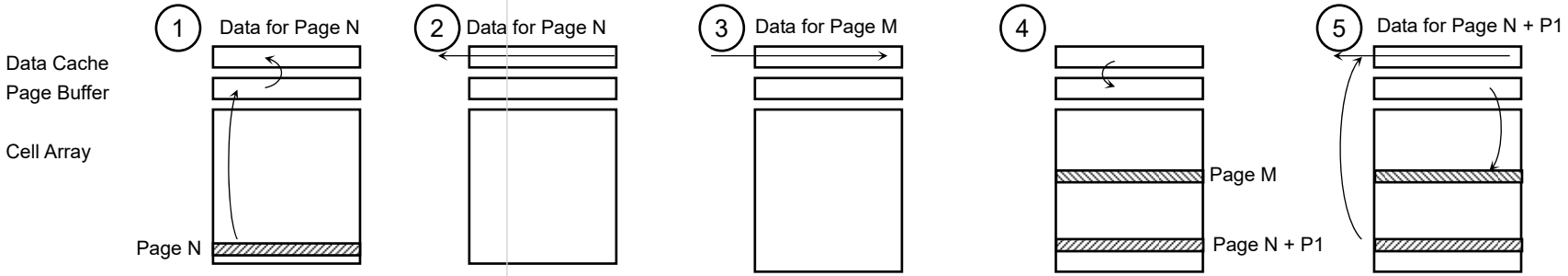
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Page Copy (2)

By using Page Copy (2), data in a page can be copied to another page after the data has been read out.
When the block address changes (increments) this sequence has to be started from the beginning.



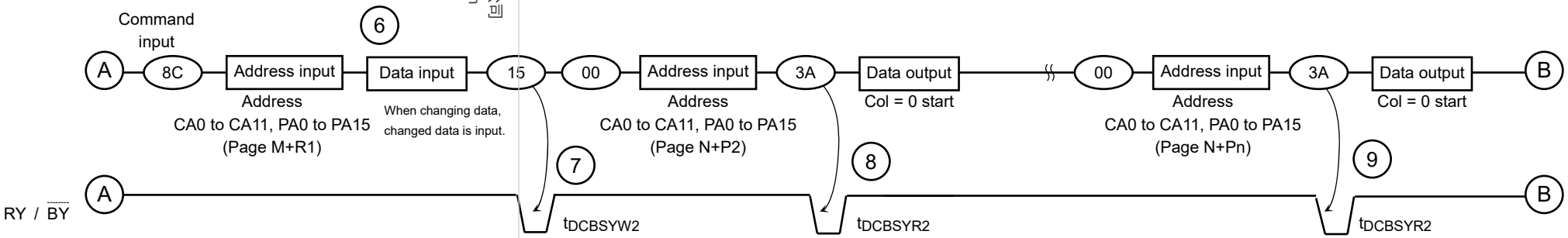


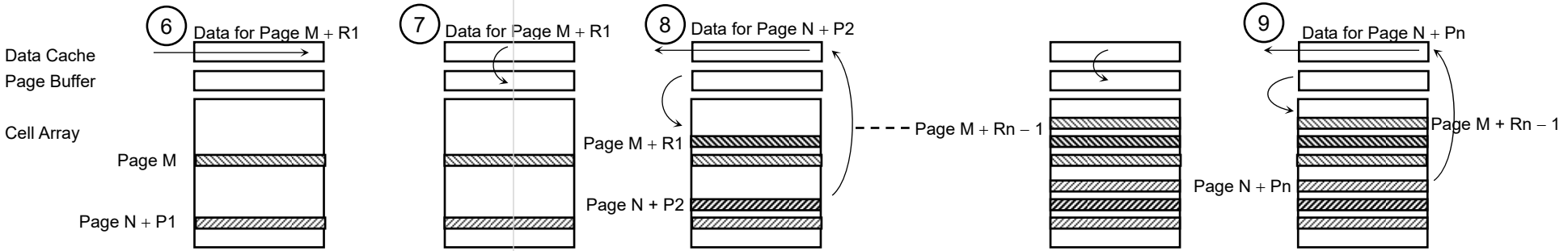
Page Copy (2) operation is as follows.

1. Data for Page N is transferred to the Data Cache.
2. Data for Page N is read out.
3. Address for Page M is input. If the data needs to be changed, changed data is input.
4. Data Cache for Page M is transferred to the Page Buffer.
5. After the Ready state, Data for Page N + P1 is output from the Data Cache while the data of Page M is being programmed.

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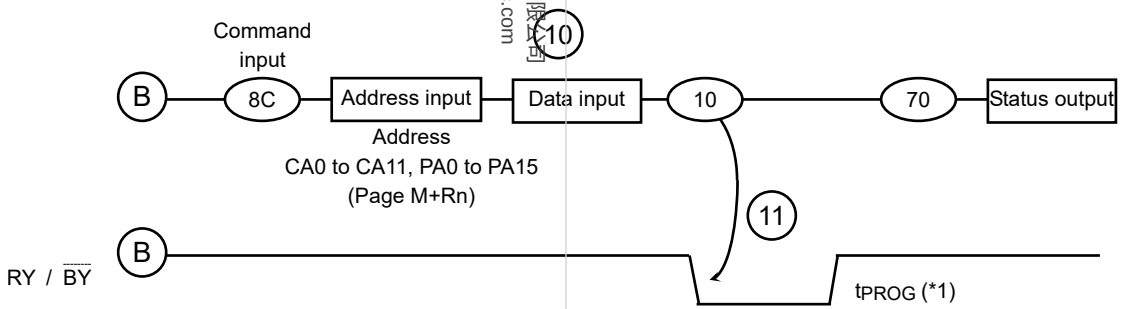


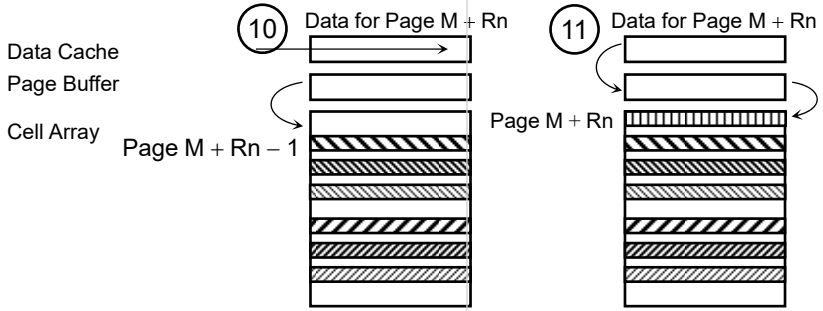


6. Address for Page (M + R1) is input. If the data needs to be changed, changed data is input.
7. After programming of page M is completed, Data Cache for Page M + R1 is transferred to the Page Buffer.
8. By the 15h command, the data in the Page Buffer is programmed to Page M + R1. Data for Page N + P2 is transferred to the Data cache.
9. The data in the Page Buffer is programmed to Page M + Rn – 1. Data for Page N + Pn is transferred to the Data Cache.

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10. Address for Page (M + Rn) is input. If the data needs to be changed, changed data is input.
11. By issuing the 10h command, the data in the Page Buffer is programmed to Page M + Rn.

(*1) Since the last page's programming by the 10h command is initiated after the previous cache program, the t_{PROG} here will be expected as the following:
t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page – (command input cycle + address input cycle + data output/input cycle time of the last page)

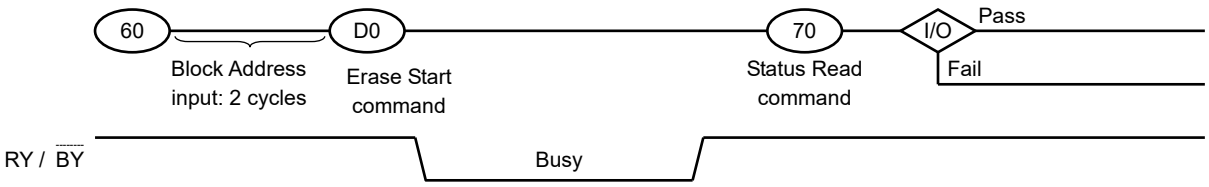
NOTE: Data input is required only if previous data output needs to be altered.
If the data has to be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that needs be changed.
If the data does not have to be changed, data input cycles are not required.

Make sure $\overline{WP}$ is held to High when the Page Copy (2) operation is performed.
Also make sure the Page Copy operation is terminated with 8Ch-10h command sequence

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Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command “D0h” which follows the Erase Setup command “60h”. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



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ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

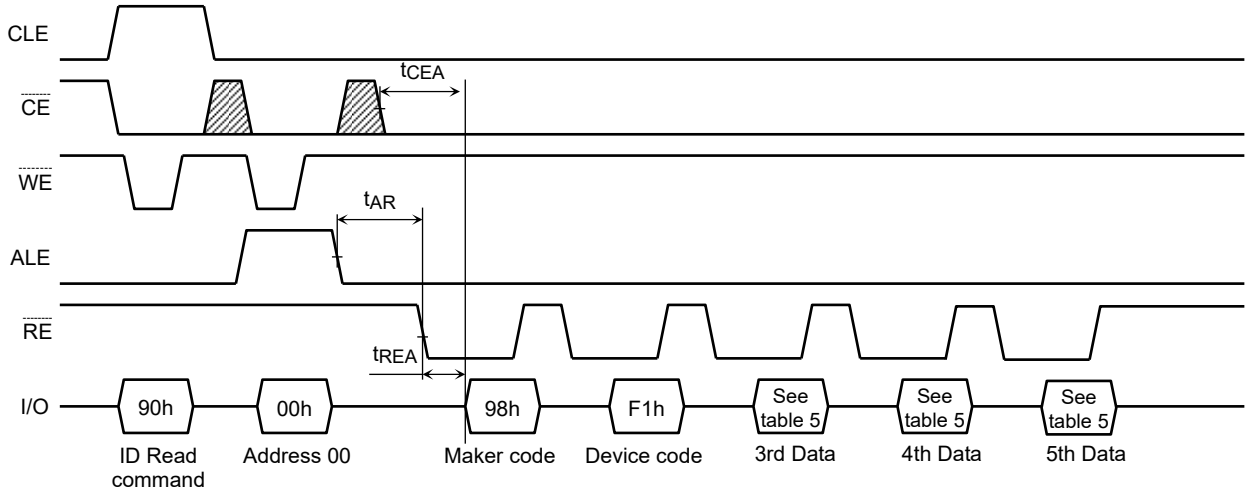


Table 5. Code table

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	1	1	1	0	0	0	1	F1h
3rd Data	Chip Number, Cell Type	1	0	0	0	0	0	0	0	80h
4th Data	Page Size, Block Size,	0	0	0	1	0	1	0	1	15h
5th Data	District Number	0	1	1	1	0	0	1	0	72h

3rd Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 level cell 4 level cell 8 level cell 16 level cell					0 0 1 1	0 1 0 1		
Reserved		1	0	0	0				

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4th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size (without redundant area)	1 KB 2 KB 4 KB 8 KB							0 0 1 1	0 1 0 1
Block Size (without redundant area)	64 KB 128 KB 256 KB 512 KB			0 0 1 1	0 1 0 1				
I/O Width	x8 x16		0 1						
Reserved		0				0	1		

5th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
District Number	1 District 2 Districts 4 Districts 8 Districts					0 0 1 1	0 1 0 1		
Reserved		0	1	1	1			1	0

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Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass /fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using $\overline{RE}$ after a “70h” command input. The Status Read command can also be used during a Read operation to monitor the Ready/Busy status.

The resulting information is outlined in Table 6.

Table 6. Status output table

	Definition	Page Program Block Erase	Cache Program	Read Cache Read
I/O1	Chip Status1 Pass: 0 Fail: 1	Pass/Fail	Pass/Fail	Invalid
I/O2	Chip Status 2 Pass: 0 Fail: 1	Invalid	Pass/Fail	Invalid
I/O3	Not Used	0	0	0
I/O4	Not Used	0	0	0
I/O5	Not Used	0	0	0
I/O6	Page Buffer Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O7	Data Cache Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O8	Write Protect Not Protected :1 Protected: 0	Not Protect/Protected	Not Protect/Protected	Not Protect/Protected

The Pass/Fail status on I/O1 and I/O2 is only valid during a Program/Erase operation when the device is in the Ready state.

Chip Status 1:

During an Auto Page Program or Auto Block Erase operation this bit indicates the Pass/Fail result. During an Auto Page Program with Data Cache operation, this bit shows the Pass/Fail results of the current page program operation and therefore this bit is only valid when I/O6 shows the Ready state.

Chip Status 2:

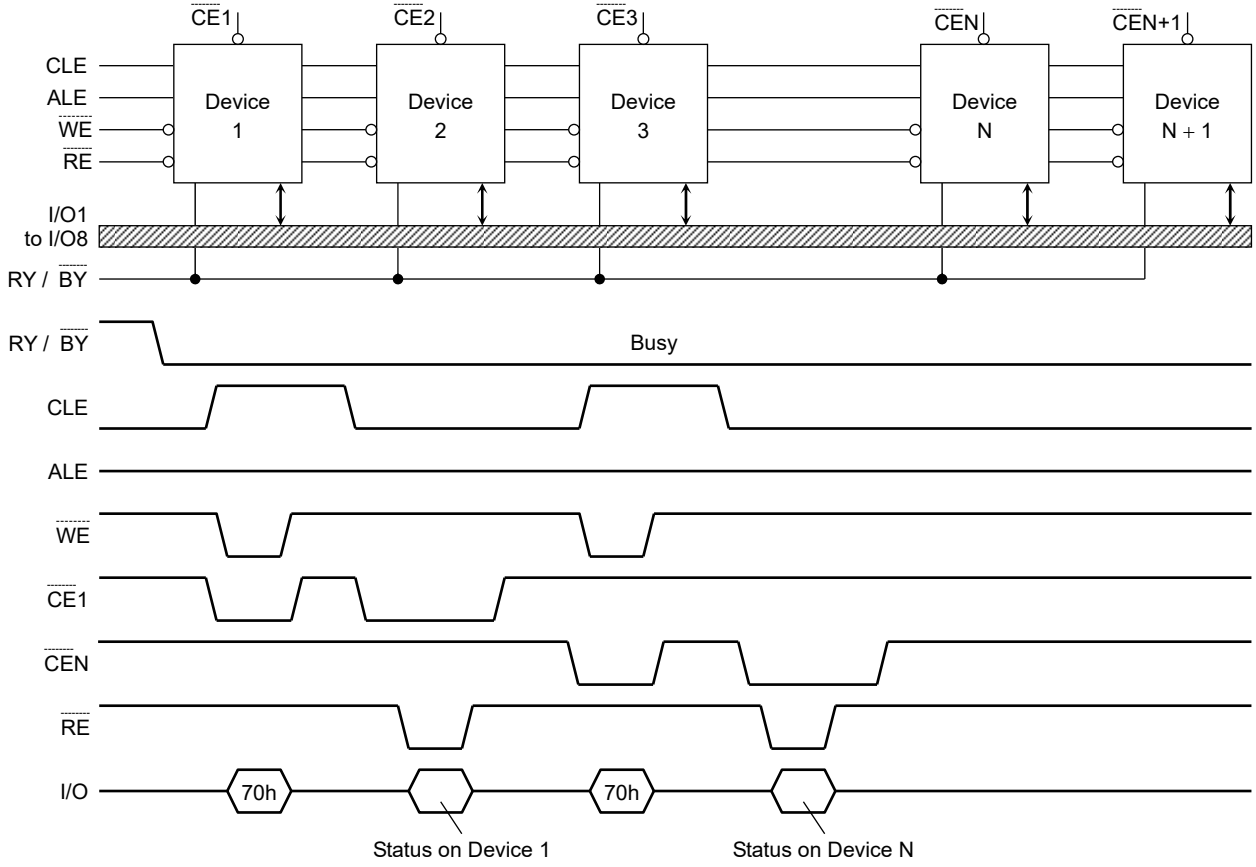
This bit shows the Pass/Fail result of the previous page program operation during Auto Page Program with Data Cache. This status is valid when I/O7 shows the Ready State.

The status output on I/O6 is the same as that of I/O7 if the command input just before 70h is not 15h or 31h.

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An application example with multiple devices is shown in the figure below.



System Design Note:
If the RY / BY pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

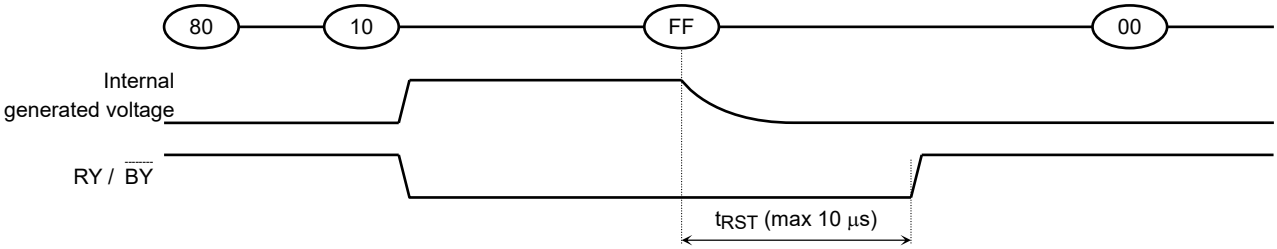
Reset

The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volts and the device enters the Wait state.

Reset during a Cache Program/Page Copy may not just stop the most recent page program but it may also stop the previous program at a page depending on when the FF reset is input.

The response to a “FFh” Reset command input during the various device operations is as follows:

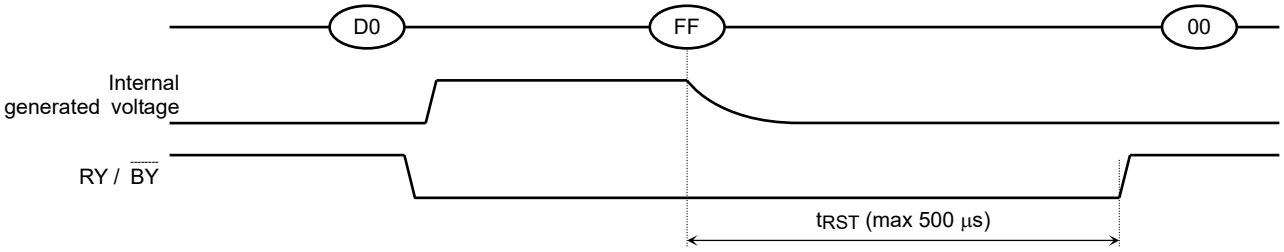
When a Reset (FFh) command is input during Program operation



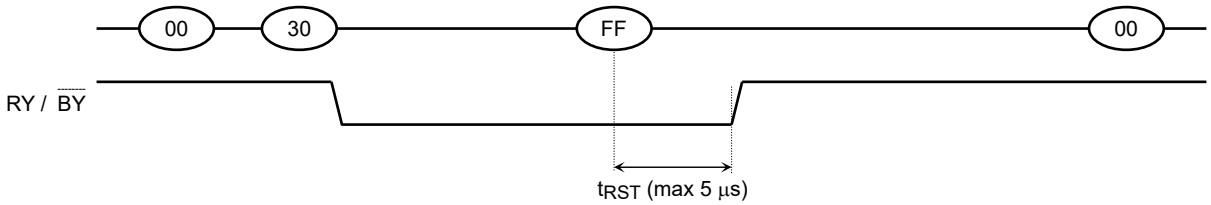
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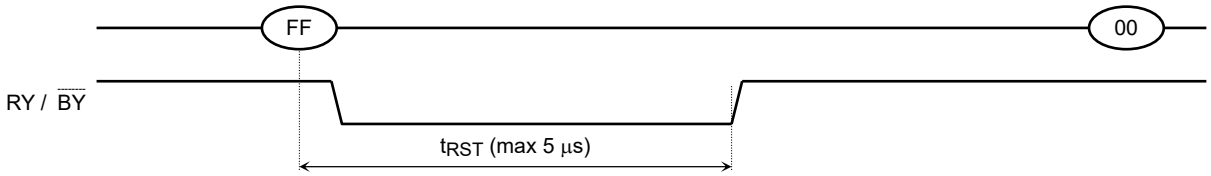
When a Reset (FFh) command is input during Erase operation



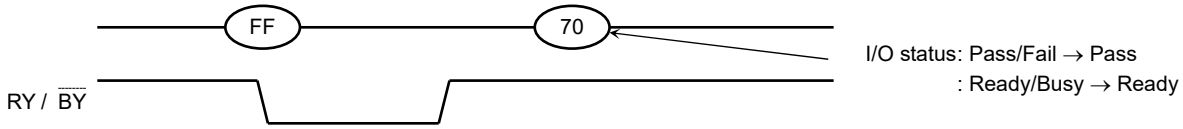
When a Reset (FFh) command is input during Read operation



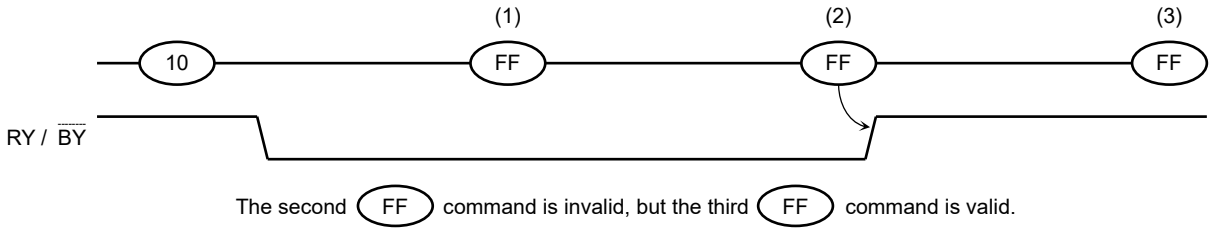
When a Reset (FFh) command is input during Ready



When a Status Read command (70h) is input after a Reset



When two or more Reset commands are input in succession



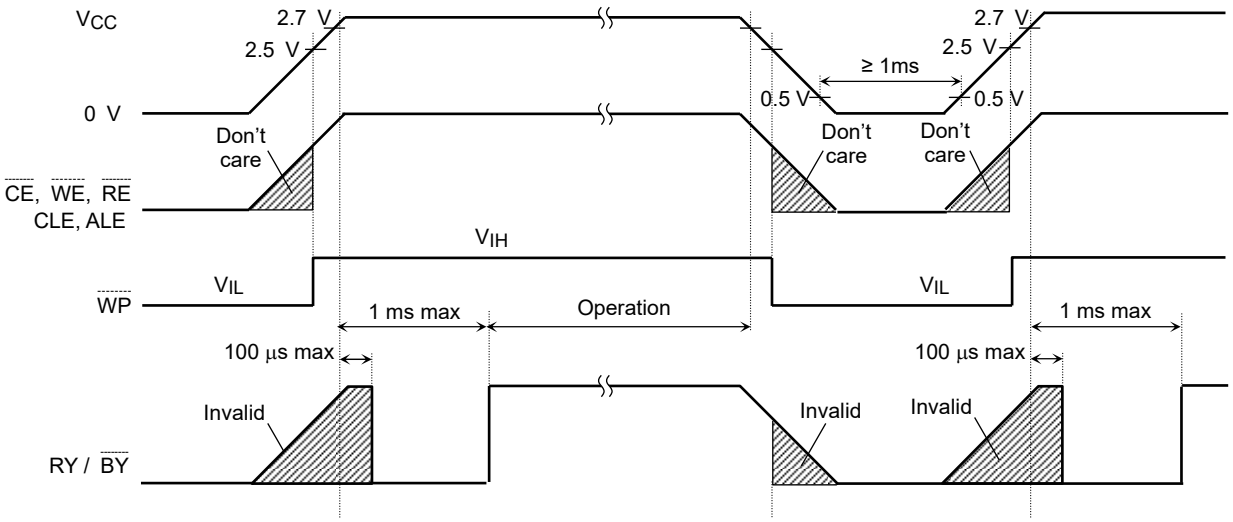
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APPLICATION NOTES AND COMMENTS

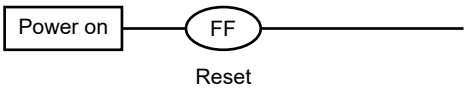
(1) Power-on/off sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence. The device's internal initialization starts after the power supply reaches an appropriate level during the power-on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.
The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off.



(2) Power-on Reset

The following sequence is necessary because some input signals may not be stable at power-on.



(3) Prohibition of unspecified commands

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of commands while in the Busy state

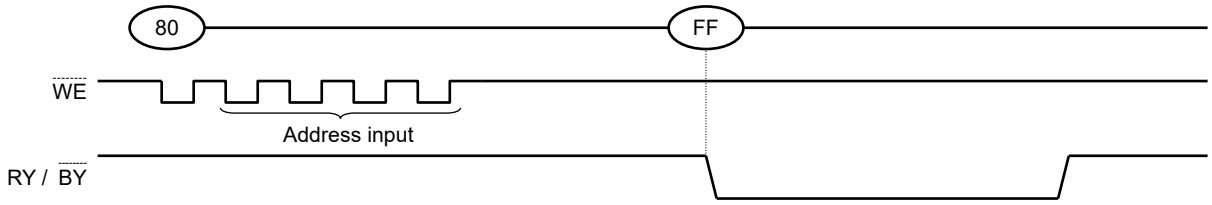
During the Busy state, do not input any command except 70h and FFh.

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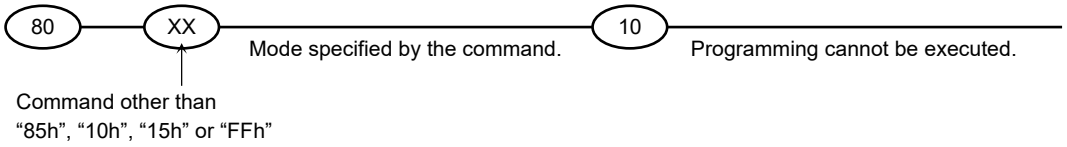
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(5) Acceptable commands after Serial Data Input command “80h”

Once the Serial Data Input command “80h” has been input, do not input any command other than the Column Address Change in Serial Data Input command “85h”, Auto Page Program command “10h”, Auto Page Program with Data Cache Command “15h”, or the Reset command “FFh”.

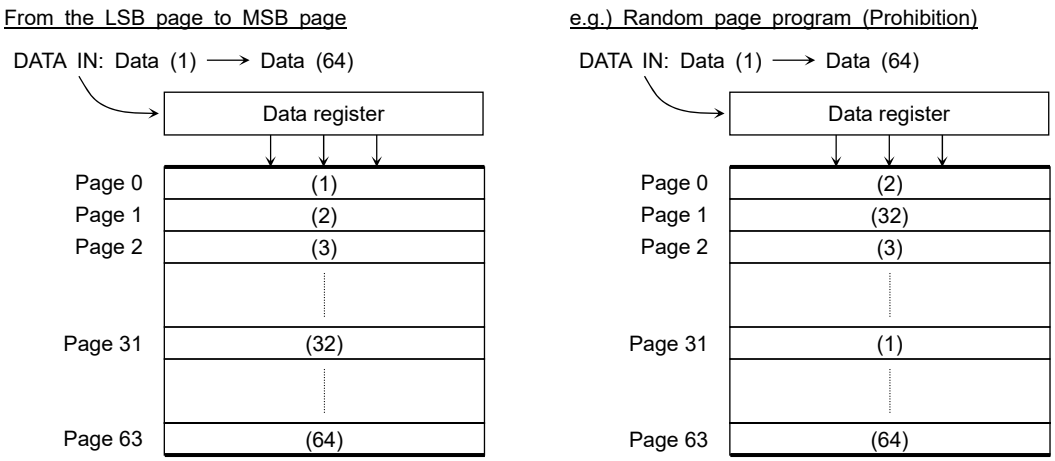


If a command other than “85h” , “10h”, “15h” or “FFh” is input, the Program operation is not performed and the device operation is set to the mode that the input command specifies.



(6) Addressing for program operation

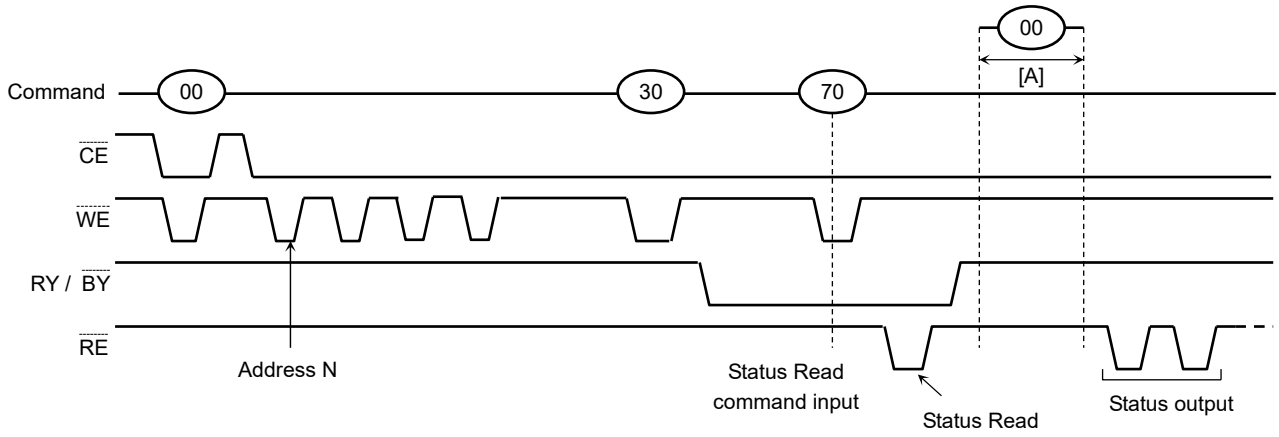
Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to the MSB (most significant bit) page of the block. Random page address programming is prohibited.



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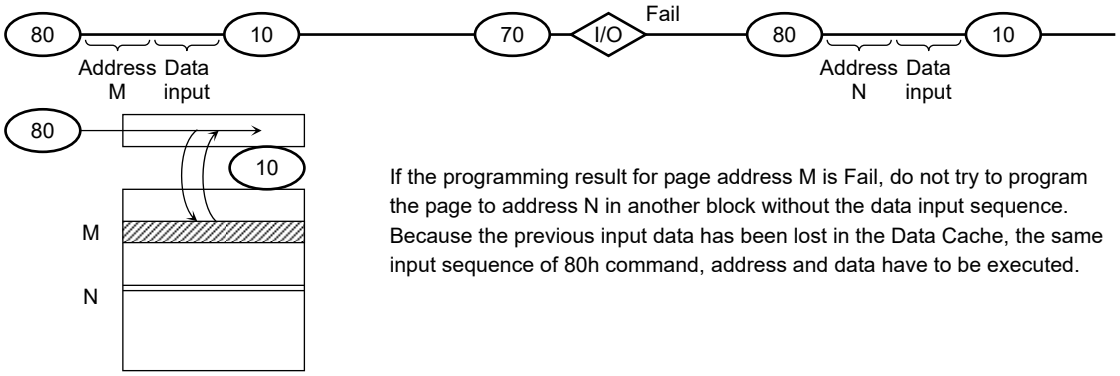
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(7) Status Read during a Read operation



The device status can be read out by inputting the Status Read command “70h” in Read mode. Once the device has been set to Status Read mode by a “70h” command, the device will not return to Read mode unless the Read command “00h” is input during [A]. If the Read command “00h” is input during [A], Status Read mode is reset, and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

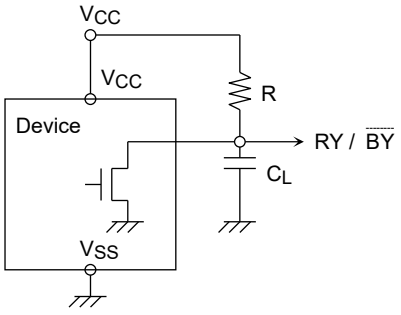
(8) Auto programming failure



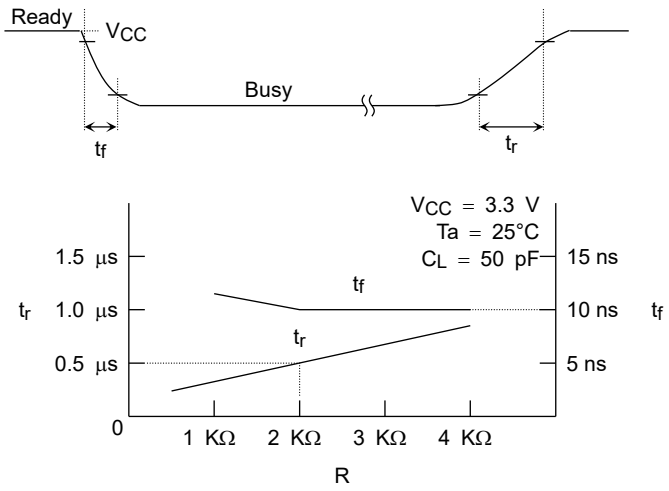
If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence. Because the previous input data has been lost in the Data Cache, the same input sequence of 80h command, address and data have to be executed.

(9) RY / $\overline{BY}$: termination for the Ready/Busy pin (RY / $\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY / $\overline{BY}$ buffer consists of an open drain circuit.



This data may vary from device to device. We recommend to use this data as a reference for selecting a resistor value.



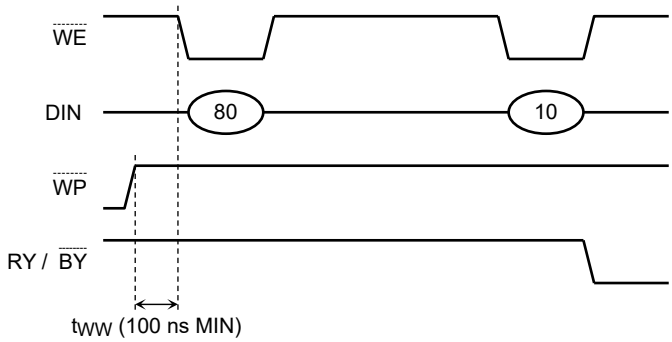
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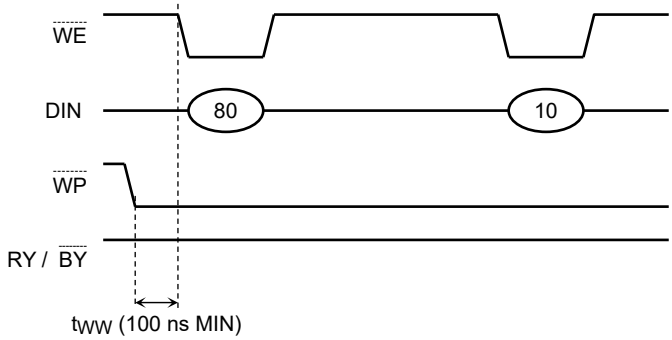
(10) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The operations are enabled and disabled as follows:

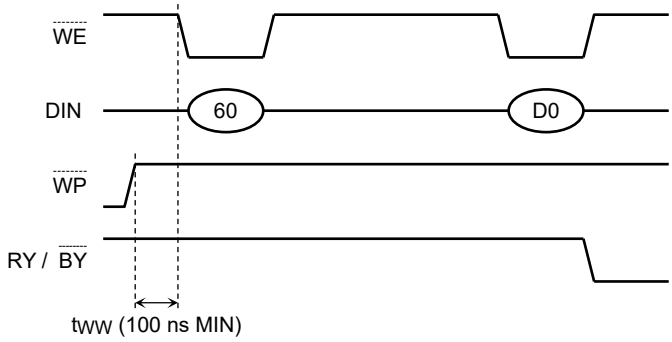
Enable Programming



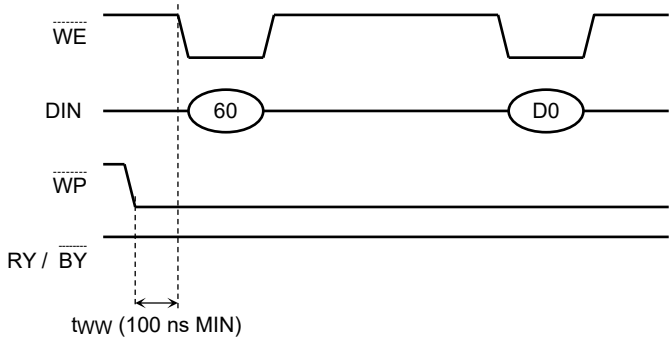
Disable Programming



Enable Erasing



Disable Erasing



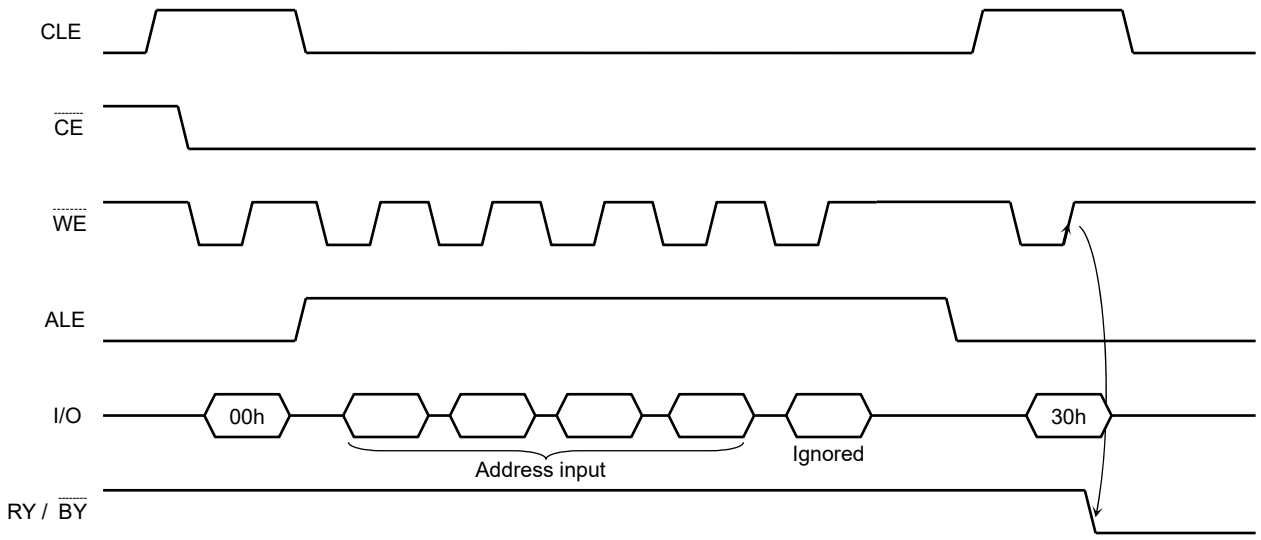
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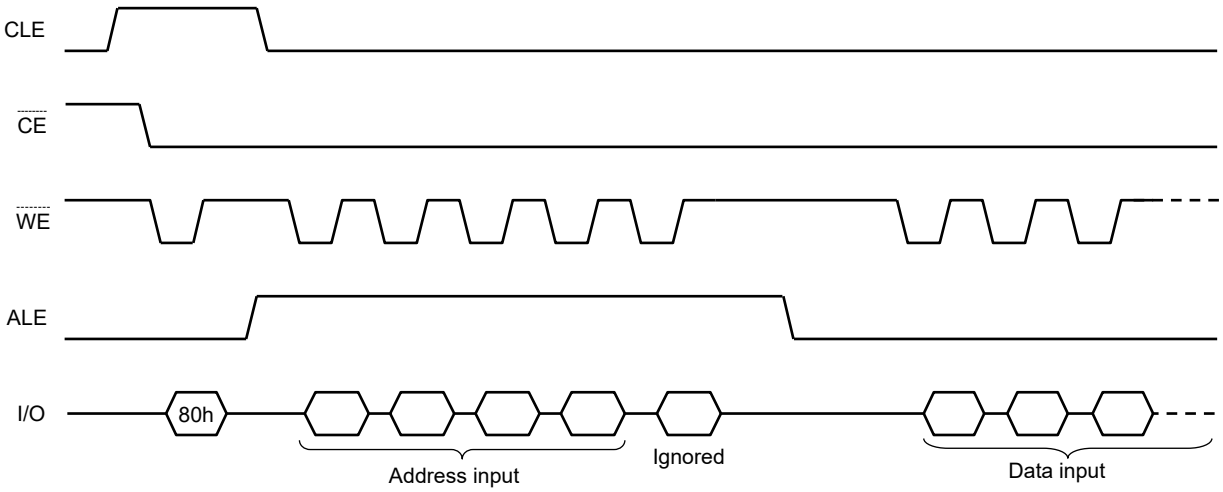
(11) When five address cycles are input

Although the device may read in a fifth address, it is ignored inside the chip.

Read operation



Program operation

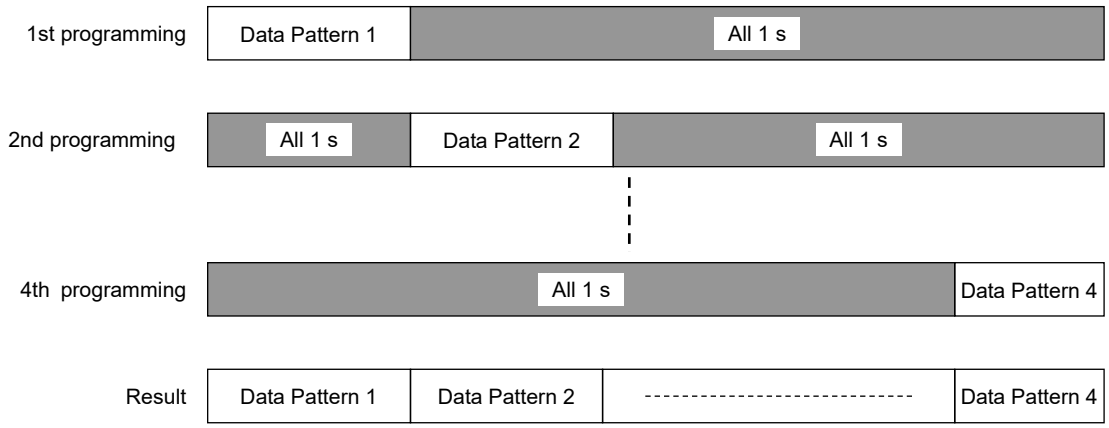


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(12) Several programming cycles on the same page (Partial Page Program)

Each segment can be programmed individually as follows:



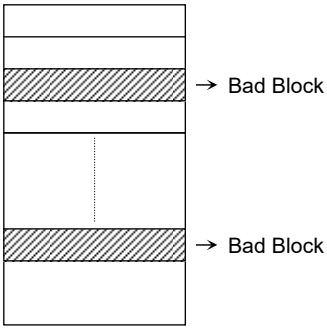
Number of partial program cycles in the same page must not exceed 4.

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(13) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block's information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

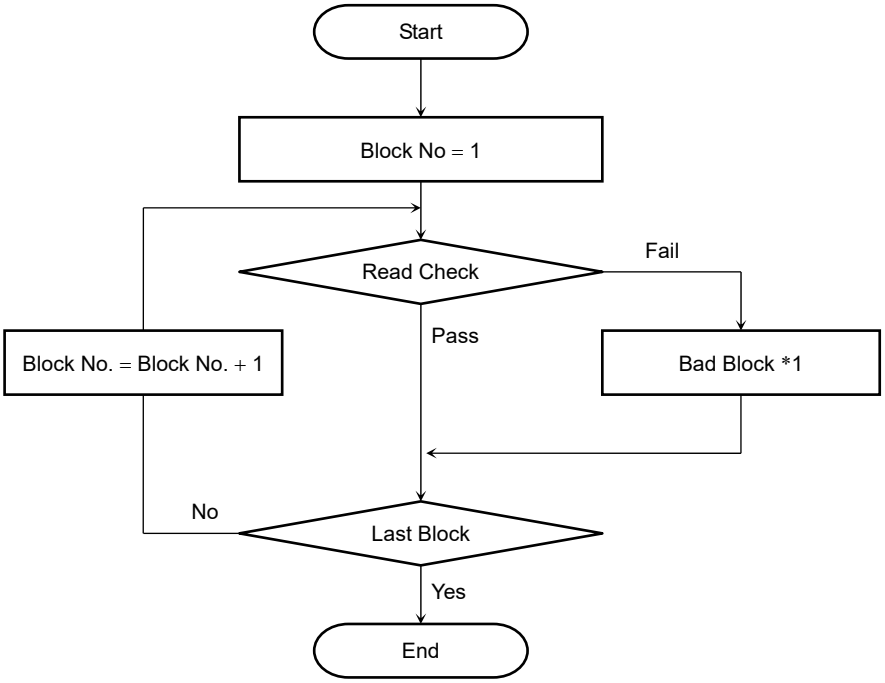
A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

The number of valid blocks over the device lifetime is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	1004	—	1024	Blocks

Bad Block Test Flow

Regarding invalid blocks, bad block mark is in whole pages.
Please read one column of any page in each block. If the data of the column is 00 (Hex), define the block as a bad block.



*1: No erase operation is allowed to detected bad blocks

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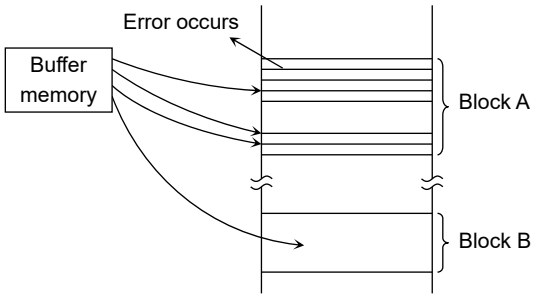
(14) Failure phenomena for Program, Erase and Read operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Read	Bit Error	Check the ECC status at host controller and take appropriate measures such as rewrite in consideration of Wear Leveling before uncorrectable ECC error occurs

- ECC: Error Correction Code. 8 bit correction per 512 Bytes is necessary.
- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (by creating a table within the system or by using another appropriate scheme).

(15) Do not turn off the power before the Write/Erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before the Write/Erase operation is complete will cause loss of data and/or damage to data.

(16) Please refer to KIOXIA soldering temperature profile for details.

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(17) Reliability Guidance

This reliability guidance is intended to provide some guidance related to using NAND Flash with 8 bit ECC for each 512 bytes. NAND Flash memory cells are gradually worn out and the reliability level of memory cells is degraded by repeating Write and Erase operation of '0' data in each block. For detailed reliability data, please refer to the reliability note for each product.
Although random bit errors may occur during use, it does not necessarily mean that a block is bad.
Generally, a block should be marked as bad when a program status failure or erase status failure is detected.
The reliability of NAND Flash memory cells during the actual usage on system level depends on the usage and environmental conditions. KIOXIA adopts the checker pattern data, 0x55 & 0xAA for alternative Write/Erase cycles, for the reliability test.

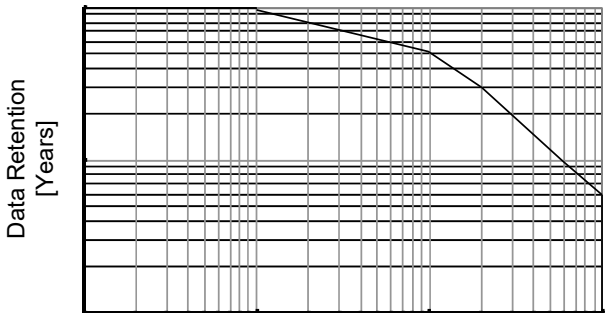
Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a Status Read after either an Auto Page Program or Auto Block Erase operation. The cumulative bad block count will increase along with the number of Write/Erase cycles.

Data Retention

The data in NAND Flash memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again. Data Retention time is generally influenced by the number of Write/Erase cycles and temperature.

Here is a graph plotting the relationship between Write/Erase Endurance and Data Retention.



Read Disturb

A Read operation may disturb the data in NAND Flash memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again. Read Disturb capability is generally influenced by the number of Write/Erase cycles.

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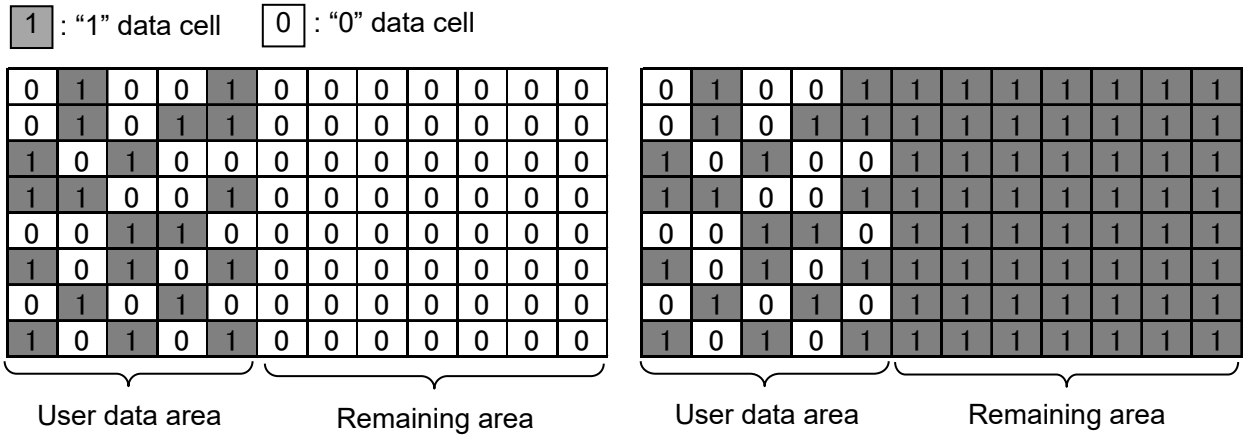
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(18) NAND Management

NAND Management such as Bad Block Management, ECC treatment and Wear Leveling, but not limited to these treatments, should be recognized and incorporated in the system design.
ECC treatment for read data is mandatory against random bit errors, and host should monitor ECC status to take appropriate measures such as rewrite in consideration of Wear Leveling before uncorrectable Error occurs. To realize robust system design generally it is necessary to prevent the concentration of Write/Erase cycles at the specific blocks by adopting Wear Leveling which manages to distribute Write/Erase cycles evenly among NAND Flash memory. And also it is necessary to avoid dummy '0' data write, e.g. '0' data padding, which accelerate block endurance degradation.

Continuous Write and Erase cycling with high percentage of '0' bits in data pattern can lead to faster block endurance degradation.

Example: NAND cell array with '0' data padding



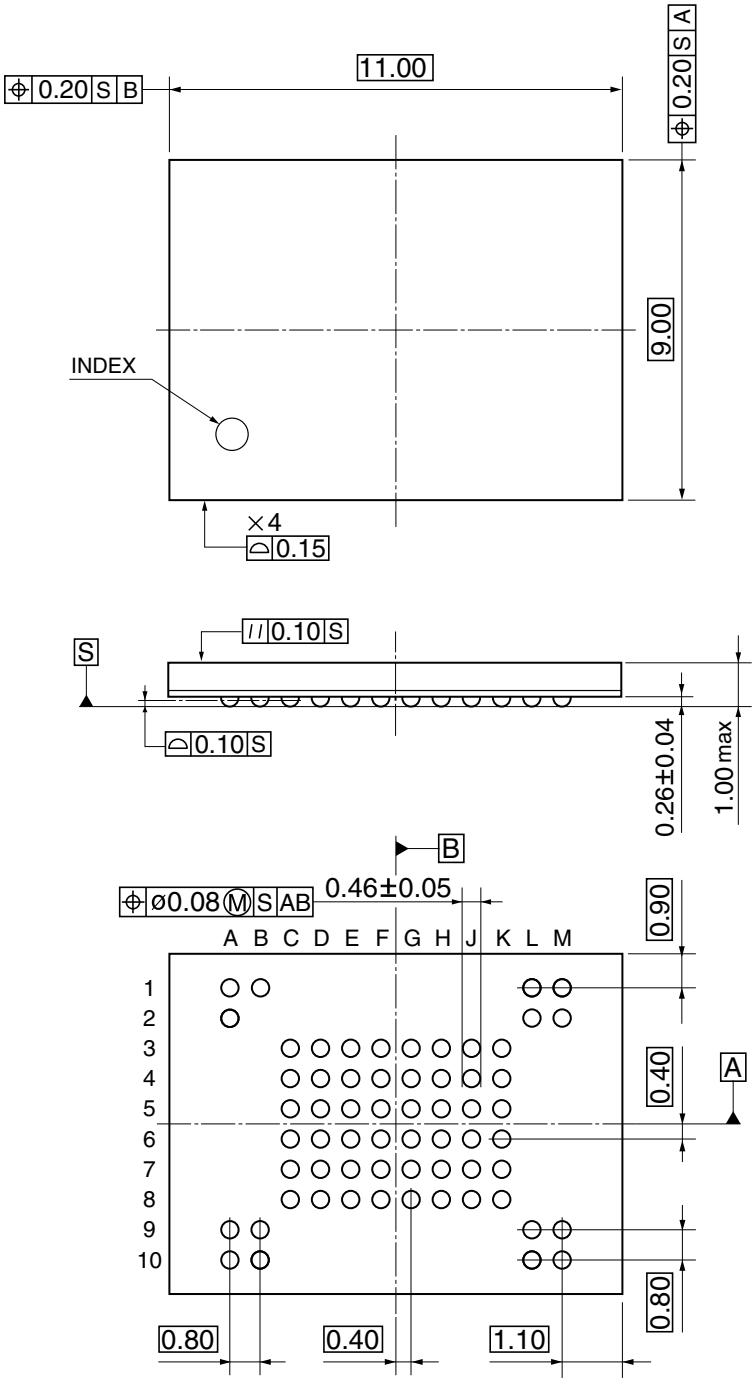
(a) Accelerate block endurance degradation by fixed dummy "0" data write

(b) "1" data for Remaining area (Recommended)

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Package Dimensions

P-TFBGA63-0911-0.80CZ Unit: mm



Weight: 0.15g (typ.)

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Revision History

Date	Rev.	Description
2012-06-15	0.10	Initial Release
2012-07-13	0.20	Described ECC bit number: 8, Changed tBERASE, Revised ID Table, Corrected typo.
2012-10-01	1.00	Deleted TENTATIVE/TBD notation.
2018-12-14	1.10	Corrected typo and described some notes. Removed Soldering Temperature and added note in ABSOLUTE MAXIMUM RATINGS, and added comments in APPLICATION NOTES AND COMMENTS. Removed the word “Recommended” from the title of DC OPERATING CONDITIONS and AC CHARACTERISTICS AND OPERATING CONDITIONS. Renewed Reliability Guidance and added NAND Management. Changed “RESTRICTIONS ON PRODUCT USE”.
2019-10-01	2.00	Rebrand as "KIOXIA"

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