KIOXIA
2Gb, 3.3V
Serial Interface NAND
Technical Data Sheet

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1. Introduction

1.1. General Description

The TC58CVG1S3HRAIG is a Serial Interface NAND Flash memory for embedded applications which supports the SPI interface. The TC58CVG1S3HRAIG is organized as (2048 + 64) bytes × 64 pages × 2048 blocks. The device has a 2112 byte data buffer which allows program and read data to be transferred between the buffer and the memory cell array in 2112-byte increments. The Erase operation is implemented in a single block unit (128 Kbytes + 4 Kbytes: 2112 bytes × 64 pages). The device has the high speed mode for sequential Page Read operation. When high speed mode is enabled, the average of t_R is shortened.
The TC58CVG1S3HRAIG has ECC logic on the chip and 8bit read errors for each (512 bytes + 16 bytes) can be corrected. The internal ECC logic has detailed Bit Flip Count Report.

1.2. Definitions and Abbreviations

SPI
Serial Peripheral Interface

Address
The address is comprised of a column address (CA) with 12 bits and a row address (RA) with 17 bits. The row address identifies the page and block to be accessed. The column address identifies the byte within a page to access.

Column
The byte location within the page

Row
Refer to the block and page to be accessed

Sector
The (512 bytes+16 bytes) unit in a page

Page
The smallest addressable unit for the Read and the Program operations

Block
Consists of multiple pages and is the smallest addressable unit for the Erase operation.

Data Buffer
Buffer used to transfer data to and from the cell array

Cell Array
Memory cells of NAND Flash

Device
The packaged NAND unit

ECC
Error Correction Code

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1.3. Features

- **Organization**

Organization (Internal ECC is enabled, default)

Memory Cell Array	2112 × 64 × 2048 × 8 bits
Data Buffer	2112 × 8 bits
Page Size	2112 bytes
Block Size	(128K + 4K) bytes

Organization (Internal ECC is disabled)

Memory Cell Array	2176 × 64 × 2048 × 8 bits
Data Buffer	2176 × 8 bits
Page Size	2176 bytes
Block Size	(128K + 8K) bytes

- **ECC**
  The device has ECC logic internally. When internal ECC is disabled, 8 bit ECC for each 512 bytes is required.

- **Mode**
  Page Read, Page Program, Block Erase, Internal Data Move, Reset, Write Enable, Write Disable, Block Lock, Get Feature, Set Feature, Block Protection, Parameter Page Read, Read ID, Unique ID Read.

- **Power Supply**
  V_{CC} = 2.7 V to 3.6 V

- **Access Time**

Cell Array to Data Buffer	155	μs max
	70	μs typ.
Data Transfer rate	104	MHz max

- **Program/Erase Time**

Programming Time	360	μs/page typ.
Block Erasing Time	2.0	ms/block typ.

- **Operating Current**

Read Operation Current with HSE ON (Average)	21	mA max
Read Operation Current with HSE OFF (Average)	15	mA max
Program Operation Current (Average)	18	mA max
Erase Operation Current (Average)	22	mA max
Standby Current	180	μA max
	35	μA typ.

- **Reliability**
  Refer to reliability note

- **Package**
  WSON8 (P-WSON8-0608-1.27-003) Weight: 0.12 g typ.

- **Part Numbering Information**
  TC58CVG1S3HRAIG 2Gb, 3.3V, WSON8 Serial Interface NAND

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2. Memory Organization

2.1. Pin Descriptions

Table 1 Pin Descriptions

Pin Name	Pin Function
$\overline{CS}$	Chip Select
SO/SO1	Serial Data Output / Serial Data Output 1
$\overline{WP}$/SO2	Write Protect / Serial Data Output 2
SI/SO0	Serial Data Input / Serial Data Output 0
$\overline{HOLD}$/SO3	Hold Input / Serial Data Output 3
SCK	Serial Clock Input
V_{CC}	Power Supply
V_{SS}	Ground

Note: If the $\overline{WP}$ pin is low and BRWD bit is set to 1, the overwriting for the BRWD (bit [7]) and the BL bits (bits [5:3]) in address A0h of the feature table shown in Table 12 is prohibited.
The users should keep the status of $\overline{WP}$ signal while $\overline{CS}$ pin is low.
The $\overline{HOLD}$ pin and the $\overline{WP}$ pin are pull up to V_{CC} internally.

2.2. Pin Assignment (Top View)

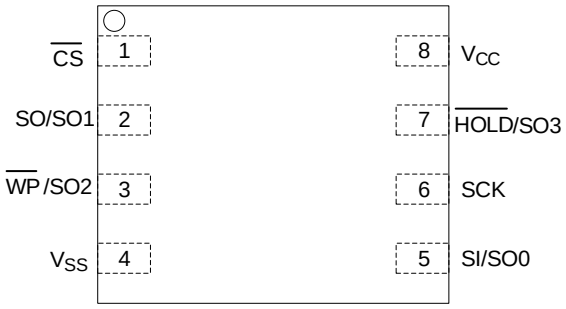


Figure 1. WSON8 Pin Assignment

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2.3. Block Diagram

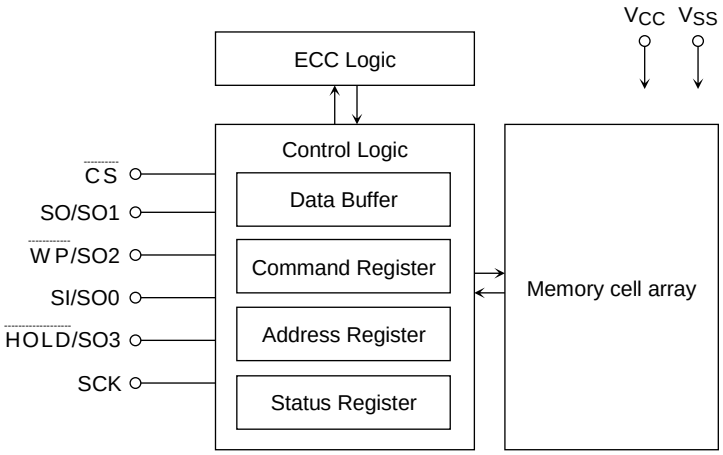


Figure 2. Block Diagram

2.4. Cell Layout

The Program operation works on page units while the Erase operation works on block units.
When internal ECC is turned ON, a page consists of 2112 bytes in which 2048 bytes are used for main memory storage and 64 bytes are used for redundancy or for other uses. When internal ECC is turned OFF, the redundancy area will be expanded to 128 bytes automatically.

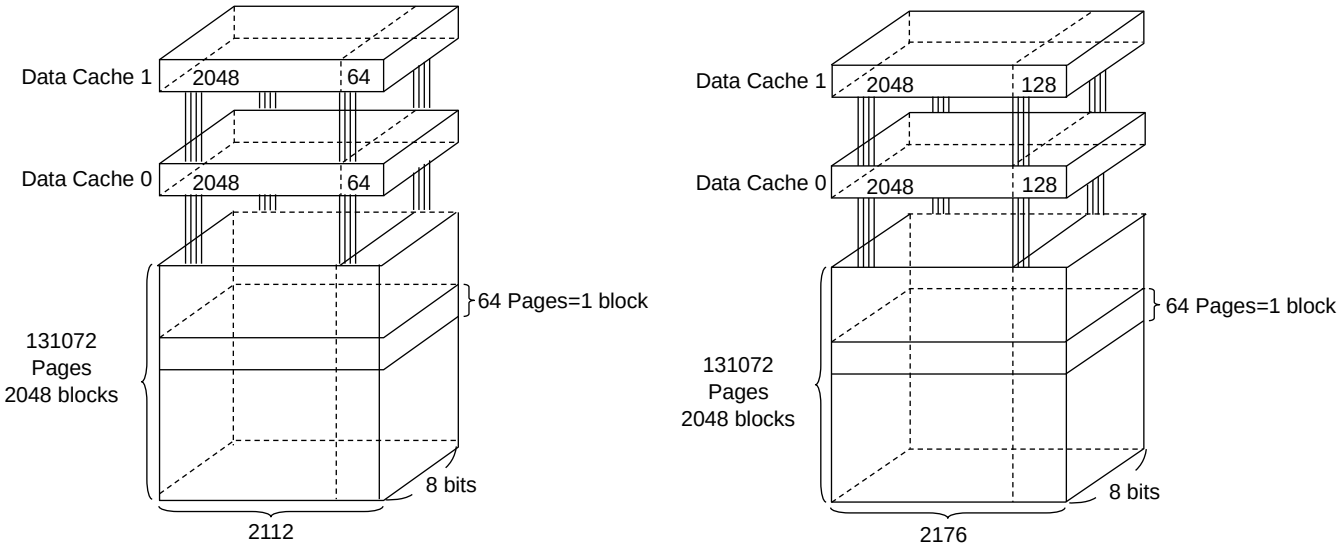


Figure 3. Cell Layout

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2.5. Addressing

There are two address types used; the column address and the row address. The column address is used to access bytes within a page. The row address is used to address pages and blocks. There are some operations that may require only row addresses, such as Block Erase.

Row Address (RA): 17 bits
Block Address (2048 blocks/device) : 11 bits
Page Address (64 pages/block) : 6 bits

Column Address (CA): 12 bits
Column Address (2112 or 2176 bytes/page) : 12 bits

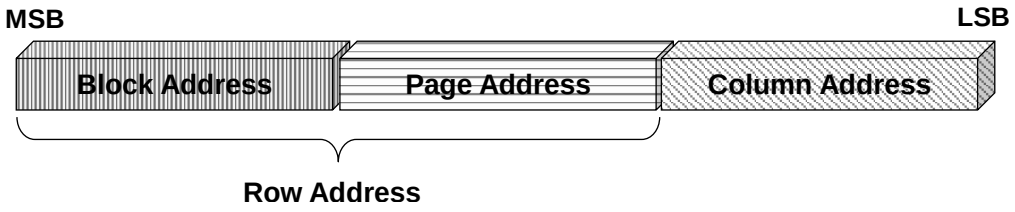


Figure 4. Addressing

2.6. Valid Blocks

Table 2 Valid Blocks

Symbol	Parameter	Min	Typ.	Max	Unit
N_{VB}	Number of Valid (Good) Blocks	2008	-	2048	Block

Note: The device occasionally contains unusable blocks.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over the lifetime.

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3. Physical Interface

3.1. Absolute Maximum Rating

Stresses greater than those listed in Table 3 may cause permanent damage to the device. This is a stress rating only.

Table 3 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	−0.3 to 3.9	V
V_{IN}	Input Voltage	−0.3 to V_{CC} + 0.3 (≤ 3.9 V)	V
$V_{I/O}$	Input / Output Voltage	−0.3 to V_{CC} + 0.3 (≤ 3.9 V)	V
P_{D1}	Power Dissipation 1	0.42	W
P_{D2}	Power Dissipation 2 (WSON8 ePAD without solder)	0.27	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55 to 150	°C
T_{OPR}	Operating Temperature	−40 to 85	°C

Note: Avoid locations where the device may be exposed to water (wet, rain, dew condensation, etc.)

3.2. Capacitance

Table 4 Capacitance (T_{OPR} = 25 °C, f = 1 MHz)

Symbol	Parameter	Condition	Min	Max	Unit
C_{IN}	Input	V_{IN} = 0 V	-	2.5	pF
C_{OUT}	Output	V_{OUT} = 0 V	-	4	pF

Note: This parameter is periodically sampled and is not tested for every device.

3.3. DC Operating Conditions

Table 5 DC Operating Condition

Symbol	Parameter	Min	Typ.	Max	Unit
V_{CC}	Power Supply Voltage	2.7	-	3.6	V
V_{IH}	High Level Input Voltage	V_{CC} × 0.8	-	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	−0.3	-	V_{CC} × 0.2	V

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3.4. Signal Timing

The device supports SPI mode 0 and mode 3. Input data is latched at the rising edge of SCK and data is output at the falling edge of SCK for mode 0 and 3. When $\overline{HOLD}$ goes Low, the communication is held. The hold state begins at the falling edge of SCK.

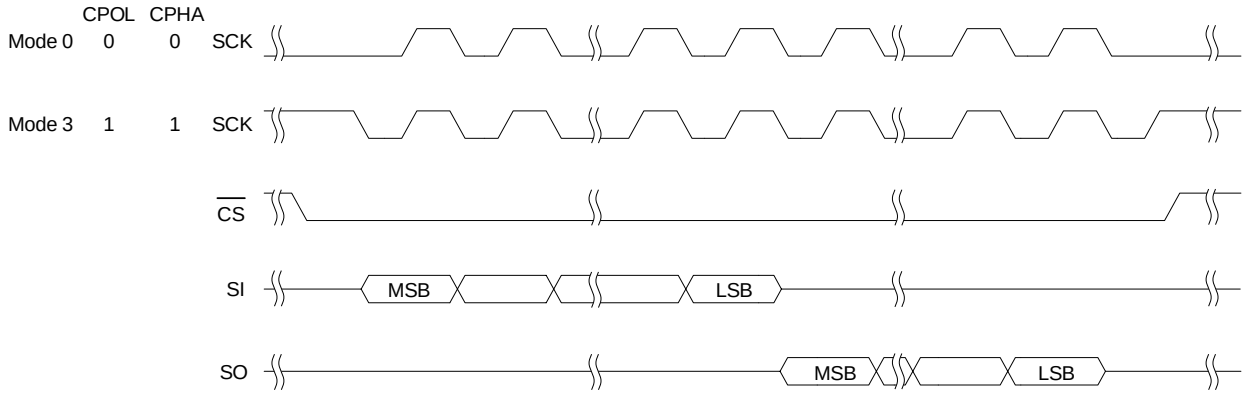


Figure 5. SPI Timing

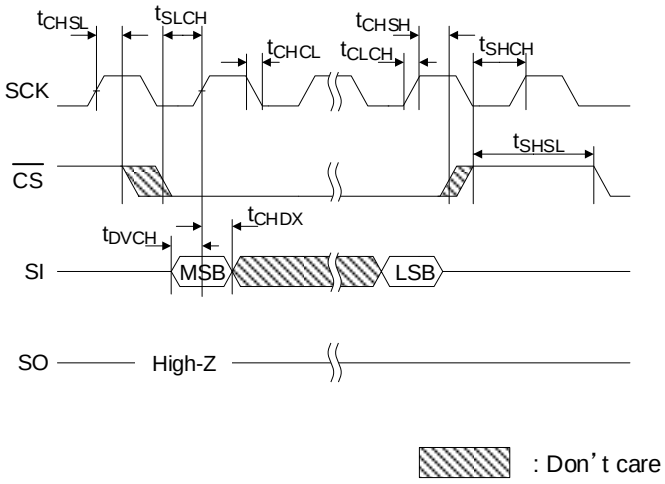


Figure 6. Serial Input Timing

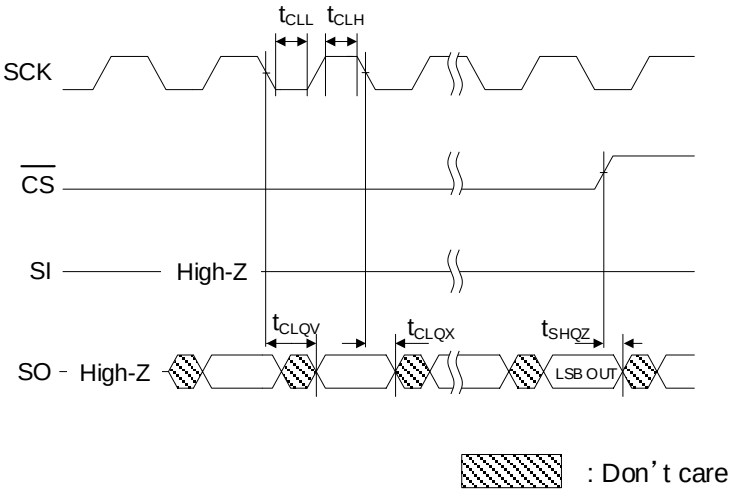


Figure 7. Serial Output Timing

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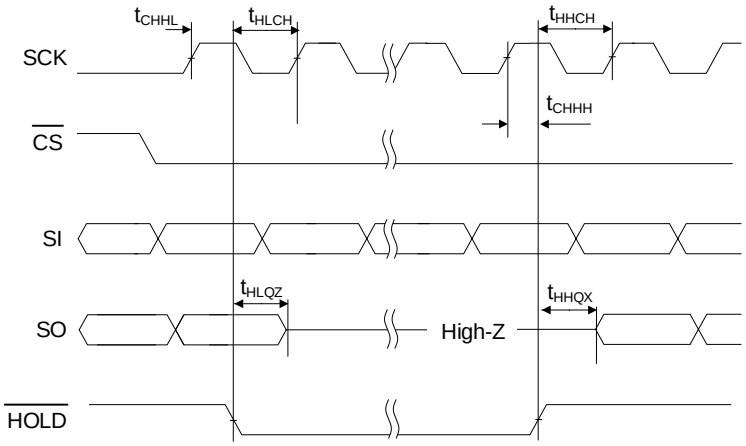


Figure 8. Hold Timing

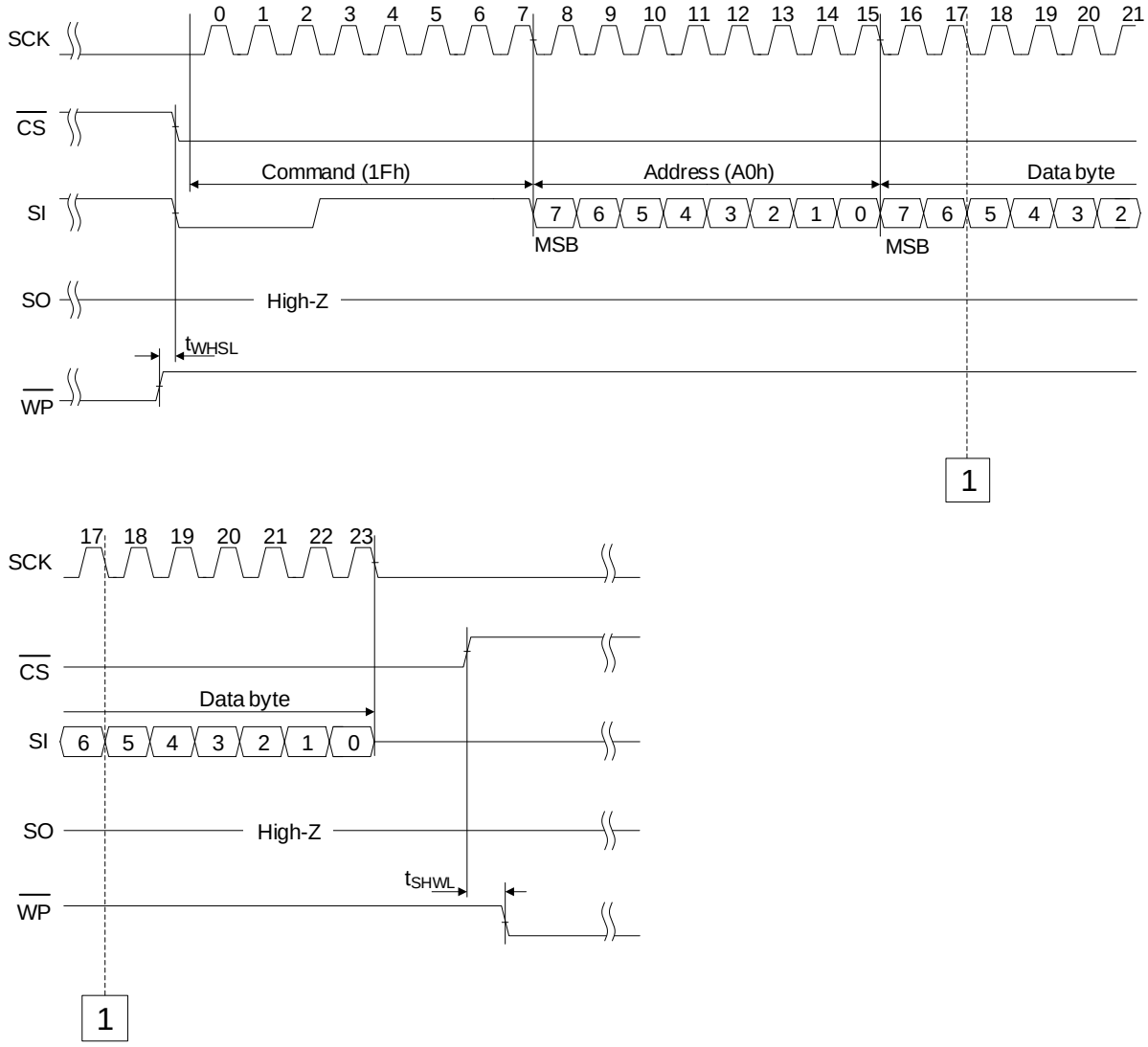


Figure 9. WP Timing (Example)

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3.5. AC Characteristics

Table 6 AC Characteristics (T_{OPR} = –40 to 85 °C, V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Min	Typ.	Max	Unit
F_C	Serial Clock Frequency for All Operations	-	-	104	MHz
t_{CLH}	Serial Clock High Time	4.5	-	-	ns
t_{CLL}	Serial Clock Low Time	4.5	-	-	ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1	-	-	V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1	-	-	V/ns
t_{SLCH}	$\overline{CS}$ Active Setup Time	4.6	-	-	ns
t_{CHSH}	$\overline{CS}$ Active Hold Time	5	-	-	ns
t_{SHCH}	$\overline{CS}$ Not Active Setup Time	5	-	-	ns
t_{CHSL}	$\overline{CS}$ Not Active Hold Time	5	-	-	ns
t_{SHSL}	$\overline{CS}$ High Time	100	-	-	ns
t_{SHQZ}	Output Disable Time	-	-	20	ns
t_{CLQX}	Output Hold Time	1	-	-	ns
t_{DVCH}	Data In Setup Time	2	-	-	ns
t_{CHDX}	Data In Hold Time	5	-	-	ns
t_{HLCH}	$\overline{HOLD}$ Low Setup Time (relative to Clock)	5	-	-	ns
t_{HHCH}	$\overline{HOLD}$ High Setup Time (relative to Clock)	5	-	-	ns
t_{CHHL}	$\overline{HOLD}$ High Hold Time (relative to Clock)	5	-	-	ns
t_{CHHH}	$\overline{HOLD}$ Low Hold Time (relative to Clock)	5	-	-	ns
t_{HLQZ}	$\overline{HOLD}$ Low to High-Z Output	-	-	7	ns
t_{HHQX}	$\overline{HOLD}$ High to Output	-	-	7	ns
t_{CLQV}	Clock Low to Output Valid	-	-	7.0 (C_L=10 pF) 7.5 (C_L=20 pF) 8.0 (C_L=30 pF)	ns
t_{WHSL}	$\overline{WP}$ Setup Time Before $\overline{CS}$ Low	20	-	-	ns
t_{SHWL}	$\overline{WP}$ Hold Time After $\overline{CS}$ High	100	-	-	ns

3.6. DC Operating Characteristics

Table 7 DC & Operating Characteristics (T_{OPR} = –40 to 85 °C, V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	-	-	±10	μA
I_{CCOA1}	Read Operation Current (Average)	F_C = 104 MHz High Speed Mode = Enable Read Buffer Command : 03h or 0Bh (x1)	-	-	21	mA
I_{CCOA2}	Read Operation Current (Average)	F_C = 104 MHz High Speed Mode = Disable Read Buffer Command : 03h or 0Bh (x1)	-	-	15	mA
I_{CCOA3}	Program Operation Current (Average)	F_C = 104 MHz	-	-	18	mA
I_{CCOA4}	Erase Operation Current (Average)	F_C = 104 MHz	-	-	22	mA
I_{CCS}	Standby Current	$\overline{CS}$= V_{CC} – 0.2 V, $\overline{WP}$ = V_{CC}, $\overline{HOLD}$ = V_{CC}	-	35	180	μA
V_{OH}	High Level Output Voltage	I_{OH} = –0.1 mA	V_{CC} – 0.2	-	-	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1 mA	-	-	0.2	V

Note: Refer to the High Speed Mode in 4.3. Page Read Operation - High Speed Mode.

I_{CCOA1} to I_{CCOA4} are the average current during the full operation sequence.

Typ. values reflect values obtained in specific test environments under typical test parameters. Actual results will vary based on the conditions and environment in which the part is used.

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3.7. Programming, Reading and Erasing Characteristics

Table 8 Programming, Reading and Erasing Characteristics (T_{OPR} = –40 to 85 °C, V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Min	Typ.	Max	Unit
t_{PROG}	Programming Time (with ECC)	-	360	500	µs
N	Number of Partial Program Cycles in the Same Page	-	-	4	times
t_{BERASE}	Block Erasing Time	-	2	7	ms
t_R	Cell Array to the Buffer (with ECC) (High Speed Mode = Disable)	-	70	155	µs
t_{RHSA4}	Average Read Time for Sequential Read (with ECC) (High Speed Mode = Enable, Read Buffer x4)	-	30	-	µs
t_{RST}	Device Reset Time (Read)	-	-	155	µs
	Device Reset Time (Program)	-	-	500	µs
	Device Reset Time (Erase)	-	-	7	ms

Note: Refer to the data pair of ECC calculation in 4.16. Internal ECC.
Refer to the High Speed Mode in 4.3. Page Read Operation - High Speed Mode.
t_R is the average busy time for page read operation of 64pages continuously in a block.
t_{RHSA4} is the average busy time for sequential page read operation with all data output in each page of 64 pages continuously in a block.
The busy time after Protect Execute command is shorter than t_{PROG} (max).
Typ. values reflect values obtained in specific test environments under typical test parameters. Actual results will vary based on the conditions and environment in which the part is used.

3.8. Power ON/OFF Sequence

The timing sequence shown in the figure below is necessary for the power ON/OFF sequence.
The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. The users cannot issue any commands while t_{VSL}. From the end of t_{VSL} to the end of t_{VOP}, Get Feature operation and Reset operation can be issued. OIP bit in the feature table indicates the busy state in this time period. All operations are available after t_{VOP}.

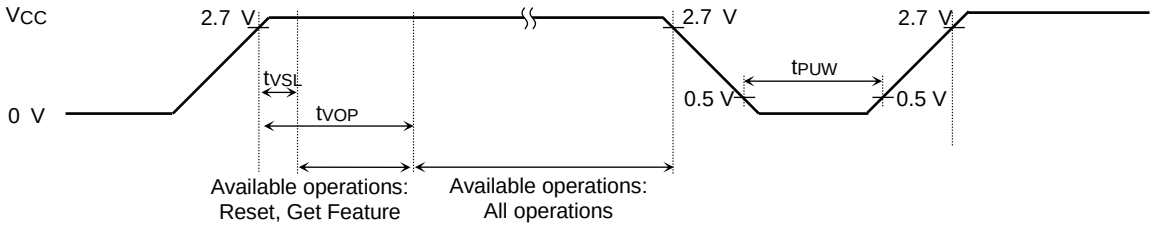


Figure 10. Power ON/OFF Timing

Table 9 Power on Timing

Symbol	Parameter	Min	Max	Unit
t_{VSL}	V_{CC}(min) to $\overline{CS}$ Low	-	100	µs
t_{VOP}	V_{CC}(min) to all operation	-	1.1	ms
t_{PUW}	Waiting time for power on	1	-	ms
V_{CCSR}	V_{CC} Slew Rate	-	216	mV/µs

3.9. AC Test Condition

Table 10 AC Test Condition

Parameter	Condition
	V_{CC}: 2.7 to 3.6 V
Input level	V_{CC} × 0.2 to V_{CC} × 0.8
Input pulse rise and fall time	2 ns
Input comparison level	V_{CC} / 2
Output data comparison level	V_{CC} / 2
Output load	C_L (30 pF) + 1 TTL

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4. Command Description and Device Operation

4.1. Command Set

Table 11 Command Set

Operation	Byte 1 (CMD)	Byte 2	Byte 3	Byte 4	Byte 5	Byte N
Read Cell Array	13h	Dummy + RA16 (Input)	RA15-RA8 (Input)	RA7-RA0 (Input)	-	-
Read Buffer	03h / 0Bh	Dummy + CA11-CA8 (Input)	CA7-CA0 (Input)	Dummy	D*-D* (Output)	D*-D* (Output)
Read Buffer x2	3Bh	Dummy + CA11-CA8 (Input)	CA7-CA0 (Input)	Dummy	D*-D* (Output)	D*-D* (Output)
Read Buffer x4	6Bh	Dummy + CA11-CA8 (Input)	CA7-CA0 (Input)	Dummy	D*-D* (Output)	D*-D* (Output)
Program Load	02h	Dummy + CA11-CA8 (Input)	CA7-CA0 (Input)	D*-D* (Input)	D*-D* (Input)	D*-D* (Input)
Program Execute	10h	Dummy+ RA16 (Input)	RA15-RA8 (Input)	RA7-RA0 (Input)	-	-
Protect Execute	2Ah	Dummy+ RA16 (Input)	RA15-RA8 (Input)	RA7-RA0 (Input)	-	-
Program Load Random Data	84h	Dummy + CA11-CA8 (Input)	CA7-CA0 (Input)	D*-D* (Input)	D*-D* (Input)	D*-D* (Input)
Block Erase	D8h	Dummy+ RA16 (Input)	RA15-RA8 (Input)	RA7-RA0 (Input)	-	-
Reset	FFh / FEh	-	-	-	-	-
Write Enable	06h	-	-	-	-	-
Write Disable	04h	-	-	-	-	-
Get Feature	0Fh	A7-A0 (Input)	D7-D0 (Output)	D7-D0 (Output)	D7-D0 (Output)	D7-D0 (Output)
Set Feature	1Fh	A7-A0 (Input)	D7-D0 (Input)	-	-	-
Read ID	9Fh	Dummy	ID Byte 0 (Output)	ID Byte 1 (Output)	Reserved (Output)	Reserved (Output)

Note: 1) Input of a command other than those specified in Table 11 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

2) During the operation in progress, do not input any command except 0Fh, FFh and FEh.

3) The users can issue the Protect Execute (2Ah) only one time for each block.

4) Once the Get Feature command is issued, the status and setting information are output continuously.

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4.2. Page Read Operation

The Read Cell Array and Read Buffer commands are required to read the data in a page. The Read Cell Array command reads the page data from the NAND cell array to the data buffer. The Read Buffer command reads the data from the data buffer. The operation sequence is as follows.

1. Read Cell Array (13h) : To read the data from the cell array to the internal data buffer
2. Get Feature (0Fh) : To read the status (OIP, ECCS0 and ECCS1 bits) of the device
3. Read Buffer (03h or 0Bh) : To output the data from the internal data buffer
   or Read Buffer x2 (3Bh)
   or Read Buffer x4 (6Bh)

Read Buffer, Read Buffer x2, Read Buffer x4 and Get Feature commands are repeatable commands.

For the Read Buffer x2 and Read Buffer x4 read modes are available as shown in Figure 13 and Figure 14.

The users are able to check the detailed bit flip count using ECC Bit Flip Count Detection and other functions using Get Feature command.

4.2.1. Read Cell Array (13h)

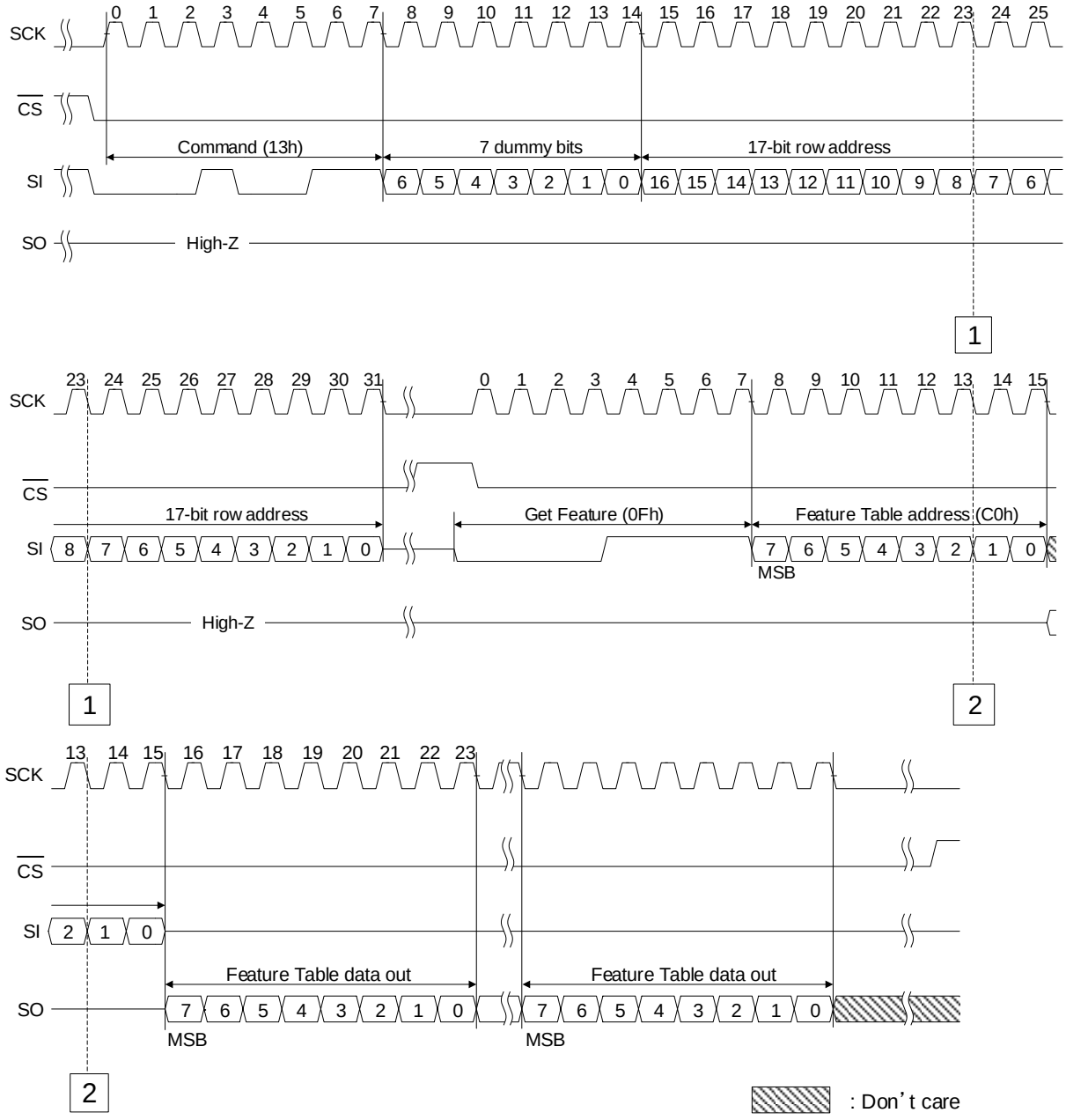
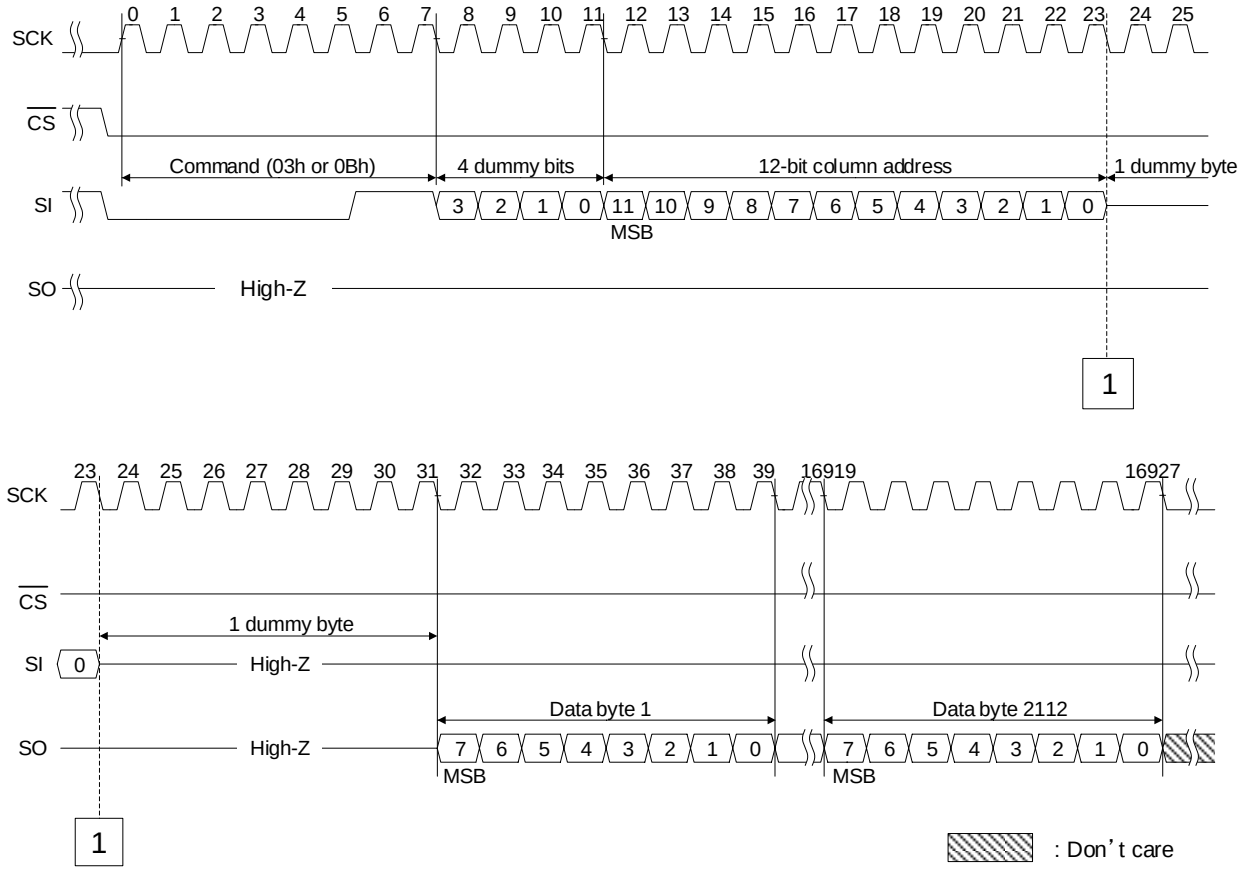


Figure 11. Page Read from Cell Array to Buffer

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4.2.2. Read Buffer (03h or 0Bh)

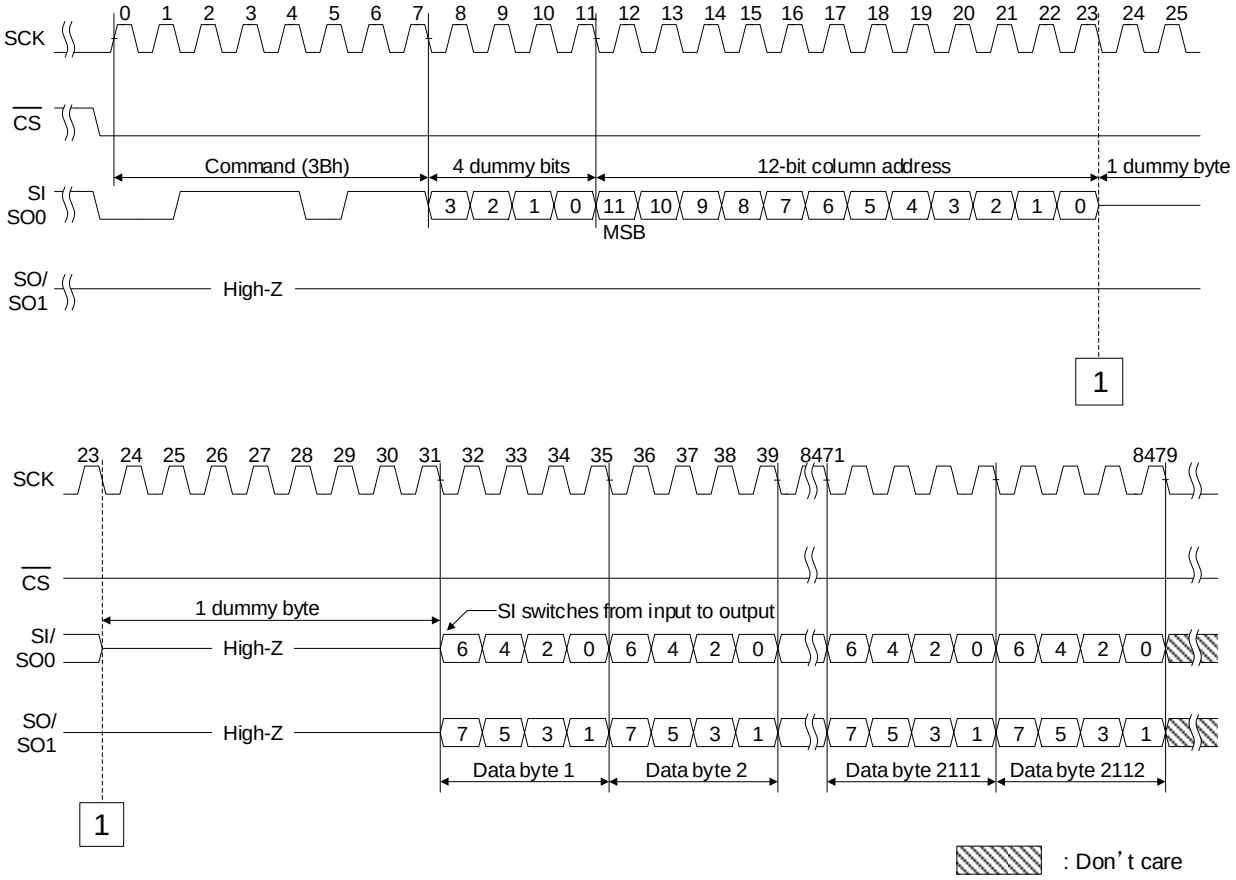


Note: When internal ECC is turned OFF, the maximum output data size is 2176 Bytes.

Figure 12. Page Read from Buffer Timing

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4.2.3. Read Buffer x2 (3Bh)



Note: When internal ECC is turned OFF, the maximum output data size is 2176 Bytes.

Figure 13. Page Read from Buffer x2 Timing

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4.2.4. Read Buffer x4 (6Bh)

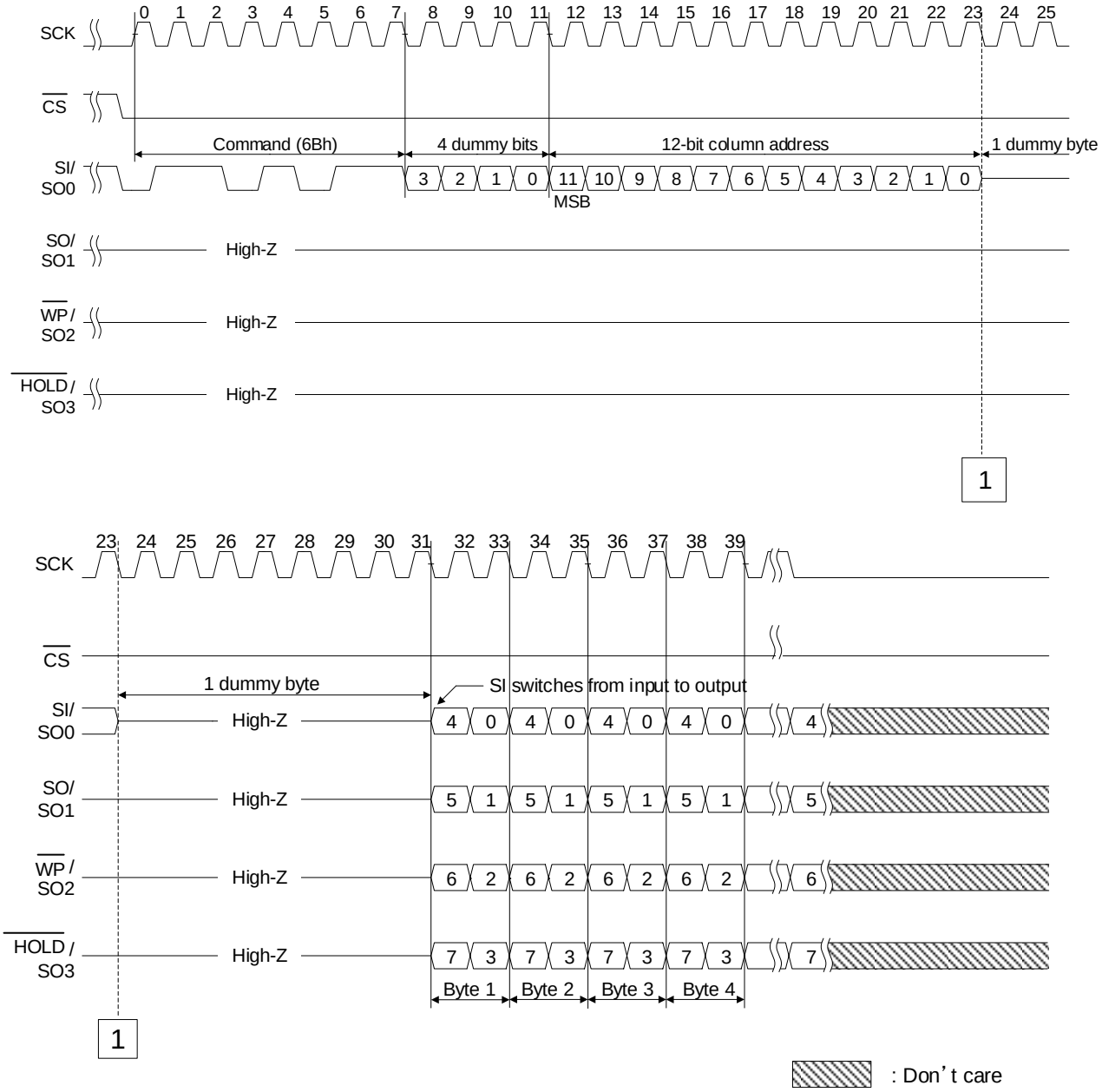


Figure 14. Page Read from Buffer x4 Timing

4.3. Page Read Operation - High Speed Mode

The device has a high speed mode for sequential read operation. When high speed mode is enabled, the average t_R is shortened. The command sequence is the same as the Page Read operation. The users set or clear the HSE bit which enables or disables the high speed mode in the feature table as shown in Table 12. High speed mode is enabled (HSE bit is set to 1) in the default condition. When the users switching the HSE bit, the users have to issue the Set Feature command just before the Read Cell Array (13h) command.
When the users use the random page read, the recommended setting of the HSE bit is 0 (disable) since t_R becomes longer.

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4.4. Page Program Operation

The Program Load and Program Execute commands are required to program data to a page. The Program Load command transfers data to the buffer. The unit of data transfer is a byte. The Program Execute command programs data from the buffer to the cell array. The operation sequence is as follows.

1. Write Enable (06h) : To enable the Program operation
2. Program Load (02h) : To transfer data to the internal data buffer
3. Program Execute (10h) : To program data from the buffer to the cell array
4. Get Feature (0Fh) : To read the status (OIP and PRG_F bits) of the device

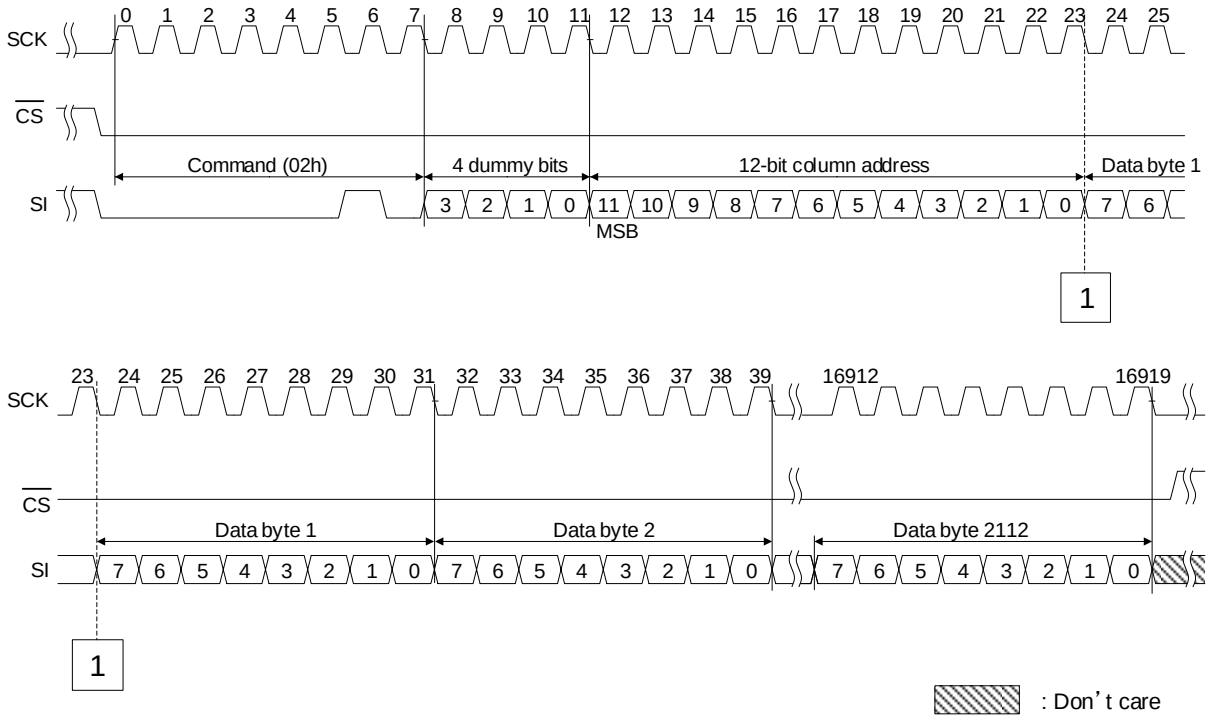
The internal data buffer is cleared by the Program Load command.

The Program Load Random Data (84h) command is also available to transfer data to the internal buffer. The users issue Program Load Random Data and the column address before the Program Execute (10h). The operation sequence is as follows.

1. Write Enable (06h) : To enable the Program operation
2. Program Load (02h) : To transfer data to the internal data buffer
3. Program Load Random Data (84h) : To transfer data to the internal data buffer
4. Program Execute (10h) : To program data from the buffer to the cell array
5. Get Feature (0Fh) : To read the status (OIP and PRG_F bits) of the device

Program Load Random Data and Get Feature commands are repeatable command.
The internal data buffer is not cleared by the Program Load Random Data command.

4.4.1. Program Load (02h)



Note: When internal ECC is turned OFF, the maximum input data size is 2176 Bytes.

Figure 15. Program Load

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4.4.2. Program Execute (10h)

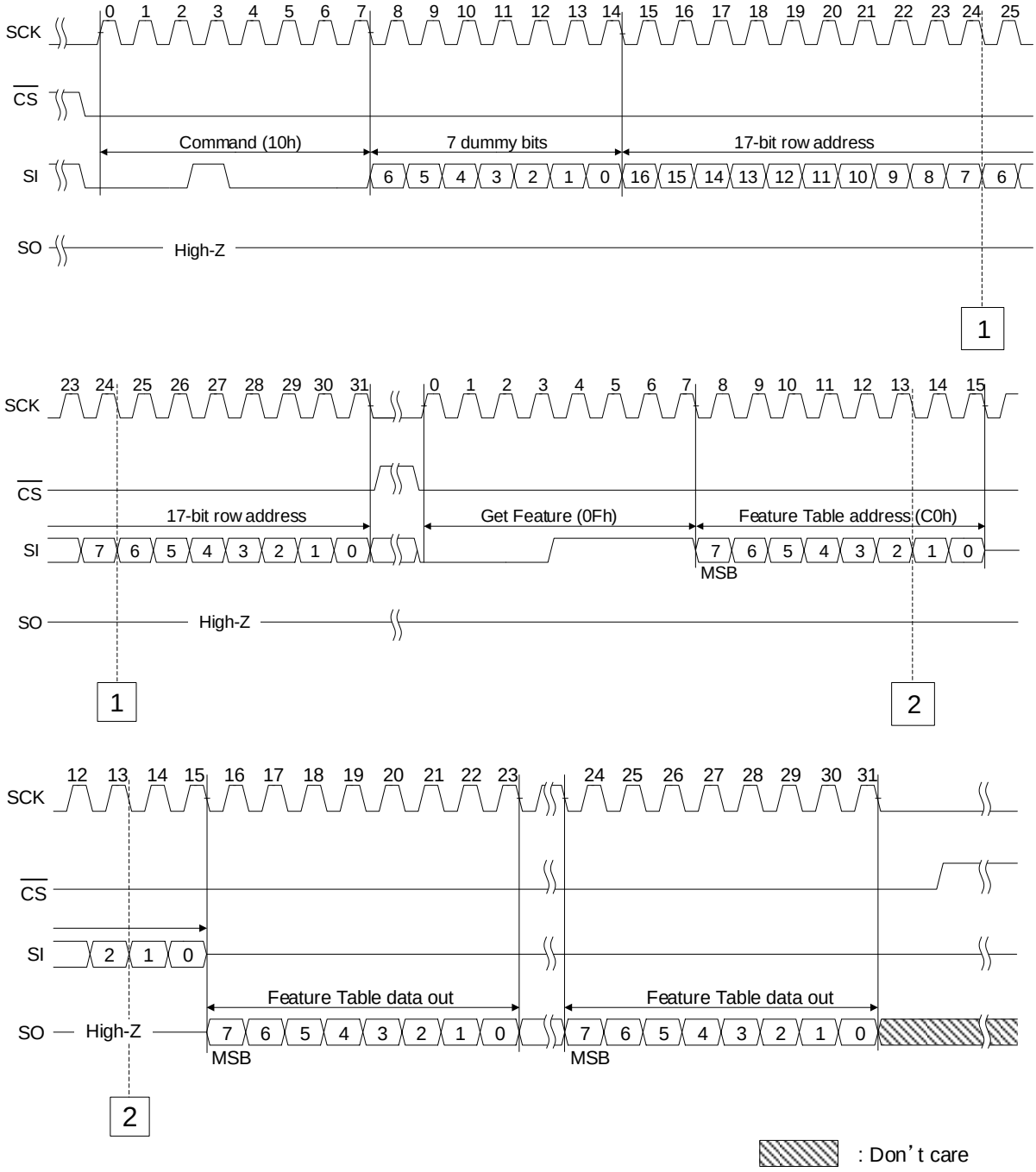
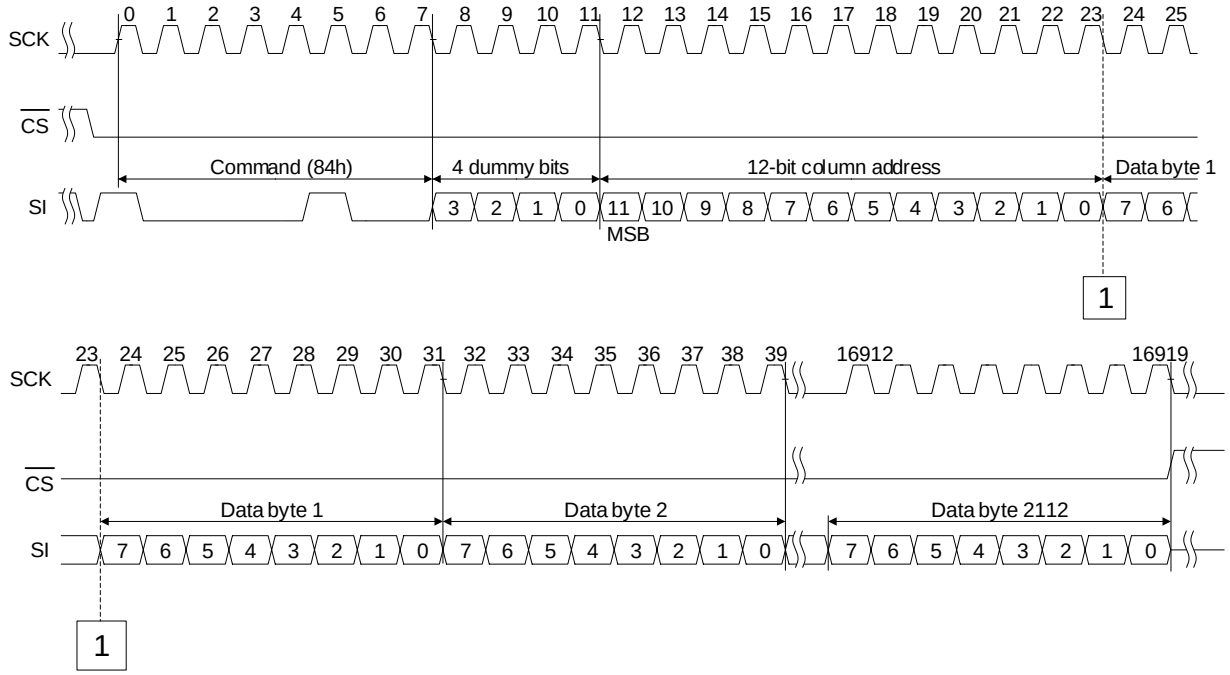


Figure 16. Program Execute Timing

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4.4.3. Program Load Random Data (84h)



Note: When internal ECC is turned OFF, the maximum input data size is 2176 Bytes.

Figure 17. Program Load Random Data Timing

4.5. Internal Data Move Operation

The Internal Data Move Operation is used to change the data in a page without data output. Before using this operation, the users must disable the Page Read High Speed Mode. The operation sequence is as follows.

1. Set Feature (1Fh) : To disable Page Read High Speed Mode
2. Read Cell Array (13h) : To read data from the cell array to internal buffer
3. Get Feature (0Fh) : To read the status (OIP, ECCS0 and ECCS1 bits) of the device
4. Write Enable (06h) : To enable the write
5. Program Load Random Data (84h) : To change the data in the internal buffer
6. Program Execute (10h) : To program data from the buffer to the cell array
7. Get Feature (0Fh) : To read the status (OIP, PRG_F bits) of the device

Program Load Random Data and Get Feature commands are repeatable command.
The status of the internal ECC depends on ECC_E bit in the feature table. When internal ECC is disabled, bit flips are not managed by the device.

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4.6. Block Erase (D8h)

The Block Erase operation erases the selected block. The page address is ignored automatically. The operation sequence is as follows.

1. Write Enable (06h) : To enable the Erase operation
2. Block Erase (D8h) : To erase data in the block
3. Get Feature (0Fh) : To read the status (OIP and ERS_F bits) of the device

Get Feature command is repeatable command.

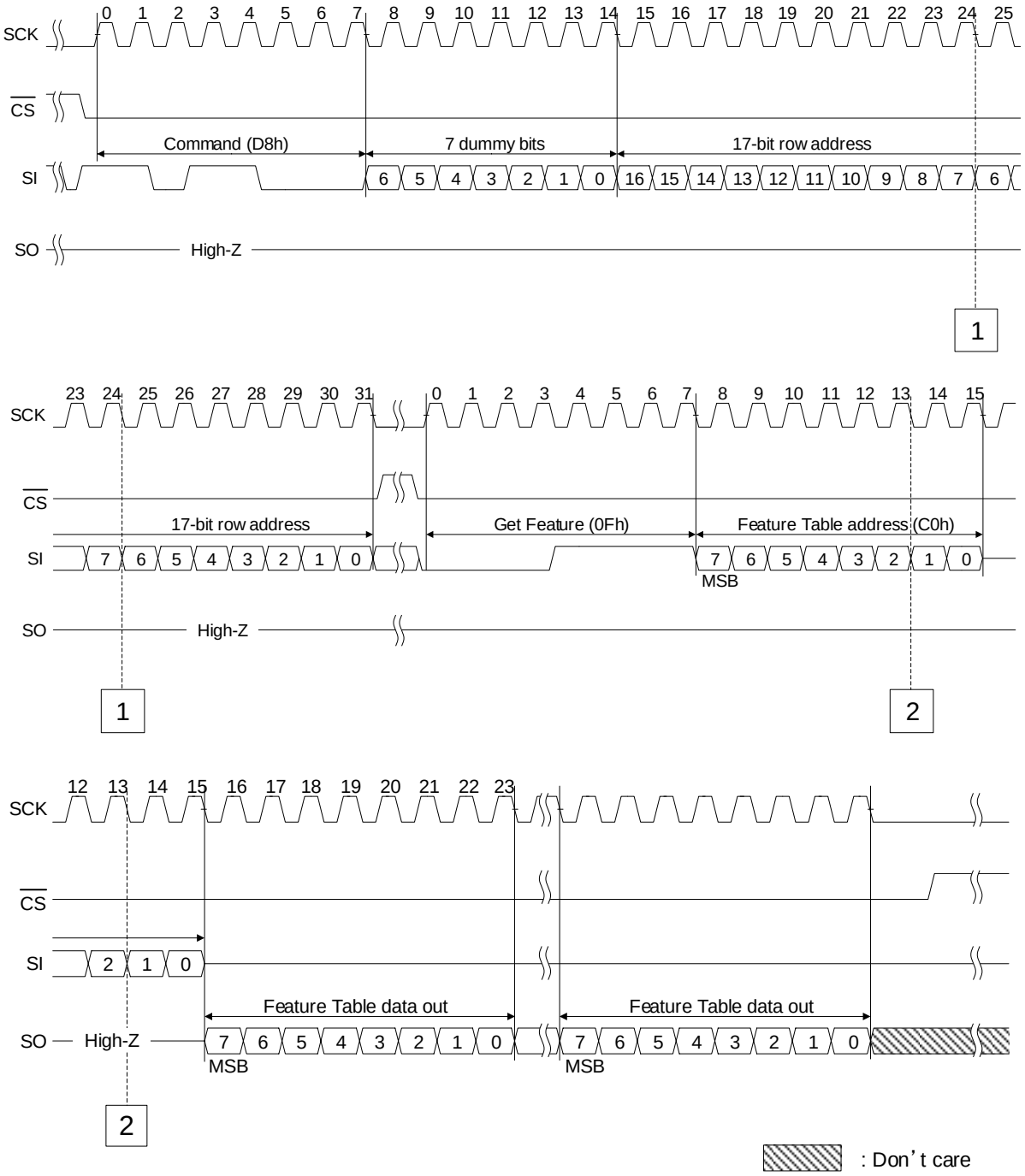


Figure 18. Block Erase Timing

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4.7. Reset (FFh or FEh)

The device offers Reset operation by command FFh or FEh. For example, in case of a Program or Erase operation, the internally generated voltage is discharged and the device enters the busy state. The operation sequence is as follows.

1. Reset (FFh or FEh) : To reset the device
2. Get Feature (0Fh) : To read the status of the device

Get Feature command is repeatable command.

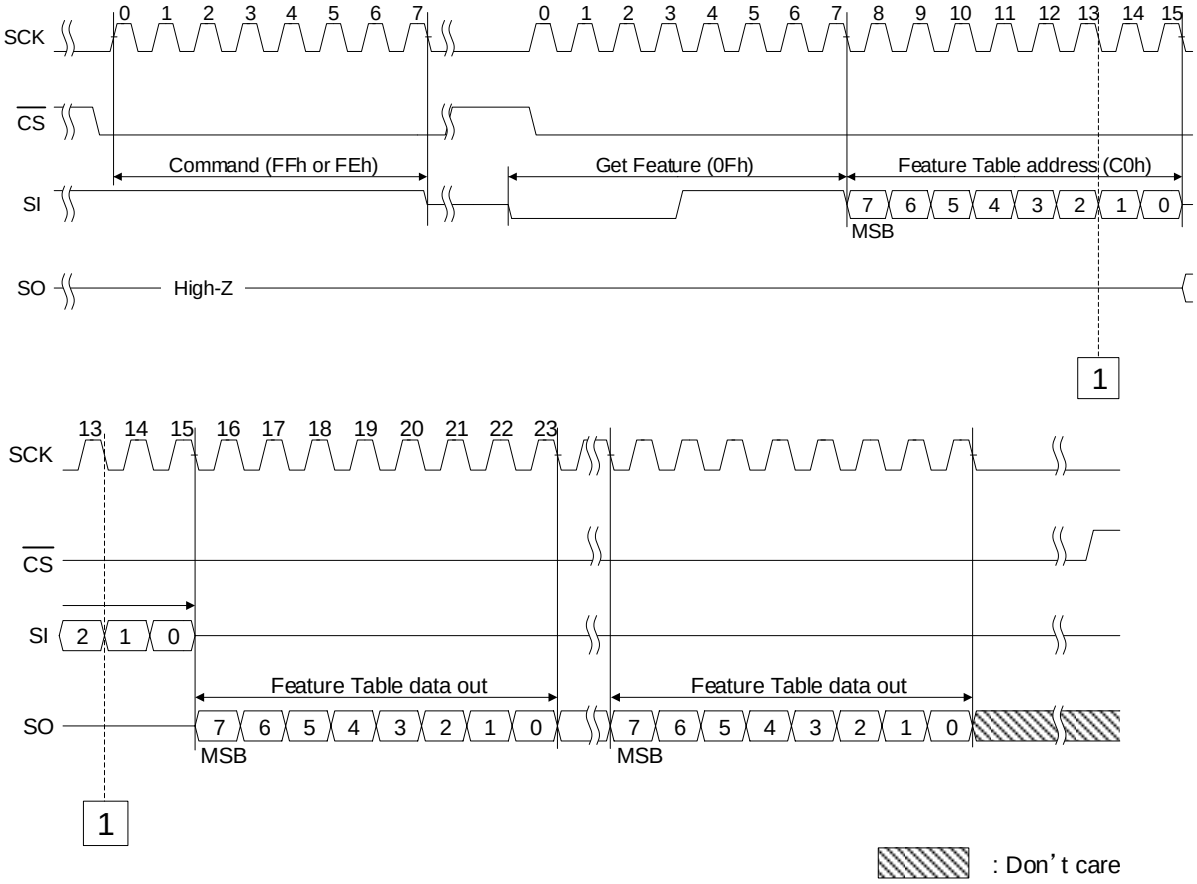


Figure 19. Reset Timing

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4.8. Write Enable (06h) / Write Disable (04h)

The Write Enable/Disable commands set or reset the WEL (Write Enable Latch) bit in the feature table shown in Table 12. The Write Enable command sets the WEL bit to 1. The Write Enable command must be issued before the Page Program, Block Protection and Block Erase operations. The Write Disable command clears the WEL bit to 0. If the WEL bit is cleared, Page Program, Block Protection and Block Erase commands are ignored by the device.

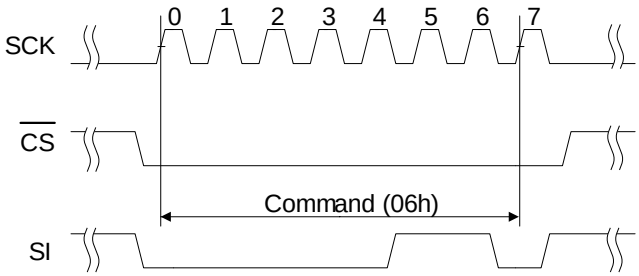


Figure 20. Write Enable Timing

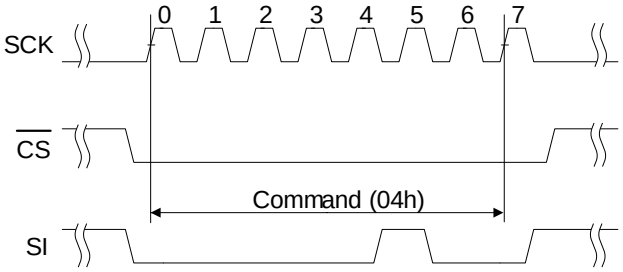


Figure 21. Write Disable Timing

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4.9. Set Feature (1Fh) / Get Feature (0Fh)

The users set individual features using the Set Feature operation and get feature settings or status of the device using the Get Feature operation. Feature settings and status are shown in Table 12. Refer to other sections for the details of each setting and status. When a feature is set once by the Set Feature command, the device keeps the bit until power OFF even if a Reset (FFh or FEh) command is issued.

Table 12 Feature Table

Address	Bit							
	7	6	5	4	3	2	1	0
A0h	BRWD (R/W)	Reserved	BL2 (R/W)	BL1 (R/W)	BL0 (R/W)	Reserved	Reserved	Reserved
B0h	PRT_E (R/W)	IDR_E (R/W)	Reserved	ECC_E (R/W)	Reserved	BBI (R)	HSE (R/W)	Reserved
C0h	Reserved	Reserved	ECCS1 (R)	ECCS0 (R)	PRG_F (R)	ERS_F (R)	WEL (R/W)	OIP (R)
10h	BFD3 (R/W)	BFD2 (R/W)	BFD1 (R/W)	BFD0 (R/W)	Reserved	Reserved	Reserved	Reserved
20h	Reserved	Reserved	Reserved	Reserved	BFS3 (R)	BFS2 (R)	BFS1 (R)	BFS0 (R)
30h	MBF3 (R)	MBF2 (R)	MBF1 (R)	MBF0 (R)	Reserved	MFS2 (R)	MFS1 (R)	MFS0 (R)
40h	BFR7 (R)	BFR6 (R)	BFR5 (R)	BFR4 (R)	BFR3 (R)	BFR2 (R)	BFR1 (R)	BFR0 (R)
50h	BFR15 (R)	BFR14 (R)	BFR13 (R)	BFR12 (R)	BFR11 (R)	BFR10 (R)	BFR9 (R)	BFR8 (R)

Note: (R/W): Read / Write, (R): Read only

The users must use the Write Enable (06h) or the Write Disable (04h) command to switch the WEL bit since Set Feature command cannot change it.

The value of Reserved bits in Feature Table is 0.

The access to any unknown address which is not defined in this Feature Table is not allowed.

The bits in Feature Table which are related to ECC functions become valid when the Internal ECC is turned on by the setting of ECC_E bit (bit [4]) in address B0h.

All the bits in Feature Table will be back to the default value after the power on sequence.

Table 13 Feature Table - A0h Address Description

Bit	Symbol	Parameter	Read / Write	Description
7	BRWD	Block Register Write Disable	R/W	When $\overline{WP}$ pin is Low and BRWD is set to 1, over write for BRWD and BL bits are prohibit. 1b: Disable 0b: Enable (Default)
6	Reserved	-	-	Reserved
5	BL2	Block Lock 2	R/W	The users set the locked blocks as entire of device or portion of device using the BL bits. 000b: All Unlocked 001b: Upper 1/64 Locked 010b: Upper 1/32 Locked 011b: Upper 1/16 Locked 100b: Upper 1/8 Locked 101b: Upper 1/4 Locked 110b: Upper 1/2 Locked 111b: All Locked (Default)
4	BL1	Block Lock 1	R/W	
3	BL0	Block Lock 0	R/W	
2	Reserved	-	-	Reserved
1	Reserved	-	-	Reserved
0	Reserved	-	-	Reserved

Note: (R/W): Read / Write, (R): Read only

Refer to the description of BRWD and BL2-0 in 4.10. Block Lock Operation.

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Table 14 Feature Table - B0h Address Description

Bit	Symbol	Parameter	Read / Write	Description
7	PRT_E	Block Protect Enable	R/W	The setting for Block Protection. 0b: Normal Operation (Default) 1b: Block Protection Enable – The Protect Execute command (2Ah) is acceptable for block protection.
6	IDR _E	ID Read Enable	R/W	The setting for Parameter Page Read and Unique ID Read. 0b: Normal Operation (Default) 1b: Parameter Page Read and Unique ID read mode
5	Reserved	-	-	Reserved
4	ECC _E	ECC Enable	R/W	The setting for internal ECC Function. 0b: Internal ECC Disable 1b: Internal ECC Enable (Default)
3	Reserved	-	-	Reserved
2	BBI	Bad Block Inhibit	R	The setting for Bad Block Inhibit Function. 0b: Not Available 1b: Bad Block Inhibit Enable (Default)
1	HSE	High Speed Mode Enable	R/W	The setting for Page Read High Speed Mode. 0b: High Speed Mode Disable 1b: High Speed Mode Enable (Default)
0	Reserved	-	-	Reserved

Note: (R/W): Read / Write, (R): Read only

Refer to the description of PRT_E in 4.11. Block Protection Operation (One Time Program).

Refer to the description of ECC_E in 4.16.1. ECC Switch.

Refer to the description of BBI in 4.15. Bad Block Inhibit.

Refer to the description of HSE in 4.3. Page Read Operation - High Speed Mode.

Table 15 Feature Table - C0h Address Description

Bit	Symbol	Parameter	Read / Write	Description
7	Reserved	-	-	Reserved
6	Reserved	-	-	Reserved
5	ECCS1	ECC Status 1	R	ECC status bits indicate the status of internal ECC operation. 00b: No bit flips were detected in previous page read. 01b: Bit flips were detected and corrected. Bit flip count was less than the threshold bit count. The threshold bit count is set by bits [7:4] in address 10h in the feature table. 10b: Multiple bit flips were detected and not corrected. 11b: Bit flips were detected and corrected. Bit flip count was equal to or more than the threshold bit count. The threshold bit count is set by bits [7:4] in address 10h in the feature table.
4	ECCS0	ECC Status 0	R	
3	PRG_F	Program Fail	R	Program fail bit indicates that a program failure has occurred in the previous Program Operation or Block Protection Operation. 0b: Program Pass 1b: Program Fail
2	ERS_F	Erase Fail	R	Erase fail bit indicates that an erase failure has occurred in the previous Erase operation. 0b: Erase Pass 1b: Erase Fail
1	WEL	Write Enable Latch	R/W	This bit indicates the status of write enable/disable. 0b: Write Disable (Default) 1b: Write Enable
0	OIP	Operation In Progress	R	This bit indicates the status of the device. This bit will be set while busy state. 0b: Operation is not in progress. Ready state. 1b: Operation is in progress. Busy state.

Note: (R/W): Read / Write, (R): Read only

The users must use the Write Enable (06h) or the Write Disable (04h) command to switch the WEL bit since Set Feature command cannot change it.

Once the Get Feature command is issued, the status and setting information are output continuously.

OIP, PRG_F, ERS_F bits are updated automatically during the status information are output continuously.

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4.9.1. Set Feature (1Fh)

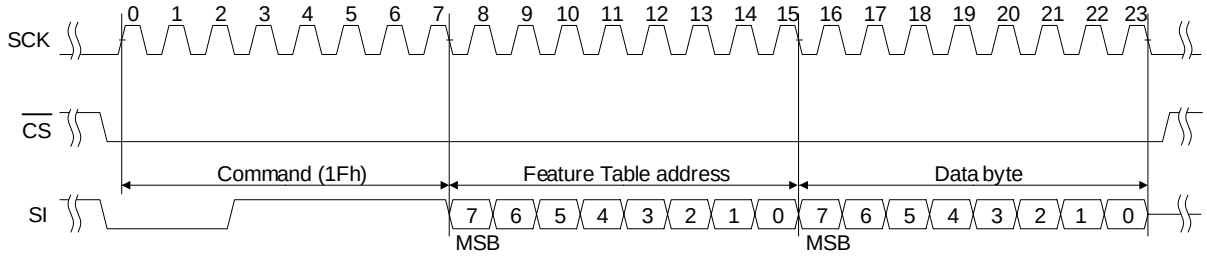


Figure 22. Set Feature Timing

4.9.2. Get Feature (0Fh)

After the Get Feature command and the address are input, the 8 bit status and setting information will be output continuously until $\overline{CS}$ goes High.

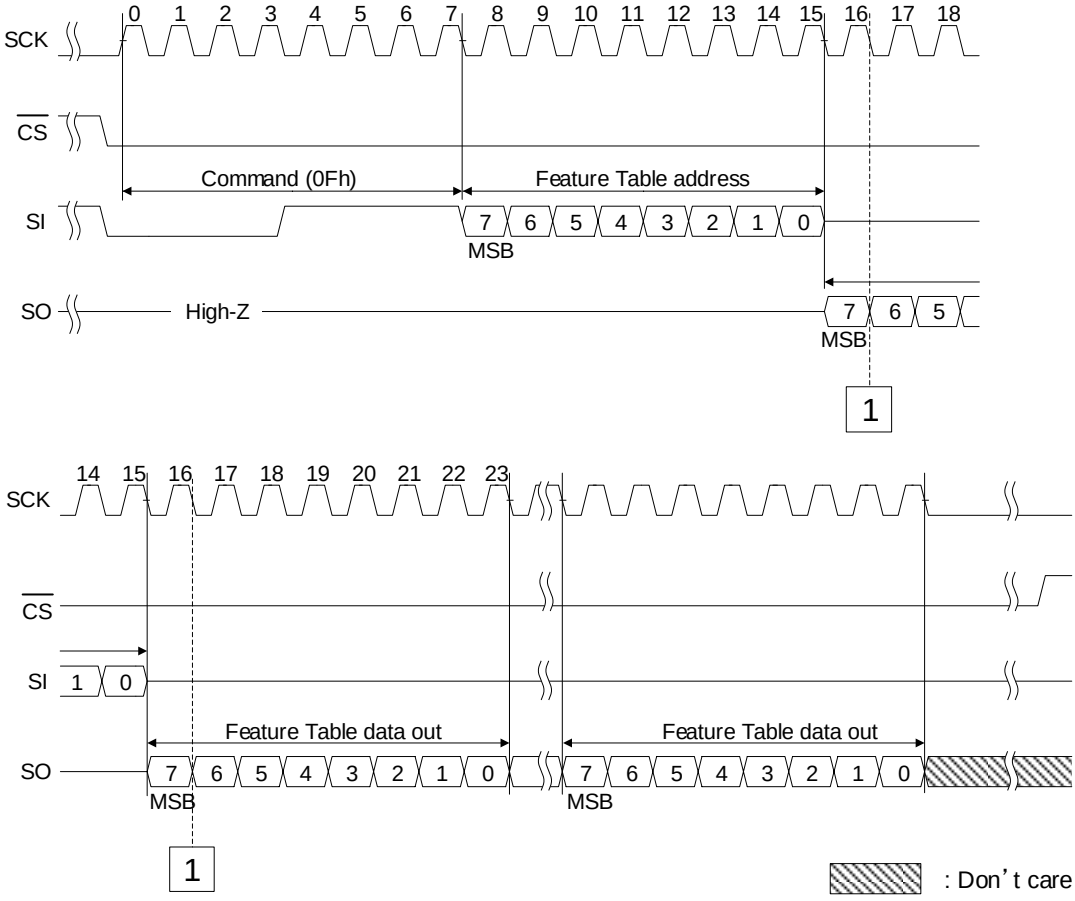


Figure 23. Get Feature Timing

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4.10. Block Lock Operation

The Block Lock Operation prevents Page Program, Block Protection and Block Erase operations. The users set the range of locked blocks as the entire device or a portion of the device using the BL bits (bits [5:3]) in address A0h of the feature table shown in Table 12. The users set the BL bits by the Set Feature operation. After the power on sequence, all blocks are locked (bits [5:3] are all set to 1). If the Program Execute (10h), Protect Execute (2Ah) or Block Erase (D8h) command is issued to locked blocks, Program Fail or Erase Fail will be indicated in the feature table shown in Table 12.
The users must clear / change the BL bits using Set Feature command to unlock the entire of the device or portion of the device. When BRWD bit is set and $\overline{WP}$ pin is Low, the users cannot switch the BRWD and the BL bits.
The Block Lock Operation is different from the Block Protection Operation.

Table 16 Block Lock Setting

BL2	BL1	BL0	Protected Area	Protected Blocks
0	0	0	All Unlocked	None
0	0	1	Upper 1/64 Locked	Block 2016 to 2047
0	1	0	Upper 1/32 Locked	Block 1984 to 2047
0	1	1	Upper 1/16 Locked	Block 1920 to 2047
1	0	0	Upper 1/8 Locked	Block 1792 to 2047
1	0	1	Upper 1/4 Locked	Block 1536 to 2047
1	1	0	Upper 1/2 Locked	Block 1024 to 2047
1	1	1	All Locked	Block 0 to 2047

4.11. Block Protection Operation (One Time Program)

The Block Protection Operation provides the function to prohibit the Program and Erase operations to user selected blocks. The users protect individual blocks using the Set Feature, Write Enable and Protect Execute commands. The last 128 blocks of the device are able to be set to protected blocks. The block protection setting is permanent. Once a block is protected, the users cannot unprotect the block.
When PRT_E (bit [7]) in address B0h of the feature table is set to 1, and the users issue the Protect Execute command (2Ah), the user block will become a protected block. The users must set the PRT_E bit (bit [7]) just before the Write Enable command for the Protect Execute. After the protection to the block, the users must clear bit [7] in address B0h using the Set Feature command. The users can issue the Protect Execute (2Ah) only one time for each block.
The Block Protection Operation is different from the Block Lock Operation.

The operation sequence to set block “N” as a protected block is as follows.

1. Set Feature (1Fh) : To set PRT_E bit [7] in address B0h to block protection mode
2. Write Enable (06h) : To enable the Protect Execute command
3. Protect Execute (2Ah) for block “N” : To protect the block “N”
4. Get Feature (0Fh) : To read the status (OIP and PRG_F bits) of the device
5. Set Feature (1Fh) : To clear PRT_E bit [7] in address B0h

Get Feature command is repeatable command.

Table 17 Block Protection Setting

PRT_E	State
0	Normal Operation (Default)
1	Block Protection Enable – The Protect Execute command (2Ah) is acceptable for block protection.

Table 18 Block Number for Block Protection

Block Number	Block Protection
Block 0 – Block 1919	The users cannot protect these blocks by block protection operation.
Block 1920 – Block 2047	The users can protect these blocks by block protection operation.

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4.11.1. Protect Execute (2Ah)

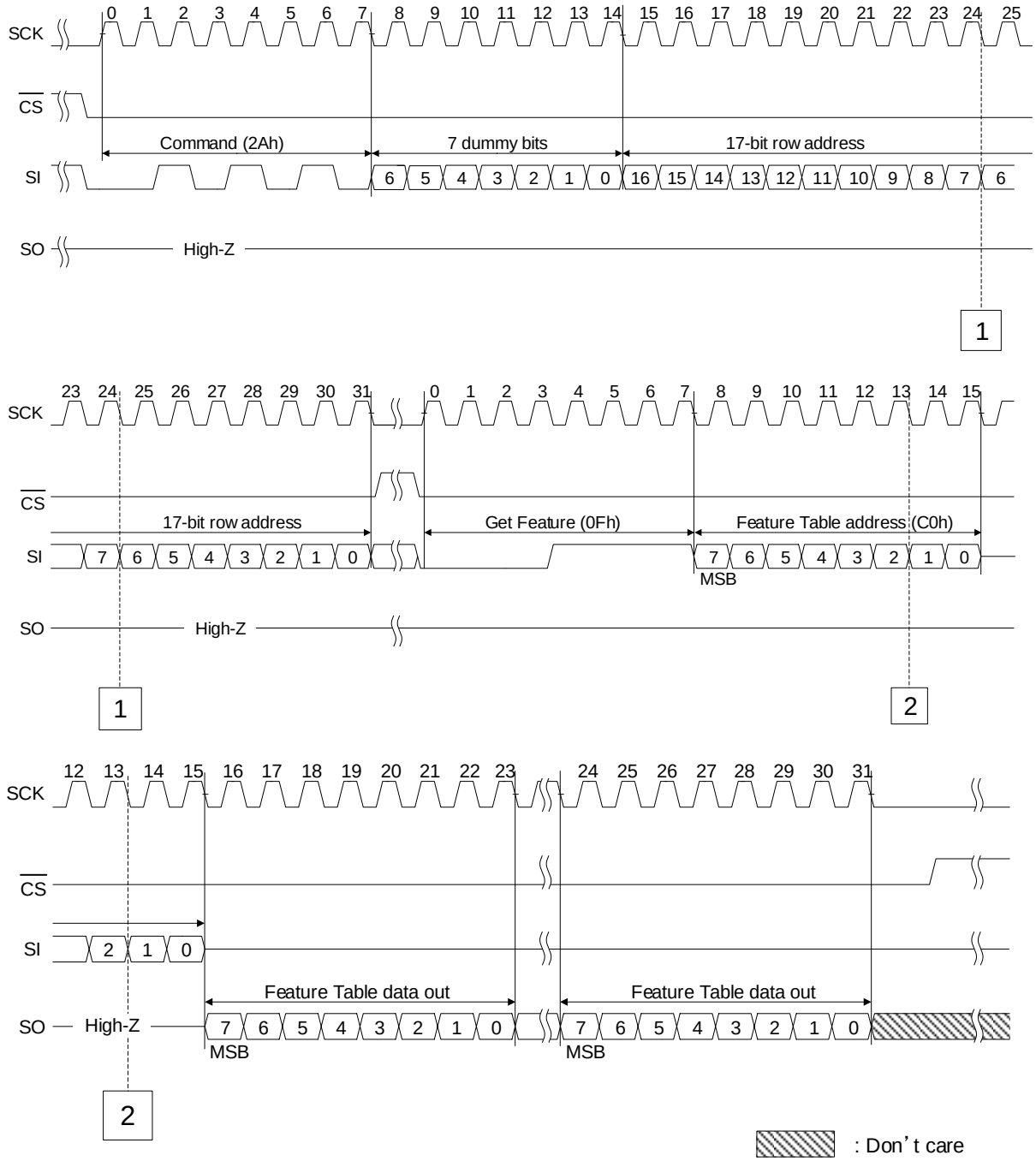


Figure 24. Protect Execute Timing

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4.12. Parameter Page Read Operation

The device has a parameter page. The operation sequence is as follows.

1. Set Feature (1Fh) with address B0h and set bit [6] : To set the IDR_E bit in the feature table
2. Read Cell Array (13h) with address 01h : To read the parameter page
3. Get Feature (0Fh) : To read the status (OIP bit) of the device
4. Read Buffer (03h or 0Bh) with address 00h : To output the parameter page
   or Read Buffer x2 (3Bh)
   or Read Buffer x4 (6Bh)
5. Set Feature (1Fh) with address B0h and clear bit [6] : To clear the IDR_E bit in the feature table

Read Buffer, Read Buffer x2, Read Buffer x4 and Get Feature commands are repeatable commands.

Table 19 Parameter Page

Byte	Parameter	Value
0 - 3	Signature	4Eh, 41h, 4Eh, 44h
4 - 31	Reserved	All 00h
32 - 43	Device manufacturer	54h, 4Fh, 53h, 48h, 49h, 42h, 41h, 20h, 20h, 20h, 20h, 20h
44 - 63	Device model; TC58CVG1S3HRAIG	54h, 43h, 35h, 38h, 43h, 56h, 47h, 31h, 53h, 33h, 48h, 52h, 41h, 49h, 47h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID	98h
65 - 79	Reserved	All 00h
80 - 83	Number of data bytes per page	00h, 08h, 00h, 00h
84 - 85	Number of spare bytes per page	40h, 00h
86 - 89	Number of data bytes per partial page	00h, 02h, 00h, 00h
90 - 91	Number of spare bytes per partial page	10h, 00h
92 - 95	Number of pages per block	40h, 00h, 00h, 00h
96 - 99	Number of blocks per unit	00h, 08h, 00h, 00h
100	Number of logical units	01h
101	Reserved	00h
102	Number of bits per cell	01h
103 - 104	Bad blocks maximum per unit	28h, 00h
105 - 106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108 - 109	Reserved	All 00h
110	Number of programs per page	04h
111	Reserved	00h
112	Number of ECC bits	00h
113 - 127	Reserved	All 00h
128	I/O pin capacitance	04h
129 - 132	Reserved	All 00h
133 - 134	t_{PROG} maximum page program time	F4h, 01h
135 - 136	t_{BERASE} maximum block erase time	58h, 1Bh
137 - 138	t_R maximum page read time	9Bh, 00h
139 - 253	Reserved	All 00h
254 - 255	Integrity CRC	EBh, 35h
256 - 511	Value of bytes 0–255	-
512 - 767	Value of bytes 0–255	-

Note: The value of all parameters are default setting of the device.
When the users change the setting of the device such as internal ECC enable/disable, parameter page is not updated.

The Integrity CRC (Cyclic Redundancy Check) field is used to verify that the contents of the Parameter Page were transferred correctly to the host. The CRC of the Parameter Page is a word (16-bit) field. The CRC calculation covers all of data between byte 0 and byte 253 of the Parameter Page inclusive.

The CRC shall be calculated on byte (8-bit) quantities starting with byte 0 in the Parameter Page. The bits in the 8-bit quantity are processed from the most significant bit (bit 7) to the least significant bit (bit 0).

The CRC shall be calculated using the following 16-bit generator polynomial:
$G(X) = X_{16} + X_{15} + X_2 + 1$
This polynomial in hex may be represented as 8005h.
The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

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4.13. Read ID (9Fh)

The ID of the device is read by command 9Fh.

Table 20 ID Table

Byte	Description	Value
Byte 0	Manufacture ID (KIOXIA)	98h
Byte 1	Device ID	CBh

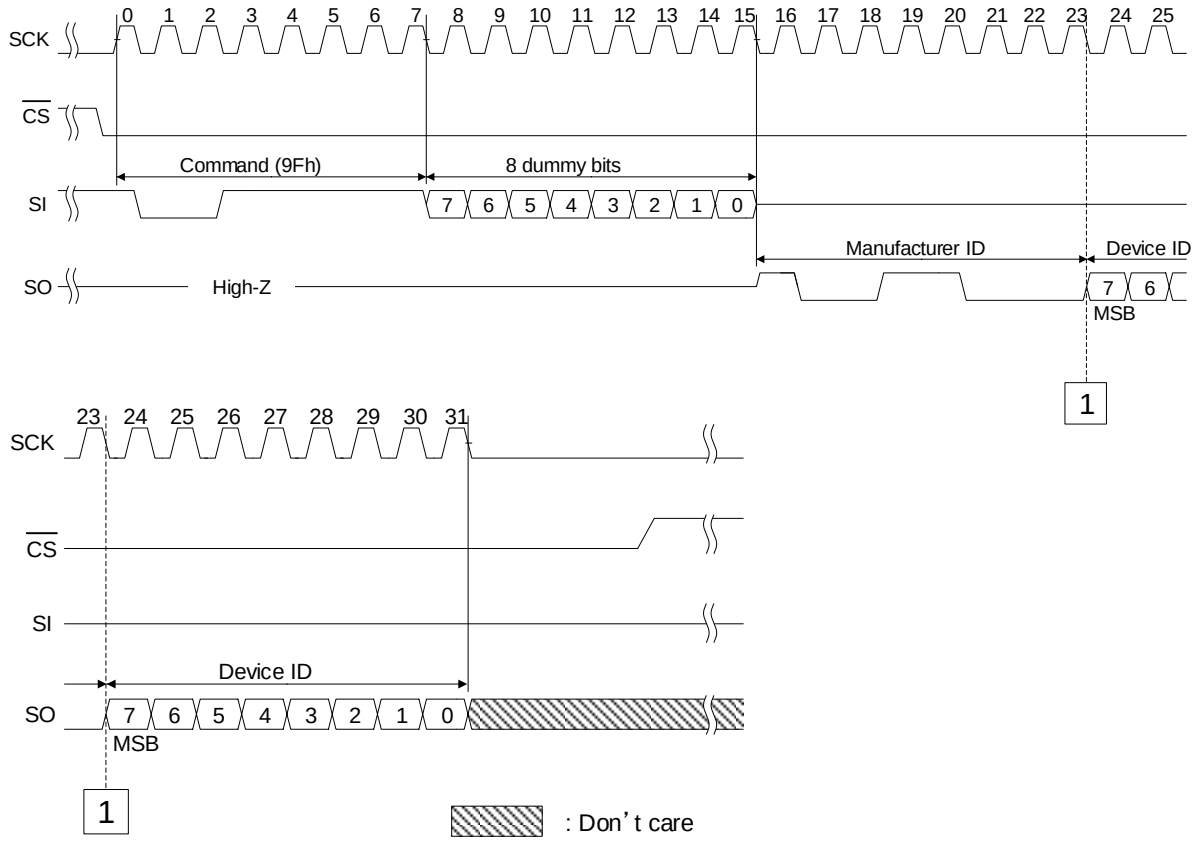


Figure 25. Read ID Timing

4.14. Unique ID Read Operation

The device has a unique ID and it is different for each device. The device has 16 copies of 32 bytes of unique ID data. The first 16 bytes of data are unique ID data and the second 16 bytes of data are the complement value of the first 16 bytes of data. The operation sequence is as follows.

1. Set Feature (1Fh) with address B0h and set bit [6] : To set the IDR_E bit in the feature table
2. Read Cell Array (13h) with address 00h : To read the unique ID
3. Get Feature (0Fh) : To read the status (OIP bit) of the device
4. Read Buffer (03h or 0Bh) with address 00h : To output the 16 copies of the Unique ID
   or Read Buffer x2 (3Bh)
   or Read Buffer x4 (6Bh)
5. Set Feature (1Fh) with address B0h and clear bit [6] : To clear the IDR_E bit in the feature table

Read Buffer, Read Buffer x2, Read Buffer x4 and Get Feature commands are repeatable commands.

4.15. Bad Block Inhibit

The device occasionally contains unusable blocks in its initial condition. The Page Program, Block Protection and Erase operation are prohibited to invalid blocks. The device has a bad block inhibit function to protect initial invalid blocks. When the users issue the Program or Erase command to the initial invalid blocks, the device ignores these commands automatically and program fail or erase fail is indicated in the feature table as shown in Table 12. The bad block inhibit function is enabled by default and this setting is permanent.

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4.16. Internal ECC

The device has internal ECC and it generates error correction code during the busy time in a Program operation. The ECC logic manages 9 bit error detection and 8bit error correction in each 528 bytes of main data and spare data. A section of the main area (512 bytes) and spare area (16 bytes) are paired for ECC calculation. During the Read operation, the device executes ECC by itself. Once the Read command is executed, the Get Feature command can be issued to check the read status. The read status remains until other valid commands are executed.
The device has the functions of Bit Flip Detection and Maximum Bit Flip Count Report. Internal ECC detects the bit flips in each sector and the maximum bit flip count in a page. These results are indicated in the feature table as shown in Table 12.

Table 21 Page Assignment

1st Main	2nd Main	3rd Main	4th Main	1st Spare	2nd Spare	3rd Spare	4th Spare	Internal ECC Parity Area
512B	512B	512B	512B	16B	16B	16B	16B	64B

Table 22 Definition of 528 bytes Data Pair

Data Pair	Column Address	
	Main Area	Spare Area
1st Data Pair (Sector 0)	0 to 511	2048 to 2063
2nd Data Pair (Sector 1)	512 to 1023	2064 to 2079
3rd Data Pair (Sector 2)	1024 to 1535	2080 to 2095
4th Data Pair (Sector 3)	1536 to 2047	2096 to 2111

Note: The ECC parity code generated by internal ECC is stored in column addresses 2112-2175 and the users cannot access to these specific addresses when internal ECC is enabled. While using the Partial Page Program, the users must program the data to main area and spare area simultaneously by the definition of data pair.

4.16.1. ECC Switch

The internal ECC is enabled after the power on sequence. The users set or clear the ECC_E bit (bit [4]) in address B0h of the feature table to enable or disable the internal ECC by the Set Feature command. If the ECC_E bit is cleared to 0 in the feature table, internal ECC will be disabled. In this case, the spare area size is changed from 64 bytes to 128 bytes automatically. When the users switching the ECC_E bit, the users must issue the Set Feature command just before the Page Read, Page Program or Block Erase operation.

4.16.2. ECC Status

The ECC Status function is used to monitor the error correction status. The device can correct up to 8 bit errors. ECC is performed on the NAND Flash main and spare areas. The ECC status is indicated in the ECCS1 and ECCS0 bit (bits [5:4]) in address C0h of the feature table shown in Table 15. The users issue the Get Feature command to read the ECC status.

4.16.3. ECC Bit Flip Count Detection

The ECC Bit Flip Count Detection function detects the bit flip count in a page. The users set the threshold bit count using the Set Feature command. The threshold bit count is decided by the bit flip detection setting bit (BFD) in address 10h in the feature table as shown in Table 12. The detected results will be indicated in the BFS bits (bits [7:0]) in address 20h. When bit flips exceed the threshold in a sector, the BFS bits are set after the Read Buffer command.

Table 23 Bit Flip Count Detection Setting (BFD)

BFD3	BFD2	BFD1	BFD0	Description
0	0	0	0	Reserved
0	0	0	1	Detect 1 bit flip in a sector
0	0	1	0	Detect 2 bit flips in a sector
0	0	1	1	Detect 3 bit flips in a sector
0	1	0	0	Detect 4 bit flips in a sector (Default)
0	1	0	1	Detect 5 bit flips in a sector
0	1	1	0	Detect 6 bit flips in a sector
0	1	1	1	Detect 7 bit flips in a sector
1	0	0	0	Detect 8 bit flips in a sector
1	1	1	1	Detect the uncorrectable error (9+ bit errors in a sector)

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Table 24 Bit Flip Count Detection Status (BFS) (Feature Table - 20h Address Description)

Bit	Symbol	Parameter	Read / Write	Description
7	Reserved	-	-	Reserved
6	Reserved	-	-	Reserved
5	Reserved	-	-	Reserved
4	Reserved	-	-	Reserved
3	BFS3	Bit Flip Count Detection Status 3	R	Bit flip count detection status 3 indicates that the bit flip count in sector 3 is more than threshold bit count. 0b: Bit flip count in sector 3 is less than the threshold. 1b: Bit flip count in sector 3 is equal to or more than the threshold bit count.
2	BFS2	Bit Flip Count Detection Status 2	R	Bit flip count detection status 2 indicates that the bit flip count in sector 2 is more than threshold bit count. 0b: Bit flip count in sector 2 is less than the threshold. 1b: Bit flip count in sector 2 is equal to or more than the threshold bit count.
1	BFS1	Bit Flip Count Detection Status 1	R	Bit flip count detection status 1 indicates that the bit flip count in sector 1 is more than threshold bit count. 0b: Bit flip count in sector 1 is less than the threshold. 1b: Bit flip count in sector 1 is equal to or more than the threshold bit count.
0	BFS0	Bit Flip Count Detection Status 0	R	Bit flip count detection status 0 indicates that the bit flip count in sector 0 is more than threshold bit count. 0b: Bit flip count in sector 0 is less than the threshold. 1b: Bit flip count in sector 0 is equal to or more than the threshold bit count.

4.16.4. ECC Bit Flip Count Report

The ECC Bit Flip Count Report function reports the bit flip count of each sector in a page. The users can read the bit flip count using the Get Feature command with address 40h and 50h.

Table 25 Bit Flip Count Report for Sector 0 (BFR)

BFR3	BFR2	BFR1	BFR0	Description
0	0	0	0	No bit flip occurred in sector 0
0	0	0	1	1 bit flip occurred in sector 0 and corrected
0	0	1	0	2 bit flips occurred in sector 0 and corrected
0	0	1	1	3 bit flips occurred in sector 0 and corrected
0	1	0	0	4 bit flips occurred in sector 0 and corrected
0	1	0	1	5 bit flips occurred in sector 0 and corrected
0	1	1	0	6 bit flips occurred in sector 0 and corrected
0	1	1	1	7 bit flips occurred in sector 0 and corrected
1	0	0	0	8 bit flips occurred in sector 0 and corrected
1	1	1	1	Bit flips over 8 bits occurred in sector 0 and were not corrected.

Table 26 Sector Definition (BFR)

BFR7	BFR6	BFR5	BFR4	BFR3	BFR2	BFR1	BFR0
Sector 1				Sector 0			

BFR15	BFR14	BFR13	BFR12	BFR11	BFR10	BFR9	BFR8
Sector 3				Sector 2			

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4.16.5. ECC Maximum Bit Flip Count Report

The ECC Maximum Bit Flip Count Report function provides the maximum bit flip count in a page. The maximum count is indicated in address 30h of the feature table shown in Table 12. The sector number in which the maximum bit flip occurred in a page is indicated in the MFS bit (bits [2:0]) in address 30h as shown in Table 28. When several sector's Maximum Bit Flip Count are the same, the lowest sector number is indicated in these bits. The users get the report using the Get Feature command.

Table 27 Maximum Bit Flip Count (MBF)

MBF3	MBF2	MBF1	MBF0	Description
0	0	0	0	No bit error is detected in the page.
0	0	0	1	Maximum bit flip count is 1 bit in a sector. Bit flip was corrected.
0	0	1	0	Maximum bit flip count is 2 bits in a sector. Bit flips were corrected.
0	0	1	1	Maximum bit flip count is 3 bits in a sector. Bit flips were corrected.
0	1	0	0	Maximum bit flip count is 4 bits in a sector. Bit flips were corrected.
0	1	0	1	Maximum bit flip count is 5 bits in a sector. Bit flips were corrected.
0	1	1	0	Maximum bit flip count is 6 bits in a sector. Bit flips were corrected.
0	1	1	1	Maximum bit flip count is 7 bits in a sector. Bit flips were corrected.
1	0	0	0	Maximum bit flip count is 8 bits in a sector. Bit flips were corrected.
1	1	1	1	Maximum bit flip count exceed 8 bits in a sector. Bit flips were not corrected.

Table 28 Maximum Bit Flip Count Sector (MFS)

MFS2	MFS1	MFS0	Description
0	0	0	Maximum bit flips occurred in sector 0
0	0	1	Maximum bit flips occurred in sector 1
0	1	0	Maximum bit flips occurred in sector 2
0	1	1	Maximum bit flips occurred in sector 3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

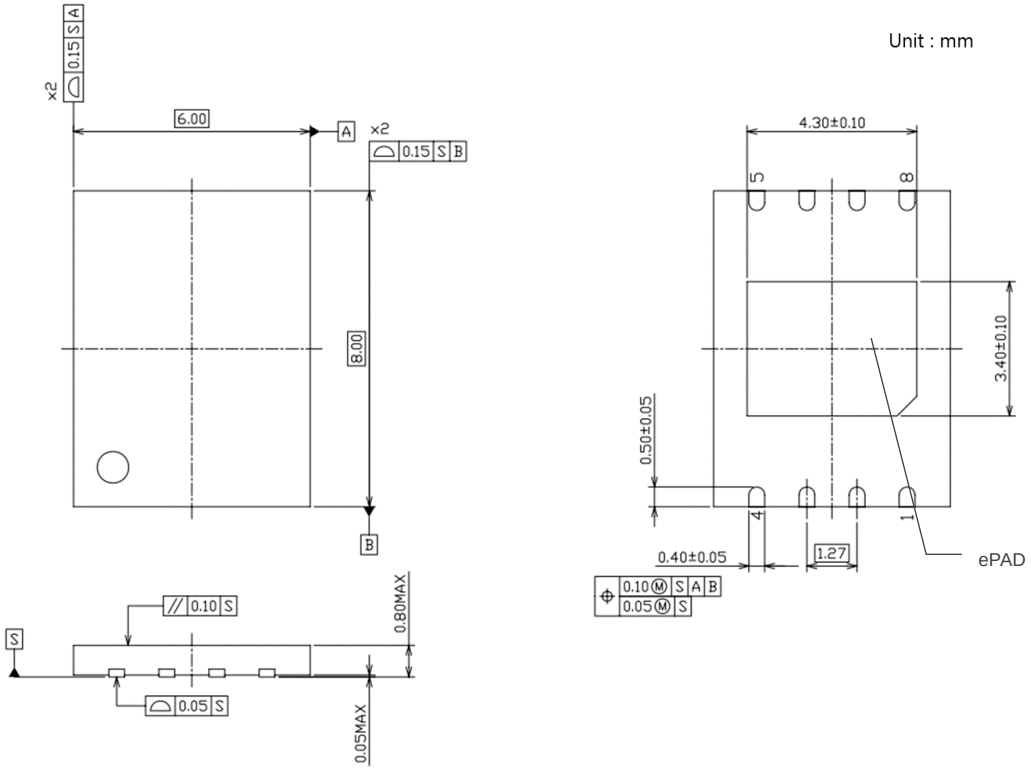
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5. Package Information

5.1. WSON8 (P-WSON8-0608-1.27-003)

The WSON8 features an exposed PAD (ePAD). The ePAD is configured on the package bottom without any connection to the chip inside. It is recommended for users to solder the ePAD onto PC board with connection to V_{SS} or None, as the adhesive strength to the PC board will be enhanced.



Weight: 0.12 g (typ.)

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6. Application Notes

6.1. Prohibition of Unspecified Commands

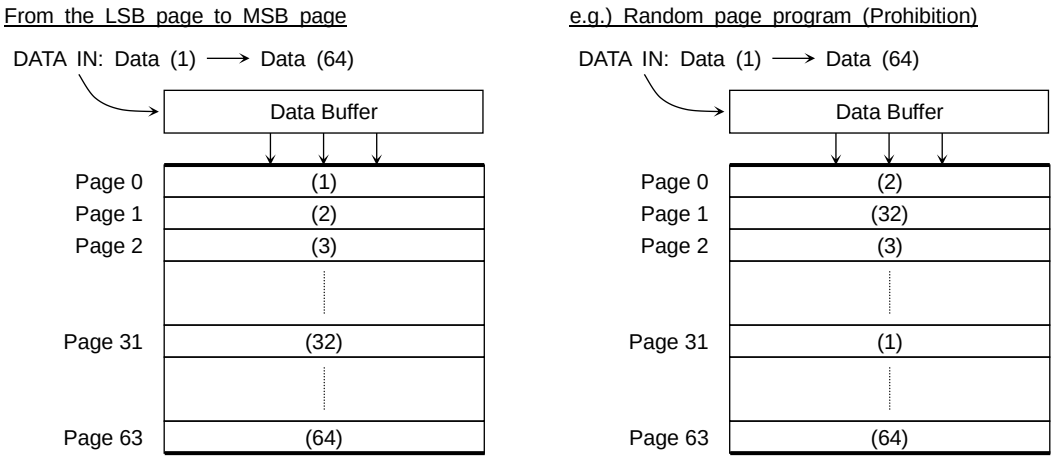
The operation commands are listed in Table 11. Input of a command other than those specified in Table 11 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

6.2. Restriction of Commands while in the Busy State

During the operation in progress, do not input any command except Get Feature (0Fh) and Reset (FFh or FEh).

6.3. Addressing for Page Program Operation

Within a block, the pages must be programmed consecutively from the LSB (Least Significant Bit) page of the block to MSB (Most Significant Bit) page of the block. Random page address programming is prohibited.



6.4. Several Programming Cycles on the Same Page (Partial Page Program)

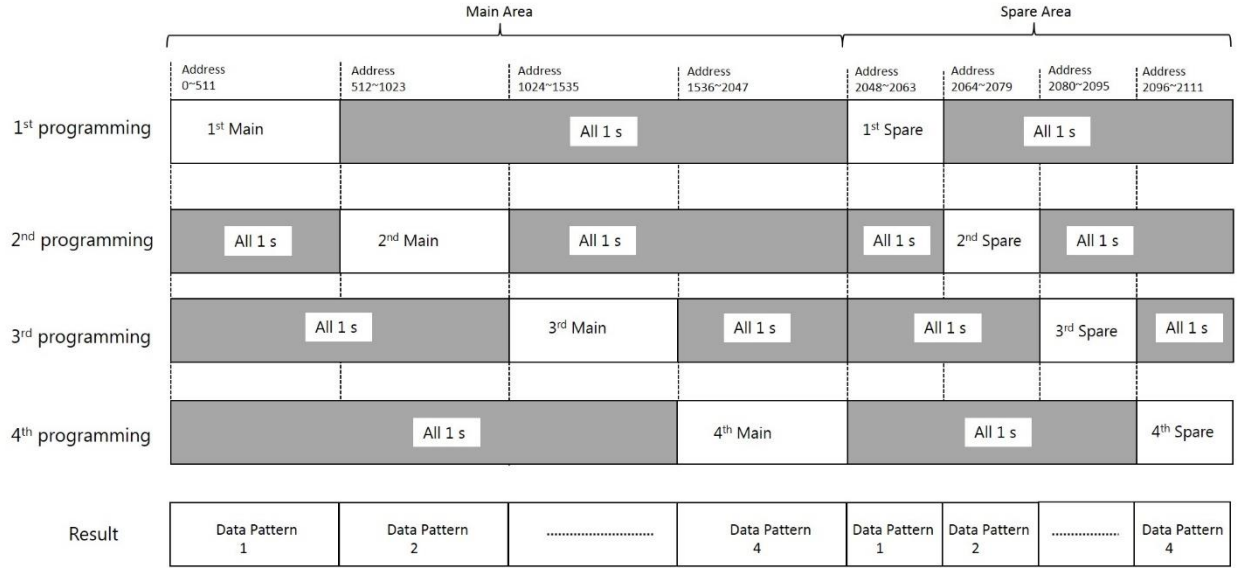
Internal ECC ON:

Partial Page Program should follow the Table 22 restriction while ECC_E bit is set to 1.

ECC Parity Code is generated during program operation on Main area (512 byte) + Spare area (16 byte), and this parity code is written to the Parity area as shown in Table 21.

While using the Partial Page Program, the user must program the data to main and spare area simultaneously by the definition of sector in section “Internal ECC”.

For example, each segment can be programmed individually as follows:

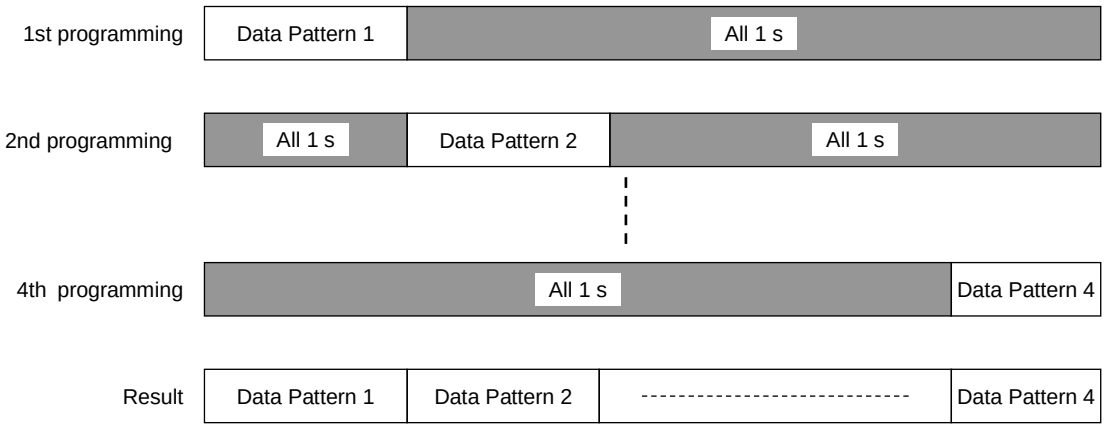


Program Load Random Data (84h) command can be used to skip column address within the selected page to improve the data input operation.

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Internal ECC OFF:
Each segment can be programmed individually as follows while ECC_E bit is set to 0.



Program Load Random Data (84h) command can be used to skip column address within the selected page to improve the data input operation.

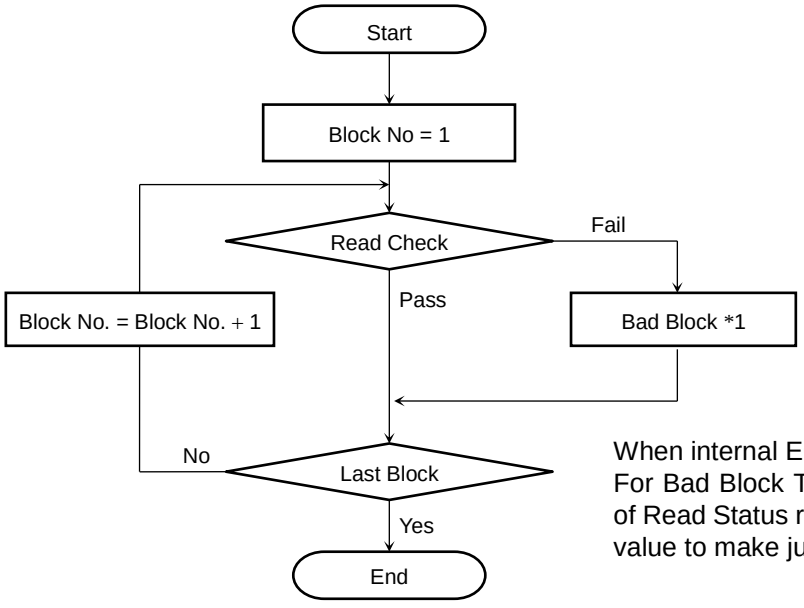
6.5. Power Off Timing

Please do not turn off the power before Page Program, Block Protection and Erase operation is completed. Avoid using the device when the battery is low. Power shortage and/or power failure before Write/Erase operation is completed will cause loss of data and/or damage to data.

6.6. Invalid Blocks (Bad Blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:
The Page Program, Block Protection and Erase operation are prohibited to the invalid blocks. When the users issue the Program or Erase command to the initial invalid blocks, the device ignores these commands automatically and Program Fail or Erase Fail is indicated in the feature table as shown in Table 12. Check if the device has any bad blocks after installation into the system. Refer to the test flow for initial bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system. A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates. The number of valid blocks over the device lifetime is as Table 2.

Regarding invalid blocks, the bad block mark is in the whole pages. Please read one column of any page in each block. If the data of the column is 00 (Hex), define the block as a bad block.



When internal ECC is turned ON:
For Bad Block Test Flow, during Read Check, irrespective of Read Status result (ECC Pass or Fail), use the read data value to make judgment for Bad Block.

*1: No erase operation is allowed to detected bad blocks.

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6.7. Failure Phenomena

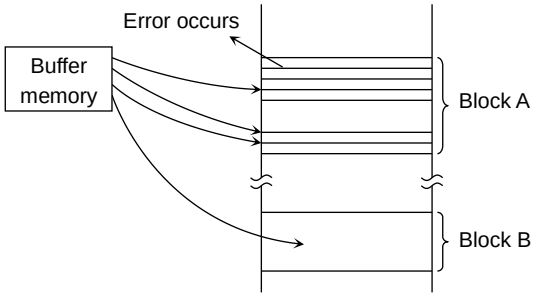
The device may fail during a Program, Erase or Read operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
	Block Protection Failure	Status Read after Block Protection → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Read	Bit Error	Check the ECC correction status by Get Feature command and take appropriate measures such as rewrite in consideration of Wear Leveling before uncorrectable ECC error occurs.

- Block Protection Failure is checked by PRG_F bit in feature table using Get Feature command after Protect Execute.

Block Replacement

Program



When an error happens in Block A, reprogramming the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent further accesses to this bad block (by creating a table within the system or by using another appropriate scheme).

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6.8 Reliability Guidance

This reliability guidance is intended to provide some guidance related to using NAND Flash with 8 bit ECC for each 512 bytes. NAND Flash memory cells are gradually worn out and the reliability level of memory cells is degraded by repeating Write and Erase operation of '0' data in each block. For detailed reliability data, please refer to the reliability note for each product.
Although random bit errors may occur during use, it does not necessarily mean that a block is bad.
Generally, a block should be marked as bad when a program status failure or erase status failure is detected.
The reliability of NAND Flash memory cells during the actual usage on system level depends on the usage and environmental conditions. KIOXIA adopts the checker pattern data, 0x55 & 0xAA for alternative Write/Erase cycles, for the reliability test.

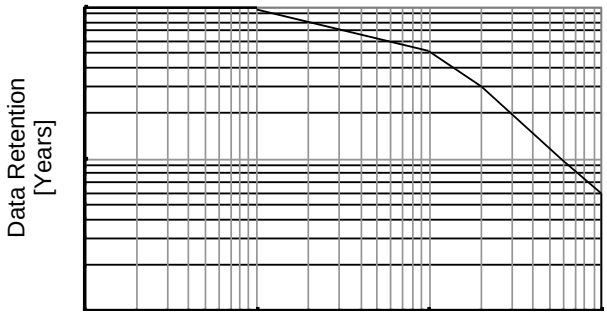
Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a Status Read after either an Auto Page Program or Auto Block Erase operation. The cumulative bad block count will increase along with the number of Write/Erase cycles.

Data Retention

The data in NAND Flash memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again.
Data Retention time is generally influenced by the number of Write/Erase cycles and temperature.

Here is a graph plotting the relationship between Write/Erase Endurance and Data Retention.



Read Disturb

A Read operation may disturb the data in NAND Flash memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again. Read Disturb capability is generally influenced by the number of Write/Erase cycles.

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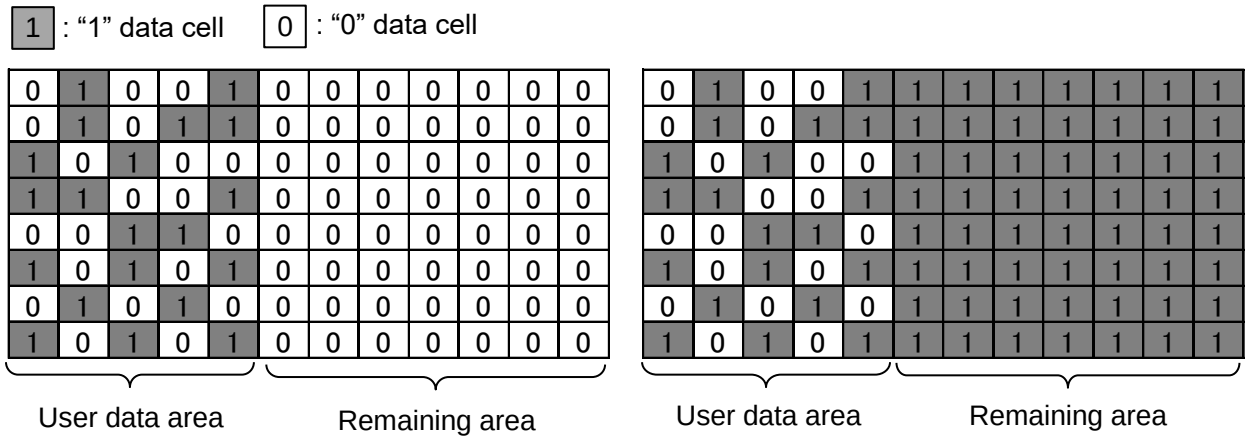
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6.9 NAND Management

NAND Management such as Bad Block Management, ECC treatment and Wear Leveling, but not limited to these treatments, should be recognized and incorporated in the system design.
ECC treatment for read data is mandatory against random bit errors, and host should monitor ECC status to take appropriate measures such as rewrite in consideration of Wear Leveling before uncorrectable Error occurs.
To realize robust system design, generally it is necessary to prevent the concentration of Write/Erase cycles at the specific blocks by adopting Wear Leveling which manages to distribute Write/Erase cycles evenly among NAND Flash memory. And also it is necessary to avoid dummy ‘0’ data write, e.g. ‘0’ data padding, which accelerate block endurance degradation.

Continuous Write and Erase cycling with high percentage of '0' bits in data pattern can lead to faster block endurance degradation.

Example: NAND cell array with ‘0’ data padding



(a) Accelerate block endurance degradation by fixed dummy “0” data write

(b) “1” data for Remaining area (Recommended)

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7. Revision History

Date	Rev.	Description
2016-06-22	1.0	Initial Release
2016-11-08	1.1	Merged the datasheet of SOP16 and WSON 8 together Added package code in 1.3. Features. Updated the specification and description in 3.7. Programming, Reading and Erasing Characteristics. Updated the description in 4.2. Page Read Operation, 4.3. Page Read Operation - High Speed Mode, 4.4. Page Program Operation, 4.5. Internal Data Move Operation, 4.6. Block Erase (D8h), 4.7. Reset (FFh or FEh), 4.10. Block Lock Operation, 4.11. Block Protection Operation (One Time Program), 4.12. Parameter Page Read Operation, 4.14. Unique ID Read Operation and 4.16. Internal ECC. Updated 6.4. Several Programming Cycles on the Same Page (Partial Page Program) and 6.7. Failure Phenomena.
2018-02-06	1.2	Separate the definition of address into RA (row address) and CA (column address) in 4.1 Command Set Table. Added description in the weight of package, the definition of Reserved bits in Feature Table and 6.9. NAND Management Corrected typo, and described some notes. Renewed Reliability Guidance.
2018-10-01	1.3	Modified Table 16 Block Lock Setting and removed note. Changed “RESTRICTIONS ON PRODUCT USE”.
2019-10-01	2.0	Rebrand as “KIOXIA” Corrected Package Weight and typo. Described some notes and deleted unnecessary parts.

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