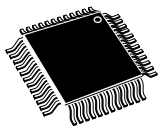
STM8S007C8

Value line, 24 MHz STM8S 8-bit MCU, 64 Kbytes Flash, true data EEPROM, 10-bit ADC, timers, 2 UARTs, SPI, I²C

Datasheet - production data

Features

- Core
  - Max f_{CPU}: up to 24 MHz, 0 wait states @ $f_{CPU} \leq$ 16 MHz
  - Advanced STM8 core with Harvard architecture and 3-stage pipeline
  - Extended instruction set
  - Max 20 MIPS @ 24 MHz
- Memories
  - Program: 64 Kbytes Flash; data retention 20 years at 55 °C after 100 cycles
  - Data: 128 bytes true data EEPROM; endurance 100 kcycles
  - RAM: 6 Kbytes
- Clock, reset and supply management
  - 2.95 to 5.5 V operating voltage
  - Low power crystal resonator oscillator
  - External clock input
  - Internal, user-trimmable 16 MHz RC
  - Internal low power 128 kHz RC
  - Clock security system with clock monitor
  - Wait, active-halt, & halt low power modes
  - Peripheral clocks switched off individually
  - Permanently active, low consumption power-on and power-down reset
- Interrupt management
  - Nested interrupt controller with 32 interrupts
  - Up to 37 external interrupts on 6 vectors
- Timers
  - 2x 16-bit general purpose timers, with 2+3 CAPCOM channels (IC, OC or PWM)
  - Advanced control timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
  - 8-bit basic timer with 8-bit prescaler
  - Auto wakeup timer
  - Window watchdog, independent watchdog



LQFP48
7 x 7mm

- Communications interfaces
  - UART with clock output for synchronous operation - LIN master mode
  - UART with LIN 2.1 compliant, master/slave modes and automatic resynchronization
  - SPI interface up to 10 Mbit/s
  - I^2C interface up to 400 Kbit/s
- 10-bit ADC with up to 16 channels
- I/Os
  - 38 I/Os including 16 high sink outputs
  - Highly robust I/O design, immune against current injection
  - Development support
  - Single wire interface module (SWIM) and debug module (DM)

This is information on a product in full production. www.st.com

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Contents

1 Introduction 8

2 Description 9

3 Block diagram 10

4 Product overview 11

4.1 Central processing unit STM8 11

4.2 Single wire interface module (SWIM) and debug module (DM) 12

4.3 Interrupt controller 12

4.4 Flash program and data EEPROM memory 12

4.5 Clock controller 14

4.6 Power management 15

4.7 Watchdog timers 15

4.8 Auto wakeup counter 16

4.9 Beeper 16

4.10 TIM1 - 16-bit advanced control timer 16

4.11 TIM2, TIM3 - 16-bit general purpose timers 16

4.12 TIM4 - 8-bit basic timer 17

4.13 Analog-to-digital converter (ADC2) 17

4.14 Communication interfaces 17

4.14.1 UART1 18

4.14.2 UART3 18

4.14.3 SPI 19

4.14.4 I^2C 20

5 Pinouts and pin descriptions 21

5.1 Alternate function remapping 25

6 Memory and register map 26

6.1 Memory map 26

6.2 Register map 27

深圳市满度科技有限公司
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Email:sales@manduic.com

7 Interrupt vector mapping 37

8 Option bytes 38

9 Electrical characteristics 42

9.1 Parameter conditions 42

9.1.1 Minimum and maximum values 42

9.1.2 Typical values 42

9.1.3 Typical curves 42

9.1.4 Typical current consumption 42

9.1.5 Pin loading conditions 43

9.1.6 Loading capacitor 43

9.1.7 Pin input voltage 43

9.2 Absolute maximum ratings 44

9.3 Operating conditions 46

9.3.1 VCAP external capacitor 48

9.3.2 Supply current characteristics 48

9.3.3 External clock sources and timing characteristics 56

9.3.4 Internal clock sources and timing characteristics 58

9.3.5 Memory characteristics 60

9.3.6 I/O port pin characteristics 61

9.3.7 Reset pin characteristics 70

9.3.8 SPI serial peripheral interface 72

9.3.9 I^2C interface characteristics 75

9.3.10 10-bit ADC characteristics 77

9.3.11 EMC characteristics 80

10 Package information 83

10.1 LQFP48 package information 83

10.2 Thermal characteristics 86

10.2.1 Reference document 86

10.2.2 Selecting the product temperature range 87

11 Part numbering 88

12 STM8 development tools 89

12.1 Emulation and in-circuit debugging tools 89

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Email:sales@manduic.com

12.2 Software tools 90
12.2.1 STM8 toolset 90
12.2.2 C and assembly toolchains 90
12.3 Programming tools 90

13 Revision history 91

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List of tables

Table 1. STM8S007C8 value line features . . . 9
Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers . . . 14
Table 3. TIM timer features . . . 17
Table 4. Legend/abbreviations for STM8S007C8 pin description table . . . 22
Table 5. STM8S007C8 pin description . . . 22
Table 6. Flash, Data EEPROM and RAM boundary addresses . . . 27
Table 7. I/O port hardware register map . . . 27
Table 8. General hardware register map . . . 29
Table 9. CPU/SWIM/debug module/interrupt controller registers . . . 35
Table 10. Interrupt mapping . . . 37
Table 11. Option bytes . . . 38
Table 12. Option byte description . . . 39
Table 13. Voltage characteristics . . . 44
Table 14. Current characteristics . . . 45
Table 15. Thermal characteristics . . . 45
Table 16. General operating conditions . . . 46
Table 17. Operating conditions at power-up/power-down . . . 47
Table 18. Total current consumption with code execution in run mode at V_{DD} = 5 V . . . 49
Table 19. Total current consumption with code execution in run mode at V_{DD} = 3.3 V . . . 50
Table 20. Total current consumption in wait mode at V_{DD} = 5 V . . . 51
Table 21. Total current consumption in wait mode at V_{DD} = 3.3 V . . . 51
Table 22. Total current consumption in active halt mode at V_{DD} = 5 V, T_A -40 to 85° C . . . 52
Table 23. Total current consumption in active halt mode at V_{DD} = 3.3 V . . . 52
Table 24. Total current consumption in halt mode at V_{DD} = 5 V, T_A -40 to 85° C . . . 53
Table 25. Total current consumption in halt mode at V_{DD} = 3.3 V . . . 53
Table 26. Wakeup times . . . 53
Table 27. Total current consumption and timing in forced reset state . . . 54
Table 28. Peripheral current consumption . . . 54
Table 29. HSE user external clock characteristics . . . 56
Table 30. HSE oscillator characteristics . . . 57
Table 31. HSI oscillator characteristics . . . 58
Table 32. LSI oscillator characteristics . . . 59
Table 33. RAM and hardware registers . . . 60
Table 34. Flash program memory/data EEPROM memory . . . 60
Table 35. I/O static characteristics . . . 61
Table 36. Output driving current (standard ports) . . . 63
Table 37. Output driving current (true open drain ports) . . . 63
Table 38. Output driving current (high sink ports) . . . 64
Table 39. NRST pin characteristics . . . 70
Table 40. SPI characteristics . . . 72
Table 41. I^2C characteristics . . . 75
Table 42. ADC characteristics . . . 77
Table 43. ADC accuracy with R_{AIN} < 10 kΩ , V_{DDA} = 5 V . . . 78
Table 44. ADC accuracy with R_{AIN} < 10 kΩ R_{AIN}, V_{DDA} = 3.3 V . . . 78
Table 45. EMS data . . . 80
Table 46. EMI data . . . 81
Table 47. ESD absolute maximum ratings . . . 81
Table 48. Electrical sensitivities . . . 82

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Table 49. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data. 84
Table 50. Thermal characteristics. 86
Table 51. Document revision history 91

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List of figures

Figure 1. STM8S007C8 value line block diagram . . . 10
Figure 2. Flash memory organisation . . . 13
Figure 3. LQFP 48-pin pinout . . . 21
Figure 4. Memory map . . . 26
Figure 5. Supply current measurement conditions . . . 42
Figure 6. Pin loading conditions . . . 43
Figure 7. Pin input voltage . . . 43
Figure 8. f_{CPUmax} versus V_{DD} . . . 47
Figure 9. External capacitor C_{EXT} . . . 48
Figure 10. Typ. $I_{DD(RUN)}$ vs V_{DD}, HSI RC osc, f_{CPU} = 16 MHz . . . 55
Figure 11. Typ. $I_{DD(WFI)}$ vs V_{DD}, HSI RC osc, f_{CPU} = 16 MHz . . . 55
Figure 12. HSE external clock source . . . 56
Figure 13. HSE oscillator circuit diagram . . . 57
Figure 14. Typical HSI frequency variation vs V_{DD} at 3 temperatures . . . 58
Figure 15. Typical LSI frequency variation vs V_{DD} @ 25 °C . . . 59
Figure 16. Typical V_{IL} and V_{IH} vs V_{DD} @ 3 temperatures . . . 62
Figure 17. Typical pull-up resistance vs V_{DD} @ 3 temperatures . . . 62
Figure 18. Typical pull-up current vs V_{DD} @ 3 temperatures . . . 63
Figure 19. Typ. V_{OL} @ V_{DD} = 5 V (standard ports) . . . 64
Figure 20. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports) . . . 65
Figure 21. Typ. V_{OL} @ V_{DD} = 5 V (true open drain ports) . . . 65
Figure 22. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports) . . . 66
Figure 23. Typ. V_{OL} @ V_{DD} = 5 V (high sink ports) . . . 66
Figure 24. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports) . . . 67
Figure 25. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (standard ports) . . . 67
Figure 26. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports) . . . 68
Figure 27. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (high sink ports) . . . 68
Figure 28. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports) . . . 69
Figure 29. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 3 temperatures . . . 70
Figure 30. Typical NRST pull-up resistance vs V_{DD} @ 3 temperatures . . . 71
Figure 31. Typical NRST pull-up current vs V_{DD} @ 3 temperatures . . . 71
Figure 32. Recommended reset pin protection . . . 72
Figure 33. SPI timing diagram - slave mode and CPHA = 0 . . . 73
Figure 34. SPI timing diagram - slave mode and CPHA = 1(1) . . . 73
Figure 35. SPI timing diagram - master mode(1) . . . 74
Figure 36. Typical application with I^2C bus and timing diagram . . . 76
Figure 37. ADC accuracy characteristics . . . 79
Figure 38. Typical application with ADC . . . 79
Figure 39. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline . . . 83
Figure 40. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint . . . 85
Figure 41. LQFP48 marking example (package top view) . . . 85
Figure 42. STM8S007C8 value line ordering information scheme(1) . . . 88

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1 Introduction

This datasheet contains the description of the STM8S007C8 value line features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S and STM8A microcontroller families reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the PM0051 (How to program STM8S and STM8A Flash program memory and data EEPROM).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

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2 Description

The STM8S007C8 value line 8-bit microcontrollers offer 64 Kbytes Flash program memory. They are referred to as high-density devices in the STM8S microcontroller family reference manual (RM0016).

The STM8S007C8 value line devices provide the following benefits: reduced system cost, performance, robustness, short development cycles, and product longevity.

The system cost is reduced thanks to a true data EEPROM for up to 100 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Device performance is ensured by 20 MIPS at 24 MHz CPU clock frequency and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

Short development cycles are guaranteed due to application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals. Full documentation is offered with a wide choice of development tools.

Product longevity is ensured in the STM8S family thanks to their advanced core which is made in a state-of-the art technology for applications with 2.95 V to 5.5 V operating supply.

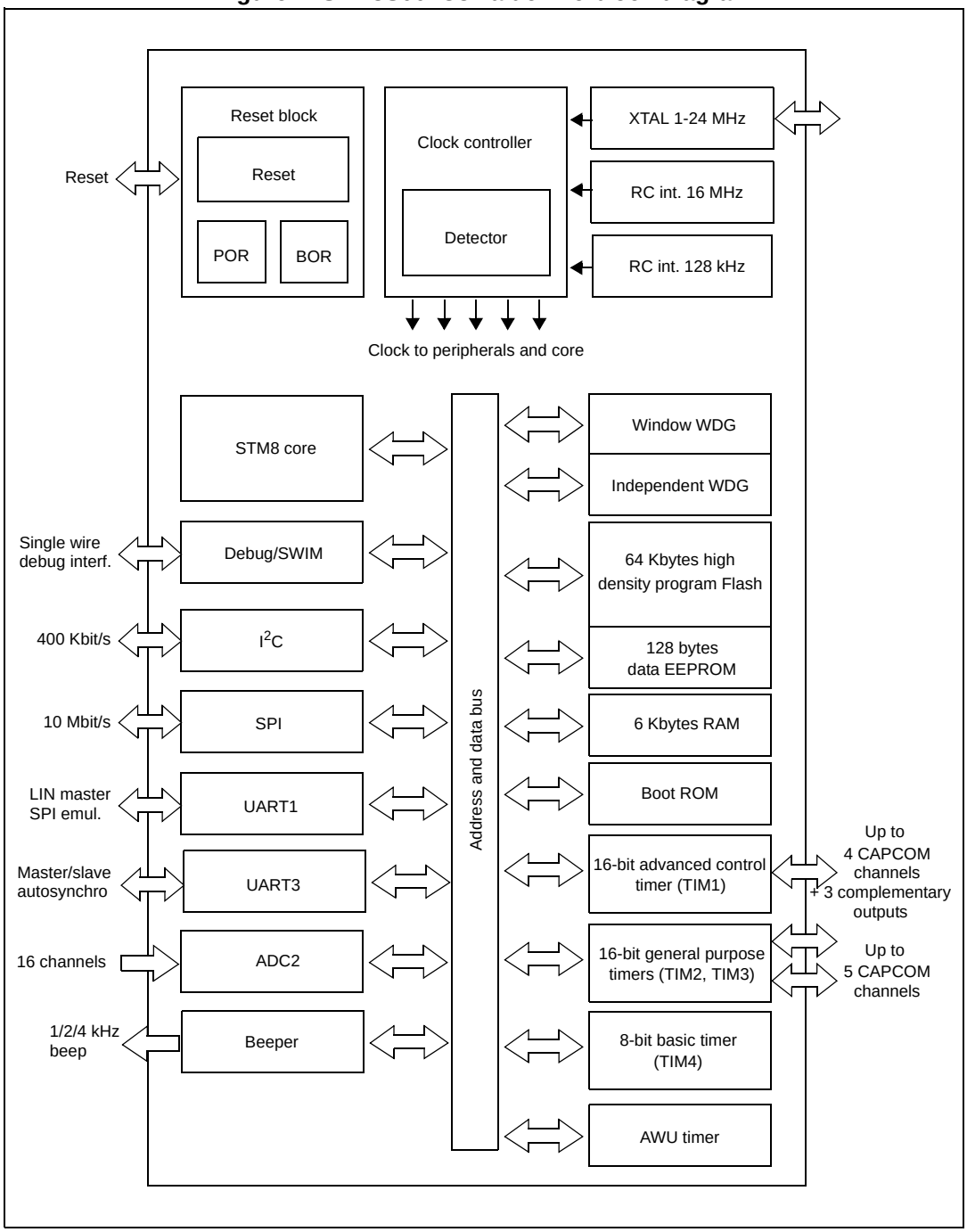
Table 1. STM8S007C8 value line features

Features	STM8S007C8
Pin count	48
Max. number of GPIOs (I/O)	38
External interrupt pins	35
Timer CAPCOM channels	9
Timer complementary outputs	3
A/D converter channels	10
High-sink I/Os	16
High-density Flash program memory	64 Kbytes
Data EEPROM	128 bytes
RAM	6 Kbytes

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3 Block diagram

Figure 1. STM8S007C8 value line block diagram



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4 Product overview

The following section intends to give an overview of the basic features of the STM8S007C8 value line functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

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4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

4.3 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 33 external interrupts on six vectors including TLI
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- 64 Kbytes of high density Flash program single voltage Flash memory
- 128 bytes true data EEPROM
- Read while write: Writing in data memory possible while executing code in program memory.
- User option byte area

Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to *Figure 2*.

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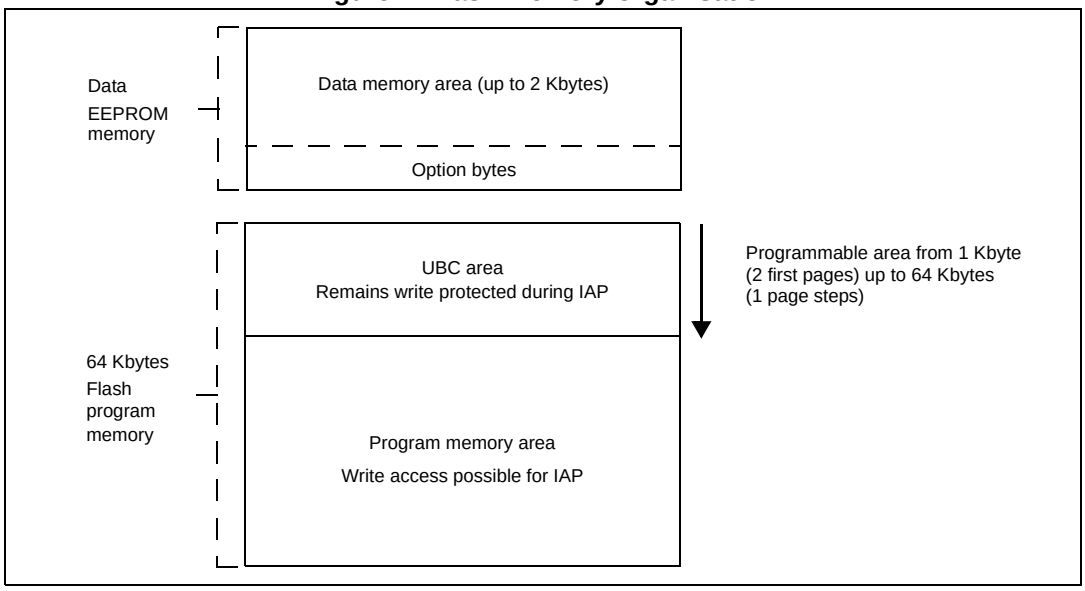
The size of the UBC is programmable through the UBC option byte (*Table 12*), in increments of 1 page (512 bytes) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: 64 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 64 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organisation



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

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4.5 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- ***Clock prescaler*:** To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- ***Safe clock switching*:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- ***Clock management*:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- ***Master clock sources*:** Four different clock sources can be used to drive the master clock:
  - 1-24 MHz high-speed external crystal (HSE)
  - Up to 24 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- ***Startup clock*:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- ***Clock security system (CSS)*:** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- ***Configurable main clock output (CCO)*:** This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART3	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	TIM3	PCKEN12	UART1	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I^2C	PCKEN24	Reserved	PCKEN20	Reserved

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4.6 Power management

For efficent power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- ***Wait mode***: In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- ***Active halt mode with regulator on***: In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- ***Active halt mode with regulator off:*** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- ***Halt mode***: In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: at 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

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Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM3 input capture channel 1 for calibration

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

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4.12 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 3. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complem. outputs	Ext. trigger	Timer synchr-onization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	No
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM3	16	Any power of 2 from 1 to 32768	Up	2	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog-to-digital converter (ADC2)

STM8S007C8 value line products contain a 10-bit successive approximation A/D converter (ADC2) with up to 10 multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DDA}
- Conversion time: 14 clock cycles
- Single and continuous modes
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: full feature UART, SPI emulation, LIN2.1 master capability, SmartCard mode, IrDA mode, single wire mode.
- UART3: full feature UART, LIN2.1 master/slave capability
- SPI: full and half-duplex, 10 Mbit/s
- I²C: up to 400 Kbit/s

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4.14.1 UART1

Main features

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

LIN master mode

- Emission: generates 13-bit synch. break frame
- Reception: detects 11-bit break frame

4.14.2 UART3

Main features

- 1 Mbit/s full duplex SCI
- LIN master capable
- High precision baud rate generator

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Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master capability

- Emission: Generates 13-bit synch break frame
- Reception: Detects 11-bit break frame

LIN slave mode

- Autonomous header handling - one single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation ±15 %
- Synch delimiter checking
- 11-bit LIN synch break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

4.14.3 SPI

- Maximum speed: 10 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

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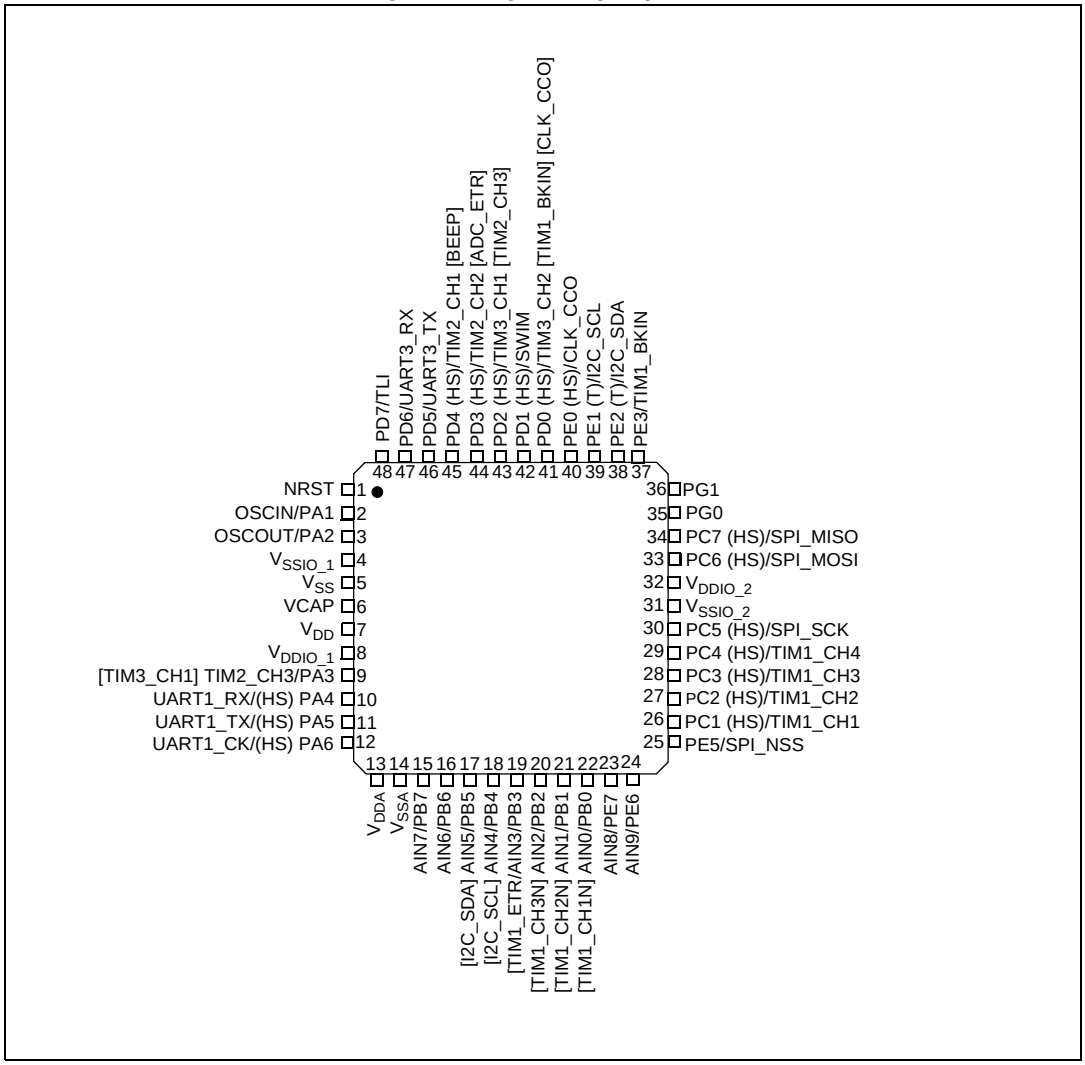
4.14.4 I²C

- I²C master features
  - Clock generation
  - Start and stop generation
- I²C slave features
  - Programmable I²C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

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5 Pinouts and pin descriptions

Figure 3. LQFP 48-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

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Table 4. Legend/abbreviations for STM8S007C8 pin description table

Type	I = input, O = output, S = power supply	
Input	floating	
	wpu = weak pull-up	
	Ext. interrupt = external interrupt	
Output	HS = high sink	
	Speed	O1 = Slow (up to 2 MHz)
		O3 = Fast/slow programmability with slow as default state after reset
		O4 = Fast/slow programmability with fast as default state after reset
	OD = open drain	
	PP = push pull	
Reset state	Bold **X** (pin state after internal reset release) Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

Table 5. STM8S007C8 pin description

Pin number	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	NRST	I/O		**X**						Reset		
2	PA1/OSCIN	I/O	**X**	X			O1	X	X	**Port A1**	Resonator/ crystal in	
3	PA2/OSCOUT	I/O	**X**	X	X		O1	X	X	**Port A2**	Resonator/ crystal out	
4	V_{SSIO_1}	S								I/O ground		
5	V_{SS}	S								Digital ground		
6	VCAP	S								1.8 V regulator capacitor		
7	V_{DD}	S								Digital power supply		
8	V_{DDIO_1}	S								I/O power supply		
9	PA3/TIM2_CH3	I/O	**X**	X	X		O1	X	X	**Port A3**	Timer 2 - channel3	TIM3_CH1 [AFR1]
10	PA4/UART1_RX (1)	I/O	**X**	X	X	HS	O3	X	X	**Port A4**	UART1 receive	
11	PA5/UART1_TX	I/O	**X**	X	X	HS	O3	X	X	**Port A5**	UART1 transmit	
12	PA6/UART1_CK	I/O	**X**	X	X	HS	O3	X	X	**Port A6**	UART1 synchronous clock	

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Table 5. STM8S007C8 pin description (continued)

Pin number	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
13	V_{DDA}	S								Analog power supply		
14	V_{SSA}	S								Analog ground		
15	PB7/AIN7	I/O	**X**	X	X		O1	X	X	**Port B7**	Analog input 7	
16	PB6/AIN6	I/O	**X**	X	X		O1	X	X	**Port B6**	Analog input 6	
17	PB5/AIN5	I/O	**X**	X	X		O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
18	PB4/AIN4	I/O	**X**	X	X		O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
19	PB3/AIN3	I/O	**X**	X	X		O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
20	PB2/AIN2	I/O	**X**	X	X		O1	X	X	**Port B2**	Analog input 2	TIM1_ CH3N [AFR5]
21	PB1/AIN1	I/O	**X**	X	X		O1	X	X	**Port B1**	Analog input 1	TIM1_ CH2N [AFR5]
22	PB0/AIN0	I/O	**X**	X	X		O1	X	X	**Port B0**	Analog input 0	TIM1_ CH1N [AFR5]
23	PE7/AIN8	I/O	**X**	X	X		O1	X	X	**Port E7**	Analog input 8	
24	PE6/AIN9	I/O	**X**	X	X		O1	X	X	**Port E6**	Analog input 9	
25	PE5/SPI_NSS	I/O	**X**	X	X		O1	X	X	**Port E5**	SPI master/slave select	
26	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	
27	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	
28	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	
29	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	
30	PC5/SPI_SCK	I/O	**X**	X	X	HS	O3	X	X	**Port C5**	SPI clock	
31	V_{SSIO_2}	S								I/O ground		
32	V_{DDIO_2}	S								I/O power supply		

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Table 5. STM8S007C8 pin description (continued)

Pin number	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
33	PC6/SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	**Port C6**	SPI master out/ slave in	
34	PC7/SPI_MISO	I/O	**X**	X	X	HS	O3	X	X	**Port C7**	SPI master in/ slave out	
35	PG0	I/O	**X**	X			O1	X	X	**Port G0**		
36	PG1	I/O	**X**	X			O1	X	X	**Port G1**		
37	PE3/TIM1_BKIN	I/O	**X**	X	X		O1	X	X	**Port E3**	Timer 1 - break input	
38	PE2/I^2C_SDA	I/O	**X**		X		O1	T(2)		**Port E2**	I^2C data	
39	PE1/I^2C_SCL	I/O	**X**		X		O1	T(2)		**Port E1**	I^2C clock	
40	PE0/CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	**Port E0**	Configurable clock output	
41	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
42	PD1/SWIM(3)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	
43	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
44	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
45	PD4/TIM2_CH1/BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
46	PD5/ UART3_TX	I/O	**X**	X	X		O1	X	X	**Port D5**	UART3 data transmit	
47	PD6/ UART3_RX(1)	I/O	**X**	X	X		O1	X	X	**Port D6**	UART3 data receive	
48	PD7/TLI	I/O	**X**	X	X		O1	X	X	**Port D7**	Top level interrupt	

1. The default state of UART1_RX and UART3_RX pins is controlled by the ROM bootloader. These pins are pulled up as part of the bootloader activation process and returned to the floating state before a return from the bootloader.
2. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented).
3. The PD1 pin is in input pull-up during the reset phase and after the internal reset release.

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Note: The slope control of true open drain pins cannot be programmed and by default is limited to 2 MHz.

5.1 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 8: Option bytes*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

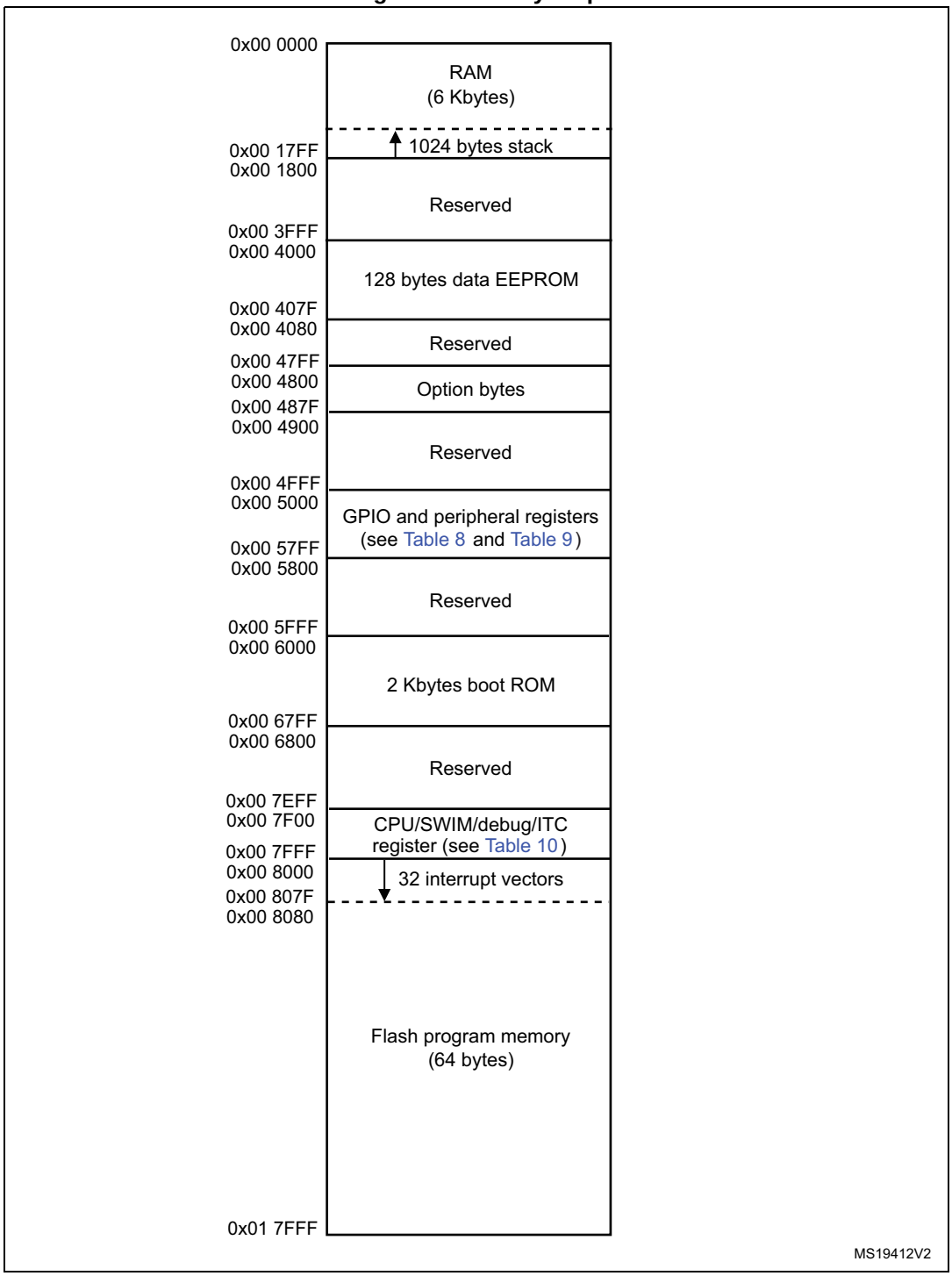
Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

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6 Memory and register map

6.1 Memory map

Figure 4. Memory map



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Table 6 lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

Table 6. Flash, Data EEPROM and RAM boundary addresses

Memory area	Size (bytes)	Start address	End address
Flash program memory	64 K	0x00 8000	0x01 7FFF
RAM	6 K	0x00 0000	0x00 17FF
Data EEPROM	128	0x00 4000	0x00 407F

6.2 Register map

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0x00
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0x00
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0x00
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0x00
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

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Table 7. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0x00
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0x00
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0x00
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0x00
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0x00
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

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Table 8. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5050 to 0x00 5059	Reserved area (10 bytes)			
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH _FPR	Flash protection register	0x00
0x00 505E		FLASH _NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5060 to 0x00 5061	Reserved area (2 bytes)			
0x00 5062	Flash	FLASH _PUKR	Flash Program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 bytes)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 bytes)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB	Reserved area (1 byte)			

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50CC	CLK	CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 bytes)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX(2)
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 bytes)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I^2C	I2C_CR1	I^2C control register 1	0x00
0x00 5211		I2C_CR2	I^2C control register 2	0x00
0x00 5212		I2C_FREQR	I^2C frequency register	0x00
0x00 5213		I2C_OARL	I^2C own address register low	0x00
0x00 5214		I2C_OARH	I^2C own address register high	0x00
0x00 5215		Reserved		

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5216	I²C	I2C_DR	I²C data register	0x00
0x00 5217		I2C_SR1	I²C status register 1	0x00
0x00 5218		I2C_SR2	I²C status register 2	0x00
0x00 5219		I2C_SR3	I²C status register 3	0x00
0x00 521A		I2C_ITR	I²C interrupt control register	0x00
0x00 521B		I2C_CCRL	I²C clock control register low	0x00
0x00 521C		I2C_CCRH	I²C clock control register high	0x00
0x00 521D		I2C_TRISER	I²C TRISE register	0x02
0x00 521E to 0x00 522F	Reserved area (18 bytes)			
0x00 5230	UART1	UART1_SR	UART1 status register	0xC0
0x00 5231		UART1_DR	UART1 data register	0xXX
0x00 5232		UART1_BRR1	UART1 baud rate register 1	0x00
0x00 5233		UART1_BRR2	UART1 baud rate register 2	0x00
0x00 5234		UART1_CR1	UART1 control register 1	0x00
0x00 5235		UART1_CR2	UART1 control register 2	0x00
0x00 5236		UART1_CR3	UART1 control register 3	0x00
0x00 5237		UART1_CR4	UART1 control register 4	0x00
0x00 5238		UART1_CR5	UART1 control register 5	0x00
0x00 5239		UART1_GTR	UART1 guard time register	0x00
0x00 523A		UART1_PSCR	UART1 prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (5 bytes)			
0x00 5240	UART3	UART3_SR	UART3 status register	C0h
0x00 5241		UART3_DR	UART3 data register	0xXX
0x00 5242		UART3_BRR1	UART3 baud rate register 1	0x00
0x00 5243		UART3_BRR2	UART3 baud rate register 2	0x00
0x00 5244		UART3_CR1	UART3 control register 1	0x00
0x00 5245		UART3_CR2	UART3 control register 2	0x00
0x00 5246		UART3_CR3	UART3 control register 3	0x00
0x00 5247		UART3_CR4	UART3 control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART3_CR6	UART3 control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
00 530C0x		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5314		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 bytes)			
0x00 5320	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5321		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5322		TIM3_SR1	TIM3 status register 1	0x00
0x00 5323		TIM3_SR2	TIM3 status register 2	0x00
0x00 5324		TIM3_EGR	TIM3 event generation register	0x00
0x00 5325		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5326		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 5327		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 5328		TIM3_CNTRH	TIM3 counter high	0x00
0x00 5329		TIM3_CNTRL	TIM3 counter low	0x00
0x00 532A		TIM3_PSCR	TIM3 prescaler register	0x00

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 532B	TIM3	TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 532C		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 532D		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 532E		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 532F		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5330		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5331 to 0x00 533F	Reserved area (15 bytes)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5342		TIM4_SR	TIM4 status register	0x00
0x00 5343		TIM4_EGR	TIM4 event generation register	0x00
0x00 5344		TIM4_CNTR	TIM4 counter	0x00
0x00 5345		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5346		TIM4_ARR	TIM4 auto-reload register	0xFF
0x00 5347 to 0x00 53FF	Reserved area (185 bytes)			
0x00 5400	ADC2	ADC _CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408 to 0x00 57FF	Reserved area (1016 bytes)			

1. Depends on the previous reset source.
2. Write only register.

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Table 9. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register Label	Register Name	Reset Status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x17(2)
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			

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Table 9. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register Label	Register Name	Reset Status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only
2. Product dependent value, see *Figure 4: Memory map*.

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7 Interrupt vector mapping

Table 10. Interrupt mapping

IRQ no.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Vector address
-	RESET	Reset	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level interrupt	-	-	0x00 8008
1	AWU	Auto wake up from halt	-	Yes	0x00 800C
2	CLK	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8	Reserved				0x00 8028
9	Reserved				0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/overflow/underflow/ trigger/break	-	-	0x00 8034
12	TIM1	TIM1 capture/compare	-	-	0x00 8038
13	TIM2	TIM2 update /overflow	-	-	0x00 803C
14	TIM2	TIM2 capture/compare	-	-	0x00 8040
15	TIM3	Update/overflow	-	-	0x00 8044
16	TIM3	Capture/compare	-	-	0x00 8048
17	UART1	Tx complete	-	-	0x00 804C
18	UART1	Receive register DATA FULL	-	-	0x00 8050
19	I^2C	I^2C interrupt	Yes	Yes	0x00 8054
20	UART3	Tx complete	-	-	0x00 8058
21	UART3	Receive register DATA FULL	-	-	0x00 805C
22	ADC2	ADC2 end of conversion	-	-	0x00 8060
23	TIM4	TIM4 update/overflow	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068
Reserved					0x00 806C to 0x00 807C

1. Except PA1

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8 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 11: Option bytes* below. Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 11. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
4800h	Read-out protection (ROP)	OPT0	ROP[7:0]								00h
4801h	User boot code (UBC)	OPT1	UBC[7:0]								00h
4802h		NOPT1	NUBC[7:0]								FFh
4803h	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	Reserved	AFR3	AFR2	AFR1	AFR0	00h
4804h		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	FFh
4805h	Watchdog option	OPT3	Reserved				LSI_EN	IWDG_HW	WWDG_HW	WWDG_HALT	00h
4806h		NOPT3	Reserved				NLSI_EN	NIWDG_HW	NWWDG_HW	NWWDG_HALT	FFh
4807h	Clock option	OPT4	Reserved				EXTCLK	CKAWUSEL	PRSC1	PRSC0	00h
4808h		NOPT4	Reserved				NEXTCLK	NCKAWUSEL	NPRSC1	NPRSC0	FFh
4809h	HSE clock startup	OPT5	HSECNT[7:0]								00h
480Ah		NOPT5	NHSECNT[7:0]								FFh
480Bh	Reserved	OPT6	Reserved								00h
480Ch		NOPT6	Reserved								FFh
480Dh	Flash wait states	OPT7	Reserved							Wait state	00h
480Eh		NOPT7	Reserved							Nwait state	FFh
487Eh	Bootloader	OPTBL	BL[7:0]								00h
487Fh		NOPTBL	NBL[7:0]								FFh

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Table 12. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** *Memory readout protection (ROP)* 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** *User boot code area* 0x00: no UBC, no write-protection 0x01: Pages 0 to 1 defined as UBC, memory write-protected 0x02: Pages 0 to 3 defined as UBC, memory write-protected 0x03: Pages 0 to 4 defined as UBC, memory write-protected ... 0xFE: Pages 0 to 255 defined as UBC, memory write-protected 0xFF: Reserved *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7***Alternate function remapping option 7* 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP **AFR6** *Alternate function remapping option 6* 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL **AFR5** *Alternate function remapping option 5* 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N **AFR4** *Alternate function remapping option 4* Reserved **AFR3** *Alternate function remapping option 3* 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN **AFR2** *Alternate function remapping option 2* 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO Note: AFR2 option has priority over AFR3 if both are activated **AFR1** *Alternate function remapping option 1* 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3 **AFR0** *Alternate function remapping option 0* 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

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Table 12. Option byte description (continued)

Option byte no.	Description
OPT3	**LSI_EN:** *Low speed internal clock enable* 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: *Independent watchdog* 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: *Window watchdog activation* 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: *Window watchdog reset on halt* 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active
OPT4	**EXTCLK:** *External clock selection* 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: *Auto wakeup unit/clock* 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for for AWU
	PRSC[1:0] AWU clock prescaler 00: 24 MHz to 128 kHz prescaler 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** *HSE crystal oscillator stabilization time* This configures the stabilization time. 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles
OPT6	Reserved
OPT7	**WAITSTATE** *Wait state configuration* This option configures the number of wait states inserted when reading from the Flash/data EEPROM memory. 1 wait state is required if f_{CPU} > 16 MHz. 0: No wait state 1: 1 wait state

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Table 12. Option byte description (continued)

Option byte no.	Description
OPTBL	**BL[7:0]** *Bootloader option byte* For STM8S products, this option is checked by the boot ROM code after reset. Depending on the content of addresses 0x487E, 0x487F, and 0x8000 (reset vector), the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 (STM8L/S bootloader manual) for more details. For STM8L products, the bootloader option bytes are on addresses 0xXXXX and 0xXXXX+1 (2 bytes). These option bytes control whether the bootloader is active or not. For more details, refer to the UM0560 (STM8L/S bootloader manual) for more details.

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9 Electrical characteristics

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

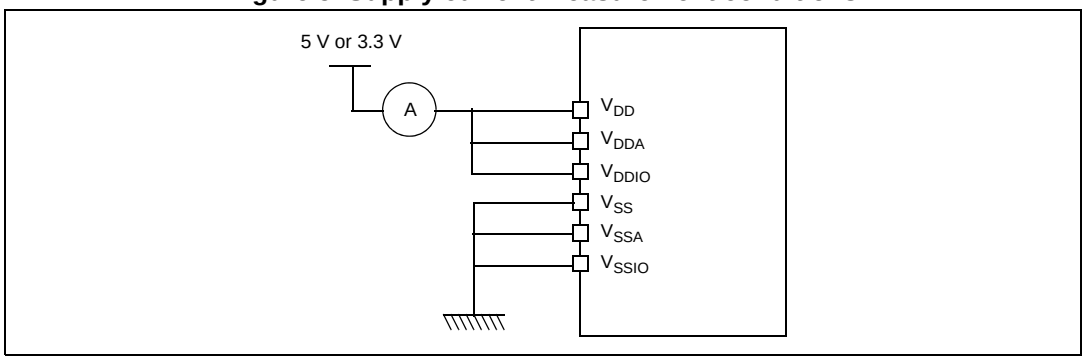
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Typical current consumption

For typical current consumption measurements, V_{DD}, V_{DDIO} and V_{DDA} are connected together in the configuration shown in *Figure 5*.

Figure 5. Supply current measurement conditions



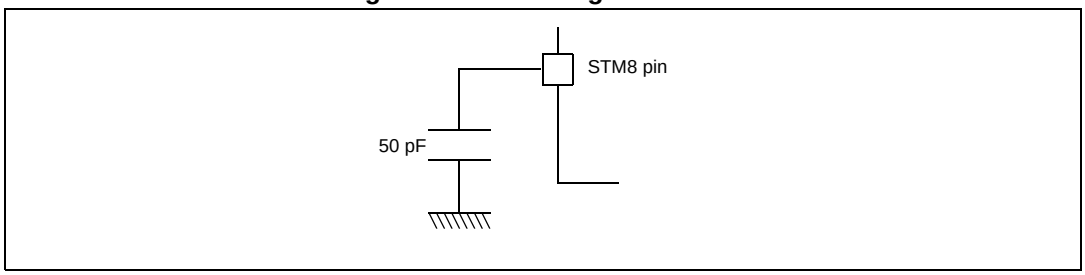
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9.1.5 Pin loading conditions

9.1.6 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

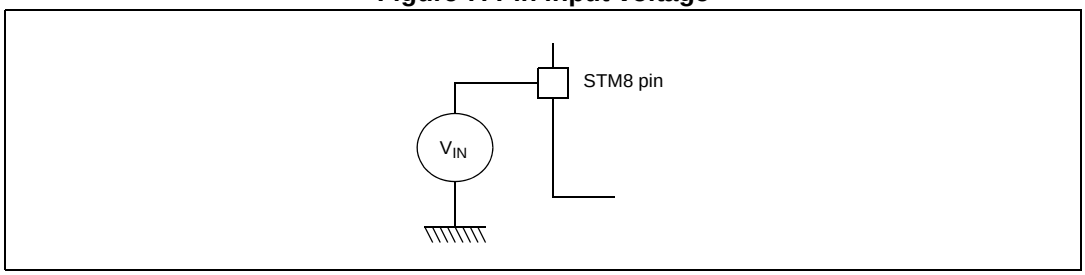
Figure 6. Pin loading conditions



9.1.7 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage



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9.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD}\rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 81*		-

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

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Table 14. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	60	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	60	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	20	
ΣI_{IO}	Total output current sourced (sum of all I/O and control pins) for devices with two V_{DDIO} pins(3)	200	
	Total output current sourced (sum of all I/O and control pins) for devices with one V_{DDIO} pin(3)	100	
	Total output current sunk (sum of all I/O and control pins) for devices with two V_{SSIO} pins(3)	160	
	Total output current sunk (sum of all I/O and control pins) for devices with one V_{SSIO} pin(3)	80	
$I_{INJ(PIN)}$(4)(5)	Injected current on NRST pin	±4	
	Injected current on OSCIN pin	±4	
	Injected current on any other pin(6)	±4	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(6)	±20	

1. Data based on characterization results, not tested in production.
2. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
3. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package between the V_{DDIO}/V_{SSIO} pins.
4. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
5. Negative injection disturbs the analog performance of the device. See note in *Section 9.3.10: 10-bit ADC characteristics on page 77*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

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9.3 Operating conditions

The device must be used in operating conditions that respect the parameters in *Table 16*. In addition, full account must be taken of all physical capacitor characteristics and tolerances.

Table 16. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	24	MHz
		-	0	16	
V_{DD}/V_{DD_IO}	Standard operating voltage	-	2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	At 1 MHz(2)	-	0.3	ohm
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 85° C for suffix 6	48-pin devices, with output on eight standard ports, two high sink ports and two open drain ports simultaneously(4)	-	443	mW
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
T_J	Junction temperature range	-	-40	105	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter specifications must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by the design of the internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ (see *Section 10.2: Thermal characteristics on page 86*) with the value for T_{Jmax} given in *Table 16* above and the value for Θ_{JA} given in *Table 50: Thermal characteristics*.
4. Refer to *Section 10.2: Thermal characteristics on page 86* for the calculation method.

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Figure 8. f_{CPUmax} versus V_{DD}

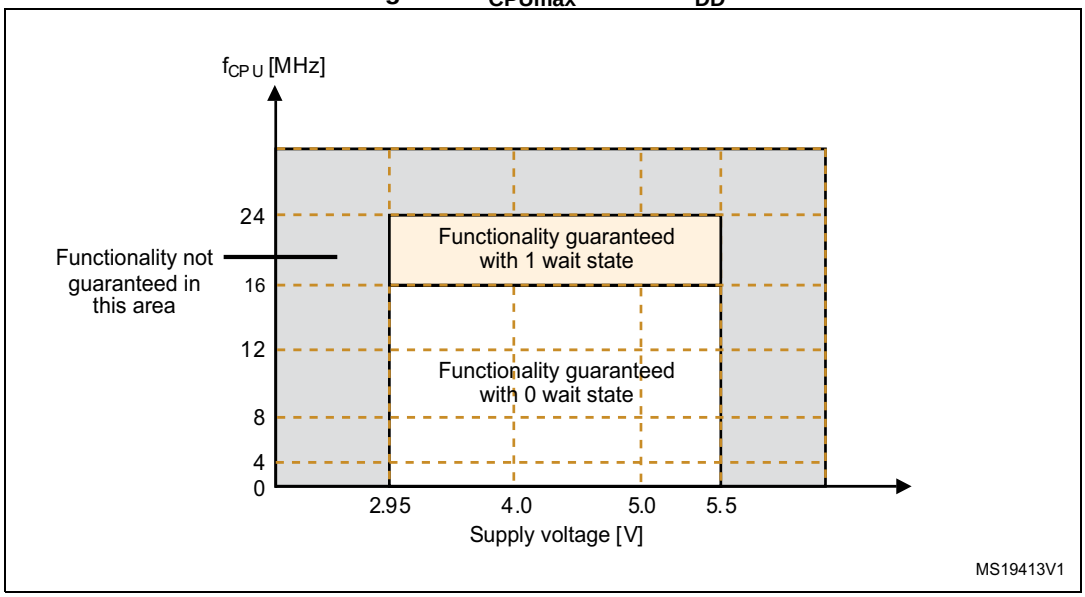


Table 17. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2(1)	-	∞	µs/V
	V_{DD} fall time rate	-	2(1)	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7(1)	ms
V_{IT+}	Power-on reset threshold(2)	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.73	2.88	V
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

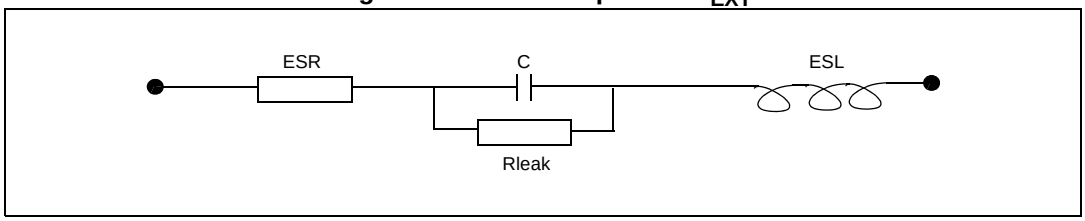
1. Guaranteed by design, not tested in production.
2. If V_{DD} is below 2.95 V, the code execution is guaranteed above the V_{IT-} and $_{VIT+}$ thresholds. RAM content is kept. The EEPROM programming sequence must not be initiated.

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9.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 16*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 9. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

9.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 5 on page 42*.

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by Peripheral Clock Gating registers) except if explicitly mentioned.
- When the MCU is clocked at 24 MHz, $T_A \leq 85$ °C and the WAITSTATE option bit is set.

Subject to general operating conditions for V_{DD} and T_A.

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Table 18. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 24 MHz	HSE crystal osc. (24 MHz)	4.4	-	mA
			HSE user ext. clock (24 MHz)	3.7	7.3(1)	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	3.3	-	
			HSE user ext. clock (16 MHz)	2.7	5.8	
			HSI RC osc. (16 MHz)	2.5	3.4	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSE user ext. clock (16 MHz)	1.2	4.1(1)	
			HSI RC osc. (16 MHz)	1.0	1.3(1)	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.55	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.45	-	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 24 MHz	HSE crystal osc. (24 MHz)	11.4	-	
			HSE user ext. clock (24 MHz)	10.8	18(1)	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	9.0	-	
			HSE user ext. clock (16 MHz)	8.2	15.2(1)	
			HSI RC osc.(16 MHz)	8.1	13.2(1)	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	1.5	-	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.1	-	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.6	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.55	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

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Table 19. Total current consumption with code execution in run mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 24 MHz	HSE crystal osc. (24 MHz)	4.0	-	mA
			HSE user ext. clock (24 MHz)	3.7	7.3	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.9	-	
			HSE user ext. clock (16 MHz)	2.7	5.8	
			HSI RC osc. (16 MHz)	2.5	3.4	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSE user ext. clock (16 MHz)	1.2	4.1	
			HSI RC osc. (16 MHz)	1.0	1.3	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16MHz/8)	0.55	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.45	-	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 24 MHz	HSE crystal osc. (24 MHz)	11.0	-	
			HSE user ext. clock (24 MHz)	10.8	18.0	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	8.4	-	
			HSE user ext. clock (16 MHz)	8.2	15.2	
			HSI RC osc. (16 MHz)	8.1	13.2	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	1.5	-	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.1	-	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.6	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.55	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration.

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Total current consumption in wait mode

Table 20. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 24 MHz	HSE crystal osc. (24 MHz)	2.4	-	mA
			HSE user ext. clock (24 MHz)	1.8	4.7	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.0	-	
			HSE user ext. clock (16 MHz)	1.4	4.4	
			HSI RC osc. (16 MHz)	1.2	1.6	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.0	-	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.55	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.5	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 21. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 24 MHz	HSE crystal osc. (24 MHz)	2.0	-	mA
			HSE user ext. clock (24 MHz)	1.8	4.7	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6	-	
			HSE user ext. clock (16 MHz)	1.4	4.4	
			HSI RC osc. (16 MHz)	1.2	1.6	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.0	-	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.55	-	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	LSI RC osc. (128 kHz)	0.5	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

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Total current consumption in active halt mode

Table 22. Total current consumption in active halt mode at V_{DD} = 5 V, T_A -40 to 85° C

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source			
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal oscillator (16 MHz)	1000	-	µA
				LSI RC oscillator (128 kHz)	200	260	
			Power-down mode	HSE crystal oscillator (16 MHz)	940	-	
				LSI RC oscillator (128 kHz)	140	-	
		Off	Operating mode	LSI RC oscillator (128 kHz)	68	-	
			Power-down mode		11	45	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 23. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source		
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	600	µA
				LSI RC osc. (128 kHz)	200	
			Power-down mode	HSE crystal osc. (16 MHz)	540	
				LSI RC osc. (128 kHz)	140	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	
			Power-down mode		9	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

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Total current consumption in halt mode

Table 24. Total current consumption in halt mode at V_{DD} = 5 V, T_A -40 to 85° C

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63.5	-	µA
		Flash in power-down mode, HSI clock after wakeup	6.5	35	

Table 25. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	61.5	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	

Low-power mode wakeup times

Table 26. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(3)	-			-	(2)	µs
		$f_{CPU} = f_{MASTER}$ = 16 MHz.			0.56	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode.(3)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
			Flash in power-down mode(5)		3(6)	-	
		MVR voltage regulator off(4)	Flash in operating mode(5)		48(6)	-	
			Flash in power-down mode(5)		50(6)	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(3)	Flash in operating mode(5)			52	-	
		Flash in power-down mode(5)			54	-	

1. Data guaranteed by design, not tested in production.
2. $t_{WU(WFI)} = 2 \times 1/f_{master} + 7 \times 1/f_{CPU}$
3. Measured from interrupt event to interrupt vector fetch.
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

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Total current consumption and timing in forced reset state

Table 27. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$I_{DD(R)}$	Supply current in reset state	V_{DD} = 5 V	1.6	-	mA
		V_{DD} = 3.3 V	0.8	-	
$t_{RESETBL}$	Reset release to bootloader vector fetch	-	-	150	µs

1. Data guaranteed by design, not tested in production.

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU} = f_{MASTER} = 16 MHz.

Table 28. Peripheral current consumption

Symbol	Parameter	Typ.	Unit
$I_{DD(TIM1)}$	TIM1 supply current (1)	220	µA
$I_{DD(TIM2)}$	TIM2 supply current (1)	120	
$I_{DD(TIM3)}$	TIM3 timer supply current (1)	100	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)	25	
$I_{DD(UART1)}$	UART1 supply current (2)	90	
$I_{DD(UART3)}$	UART3 supply current (2)	110	
$I_{DD(SPI)}$	SPI supply current (2)	40	
$I_{DD(I2C)}$	I^2C supply current (2)	50	
$I_{DD(ADC2)}$	ADC2 supply current when converting (3)	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions. Not tested in production.

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Current consumption curves

Figure 10 and *Figure 11* show typical current consumption measured with code executing in RAM.

Figure 10. Typ. $I_{DD(RUN)}$ vs V_{DD}, HSI RC osc, f_{CPU} = 16 MHz

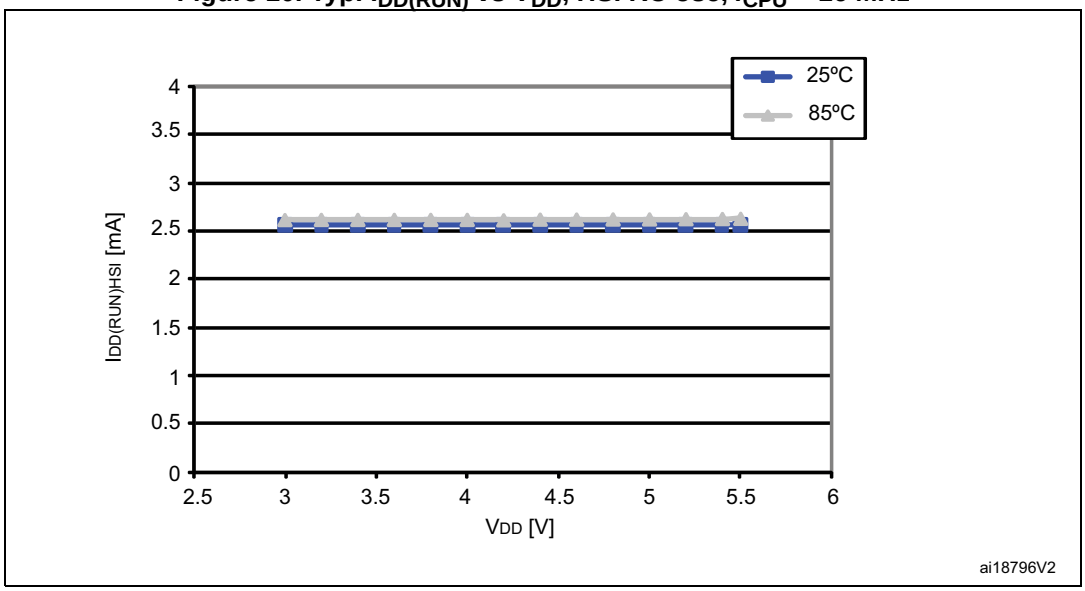
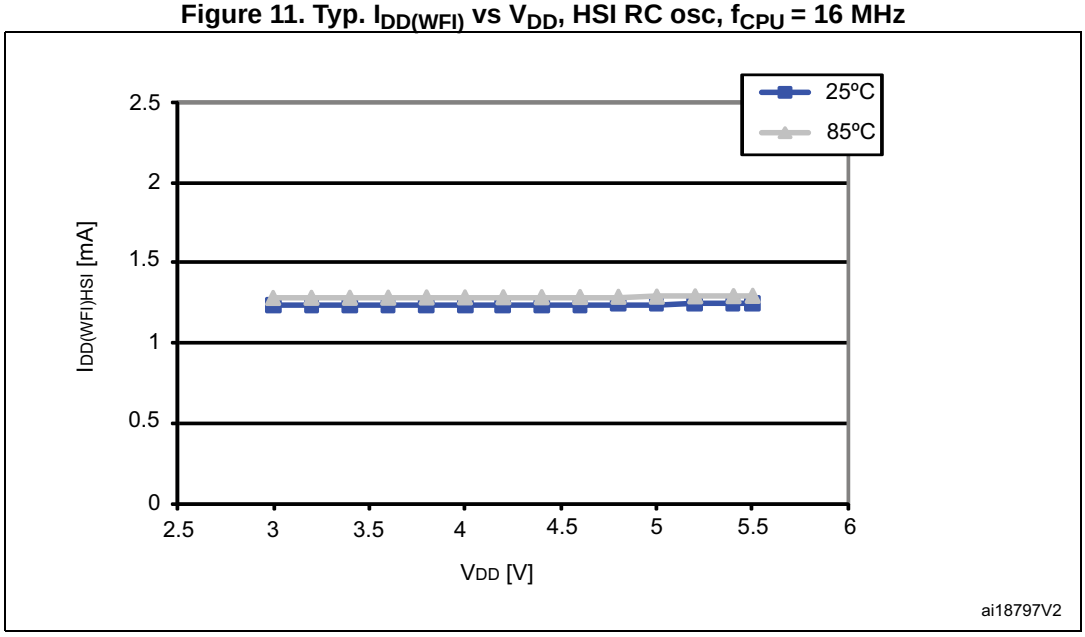


Figure 11. Typ. $I_{DD(WFI)}$ vs V_{DD}, HSI RC osc, f_{CPU} = 16 MHz



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9.3.3 External clock sources and timing characteristics

HSE user external clock

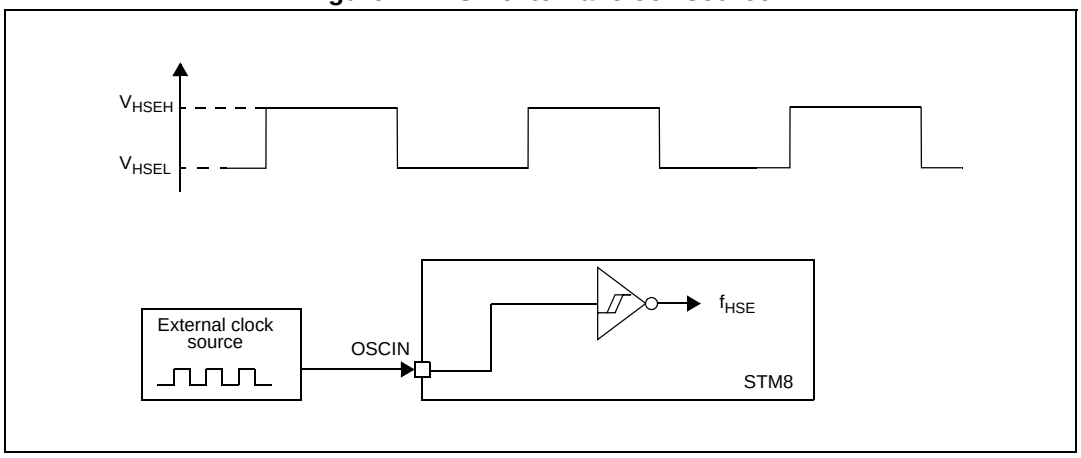
Subject to general operating conditions for V_{DD} and T_A.

Table 29. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	-	24	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage		V_{SS}	-	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	1	µA

1. Data based on characterization results, not tested in production.

Figure 12. HSE external clock source



HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

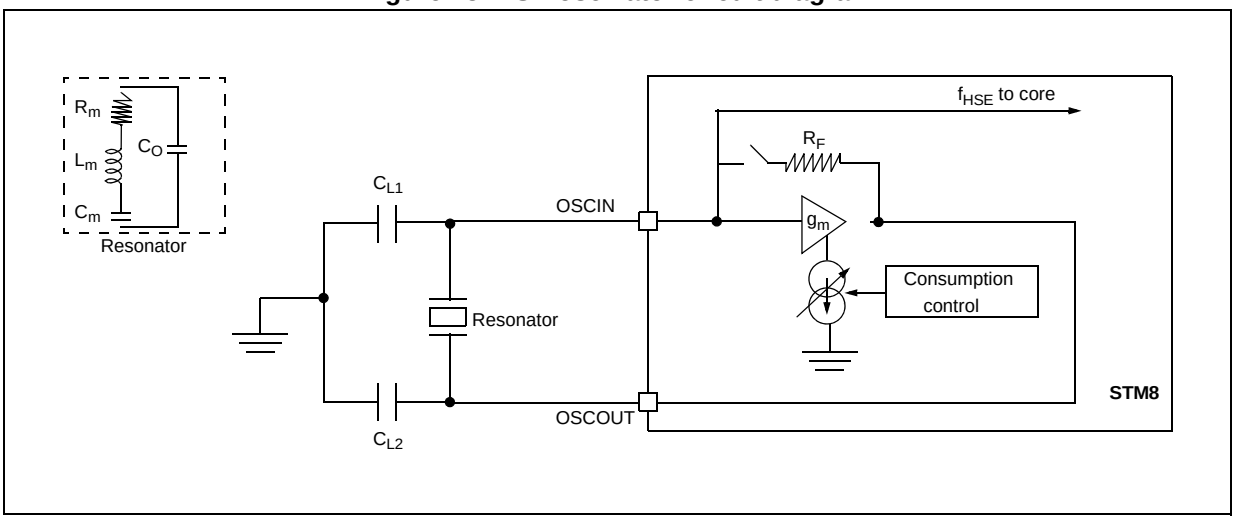
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Table 30. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency	-	1	-	24	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance (2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 24 MHz	-	-	6 (startup) 2 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 24 MHz	-	-	6 (startup) 1.5 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 13. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
C_{L1}=C_{L2}=C: Grounded external capacitance
g_m >> g_{mcrit}

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9.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A. f_{HSE}

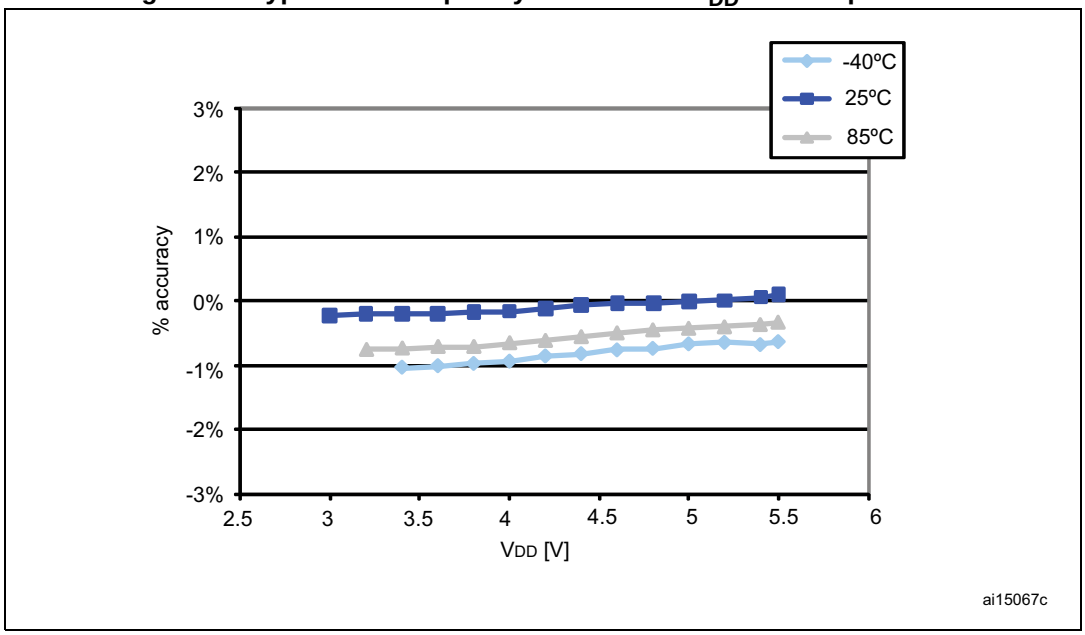
High speed internal RC oscillator (HSI)

Table 31. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	Accuracy of HSI oscillator	Trimmed by the CLK_HSITRIMR register for given V_{DD} and T_A conditions	-1.0(1)	-	1.0	%
	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 5 V, T_A = 25 °C	-	5	-	
		V_{DD} = 5 V, -40 °C ≤ T_A ≤ 85 °C	-5	-	5	
$t_{su(HSI)}$	HSI oscillator wakeup time including calibration	-	-	-	1.0(1)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	170	250(2)	µA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production

Figure 14. Typical HSI frequency variation vs V_{DD} at 3 temperatures



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Low speed internal RC oscillator (LSI)

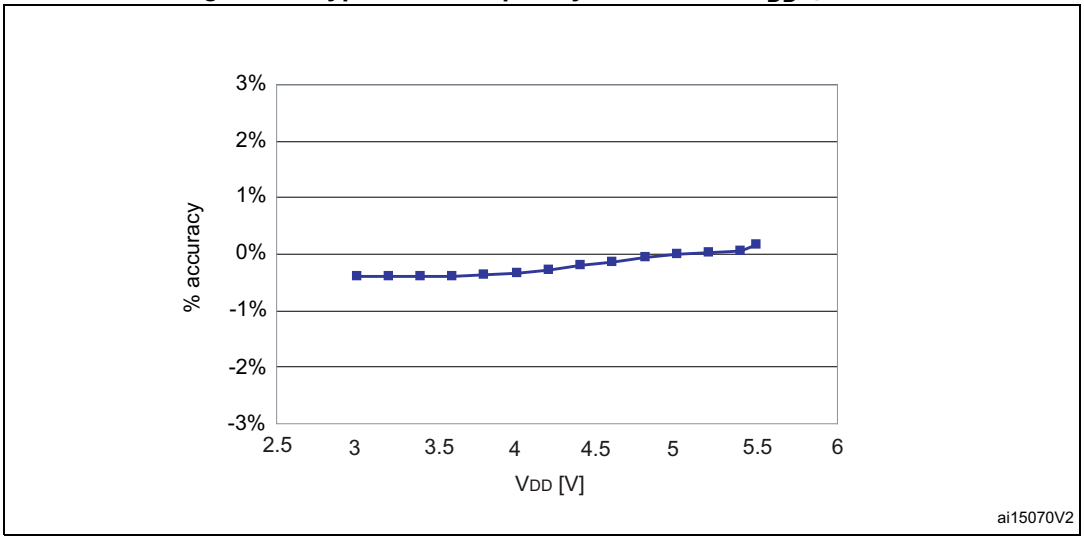
Subject to general operating conditions for V_{DD} and T_A.

Table 32. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	128	-	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7(1)	µs
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	5	-	µA

1. Guaranteed by design, not tested in production.

Figure 15. Typical LSI frequency variation vs V_{DD} @ 25 °C



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9.3.5 Memory characteristics

RAM and hardware registers

Table 33. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	V_{IT-max}(2)	V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production.
2. Refer to *Table 17 on page 47* for the value of V_{IT-max}.

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 85 °C.

Table 34. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	$f_{CPU} \leq$ 16 MHz	2.95	-	5.5	V
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)	-	-	6.0	6.6	ms
	Fast programming time for 1 block (128 bytes)	-	-	3.0	3.3	ms
t_{erase}	Erase time for 1 block (128 bytes)	-	-	3.0	3.3	ms
N_{RW}	Erase/write cycles(2) (program memory)	T_A = 85 °C	100	-	-	cycles
	Erase/write cycles(2) (data memory)		100 k	-	-	
t_{RET}	Data retention (program memory) after 100 erase/write cycles at T_A = 85 °C	T_{RET} = 55° C	20	-	-	years
	Data retention (data memory) after 10 k erase/write cycles at T_A = 85 °C		20	-	-	
	Data retention (data memory) after 100 k erase/write cycles at T_A = 85 °C	T_{RET} = 85° C	1.0	-	-	
I_{DD}	Supply current (Flash programming or erasing for 1 to 128 bytes)	-	-	2.0	-	mA

1. Data based on characterization results, not tested in production.
2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

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9.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 35. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5 V	-0.3	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	V
V_{hys}	Hysteresis(1)		-	700	-	mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	30	55	80	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	20(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	ns
I_{lkg}	Input leakage current, analog and digital	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±250 (3)	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O	Injection current ±4 mA	-	-	±1(3)	µA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. Data guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

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Figure 16. Typical V_{IL} and V_{IH} vs V_{DD} @ 3 temperatures

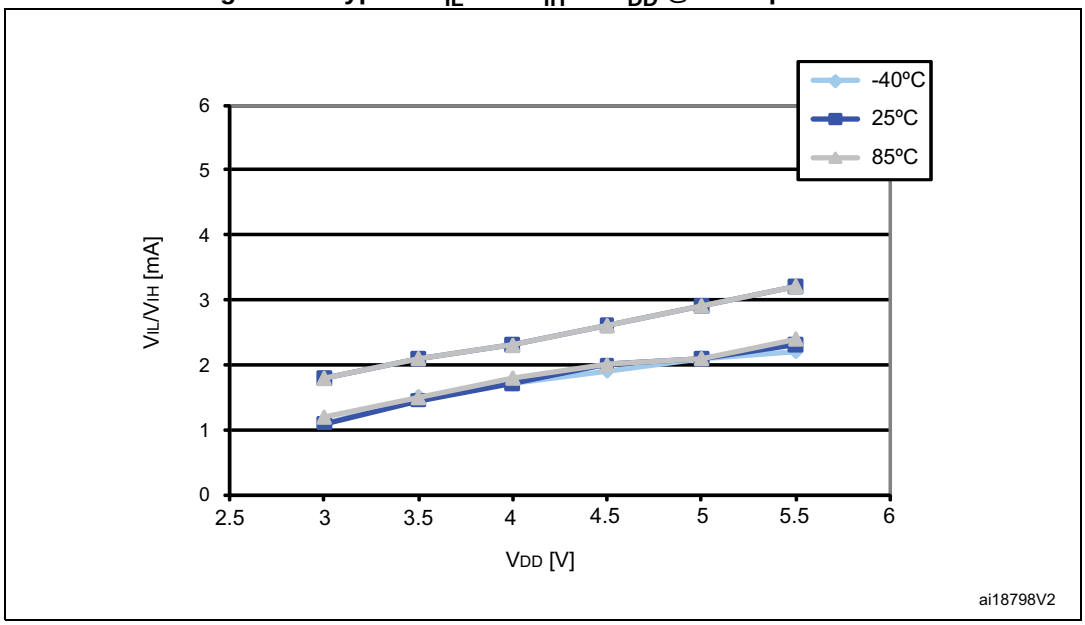
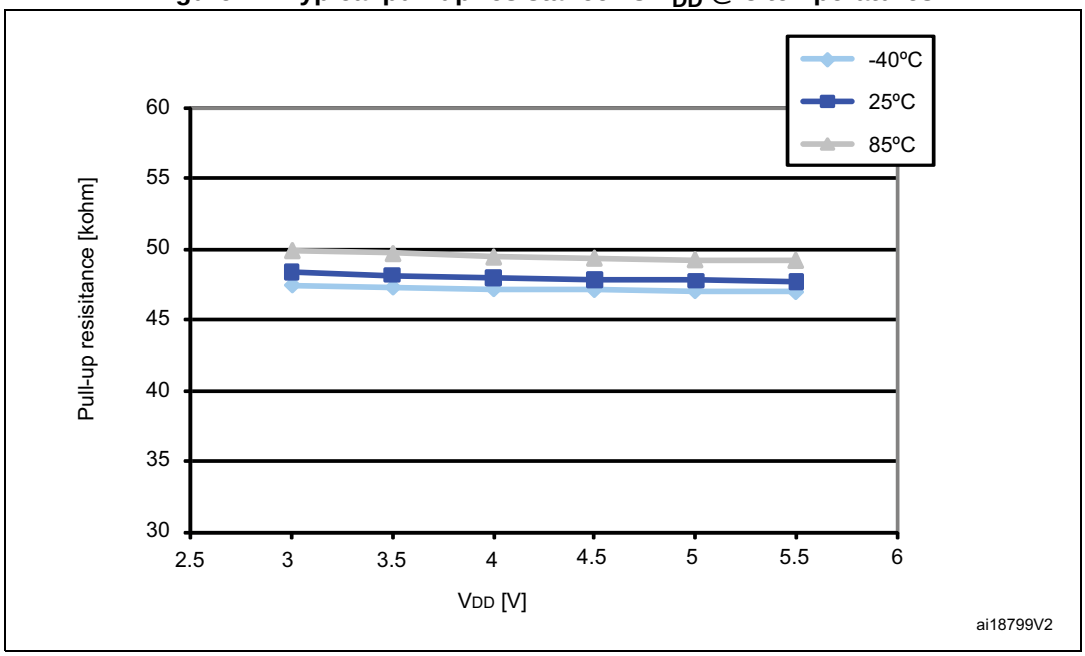
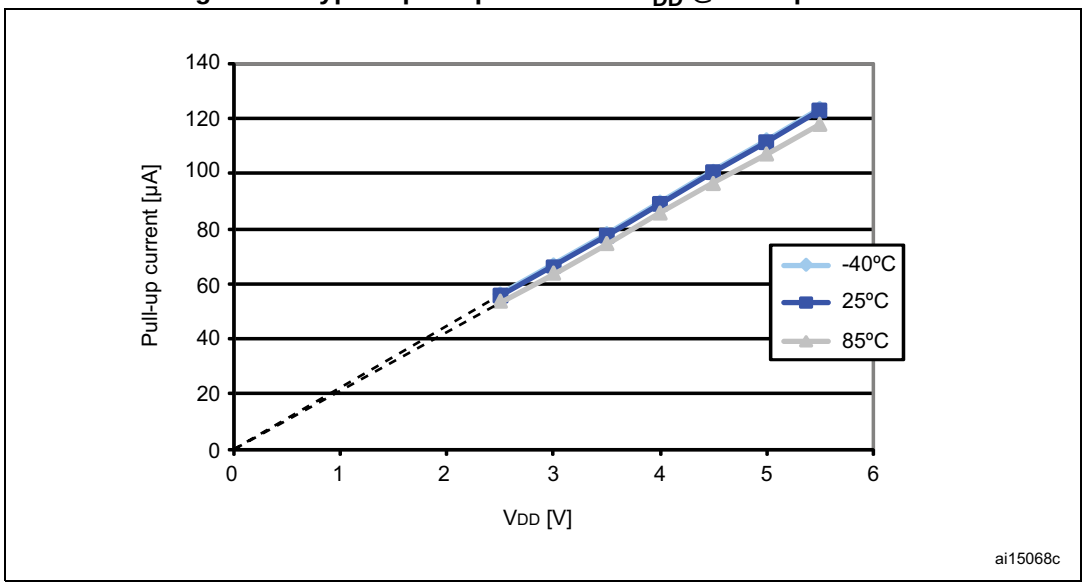


Figure 17. Typical pull-up resistance vs V_{DD} @ 3 temperatures



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Figure 18. Typical pull-up current vs V_{DD} @ 3 temperatures



1. The pull-up is a pure resistor (slope goes through 0).

Table 36. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO} = 10 mA, V_{DD} = 5 V	-	2	V
	Output low level with 4 pins sunk	I_{IO} = 4 mA, V_{DD} = 3.3 V	-	1(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	2.8	-	V
	Output high level with 4 pins sourced	I_{IO} = 4 mA, V_{DD} = 3.3 V	2.1(1)	-	

1. Data based on characterization results, not tested in production

Table 37. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO} = 10 mA, V_{DD} = 5 V	1	V
		I_{IO} = 10 mA, V_{DD} = 3.3 V	1.5(1)	
		I_{IO} = 20 mA, V_{DD} = 5 V	2(1)	

1. Data based on characterization results, not tested in production

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Table 38. Output driving current (high sink ports)

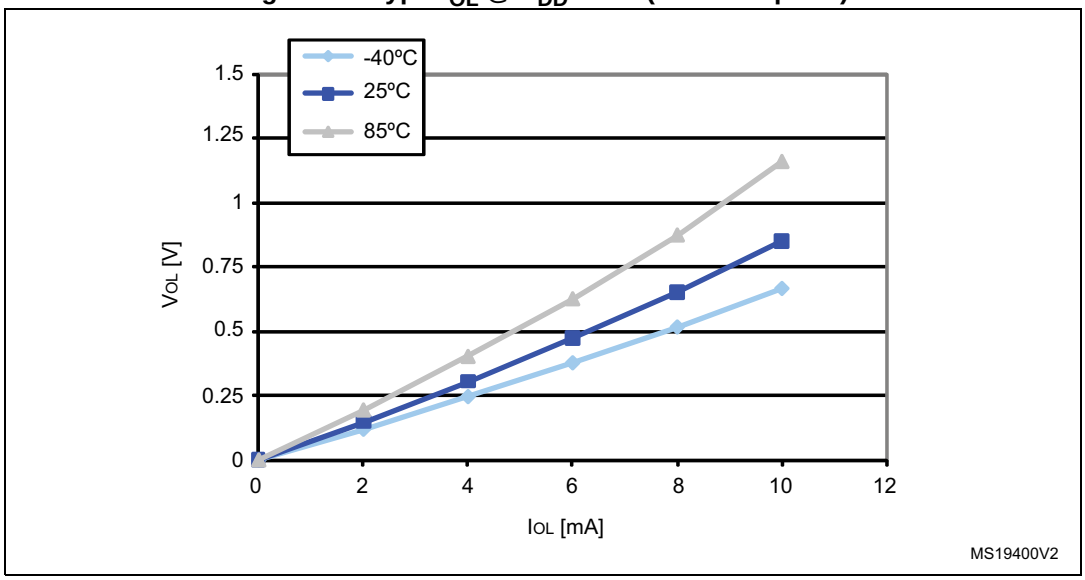
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO} = 10 mA, V_{DD} = 5 V	-	0.8	V
	Output low level with 4 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V	-	1(1)	
	Output low level with 4 pins sunk	I_{IO} = 20 mA, V_{DD} = 5 V	-	1.5(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	4.0	-	
	Output high level with 4 pins sourced	I_{IO} = 10 mA, V_{DD} = 3.3 V	2.1(1)	-	
	Output high level with 4 pins sourced	I_{IO} = 20 mA, V_{DD} = 5 V	3.3(1)	-	

1. Data based on characterization results, not tested in production

Typical output level curves

Figure 20 to *Figure 27* show typical output level curves measured with output on a single pin.

Figure 19. Typ. V_{OL} @ V_{DD} = 5 V (standard ports)



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Figure 20. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

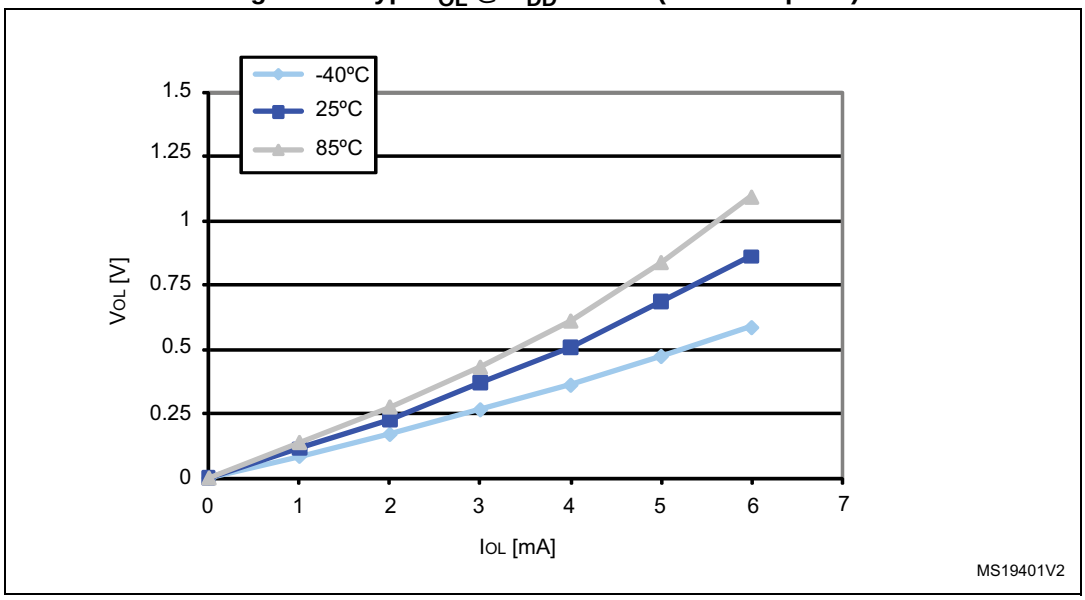
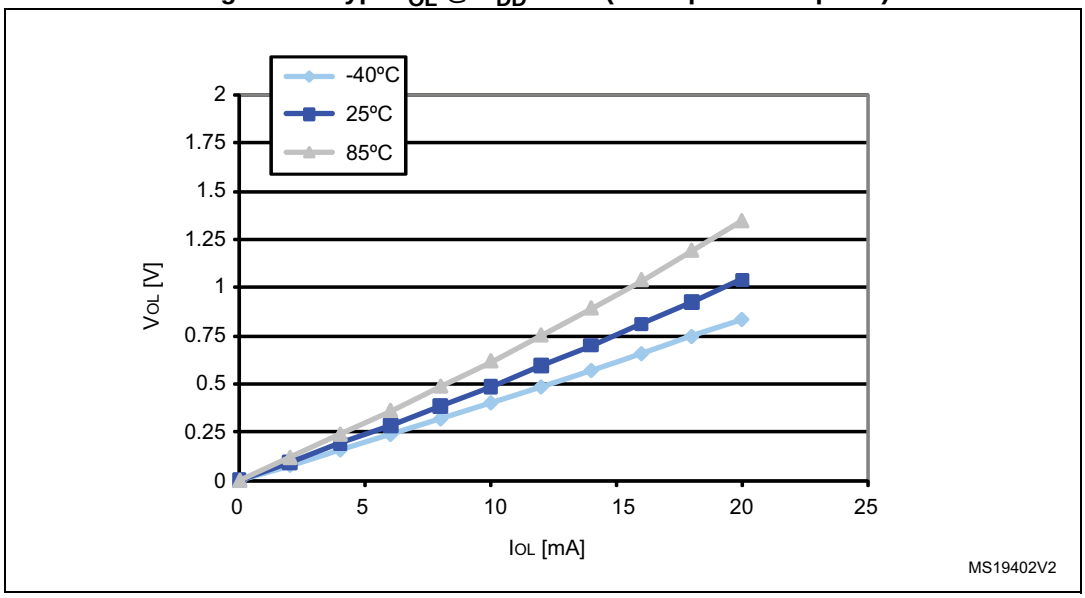


Figure 21. Typ. V_{OL} @ V_{DD} = 5 V (true open drain ports)



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Figure 22. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

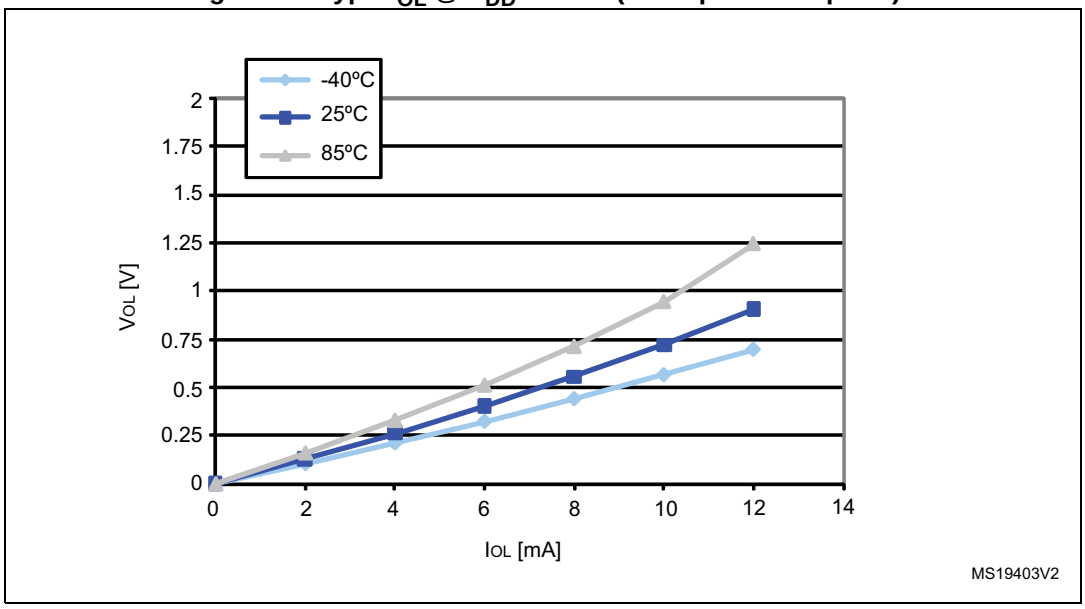
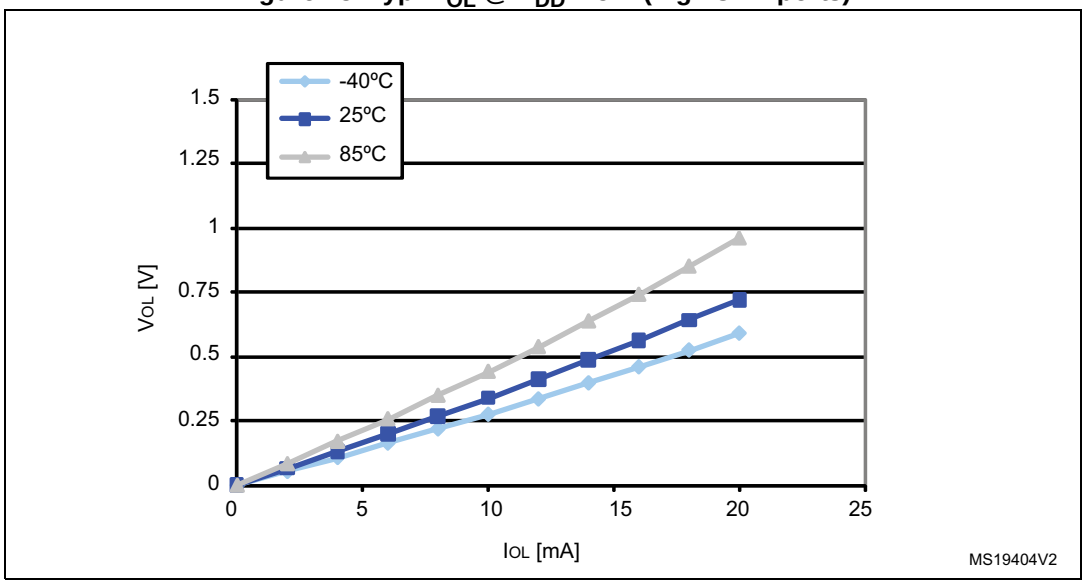


Figure 23. Typ. V_{OL} @ V_{DD} = 5 V (high sink ports)



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Figure 24. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

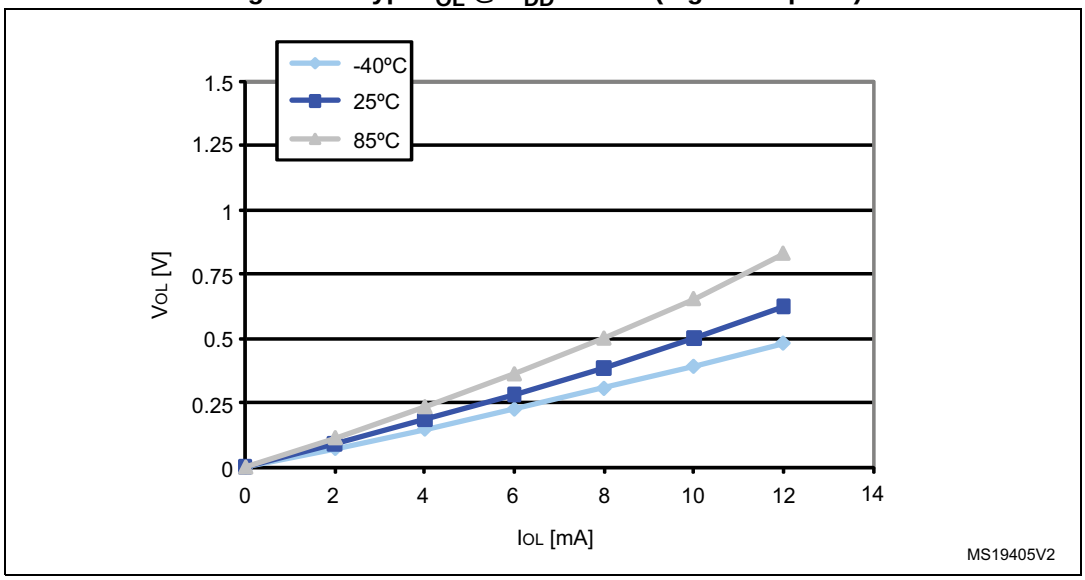
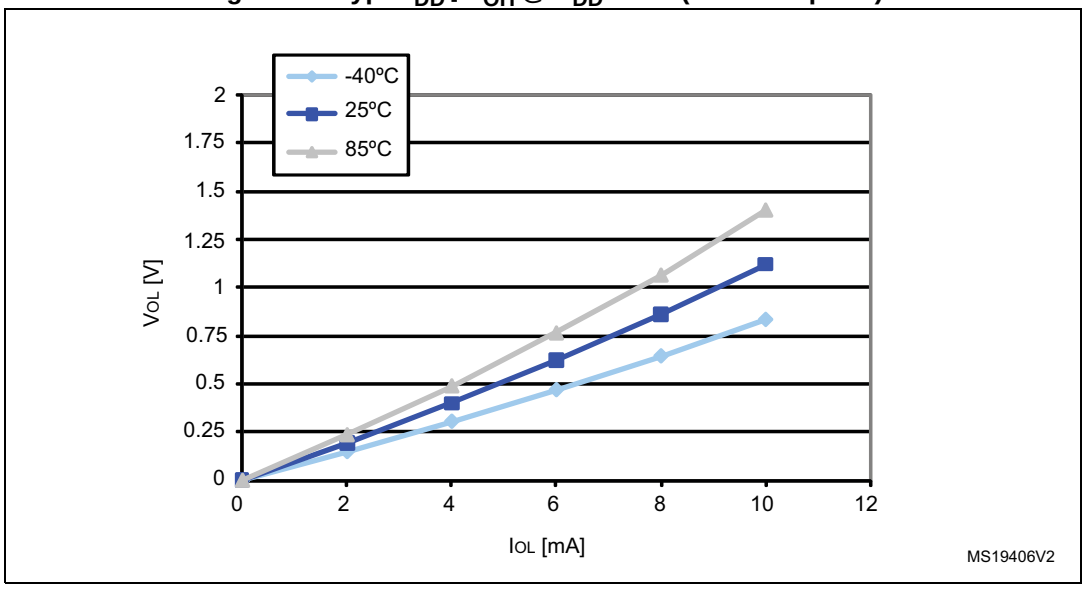


Figure 25. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (standard ports)



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Figure 26. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

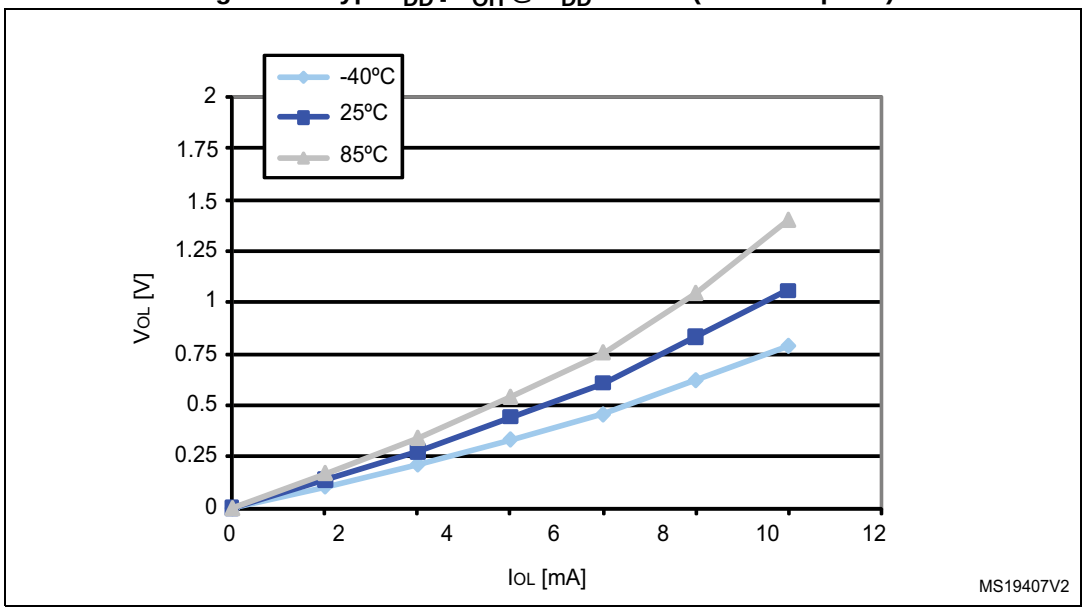
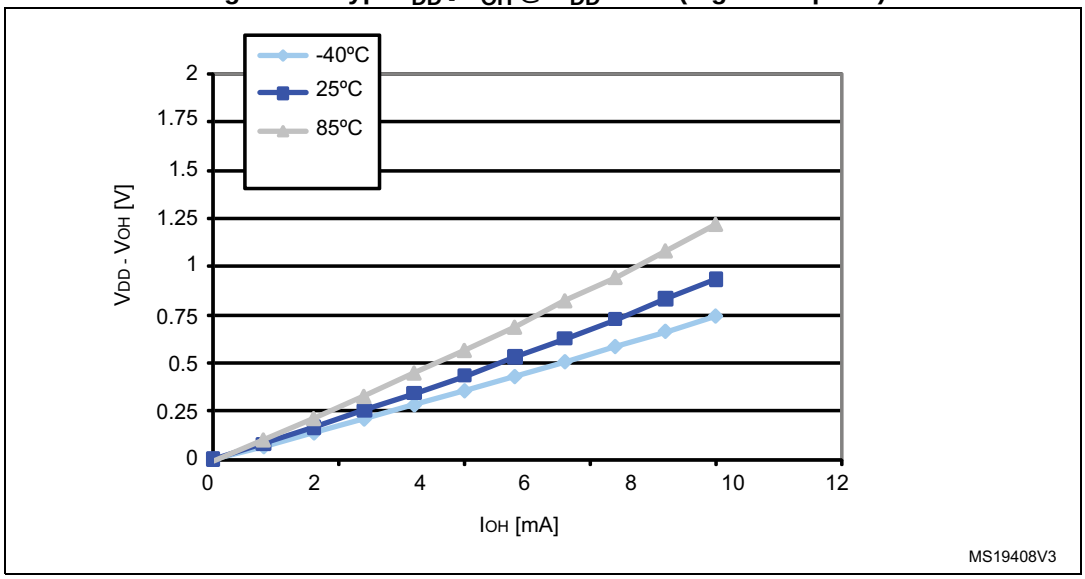
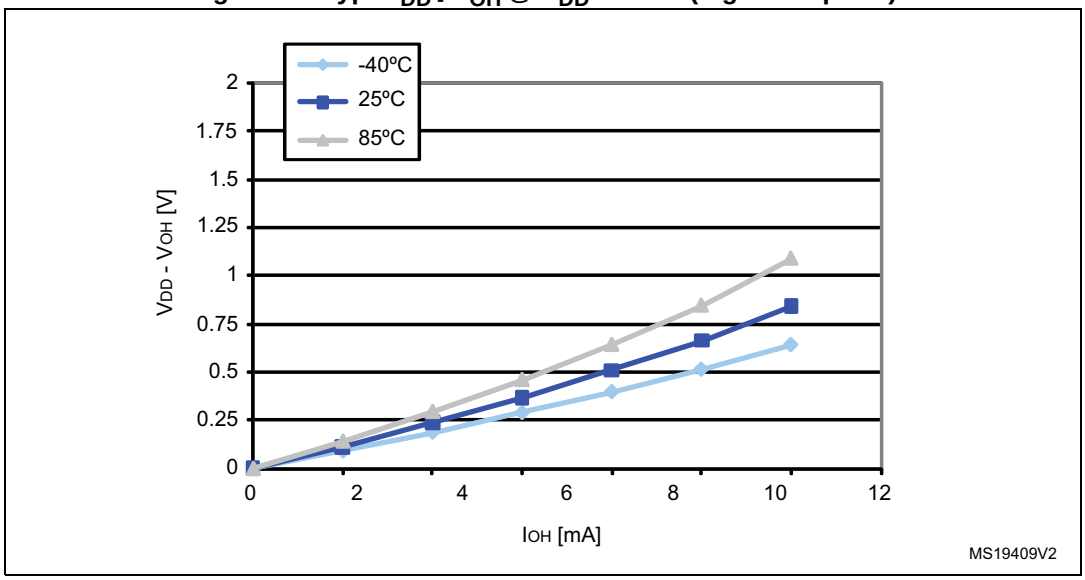


Figure 27. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (high sink ports)



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Figure 28. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)



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9.3.7 Reset pin characteristics

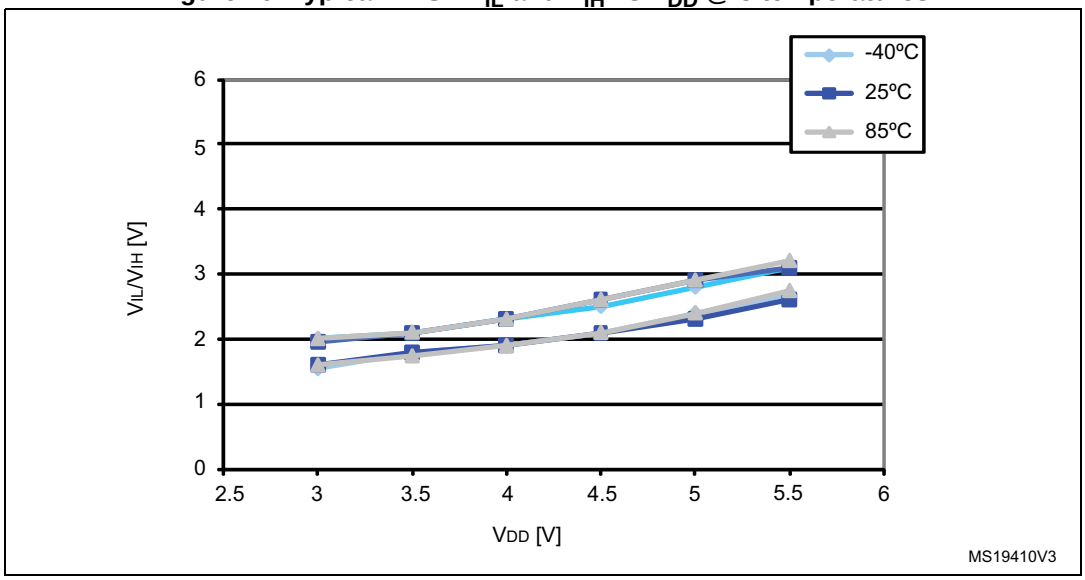
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	-0.3 V	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	0.7 x V_{DD}	-	V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL}= 2 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor (2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse (3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse (3)	-	500	-	-	ns
$t_{OP(NRST)}$	NRST output pulse (1)	-	15	-	-	µs

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor
3. Data guaranteed by design, not tested in production.

Figure 29. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 3 temperatures



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Figure 30. Typical NRST pull-up resistance vs V_{DD} @ 3 temperatures

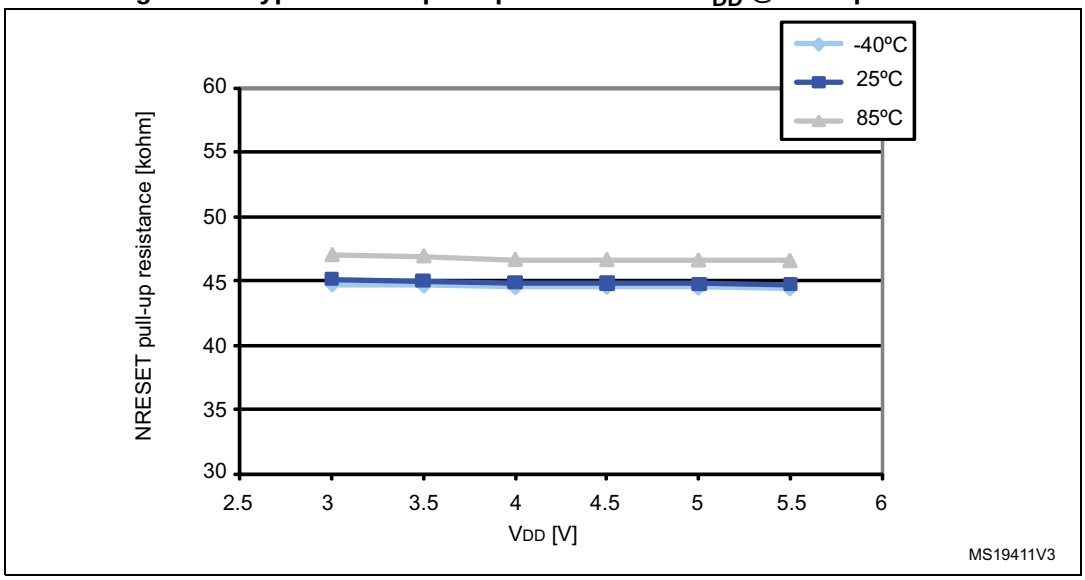
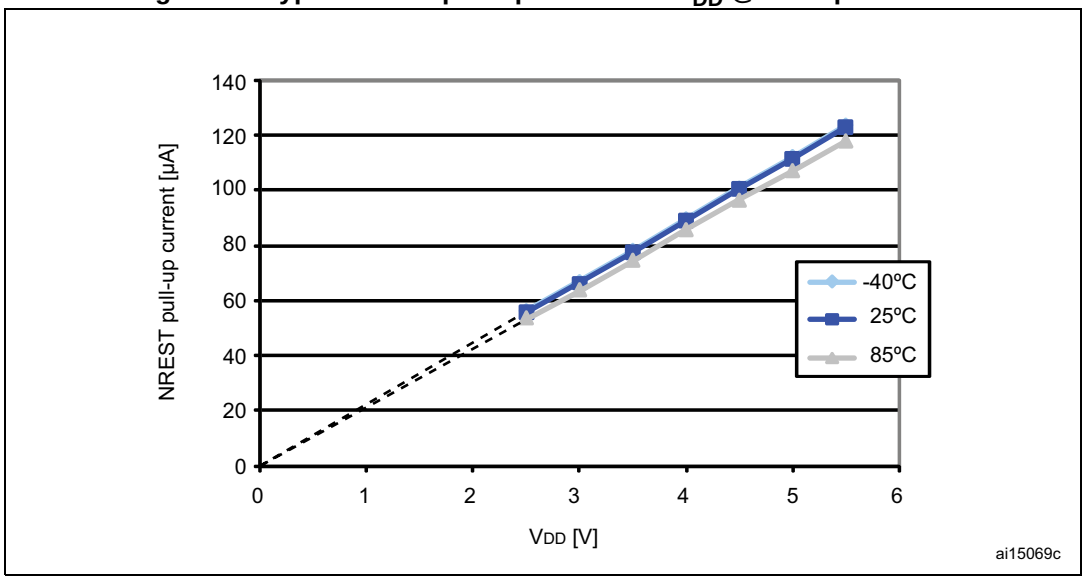


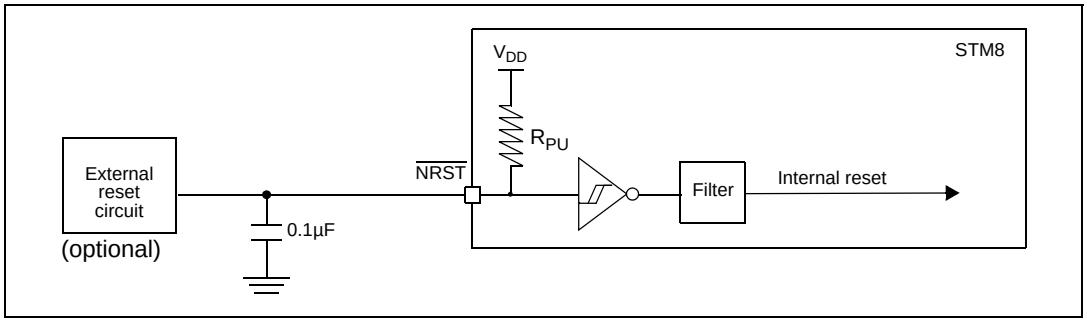
Figure 31. Typical NRST pull-up current vs V_{DD} @ 3 temperatures



The reset network shown in *Figure 32* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 35*. Otherwise the reset is not taken into account internally. For power consumption sensitive applications, the capacity of the external reset capacitor can be reduced to limit charge/discharge current. If the NRST signal is used to reset the external circuitry, care must be taken of the charge/discharge time of the external capacitor to fulfill the external device's reset timing conditions. The minimum recommended capacity is 10 nF.

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Figure 32. Recommended reset pin protection



9.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 40* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 40. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	10	MHz
		Slave mode	0	6	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	25	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4 x t_{MASTER}	-	
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	70	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode	7	-	
		Slave mode	10	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode	-	3 x t_{MASTER}	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	25	-	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	75	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	30	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	31	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	12	-	

1. Values based on design simulation and/or characterization results, and not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

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Figure 33. SPI timing diagram - slave mode and CPHA = 0

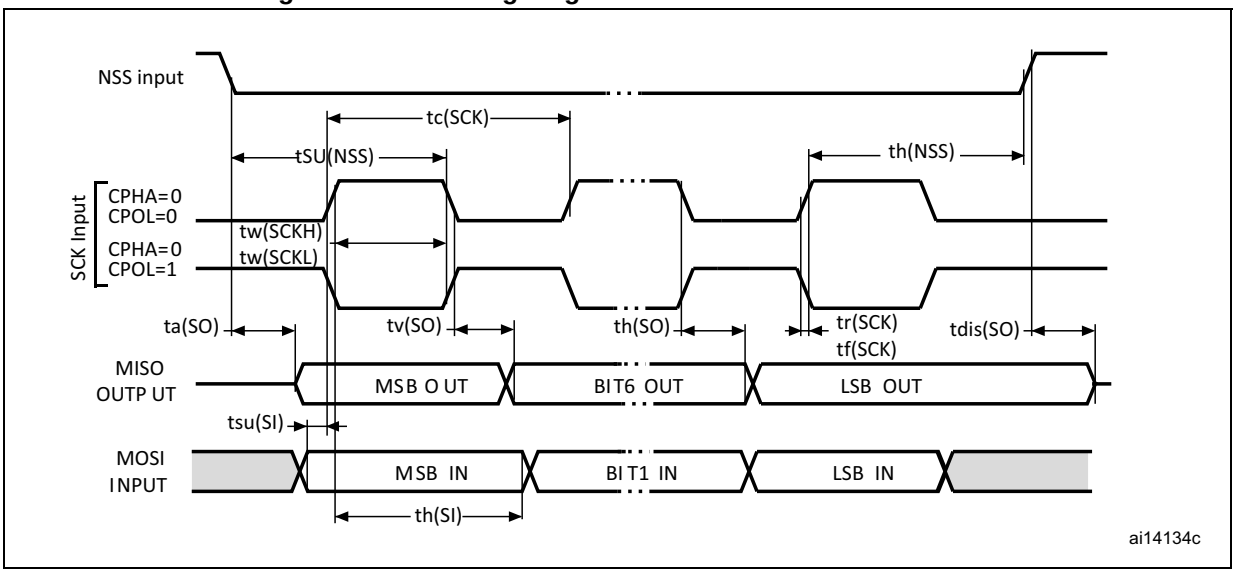
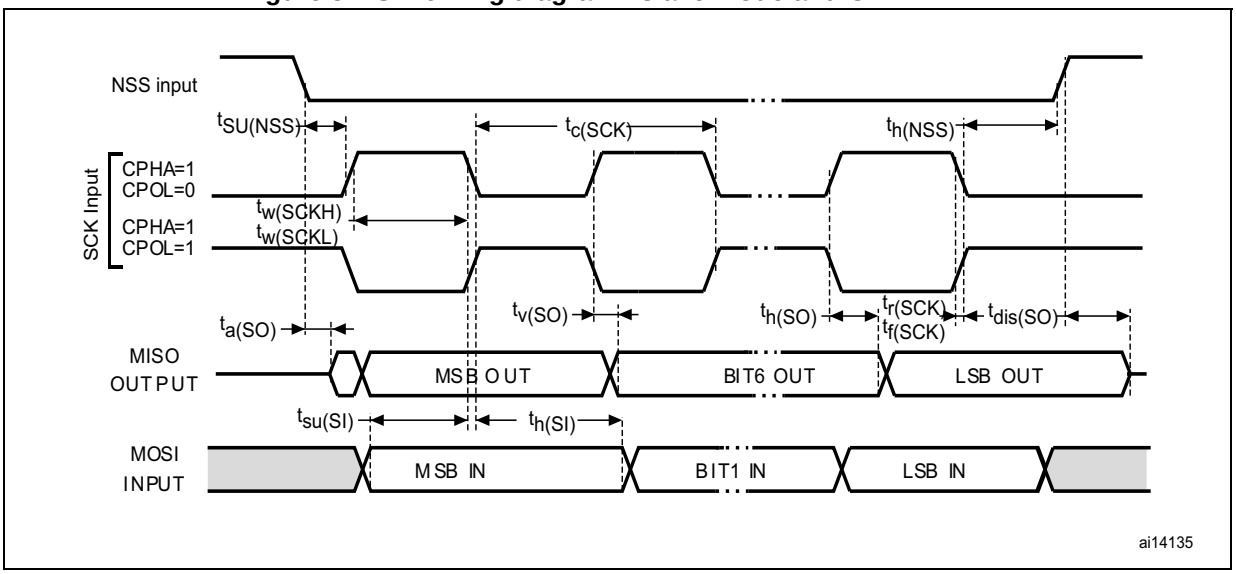


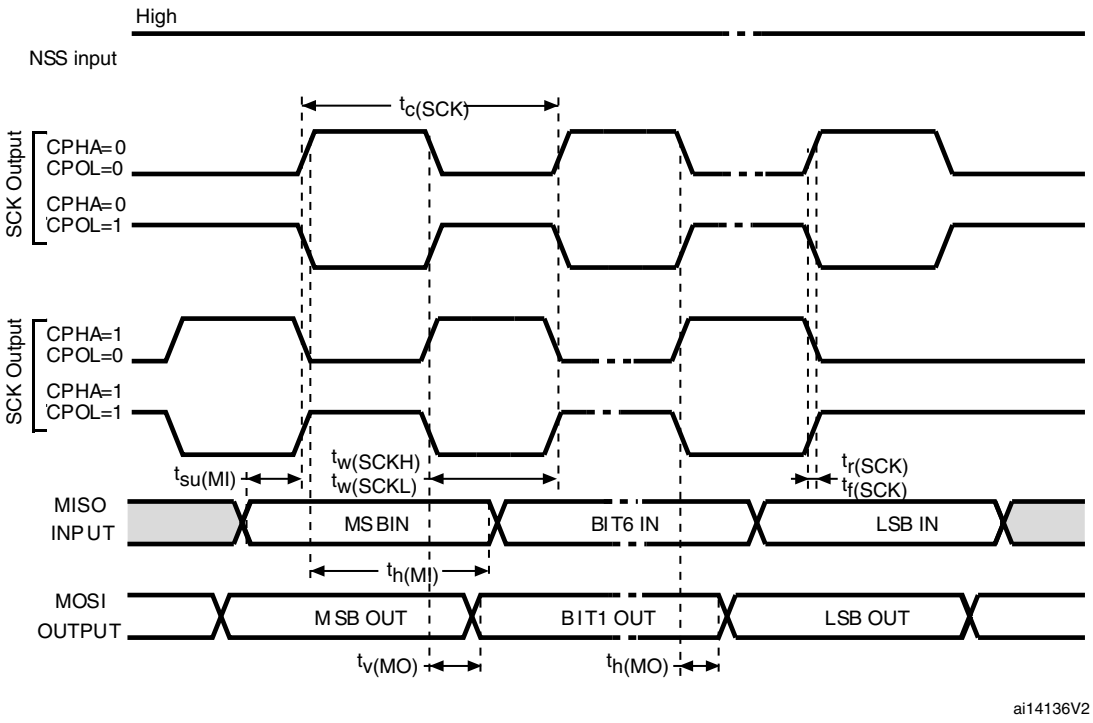
Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

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Figure 35. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

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9.3.9 I²C interface characteristics

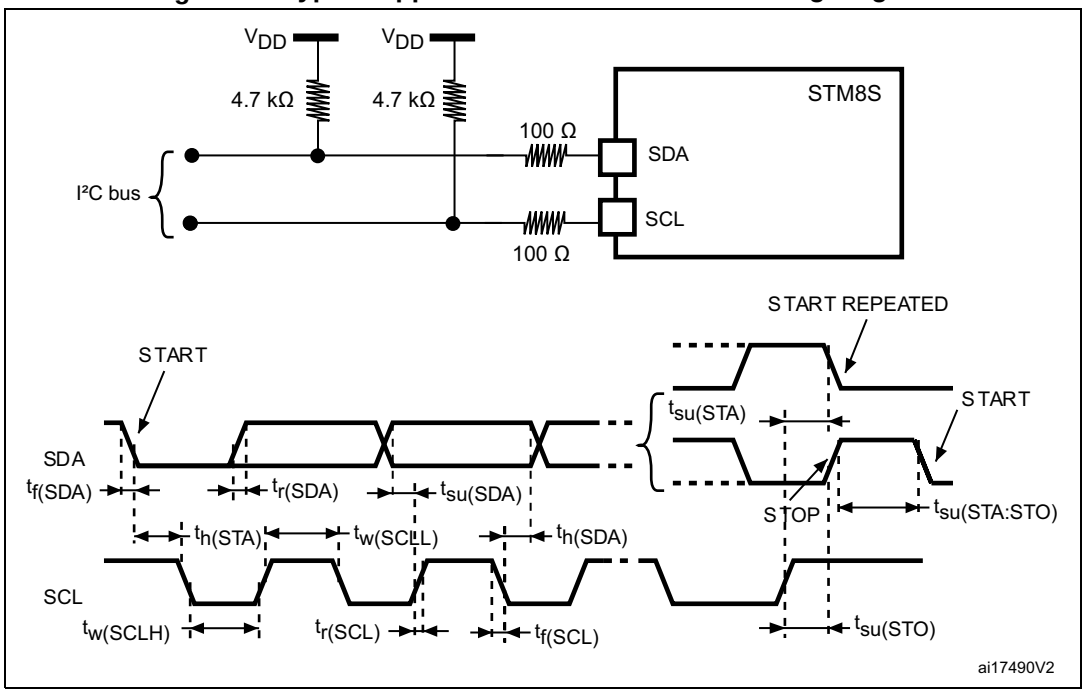
Table 41. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

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Figure 36. Typical application with I²C bus and timing diagram



1. Measurement points are made at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

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9.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 42. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DDA} = 3 to 5.5 V	1	-	4	MHz
		V_{DDA} = 4.5 to 5.5 V	1	-	6	
V_{DDA}	Analog supply	-	3	-	5.5	V
V_{REF+}	Positive reference voltage	-	2.75(1)	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	0.5(1)	V
V_{AIN}	Conversion voltage range(2)	-	V_{SSA}	-	V_{DDA}	V
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(2)	Sampling time	f_{ADC} = 4 MHz	0.75			µs
		f_{ADC} = 6 MHz	0.5			
t_{STAB}	Wakeup time from standby	-	-	7	-	µs
t_{CONV}	Total conversion time (including sampling time, 10-bit resolution)	f_{ADC} = 4 MHz	3.5			µs
		f_{ADC} = 6 MHz	2.33			µs
		-	14			$1/f_{ADC}$

1. Data guaranteed by design, not tested in production..
2. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

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Table 43. ADC accuracy with R_{AIN} < 10 kΩ , V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error (1)	f_{ADC} = 2 MHz	1.0	2.5	LSB
		f_{ADC} = 4 MHz	1.4	3	
		f_{ADC} = 6 MHz	1.6	3.5	
$\|E_O\|$	Offset error (1)	f_{ADC} = 2 MHz	0.6	2.0	
		f_{ADC} = 4 MHz	1.1	2.5	
		f_{ADC} = 6 MHz	1.2	2.5	
$\|E_G\|$	Gain error (1)	f_{ADC} = 2 MHz	0.2	2	
		f_{ADC} = 4 MHz	0.6	2.5	
		f_{ADC} = 6 MHz	0.8	2.5	
$\|E_D\|$	Differential linearity error (1)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.8	1.5	
$\|E_L\|$	Integral linearity error (1)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.6	1.5	
		f_{ADC} = 6 MHz	0.6	1.5	

1. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 9.3.6* does not affect the ADC accuracy.

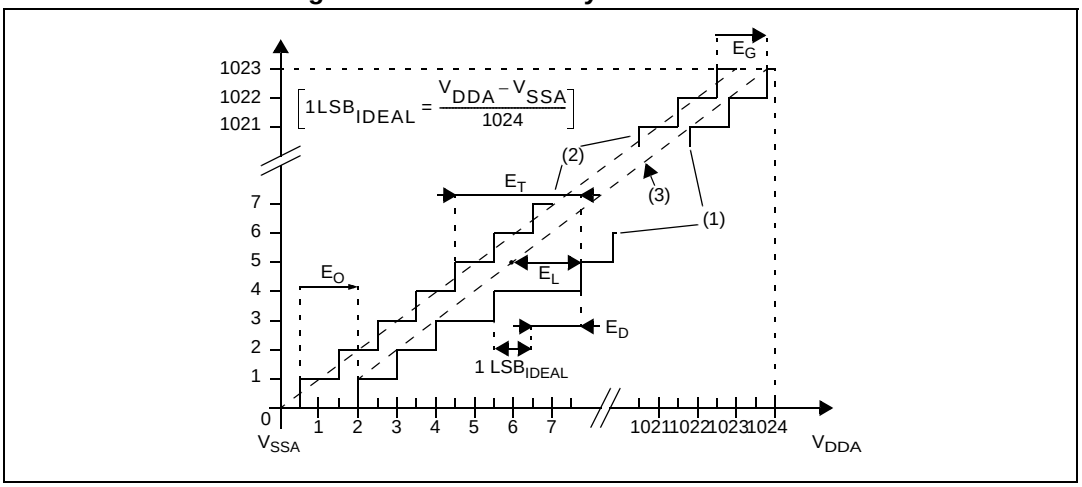
Table 44. ADC accuracy with R_{AIN} < 10 kΩ R_{AIN}, V_{DDA} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error(1)	f_{ADC} = 2 MHz	1.1	2.0	LSB
		f_{ADC} = 4 MHz	1.6	2.5	
$\|E_O\|$	Offset error(1)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	1.3	2.0	
$\|E_G\|$	Gain error(1)	f_{ADC} = 2 MHz	0.2	1.5	
		f_{ADC} = 4 MHz	0.5	2.0	
$\|E_D\|$	Differential linearity error(1)	f_{ADC} = 2 MHz	0.7	1.0	
		f_{ADC} = 4 MHz	0.7	1.0	
$\|E_L\|$	Integral linearity error(1)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.6	1.5	

1. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 9.3.6* does not affect the ADC accuracy.

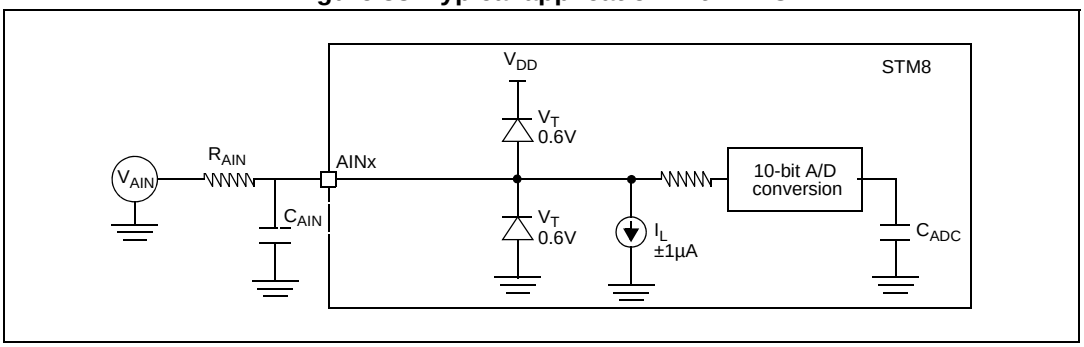
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Figure 37. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 38. Typical application with ADC



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9.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 45. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 5 V, T_A = 25 °C, f_{MASTER} = 16 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 5 V, T_A = 25 °C, f_{MASTER} = 16 MHz, conforming to IEC 61000-4-4	4A

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Electromagnetic interference (EMI)

Emission tests conform to the SAE IEC 61967-2 standard for test software, board layout and pin loading.

Table 46. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{HSE}/f_{CPU}(1)			
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	24 MHz/ 24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V T_A = 25 °C LQFP48 package conforming to SAE IEC 61967-2	0.1MHz to 30 MHz	14	13	24	dBµV
			30 MHz to 130 MHz	19	23	17	
			130 MHz to 1 GHz	-4	-4	7	
	SAE EMI level		SAE EMI level	1.5	2	2.5	

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	A	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	IV	1000	V

1. Data based on characterization results, not tested in production.

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Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) is performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 48. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	$T_A = 25$ °C	A
		$T_A = 85$ °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

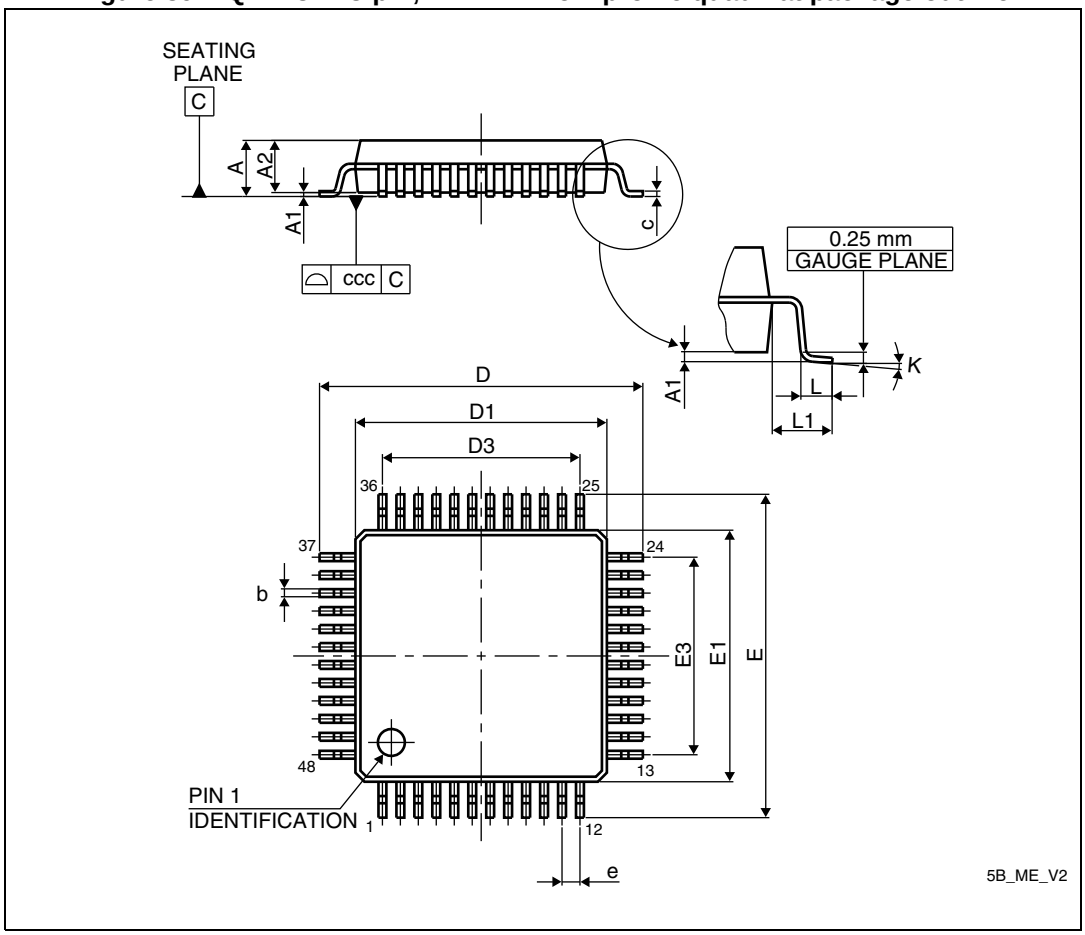
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10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*. ECOPACK® is an ST trademark.

10.1 LQFP48 package information

Figure 39. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

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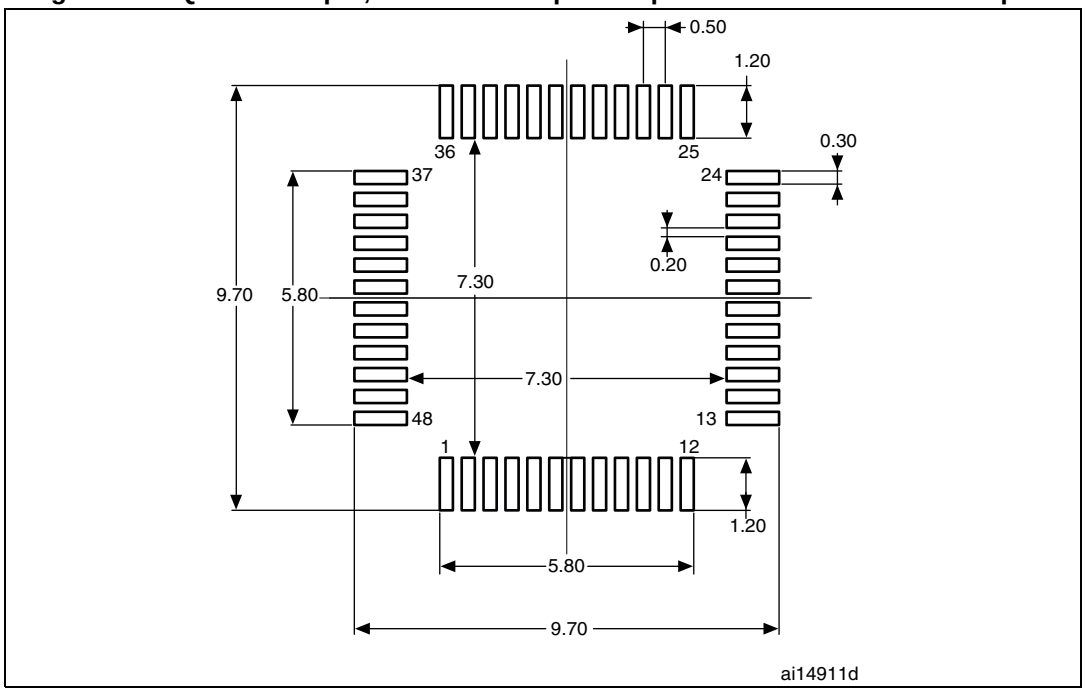
Table 49. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

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Figure 40. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

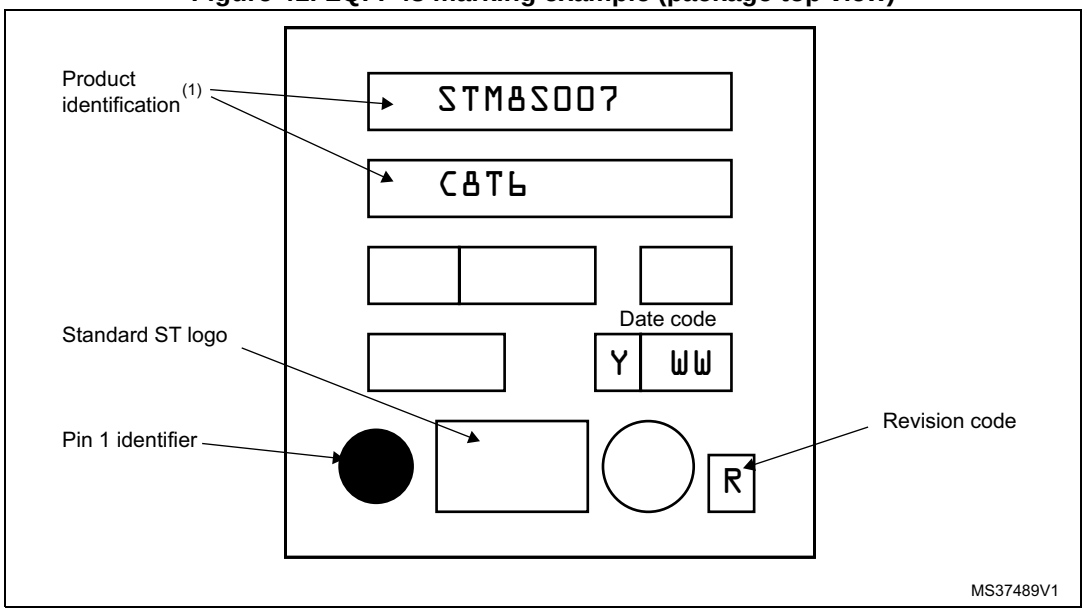


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 41. LQFP48 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

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10.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 16: General operating conditions*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins, where: $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$, and taking account of the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 50. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10.2.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

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10.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Figure 42: STM8S007C8 value line ordering information scheme(1)*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature T_{Amax}= 82 °C (measured according to JESD51-2)
- I_{DDmax} = 15 mA, V_{DD} = 5.5 V
- Maximum eight standard I/Os used at the same time in output at low level with I_{OL} = 10 mA, V_{OL}= 2 V
- Maximum four high sink I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.5 V
- Maximum two true open drain I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 2 V

  P_{INTmax} = 15 mA x 5.5 V = 82.5 mW

  P_{IOmax} = (10 mA x 2 V x 8) + (20 mA x 2 V x 2) + (20 mA x 1.5 V x 4) = 360 mW

  This gives: P_{INTmax} = 82.5 mW and P_{IOmax} 360 mW:

  P_{Dmax} = 82.5 mW + 360 mW

  Thus: P_{Dmax} = 443 mW

Using the values obtained in *Table 50: Thermal characteristics on page 86* T_{Jmax} is calculated as follows for LQFP64 10 x 10 mm = 46 °C/W:

T_{Jmax} = 82 °C + (46 °C/W x 443 mW) = 82 °C + 20 °C = 102 °C

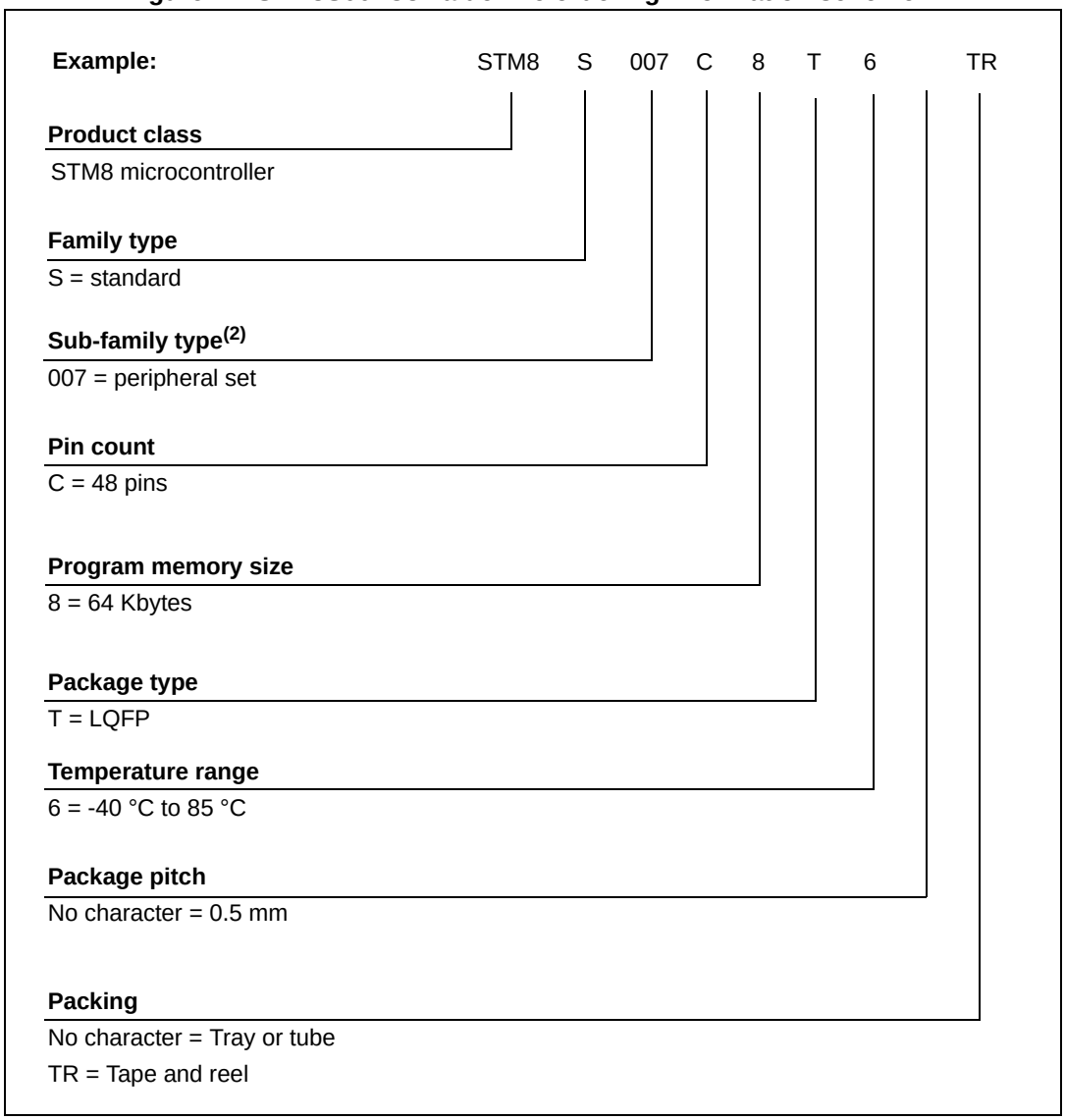
This is within the range of the suffix 6 version parts (-40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6.

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11 Part numbering

Figure 42. STM8S007C8 value line ordering information scheme(1)



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.
2. Refer to *Table 1: STM8S007C8 value line features* for detailed description.

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12 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

12.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

STice key features

- Occurrence and time profiling and code coverage (new features)
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Program and data trace recording up to 128 KB records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows users to specify the components users need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

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12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

12.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST Visual Develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify the user STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- ***Raisonance C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- ***STM8 assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows users to assemble and link the user application source code.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on user application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the user STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

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13 Revision history

Table 51. Document revision history

Date	Revision	Changes
31-Oct-2011	1	Initial release.
06-Jan-2012	2	*Table 34: Flash program memory/data EEPROM memory*: updated V_{DD} condition; updated t_{RET} parameters. *Table 39: NRST pin characteristics*: updated typ and max values of the NRST Pull-up resistor.
26-Apr-2012	3	Added the document status on the cover page (datasheet-production data). Modified temperature range and ACC_{HSI} values in *Table 31: HSI oscillator characteristics on page 58* (ACC_{HSI} parameter). Modified *Figure 35: SPI timing diagram - master mode(1) on page 74* (SCK output instead of SCK input).
10-Mar-2015	4	Updated the disclaimer. Added *Figure 41: LQFP48 marking example (package top view)*.
25-Mar-2015	5	Updated: – *Figure 27: Typ. VDD - VOH @ VDD = 5 V (high sink ports)*, – *Figure 29: Typical NRST VIL and VIH vs VDD @ 3 temperatures*, – *Figure 30: Typical NRST pull-up resistance vs VDD @ 3 temperatures*. Added a note to Power-on reset threshold parameter in *Table 17: Operating conditions at power-up/power-down*.

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