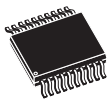
STM8L051F3

Value Line, 8-bit ultralow power MCU, 8-KB Flash, 256-byte data EEPROM, RTC, timers, USART, I2C, SPI, ADC

Datasheet – production data

Features

- Operating conditions
  - Operating power supply: 1.8 V to 3.6 V
    Temperature range: –40 °C to 85 °C
- Low power features
  - 5 low power modes: Wait, Low power run (5.1 µA), Low power wait (3 µA), Active-halt with RTC (1.3 µA), Halt (350 nA)
  - Ultra-low leakage per I/0: 50 nA
  - Fast wakeup from Halt: 5 µs
- Advanced STM8 core
  - Harvard architecture and 3-stage pipeline
  - Max freq: 16 MHz, 16 CISC MIPS peak
  - Up to 40 external interrupt sources
- Reset and supply management
  - Low power, ultra-safe BOR reset with 5 selectable thresholds
  - Ultra low power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 32 kHz and 1 to 16 MHz crystal oscillators
  - Internal 16 MHz factory-trimmed RC
  - Internal 38 kHz low consumption RC
  - Clock security system
- Low power RTC
  - BCD calendar with alarm interrupt
  - Digital calibration with +/- 0.5 ppm accuracy
  - LSE security system
  - Auto-wakeup from Halt w/ periodic interrupt
- Memories
  - 8 Kbytes of Flash program memory and 256 bytes of data EEPROM with ECC
  - Flexible write and read protection modes
  - 1 Kbyte of RAM



TSSOP20

- DMA
  - 4 channels supporting ADC, SPI, I2C, USART, timers
  - 1 channel for memory-to-memory
- 12-bit ADC up to 1 Msps/28 channels
  - Internal reference voltage
- Timers
  - Two 16-bit timers with 2 channels (used as IC, OC, PWM), quadrature encoder
  - One 8-bit timer with 7-bit prescaler
  - 2 watchdogs: 1 Window, 1 Independent
  - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
  - Synchronous serial interface (SPI)
  - Fast I^2C 400 kHz SMBus and PMBus
  - USART
- Up to 18 I/Os, all mappable on interrupt vectors
- Development support
  - Fast on-chip programming and non-intrusive debugging with SWIM
  - Bootloader using USART

This is information on a product in full production.

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1 Introduction

This document describes the features, pinout, mechanical data and ordering information for the low density value line STM8L051F3 microcontroller with 8-Kbyte Flash memory density.

For further details on the whole STMicroelectronics low density family please refer to *Section 2.2: Ultra low power continuum*.

For detailed information on device operation and registers, refer to the reference manual (RM0031).

For information on to the Flash program memory and data EEPROM, refer to the programming manual (PM0054).

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

Low density value line devices provide the following benefits:

- Integrated system
  - 8 Kbytes of low-density embedded Flash program memory
  - 256 bytes of data EEPROM
  - 1 Kbyte of RAM
  - Internal high-speed and low-power low speed RC
  - Embedded reset
- Ultra low power consumption
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals
  - Wide choice of development tools

These features make the value line STM8L05xxx ultra low power microcontroller family suitable for a wide range of consumer and mass market applications.

Refer to *Table 1: Low density value line STM8L05xxx low power device features and peripheral counts* and *Section 3: Functional overview* for an overview of the complete range of peripherals proposed in this family.

Figure 1 shows the block diagram of the low density value line STM8L05xxx family.

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2 Description

The low density value line STM8L05xxx devices are members of the STM8L ultra low power 8-bit family.

The value line STM8L05xxx ultra low power family features an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-Application debugging and ultra-fast Flash programming.

Low density value line STM8L05xxx microcontrollers feature embedded data EEPROM and low power, low-voltage, single-supply program Flash memory.

The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, a real-time clock, two 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as an SPI, an I^2C interface, and one USART.

The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

All value line STM8L ultra low power products are based on the same architecture with the same memory mapping and a coherent pinout.

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2.1 Device overview

Table 1. Low density value line STM8L05xxx low power device features and peripheral counts

Features		STM8L051F3
Flash (Kbytes)		8
Data EEPROM (Bytes)		256
RAM (Kbytes)		1
Timers	Basic	1 (8-bit)
	General purpose	2 (16-bit)
Communication interfaces	SPI	1
	I2C	1
	USART	1
GPIOs		18 (1)
12-bit synchronized ADC (number of channels)		1 (10)
Others		RTC, window watchdog, independent watchdog, 16-MHz and 32-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator
CPU frequency		16 MHz
Operating voltage		1.8 to 3.6 V
Operating temperature		– 40 to +85 °C
Package		TSSOP20

1. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

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2.2 Ultra low power continuum

The ultra low power value line STM8L05xxx and STM8L15xxx are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the STM8L family, the devices are part of STMicroelectronics microcontrollers ultra low power strategy which also includes STM8L101xx and STM32L15xxx. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 µm ultra-low leakage process.

Note: 1 The STM8L05xxx are pin-to-pin compatible with STM8L101xx devices.

2 The STM32L family is pin-to-pin compatible with the general purpose STM32F family. Please refer to STM32L15x documentation for more information on these devices.

Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex™-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra low power performance to range from 5 up to 33.3 DMIPs.

Shared peripherals

STM8L05xx, STM8L15xx and STM32L15xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripheral: ADC1
- Digital peripherals: RTC and some communication interfaces

Common system strategy

To offer flexibility and optimize performance, the STM8L and STM32L devices use a common architecture:

- Same power supply range from 1.8 to 3.6 V
- Architecture optimized to reach ultra low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy for both STM8L and STM32L including power-on reset, power-down reset, brownout reset and programmable voltage detector.

Features

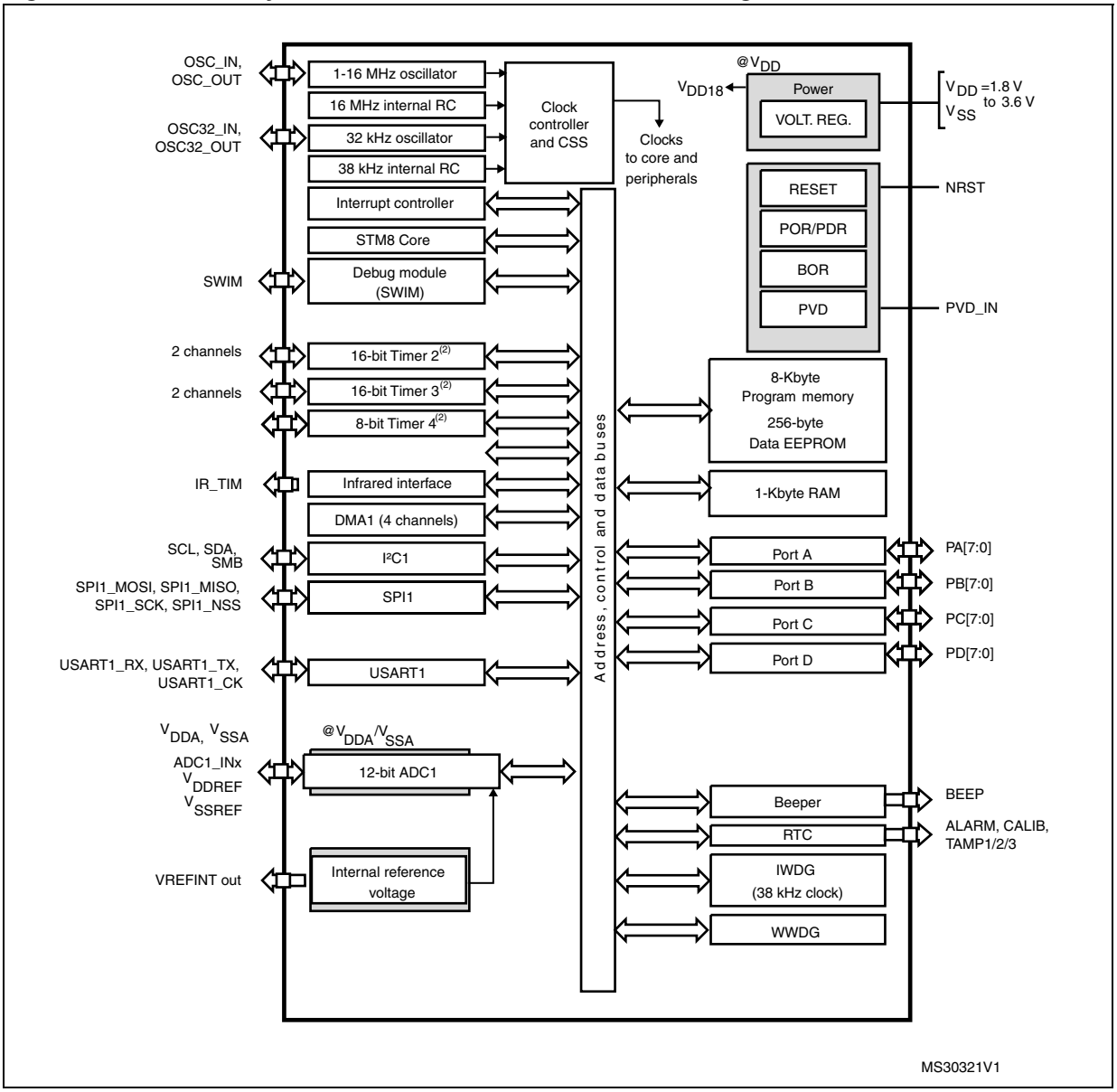
ST ultra low power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbytes

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3 Functional overview

Figure 1. Low density value line STM8L05xxx device block diagram



1. **Legend**:
ADC: Analog-to-digital converter
BOR: Brownout reset
DMA: Direct memory access
I²C: Inter-integrated circuit multimaster interface
IWDG: Independent watchdog
POR/PDR: Power-on reset / power-down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

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3.1 Low power modes

The low density value line STM8L05xxx devices support five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode).
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash memory and data EEPROM are stopped and the voltage regulator is configured in ultra low power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1) and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs.

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3.2 Central processing unit STM8

3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64-Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The low density value line STM8L05xxx features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 17 external interrupt sources on 11 vectors
- Trap and reset interrupts

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3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.8 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1}; V_{DD1} = 1.8 to 3.6 V: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD1} pins, the corresponding ground pin is V_{SS1}.
- V_{SSA}; V_{DDA} = 1.8 to 3.6 V: external power supplies for analog peripherals. V_{DDA} and V_{SSA} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{SS2}; V_{DD2} = 1.8 to 3.6 V: external power supplies for I/Os. V_{DD2} and V_{SS2} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{REF+}, V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. When the microcontroller operates between 1.8 and 3.6 V, BOR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains in reset state when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The low density value line STM8L05xxx embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

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3.4 Clock management

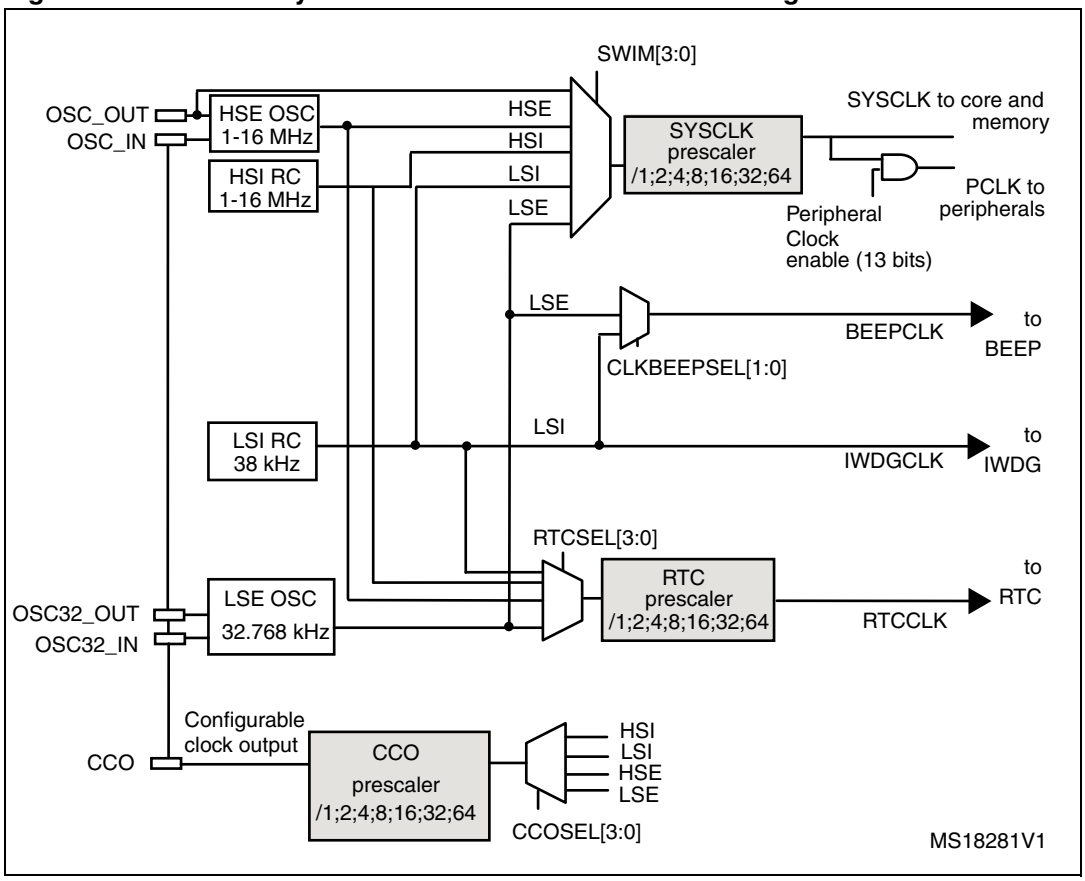
The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** four different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC clock sources:** the above four sources can be chosen to clock the RTC whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, it is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

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Figure 2. Low density value line STM8L05xxx clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to Section HSE clock in the STM8L15x and STM8L16x reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to Section LSE clock in the STM8L15x and STM8L16x reference manual (RM0031).

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3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from every second to every year

3.6 Memories

The low density value line STM8L05xxx devices have the following main features:

- Up to 1 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
  - 8 Kbytes of low-density embedded Flash program memory
  - 256 bytes of Data EEPROM
  - Option bytes

The EEPROM embeds the error correction code (ECC) feature.

The option byte protects part of the Flash program memory from write and readout piracy.

3.7 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, I2C1, SPI1, USART1, and the three timers.

3.8 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 10 channels (including 1 fast channel) and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

Note: ADC1 can be served by DMA1.

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3.9 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface controls the routing of internal analog signals to ADC1 and the internal reference voltage V_{REFINT}.

3.10 Timers

Low density value line STM8L05xxx devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 2 compares the features of the advanced control, general-purpose and basic timers.

Table 2. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	up/down	Any power of 2 from 1 to 128	Yes	2	None
TIM3						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

3.10.1 16-bit general purpose timers (TIM2, TIM3)

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.10.2 8-bit basic timer (TIM4)

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.11 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

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3.11.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.11.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.12 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.13 Communication interfaces

3.13.1 SPI

The serial peripheral interfaces (SPI1) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 can be served by the DMA1 Controller.

3.13.2 I^2C

The I^2C bus interface (I2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

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3.13.3 USART

The USART interface (USART1) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1 can be served by the DMA1 Controller.

3.14 Infrared (IR) interface

The low density STM8L05xxx devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.15 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

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Bootloader

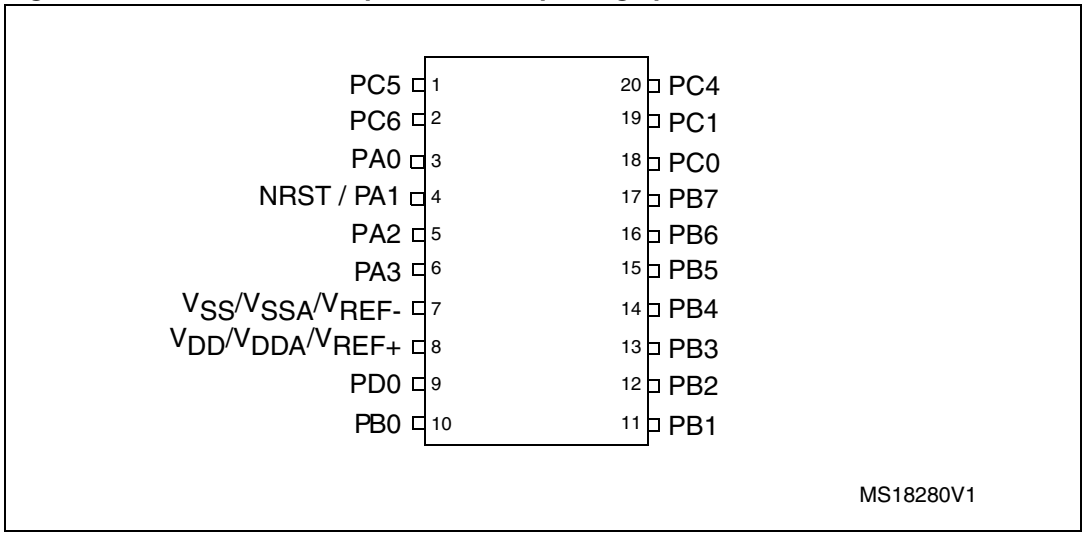
The low density value line STM8L05xxx ultra low power devices feature a built-in bootloader (see *UM0560: STM8 bootloader user manual*).

The bootloader is used to download application software into the device memories, including RAM, program and data memory, using standard serial interfaces. It is a complementary solution to programming via the SWIM debugging interface.

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4 Pin description

Figure 3. STM8L051F3 20-pin TSSOP20 package pinout



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Table 3. Legend/abbreviation for *Table 4*

Type	I= input, O = output, S = power supply	
Level	Output	HS = high sink/source (20 mA)
	Input	FT - five volt tolerant
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 4. Low density value line STM8L05xxx pin description

pin n°				Input			Output				
TSSOP20	Pin name	Type	I/O level	floating	wpu	Ext. interrupt	High sink/source	OD	PP	Main function (after reset)	Default alternate function
4	NRST/PA1(1)	I/O			X		HS		X	**Reset**	PA1
5	PA2/OSC_IN/*[USART_TX]*(2)/ *[SPI_MISO]*(2)	I/O		X	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART transmit] / [SPI master in- slave out]*
6	PA3/OSC_OUT/*[USART_RX]*(2)/ *[SPI_MOSI]*(2)	I/O		X	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART receive]/ [SPI master out/slave in]/*
10	PB0(3)/TIM2_CH1/ADC1_IN18	I/O		X	X	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / ADC1_IN18
11	PB1/TIM3_CH1/ADC1_IN17	I/O		X	X	X	HS	X	X	**Port B1**	Timer 3 - channel 1 / ADC1_IN17
12	PB2/ TIM2_CH2/ ADC1_IN16	I/O		X	X	X	HS	X	X	**Port B2**	Timer 2 - channel 2 ADC1_IN16
13	PB3/TIM2_ETR/ ADC1_IN15/RTC_ALARM	I/O		X	X	X	HS	X	X	**Port B3**	Timer 2 - external trigger / ADC1_IN15 / RTC_ALARM
14	PB4(3)/SPI1_NSS/ADC1_IN14	I/O		X	X	X	HS	X	X	**Port B4**	SPI master/slave select / ADC1_IN14
15	PB5/SPI_SCK/ /ADC1_IN13	I/O		X	X	X	HS	X	X	**Port B5**	[SPI clock] / ADC1_IN13
16	PB6/SPI1_MOSI/ ADC1_IN12	I/O		X	X	X	HS	X	X	**Port B6**	SPI master out/ slave in / ADC1_IN12
17	PB7/SPI1_MISO/ADC1_IN11	I/O		X	X	X	HS	X	X	**Port B7**	SPI1 master in- slave out/ ADC1_IN11
18	PC0/I2C_SDA	I/O	FT	X		X		T(4)		**Port C0**	I2C data
19	PC1/I2C_SCL	I/O	FT	X		X		T(3)		**Port C1**	I2C clock
20	PC4/USART_CK]/ I2C_SMB/CCO/ADC1_IN4	I/O		X	X	X	HS	X	X	**Port C4**	USART synchronous clock / I2C1_SMB / Configurable clock output / ADC1_IN4

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Table 4. Low density value line STM8L05xxx pin description (continued)

pin n°	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
TSSOP20				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
1	PC5/OSC32_IN /*[SPI1_NSS](2)*/ */[USART_TX](2)*/TIM2_CH1	I/O		**X**	X	X	HS	X	X	**Port C5**	LSE oscillator input / *[SPI master/slave select] / [USART transmit]/Timer 2 -channel 1*
2	PC6/OSC32_OUT/*[SPI_SCK](2) /[USART_RX](2)*/TIM2_CH2	I/O		**X**	X	X	HS	X	X	**Port C6**	LSE oscillator output */ [SPI clock] / [USART receive]/ Timer 2 -channel 2*
9	PD0/TIM3_CH2/*[ADC1_TRIG](2)*/ADC1_IN22	I/O		**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / ADC1_IN22
8	V_{DD} / V_{DDA} / V_{REF+}	S								Digital supply voltage / ADC1 positive voltage reference	
7	V_{SS} / V_{REF-} / V_{SSA}									Ground voltage / ADC1 negative voltage reference / Analog ground voltage	
3	PA0(5)/*[USART_CK](2)*/ SWIM/BEEP/IR_TIM (6)	I/O		X	**X**	X	HS (6)	X	X	**Port A0**	*[USART1 synchronous clock](2)* / SWIM input and output / Beep output / Infrared Timer output

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15xxx and STM8L16xxx reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented).
5. The PA0 pin is in input pull-up during the reset phase and after reset release.
6. High Sink LED driver capability available on PA0.

Note: The slope control of all GPIO pins, except true open drain pins, can be programmed. By default, the slope control is limited to 2 MHz.

4.1 System configuration options

As shown in *Table 4: Low density value line STM8L05xxx pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in the STM8L15xx and STM8L16xx reference manual (RM0031).

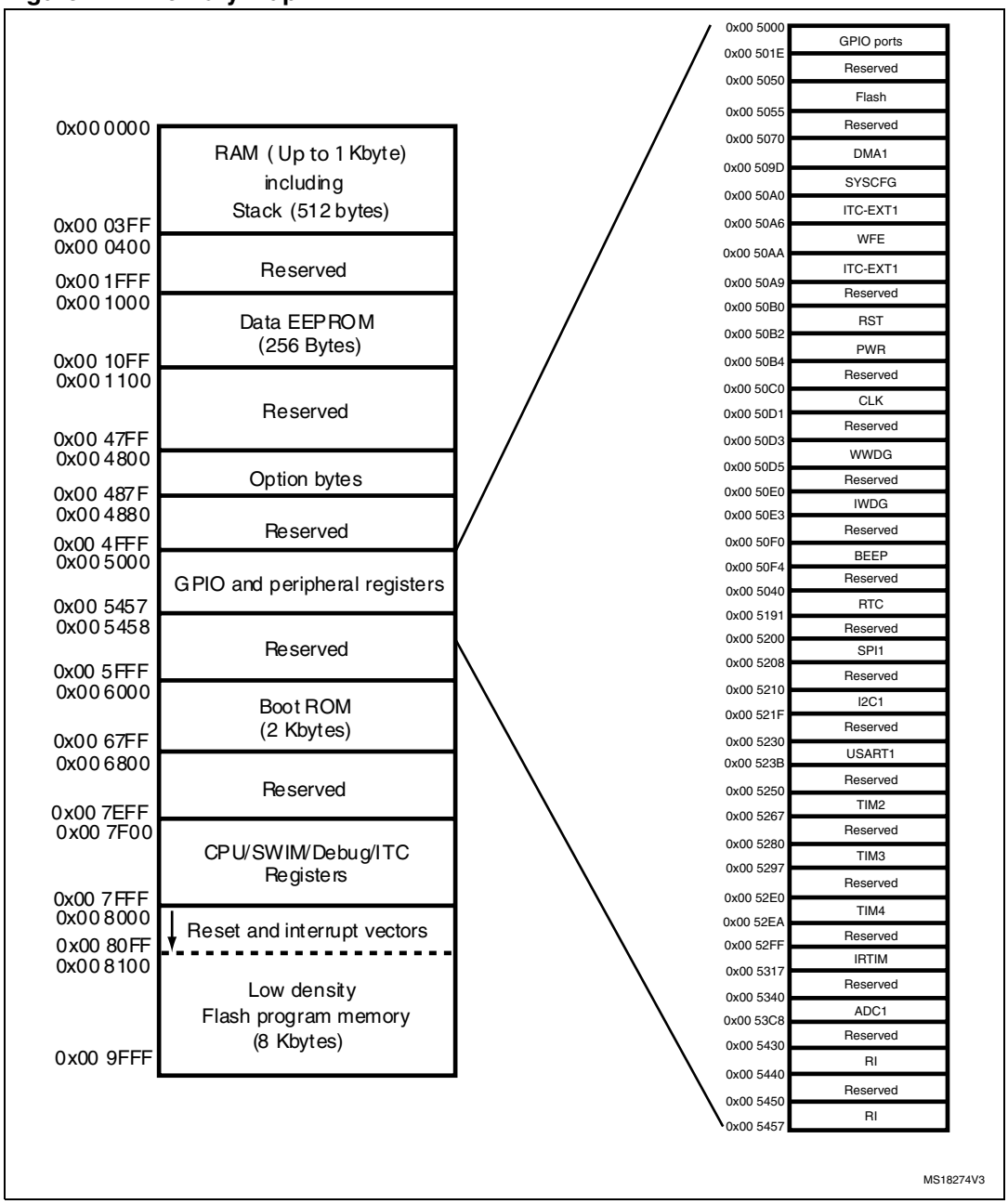
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5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 4*.

Figure 4. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

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Table 5. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	1 Kbyte	0x00 0000	0x00 03FF
Flash program memory	8 Kbytes	0x00 8000	0x00 9FFF

5.2 Register map

Table 6. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x01
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014 to 0x00 501D	Reserved area (0 bytes)			

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Table 7. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 502E to 0x00 5049	Reserved area (44 bytes)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5055 to 0x00 506F	Reserved area (27 bytes)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 bytes)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00

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Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 507D to 0x00 507E	DMA1	Reserved area (2 bytes)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00
0x00 5084		Reserved area (1 byte)		
0x00 5085		DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088		Reserved area (2 bytes)		
0x00 5089		DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092		Reserved area (2 bytes)		
0x00 5093		DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00

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Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5098	DMA1	DMA_C3M0EAR	DMA channel 3 memory 0 extended address register	0x00
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509C		Reserved area (3 bytes)		
0x00 509D	SYSCFG	SYSCFG_RMPCR3	Remapping register 3	0x00
0x00 509E		SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9		WFE_CR4	WFE control register 4	0x00
0x00 50AA	ITC - EXTI	EXTI_CR4	External interrupt control register 4	0x00
0x00 50AB		EXTI_CONF2	External interrupt port select register 2	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_CKDIVR	CLK Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	CLK Clock RTC register	0x00(1)
0x00 50C2		CLK_ICKCR	CLK Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	CLK Peripheral clock gating register 1	0x00

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Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C4	CLK	CLK_PCKENR2	CLK Peripheral clock gating register 2	0x00
0x00 50C5		CLK_CCOR	CLK Configurable clock control register	0x00
0x00 50C6		CLK_ECKCR	CLK External clock control register	0x00
0x00 50C7		CLK_SCSR	CLK System clock status register	0x01
0x00 50C8		CLK_SWR	CLK System clock switch register	0x01
0x00 50C9		CLK_SWCR	CLK Clock switch control register	0xX0
0x00 50CA		CLK_CSSR	CLK Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	CLK Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	CLK HSI calibration register	0xXX
0x00 50CD		CLK_HSITRIMR	CLK HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	CLK HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	CLK Main regulator control status register	0bxx11 1 00X
0x00 50D0		CLK_PCKENR3	CLK Peripheral clock gating register 3	0x00
0x00 50D1 to 0x00 50D2	Reserved area (2 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0x01
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 bytes)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to0x00 513F	Reserved area (76 bytes)			
0x00 5140	RTC	RTC_TR1	RTC Time register 1	0x00
0x00 5141		RTC_TR2	RTC Time register 2	0x00
0x00 5142		RTC_TR3	RTC Time register 3	0x00

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Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5143	RTC	Reserved area (1 byte)		
0x00 5144		RTC_DR1	RTC Date register 1	0x01
0x00 5145		RTC_DR2	RTC Date register 2	0x21
0x00 5146		RTC_DR3	RTC Date register 3	0x00
0x00 5147		Reserved area (1 byte)		
0x00 5148		RTC_CR1	RTC Control register 1	0x00(1)
0x00 5149		RTC_CR2	RTC Control register 2	0x00(1)
0x00 514A		RTC_CR3	RTC Control register 3	0x00(1)
0x00 514B		Reserved area (1 byte)		
0x00 514C		RTC_ISR1	RTC Initialization and status register 1	0x01
0x00 514D		RTC_ISR2	RTC Initialization and Status register 2	0x00
0x00 514E 0x00 514F		Reserved area (2 bytes)		
0x00 5150		RTC_SPRERH	RTC Synchronous prescaler register high	0x00(1)
0x00 5151		RTC_SPRERL	RTC Synchronous prescaler register low	0xFF(1)
0x00 5152		RTC_APRER	RTC Asynchronous prescaler register	0x7F(1)
0x00 5153		Reserved area (1 byte)		
0x00 5154		RTC_WUTRH	RTC Wakeup timer register high	0xFF(1)
0x00 5155		RTC_WUTRL	RTC Wakeup timer register low	0xFF(1)
0x00 5156		Reserved area (1 byte)		
0x00 5157		RTC_SSRL	RTC Subsecond register low	0x00
0x00 5158		RTC_SSRH	RTC Subsecond register high	0x00
0x00 5159		RTC_WPR	RTC Write protection register	0x00
0x00 5158		RTC_SSRH	RTC Subsecond register high	0x00
0x00 5159		RTC_WPR	RTC Write protection register	0x00
0x00 515A		RTC_SHIFTRH	RTC Shift register high	0x00
0x00 515B		RTC_SHIFTRL	RTC Shift register low	0x00
0x00 515C		RTC_ALRMAR1	RTC Alarm A register 1	0x00(1)
0x00 515D		RTC_ALRMAR2	RTC Alarm A register 2	0x00(1)
0x00 515E		RTC_ALRMAR3	RTC Alarm A register 3	0x00(1)
0x00 515F		RTC_ALRMAR4	RTC Alarm A register 4	0x00(1)
0x00 5160 to 0x00 5163		Reserved area (4 bytes)		
0x00 5164		RTC_ALRMASSRH	RTC Alarm A subsecond register high	0x00(1)
0x00 5165		RTC_ALRMASSRL	RTC Alarm A subsecond register low	0x00(1)

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Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5166	RTC	RTC_ALRMASSMSKR	RTC Alarm A masking register	0x00(1)
0x00 5167 to 0x00 5169		Reserved area (3 bytes)		
0x00 516A		RTC_CALRH	RTC Calibration register high	0x00(1)
0x00 516B		RTC_CALRL	RTC Calibration register low	0x00(1)
0x00 516C		RTC_TCR1	RTC Tamper control register 1	0x00(1)
0x00 516D		RTC_TCR2	RTC Tamper control register 2	0x00(1)
0x00 516E to 0x00 518A		Reserved area (36 bytes)		
0x00 5190		CSSLSE_CSR	CSS on LSE control and status register	0x00(1)
0x00 519A to 0x00 51FF	Reserved area (111 bytes)			
0x00 5200	SPI1	SPI1_CR1	SPI1 control register 1	0x00
0x00 5201		SPI1_CR2	SPI1 control register 2	0x00
0x00 5202		SPI1_ICR	SPI1 interrupt control register	0x00
0x00 5203		SPI1_SR	SPI1 status register	0x02
0x00 5204		SPI1_DR	SPI1 data register	0x00
0x00 5205		SPI1_CRCPR	SPI1 CRC polynomial register	0x07
0x00 5206		SPI1_RXCRCR	SPI1 Rx CRC register	0x00
0x00 5207		SPI1_TXCRCR	SPI1 Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		I2C1_OAR2	I2C1 own address register for dual mode	0x00
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0X
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00

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Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 521D	I2C1	I2C1_TRISER	I2C1 TRISE register	0x02
0x00 521E		I2C1_PECR	I2C1 packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 bytes)			
0x00 5230	USART1	USART1_SR	USART1 status register	0xC0
0x00 5231		USART1_DR	USART1 data register	0xXX
0x00 5232		USART1_BRR1	USART1 baud rate register 1	0x00
0x00 5233		USART1_BRR2	USART1 baud rate register 2	0x00
0x00 5234		USART1_CR1	USART1 control register 1	0x00
0x00 5235		USART1_CR2	USART1 control register 2	0x00
0x00 5236		USART1_CR3	USART1 control register 3	0x00
0x00 5237		USART1_CR4	USART1 control register 4	0x00
0x00 5238		USART1_CR5	USART1 control register 5	0x00
0x00 5239		USART1_GTR	USART1 guard time register	0x00
0x00 523A		USART1_PSCR	USART1 prescaler register	0x00
0x00 523B to 0x00 524F	Reserved area (21 bytes)			
0x00 5250	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5251		TIM2_CR2	TIM2 control register 2	0x00
0x00 5252		TIM2_SMCR	TIM2 Slave mode control register	0x00
0x00 5253		TIM2_ETR	TIM2 external trigger register	0x00
0x00 5254		TIM2_DER	TIM2 DMA1 request enable register	0x00
0x00 5255		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5256		TIM2_SR1	TIM2 status register 1	0x00
0x00 5257		TIM2_SR2	TIM2 status register 2	0x00
0x00 5258		TIM2_EGR	TIM2 event generation register	0x00
0x00 5259		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 525A		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 525B		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 525C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 525D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 525E		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 525F		TIM2_ARRH	TIM2 auto-reload register high	0xFF

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Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5260	TIM2	TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5261		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5262		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5263		TIM2_CCR2H	TIM2 capture/compare register 2 high	0x00
0x00 5264		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5265		TIM2_BKR	TIM2 break register	0x00
0x00 5266		TIM2_OISR	TIM2 output idle state register	0x00
0x00 5267 to 0x00 527F	Reserved area (25 bytes)			
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 Slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_DER	TIM3 DMA1 request enable register	0x00
0x00 5285		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5286		TIM3_SR1	TIM3 status register 1	0x00
0x00 5287		TIM3_SR2	TIM3 status register 2	0x00
0x00 5288		TIM3_EGR	TIM3 event generation register	0x00
0x00 5289		TIM3_CCMR1	TIM3 Capture/Compare mode register 1	0x00
0x00 528A		TIM3_CCMR2	TIM3 Capture/Compare mode register 2	0x00
0x00 528B		TIM3_CCER1	TIM3 Capture/Compare enable register 1	0x00
0x00 528C		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528D		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528E		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528F		TIM3_ARRH	TIM3 Auto-reload register high	0xFF
0x00 5290		TIM3_ARRL	TIM3 Auto-reload register low	0xFF
0x00 5291		TIM3_CCR1H	TIM3 Capture/Compare register 1 high	0x00
0x00 5292		TIM3_CCR1L	TIM3 Capture/Compare register 1 low	0x00
0x00 5293		TIM3_CCR2H	TIM3 Capture/Compare register 2 high	0x00
0x00 5294		TIM3_CCR2L	TIM3 Capture/Compare register 2 low	0x00
0x00 5295		TIM3_BKR	TIM3 break register	0x00
0x00 5296		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5297 to 0x00 52DF	Reserved area (72 bytes)			

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Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5317 to 0x00 533F	Reserved area (41 bytes)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00
0x00 534E		ADC1_TRIGR1	ADC1 trigger disable 1	0x00
0x00 534F		ADC1_TRIGR2	ADC1 trigger disable 2	0x00
0x00 5350		ADC1_TRIGR3	ADC1 trigger disable 3	0x00
0x00 5351		ADC1_TRIGR4	ADC1 trigger disable 4	0x00

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Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53C8 to 0x00 542F	Reserved area(104 bytes)			
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	RI Timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	RI Timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	RI I/O input register 1	0xXX
0x00 5434		RI_IOIR2	RI I/O input register 2	0xXX
0x00 5435		RI_IOIR3	RI I/O input register 3	0xXX
0x00 5436		RI_IOCMR1	RI I/O control mode register 1	0x00
0x00 5437		RI_IOCMR2	RI I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	RI I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	RI I/O switch register 1	0x00
0x00 543A		RI_IOSR2	RI I/O switch register 2	0x00
0x00 543B		RI_IOSR3	RI I/O switch register 3	0x00
0x00 543C		RI_IOGCR	RI I/O group control register	0xFF
0x00 543D		RI_ASCR1	Analog switch register 1	0x00
0x00 543E		RI_ASCR2	RI Analog switch register 2	0x00
0x00 543F		RI_RCR	RI Resistor control register	0x00
0x00 5440 to 0x00 544F	Reserved area (16 bytes)			
0x00 5450	RI	RI_CR	RI I/O control register	0x00
0x00 5451		RI_MASKR1	RI I/O mask register 1	0x00
0x00 5452		RI_MASKR2	RI I/O mask register 2	0x00
0x00 5453		RI_MASKR3	RI I/O mask register 3	0x00
0x00 5454		RI_MASKR4	RI I/O mask register 4	0x00
0x00 5455		RI_IOIR4	RI I/O input register 4	0xXX
0x00 5456		RI_IOCMR4	RI I/O control mode register 4	0x00
0x00 5457		RI_IOSR4	RI I/O switch register 4	0x00

1. These registers are not impacted by a system reset. They are reset at power-on.

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Table 8. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	CPU	Reserved area (85 bytes)		
0x00 7F60		CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC-SPR	ITC_SPR1	Interrupt Software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt Software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt Software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt Software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt Software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt Software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt Software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt Software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00

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Table 8. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F97	DM	DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only

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6 Interrupt vector mapping

Table 9. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	TLI(2)	External Top level Interrupt	-	-	-	-	0x00 8008
1	FLASH	FLASH end of programing/ write attempted to protected page interrupt	-	-	Yes	Yes	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1 half transaction/transaction complete interrupt	-	-	Yes	Yes	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3 half transaction/transaction complete interrupt	-	-	Yes	Yes	0x00 8014
4	RTC	RTC alarm A/wakeup/ tamper 1/tamper 2/tamper 3	Yes	Yes	Yes	Yes	0x00 8018
5	PVD	PVD interrupt	Yes	Yes	Yes	Yes	0x00 801C
6	EXTIB	External interrupt port B	Yes	Yes	Yes	Yes	0x00 8020
7	EXTID	External interrupt port D	Yes	Yes	Yes	Yes	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes	0x00 8044
16	Reserved						0x00 8048
17	CLK	CLK system clock switch/CSS interrupt	-	-	Yes	Yes	0x00 804C
18	ADC1	ACD1 end of conversion/ analog watchdog/ overrun interrupt	Yes	Yes	Yes	Yes	0x00 8050
19	TIM2	TIM2 update /overflow/trigger/break interrupt	-	-	Yes	Yes	0x00 8054

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Table 9. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
20	TIM2	TIM2 Capture/Compare interrupt	-	-	Yes	Yes	0x00 8058
21	TIM3	TIM3 Update /Overflow/Trigger/Break interrupt	-	-	Yes	Yes	0x00 805C
22	TIM3	TIM3 Capture/Compare interrupt	-	-	Yes	Yes	0x00 8060
23	RI	RI trigger interrupt	-	-	Yes	-	0x00 8064
24	Reserved						0x00 8068
25	TIM4	TIM4 update/overflow/ trigger interrupt	-	-	Yes	Yes	0x00 806C
26	SPI1	SPI1 TX buffer empty/ RX buffer not empty/ error/wakeup interrupt	Yes	Yes	Yes	Yes	0x00 8070
27	USART 1	USART1 transmit data register empty/ transmission complete interrupt	-	-	Yes	Yes	0x00 8074
28	USART 1	USART1 received data ready/overrun error/ idle line detected/parity error/global error interrupt	-	-	Yes	Yes	0x00 8078
29	I^2C1	I^2C1 interrupt(3)	Yes	Yes	Yes	Yes	0x00 807C

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode. In WFE mode, the interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When the interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
2. The TLI interrupt is the logic OR between TIM2 overflow interrupt, and TIM4 overflow interrupts.
3. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

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7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 10* for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L05x/15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 10. Option byte addresses

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x01
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

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Table 11. Option byte description

Option byte No.	Option description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Disable readout protection (write access via SWIM protocol) Refer to Readout protection section in the STM8L05x/15x and STM8L16x reference manual (RM0031).
OPT1	**UBC[7:0]** Size of the user boot code area 0x00: UBC is not protected. 0x01: Page 0 is write protected. 0x02: Page 0 and 1 reserved for the UBC and write protected. It covers only the interrupt vectors. 0x03: Page 0 to 2 reserved for UBC and write protected. 0x7F to 0xFF - All 128 pages reserved for UBC and write protected. The protection of the memory area not protected by the UBC is enabled through the MASS keys. Refer to User boot code section in the STM8L05x/15x and STM8L16x reference manual (RM0031).
OPT2	Reserved
OPT3	**IWDG_HW:** Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: Independent window watchdog off on Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode
	WWDG_HW: Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware
	WWDG_HALT: Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode
OPT4	**HSECNT**: Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles
	LSECNT: Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles Refer to *Table 29: LSE oscillator characteristics on page 62*.

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Table 11. Option byte description (continued)

Option byte No.	Option description
OPT5	**BOR_ON**: 0: Brownout reset off 1: Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 20* for details on the thresholds according to the value of BOR_TH bits.
OPTBL	**OPTBL[15:0]**: This option is checked by the boot ROM code after reset. Depending on content of addresses 00 480B, 00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details.

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8 Electrical parameters

8.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

8.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics is indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

8.1.2 Typical values

Unless otherwise specified, typical data is based on T_A = 25 °C, V_{DD} = 3 V. It is given only as design guidelines and is not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

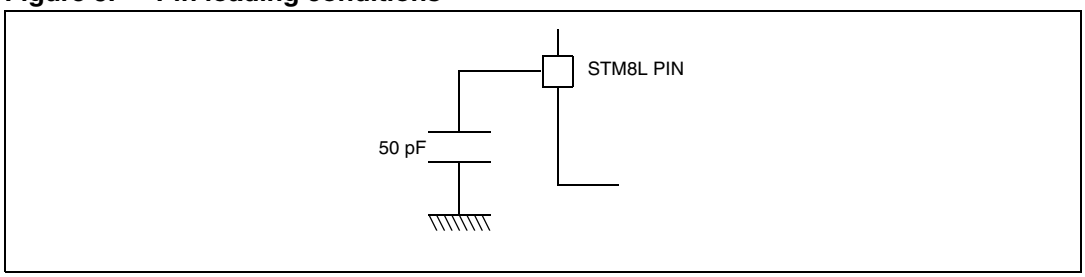
8.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

8.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 5*.

Figure 5. Pin loading conditions

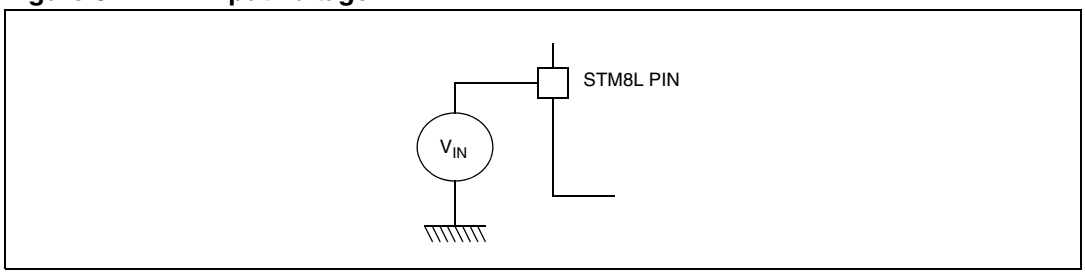


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8.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 6*.

Figure 6. Pin input voltage



8.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 12. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage (including V_{DDA} and V_{DD2})(1)	- 0.3	4.0	V
V_{IN}(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on five-volt tolerant (FT) pins (PA7 and PE0)	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on 3.6 V tolerant (TT) pins	V_{SS} - 0.3	4.0	
	Input voltage on any other pin	V_{SS} - 0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 87*		

1. All power (V_{DD1}, V_{DD2}, V_{DDA}) and ground (V_{SS1}, V_{SS2}, V_{SSA}) pins must always be connected to the external power supply.
2. V_{IN} maximum must always be respected. Refer to *Table 13.* for maximum allowed injected current values.

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Table 13. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5 / +0	
	Injected current on five-volt tolerant (FT) pins (PA7 and PE0) (1)	- 5 / +0	
	Injected current on 3.6 V tolerant (TT) pins (1)	- 5 / +0	
	Injected current on any other pin (2)	- 5 / +5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (3)	± 25	

1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 12.* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 12.* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 14. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

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8.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

8.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{SYSCLK}(1)	System clock frequency	1.8 V ≤ V_{DD} < 3.6 V	0	16	MHz
V_{DD}	Standard operating voltage		1.8	3.6	V
V_{DDA}	Analog operating voltage	Must be at the same potential as V_{DD}	1.8	3.6	V
P_D(2)	Power dissipation at T_A= 85 °C	TSSOP20		181	mW
T_A	Temperature range	1.8 V ≤ V_{DD} < 3.6 V	-40	85	°C
T_J	Junction temperature range	-40 °C ≤ T_A < 85 °C	-40	105(3)	°C

1. $f_{SYSCLK} = f_{CPU}$
2. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in “Thermal characteristics” table.
3. T_{Jmax} is given by the test limit. Above this value, the product behavior is not guaranteed.

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8.3.2 Embedded reset and power control block characteristics

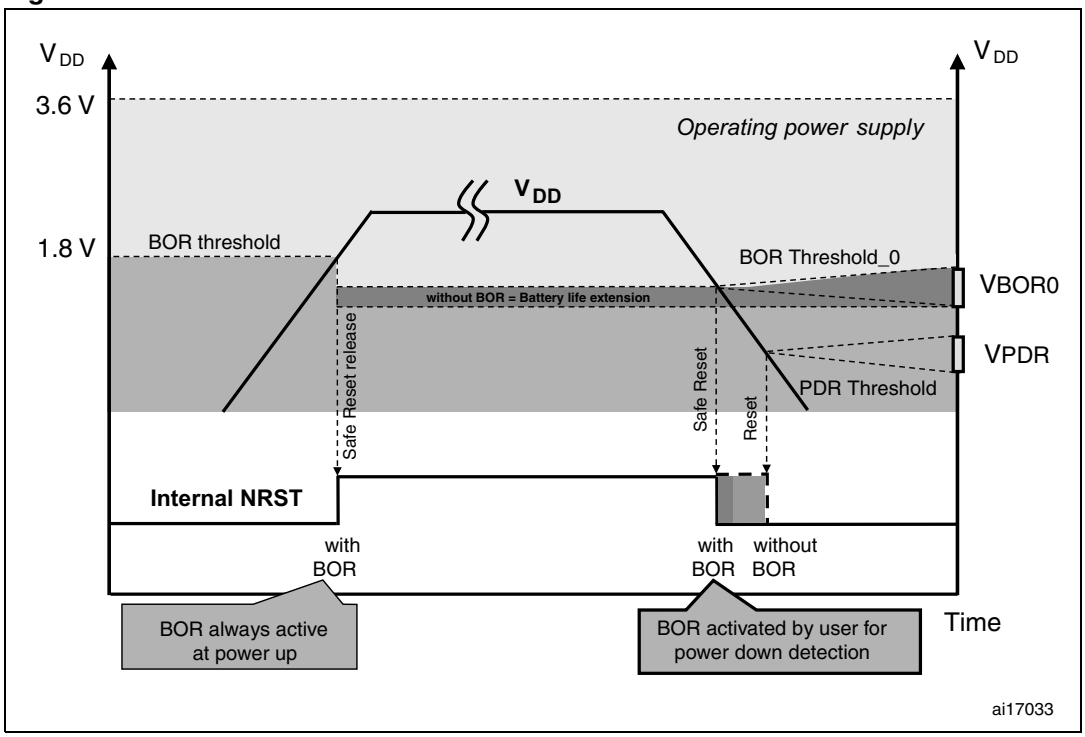
Table 16. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	BOR detector enabled	0(1)		∞ (1)	µs/V
	V_{DD} fall time rate	BOR detector enabled	20(1)		∞ (1)	
t_{TEMP}	Reset release delay	V_{DD} rising		3		ms
V_{PDR}	Power-down reset threshold	Falling edge	1.30(2)	1.50	1.65	V
V_{BOR0}	Brown-out reset threshold 0 (BOR_TH[2:0]=000)	Falling edge	1.67	1.70	1.74	V
		Rising edge	1.69	1.75	1.80	
V_{BOR1}	Brown-out reset threshold 1 (BOR_TH[2:0]=001)	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.04	2.07	
V_{BOR2}	Brown-out reset threshold 2 (BOR_TH[2:0]=010)	Falling edge	2.22	2.3	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3 (BOR_TH[2:0]=011)	Falling edge	2.45	2.55	2.60	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4 (BOR_TH[2:0]=100)	Falling edge	2.68	2.80	2.85	
		Rising edge	2.78	2.90	2.95	
V_{PVD0}	PVD threshold 0	Falling edge	1.80	1.84	1.88	V
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.2	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	

1. Data guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

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Figure 7. POR/BOR thresholds



8.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

In the following table, data is based on characterization results, unless otherwise specified.

Subject to general operating conditions for V_{DD} and T_A.

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Table 17. Total current consumption in Run mode

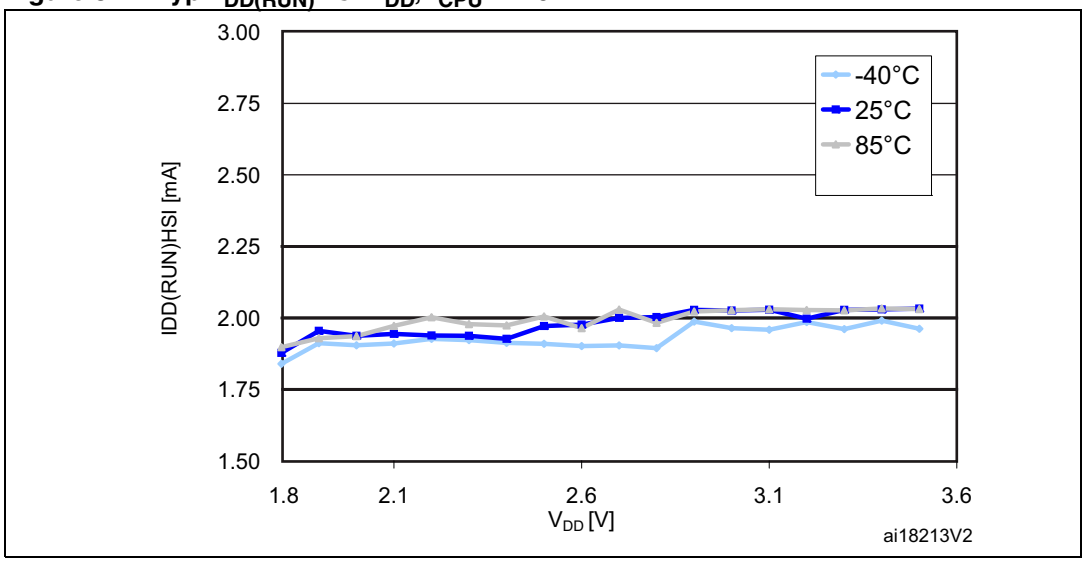
Symbol	Parameter	Conditions(1)			Typ	Max		Unit
						55 °C	85 °C	
$I_{DD(RUN)}$	Supply current in run mode(2)	All peripherals OFF, code executed from RAM, V_{DD} from 1.8 V to 3.6 V	HSI RC osc. (16 MHz)(3)	f_{CPU} = 125 kHz	0.39	0.47	0.49	mA
				f_{CPU} = 1 MHz	0.48	0.56	0.58	
				f_{CPU} = 4 MHz	0.75	0.84	0.86	
				f_{CPU} = 8 MHz	1.10	1.20	1.25	
				f_{CPU} = 16 MHz	1.85	1.93	2.12(5)	
			HSE external clock ($f_{CPU}=f_{HSE}$)(4)	f_{CPU} = 125 kHz	0.05	0.06	0.09	
				f_{CPU} = 1 MHz	0.18	0.19	0.20	
				f_{CPU} = 4 MHz	0.55	0.62	0.64	
				f_{CPU} = 8 MHz	0.99	1.20	1.21	
				f_{CPU} = 16 MHz	1.90	2.22	2.23(5)	
			LSI RC osc. (typ. 38 kHz)	$f_{CPU} = f_{LSI}$	0.040	0.045	0.046	
			LSE external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.035	0.040	0.048(5)	
$I_{DD(RUN)}$	Supply current in Run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.8 V to 3.6 V	HSI RC osc.(6)	f_{CPU} = 125 kHz	0.43	0.55	0.56	mA
				f_{CPU} = 1 MHz	0.60	0.77	0.80	
				f_{CPU} = 4 MHz	1.11	1.34	1.37	
				f_{CPU} = 8 MHz	1.90	2.20	2.23	
				f_{CPU} = 16 MHz	3.8	4.60	4.75	
			HSE external clock ($f_{CPU}=f_{HSE}$) (4)	f_{CPU} = 125 kHz	0.30	0.36	0.39	
				f_{CPU} = 1 MHz	0.40	0.50	0.52	
				f_{CPU} = 4 MHz	1.15	1.31	1.40	
				f_{CPU} = 8 MHz	2.17	2.33	2.44	
				f_{CPU} = 16 MHz	4.0	4.46	4.52	
			LSI RC osc.	$f_{CPU} = f_{LSI}$	0.110	0.123	0.130	
			LSE ext. clock (32.768 kHz)(7)	$f_{CPU} = f_{LSE}$	0.100	0.101	0.104	

1. All peripherals OFF, V_{DD} from 1.8 V to 3.6 V, HSI internal RC osc. , $f_{CPU}=f_{SYSCLK}$
2. CPU executing typical data processing
3. The run from RAM consumption can be approximated with the linear formula: I_{DD}(run_from_RAM) = Freq * 90 µA/MHz + 380 µA

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4. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 28*.
5. Tested in production.
6. The run from Flash consumption can be approximated with the linear formula: I_{DD}(run_from_Flash) = Freq * 195 µA/MHz + 440 µA
7. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 29*.

Figure 8. Typ. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from RAM

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In the following table, data is based on characterization results, unless otherwise specified.

Table 18. Total current consumption in Wait mode

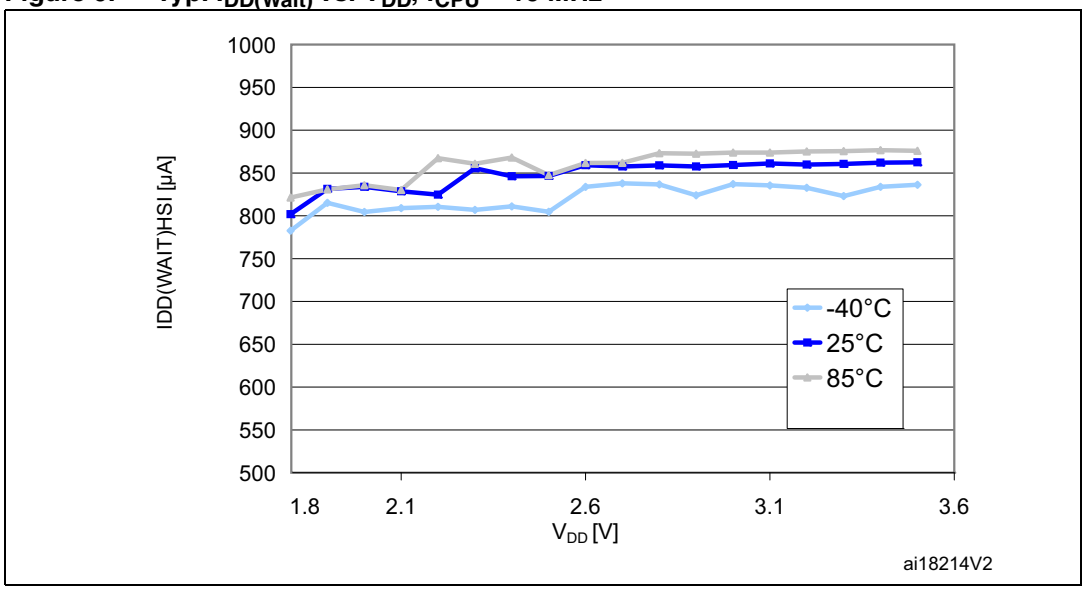
Symbol	Parameter	Conditions[1]			Typ	Max		Unit
						55°C	85°C	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from RAM with Flash in I_{DDQ} mode[2], V_{DD} from 1.8 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.33	0.39	0.41	mA
				f_{CPU} = 1 MHz	0.35	0.41	0.44	
				f_{CPU} = 4 MHz	0.42	0.51	0.52	
				f_{CPU} = 8 MHz	0.52	0.57	0.58	
				f_{CPU} = 16 MHz	0.68	0.76	0.79	
			HSE external clock (f_{CPU}=f_{HSE})[3]	f_{CPU} = 125 kHz	0.032	0.056	0.068	
				f_{CPU} = 1 MHz	0.078	0.121	0.144	
				f_{CPU} = 4 MHz	0.218	0.26	0.30	
				f_{CPU} = 8 MHz	0.40	0.52	0.57	
				f_{CPU} = 16 MHz	0.760	1.01	1.05	
			LSI	f_{CPU} = f_{LSI}	0.035	0.044	0.046	
			LSE[4] external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.032	0.036	0.038	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.8 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.38	0.48	0.49	mA
				f_{CPU} = 1 MHz	0.41	0.49	0.51	
				f_{CPU} = 4 MHz	0.50	0.57	0.58	
				f_{CPU} = 8 MHz	0.60	0.66	0.68	
				f_{CPU} = 16 MHz	0.79	0.84	0.86	
			HSE[3] external clock (f_{CPU}=HSE)	f_{CPU} = 125 kHz	0.06	0.08	0.09	
				f_{CPU} = 1 MHz	0.10	0.17	0.18	
				f_{CPU} = 4 MHz	0.24	0.36	0.39	
				f_{CPU} = 8 MHz	0.50	0.58	0.61	
				f_{CPU} = 16 MHz	1.00	1.08	1.14	
			LSI	f_{CPU} = f_{LSI}	0.055	0.058	0.065	
			LSE[4] external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.051	0.056	0.060	

1. All peripherals OFF, V_{DD} from 1.8 V to 3.6 V, HSI internal RC osc. , f_{CPU} = f_{SYSCLK}
2. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
3. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 28*.

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4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 29*.

Figure 9. Typ. $I_{DD(Wait)}$ vs. V_{DD}, f_{CPU} = 16 MHz 1)



1. Typical current consumption measured with code executed from Flash memory.

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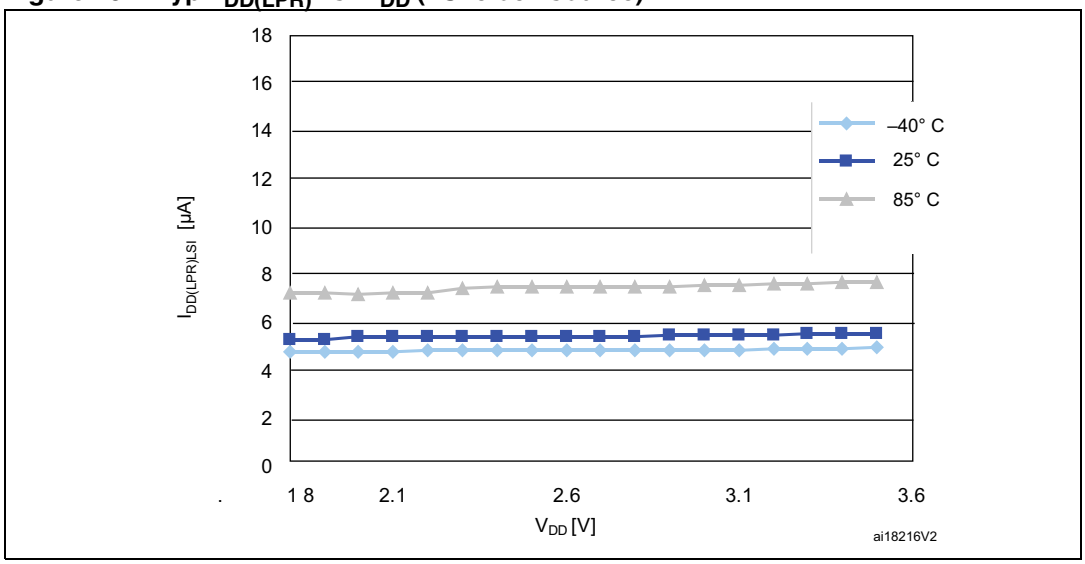
In the following table, data is based on characterization results, unless otherwise specified.

Table 19. Total current consumption and timing in Low power run mode at V_{DD} = 1.8 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ	Max	Unit
$I_{DD(LPR)}$	Supply current in Low power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.1	5.4	µA
				T_A = 55 °C	5.7	6	
				T_A = 85 °C	6.8	7.5	
			with TIM2 active(2)	T_A = -40 °C to 25 °C	5.4	5.7	
				T_A = 55 °C	6.0	6.3	
				T_A = 85 °C	7.2	7.8	
		LSE (3) external clock (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.25	5.6	
				T_A = 55 °C	5.67	6.1	
				T_A = 85 °C	5.85	6.3	
			with TIM2 active (2)	T_A = -40 °C to 25 °C	5.59	6	
				T_A = 55 °C	6.10	6.4	
				T_A = 85 °C	6.30	7	

1. No floating I/Os
2. Timer 2 clock enabled and counter running
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 29*

Figure 10. Typ. $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source)



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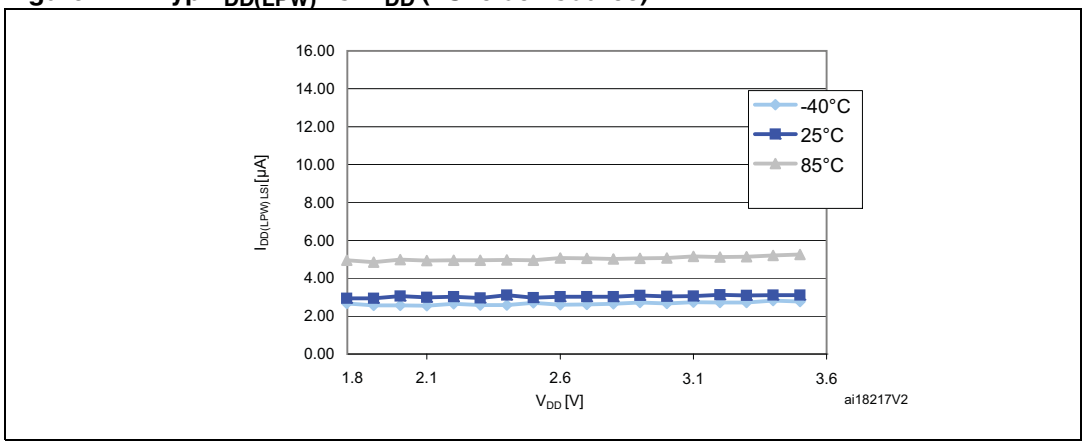
In the following table, data is based on characterization results, unless otherwise specified.

Table 20. Total current consumption in Low power wait mode at V_{DD} = 1.8 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ	Max	Unit
$I_{DD(LPW)}$	Supply current in Low power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3	3.3	µA
				T_A = 55 °C	3.3	3.6	
				T_A = 85 °C	4.4	5	
			with TIM2 active(2)	T_A = -40 °C to 25 °C	3.4	3.7	
				T_A = 55 °C	3.7	4	
				T_A = 85 °C	4.8	5.4	
		LSE external clock(3) (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	2.35	2.7	
				T_A = 55 °C	2.42	2.82	
				T_A = 85 °C	3.10	3.71	
			with TIM2 active (2)	T_A = -40 °C to 25 °C	2.46	2.75	
				T_A = 55 °C	2.50	2.81	
				T_A = 85 °C	3.16	3.82	

1. No floating I/Os.
2. Timer 2 clock enabled and counter is running.
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 29*.

Figure 11. Typ. $I_{DD(LPW)}$ vs. V_{DD} (LSI clock source)



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In the following table, data is based on characterization results, unless otherwise specified.

Table 21. Total current consumption and timing in Active-halt mode at V_{DD} = 1.8 V to 3.6 V

Symbol	Parameter	Conditions (1)		Typ	Max	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	T_A = -40 °C to 25 °C	0.9	2.1	µA
			T_A = 55 °C	1.2	3	
			T_A = 85 °C	1.5	3.4	
		LSE external clock (32.768 kHz)(2)	T_A = -40 °C to 25 °C	0.5	1.2	
			T_A = 55 °C	0.62	1.4	
			T_A = 85 °C	0.88	2.1	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)			2.4		mA
$t_{WU_HSI(AH)}$ (3)(4)	Wakeup time from Active-halt mode to Run mode (using HSI)			4.7	7	µs
$t_{WU_LSI(AH)}$ (3) (4)	Wakeup time from Active-halt mode to Run mode (using LSI)			150		µs

1. No floating I/O, unless otherwise specified.
2. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 29*.
3. Wakeup time until start of interrupt vector fetch.
The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.
4. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

Table 22. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

Symbol	Parameter	Condition(1)		Typ	Unit
$I_{DD(AH)}$ (2)	Supply current in Active-halt mode	V_{DD} = 1.8 V	LSE	1.15	µA
			LSE/32(3)	1.05	
		V_{DD} = 3 V	LSE	1.30	
			LSE/32(3)	1.20	
		V_{DD} = 3.6 V	LSE	1.45	
			LSE/32(3)	1.35	

1. No floating I/O, unless otherwise specified.
2. Based on measurements on bench with 32.768 kHz external crystal oscillator.
3. RTC clock is LSE divided by 32.

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In the following table, data is based on characterization results, unless otherwise specified.

Table 23. Total current consumption and timing in Halt mode at V_{DD} = 1.8 to 3.6 V

Symbol	Parameter	Condition(1)	Typ	Max	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (Ultra-low-power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	350	1400(2)	nA
		T_A = 55 °C	580	2000	
		T_A = 85 °C	1160	2800(2)	
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)		2.4		mA
$t_{WU_HSI(Halt)}$(3)(4)	Wakeup time from Halt to Run mode (using HSI)		4.7	7	µs
$t_{WU_LSI(Halt)}$ (3)(4)	Wakeup time from Halt mode to Run mode (using LSI)		150		µs

1. T_A = -40 to 85 °C, no floating I/O, unless otherwise specified.
2. Tested in production.
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.
4. Wakeup time until start of interrupt vector fetch.
The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.

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Current consumption of on-chip peripherals

Table 24. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM2)}$	TIM2 supply current (1)		8	µA/MHz
$I_{DD(TIM3)}$	TIM3 supply current (1)		8	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (2)		6	
$I_{DD(SPI1)}$	SPI1 supply current (2)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (2)		5	
$I_{DD(DMA1)}$	DMA1 supply current(2)		3	
$I_{DD(WWDG)}$	WWDG supply current(2)		2	
$I_{DD(ALL)}$	Peripherals ON(3)		44	µA/MHz
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (5)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (5)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, USART1, SPI1, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.
5. Including supply current of internal reference voltage.

Table 25. Current consumption under external reset

Symbol	Parameter	Conditions		Typ	Unit
$I_{DD(RST)}$	Supply current under external reset (1)	All pins are externally tied to V_{DD}	V_{DD} = 1.8 V	48	µA
			V_{DD} = 3 V	76	
			V_{DD} = 3.6 V	91	

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset.

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8.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 26. HSE external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency(1)		1		16	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7 x V_{DD}		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		0.3 x V_{DD}	
$C_{in(HSE)}$	OSC_IN input capacitance(1)			2.6		pF
I_{LEAK_HSE}	OSC_IN input leakage current	$V_{SS} < V_{IN} < V_{DD}$			±1	µA

1. Data guaranteed by Design, not tested in production.

LSE external clock (LSEBYP=1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 27. LSE external clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency(1)		32.768		kHz
V_{LSEH}(2)	OSC32_IN input pin high level voltage	0.7 x V_{DD}		V_{DD}	V
V_{LSEL}(2)	OSC32_IN input pin low level voltage	V_{SS}		0.3 x V_{DD}	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		0.6		pF
I_{LEAK_LSE}	OSC32_IN input leakage current			±1	µA

1. Data guaranteed by Design, not tested in production.
2. Data based on characterization results, not tested in production.

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HSE crystal/ceramic resonator oscillator

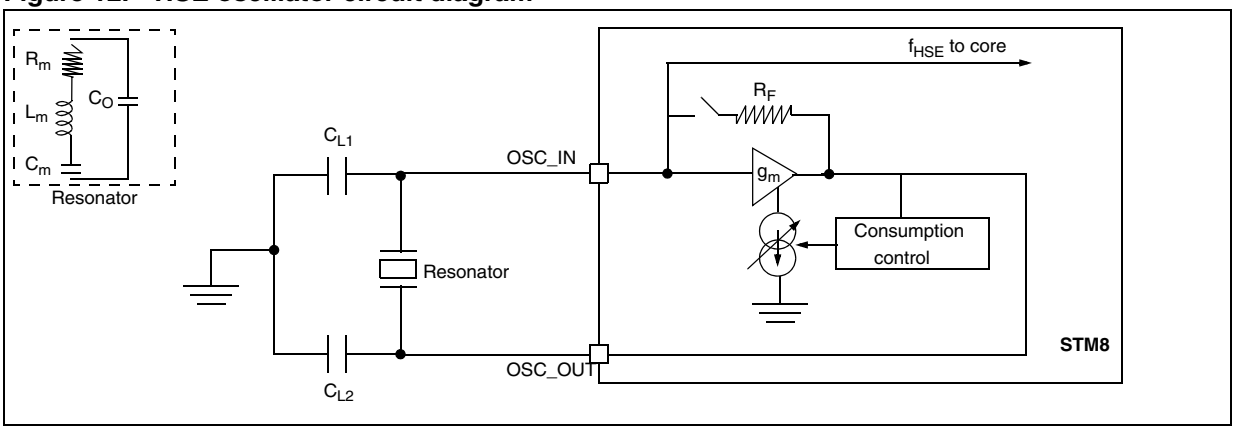
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 28. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High speed external oscillator frequency		1		16	MHz
R_F	Feedback resistor			200		kΩ
$C^{(1)}$	Recommended load capacitance (2)			20		pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz			2.5 (startup) 0.7 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} =16 MHz			2.5 (startup) 0.46 (stabilized)(3)	
g_m	Oscillator transconductance		3.5(3)			mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized		1		ms

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data guaranteed by Design. Not tested in production.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 12. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification), C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification), $C_{L1}=C_{L2}=C$: Grounded external capacitance
$g_m >> g_{mcrit}$

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LSE crystal/ceramic resonator oscillator

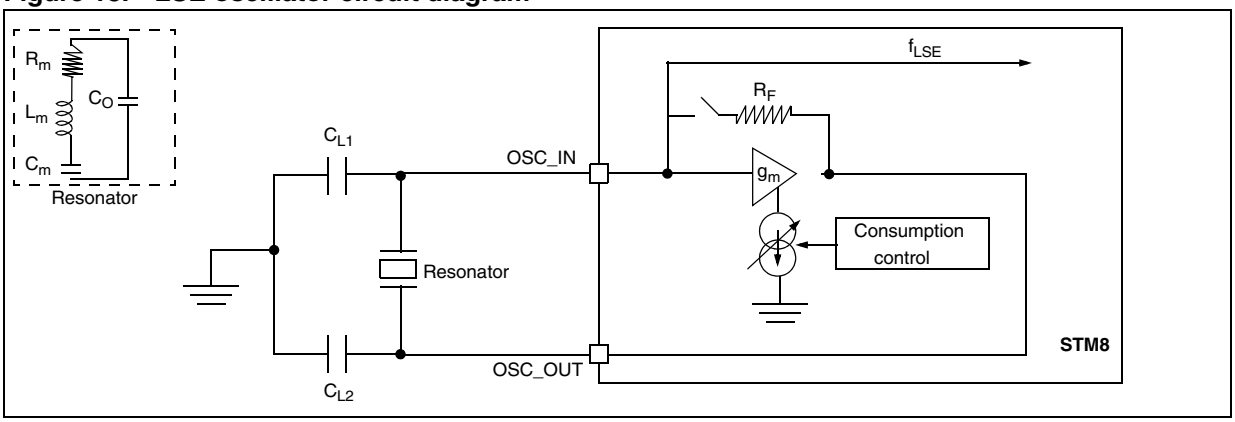
The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 29. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency			32.768		kHz
R_F	Feedback resistor	ΔV = 200 mV		1.2		MΩ
C(1)	Recommended load capacitance (2)			8		pF
$I_{DD(LSE)}$	LSE oscillator power consumption				1.4(3)	µA
		V_{DD} = 1.8 V		450		nA
		V_{DD} = 3 V		600		
		V_{DD} = 3.6 V		750		
g_m	Oscillator transconductance		3(3)			µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized		1		s

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Data guaranteed by Design. Not tested in production.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 13. LSE oscillator circuit diagram



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Internal clock sources

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High speed internal RC oscillator (HSI)

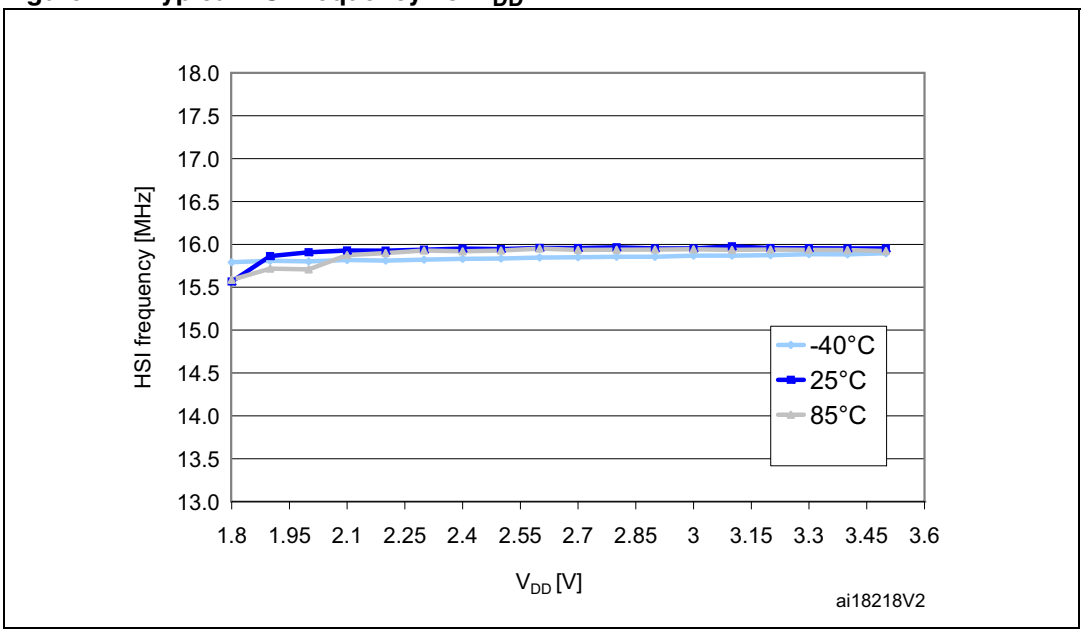
In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V		16		MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1 (2)		1(2)	%
		1.8 V ≤ V_{DD} ≤ 3.6 V, -40 °C ≤ T_A ≤ 85 °C	-5		5	%
TRIM	HSI user trimming step(3)	Trimming code ≠ multiple of 16		0.4	0.7	%
		Trimming code = multiple of 16			± 1.5	%
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)			3.7	6(4)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			100	140(4)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 85 °C unless otherwise specified.
2. Tested in production.
3. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.
4. Guaranteed by design, not tested in production.

Figure 14. Typical HSI frequency vs. V_{DD}



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Low speed internal RC oscillator (LSI)

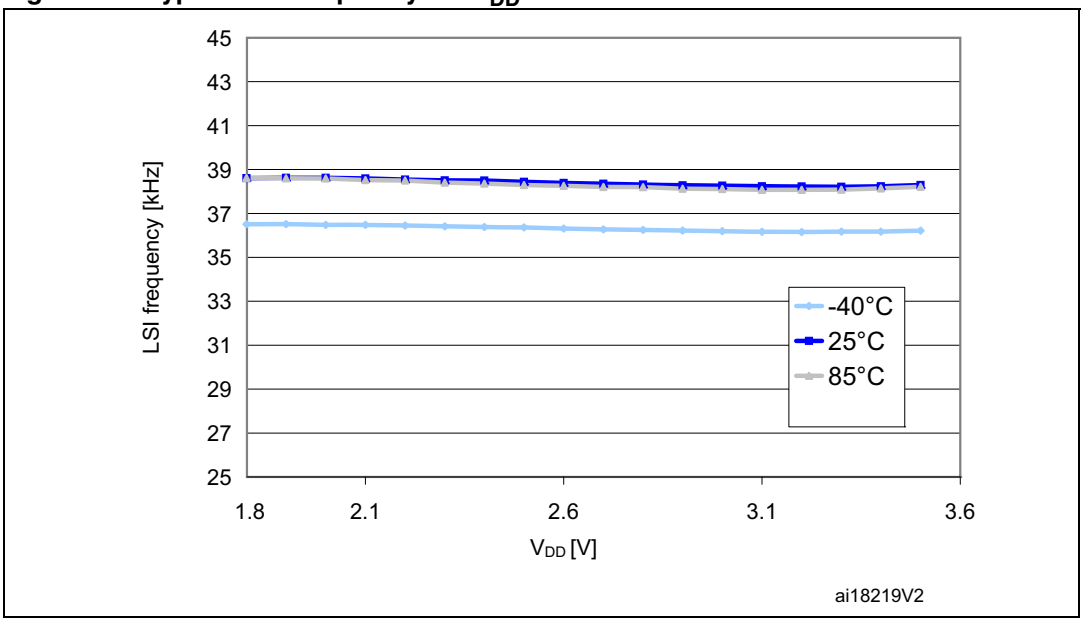
In the following table, data is based on characterization results, not tested in production.

Table 31. LSI oscillator characteristics

Symbol	Parameter (1)	Conditions(1)	Min	Typ	Max	Unit
f_{LSI}	Frequency		26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time				200(2)	µs
$I_{DD(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤ T_A ≤ 85 °C	-12		11	%

1. V_{DD} = 1.8 V to 3.6 V, T_A = -40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. This is a deviation for an individual part, once the initial frequency has been measured.

Figure 15. Typical LSI frequency vs. V_{DD}



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8.3.5 Memory characteristics

T_A = -40 to 85 °C unless otherwise specified.

Table 32. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.8			V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 33. Flash program and data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.8		3.6	V
t_{prog}	Programming time for 1 or 64 bytes (block) erase/write cycles (on programmed byte)			6		ms
	Programming time for 1 to 64 bytes (block) write cycles (on erased byte)			3		ms
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V		0.7		mA
		T_A=+25 °C, V_{DD} = 1.8 V				
t_{RET} (2)	Data retention (program memory) after 100 erase/write cycles at T_A= –40 to +85 °C	T_{RET} = +85 °C	30(1)			years
	Data retention (data memory) after 100000 erase/write cycles at T_A= –40 to +85 °C	T_{RET} = +85 °C	30(1)			
N_{RW} (3)	Erase/write cycles (program memory)	T_A = –40 to +85 °C	100(1)			cycles
	Erase/write cycles (data memory)		100(1) (4)			kcycles

1. Data based on characterization results, not tested in production.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

8.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

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Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

Table 34. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on true open-drain pins (PC0 and PC1)	-5	+0	mA
	Injected current on all five-volt tolerant (FT) pins	-5	+0	
	Injected current on all 3.6 V tolerant (TT) pins	-5	+0	
	Injected current on any other pin	-5	+5	

8.3.7 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

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Table 35. I/O static characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
V_{IL}	Input low level voltage(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS}-0.3		0.3 x V_{DD}	V
		Input voltage on five-volt tolerant (FT) pins (PA7 and PE0)	V_{SS}-0.3		0.3 x V_{DD}	
		Input voltage on 3.6 V tolerant (TT) pins	V_{SS}-0.3		0.3 x V_{DD}	
		Input voltage on any other pin	V_{SS}-0.3		0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Input voltage on true open-drain pins (PC0 and PC1) with V_{DD} < 2 V	0.70 x V_{DD}		5.2	V
		Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} \geq$ 2 V			5.5	
		Input voltage on five-volt tolerant (FT) pins (PA7 and PE0) with V_{DD} < 2 V	0.70 x V_{DD}		5.2	
		Input voltage on five-volt tolerant (FT) pins (PA7 and PE0) with $V_{DD} \geq$ 2 V			5.5	
		Input voltage on 3.6 V tolerant (TT) pins			3.6	
		Input voltage on any other pin	0.70 x V_{DD}		V_{DD}+0.3	
V_{hys}	Schmitt trigger voltage hysteresis (3)	I/Os		200		mV
		True open drain I/Os		200		
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ High sink I/Os	-	-	50 (5)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200(5)	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200(5)	
R_{PU}	Weak pull-up equivalent resistor(2)(6)	$V_{IN}=V_{SS}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. V_{DD} = 3.0 V, T_A = -40 to 85 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 19*).

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Figure 16. Typical V_{IL} and V_{IH} vs. V_{DD} (high sink I/Os)

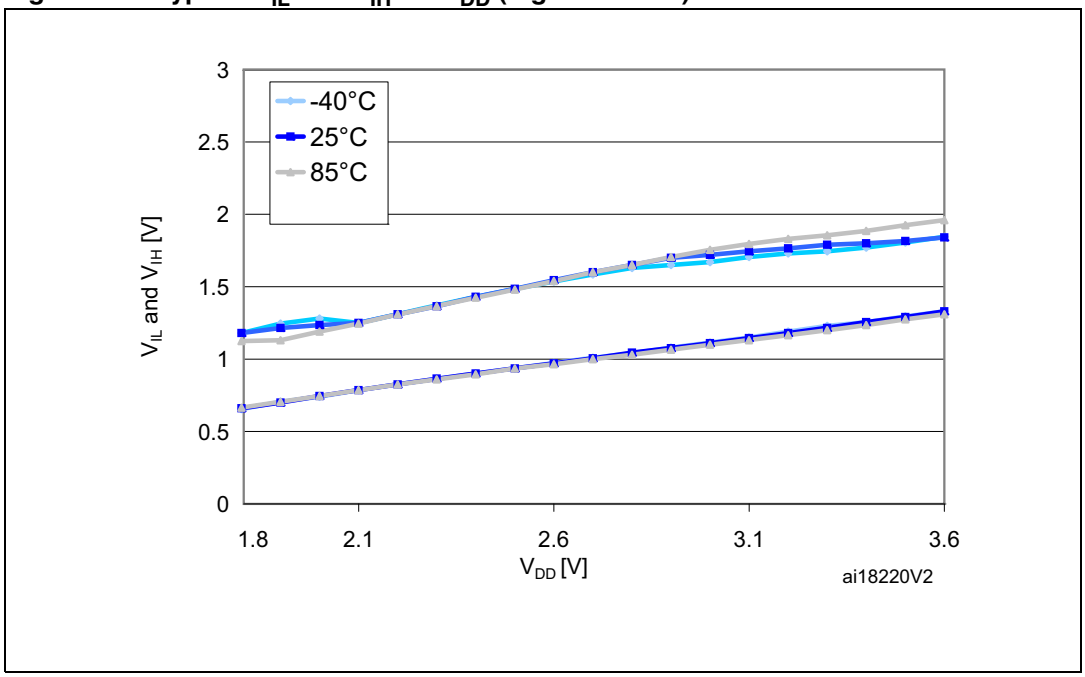
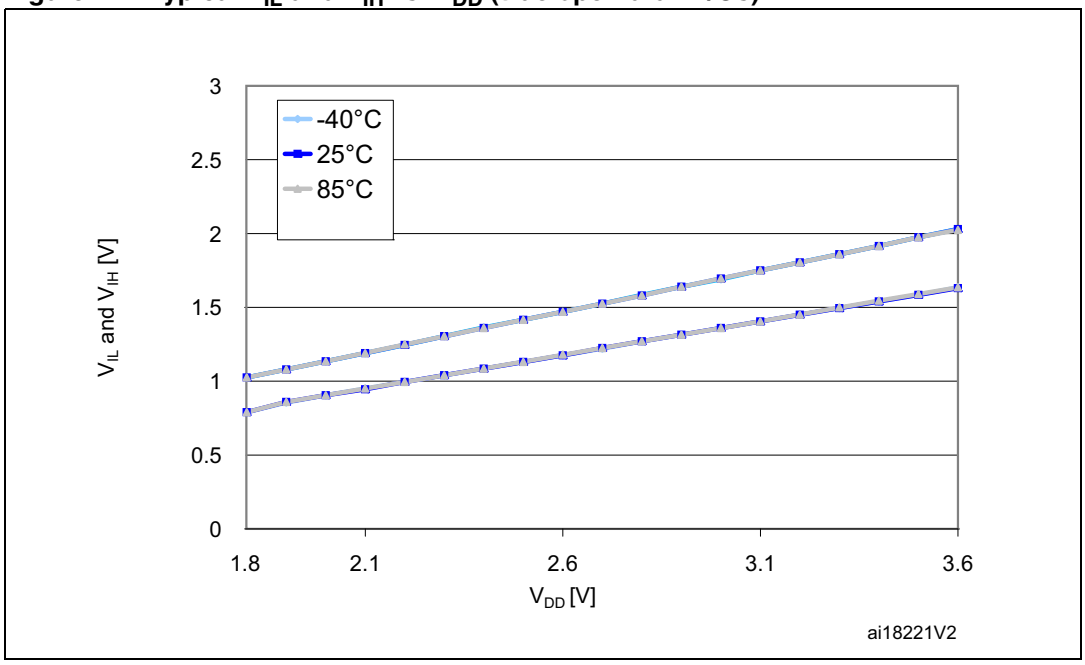


Figure 17. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)



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Figure 18. Typical pull-up resistance R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

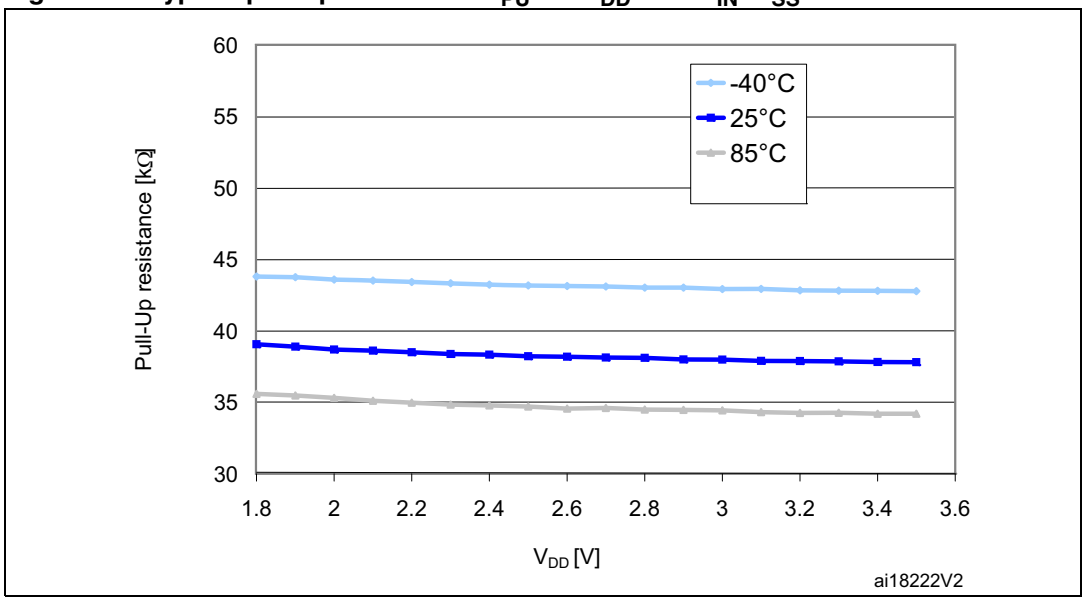
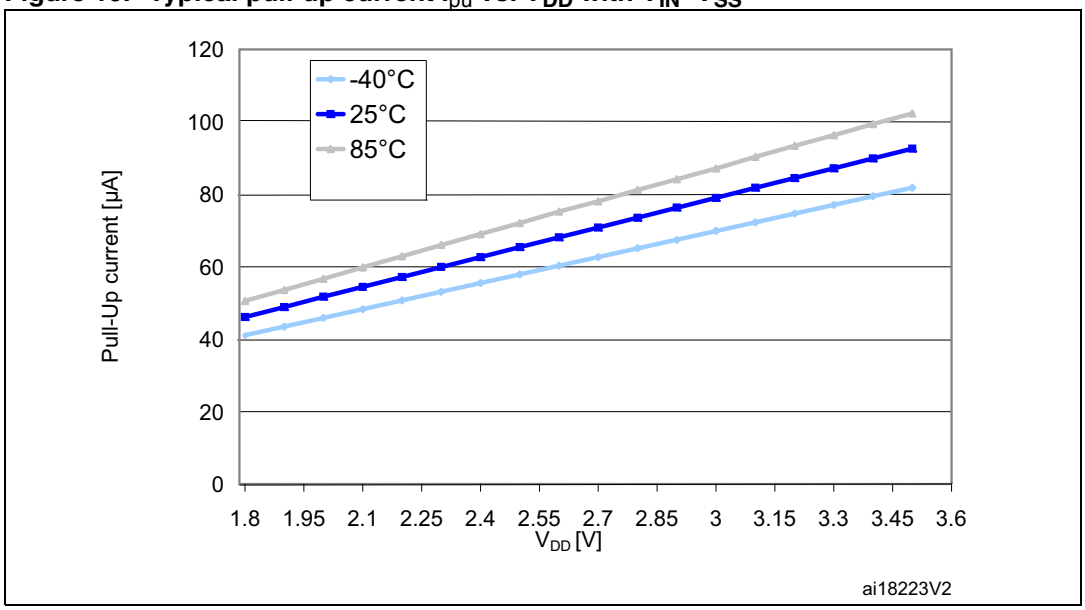


Figure 19. Typical pull-up current I_{pu} vs. V_{DD} with $V_{IN}=V_{SS}$



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Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 36. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V		0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V		0.45	V
			I_{IO} = +10 mA, V_{DD} = 3.0 V		0.7	V
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45		V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45		V
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7		V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 37. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V		0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V		0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 38. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V		0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

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Figure 20. Typ. V_{OL} @ V_{DD} = 3.0 V (high sink ports)

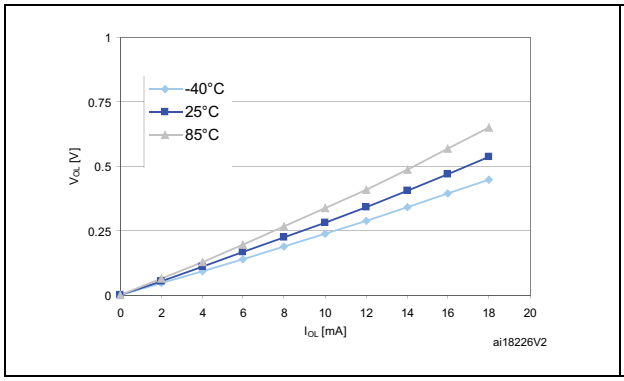


Figure 21. Typ. V_{OL} @ V_{DD} = 1.8 V (high sink ports)

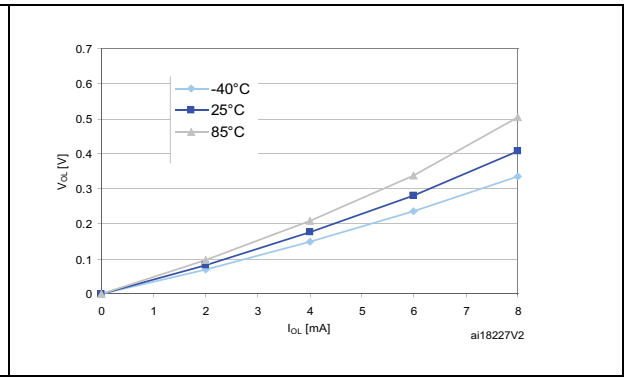


Figure 22. Typ. V_{OL} @ V_{DD} = 3.0 V (true open drain ports)

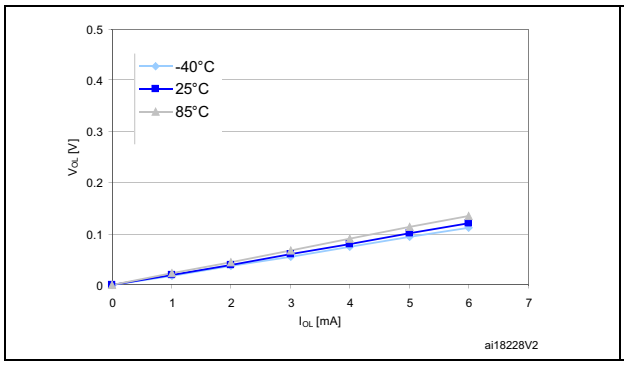


Figure 23. Typ. V_{OL} @ V_{DD} = 1.8 V (true open drain ports)

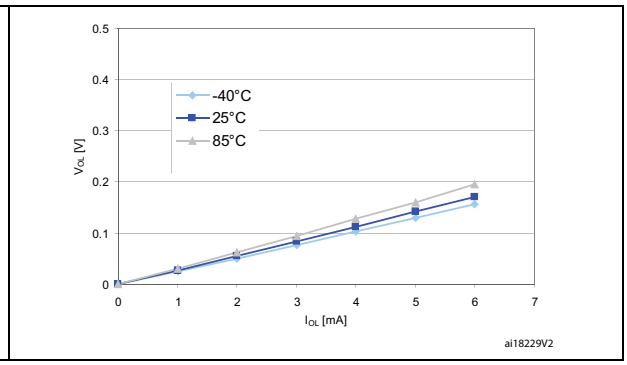


Figure 24. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.0 V (high sink ports)

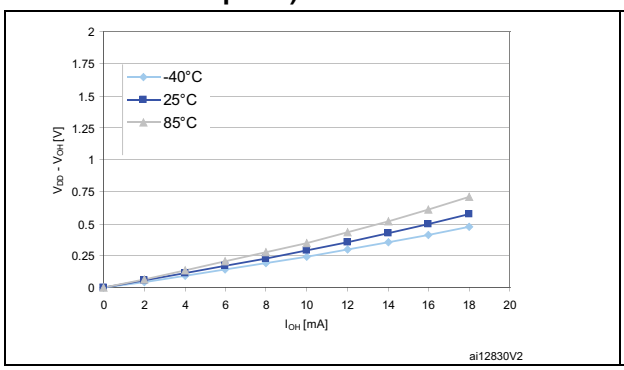
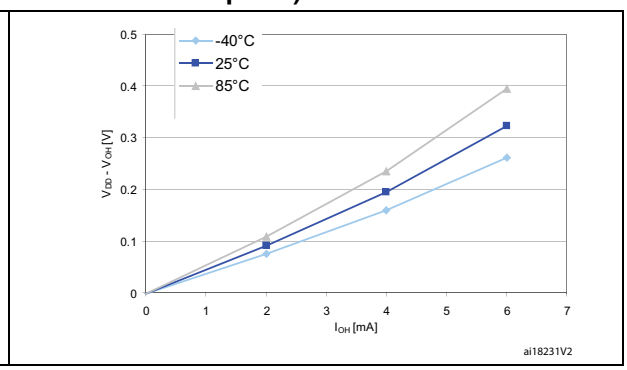


Figure 25. Typ. V_{DD} - V_{OH} @ V_{DD} = 1.8 V (high sink ports)



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NRST pin

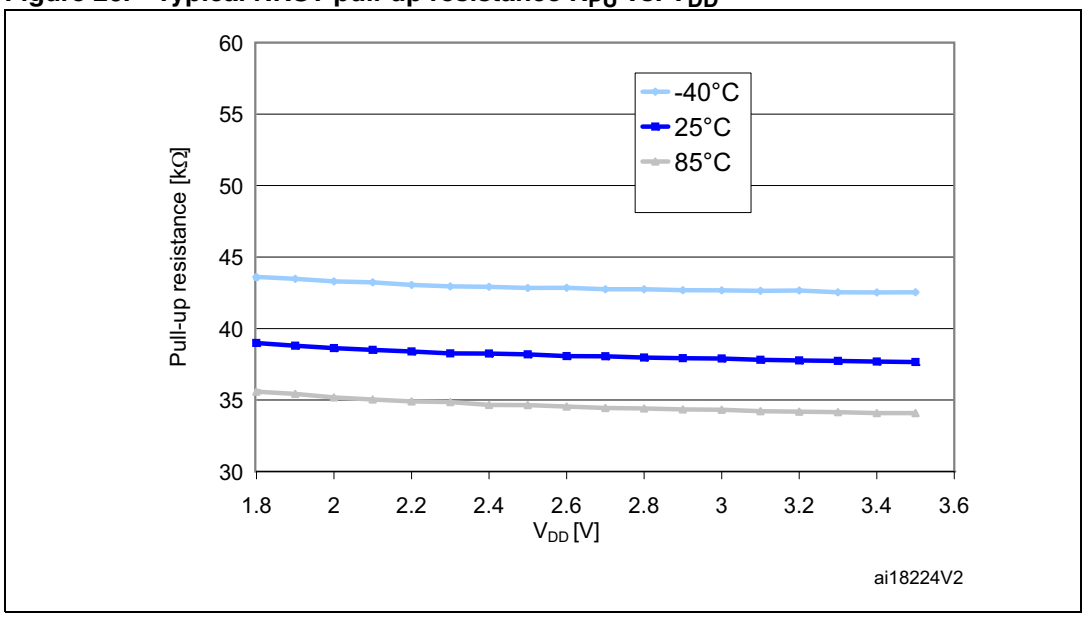
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 39. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)		V_{SS}		0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)		1.4		V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL} = 2 mA for 2.7 V ≤ V_{DD} ≤ 3.6 V			0.4	
		I_{OL} = 1.5 mA for V_{DD} < 2.7 V				
V_{HYST}	NRST input hysteresis(3)		10%V_{DD} (2)			mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor (1)		30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)				50	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)		300			

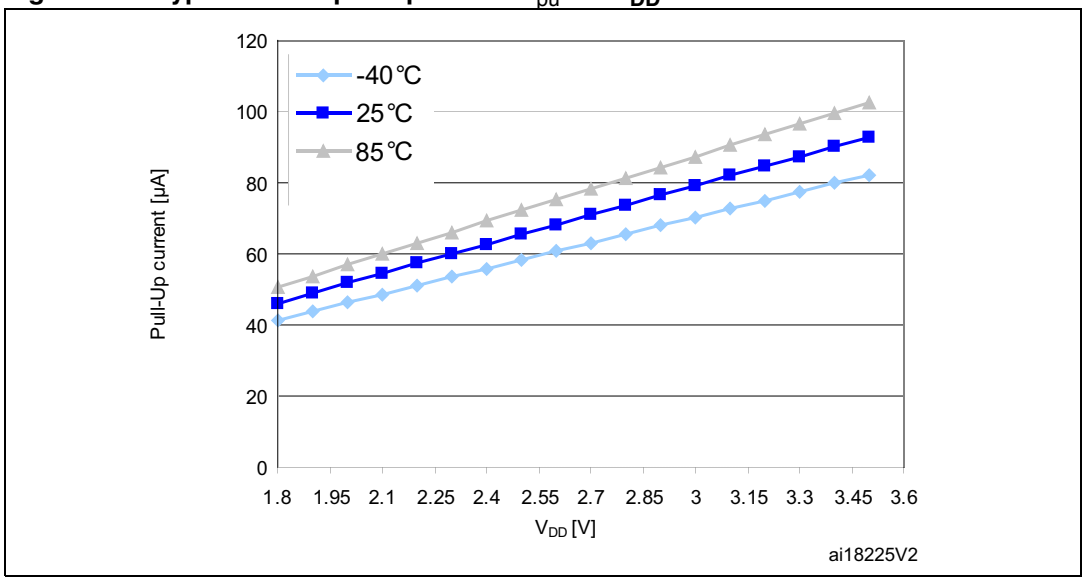
1. Data based on characterization results, not tested in production.
2. 200 mV min.
3. Data guaranteed by design, not tested in production.

Figure 26. Typical NRST pull-up resistance R_{PU} vs. V_{DD}



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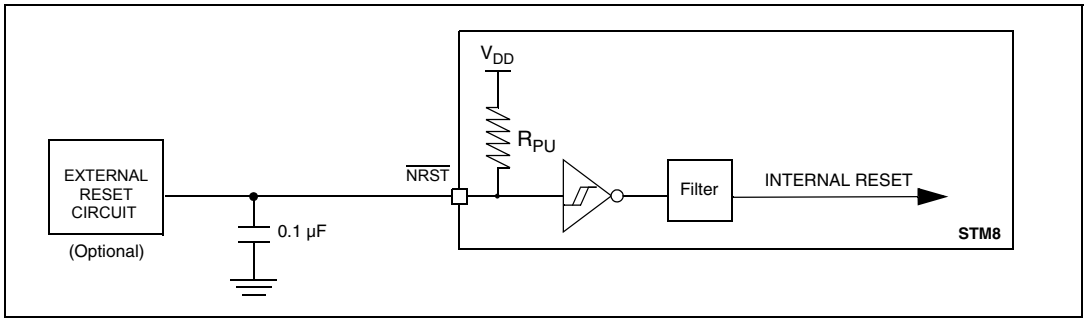
Figure 27. Typical NRST pull-up current I_{pu} vs. V_{DD}



The reset network shown in *Figure 28* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max. level specified in *Table 39*. Otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, attention must be paid to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. The minimum recommended capacity is 10 nF.

Figure 28. Recommended NRST pin configuration



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8.3.8 Communication interfaces

SPI1 - Serial peripheral interface

Unless otherwise specified, the parameters given in *Table 40* are derived from tests performed under ambient temperature, f_{SYSCLK} frequency and V_{DD} supply voltage conditions summarized in *Section 8.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 40. SPI1 characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI1 clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI1 clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x $1/f_{SYSCLK}$	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x $1/f_{SYSCLK}$	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

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Figure 29. SPI1 timing diagram - slave mode and CPHA=0

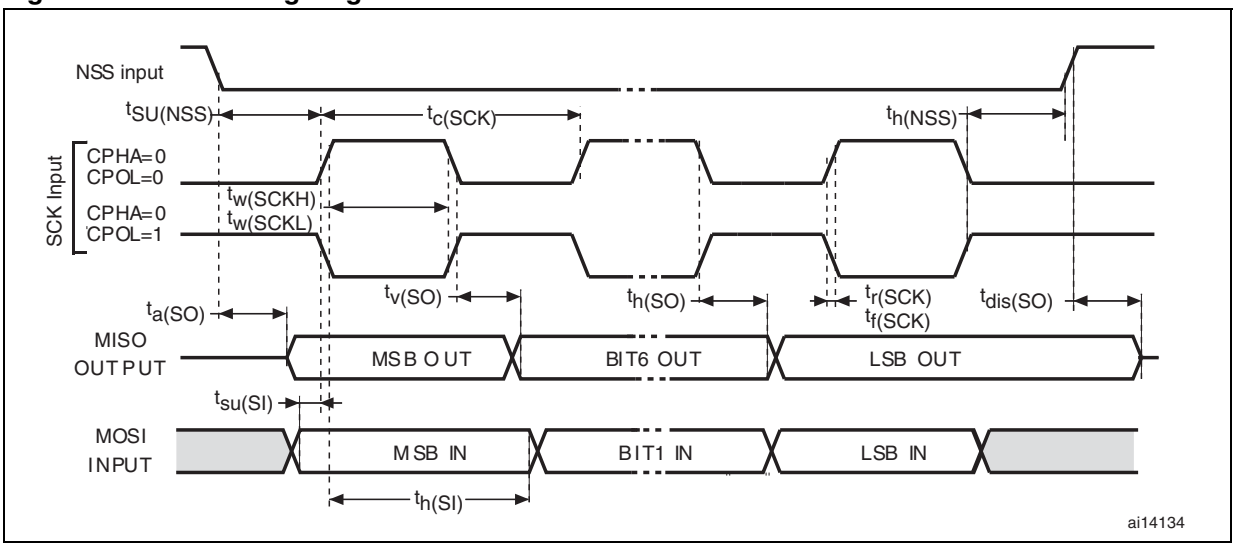
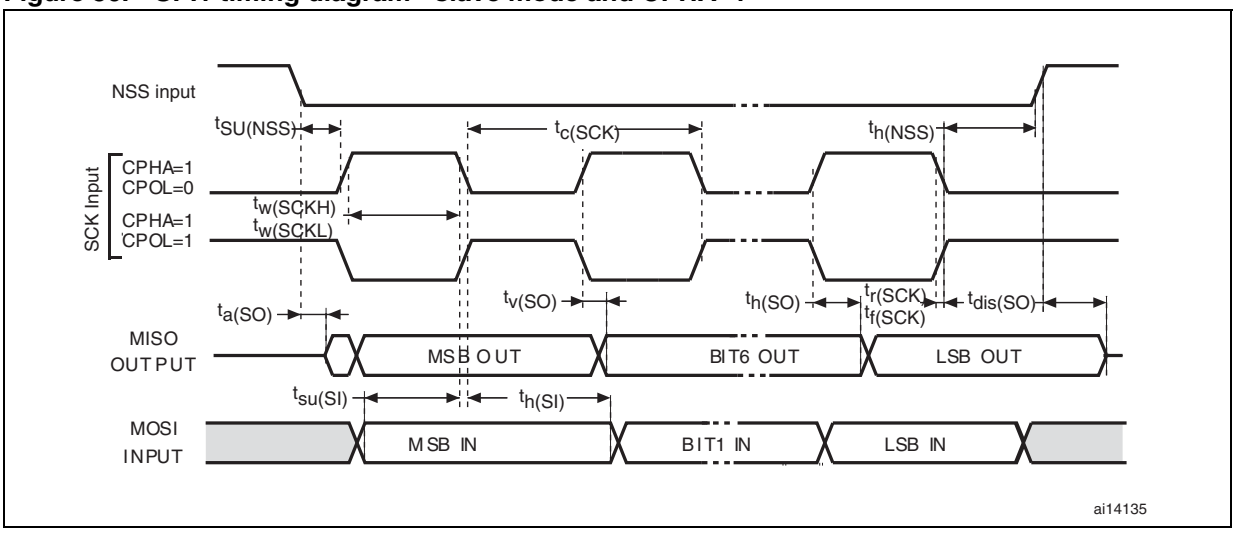


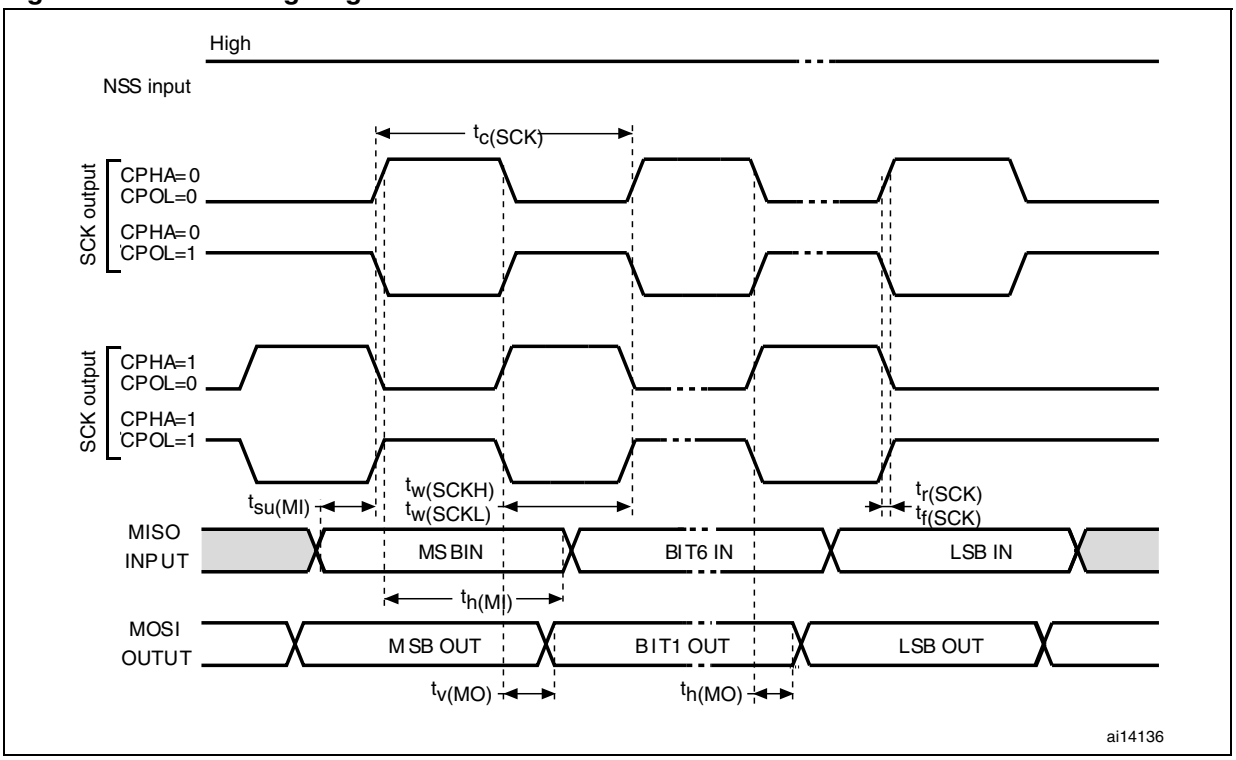
Figure 30. SPI1 timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

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Figure 31. SPI1 timing diagram - master mode



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

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I²C - Inter IC control interface

Subject to general operating conditions for V_{DD}, f_{SYSCLK}, and T_A unless otherwise specified.

The STM8L I²C interface (I2C1) meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 41. I²C characteristics

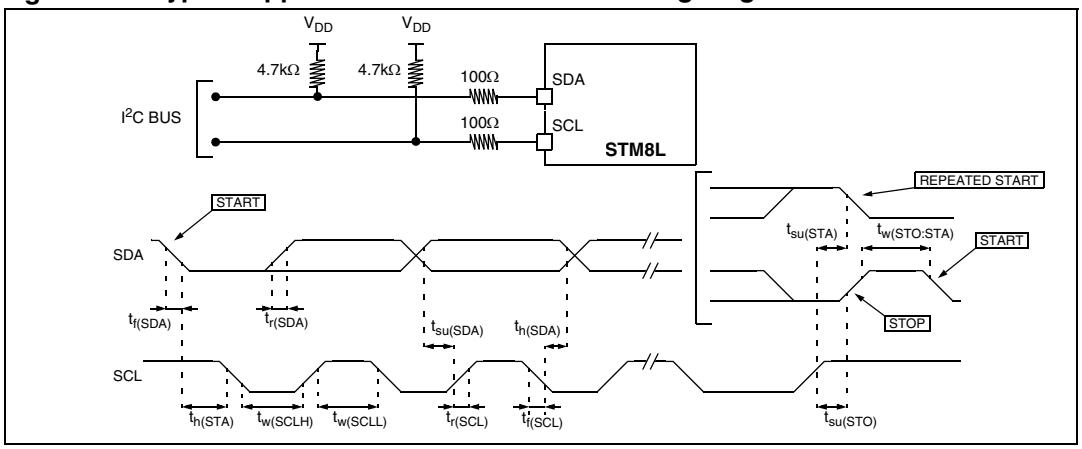
Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I²C speed (400 kHz).
2. Data based on standard I²C protocol requirement, not tested in production.

Note: For speeds around 200 kHz, the achieved speed can have a ± 5% tolerance
For other speed ranges, the achieved speed can have a ± 2% tolerance
The above variations depend on the accuracy of the external components used.

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Figure 32. Typical application with I²C bus and timing diagram 1)



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

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8.3.9 Embedded reference voltage

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 42. Reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max.	Unit
I_{REFINT}	Internal reference voltage consumption			1.4		µA
$T_{S_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage			5	10	µs
I_{BUF}(2)	Internal reference voltage buffer consumption (used for ADC)			13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output		1.202(3)	1.224	1.242(3)	V
I_{LPBUF}(2)	Internal reference voltage low power buffer consumption			730	1200	nA
I_{REFOUT}(2)	Buffer output current(4)				1	µA
C_{REFOUT}	Reference voltage output load				50	pF
$t_{VREFINT}$	Internal reference voltage startup time			2	3	ms
t_{BUFEN}(2)	Internal reference voltage buffer startup time once enabled (1)				10	µs
$ACC_{VREFINT}$	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte(5)				± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤ T_A ≤ 85 °C		20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤ T_A ≤ 50 °C			20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours				TBD	ppm

1. Defined when ADC output reaches its final value ±1/2LSB
2. Data guaranteed by Design. Not tested in production.
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guaranty less than 1% V_{REFOUT} deviation.
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

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8.3.10 12-bit ADC1 characteristics

In the following table, data is guaranteed by design, not tested in production.

Table 43. ADC1 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage		1.8		3.6	V
V_{REF+}	Reference supply voltage	2.4 V ≤ V_{DDA}≤ 3.6 V	2.4		V_{DDA}	V
		1.8 V ≤ V_{DDA}≤ 2.4 V	V_{DDA}			V
V_{REF-}	Lower reference voltage		V_{SSA}			V
I_{VDDA}	Current on the V_{DDA} input pin			1000	1450	µA
I_{VREF+}	Current on the V_{REF+} input pin			400	700 (peak)(1)	µA
					450 (average)(1)	µA
V_{AIN}	Conversion voltage range		0(2)		V_{REF+}	
T_A	Temperature range		-40		85	°C
R_{AIN}	External resistance on V_{AIN}	on PF0 fast channel			50(3)	kΩ
		on all other channels				
C_{ADC}	Internal sample and hold capacitor	on PF0 fast channel		16		pF
		on all other channels				
f_{ADC}	ADC sampling clock frequency	2.4 V≤ V_{DDA}≤ 3.6 V without zooming	0.320		16	MHz
		1.8 V≤ V_{DDA}≤ 2.4 V with zooming	0.320		8	MHz
f_{CONV}	12-bit conversion rate	V_{AIN} on PF0 fast channel			1(4)(5)	MHz
		V_{AIN} on all other channels			760(4)(5)	kHz
f_{TRIG}	External trigger frequency				t_{conv}	$1/f_{ADC}$
t_{LAT}	External trigger latency				3.5	$1/f_{SYSCLK}$

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Table 43. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	V_{AIN} on PF0 fast channel V_{DDA} < 2.4 V	0.43(4)(5)			µs
		V_{AIN} on PF0 fast channel 2.4 V ≤ V_{DDA}≤ 3.6 V	0.22(4)(5)			µs
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(4)(5)			µs
		V_{AIN} on slow channels 2.4 V ≤ V_{DDA}≤ 3.6 V	0.41(4)(5)			µs
t_{conv}	12-bit conversion time		12 + t_S			$1/f_{ADC}$
		16 MHz	1(4)			µs
t_{WKUP}	Wakeup time from OFF state				3	µs
t_{IDLE}(6)	Time before a new conversion	T_A = +25 °C			1(7)	s
		T_A = +70 °C			20(7)	ms
$t_{VREFINT}$	Internal reference voltage startup time				refer to *Table 42*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} or V_{DDA} must be tied to ground.
3. Guaranteed by design, not tested in production.
4. Minimum sampling and conversion time is reached for maximum Rext = 0.5 kΩ.
5. Value obtained for continuous conversion on fast channel.
6. The time between 2 conversions, or between ADC ON and the first conversion must be lower than t_{IDLE}.
7. The t_{IDLE} maximum value is ∞ on the “Z” revision code of the device.

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In the following three tables, data is guaranteed by characterization result, not tested in production.

Table 44. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
DNL	Differential non linearity	f_{ADC} = 16 MHz	1	1.6	LSB
		f_{ADC} = 8 MHz	1	1.6	
		f_{ADC} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC} = 16 MHz	1.2	2	
		f_{ADC} = 8 MHz	1.2	1.8	
		f_{ADC} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC} = 16 MHz	2.2	3.0	
		f_{ADC} = 8 MHz	1.8	2.5	
		f_{ADC} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC} = 16 MHz	1.5	2	LSB
		f_{ADC} = 8 MHz	1	1.5	
		f_{ADC} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC} = 16 MHz	1	1.5	
		f_{ADC} = 8 MHz			
		f_{ADC} = 4 MHz			

Table 45. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	LSB
TUE	Total unadjusted error	2	4	LSB
Offset	Offset error	1	2	LSB
Gain	Gain error	1.5	3	LSB

Table 46. ADC1 accuracy with V_{DDA} = V_{REF+} = 1.8 V to 2.4 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	LSB
TUE	Total unadjusted error	3	5	LSB
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

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Figure 33. ADC1 accuracy characteristics

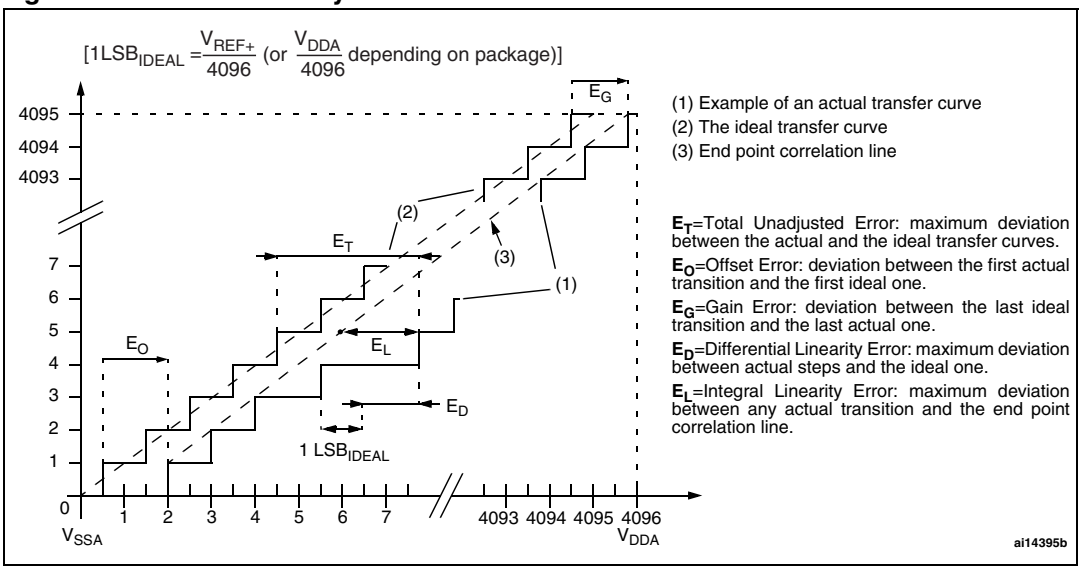
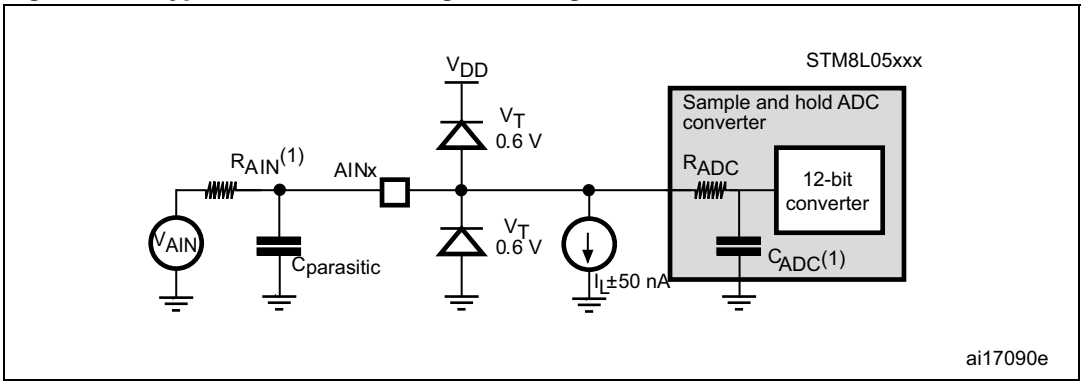


Figure 34. Typical connection diagram using the ADC



1. Refer to *Table 43* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

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Figure 35. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

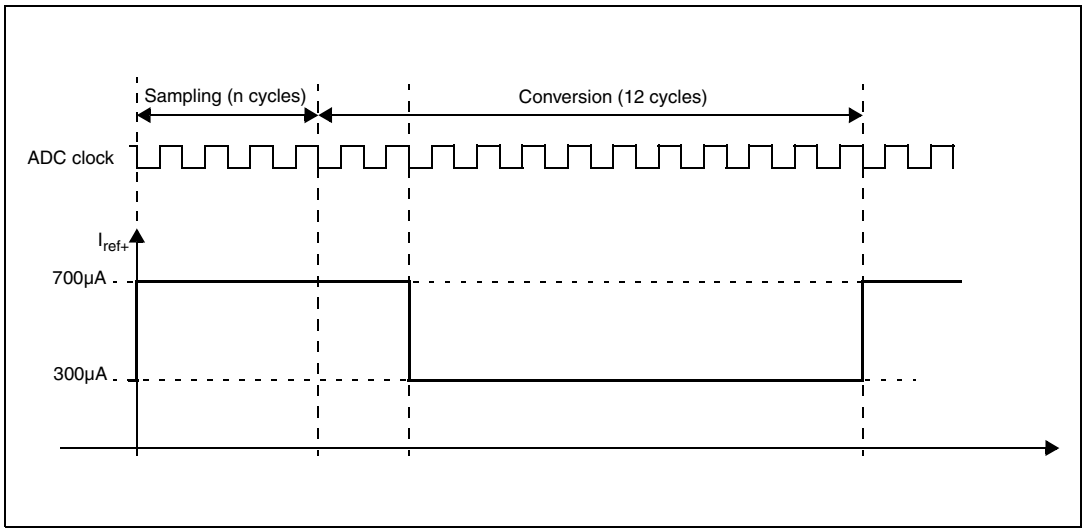


Table 47. R_{AIN} max for f_{ADC} = 16 MHz(1)

Ts (cycles)	Ts (µs)	R_{AIN} max (kohm)			
		Slow channels		Fast channels	
		2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.3 V	1.8 V < V_{DDA} < 2.4 V
4	0.25	Not allowed	Not allowed	0.7	Not allowed
9	0.5625	0.8	Not allowed	2.0	1.0
16	1	2.0	0.8	4.0	3.0
24	1.5	3.0	1.8	6.0	4.5
48	3	6.8	4.0	15.0	10.0
96	6	15.0	10.0	30.0	20.0
192	12	32.0	25.0	50.0	40.0
384	24	50.0	50.0	50.0	50.0

1. Guaranteed by design, not tested in production.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 36* or *Figure 37*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

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Figure 36. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

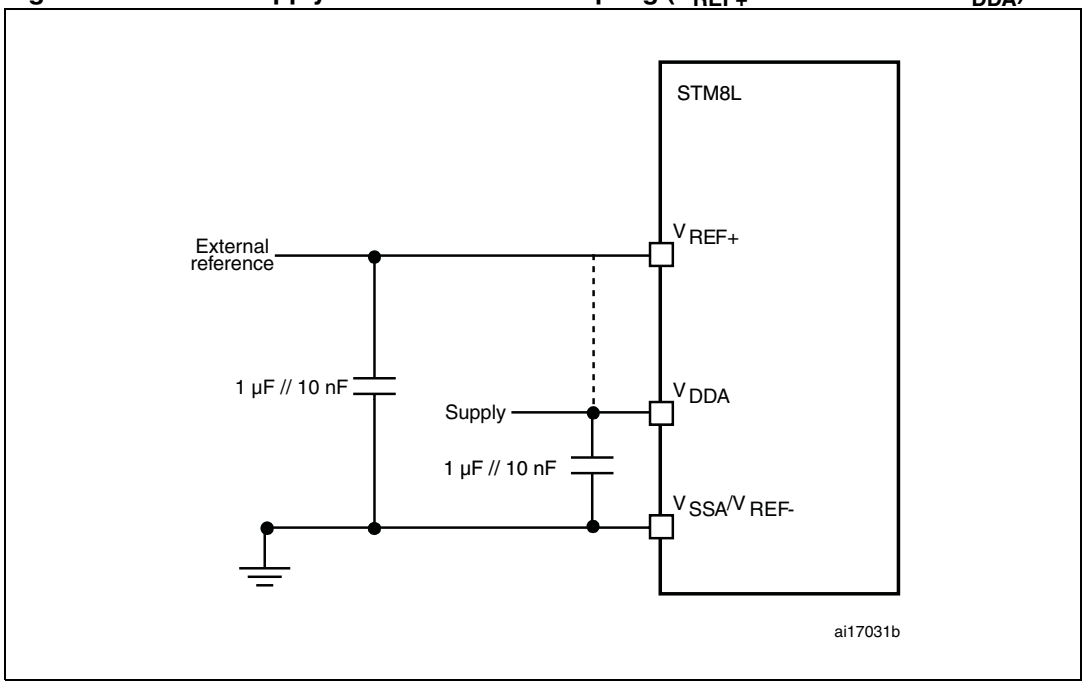
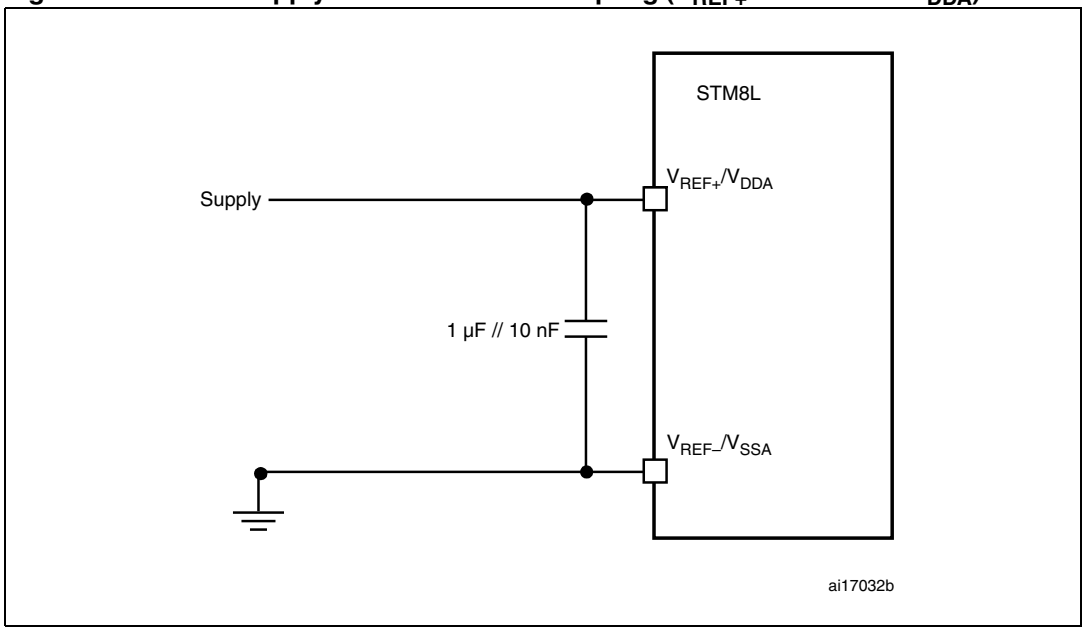


Figure 37. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



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8.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 48. EMS data

Symbol	Parameter	Conditions		Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU}= 16 MHz, conforms to IEC 61000		3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU} = 16 MHz, conforms to IEC 61000	Using HSI	4A
			Using HSE	2B

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC61967-2 which specifies the board and the loading of each pin.

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Table 49. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. 16 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP32 conforming to IEC61967-2	0.1 MHz to 30 MHz	-3	dBµV
			30 MHz to 130 MHz	9	
			130 MHz to 1 GHz	4	
			SAE EMI Level	2	-

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/A115A standard.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		500	

1. Data based on characterization results, not tested in production.

Static latch-up

- **LU**: 3 complementary static tests are required on 6 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 51. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

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9 Package characteristics

9.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

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9.2 Package mechanical data

9.2.1 20-lead thin shrink small package (TSSOP20)

Figure 38. TSSOP20 20-lead thin shrink small package outline

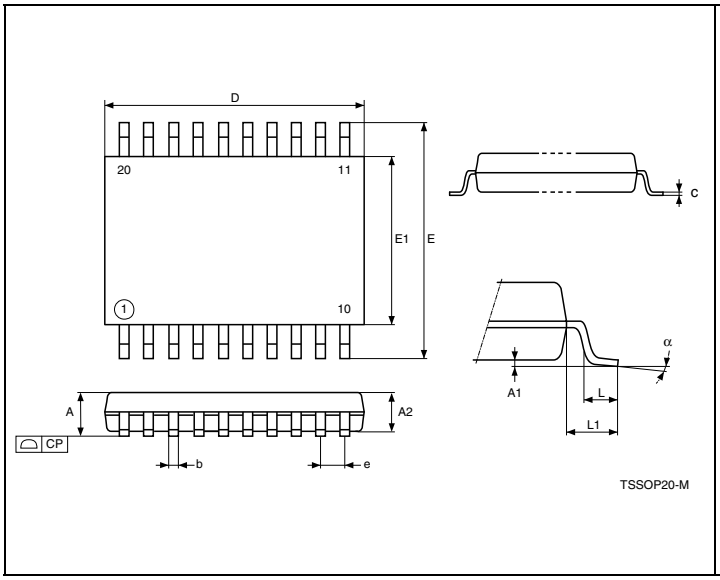
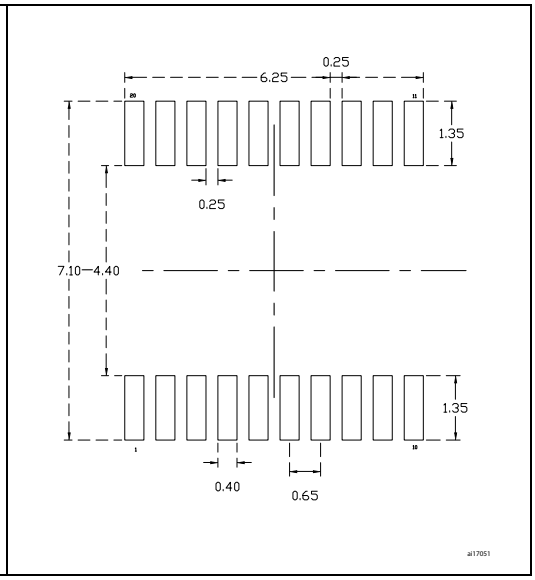


Figure 39. TSSOP20 recommended footprint



1. Drawing is not to scale
2. Dimensions are in millimeters

Table 52. TSSOP20 20-lead thin shrink small package, mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.0472
A1	0.05		0.15	0.0020		0.0059
A2	0.8	1	1.05	0.0315	0.0394	0.0413
b	0.19		0.3	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.2520	0.2559	0.2598
E	6.2	6.4	6.6	0.2441	0.252	0.2598
E1	4.3	4.4	4.5	0.1693	0.1732	0.1772
e	-	0.65	-		0.0256	-
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

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9.3 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 15: General operating conditions on page 48*.

The maximum chip-junction temperature, T_{Jmax}, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 53. Thermal characteristics(1)

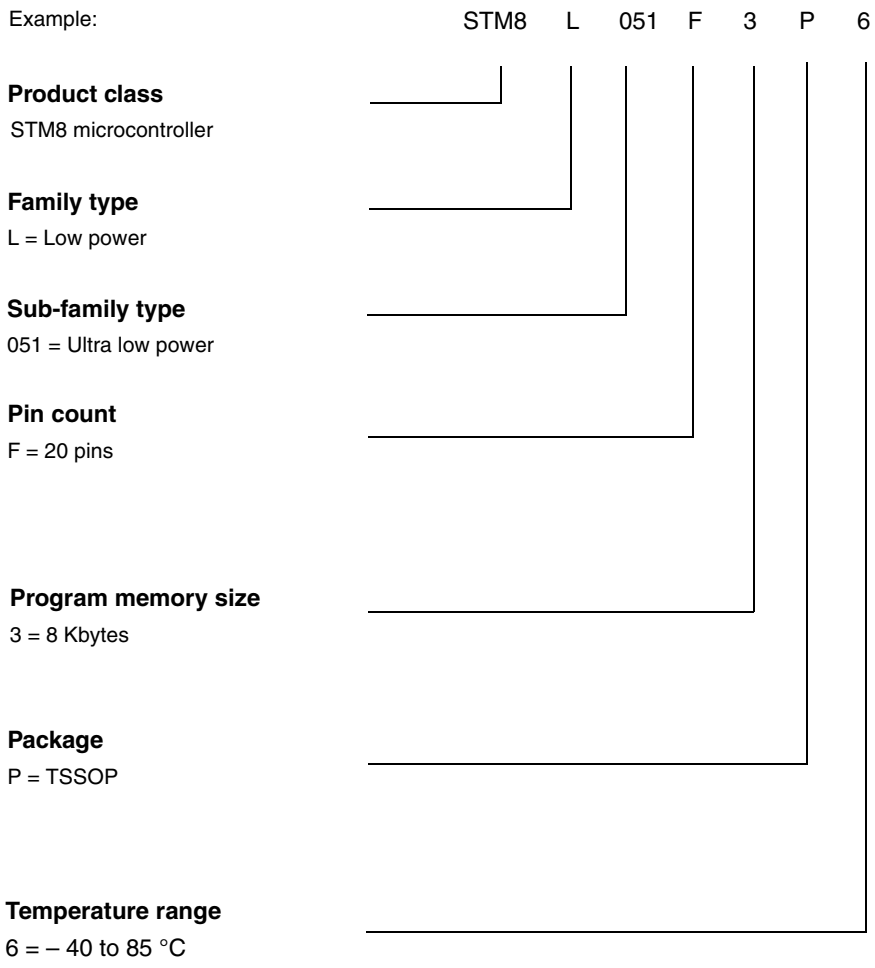
Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TSSOP20	110	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

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10 Device ordering information

Figure 40. Low density value line STM8L051F3 ordering information scheme



For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please contact the ST sales office nearest to you.

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11 Revision history

Table 54. Document revision history

Date	Revision	Changes
01-Aug-2012	1	Initial release.

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