STM32WL55xx STM32WL54xx

Multiprotocol LPWAN dual core 32-bit Arm® Cortex®-M4/M0+ LoRa®, (G)FSK, (G)MSK, BPSK, up to 256KB flash, 64KB SRAM

Datasheet - production data

Features

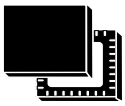
Includes ST state-of-the-art patented technology

Radio

- Frequency range: 150 MHz to 960 MHz
- Modulation: LoRa®, (G)FSK, (G)MSK and BPSK
- RX sensitivity: –123 dBm for 2-FSK (at 1.2 Kbit/s), –148 dBm for LoRa® (at 10.4 kHz, spreading factor 12)
- Transmitter high output power, programmable up to +22 dBm
- Transmitter low output power, programmable up to +15 dBm
- Available integrated passive device (IPD) companion chips for optimized matching, filtering and balun, all in one very compact solution covering each package and each main use cases (22 dBm @ 915 MHz, 14 dBm @ 868 MHz, 17 dBm @ 490 MHz)
- Compliant with the following radio frequency regulations such as ETSI EN 300 220, EN 300 113, EN 301 166, FCC CFR 47 Part 15, 24, 90, and the Japanese ARIB STD-T30, T-67, T-108
- Compatible with standardized or proprietary protocols such as LoRaWAN®, Sigfox™, W-MBus and more (fully open wireless system-on-chip)

Ultra-low-power platform

- 1.8 V to 3.6 V power supply
- –40 °C to +105 °C temperature range
- Shutdown mode: 31 nA (V_{DD} = 3 V)
- Standby (+ RTC) mode: 360 nA (V_{DD} = 3 V)
- Stop2 (+ RTC) mode: 1.07 µA (V_{DD} = 3 V)



UFQFPN48
(7 x 7 mm)



UFBGA73
(5 x 5 mm)

- Active-mode MCU: < 72 µA/MHz (CoreMark®)
- Active-mode RX: 4.82 mA
- Active-mode TX: 15 mA at 10 dBm and 87 mA at 20 dBm (LoRa® 125 kHz)

Core

- 32-bit Arm® Cortex®-M4 CPU
  - Adaptive real-time accelerator (ART Accelerator) allowing 0-wait-state execution from flash memory, frequency up to 48 MHz, MPU and DSP instructions
  - 1.25 DMIPS/MHz (Dhrystone 2.1)
- **32-bit Arm®Cortex®-M0+ CPU**
  - Frequency up to 48 MHz, MPU
  - 0.95 DMIPS/MHz (Dhrystone 2.1)

Security and identification

- Hardware encryption AES 256-bit
- True random number generator (RNG)
- Sector protection against read/write operations (PCROP, RDP, WRP)
- CRC calculation unit
- Unique device identifier (64-bit UID compliant with IEEE 802-2001 standard)
- 96-bit unique die identifier
- Hardware public key accelerator (PKA)
- Key management services
- Secure sub-GHz MAC layer
- Secure firmware update (SFU)
- Secure firmware install (SFI)

This is information on a product in full production. www.st.com

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Supply and reset management

- High-efficiency embedded SMPS step-down converter
- SMPS to LDO smart switch
- Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
- Ultra-low-power POR/PDR
- Programmable voltage detector (PVD)
- V_{BAT} mode with RTC and 20x32-bit backup registers

Clock sources

- 32 MHz crystal oscillator
- TCXO support: programmable supply voltage
- 32 kHz oscillator for RTC with calibration
- High-speed internal 16 MHz factory trimmed RC (± 1 %)
- Internal low-power 32 kHz RC
- Internal multi-speed low-power 100 kHz to 48 MHz RC
- PLL for CPU, ADC and audio clocks

Memories

- 256-Kbyte flash memory
- 64-Kbyte RAM
- 20x32-bit backup register
- Bootloader supporting USART and SPI interfaces
- OTA (over-the-air) firmware update capable
- Sector protection against read/write operations

Rich analog peripherals (down to 1.62 V)

- 12-bit ADC 2.5 Msps, up to 16 bits with hardware oversampling, conversion range up to 3.6 V
- 12-bit DAC, low-power sample-and-hold
- 2x ultra-low-power comparators

System peripherals

- Mailbox and semaphores for communication between Cortex®-M4 and Cortex®-M0+ firmware

Controllers

- 2x DMA controller (7 channels each) supporting ADC, DAC, SPI, I2C, LPUART, USART, AES and timers
- 2x USART (ISO 7816, IrDA, SPI)
- 1x LPUART (low-power)
- 2x SPI 16 Mbit/s (1 over 2 supporting I2S)
- 3x I2C (SMBus/PMBus®)
- 2x 16-bit 1-channel timer
- 1x 16-bit 4-channel timer (supporting motor control)
- 1x 32-bit 4-channel timer
- 3x 16-bit ultra-low-power timer
- 1x RTC with 32-bit sub-second wakeup counter
- 1x independent SysTick
- 1x independent watchdog
- 1x window watchdog

Up to 43 I/Os, most 5 V-tolerant

Development support

- Serial-wire debug (SWD), JTAG
- Dual CPU cross trigger capabilities

All packages ECOPACK2 compliant

Table 1. Device summary

Reference	Part number
STM32WL55xx	STM32WL55CC, STM32WL55JC
STM32WL54xx	STM32WL54CC, STM32WL54JC

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1 Introduction

This document provides information on the STM32WL55/54xx microcontrollers.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32WL55/54xx errata sheet (ES0500), available on the STMicroelectronics website www.st.com.

For information on the Arm®(a) Cortex®-M4 and Cortex®-M0+ cores, refer respectively to the Cortex®-M4 Technical Reference Manual and to the Cortex®-M0+ Technical Reference Manual available from the www.arm.com website.

For information on LoRa® modulation, refer to the Semtech website (https://www.semtech.com/technology/lora).

2 Description

The STM32WL55/54xx long-range wireless and ultra-low-power devices embed a powerful and ultra-low-power LPWAN-compliant radio solution, enabling the following modulations: LoRa®, (G)FSK, (G)MSK, and BPSK.

The LoRa® modulation is available in STM32WLx5xx only.

These devices are designed to be extremely low-power and are based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 48 MHz. This core implements a full set of DSP instructions. It is complemented by an Arm® Cortex®-M0+ microcontroller. Both cores implement an independent memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (256-Kbyte flash memory, 64-Kbyte SRAM), and an extensive range of enhanced I/Os and peripherals.

The devices also embed several protection mechanisms for embedded flash memory and SRAM: readout protection, write protection and proprietary code readout protection.

In addition, the STM32WL55/54xx devices support the following secure services running on Arm® Cortex-M0+: unique boot entry capable, secure sub-GHz MAC layer, secure firmware update, secure firmware install and storage and management of secure keys.

These devices offer a 12-bit ADC, a 12-bit DAC low-power sample-and-hold, two ultra-low-power comparators associated with a high-accuracy reference voltage generator.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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The devices embed a low-power RTC with a 32-bit sub-second wakeup counter, one 16-bit single-channel timer, two 16-bit four-channel timers (supporting motor control), one 32-bit four-channel timer and three 16-bit ultra-low-power timers.

These devices also embed two DMA controllers (7 channels each) allowing any transfer combination between memory (flash memory, SRAM1 and SRAM2) and peripheral, using the DMAMUX1 for flexible DMA channel mapping.

The devices also feature the following standard and advanced communication interfaces: inter-processor communication controller (mailbox) and semaphores for communication between the two Arm® Cortex®-M cores, two USARTs (supporting LIN, smartcard, IrDA, modem control and ISO7816), one low-power UART (LPUART), three I2Cs (SMBus/PMBus), two SPIs (up to 16 MHz, one supporting I^2S).

The operating temperature/voltage ranges are –40 °C to +105 °C (+85 °C with radio) from a 1.8 V to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The devices integrate a high-efficiency SMPS step-down converter and independent power supplies for ADC, DAC and comparator analog inputs.

A V_{BAT} dedicated supply allows the LSE 32.768 kHz oscillator, the RTC and the backup registers to be backed up. The devices can maintain these functions even if the main V_{DD} is not present, through a CR2032-like battery, a supercap or a small rechargeable battery.

Table 2. Main features and peripheral count

Feature		STM32WL55Cx STM32WL54Cx	STM32WL55Jx STM32WL54Jx
CPU		Arm Cortex-M4 and Cortex-M0	
Maximum CPU frequency (MHz)		48	
Flash memory density (Kbytes)		256	
SRAM density (Kbytes)	SRAM1	32	
	SRAM2	32	
Radio	LoRa	Available on STM32WL55xx devices. Not available on STM32WL54xx devices	
	(G)FSK	Yes	
	(G)MSK Tx		
	BPSK Tx		
Radio PA	Low output power (up to 15 dBm)	Yes	
	High output power (up to 22 dBm)		
Timer	General purpose	4	
	Low-power	3	
	SysTick	1	

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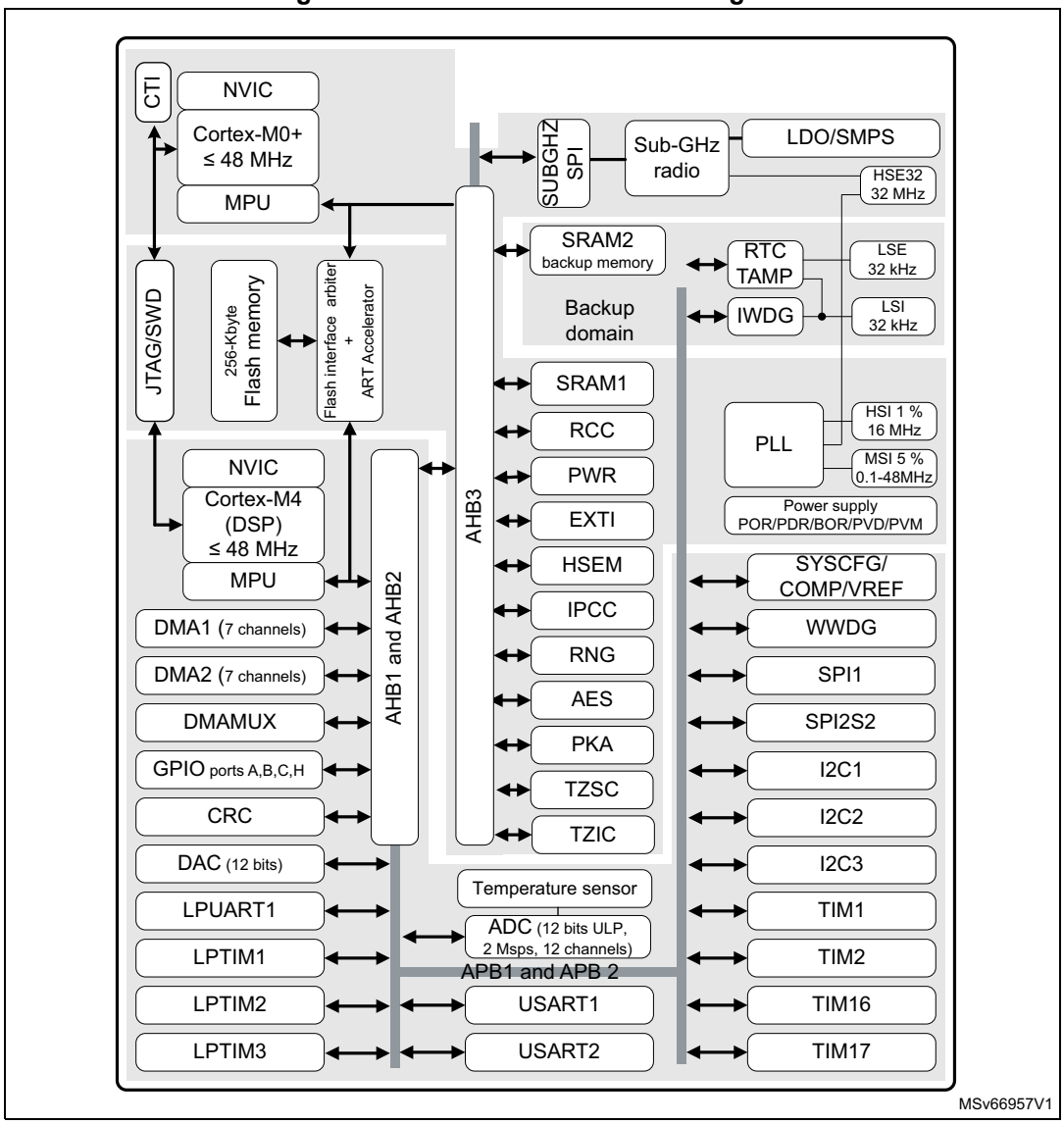
Table 2. Main features and peripheral count (continued)

Feature		STM32WL55Cx STM32WL54Cx	STM32WL55Jx STM32WL54Jx
Communication interface	SPI/I^2S	2 (1 supporting I^2S)	
	I^2C	3	
	USART	2	
	LPUART	1	
Watchdog	Independent	1	
	Window	1	
RTC (with wakeup counter)		1	
DMA (7 channels)		2	
Mailbox and semaphores		1	
Security	AES 256 bits	1	
	RNG	1	
	PKA	1	
	PCROP, RDP, WRP	1	
	CRC	1	
	64-bit UID compliant with IEEE 802-2001 standard	1	
	96-bit die ID	1	
	Storage and management of secure keys	1	
	Secure sub-GHz MAC layer	1	
	Secure firmware update	1	
	Secure firmware install	1	
Tamper pins		3	
Wakeup pins		3	
GPIOs		29	43
ADC (number of channels, ext + int)		1 (9 + 4)	1 (12 + 4)
DAC (number of channels)		1 (1)	
Internal VREFBUF		No	Yes
Analog comparator		2	
Operating voltage		1.8 to 3.6 V	
Ambient operating temperature		–40 °C to +105 °C / –40 °C to +85 °C (with radio)(1)	
Junction temperature		–40 °C to +125 °C / –40 °C to +105 °C (with radio)	
Package		UFQFPN48 (7x7 mm)	UFBGA73 (5x5 mm)

1. Devices with suffix 6 operate up to 85 °C. Devices with suffix 7 can operate up to 105 °C except radio.

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Figure 1. STM32WL55/54xx block diagram



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3 Functional overview

3.1 Architecture

The devices embed a sub-GHz RF subsystem that interfaces with a generic microcontroller subsystem using an Arm Cortex-M4 (called CPU1) and an Arm Cortex-M0+ (called CPU2).

An RF low-layer stack is needed and is to be run on CPU1 or CPU2, whereas the host application code is preferably run on CPU1.

The RF subsystem communication is done through an internal SPI interface.

All secure code must be run by CPU2.

3.2 Arm Cortex-M cores

With its embedded Arm cores, the STM32WL55/54xx devices are compatible with all Arm tools and software.

Figure 1 shows the general block diagram of the STM32WL55/54xx devices.

Arm Cortex-M4

The Arm Cortex-M4 is a processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm Cortex-M4 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

This processor supports a set of DSP instructions that allow efficient signal processing and complex algorithm execution.

Arm Cortex-M0+

The Arm Cortex-M0+ is an entry-level processor for embedded systems. It has been developed to provide lowest power consumption in the Cortex-M family, while delivering good computation performance and response to interrupts.

The Arm Cortex-M0+ 32-bit RISC processor features good code-efficiency with ultra-low power consumption in the memory size usually associated with 8-bit and 16-bit devices.

3.3 Adaptive real-time memory accelerator (ART Accelerator)

The ART Accelerator is a memory accelerator that is optimized for STM32 industry-standard Arm Cortex-M4 processor. The ART Accelerator balances the inherent performance advantage of the Arm Cortex-M4 over flash memory technologies, that normally require the processor to wait for the flash memory at higher frequencies.

To release the processor near 60 DMIPS performance at 48 MHz, the ART Accelerator implements an instruction prefetch queue and branch cache, that increases the program execution speed from the 64-bit flash memory. Based on CoreMark benchmark, the

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performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from flash memory at a CPU frequency up to 48 MHz.

3.4 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU1 and CPU2 accesses to memory, to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to eight protected areas that can in turn be divided up into eight subareas. The protection area sizes are between 32 bytes and the whole 4 Gbytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.5 Memories

3.5.1 Embedded flash memory

The flash memory interface manages the accesses from CPU1 AHB ICode/DCode and CPU2 AHB Sbus to the flash memory. It implements the access, the erase and program flash memory operations, and the read and write protection.

The main features of the flash memory are listed below:

- Memory organization: 1 bank
  - main memory: up to 256 Kbytes
  - page size: 2 Kbytes
- 72-bit wide data read (64 bits plus 8 ECC bits)
- 72-bit wide data write (64 bits plus 8 ECC bits)
- Page erase and mass erase

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection. The flash memory cannot be read from or written to if either debug features are connected, boot in SRAM or bootloader is selected.
  - Level 2: chip readout protection. Debug features (JTAG and serial wire), boot in SRAM and bootloader selection are disabled (JTAG fuse). This selection can only be reverted by the secure CPU2.

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Table 3. Access status versus RDP level and execution mode

Area	RDP level	User execution			Debug, boot from SRAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	NA	NA	NA
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	NA	NA	NA
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No(1)	No(1)	NA	NA	NA
Backup registers	1	Yes	Yes	NA(2)	No	No	NA(2)
	2	Yes	Yes	NA	NA	NA	NA
SRAM2	1	Yes	Yes	Yes(2)	No	No	No(2)
	2	Yes	Yes	Yes	NA	NA	NA

1. The option byte can be modified by the sub-GHz radio.
2. Erased when RDP changes from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas can be selected, with 4-Kbyte granularity.
- Proprietary code readout protection (PCROP): two parts of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU1/2, as an instruction code, while all other accesses (DMA, debug and CPU1/2 data read, write and erase) are strictly prohibited. Two areas can be selected, with 2-Kbyte granularity. An additional option bit (PCROP_RDP) is used to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

A section of the flash memory can be secured for CPU2, and, in that case, cannot be accessed by CPU1.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection
- address of the ECC fail can be read in the FLASH_ECCR register

The embedded flash memory is shared between CPU1 and CPU2 on a time sharing basis. A dedicated hardware mechanism allows both CPUs to suspend write/erase operations.

3.5.2 Embedded SRAM

The devices feature up to 64 Kbytes of embedded SRAM, split in two blocks:

- SRAM1: up to 32 Kbytes mapped at address 0x2000 0000
- SRAM2: up to 32 Kbytes located at address 0x2000 8000 (contiguous to SRAM1 in case of SRAM1 32-Kbyte configuration), also mirrored at 0x1000 0000, with hardware parity check (this SRAM can be retained in Standby mode)

The SRAMs can be accessed in read/write with 0 wait states for all CPU1/2 clock speeds.

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3.6 Security memory management

The devices contain many security blocks both for the sub-GHz MAC layer and the Host application, such as:

- securable RNG
- customer keys storage
- secure flash memory partition for CPU2 only access
- secure SRAM partition, that can be accessed only by CPU2
- securable sub-GHz radio sub-system
- securable DMA channels
- securable AES: 128-and 256-bit AES, supporting ECB, CBC, CTR, GCM, GMAC and CCM chaining modes
- securable PKA:
  - modular arithmetic including exponentiation with maximum modulo size of 3136 bits
  - elliptic curves over prime field scalar multiplication, ECDSA signature, ECDSA verification with maximum modulo size of 521 bits
- cyclic redundancy check calculation unit (CRC)

3.7 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of the following boot options:

- Boot from user flash memory
- Boot from boot system memory (where embedded bootloader is located)
- Boot from embedded SRAM
- Boot from system memory (where the embedded SFI is located)

The bootloader makes possible to download code from USART or SPI.

If the boot selection uses the BOOT0 pin to boot from the main flash memory, but the first flash memory location is found empty, the flash empty check mechanism forces boot from the system memory (containing the embedded bootloader). Then, due to the bootloader activation, some of the GPIOs are reconfigured from the high-Z state. Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details concerning the bootloader and GPIOs configuration.

This feature can be disabled by configuring the option bytes (instead of BOOT0 pin) to force boot from the main flash memory (nSWBOOT0 = 0, nBOOT0 = 1).

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3.8 Global security controller (GTZC)

The GTZC includes the following sub-blocks:

- TZSC: security controller

  This sub-block defines the secure/privileged state of slave peripherals. It also controls the unprivileged area size for the watermark memory peripheral controller (MPCWM).
- TZIC: security illegal access controller

  This sub-block gathers all illegal access events in the system and generates a secure interrupt towards the secure CPU2 NVIC.

These sub-blocks are used to configure the system security and privilege such as:

- on-chip flash memory and RAM with programmable privileged protection on both secure and non-secure memory areas
- AHB and APB peripherals with programmable security and/or privileged access

3.9 Sub-GHz radio

3.9.1 Sub-GHz radio introduction

The sub-GHz radio is an ultra-low-power sub-GHz radio operating in the 150 - 960 MHz ISM band. LoRa and (G)FSK modulations in transmit and receive, and BPSK/(G)MSK in transmit only, allow an optimal trade-off between range, data rate and power consumption. This sub-GHz radio is compliant with the LoRaWAN® specification v1.0 and radio regulations such as ETSI EN 300 220, EN 300 113, EN 301 166, FCC CFR 47 part 15, 24, 90, 101 and the ARIB STD-T30, T-67, T-108.

The sub-GHz radio consists of:

- an analog front-end transceiver, capable of outputting up to + 15 dBm maximum power on its RFO_LP pin and up to + 22 dBm maximum power on RFO_HP pin
- a digital modem bank providing the following modulation schemes:
  - LoRa Rx/Tx with bandwidth (BW) from 7.8 - 500 kHz, spreading factor (SF) 5 - 12, bit rate (BR) from 0.013 to 17.4 Kbit/s (real bitrate)
  - FSK and GFSK Rx/Tx with BR from 0.6 to 300 Kbit/s
  - (G)MSK Tx with BR from 0.1 to 10 Kbit/s
  - BPSK Tx only with bitrate for 100 and 600 bit/s
- a digital control including all data processing and sub-GHz radio configuration control
- a high-speed clock generation

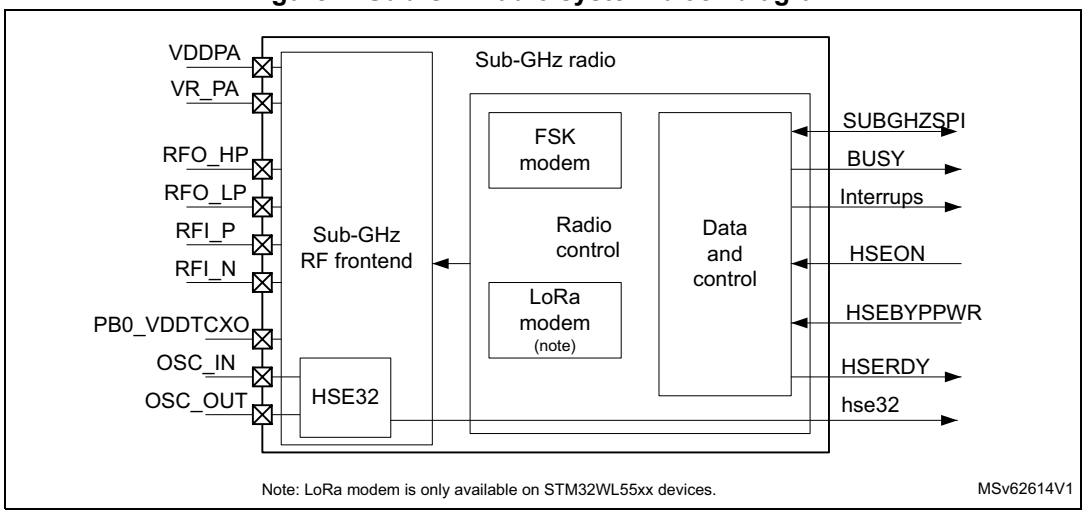
3.9.2 Sub-GHz radio general description

The sub-GHz radio provides an internal processing unit to handle communication with the system CPU. Communication is handled by commands sent over the SPI interface, and a set of interrupts is used to signal events. BUSY information signals operation activity and is used to indicate when the sub-GHz radio commands cannot be received.

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The block diagram of the sub-GHz radio system is shown in the figure below.

Figure 2. Sub-GHz radio system block diagram



3.9.3 Transmitter

The transmit chain comprises the modulated output from the modem, that directly modulates the RF-PLL. An optional pre-filtering of the bit stream can be enabled to reduce the power in the adjacent channel also dependent on the selected modulation scheme. The modulated signal from the RF-PLL directly drives the high output power PA (HP PA) or low output power PA (LP PA). The transmitted packet payload size depends on the modulation scheme.

Transmitter high output power

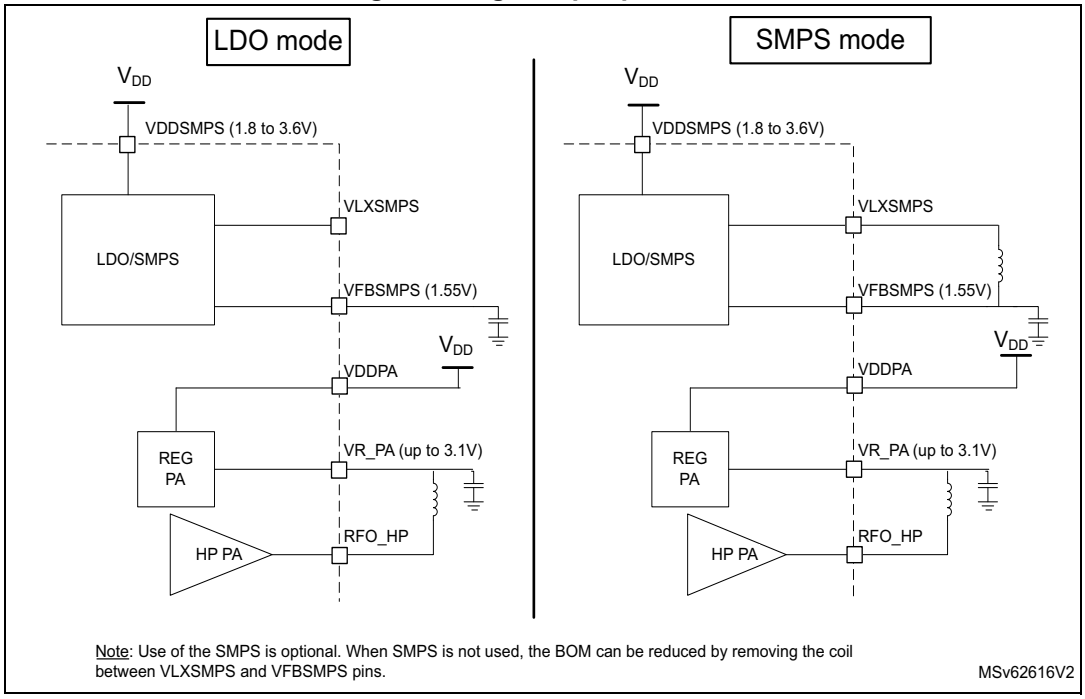
Transmit high output power up to + 22 dBm, is supported through the RFO_HP RF pin.

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For this, the REG PA must be supplied directly from V_{DD} on VDDSMPS pin, as shown in the figure below.

The output power range is programmable in 32 steps of ~ 1 dB. The power amplifier ramping timing is also programmable.This allows adaptation to meet radio regulation requirements.

Figure 3. High output power PA



The table below gives the maximum transmit output power versus the V_{DDPA} supply level.

Table 4. Sub-GHz radio transmit high output power

V_{DDPA} supply (V)	Transmit output power (dBm)
3.3	+ 22
2.7	+ 20
2.4	+ 19
1.8	+ 16

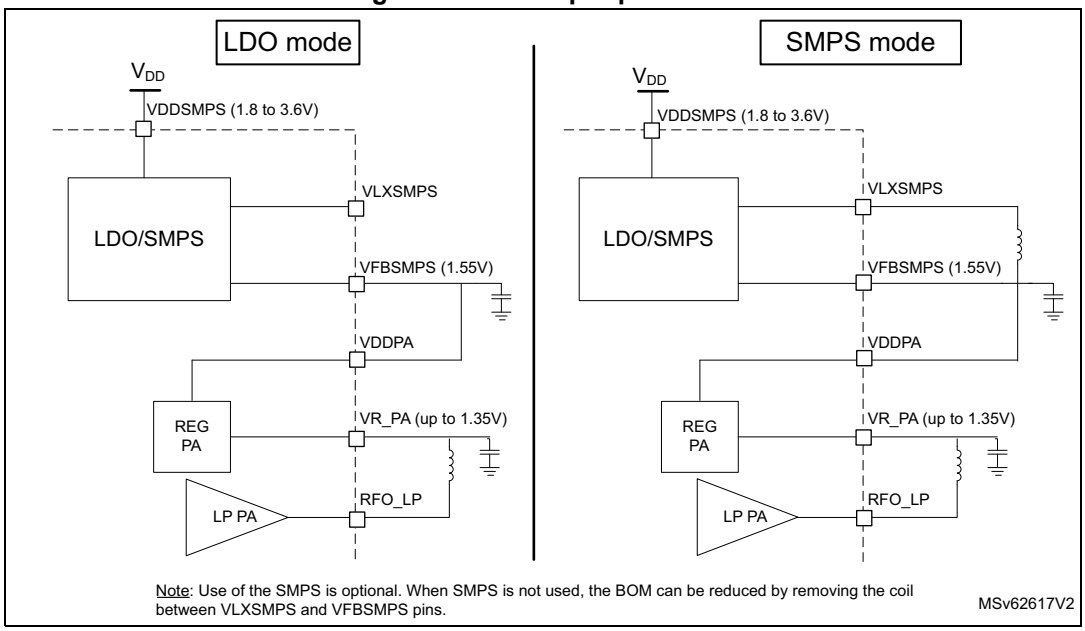
Transmitter low output power

The transmit low output power up to + 15 dBm on full V_{DD} range (1.8 to 3.6 V), is supported through the RFO_LP RF pin. For this, the REG PA must be supplied from the regulated V_{FBSMPS} supply at 1.55 V, as shown in the figure below.

The output power range is programmable in 32 steps of ~1 dB. The power amplifier ramping timing is also programmable.This allows adaptation to meet radio regulation requirements.

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Figure 4. Low output power PA



3.9.4 Receiver

The receive chain comprises a differential low-noise amplifier (LNA), a down-converter to low-IF by mixer operation in quadrature configuration. The I and Q signals are low pass filtered and a ΣΔ ADC converts them into the digital domain. In the digital modem, the signals are decimated, further down converted and channel filtered. The demodulation is done according to the selected modulation scheme.

The down mixing to low-IF is done by mixing the receive signal with the local RF-PLL located in the negative frequency, where $-f_{lo} = -f_{rf} + -f_{if}$. (where f_{lo} is the local RF-PLL frequency, f_{rf} is the received signal and f_{if} is the intermediate frequency). The wanted signal is located at $f_{rf} = f_{lo} + f_{if}$.

The receiver features automatic I and Q calibration, that improves image rejection. The calibration is done automatically at startup before using the receiver, and can be requested by command.

The receiver supports LoRa, (G)MSK and (G)FSK modulations. The received packet payload size depends on the modulation scheme.

3.9.5 RF-PLL

The RF-PLL is used as the frequency synthesizer for the generation of the local oscillator frequency (f_{lo}) for both transmit and receive chains. The RF-PLL uses auto calibration and uses the 32 MHz HSE32 reference. The sub-GHz radio covers all continuous frequencies in the range between 150 to 960 MHz.

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3.9.6 Intermediate frequencies

The sub-GHz radio receiver operates mostly in low-IF configuration, except for specific high-bandwidth settings.

Table 5. FSK mode intermediate frequencies

Setting name	Bandwidth (kHz)	f_{if} (kHz)
RX_BW_467	467.0	250
RX_BW_234	234.3	
RX_BW_117	117.3	
RX_BW_58	58.6	
RX_BW_29	29.3	
RX_BW_14	14.6	
RX_BW_7	7.3	
RX_BW_373	373.6	200
RX_BW_187	187.2	
RX_BW_93	93.8	
RX_BW_46	46.9	
RX_BW_23	23.4	
RX_BW_11	11.7	
RX_BW_5	5.8	
RX_BW_312	312.0	167
RX_BW_156	156.2	
RX_BW_78	78.2	
RX_BW_39	39.0	
RX_BW_19	19.5	
RX_BW_9	9.7	
RX_BW_4	4.8	

Table 6. LoRa mode intermediate frequencies

Setting name	Bandwidth (kHz)	f_{if} (kHz)
LORA_BW_500	500	0
LORA_BW_250	250	250
LORA_BW_125	125	
LORA_BW_62	62.5	
LORA_BW_41	41.67	167
LORA_BW_31	31.25	250
LORA_BW_20	20.83	167

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Table 6. LoRa mode intermediate frequencies (continued)

Setting name	Bandwidth (kHz)	f_{if} (kHz)
LORA_BW_15	15.63	250
LORA_BW_10	10.42	167
LORA_BW_7	7.81	250

3.9.7 IPDs for STM32WL and reference designs

For reference designs covering different packages and performance, cost and complexity trade-offs, refer to the data brief *STM32WL reference designs* (DB4597).

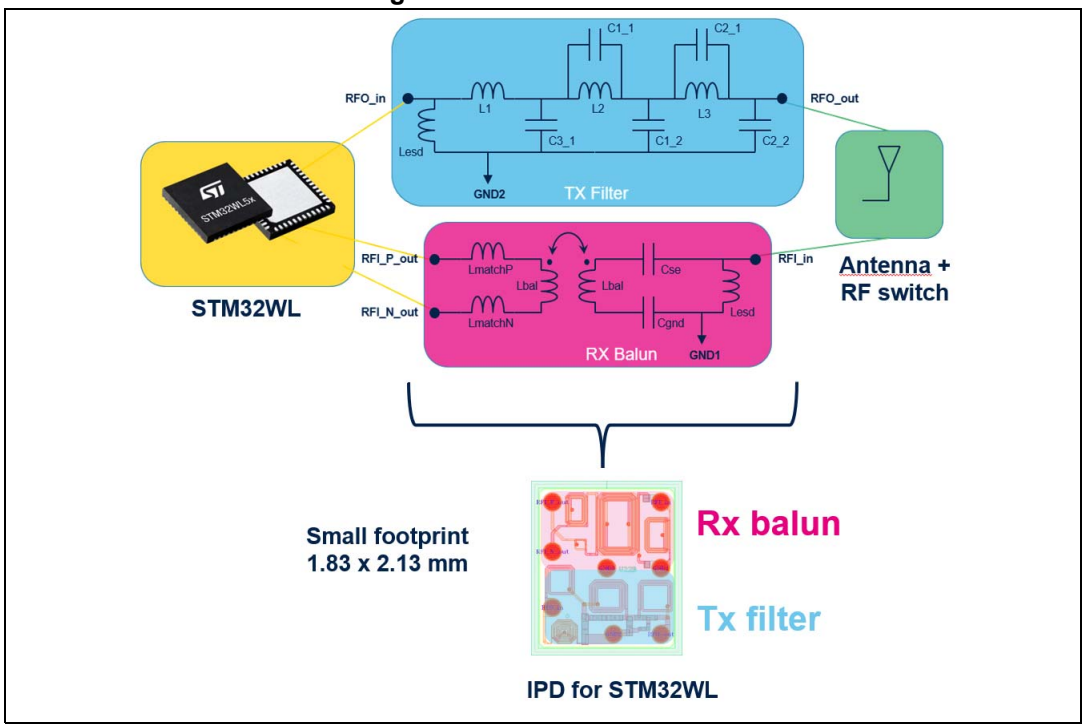
The table below lists the IPD variants used to optimize main use cases in term of maximum output power, frequency range, and PCB characteristics of the target board.

Table 7. IPDs for STM32WL

IPD	Power Frequency	PCB # of layers	MCU package	STM32WL part number
BALFHB-WL-01D3	22 dBm 915 MHz	4	UFBGA73	STM32WL54JC, STM32WL55JC
BALFHB-WL-02D3		4	UFQFPN48	STM32WL54CC, STM32WL55CC
BALFHB-WL-03D3		2	UFQFPN48	STM32WL54CC, STM32WL55CC
BALFHB-WL-04D3	15 dBm 868_915 MHz	4	UFBGA73	STM32WL54JC, STM32WL55JC
BALFHB-WL-05D3		4	UFQFPN48	STM32WL54CC, STM32WL55CC
BALFHB-WL-06D3		2	UFQFPN48	STM32WL54CC, STM32WL55CC
BALFLB-WL-07D3	17 dBm 490 MHz	4	UFBGA73	STM32WL54JC, STM32WL55JC
BALFLB-WL-08D3		4	UFQFPN48	STM32WL54CC, STM32WL55CC
BALFLB-WL-09D3		2	UFQFPN48	STM32WL54CC, STM32WL55CC

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Figure 5. IPDs for STM32WL



3.10 Power supply management

The devices embed two different regulators: one LDO and one DC/DC (SMPS). The SMPS can be optionally switched-on by software to improve the power efficiency. As LDO and SMPS operate in parallel, the SMPS switch-on is transparent to the user and only the power efficiency is affected.

3.10.1 Power supply schemes

The devices require a V_{DD} operating voltage supply between 1.8 V and 3.6 V. Several independent supplies (V_{DDSMPS}, V_{FBSMPS}, V_{DDA}, V_{DDRF}) can be provided for specific peripherals:

- **V_{DD}** = 1.8 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the system analog blocks such as reset, power management, internal clocks and low-power regulator. It is provided externally through VDD pins.
- **V_{DDSMPS}** = 1.8 V to 3.6 V

  V_{DDSMPS} is the external power supply for the SMPS step-down converter. It is provided externally through VDDSMPS supply pin and must be connected to the same supply as V_{DD}.
- **V_{FBSMPS}** = 1.45 V to 1.62 V (1.55 V typical)

  V_{FBSMPS} is the external power supply for the main system regulator. It is provided externally through VFBSMPS pin and is supplied through the SMPS step-down

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converter.

- **V_{DDA}** = 0 V to 3.6 V (DAC minimum voltage is 1.71 V without buffer and 1.8 V with buffer. COMP and ADC minimum voltage is 1.62 V. VREFBUF minimum voltage is 2.4 V)

  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage (see power-up and power-down limitations below) and must preferably be connected to V_{DD} when these peripherals are not used.

- **V_{DDRF}** = 1.8 V to 3.6 V

  V_{DDRF} is an external power supply for the radio. It is provided externally through the VDDRF pin and must be connected to the same supply as V_{DD}.

- **$V_{DDRF1V5}$** = 1.45 V to 1.62 V

  $V_{DDRF1V5}$ is an external power supply for the radio. It is provided externally through the VDDRF1V5 pin and must be connected externally to VFBSMPS.

- **V_{BAT}** = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, TAMP, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

- **VREF-, VREF+**

  V_{REF+} is the input reference voltage for ADC and DAC. It is also the output of the internal voltage reference buffer when enabled.

  – When V_{DDA} < 2 V, V_{REF+} must be equal to V_{DDA}.

  – When V_{DDA} ≥ 2 V, V_{REF+} must be between 2 V and V_{DDA}.

  V_{REF+} can be grounded when ADC/DAC is not active. The internal voltage reference buffer supports the following output voltages, configured with VRS bit in the VREFBUF_CSR register:

  – V_{REF+} around 2.048 V: this requires V_{DDA} ≥ 2.4 V.

  – V_{REF+} around 2.5 V: this requires V_{DDA} ≥ 2.8 V.

During power up and power down, the following power sequence is required:

1. When V_{DD} < 1 V other power supplies (V_{DDA}) must remain below V_{DD} + 300 mV.

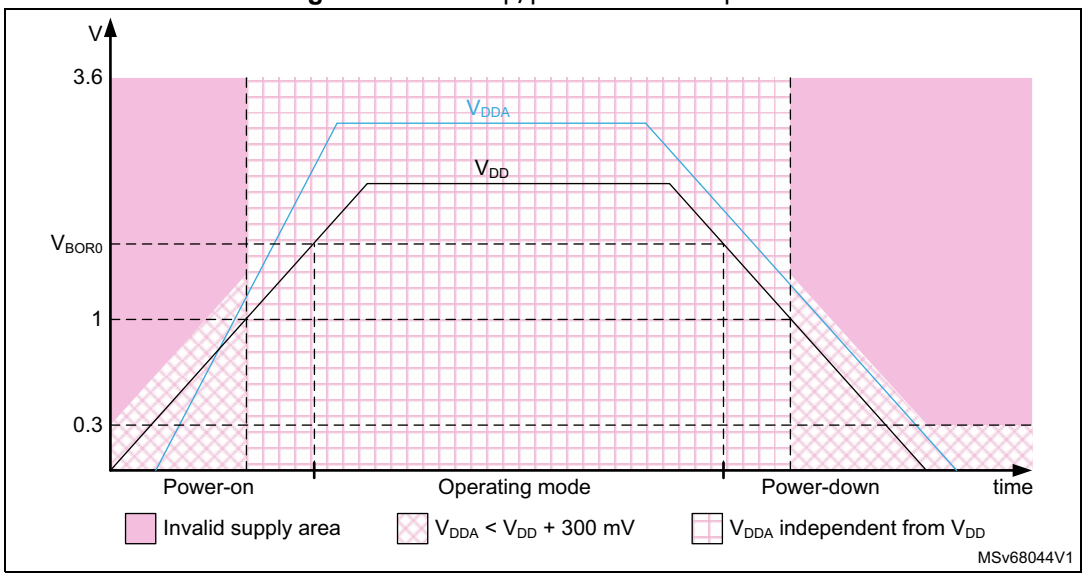
   During power down, V_{DD} can temporarily become lower then other supplies only if the energy provided to the device remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during this transient phase.

2. When V_{DD} > 1 V, all other power supplies (V_{DDA}) become independent.

An embedded linear voltage regulator is used to supply the internal digital power V_{CORE}. V_{CORE} is the power supply for digital peripherals, SRAM1 and SRAM2. The flash memory is supplied by V_{CORE} and V_{DD}. V_{CORE} is split in two parts: V_{DDO} part and an interruptible part V_{DDI}.

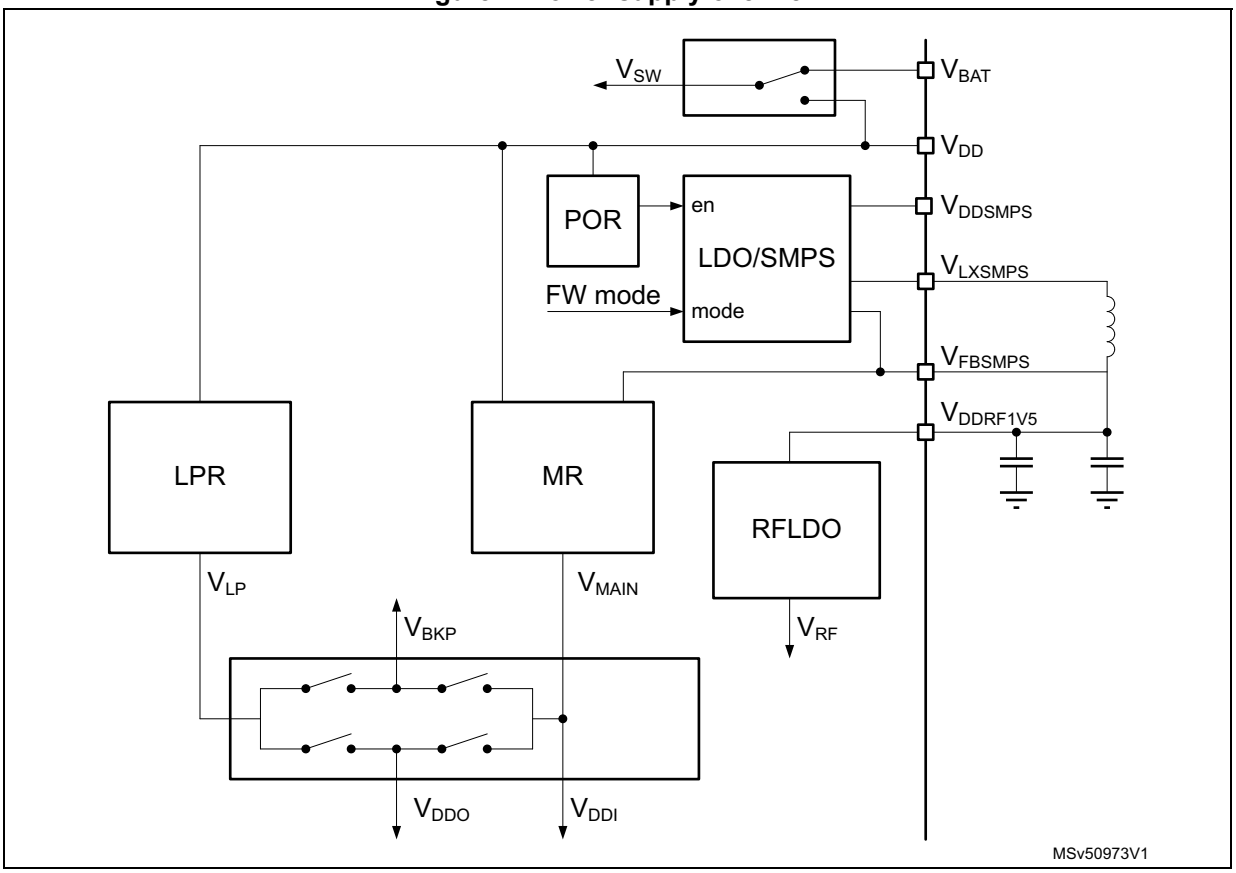
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Figure 6. Power-up/power-down sequence



Note: V_{DD}, V_{DDRF} and V_{DDSMPS} must be wired together, so they can follow the same voltage sequence.

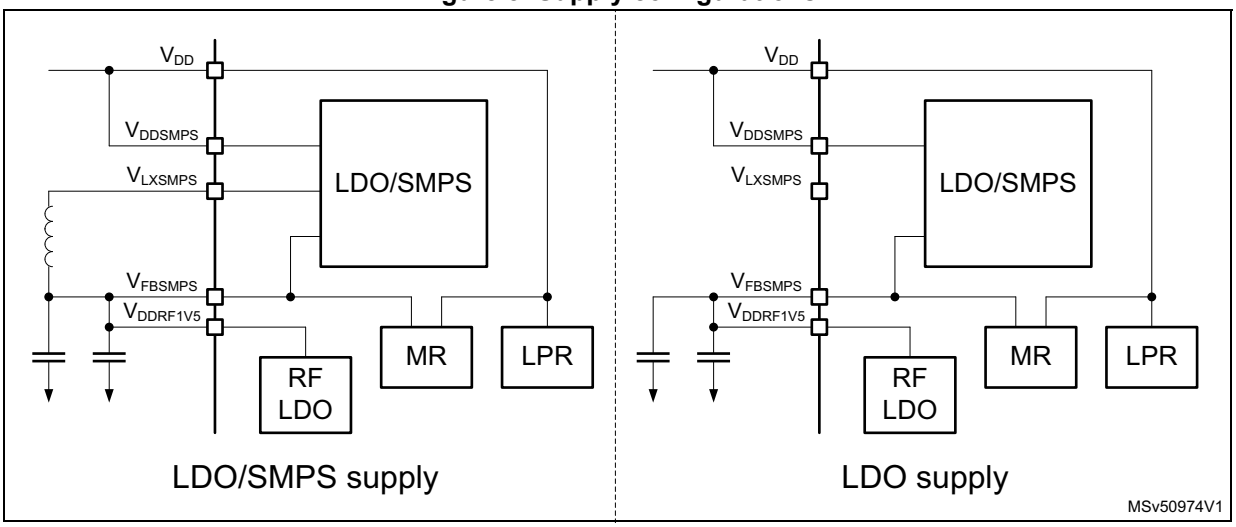
Figure 7. Power supply overview



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The different supply configurations are shown in the figure below.

Figure 8. Supply configurations



The LDO or SMPS step-down converter operating mode can be configured by one of the following:

- by the MCU using the SMPSEN setting in PWR control register 5 (PWR_CR5), that depends upon the MCU system operating mode (Run, Stop, Standby or Shutdown).
- by the sub-GHz radio using `SetRegulatorMode()` command and the sub-GHz radio operating mode (Sleep, Calibrate, Standby, Standby with HSE32 or Active).

After any POR and NRST reset, the LDO mode is selected. The SMPS selection has priority over LDO selection.

While the sub-GHz radio is in Standby with HSE32 or in Active mode, the supply mode is not altered until the sub-GHz radio enters Standby or Sleep mode. The sub-GHz radio activity may add a delay for entering the MCU software requested supply mode.

The LDO or SMPS supply mode can be checked with the SMPSRDY flag in power status register 2 (PWR_SR2).

Note: When the radio is active, the supply mode is not changed until after the radio activity is finished.

During Stop 1, Stop 2 and Standby modes, when the sub-GHz radio is not active, the LDO or SMPS step-down converter is switched off. When exiting low-power modes (except Shutdown), the SMPS step-down converter is set by hardware to the mode selected by the SMPSEN bit in PWR control register 5 (PWR_CR5). SMPSEN is retained in Stop and Standby modes.

Independently from the MCU software selected supply operating mode, the sub-GHz radio allows the supply mode selection while the sub-GHz radio is active (thanks to the sub-GHz radio *`SetRegulatorMode()`*command*)*.

The maximum load current delivered by the SMPS can be selected by the sub- GHz radio SUBGHZ_SMPSC2R register.

The inrush current of the LDO and SMPS step-down converter can be controlled via the sub- GHz radio SUBGHZ_PCR register. This information is retained in all but the sub-GHz radio Deep-sleep mode.

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The SMPS needs a clock to be functional. If for any reason this clock stops, the device may be destroyed. To avoid this situation, a clock detection is used to, in case of a clock failure, switch off the SMPS and enable the LDO. The SMPS clock detection is enabled by the sub-GHz radio SUBGHZ_SMPSC0R.CLKDE. By default, the SMPS clock detection is disabled and must be enabled before enabling the SMPS.

Danger: Before enabling the SMPS, the SMPS clock detection must be enabled in the sub-GHz radio SUBGHZ_SMPSC0R.CLKDE.

3.10.2 Power supply supervisor

The devices integrate a power-on reset/power-down reset, coupled with a Brownout reset (BOR) circuitry.

BOR0 level cannot be disabled. Other BOR levels can be enabled by user option. When enabled, BOR is active in all power modes except in Shutdown

Five BOR thresholds can be selected through option bytes.

During power-on, BOR keeps the device under reset until the supply voltage V_{DD} reaches the specified V_{BORx} threshold:

- When V_{DD} drops below the selected threshold, a device reset is generated.
- When V_{DD} is above the V_{BORx} upper limit, the device reset is released and the system can start.

The devices feature an embedded PVD (programmable voltage detector) that monitors the V_{DD} power supply and compares it with the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state.

The PVD is enabled by software and can be configured to monitor the V_{DD} supply level needed for the sub-GHz radio operation. For this, the PVD must select its lowest threshold, and the PVD and the wakeup must be enabled by the EWPVD bit in PWR_CR3 register. Only a voltage drop below the PVD level generates a wakeup event.

In addition, the devices embed a PVM (peripheral voltage monitor) that compares the independent supply voltage V_{DDA} with a fixed threshold to ensure that the peripheral is in its functional supply range.

Finally, a radio end-of-life monitor provides information on the V_{DD} supply when V_{DD} is too low to operate the sub-GHz radio. When reaching the EOL level, the software must stop all radio activity in a safe way.

3.10.3 Linear voltage regulator

Two embedded linear voltage regulators supply all the digital circuitries, except for the Standby circuitry and the Backup domain. The main regulator (MR) output voltage (V_{CORE}) can be programmed by software to two different power ranges (range 1 and range 2), to optimize the consumption depending on the system maximum operating frequency.

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The voltage regulators are always enabled after a reset. Depending on the application modes, the V_{CORE} supply is provided either by the main regulator or by the low-power regulator (LPR).

When MR is used, a dynamic voltage scaling is proposed to optimize power as follows:

- range 1: high-performance range

  The system clock frequency can be up to 48 MHz. The flash memory access time for read access is minimum. Write and erase operations are possible.
- range 2: low-power range

  The system clock frequency can be up to 16 MHz.The flash memory access time for a read access is increased as compared to range 1. Write and erase operations are possible.

Note: MR is supplied by V_{DD} during power-on or at wakeup from Stop1, Stop2, Standby or Shutdown mode. MR is powered by LDO/SMPS after these transition phases.

3.10.4 VBAT operation

The VBAT pin is used to power the device V_{BAT} domain (RTC, LSE and backup registers) from an external battery, an external super-capacitor, or from V_{DD} when no external battery nor an external super-capacitor are present. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal V_{BAT} battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied only from V_{BAT}, external interrupts and RTC alarm/events do not exit it from VBAT operation.

3.11 Low-power modes

The devices support several low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources.

By default, the microcontroller is in Run mode, range 1, after a system or a power-on reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**: CPU clock off, all peripherals including CPU core peripherals (among them NVIC, SysTick) can run and wake up the CPU when an interrupt or an event occurs.
- **Low-power run mode (LPRun)**: when the system clock frequency is reduced below 2 MHz. The code is executed from the SRAM or from the flash memory. The regulator is in low-power mode to minimize the operating current.
- **Low-power sleep mode (LPSleep)**: entered from the LPRun mode.
- **Stop 0 and Stop 1 modes**: the content of SRAM1, SRAM2 and of all registers is retained. All clocks in the V_{CORE} domain are stopped. PLL, MSI, HSI16 and HSE32 are disabled. LSI and LSE can be kept running.

  RTC can remain active (Stop mode with RTC, Stop mode without RTC). The sub-GHz radio may remain active independently from the CPUs.

  Some peripherals with the wakeup capability can enable HSI16 RC during the Stop

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mode to detect their wakeup condition.

Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption compared with Stop 2.

In Stop 0 mode, the main regulator remains on, resulting in the fastest wakeup time but with much higher consumption. The active peripherals and wakeup sources are the same as in Stop 1 mode that uses the low-power regulator.

The system clock, when exiting Stop 0 or Stop 1 mode, can be either MSI up to 48 MHz or HSI16, depending on the software configuration.

- **Stop 2 mode**: part of the V_{CORE} domain is powered off. Only SRAM1, SRAM2, CPUs and some peripherals preserve their contents (see *Table 8*).

  All clocks in the V_{CORE} domain are stopped. PLL, MSI, HSI16 and HSE32 are disabled. LSI and LSE can be kept running.

  RTC can remain active (Stop 2 mode with RTC, Stop 2 mode without RTC). The sub-GHz radio may also remain active independent from the CPUs.

  Some peripherals with the wakeup capability can enable HSI16 RC during the Stop 2 mode to detect their wakeup condition (see *Table 8*).

  The system clock when exiting from Stop 2 mode, can be either MSI up to 48 MHz or HSI16, depending on the software configuration.

- **Standby mode**: V_{CORE} domain is powered off. However, it is possible to preserve the SRAM2 content as detailed below:
  - Standby mode with SRAM2 retention when the RRS bit is set in the PWR control register 3 (PWR_CR3). In this case, SRAM2 is supplied by the low-power regulator.
  - Standby mode when the RRS bit is cleared in the PWR control register 3 (PWR_CR3). In this case the main regulator and the low-power regulator are powered off.

  All clocks in the V_{CORE} domain are stopped. PLL, MSI, HSI16 and HSE32 are disabled. LSI and LSE can be kept running.

  Th RTC can remain active (Standby mode with RTC, Standby mode without RTC). The sub-GHz radio and the PVD may also remain active when enabled independent from the CPUs. In Standby mode, the PVD selects its lowest level.

  The system clock, when exiting Standby modes, is MSI at 4 MHz.

- **Shutdown mode**: V_{CORE} domain is powered off. All clocks in the V_{CORE} domain are stopped. PLL, MSI, HSI16, LSI and HSE32 are disabled. LSE can be kept running. The system clock when exiting the Shutdown mode, is MSI at 4 MHz. In this mode, the supply voltage monitoring is disabled and the product behavior is not guaranteed in case of a power voltage drop.

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The table below summarizes the peripheral features over all available modes. Wakeup capability is detailed in gray cells.

Table 8. Functionalities depending on system operating mode(1)

Peripheral	Run	Sleep	LPRun	LPSleep	Stop 0		Stop 1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU1	Y	R	Y	R	R	-	R	-	R	-	-	-	-	-	-
CPU2	Y	R	Y	R	R	-	R	-	R	-	-	-	-	-	-
Sub-GHz radio system	O	O	O	O	O	O	O	O	O	O	O	O	-	-	-
Flash memory (256 Kbytes)	Y	O(2)	O(3)	O(2) (3)	R	-	R	-	R	-	R	-	R	-	R
Flash memory interface	Y	Y	Y	Y	R	-	R	-	R	-	-	-	-	-	-
SRAM1	Y	O(2)	Y	O(2)	R	-	R	-	R	-	-	-	-	-	-
SRAM2	Y	O(2)	Y	O(2)	R	-	R	-	R	-	O(4)	-	-	-	-
Backup registers	Y	Y	Y	Y	R	-	R	-	R	-	R	-	R	-	R
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	O	O	O	O(5)	O(5)	-	-	-
Peripheral voltage monitor (PVM3)	O	O	O	O	O	O	O	O	O	O	-	-	-	-	-
DMAx (x = 1, 2)	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
DMAMUX1	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
High-speed internal (HSI16)	O	O	O	O	O(6)	-	O(6)	-	O(6)	-	-	-	-	-	-
High-speed external (HSE32)	O	O	O(7)	O(7)	O(7)	-	O(7)	-	O(7)	-	O(7)	-	-	-	-
Low-speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	O	-	-	-	-
Low-speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O	-	O
Multi-speed internal (MSI)	O	O	O	O	O	-	O	-	O	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC/auto wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of tamper pins	3	3	3	3	3	O	3	O	3	O	3	O	3	O	3
USARTx (x= 1, 2)	O	O	O	O	O(8)	O(8)	O(8)	O(8)	-	-	-	-	-	-	-
Low-power UART (LPUART1)	O	O	O	O	O(8)	O(8)	O(8)	O(8)	O(8)	O(8)	-	-	-	-	-
I2Cx (x = 1, 2)	O	O	O	O	O(9)	O(9)	O(9)	O(9)	-	-	-	-	-	-	-
I2C3	O	O	O	O	O(9)	O(9)	O(9)	O(9)	O(9)	O(9)	-	-	-	-	-

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Table 8. Functionalities depending on system operating mode(1) (continued)

Peripheral	Run	Sleep	LPRun	LPSleep	Stop 0		Stop 1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
SPI1	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
SUBGHZSPI	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
SPI2S2	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
ADC	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
DAC	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	O	-	R	-	-	-	-	-	-
COMPx (x = 1, 2)	O	O	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
TIMx (x = 1, 2, 16, 17)	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
LPTIM1	O	O	O	O	O	O	O	O	O	O	-	-	-	-	-
LPTIMx (x = 2, 3)	O	O	O	O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	R	-	R	-	R	-	-	-	-	-	-
SysTick timer	O	O	O	O	R	-	R	-	R	-	-	-	-	-	-
True random number generator (RNG)	O (10)	O (10)	R	R	R	-	R	-	-	-	-	-	-	-	-
AES hardware accelerator	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
PKA hardware accelerator	O	O	O	O	R	-	R	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	R	-	R	-	R	-	-	-	-	-	-
IPCC	O	R	O	R	R	-	R	-	R	-	-	-	-	-	-
HSEM	O	R	O	R	R	-	R	-	-	-	-	-	-	-	-
GTZC TZSC	O	R	O	R	R	-	R	-	R	-	-	-	-	-	-
GTZC TZIC	O	R	O	R	R	-	R	-	R	-	-	-	-	-	-
EXTI	O	O	O	O	R	O	R	O	R	O	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	O	O	R (11)	3 pins (12)	(13)	3 pins (12)	-

1. Legend: Y = Yes (enabled). O = Optional (disabled by default and can be enabled by software). R = data retained. - = Not available. Gray cells indicate wakeup capability.
2. The SRAM clock can be gated on or off.
3. Flash memory can be placed in power-down mode.

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4. The SRAM2 content can optionally be retained when the PWR_CR3.RRS bit is set.
5. Only when the sub-GHz radio is active.
6. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral that requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
7. HSE32 can be used by sub-GHz radio system.
8. USART reception is functional in Stop 0 and Stop 1 modes. LPUART1 reception is functional is Stop 0, Stop 1, and Stop 2 modes. LPUART1 generates a wakeup interrupt on Start address match or received frame event.
9. I2Cx (x= 1, 2) address detection is functional in Stop 0 and Stop 1 modes. I2C3 address detection is functional in Stop 0, Stop 1 and Stop 2 modes. I2C3 generates a wakeup interrupt in case of address match.
10. Voltage scaling range 1 only.
11. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
12. The I/Os with wakeup from Standby/Shutdown capability are PA0, PC13 and PB3.
13. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode, but the configuration is lost when exiting the Shutdown mode.

Table 9. Low-power mode summary

Mode name	Entry	Wakeup source(1)	Wakeup system clock	Effect on clocks	Voltage regulators	
					MR	LPR
Sleep (Sleep-now or Sleep-on-exit)	WFI or return from ISR	Any interrupt	Same as before entering Sleep mode	CPU clock OFF No effect on other clocks or analog clock sources	ON	ON
	WFE	Wakeup event				
LPRun	Set LPR bit	Clear LPR bit	Same as LPRun clock	None	OFF	ON
LPSleep	Set LPR bit + WFI or return from ISR	Any interrupt	Same as before entering LPSleep mode	CPU clock OFF No effect on other clocks or analog clock sources	OFF	ON
	Set LPR bit + WFE	Wakeup event			OFF	ON
Stop 0	LPMS = 0b000 + SLEEPDEEP bit + WFI or return from ISR or WFE	Any EXTI line (configured in the EXTI registers). Specific peripherals events	HSI16 when STOPWUCK = 1 in RCC_CFGR. MSI with the frequency before entering the Stop mode when STOPWUCK = 0.	All clocks OFF except HSI16, LSI and LSE	ON	ON
Stop 1	LPMS = 0b001 + SLEEPDEEP bit + WFI or return from ISR or WFE				OFF	
Stop 2 (with I2C3, LPUART1, LPTIM1, SRAM1, SRAM2)	LPMS = 0b010+ SLEEPDEEP bit + WFI or return from ISR or WFE					

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Table 9. Low-power mode summary (continued)

Mode name	Entry	Wakeup source(1)	Wakeup system clock	Effect on clocks	Voltage regulators	
					MR	LPR
Standby (with SRAM2)	LPMS = 0b011+ Set RRS bit + SLEEPDEEP bit + WFI or return from ISR or WFE	Wakeup PVD, RFIRQ, wakeup RFBUSY, WKUP pin edge, RTC and TAMP event, LSECSS, external reset in NRST pin, IWDG reset	MSI 4 MHz	All clocks OFF except LSI and LSE	OFF	ON
Standby	LPMS = 0b011 + Clear RRS bit + SLEEPDEEP bit + WFI or return from ISR or WFE				OFF	OFF
Shutdown	LPMS = 0b1xx + SLEEPDEEP bit + WFI or return from ISR or WFE	WKUP pin edge, RTC and TAMP event, external reset in NRST pin	MSI 4 MHz	All clocks OFF except LSE	OFF	OFF

1. Refer to *Table 8: Functionalities depending on system operating mode*.

Relation between MCU and sub-GHz radio operating modes

The CPUs and sub-GHz radio have their own operating modes (see the table below).

Table 10. MCU and sub-GHz radio operating modes

CPU operating mode	Sub-GHz radio operating mode	Description
Run, Sleep	Sleep, Calibration, Standby, Active (FS, TX, RX)(1)	LDO or SMPS regulator active, MCU running in main regulator (MR) mode
LPRun, LPSleep	Deep-Sleep	LDO and SMPS regulator off, MCU running in low power regulator (LPR) mode
	Sleep, Calibration, Standby, Active (FS, TX, RX)	LDO or SMPS regulator active, MCU running in low power regulator (LPR) mode
Stop 0	Sleep, Calibration, Standby, Active (FS, TX, RX)(1)	LDO or SMPS regulator active, MCU running in main regulator (MR) mode
Stop 1 and Stop 2	Deep-Sleep	LDO and SMPS regulator off, MCU using low power regulator (LPR) mode
	Sleep, Calibration, Standby, Active (FS, TX, RX)	LDO or SMPS regulator active, MCU using low power regulator (LPR) mode
Standby	Deep-Sleep	LDO and SMPS regulator off, MCU regulator off or on in low power (LPR) mode(2).
	Sleep, Calibration, Standby, Active (FS, TX, RX)	LDO or SMPS regulator active, MCU regulator off or on in low power (LPR) mode(2)
Shutdown	Deep-Sleep(3)	LDO and SMPS regulator off, MCU regulator off

1. In the MCU Run, Sleep and Stop 0 modes, the sub-GHz radio is prevented from entering Deep-sleep mode.
2. When retaining SRAM2 in Standby mode, the MCU uses the low-power regulator (LPR) mode.

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3. When the CPU is in Shutdown mode, the sub-GHz radio cannot be activated and is forced in Deep-sleep mode.

3.11.1 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is "analog state" (the I/O Schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

This excludes the five serial-wire JTAG debug ports that are in pull-up/pull-down after reset.

3.12 Peripheral interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources and, consequently, reducing power-supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, LPRun, LPSleep, Stop 0, Stop 1 and Stop 2 modes.

Table 11. Peripherals interconnect matrix(1) (2)

Source	Destination													
	TIM1	TIM2	TIM16	TIM17	LPTIM1	LPTIM2	LPTIM3	ADC	DAC	COMP1	COMP2	DMAMUX1	IRTIM	SUBGHZSPI
TIM1	-	X	-	-	-	-	-	X	X	X	X	-	-	-
TIM2	X	-	-	-	-	-	-	X	X	X	X	-	-	-
TIM16	-	-	-	-	-	-	-	-	-	-	-	-	X	-
TIM17	X	-	-	-	-	-	-	-	-	-	-	-	X	-
LPTIM1	-	-	-	-	-	-	X	-	X	-	-	X	-	-
LPTIM2	-	-	-	-	-	-	X	-	X	-	-	X	-	-
LPTIM3	-	-	-	-	-	-	-	-	-	-	-	X	-	X
ADC	X	-	-	-	-	-		-	-	-	-	-	-	-
Temperature sensor	-	-	-	-	-	-	-	X	-	-	-	-	-	-
VBAT(3)	-	-	-	-	-	-	-	X	-	-	-	-	-	-
VREFINT	-	-	-	-	-	-	-	X	-	-	-	-	-	-
HSE32	-	-	-	X	-	-	-	-	-	-	-	-	-	-
LSE	-	X	X	-	-	-	-	-	-	-	-	-	-	-
MSI	-	-	-	X	-	-	-	-	-	-	-	-	-	-
LSI	-	-	X	-	-	-	-	-	-	-	-	-	-	-
MCO	-	-	-	X	-	-	-	-	-	-	-	-	-	-

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Table 11. Peripherals interconnect matrix(1) (2) (continued)

Source	Destination													
	TIM1	TIM2	TIM16	TIM17	LPTIM1	LPTIM2	LPTIM3	ADC	DAC	COMP1	COMP2	DMAMUX1	IRTIM	SUBGHZSPI
GPIO EXTI	-	-	-	-	-	-	-	X	X	-	-	X	-	-
RTC	-	-	X	-	X	X	-	-	-	-	-	-	-	-
TAMP	-	-	-	-	X	X	-	-	-	-	-	-	-	-
COMP1	X	X	X	X	X	X	-	-	-	-	-	-	-	-
COMP2	X	X	X	X	X	X	-	-	-	-	-	-	-	-
SYST ERR	X	-	X	X	-	-	-	-	-	-	-	-	-	-

1. For more details, refer to section “Interconnection details” of the reference manual.
2. The “-” symbol in grayed cells means no interconnect.
3. VDD on STM32WL55/4UxYx devices.

3.13 Reset and clock controller (RCC)

The following different clock sources can be used to drive the system clock (SYSCLK):

- HSI16 (high-speed internal) 16 MHz RC oscillator clock
- MSI (multi-speed internal) RC oscillator clock from 100 kHz to 48 MHz
- HSE32 (high-speed external) 32 MHz oscillator clock, with trimming capacitors.
- PLL clock

The MSI is used as system clock source after startup from reset, configured at 4 MHz.

The devices have the following additional clock sources:

- LSI: 32 kHz low-speed internal RC that may drive the independent watchdog and optionally the RTC used for auto-wakeup from Stop and Standby modes.
- LSE: 32.768 kHz low-speed external crystal that optionally drives the RTC used for auto-wakeup from Stop, Standby and Shutdown modes, or the real-time clock (RTCCLK).

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

Several prescalers can be used to configure the AHB frequencies (HCLK3/PCLK3, HCLK1, HCLK2), the high-speed APB2 (PCLK2) and the low-speed APB1 (PCLK1) domains. The maximum frequency of the AHB (HCLK3, HCLK1, and HCLK2), the PCLK1 and the PCLK2 domains is 48 MHz.

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Most peripheral clocks are derived from their bus clock (HCLK, PCLK) except the following:

- The clock used for true RNG, is derived (selected by software) from one of the following sources:
  - PLL VCO (PLLQCLK) (only available in Run mode)
  - MSI (only available in Run mode)
  - LSI clock
  - LSE clock
- The ADC clock is derived (selected by software) from one of the following sources:
  - system clock (SYSCLK) (only available in Run mode)
  - HSI16 clock (only available in Run mode)
  - PLL VCO (PLLPCLK) (only available in Run mode)
- The DAC uses the LSI clock in sample and hold mode
- The (LP)U(S)ARTs clocks are derived (selected by software) from one of the following sources:
  - system clock (SYSCLK) (only available in Run mode)
  - HSI16 clock (available in Run and Stop modes)
  - LSE clock (available in Run and Stop modes)
  - APB clock (PCLK depending on which APB the U(S)ART is mapped) (available in CRun and CSleep when also enabled in (LP)U(S)ARTxSMEN)

  The wakeup from Stop mode is supported only when the clock is HSI16 or LSE.
- The I2Cs clocks are derived (selected by software) from one of the following sources:
  - system clock (SYSCLK) (only available in Run mode)
  - HSI16 clock (available in Run and Stop modes)
  - APB clock (PCLK depending on which APB the I2C is mapped) (available in CRun and CSleep when also enabled in I2CxSMEN.)

  The wakeup from Stop mode is supported only when the clock is HSI16.
- The SPI2S2 I2S clock is derived (selected by software) from one of the following sources:
  - HSI16 clock (only available in Run mode)
  - PLL VCO (PLLQCLK) (only available in Run mode)
  - external input I2S_CK (available in Run and Stop modes)
- The low-power timers (LPTIMx) clock is derived (selected by software) from one of the following sources:
  - LSI clock (available in Run and Stop modes)
  - LSE clock (available in Run and Stop modes)
  - HSI16 clock (only available in Run mode)
  - APB clock (PCLK depending on which APB the LPTIMx is mapped) (available in Run and CStop when enabled in LPTIMxSMEN.)
  - external clock mapped on LPTIMx_IN1 (available in Run and Stop modes)

  The functionality in Stop mode (including wakeup) is supported only when the clock is LSI or LSE, or in external clock mode.

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- The RTC clock is derived (selected by software) from one of the following sources:
  - LSE clock
  - LSI clock
  - HSE32 clock divided by 32

  The functionality in Stop mode (including wakeup) is supported only when the clock is LSI or LSE.
- The IWDG clock is always the LSI clock.

The RCC feeds the CPU1 system timer (SysTick) external clock with the AHB clock (HCLK1) divided by eight. The SysTick can work either with this clock or directly with the CPU1 clock (HCLK1), configurable in the SysTick control and status register.

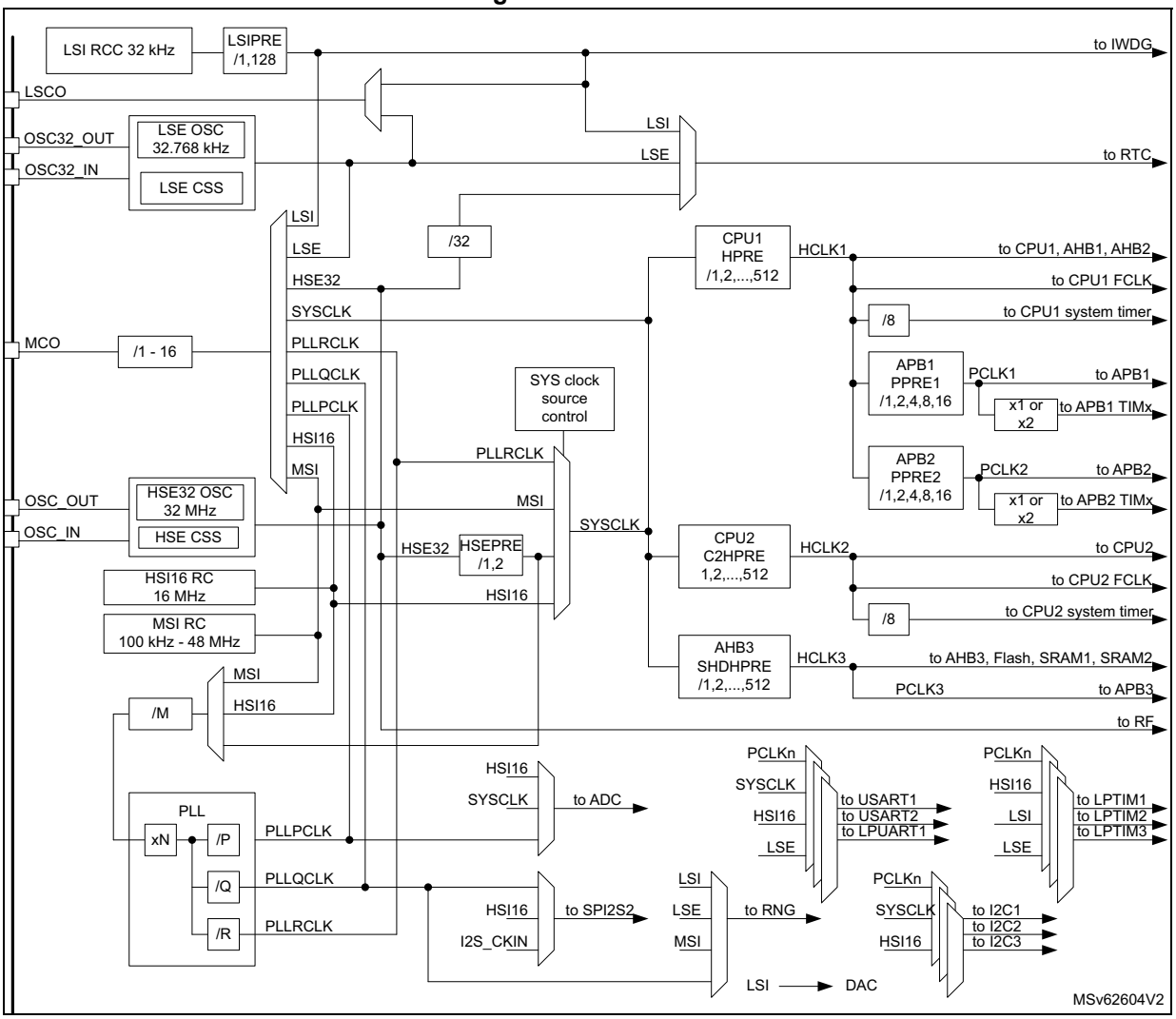
FCLK1 acts as CPU1 free-running clock. For more details, refer to the programming manual *STM32 Cortex-M4 MCUs and MPUs* programming manual (PM0214).

The RCC feeds the CPU2 system timer (SysTick) external clock with the AHB clock (HCLK2) divided by eight. The SysTick can work either with this clock or directly with the CPU2 clock (HCLK2), configurable in the SysTick control and status register.

FCLK2 acts as CPU2 free-running clock.

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Figure 9. Clock tree



1. For full details about the internal and external clock source characteristics, refer to the electrical characteristics section in the device datasheet.
2. The ADC clock can additionally be derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2 or 4). When the programmable factor is 1, the AHB prescaler must be equal to 1.

3.14 Hardware semaphore (HSEM)

The HSEM provides a 16- (32-bit) register based semaphores. The semaphores can be used to ensure synchronization between different processes running between different cores. The HSEM provides a non blocking mechanism to lock semaphores in an atomic way. The following functions are provided:

- Locking a semaphore can be done in two ways:
  - 2-step lock: by writing COREID and PROCID to the semaphore, followed by a read check
  - 1-step lock: by reading the COREID from the semaphore
- Interrupt generation when a semaphore is unlocked: Each semaphore may generate an interrupt on one of the interrupt lines.

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- Semaphore clear protection: A semaphore is only unlocked when COREID and PROCID match.
- Global semaphore clear per COREID

3.15 Inter-processor communication controller (IPCC)

The IPCC is used for communicating data between two processors.

The IPCC block provides a non blocking signaling mechanism to post and retrieve communication data in an atomic way. It provides the signaling for twelve channels:

- six channels in the direction from processor 1 to processor 2
- six channels in the opposite direction

It is then possible to have two different communication types in each direction.

The IPCC communication data must be located in a common memory, that is not part of the IPCC block.

3.16 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.17 Direct memory access controller (DMA)

The DMA (direct memory access) is used to provide high-speed data transfer between peripherals and memory, as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The DMA controller has 14 channels in total. A full cross matrix allows the peripherals, with DMA support, to be mapped on any of the available DMA channels. Each DMA channel has an arbiter for handling the priority between DMA requests.

The DMA main features are listed below:

- 14 independently configurable channels (requests)
- a full cross matrix between peripherals and all 14 channels and an hardware trigger possibility through the DMAMUX1
- software programmable priorities between requests from channels of one DMA (four levels: very-high, high, medium, low), plus hardware priorities management in case of equality (example: request 1 has priority over request 2)
- independent source and destination transfer size (byte, half-word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- support for circular buffer management

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- three event flags (DMA half-transfer, DMA transfer complete and DMA transfer error), logically ORed together in a single interrupt request for each channel
- memory-to-memory transfer
- peripheral-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfers
- access to flash memory, SRAM, APB and AHB peripherals, as source and destination
- programmable number of data to be transferred (up to 65536)
- secure and privileged support per channel level configuration

Table 12. DMA1 and DMA2 implementation

Feature	DMA1	DMA2
Number of channels	7	7

DMAMUX1 is used to route the peripherals with DMA source support, to any DMA channel.

3.18 Interrupts and events

3.18.1 Nested vectored interrupt controller (NVIC)

The devices embed an NIVC able to manage 16 priority levels, and to handle up to 62 maskable interrupt channels plus the 16 interrupt lines of the Cortex-M4.

The device also embeds an NVIC able to manage four priority levels, and handles up to 32 maskable interrupt channels plus the 16 interrupt lines of the Cortex-M0+.

The NVIC benefits are the following:

- low-latency interrupt processing
- interrupt entry vector table address passed directly to the core
- early processing of interrupts
- processing of late-arriving higher-priority interrupts
- support for tail chaining
- processor state automatically saved
- interrupt entry restored on interrupt exit, with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.18.2 Extended interrupt/event controller (EXTI)

The EXTI manages wakeup through configurable and direct event inputs. It provides wake-up requests to the power control, and generates interrupt requests to the CPU1/2 NVIC and events to the CPU1/2 event input.

Configurable events/interrupts come from peripherals that are able to generate a pulse and allow the selection between the event/interrupt trigger edge and a software trigger.

Direct events/interrupts come from peripherals having their own clearing mechanism.

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3.19 Cyclic redundancy check (CRC)

The CRC calculation unit is used to get a CRC code from 8-, 16- or 32-bit data word and a generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps to compute a signature of he software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

3.20 Analog-to-digital converter (ADC)

A native 12-bit ADC is embedded into the devices. It can be extended to 16-bit resolution through hardware oversampling. The ADC has up to 12 external channels and four internal channels (temperature sensor, voltage reference, V_{BAT}[a] monitoring, DAC output). The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU1/2 frequency, allowing maximum sampling rate of ~2 Msps even with a low CPU speed. An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate in the whole V_{DD} supply range.

The ADC features a hardware oversampler up to 256 samples, improving the resolution to 16 bits. Refer to the application note *Improving STM32F1 Series, STM32F3 Series and STM32Lx Series ADC resolution by oversampling* (AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions with timers.

3.20.1 Temperature sensor

The temperature sensor (TS) generates a V_{TS} voltage that varies linearly with temperature.

The temperature sensor is internally connected to the ADC VIN[12] input channel, to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor may vary from part to part due to process variation, the uncalibrated internal temperature sensor is suitable only for relative temperature measurements.

To improve the accuracy of the temperature sensor, each part is individually factory-calibrated by ST. The resulting calibration data is stored in the device engineering bytes, accessible in read-only mode.

a. VDD on STM32WL55/54UxYx devices.

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Table 13. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.3 V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.3 V (± 10 mV)	0x1FFF 75C8 - 0x1FFF 75C9

3.20.2 Internal voltage reference (V_{REFINT})

V_{REFINT} provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to the ADC VIN[13] input channel.

V_{REFINT} is individually and precisely measured, for each part, by ST, during production test and stored in the device engineering bytes. It is accessible in read-only mode.

Table 14. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.3 V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.20.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT}[(a)] battery voltage using the ADC VIN[14] input channel. As V_{BAT} may be higher than V_{DDA}, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by three. As a consequence, the converted digital value is one third the V_{BAT} voltage.

3.21 Digital-to-analog converter (DAC)

The 1-channel 12-bit buffered DAC converts a digital value into an analog voltage available on the channel output. The architecture of each channel is based on an integrated resistor string and an inverting amplifier. The digital circuitry is common for both channels.

DAC main features:

- 1 DAC output channel
- 8-bit or 12-bit output mode
- buffer offset calibration (factory and user trimming)
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- independent or simultaneous conversion for DAC channels

a. V_{DD} on STM32WL55/54UxYx devices.

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- DMA capability for either DAC channel
- triggering with timer events, synchronized with DMA
- triggering with external events

Sample-and-hold low-power mode, with internal or external capacitor

3.22 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer that can be used as voltage reference for ADC, and also as voltage reference for external components through the VREF+ pin.

VREFBUF supports two voltages: 2.048 V and 2.5 V.

An external voltage reference can be provided through the VREF+ pin when VREFBUF is off.

3.23 Comparator (COMP)

The devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- external I/O
- internal reference voltage or submultiple (1/4, 1/2, 3/4)

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers, and can be also combined into a window comparator.

3.24 True random number generator (RNG)

The devices embed a true RNG that delivers 32-bit random numbers generated by an integrated analog circuitry.

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

3.25 Advanced encryption standard hardware accelerator (AES)

The AES encrypts or decrypts data, using an algorithm and implementation fully compliant with the advanced encryption standard (AES) defined in FIPS (federal information processing standards) publication 197.

Multiple chaining modes are supported (ECB, CBC, CTR, GCM, GMAC, CCM), for key sizes of 128 or 256 bits. The AES supports DMA single transfers for incoming and outgoing data (two DMA channels required).

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3.26 Public key accelerator (PKA)

The PKA is used to compute cryptographic public key primitives, specifically those related to RSA (Rivest, Shamir and Adleman), Diffie-Hellmann or ECC (elliptic curve cryptography) over GF(p) (Galois fields). These operations are executed in the Montgomery domain.

3.27 Timer and watchdog

The devices include one advanced 16-bit timer, one general-purpose 32-bit timer, two 16-bit basic timers, three low-power timers, two watchdog timers and a SysTick timer.

The table below compares the features of the advanced control, general purpose and basic timers.

Table 15. Timer features

Timer type	Timer name	Counter resolution (bits)	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16	Up, down and up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM2	32					NA
	TIM16	16	Up			2	1
	TIM17						
Low power	LPTIM1 LPTIM2 LPTIM3					1	

3.27.1 Advanced-control timer (TIM1)

The advanced-control timer TIM1 can be seen as a three-phase PWM multiplexed on six channels. Each channel has complementary PWM outputs with programmable inserted dead-times. Each channel can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 - 100 %)
- one-pulse mode output

In debug mode, the TIM1 counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose timers (described in the next section) using the same architecture. TIM1 can then work together with TIM2 via the peripheral interconnect matrix, for synchronization or event chaining.

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3.27.2 General-purpose timers (TIM2, TIM16, TIM17)

Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

TIM2 main features:

- full-featured general-purpose timer
- four independent channels for input capture/output compare, PWM or one-pulse mode output
- counter that can be frozen in debug mode
- independent DMA request generation, support of quadrature encoders

TIM16 and TIM17 main features:

- general-purpose timers with mid-range features
- 16-bit auto-reload upcounters and 16-bit prescalers
- 1 channel and 1 complementary channel
- channels that can all be used for input capture/output compare, PWM or one-pulse mode output
- counter that can be frozen in debug mode
- independent DMA request generation

3.27.3 Low-power timers (LPTIM1, LPTIM2 and LPTIM3)

These low-power timers have an independent clock and run in Stop mode if they are clocked by LSE, LSI, or by an external clock. They are able to wake up the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 and LPTIM3 are active in Stop 0 and Stop 1 modes.

LPTIM1/2/3 main features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- configurable output: pulse, PWM
- continuous/one-shot mode
- selectable software/hardware input trigger
- selectable clock source
- internal clock sources: LSE, either LSI, HSI16 or APB clock
- external clock source over LPTIM input (works even with no internal clock source running, used by pulse counter application)
- programmable digital glitch filter
- encoder mode (LPTIM1 only)

3.27.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and a 8-bit prescaler. The IWDG is clocked from an independent 32 kHz internal RC (LSI). As the IWDG operates independently from the main clock, it can operate in Stop and Standby modes.

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The IWDG can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. The IWDG is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.27.5 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. The WWDG can be used as a watchdog to reset the device when a problem occurs.

The WWDG is clocked from the main clock and has an early warning interrupt capability. The counter can be frozen in debug mode.

3.27.6 SysTick timer

This timer is dedicated to real-time operating systems, but can also be used as a standard down counter.

SysTick timer main features:

- 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source

3.28 Real-time clock (RTC), tamper and backup registers

The RTC is an independent BCD timer/counter. The RTC provides a time-of-day clock/calendar with programmable alarm interrupts.

As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low-power mode or under reset).

The RTC provides an automatic wakeup to manage all low-power modes.

The RTC is functional in VBAT mode.

Twenty 32-bit backup registers are retained in all low-power modes and also in VBAT mode. These registers can be used to store sensitive data as their content is protected by a tamper detection circuit.

Three tamper pins and four internal tampers are available for anti-tamper detection. The external tamper pins can be configured for edge or level detection with or without filtering.

3.29 Inter-integrated circuit interface (I2C)

The device embeds three I2Cs, with features implementation listed in the he table below.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C bus specification and user manual rev. 5 compatibility:
  - slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 Kbit/s

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  - Fast-mode (Fm), with a bitrate up to 400 Kbit/s
  - Fast-mode plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - programmable setup and hold times
  - clock stretching (optional)
- SMBus (system management bus) specification rev 2.0 compatibility:
  - hardware PEC (packet error checking) generation and verification with ACK control
  - address resolution protocol (ARP) support
  - SMBus alert
- PMBus (power system management protocol) specification rev 1.1 compatibility
- independent clock: a choice of independent clock sources allowing the I^2C communication speed to be independent from the PCLK reprogramming (see *Figure 9*)
- wakeup from Stop mode on address match
- programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 16. I2C implementation

I2C features(1)	I2C1(2)	I2C2(2)	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard-mode (up to 100 Kbit/s)	X	X	X
Fast-mode (up to 400 Kbit/s)	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Independent clock	X	X	X
Wakeup from Stop mode	X(3)	X(3)	X(4)
SMBus/PMBus	X	X	X

1. X = supported.
2. The register content is lost in Stop 2 mode.
3. Wakeup supported from Stop 0 and Stop 1 modes.
4. Wakeup supported from Stop 0, Stop 1 and Stop 2 modes.

3.30 Universal synchronous/asynchronous receiver transmitter (USART/UART)

The devices embed two universal synchronous receiver transmitters, USART1 and USART2 (see *Table 17* for the implementation details).

Each USART provides asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode. Each USART has LIN Master/Slave capability and provides hardware management of the CTS and RTS signals, and RS485 driver enable.

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The USART is able to communicate at speeds of up to 4 Mbit/s, and also provides Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

The USART supports synchronous operation (SPI mode), and can be used as an SPI master.

The USART has a clock domain independent from the CPU clock, allowing the USART to wake up the MCU from Stop mode, using baudrates up to 200 kbaud.

The wakeup events from Stop mode are programmable and can be one of the following:

- start bit detection
- any received data frame
- a specific programmed data frame

The USART interface can be served by the DMA controller.

3.31 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one low-power UART (LPUART1) that enables asynchronous serial communication with minimum power consumption. The LPUART supports half-duplex single-wire communication and modem operations (CTS/RTS), allowing multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode using baudrates up to 220 Kbaud. The wakeup events from Stop mode are programmable and can be one of the following:

- start bit detection
- any received data frame
- a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low-energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

Table 17. USART/LPUART features

USART modes/features(1)	USART1/2	LPUART1
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (Master/Slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-

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Table 17. USART/LPUART features (continued)

USART modes/features(1)	USART1/2	LPUART1
Dual clock domain and wakeup from low-power mode	X	X
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver enable	X	X
USART data length	7, 8 and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	8	

1. X = supported.

3.32 Serial peripheral interface (SPI)/integrated-interchip sound interface (I2S)

The SPI/I2S interface can be used to communicate with external devices using the SPI protocol or the I^2S audio protocol. SPI or I2S mode is selectable by software. SPI Motorola® mode is selected by default after a device reset.

The SPI protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices. The SPI interface can be configured as master and, in this case, it provides the communication clock (SCK) to the external slave device. The SPI interface can also operate in multimaster configuration.

The I^2S protocol is also a synchronous serial communication interface. It can operate in slave or master mode with half-duplex communication. It can address four different audio standards including the Philips I^2S standard, the MSB- and LSB-justified standards and the PCM standard.

Table 18. SPI and SPI/I2S implementation(1)

Features	SPI1	SPI2S2	SUBGHZSPI
Enhanced NSSP and TI modes	Yes		
Hardware CRC calculation	Yes	Yes	No
I^2S support	No	Yes	No
Data size configurable (bits)	from 4 to 16		
Rx/Tx FIFO size (bits)	32		
Wakeup capability from LPSleep	Yes		

1. The SPI1 and SPI2S2 instances are general purpose type while the SUBGHZSPI instance is dedicated for Sub-GHz radio control exclusively. Radio is controlled internally through SUBGHZSPI and, for debug purpose only, from the external.

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3.33 Development support

Serial-wire JTAG debug port (SWJ-DP)

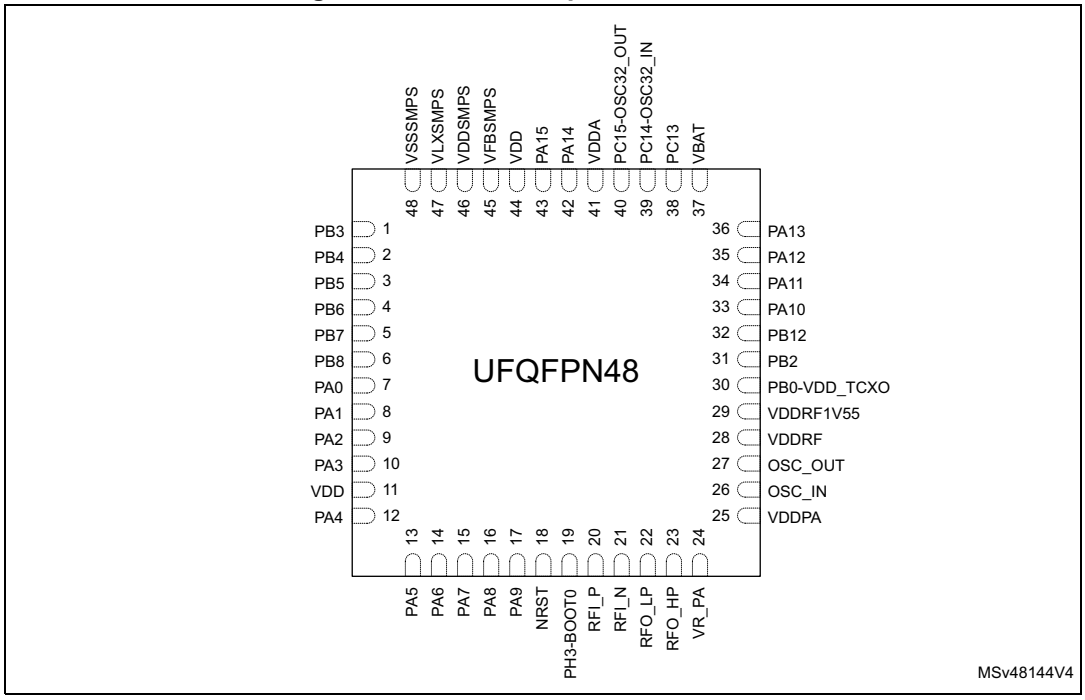
The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial-wire debug port, that enables either a serial-wire debug or a JTAG probe to be connected to the target.

The debug is performed using only two pins instead of the five required by the JTAG (JTAG pins can then be reused as GPIOs with alternate function). The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

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4 Pinouts, pin description and alternate functions

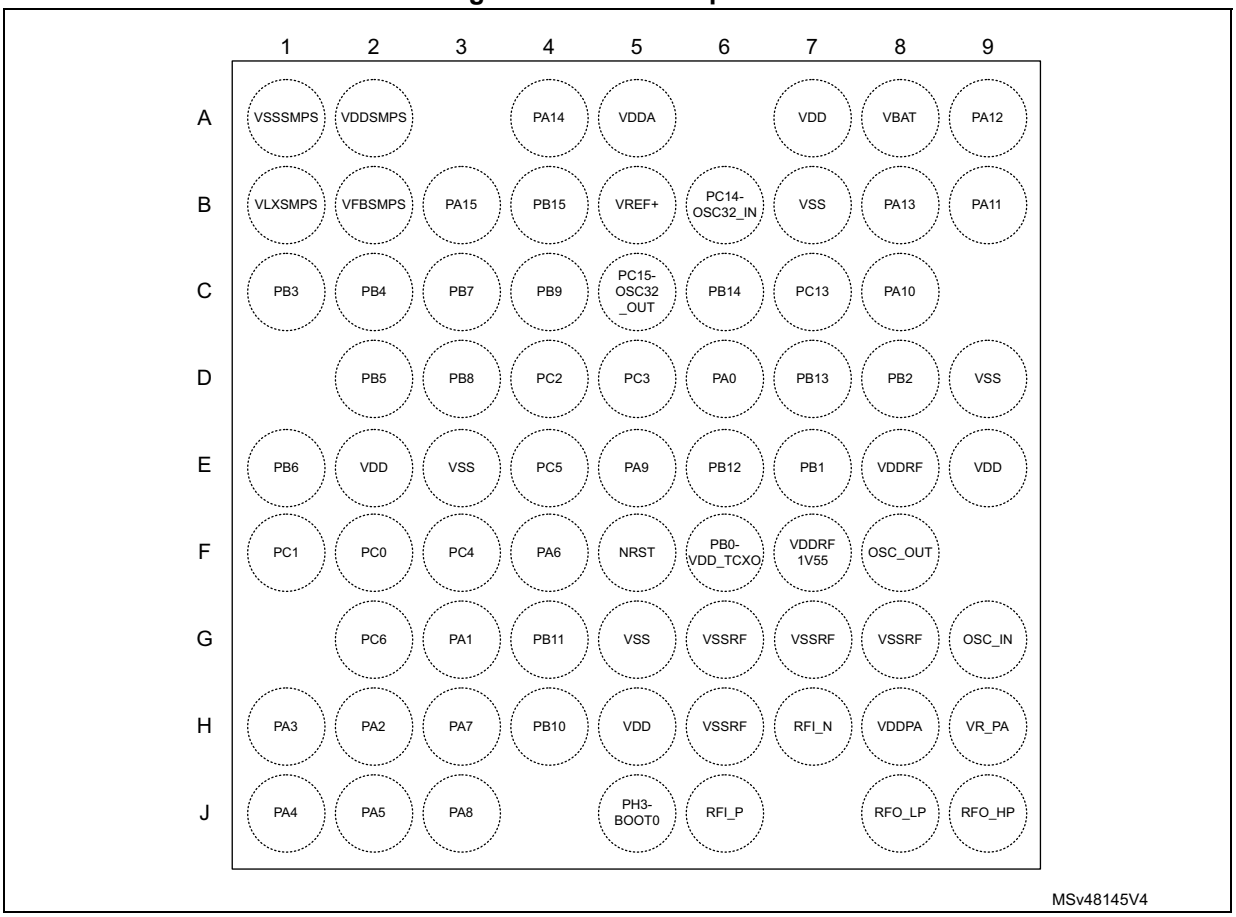
Figure 10. UFQFPN48 pinout



1. The above figure shows the package top view.
2. The exposed pad must be connected to the ground plain.

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Figure 11. UFBGA73 pinout



1. The above figure shows the package top view.

Table 19. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
	O	Output only pin
I/O structure	FT	5 V tolerant I/O
	RF	Radio RF pin
	TT	3 V tolerant I/O
	Option for FT I/Os	
	_f	I/O, Fm+ capable
	_a	I/O, with Analog switch function supplied by V_{DDA}

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Table 19. Legend/abbreviations used in the pinout table (continued)

Name		Abbreviation	Definition
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 20. STM32WL55/54xx pin definition

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	UFBGA73						
-	-	VSS	S	-	-	-	-
1	C1	PB3	I/O	FT_a	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, RF_IRQ0, USART1_RTS, DEBUG_RF_DTB1, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC_IN2, TAMP_IN3/WKUP3
2	C2	PB4	I/O	FT_fa	-	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_LDORDY, TIM17_BKIN, CM4_EVENTOUT	COMP1_INP, COMP2_INP, ADC_IN3
3	D2	PB5	I/O	FT_a	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, RF_IRQ1, USART1_CK, COMP2_OUT, TIM16_BKIN, CM4_EVENTOUT	-
-	E3	VSS	S	-	-	-	-
-	E2	VDD	S	-	-	-	-
4	E1	PB6	I/O	FT_f	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, TIM16_CH1N, CM4_EVENTOUT	-
5	C3	PB7	I/O	FT_f	-	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TIM17_CH1N, CM4_EVENTOUT	-
6	D3	PB8	I/O	FT_f	-	TIM1_CH2N, I2C1_SCL, RF_IRQ2, TIM16_CH1, CM4_EVENTOUT	-
-	C4	PB9	I/O	FT_f	-	TIM1_CH3N, I2C1_SDA, SPI2_NSS/I2S2_WS, IR_OUT, TIM17_CH1, CM4_EVENTOUT	-

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Table 20. STM32WL55/54xx pin definition (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	UFBGA73						
-	F2	PC0	I/O	FT_f	-	LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LPTIM2_IN1, CM4_EVENTOUT	-
-	F1	PC1	I/O	FT_f	-	LPTIM1_OUT, SPI2_MOSI/I2S2_SD, I2C3_SDA, LPUART1_TX, CM4_EVENTOUT	-
-	D4	PC2	I/O	FT	-	LPTIM1_IN2, SPI2_MISO, CM4_EVENTOUT	-
-	D5	PC3	I/O	FT	-	LPTIM1_ETR, SPI2_MOSI/I2S2_SD, LPTIM2_ETR, CM4_EVENTOUT	-
-	F3	PC4	I/O	FT	-	CM4_EVENTOUT	-
-	E4	PC5	I/O	FT	-	CM4_EVENTOUT	-
-	G2	PC6	I/O	FT	-	I2S2_MCK, CM4_EVENTOUT	-
7	D6	PA0	I/O	FT_a	-	TIM2_CH1, I2C3_SMBA, I2S_CKIN, USART2_CTS, COMP1_OUT, DEBUG_PWR_REGLP1S, TIM2_ETR, CM4_EVENTOUT	TAMP_IN2/WKUP1
8	G3	PA1	I/O	FT_a	-	TIM2_CH2, LPTIM3_OUT, I2C1_SMBA, SPI1_SCK, USART2_RTS, LPUART1_RTS, DEBUG_PWR_REGLP2S, CM4_EVENTOUT	-
9	H2	PA2	I/O	FT_a	-	LSCO, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT, DEBUG_PWR_LDORDY, CM4_EVENTOUT	LSCO
10	H1	PA3	I/O	FT_a	-	TIM2_CH4, I2S2_MCK, USART2_RX, LPUART1_RX, CM4_EVENTOUT	-
-	G5	VSS	S	-	-	-	-
11	H5	VDD	S	-	-	-	-

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Table 20. STM32WL55/54xx pin definition (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	UFBGA73						
12	J1	PA4	I/O	FT	-	RTC_OUT2, LPTIM1_OUT, SPI1_NSS, USART2_CK, DEBUG_SUBGHZSPI_ NSSOUT, LPTIM2_OUT, CM4_EVENTOUT	-
13	J2	PA5	I/O	FT	-	TIM2_CH1, TIM2_ETR, SPI2_MISO, SPI1_SCK, DEBUG_SUBGHZSPI_ SCKOUT, LPTIM2_ETR, CM4_EVENTOUT	-
14	F4	PA6	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI1_MISO, LPUART1_CTS, DEBUG_SUBGHZSPI_ MISOOUT, TIM16_CH1, CM4_EVENTOUT	-
15	H3	PA7	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, COMP2_OUT, DEBUG_SUBGHZSPI_ MOSIOUT, TIM17_CH1, CM4_EVENTOUT	-
16	J3	PA8	I/O	FT_a	-	MCO, TIM1_CH1, SPI2_SCK/I2S2_CK, USART1_CK, LPTIM2_OUT, CM4_EVENTOUT	-
17	E5	PA9	I/O	FT_fa	-	TIM1_CH2, SPI2_NSS/I2S2_WS, I2C1_SCL, SPI2_SCK/I2S2_CK, USART1_TX, CM4_EVENTOUT	-
-	H4	PB10	I/O	FT_f	-	TIM2_CH3, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_RX, COMP1_OUT, CM4_EVENTOUT	-
-	G4	PB11	I/O	FT_f	-	TIM2_CH4, I2C3_SDA, LPUART1_TX, COMP2_OUT, CM4_EVENTOUT	-
18	F5	NRST	I/O	FT	-	-	-
19	J5	PH3-BOOT0	I/O	FT	-	CM4_EVENTOUT	BOOT0
-	-	VDD	S	-	-	-	-
-	-	VSS	S	-	-	-	-
-	H6	VSSRF	S	-	-	-	-

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Table 20. STM32WL55/54xx pin definition (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	UFBGA73						
-	G6	VSSRF	S	-	-	-	-
20	J6	RFI_P	I	RF	-	-	-
21	H7	RFI_N	I	RF	-	-	-
-	G7	VSSRF	S	-	-	-	-
-	-	VSSRF	S	-	-	-	-
22	J8	RFO_LP	O	RF	-	-	-
-	G8	VSSRF	S	-	-	-	-
23	J9	RFO_HP	O	RF	-	-	-
-	-	VSSRF	S	-	-	-	-
24	H9	VR_PA	S	-	-	-	-
25	H8	VDDPA	S	-	-	-	-
-	-	VSSRF	S	-	-	-	-
26	G9	OSC_IN	I	RF	-	-	-
27	F8	OSC_OUT	O	RF	-	-	-
-	-	VSSRF	S	-	-	-	-
28	E8	VDDRF	S	-	-	-	-
29	F7	VDDRF1V55	S	-	-	-	-
-	D9	VSS	S	-	-	-	-
-	E9	VDD	S	-	-	-	-
30	F6	PB0-VDD_TCXO	I/O	TT	-	COMP1_OUT, CM4_EVENTOUT	-
-	E7	PB1	I/O	FT_a	-	LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT	COMP2_INP, ADC_IN5
31	D8	PB2	I/O	FT_a	-	LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, DEBUG_RF_SMPSRDY, CM4_EVENTOUT	COMP1_INP, COMP2_INM, ADC_IN4
32	E6	PB12	I/O	FT	-	TIM1_BKIN, I2C3_SMBA, SPI2_NSS/I2S2_WS, LPUART1_RTS, CM4_EVENTOUT	-

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Table 20. STM32WL55/54xx pin definition (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	UFBGA73						
-	D7	PB13	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_CTS, CM4_EVENTOUT	ADC_IN0
-	C6	PB14	I/O	FT_fa	-	TIM1_CH2N, I2S2_MCK, I2C3_SDA, SPI2_MISO, CM4_EVENTOUT	ADC_IN1
33	C8	PA10	I/O	FT_fa	-	RTC_REFIN, TIM1_CH3, I2C1_SDA, SPI2_MOSI/I2S2_SD, USART1_RX, DEBUG_RF_HSE32RDY, TIM17_BKIN, CM4_EVENTOUT	COMP1_INM, COMP2_INM, DAC_OUT1, ADC_IN6
34	B9	PA11	I/O	FT_fa	-	TIM1_CH4, TIM1_BKIN2, LPTIM3_ETR, I2C2_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_NRESET, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC_IN7
35	A9	PA12	I/O	FT_fa	-	TIM1_ETR, LPTIM3_IN1, I2C2_SCL, SPI1_MOSI, RF_BUSY, USART1_RTS, CM4_EVENTOUT	ADC_IN8
36	B8	PA13	I/O	FT_a	-	JTMS-SWDIO, I2C2_SMBA, IR_OUT, CM4_EVENTOUT	ADC_IN9
-	B7	VSS	S	-	-	-	-
-	A7	VDD	S	-	-	-	-
37	A8	VBAT	S	-	-	-	-
38	C7	PC13	I/O	FT	-	CM4_EVENTOUT	TAMP_IN1/ RTC_OUT1/RTC_TS/ WKUP2
39	B6	PC14-OSC32_IN	I/O	FT	-	CM4_EVENTOUT	OSC32_IN
40	C5	PC15-OSC32_OUT	I/O	FT	-	CM4_EVENTOUT	OSC32_OUT
-	B5	VREF+	S	-	-	-	-
41	A5	VDDA	S	-	-	-	-
-	-	VSS	S	-	-	-	-
42	A4	PA14	I/O	FT_a	-	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, CM4_EVENTOUT	ADC_IN10

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Table 20. STM32WL55/54xx pin definition (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	UFBGA73						
43	B3	PA15	I/O	FT_fa	-	JTDI, TIM2_CH1, TIM2_ETR, I2C2_SDA, SPI1_NSS, CM4_EVENTOUT	COMP1_INM, COMP2_INP, ADC_IN11
-	B4	PB15	I/O	FT_f		TIM1_CH3N, I2C2_SCL, SPI2_MOSI/I2S2_SD, CM4_EVENTOUT	-
44	-	VDD	S	-	-	-	-
-	-	VSS	S	-	-	-	-
49(1)	-	VSS	S	-	-	-	-
45	B2	VFBSMPS	S	-	-	-	-
46	A2	VDDSMPS	S	-	-	-	-
47	B1	VLXSMPS	S	-	-	-	-
48	A1	VSSSMPS	S	-	-	-	-

1. Pin 49 is an exposed pad that must be connected to V_{SS}.

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Table 21. Alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2/ TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	RF	USART1 / USART2	LPUART1	-	-	-	COMP1/ COMP2/ TIM1	DEBUG	TIM2/ TIM16/ TIM17/ LPTIM2	EVENOUT
Port A	PA0	-	TIM2_CH1	-	-	I2C3_SMBA	I2S_CKIN	-	USART2_CTS	-	-	-	-	COMP1_OUT	DEBUG_PWR_REGLP1S	TIM2_ETR	CM4_EVENTOUT
	PA1	-	TIM2_CH2	-	LPTIM3_OUT	I2C1_SMBA	SPI1_SCK	-	USART2_RTS	LPUART1_RTS	-	-	-	-	DEBUG_PWR_REGLP2S	-	CM4_EVENTOUT
	PA2	LSCO	TIM2_CH3	-	-	-	-	-	USART2_TX	LPUART1_TX	-	-	-	COMP2_OUT	DEBUG_PWR_LDORDY	-	CM4_EVENTOUT
	PA3	-	TIM2_CH4	-	-	-	I2S2_MCK	-	USART2_RX	LPUART1_RX	-	-	-	-	-	-	CM4_EVENTOUT
	PA4	RTC_OUT2	LPTIM1_OUT	-	-	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	DEBUG_SUBGHZSPI_NSSOUT	LPTIM2_OUT	CM4_EVENTOUT
	PA5	-	TIM2_CH1	TIM2_ETR	SPI2_MISO	-	SPI1_SCK	-	-	-	-	-	-	-	DEBUG_SUBGHZSPI_SCKOUT	LPTIM2_ETR	CM4_EVENTOUT
	PA6	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI1_MISO	-	-	LPUART1_CTS	-	-	-	TIM1_BKIN	DEBUG_SUBGHZSPI_MISOOUT	TIM16_CH1	CM4_EVENTOUT
	PA7	-	TIM1_CH1N	-	-	I2C3_SCL	SPI1_MOSI	-	-	-	-	-	-	COMP2_OUT	DEBUG_SUBGHZSPI_MOSIOUT	TIM17_CH1	CM4_EVENTOUT
	PA8	MCO	TIM1_CH1	-	-	-	SPI2_SCK/ I2S2_CK	-	USART1_CK	-	-	-	-	-	-	LPTIM2_OUT	CM4_EVENTOUT
	PA9	-	TIM1_CH2	-	SPI2_NSS/ I2S2_WS	I2C1_SCL	SPI2_SCK/ I2S2_CK	-	USART1_TX	-	-	-	-	-	-	-	CM4_EVENTOUT
	PA10	RTC_REFIN	TIM1_CH3	-	-	I2C1_SDA	SPI2_MOSI/ I2S2_SD	-	USART1_RX	-	-	-	-	-	DEBUG_RF_HSE32RDY	TIM17_BKIN	CM4_EVENTOUT
	PA11	-	TIM1_CH4	TIM1_BKIN2	LPTIM3_ETR	I2C2_SDA	SPI1_MISO	-	USART1_CTS	-	-	-	-	TIM1_BKIN2	DEBUG_RF_NRESET	-	CM4_EVENTOUT

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Table 21. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2/ TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	RF	USART1 / USART2	LPUART1	-	-	-	COMP1/ COMP2/ TIM1	DEBUG	TIM2/ TIM16/ TIM17/ LPTIM2	EVENOUT
Port A (continued)	PA12	-	TIM1_ ETR	-	LPTIM3_ IN1	I2C2_ SCL	SPI1_ MOSI	RF_BUSY	USART1_ RTS	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	I2C2_ SMBA	-	-	-	IR_OUT	-	-	-	-	-	-	CM4_ EVENTOUT
	PA14	JTCK-SWCLK	LPTIM1_ OUT	-	-	I2C1_ SMBA	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PA15	JTDI	TIM2_ CH1	TIM2_ ETR	-	I2C2_ SDA	SPI1_ NSS	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
Port B	PB0	-	-	-	-	-	-	-	-	-	-	-	-	COMP1_ OUT	-	-	CM4_ EVENTOUT
	PB1	-	-	-	-	-	-	-	-	LPUART1_ RTS_DE	-	-	-	-	-	LPTIM2_ IN1	CM4_ EVENTOUT
	PB2	-	LPTIM1_ OUT	-	-	I2C3_ SMBA	SPI1_ NSS	-	-	-	-	-	-	-	DEBUG_RF_ SMPSRDY	-	CM4_ EVENTOUT
	PB3	JTDO/ TRACE SWO	TIM2_ CH2	-	-	-	SPI1_ SCK	RF_IRQ0	USART1_ RTS	-	-	-	-	-	DEBUG_RF_ DTB1	-	CM4_ EVENTOUT
	PB4	NJTRST	-	-	-	I2C3_ SDA	SPI1_ MISO	-	USART1_ CTS	-	-	-	-	-	DEBUG_RF_ LDORDY	TIM17_ BKIN	CM4_ EVENTOUT
	PB5	-	LPTIM1_ IN1	-	-	I2C1_ SMBA	SPI1_ MOSI	RF_IRQ1	USART1_ CK	-	-	-	-	COMP2_ OUT	-	TIM16_ BKIN	CM4_ EVENTOUT
	PB6	-	LPTIM1_ ETR	-	-	I2C1_ SCL	-	-	USART1_ TX	-	-	-	-	-	-	TIM16_ CH1N	CM4_ EVENTOUT
	PB7	-	LPTIM1_ IN2	-	TIM1_ BKIN	I2C1_ SDA	-	-	USART1_ RX	-	-	-	-	-	-	TIM17_ CH1N	CM4_ EVENTOUT
	PB8	-	TIM1_ CH2N	-	-	I2C1_ SCL	-	RF_IRQ2	-	-	-	-	-	-	-	TIM16_ CH1	CM4_ EVENTOUT
	PB9	-	TIM1_ CH3N	-	-	I2C1_ SDA	SPI2_ NSS/ I2S2_WS	-	-	IR_OUT	-	-	-	-	-	TIM17_ CH1	CM4_ EVENTOUT
	PB10	-	TIM2_ CH3	-	-	I2C3_ SCL	SPI2_ SCK/ I2S2_CK	-	-	LPUART1_ RX	-	-	-	COMP1_ OUT	-	-	CM4_ EVENTOUT

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Table 21. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2/ TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	RF	USART1 / USART2	LPUART1	-	-	-	COMP1/ COMP2/ TIM1	DEBUG	TIM2/ TIM16/ TIM17/ LPTIM2	EVENOUT
Port B (continued)	PB11	-	TIM2_CH4	-	-	I2C3_SDA	-	-	-	LPUART1_TX	-	-	-	COMP2_OUT	-	-	CM4_EVENTOUT
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C3_SMBA	SPI2_NSS/ I2S2_WS	-	-	LPUART1_RTS	-	-	-	-	-	-	CM4_EVENTOUT
	PB13	-	TIM1_CH1N	-	-	I2C3_SCL	SPI2_SCK/ I2S2_CK	-	-	LPUART1_CTS	-	-	-	-	-	-	CM4_EVENTOUT
	PB14	-	TIM1_CH2N	-	I2S2_MCK	I2C3_SDA	SPI2_MISO	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PB15	-	TIM1_CH3N	-	-	I2C2_SCL	SPI2_MOSI/ I2S2_SD	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT

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Table 21. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2S2/ TIM1/ LPTIM3	I2C1/ I2C2/ I2C3	SPI1/ SPI2S2	RF	USART1 / USART2	LPUART1	-	-	-	COMP1/ COMP2/ TIM1	DEBUG	TIM2/ TIM16/ TIM17/ LPTIM2	EVENOUT
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	-	-	LPUART1_RX	-	-	-	-	-	LPTIM2_IN1	CM4_EVENTOUT
	PC1	-	LPTIM1_OUT	-	SPI2_MOSI/ I2S2_SD	I2C3_SDA	-	-	-	LPUART1_TX	-	-	-	-	-	-	CM4_EVENTOUT
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI/ I2S2_SD	-	-	-	-	-	-	-	-	LPTIM2_ETR	CM4_EVENTOUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PC6	-	-	-	-	-	I2S2_MCK	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT
Port H	PH3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} and, for parameter values based on characterization results, measurements are performed on the UFQFPN48 package.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies, by tests in production on 100 % of the devices, with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = V_{BAT} = 3 V. Typical values are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95 % of the devices have an error less than or equal to the value indicated (mean ± 2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 12*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 13*.

Figure 12. Pin loading conditions

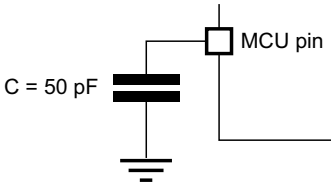
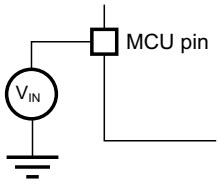


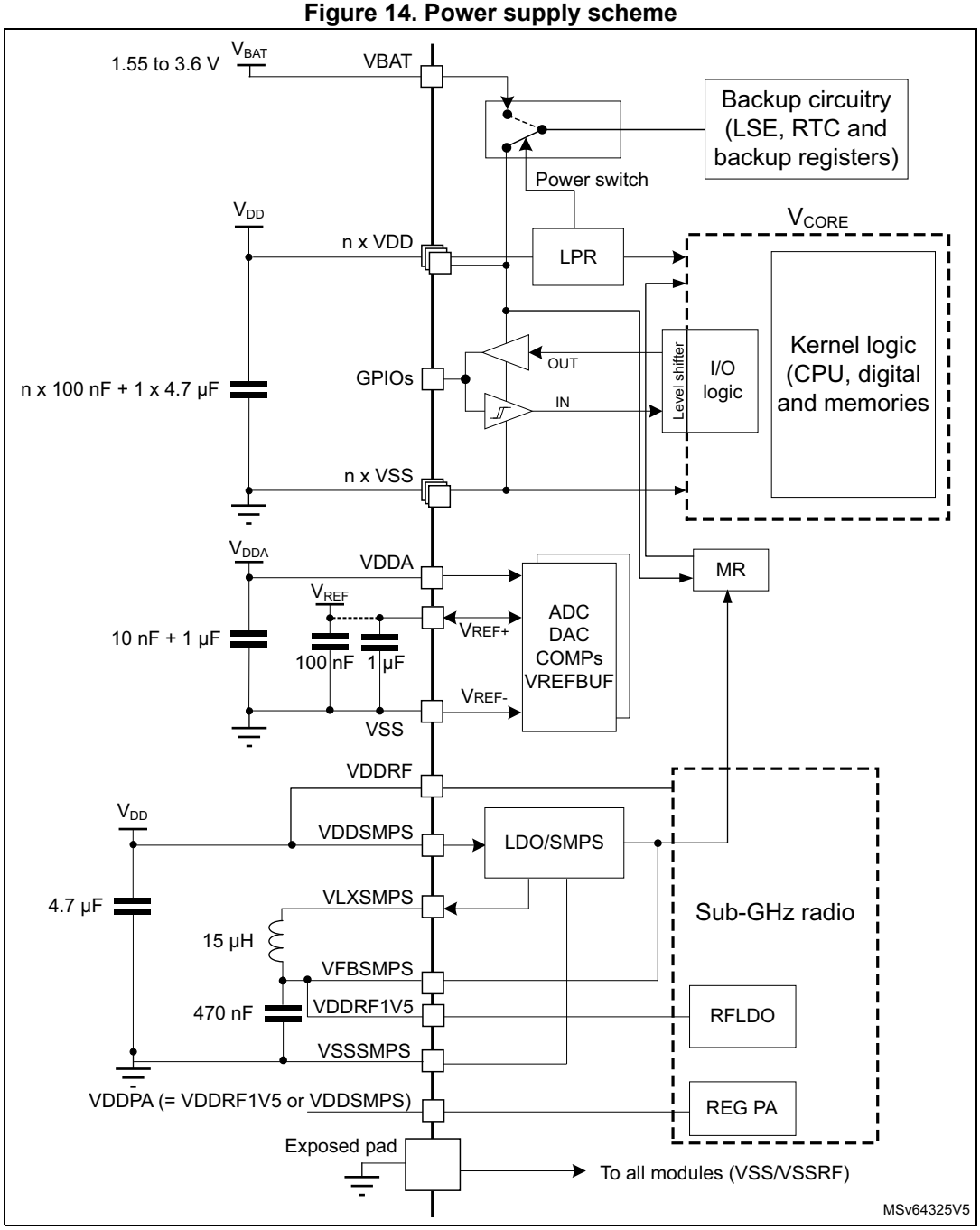
Figure 13. Pin input voltage



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5.1.6 Power supply scheme

Figure 14. Power supply scheme



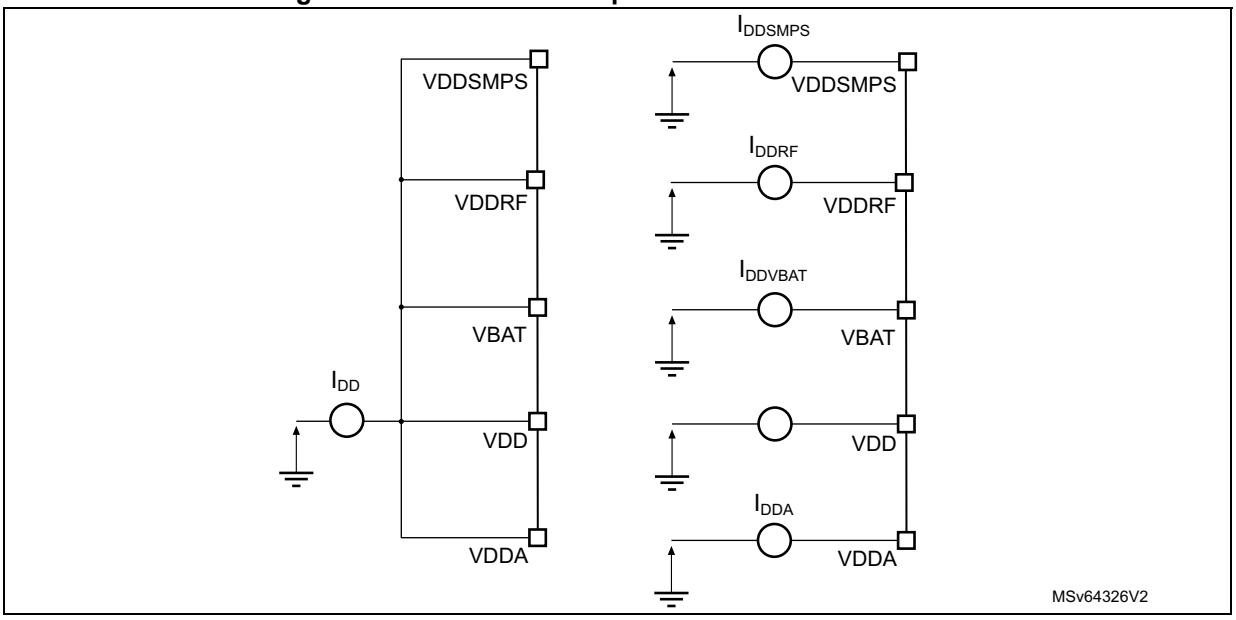
Caution: Each power supply pair (such as V_{DD}/V_{SS} or V_{DDA}/V_{SS}) must be decoupled with filtering ceramic capacitors as shown in the above figure. These capacitors must be placed as close as possible to (or below) the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Note: For the UFQFPN48 package, VREF+ is internally connected to VDDA.

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5.1.7 Current consumption measurement

Figure 15. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in the tables below, may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 22. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDRF}, V_{DDSMPS}, V_{BAT}, V_{REF+})	–0.3	3.9	V
V_{IN}(2)	Input voltage on FT_xx pins	V_{SS} - 0.3	min (V_{DD}, V_{DDA}, V_{DDRF}, V_{DDSMPS}) + 3.9(3)(4)	
	Input voltage on TT pins		3.9	
	Input voltage on any other pin		3.9	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(5)	-	50	
V_{REF+} - V_{DDA}	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V

1. All main power (VDD, VDDRF, VDDA, VBAT) and ground (VSS) pins must always be connected to the external power supply, in the permitted range.

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2. V_{IN} maximum must always be respected. Refer to the next table for the maximum allowed injected current values.
3. This formula must be applied only on the power supplies related to the I/O structure described in *Table 20: STM32WL55/54xx pin definition*.
4. To sustain a voltage higher than 4 V, the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 23. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)	130	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	130	
$IV_{DD(PIN)}$	Maximum current into each VDD power pin (source)(1)	130	
$IV_{SS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin, except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xx, TT and RST pins, except PB0	–5 / +0(4)	
	Injected current on PB0	-5/0	
$\sum\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)(5)	25	

1. All main power (VDD, VDDRF, VDDA, VBAT) and ground (VSS) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.
3. Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to the previous table for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 24. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	125	

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5.3 Operating conditions

5.3.1 Main performances

Table 25. Main performances at V_{DD} = 3 V

Parameter		Test conditions	Typ	Unit
I_{CORE}	Core current consumption	VBAT (V_{BAT} = 3V, V_{DD} = 0 V)	0.005	µA
		Shutdown	0.031	
		Standby (32-Kbyte RAM retention)	0.360	
		Stop 2, RTC enabled	1	
		Sleep (16 MHz)	770	
		LPRun (2 MHz)	220	
		Run, SMPS ON (48 MHz)	3450	
Rx boosted		LoRa 125 kHz, SMPS ON	4.82	mA
Tx low power		434 to 490 MHz, 14 dBm, 3.3 V	21	
		868 to 915 MHz, 14 dBm, 3.3 V	26	
Tx high power		434 to 490 MHz, 22 dBm, 3.3 V	110.5	
		868 to 915 MHz, 22 dBm, 3.3 V	120	

5.3.2 General operating conditions

Table 26. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-			
f_{PCLK2}	Internal APB2 clock frequency	-			
V_{DD}	Standard operating voltage	-	1.8(1)	3.6	V
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	
		DAC used	1.71		
		VREFBUF used	2.4		
		ADC, DAC, COMP and VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	
V_{FBSMPS}	SMPS feedback voltage	-	1.4	3.6	V
V_{DDRF}	Minimum RF voltage	-	1.8	3.6	
V_{IN}	I/O input voltage	TT I/O	–0.3	V_{DD} + 0.3	
		All I/O except TT	–0.3	min between min (V_{DD}, V_{DDA}) + 3.6 V and 5.5 V(2)(3)	

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Table 26. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6 version or T_A = 105 °C for suffix 7(4)	UFBGA73	-	392.0	mW
T_A	Ambient temperature for suffix 6 version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(5)		105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	–40	105	
		Low-power dissipation(5)		125	
T_J	Junction temperature range	Suffix 6 version	–40	105	°C
		Suffix 7 version		125	

1. When the reset is released, the functionality is guaranteed down to V_{BOR0} min.
2. This formula has to be applied only on the power supplies related to the I/O structure described in *Table 20: STM32WL55/54xx pin definition*. Maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}) + 3.6 V and 5.5 V.
3. For operation with voltage higher than min (V_{DD}, V_{DDA}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 102: Package thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range, as long as T_J does not exceed T_J max (see *Table 102: Package thermal characteristics*).

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5.3.3 Sub-GHz radio characteristics

Electrical characteristics of the sub-GHz radio are given with the following conditions unless otherwise specified:

- V_{DD} = 3.3 V. The current consumption is measured as described in *Figure 15*.
  I_{DD} includes current consumption of all supplies (V_{DDRF}, V_{DDSMPS}, V_{DD}, V_{DDA}, V_{BAT}).
  All peripherals except Sub-GHz radio are disabled and the system is in Standby mode.
- Temperature = 25 °C
- HSE32 = 32 MHz
- F_{RF} = 434/868/915 MHz
- All RF impedances matched using reference design
- Reference design implementing a 32 MHz crystal oscillator
- Transmit mode output power defined in 50 Ω load
- FSK BER (bit error rate) = 0.1 %, 2-level FSK modulation without pre-filtering, BR = 4.8 Kbit/s, FDA = 5 kHz, BW_F = 20 kHz
- LoRa PER (packet error rate) = 1 %, packet of 64 bytes, preamble of 8 bytes, error correction code CR = 4/5, CRC on payload enabled, no reduced encoding, no implicit header
- Sensitivities given using highest LNA gain step
- Power consumption measured with -140 dBm signal and AGC ON
- Blocking immunity, ACR and co-channel rejection, given for a single tone interferer and referenced to sensitivity +6 dB, blocking tests performed with unmodulated signal
- Bandwidth expressed on DSB (double-sided band)

Table 27. Operating range of RF pads

Pad	Description	Max	Unit
RFI_P/RFI_N	RF input power when in RX operation mode(1)	0	dBm
RFO_LP/RFO_HP/VR_PA	Voltage standing wave ratio (VSWR)	10:1	-

1. When not in RX operation mode (typically on DirectTie implementations), up to 22 dBm is accepted.

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Table 28. Sub-GHz radio power consumption

Symbol	Mode	Conditions		Min	Typ	Max	Unit
I_{DD}	Deep-Sleep mode (Sleep with cold start)(1)(2)	All blocks off		-	50	-	nA
	Sleep mode (with warm start)(2)(3)	Configuration retained		-	140	-	
		Configuration retained + RC64k		-	810	-	
	Sleep, LDO mode(4)	LDO, band-gap, RC 13 MHz on	HSE32 off	-	414	-	µA
			HSE32 on	-	564	-	
	Sleep, SMPS mode(4)	Band-gap, RC 13 MHz on, SMPS 40 mA max	HSE32 off	-	700	-	
			HSE32 on	-	950	-	
	Standby mode (RC 13 MHz on)	RC 13 MHz on, HSE32 off		-	0.7	-	mA
	Standby mode (HSE32)	SMPS mode	40 mA max settings	-	1.05	-	
		LDO mode		-	0.99	-	
	Synthesizer mode	SMPS mode used with 40 mA drive capability		-	2.66	-	
		LDO mode		-	4.05	-	
	Receive mode, SMPS mode used	SMPS 40 mA max	FSK 4.8 Kbit/s	-	4.47	-	mA
			LoRa 125 kHz	-	4.82	-	
			Rx boosted, FSK 4.8 Kbit/s	-	5.12	-	
			RX boosted, LoRa 125 kHz	-	5.46	-	
	Receive mode, LDO mode used	FSK 4.8 Kbit/s		-	8.18	-	
		LoRa 125 kHz			8.90		
		RX boosted	FSK 4.8 Kbit/s		9.52		
			LoRa 125 kHz		10.22		

1. Cold start is equivalent to device at POR or when the device wakes up from Sleep mode with all blocks off.
2. Only Sub-GHz radio power consumption.
3. Warm start only happens when the device wakes up from Sleep mode with its configuration retained,
4. System in Stop 0 mode range 2.

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Table 29. Sub-GHz radio power consumption in transmit mode

Symbol	Frequency band (MHz)	PA match (conditions)	Power output[1]	Typ	Unit
I_{DD}	868 to 915	Low power (optimized for 14 dBm)	+14 dBm, V_{DDRF} = 3.3 V	23.5	mA
			+10 dBm, V_{DDRF} = 3.3 V	17.5	
			+14 dBm, V_{DDRF} = 1.8 V	41.5	
			+10 dBm, V_{DDRF} = 1.8 V	28.5	
		Low power (optimal settings)[2]	+15 dBm, V_{DDRF} = 3.3 V	25.5	
			+10 dBm, V_{DDRF} = 3.3 V	15	
			+15 dBm, V_{DDRF} = 1.8 V	51	
			+10 dBm, V_{DDRF} = 1.8 V	25	
	434 to 490	Low power (optimized for 14 dBm)	+14 dBm, V_{DDRF} = 3.3 V	22.5	
			+10 dBm, V_{DDRF} = 3.3 V	13.5	
			+14 dBm, V_{DDRF} = 1.8	39.5	
			+10 dBm, V_{DDRF} = 1.8 V	22.5	
		Low power (optimal settings)	+15 dBm, V_{DDRF} = 3.3 V	24.5	
			+10 dBm, V_{DDRF} = 3.3 V	13.5	
			+15 dBm, V_{DDRF} = 1.8 V	43	
			+10 dBm, V_{DDRF} = 1.8 V	21.5	
	868 to 915	Low-power PA, SMPS OFF	+14 dBm, V_{DDRF} = 3.3 V	45.5	
	434 to 490			43.5	
	868 to 915	High power (optimized for 22 dBm)	+22 dBm, V_{DDRF} = 3.3 V	120	
			+20 dBm, V_{DDRF} = 3.3 V	107.5	
			+17 dBm, V_{DDRF} = 3.3 V	98	
			+14 dBm, V_{DDRF} = 3.3 V	92	
		High power (optimal settings)	+20 dBm, V_{DDRF} = 3.3 V	92.5	
			+17 dBm, V_{DDRF} = 3.3 V	58	
			+14 dBm, V_{DDRF} = 3.3 V	45.5	
	434 to 490	High power (optimized for 22 dBm)	+22 dBm, V_{DDRF} = 3.3 V	110.5	
			+20 dBm, V_{DDRF} = 3.3 V	90	
			+17 dBm, V_{DDRF} = 3.3 V	71	
			+14 dBm, V_{DDRF} = 3.3 V	59	
		High power (optimal settings)	+20 dBm, V_{DDRF} = 3.3 V	72	
			+17 dBm, V_{DDRF} = 3.3 V	43.5	
			+14 dBm, V_{DDRF} = 3.3 V	38	

1. These power outputs correspond to the settings programmed in the device. Depending on the board, up to 2 dB less than the setting are expected.
2. Optimal settings can be used to optimize power consumption when the output power is **NOT** 22 dBm (high power) or 14 dBm (low power). In that case, a dedicated firmware configuration associated to a dedicated board matching network (see AN5457 for details) corresponding to the custom output power, can be used.

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Table 30. Sub-GHz radio general specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Frequency synthesizer range	Low-power PA	150	-	960	MHz
FSTEP	Frequency synthesizer step	High-resolution mode HSE32 / $2^{(2)(5)}$	-	095	-	Hz
PHN(1) (2)	Synthesizer phase noise (868 to 915 MHz)	100 kHz offset	-	–100	-	dBc/Hz
		1 MHz offset	-	–120	-	
		10 MHz offset	-	–135	-	
TS_FS	Synthesizer wakeup time	From Standby, HSE32 mode	-	40	-	µs
TS_HOP	Synthesizer hop time	10 MHz step	-	40	-	
TS_OSC	Crystal oscillator wakeup time	From Standby, RC(3) normal mode from HSE32 off	-	170	-	
OSC_TRM	Crystal oscillator trimming range for crystal frequency error compensation(4)	Min/max XTAL specifications	±15	±30	-	ppm
BR_F	Bitrate, FSK	Programmable (min modulation index is 0.5)	0.6	-	300(5)	Kbit/s
FDA	Frequency deviation, FSK	Programmable (FDA + BR_F/2 ≤ 250 kHz)	0.6	-	200	kHz
BR_L	Bitrate, LoRa	Min for SF12, BW_L = 7.8 kHz Max for SF5, BW_L = 500 kHz	0.018	-	62.5(6)	Kbit/s
BW_L	Signal BW, LoRa	Programmable	7.8	-	500(6)	kHz
SF	Spreading factor for LoRa	Programmable, chips/symbol = 2^{SF}	5	-	12	-

1. Phase Noise specifications are given for the recommended PLL bandwidth to be used for the specific modulation/BR, optimized settings may be used for specific applications.
2. Phase Noise is not constant over frequency, due to the topology of the PLL. For two frequencies close to each other, the phase noise may change significantly
3. Wakeup time till crystal oscillator frequency is within ±10 ppm.
4. OSC_TRIM is the available trimming range to compensate for crystal initial frequency error and to allow crystal temperature compensation implementation. The total available trimming range is higher and allows the compensation for all device process variations
5. Maximum bit rate is assumed to scale with the RF frequency: for example 300 Kbit /s in the 869-to-915 MHz frequency band and only 50 Kbit/s at 150 MHz.
6. For RF frequencies below 400 MHz, there is a scaling between the frequency and supported bandwidth. Some bandwidths may not be available below 400 MHz.

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Table 31. Sub-GHz radio receive mode specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
RXS_2FB	Sensitivity 2-FSK, RX boosted gain, split RF paths for RX and Tx, RF switch insertion loss excluded	BR = 0.6 Kbit/s, FDA = 0.8 kHz, BW = 4 kHz	-	–125	-	dBm
		BR = 1.2 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	–123	-	
		BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	–117	-	
		BR = 38.4 Kbit/s, FDA = 40 kHz, BW = 160 kHz	-	–108	-	
		BR = 250 Kbit/s, FDA = 125 kHz, BW = 500 kHz	-	–103	-	
RXS_LB	Sensitivity LoRa, RX boosted gain, split RF paths for RX and Tx, RF switch insertion loss excluded	BW = 10.4 kHz, SF = 7	-	–135	-	
		BW = 10.4 kHz, SF = 12	-	–148	-	
		BW = 125 kHz, SF = 7	-	–125	-	
		BW = 125 kHz, SF = 12	-	–138	-	
		BW = 250 kHz, SF = 7	-	–122	-	
		BW = 250 kHz, SF = 12	-	–135	-	
		BW = 500 kHz, SF = 7	-	–118	-	
		BW = 500 kHz, SF = 12	-	–130	-	
RSX_2F	Sensitivity 2-FSK, RX power saving gain with direct tie connection between RX and Tx	BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	–115	-	
RXS_L	Sensitivity LoRa, RX power saving gain with direct tie connection between RX and Tx	BW = 125 kHz, SF = 12	-	–135	-	
CCR_F	Co-channel rejection, FSK	-	-	–9	-	dB
CCR_L	Co-channel rejection, LoRa	SF = 7	-	7	-	
		SF = 12	-	19	-	
ACR_F	Adjacent channel rejection, FSK	Offset = ±50 kHz	-	44	-	
ACR_L	Adjacent channel rejection, LoRa	Offset = ±1.5 x BW_L, BW = 125 kHz, SF = 7	-	60	-	
		Offset = ±1.5 x BW_L, BW = 125 kHz, SF = 12	-	71	-	
BI_F	Blocking immunity, FSK	Offset = ±1 MHz, BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	67	-	
		Offset = ±2 MHz, BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	70	-	
		Offset = ±10 MHz, BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	76	-	

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Table 31. Sub-GHz radio receive mode specifications (continued)

Symbol	Description	Conditions	Min	Typ	Max	Unit
BI_L	Blocking immunity, LoRa	Offset = ±1 MHz, BW = 125 kHz, SF = 12	-	87	-	dB
		Offset = ±2 MHz, BW = 125 kHz, SF = 12	-	91	-	
		Offset = ±10 MHz, BW = 125 kHz, SF = 12	-	96	-	
IIP3	Third order input intercept point	Unwanted tones are 1 MHz and 1.96 MHz above LO. 868 to 915 MHz band	-	–9	-	dBm
		Unwanted tones are 1 MHz and 1.96 MHz above LO. 433 MHz band	-	–15	-	
IMA	Image attenuation	Without IQ calibration	-	30	-	dB
		With IQ calibration	-	54	-	
BW_F	DSB channel filter BW, FSK	Programmable, typical values	4.8	-	467	kHz
TS_RX	Receiver wakeup time	FS to RX	-	41	-	µs
FERR_L	Maximum tolerated frequency offset between transmitter and receiver, SF7 to SF12	All bandwidths, ±25 % of BW. The tighter limit between this line and the three lines below applies.	-	±25	-	BW
	Maximum tolerated frequency offset between transmitter and receiver, SF10 to SF12	SF12	–50	-	50	ppm
		SF11	–100	-	100	
		SF10	–200	-	200	

Table 32. Sub-GHz radio transmit mode specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
TXOP	Max RF output power	Highest power step setting for low-power PA (LP PA)	-	+15(1)	-	dBm
		Highest power step setting for high-power PA (HP PA)	-	+22	-	
TXDRP	RF output power drop versus supply voltage	LP PA, under SMPS or LDO VDDop range from 1.8 to 3.7 V	-	0.5	-	dB
		HP PA, +22 dBm, V_{DD} = 2.7 V	-	2	-	
		HP PA, +22 dBm, V_{DD} = 2.4 V	-	3	-	
		HP PA, +22 dBm, V_{DD} = 1.8 V	-	6	-	
TXPRNG	RF output power range	Programmable in 31 steps, typical value	TXOP-31	-	TXOP	dBm
TXACC	RF output power step accuracy	-	-	±2	-	dB

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Table 32. Sub-GHz radio transmit mode specifications (continued)

Symbol	Description	Conditions	Min	Typ	Max	Unit
TXRMP	PA ramping time	Programmable	10	-	3400	µs
TS_TX	TX wakeup time	Frequency synthesizer enabled	-	36 + PA ramping	-	

1. For low-power PA, +15 dBm maximum RF output power can be reached with optimal settings.

Table 33. Sub-GHz radio power management specifications

Symbol	Description	Conditions	Frequency (MHz)			Unit
			470	490	868	
TRPOR	Required POR reset pulse duration	For V_{DD} ≥ 1.8 V	50	100	-	µs
VEOLL	End-of-life low-threshold voltage	-	1.81	1.89	1.96	V
VEOLH	End-of-life high-threshold voltage	-	1.86	1.94	2.1	
VEOLD	End-of-life hysteresis voltage	VEOLH - VEOLL	50	53	56	mV
VREG	Main regulated supply	LDO or SMPS over process, voltage and temperature range	1.47	1.55	1.62	V
LDTRSMPS	Load transient for ILSMPS 100 µA to 100 mA in 10 µs LDO running	High BW mode	-	25	-	mV
		Low BW mode	-	47	-	
ILSMPS	SMPS load current	-	-	-	100	mA
IDDSMPS	SMPS quiescent current	SMPS high power, V_{DD} = 3.3 V	-	538	-	µA
		SMPS low power, V_{DD} = 3.3 V	-	460	-	
EFFSMPS	SMPS converter average efficiency EFF = VREG x ILOAD / V_{DDSMPS} x IDD	SMPS 100 mA max V_{DD} = 3.3 V, ILSMPS = 6 mA	-	71	-	%
		SMPS 100 mA max V_{DD} = 3.3 V, ILSMPS = 50 mA	-	89	-	
		SMPS 100 mA max V_{DD} = 1.8 V, ILSMPS = 6 mA	-	88	-	
		SMPS 100 mA max V_{DD} = 2.0 V, ILSMPS = 50 mA	-	91	-	
		SMPS 100 mA max V_{DD} = 3.3 V, ILSMPS = 100 mA	-	86	-	
Cout	Shared between LDO and SMPS	±20 % tolerance	-	470	-	nF
Lout	SMPS inductor	-	-	15	-	µH
TSSMPS	Sleep and Sleep, SMPS startup time	For ILIM = 50 mA	-	70	-	µs

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Table 33. Sub-GHz radio power management specifications (continued)

Symbol	Description	Conditions	Frequency (MHz)			Unit
			470	490	868	
IDDLDO	LDO quiescent current	V_{DD} = 3.3 V, ILOAD = 0 to 100 mA, current limiter off	-	95	-	µA
		V_{DD} = 3.3 V, ILOAD = 100 mA, current limiter on	-	380	-	
		V_{DD} = 3.3 V, ILOAD = 50 mA, current limiter on	-	280	-	
ILDO	LDO load current	-	-	100	-	mA
LDTRLDO	Load transient for ILDO 100 µA to 100 mA in 10 µs	-	-	25	-	mV
TSLDO	Sleep and Sleep, LDO startup time	For ILIM = 50 mA	-	60	-	µs
VDIG	Digital regulator target voltage	-	1.14	1.2	1.26	V
ILM(1)	Current limiter max value	-	25	50	200	mA

1. The default current limiter value is set to 50 mA.

5.3.4 Operating conditions at power-up/power-down

Parameters given in the table below are derived from tests performed under the ambient temperature condition summarized in *Table 26: General operating conditions*.

Table 34. Operating conditions at power-up/power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	∞	µs/V
	V_{DD} fall time rate	10	∞	
t_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
t_{VDDRF}	V_{DDRF} rise time rate	-	∞	
	V_{DDRF} fall time rate	-	∞	

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5.3.5 Embedded reset and power-control block characteristics

Parameters given in the table below are derived from tests performed under the ambient temperature conditions summarized in *Table 26: General operating conditions*.

Table 35. Embedded reset and power-control block characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$t_{RSTTEMPO}$[2]	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}[2]	Brownout reset threshold 0	Rising edge	1.72	1.76	1.80	V
		Falling edge	1.70	1.74	1.78	
V_{BOR1}	Brownout reset threshold 1	Rising edge	2.06	2.10	2.14	
		Falling edge	1.96	2.00	2.04	
V_{BOR2}	Brownout reset threshold 2	Rising edge	2.26	2.31	2.35	
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brownout reset threshold 3	Rising edge	2.56	2.61	2.66	
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brownout reset threshold 4	Rising edge	2.85	2.90	2.95	
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	1.88	1.95	2.02	
		Falling edge	1.83	1.90	1.97	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA

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Table 35. Embedded reset and power-control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
I_{DD} (PVM3)[2]	PVM3 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run and Sleep modes, or temperature sensor enable in LPRun and LPSleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except Shutdown) and its consumption is therefore included in the supply current characteristics tables.

5.3.6 Embedded voltage reference

Parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 26: General operating conditions*.

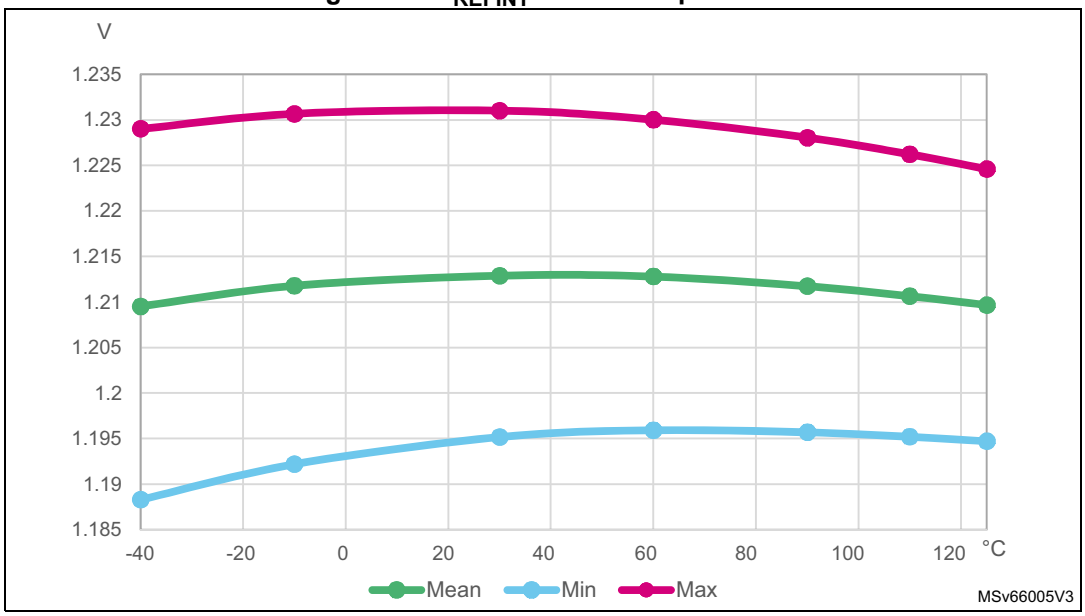
Table 36. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_J < +105 °C	1.182	1.212	1.232	V
$t_{S_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3.3 V	-	5	7.5(2)	mV
T_{Coeff}	Temperature coefficient	–40 °C < T_J < +105 °C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25 °C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

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Figure 16. V_{REFINT} versus temperature



5.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 15*.

Typical and maximum current consumption

The device is put under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled, except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait-states number, depending on the f_{HCLK} frequency. Refer to the table 'Number of wait states according to flash clock (HCLK3) frequency' in the reference manual (RM0461).
- $f_{PCLK} = f_{HCLK}$ when the peripherals are enabled.
- $f_{PCLK} = f_{HCLK} = f_{HCLKS}$ for the flash memory and shared peripherals.

Parameters given in the tables below (*Table 37* to *Table 56*) are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 26: General operating conditions*.

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Table 37. Current consumption in Run and LPRun modes on CPU1, CoreMark code with data running from flash memory, ART enable (cache ON, prefetch OFF)

Symbol	Parameter	Conditions			Typ				Max(1)			Unit
		-	Voltage scaling	f_{HCLK} (MHz)	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	Range 2	16	1.85	1.90	1.95	2.10	2.20	2.40	2.80	mA
				8	1.10	1.15	1.20	1.30	1.40	1.60	1.90	
				2	0.585	0.610	0.670	0.760	-	-	-	
			SMPS Range 2	16	1.50	1.45	1.65	1.70	-	-	-	
				8	1.00	1.05	1.05	1.10	-	-	-	
				2	0.730	0.750	0.780	0.830	-	-	-	
			Range 1	48	5.55	5.65	5.80	5.95	7.40	11.0	14.0	
				32	3.85	3.95	4.05	4.20	5.60	8.40	13.0	
				16	2.15	2.20	2.30	2.45	3.70	6.60	11.0	
			SMPS Range 1	48	3.40	3.45	3.55	3.60	-	-	-	
				32	2.50	2.55	2.60	2.65	-	-	-	
				16	1.60	1.60	1.65	1.70	-	-	-	
I_{DD} (LPRun)	Supply current in LPRun mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled		2	0.220	0.235	0.290	0.380	0.270	0.490	0.880	
				1	0.120	0.135	0.185	0.275	0.150	0.390	0.780	
				0.4	0.058	0.0715	0.120	0.210	0.084	0.330	0.710	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 38. Current consumption in Run and LPRun modes on CPU1 and CPU2, CoreMark code with data running from SRAM1

Symbol	Parameter	Conditions			Typ				Unit
		-	Voltage scaling	f_{HCLK} (MHz)	25 °C	55 °C	85 °C	105 °C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	Range 2	16	2.5	2.55	2.65	2.75	mA
			Range 1	48	8.00	8.15	8.35	8.55	
				32	5.80	5.90	6.05	6.25	
			SMPS Range 1	48	4.75	4.85	4.95	5.00	
				32	3.50	3.60	3.65	3.75	
				16	2.20	2.25	2.30	2.40	
I_{DD} (LPRun)	Supply current in LPRun mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled		2	0.350	-	-	-	
				1	0.185	-	-	-	
				0.4	0.0805	-	-	-	

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Table 39. Current consumption in Run and LPRun modes on CPU1, CoreMark code with data running from SRAM1

Symbol	Parameter	Conditions			Typ				Max(1)			Unit
		-	Voltage scaling	f_{HCLK} (MHz)	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	Range 2	16	1.90	1.90	2.00	2.10	2.20	2.40	2.80	mA
				8	1.10	1.15	1.20	1.30	1.40	1.60	2.00	
				2	-	-	-	-	-	-	-	
			SMPS Range 2	16	1.40	1.45	1.50	1.55	-	-	-	
				8	1.00	1.05	1.05	1.10	-	-	-	
				2	0.730	0.750	0.780	0.825	-	-	-	
			Range 1	48	5.65	5.75	5.90	6.05	6.50	6.70	7.10	
				32	3.90	4.00	4.10	4.25	4.60	4.80	5.20	
				16	2.20	2.25	2.30	2.45	2.50	2.80	3.20	
			SMPS Range 1	48	3.45	3.50	3.60	3.65	-	-	-	
				32	2.50	2.55	2.60	2.70	-	-	-	
				16	1.60	1.60	1.65	1.70	-	-	-	
I_{DD} (LPRun)	Supply current in LPRun mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled		2	0.220	0.230	0.285	0.375	0.240	0.480	0.860	
				1	0.120	0.130	0.180	0.270	0.140	0.380	0.770	
				0.4	0.052	0.064	0.115	0.205	0.077	0.320	0.710	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 40. Typical current consumption in Run and LPRun modes on CPU1, with different codes running from flash memory, ART enable (cache ON, prefetch OFF)

Symbol	Parameter	Conditions			Typ	Unit	Typ	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	Range 2 f_{HCLK} = 16 MHz	Reduced code	1.90	mA	118.75	µA/MHz
				CoreMark(1)	1.85		115.63	
				Dhrystone 2.1	1.85		115.63	
				Fibonacci	1.80		112.50	
				While(1)	1.60		100.00	
			SMPS Range 2 f_{HCLK} = 16 MHz	Reduced code	1.45		90.63	
				CoreMark(1)	1.40		87.50	
				Dhrystone 2.1	1.40		87.50	
				Fibonacci	1.40		87.50	
				While(1)	1.30		81.25	
			Range 1 f_{HCLK} = 48 MHz	Reduced code	5.70		118.75	
				CoreMark(1)	5.55		115.63	
				Dhrystone 2.1	5.50		114.58	
				Fibonacci	5.40		112.50	
				While(1)	4.65		96.88	
			SMPS Range 1 f_{HCLK} = 48 MHz	Reduced code	3.50		72.92	
				CoreMark(1)	3.40		70.83	
				Dhrystone 2.1	3.40		70.83	
				Fibonacci	3.30		68.75	
				While(1)	2.90		60.42	

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Table 40. Typical current consumption in Run and LPRun modes on CPU1, with different codes running from flash memory, ART enable (cache ON, prefetch OFF) (continued)

Symbol	Parameter	Conditions			Typ	Unit	Typ	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(LPRun)	Supply current in LPRun mode	$f_{HCLK} = f_{MSI}$ = 2 MHz All peripherals disabled		Reduced code	0.225	mA	112.50	µA/MHz
				CoreMark(1)	0.220		110.00	
				Dhrystone 2.1	0.220		110.00	
				Fibonacci	0.240		120.00	
				While(1)	0.175		87.50	

1. CoreMark used for characterization results provided in *Table 37* and *Table 40*.

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Table 41. Typical current consumption in Run and LPRun modes on CPU1, with different codes running from SRAM1

Symbol	Parameter	Conditions			Typ	Unit	Typ	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	Range 2 f_{HCLK} = 16 MHz	Reduced code	1.95	mA	121.88	µA/MHz
				CoreMark(1)	1.90		118.75	
				Dhrystone 2.1	1.90		118.75	
				Fibonacci	1.90		118.75	
				While(1)	1.75		109.38	
			Range 2 SMPS ON f_{HCLK} = 16 MHz	Reduced code	1.45		90.63	
				CoreMark(1)	1.45		90.63	
				Dhrystone 2.1	1.45		90.63	
				Fibonacci	1.45		90.63	
				While(1)	1.35		84.38	
			Range 1 f_{HCLK} = 48 MHz	Reduced code	5.90		122.92	
				CoreMark(1)	5.65		117.71	
				Dhrystone 2.1	5.70		118.75	
				Fibonacci	5.65		117.71	
				While(1)	5.10		106.25	
			Range 1 SMPS ON f_{HCLK} = 48 MHz	Reduced code	3.60		75.00	
				CoreMark(1)	3.45		71.88	
				Dhrystone 2.1	3.50		72.92	
				Fibonacci	3.45		71.88	
				While(1)	3.15		65.63	

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Table 41. Typical current consumption in Run and LPRun modes on CPU1, with different codes running from SRAM1 (continued)

Symbol	Parameter	Conditions			Typ	Unit	Typ	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(LPRun)(2)	Supply current in LPRun mode	$f_{HCLK} = f_{MSI}$ = 2 MHz All peripherals disabled		Reduced code	0.225	mA	112.50	µA/MHz
				CoreMark(1)	0.220		110.00	
				Dhrystone 2.1	0.225		112.50	
				Fibonacci	0.225		112.50	
				While(1)	0.195		97.50	

1. CoreMark used for characterization results provided in *Table 37* and *Table 40*.
2. Flash memory in power-down mode.

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Table 42. Current consumption in Sleep and LPSleep modes on CPU1, flash memory ON

Symbol	Parameter	Conditions			Typ				Max(1)			Unit
		-	Voltage scaling	f_{HCLK} (MHz)	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD}(Sleep)	Supply current in Sleep mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	Range 2	16	0.770	0.800	0.860	0.955	1.00	1.30	1.60	mA
				8	0.570	0.600	0.655	0.745	0.780	0.990	1.40	
				2	0.445	0.470	0.525	0.615	0.650	0.860	1.30	
			Range 1	48	1.70	1.70	1.80	1.90	2.10	2.30	2.70	
				32	1.25	1.30	1.40	1.50	1.60	1.90	2.30	
				16	0.845	0.875	0.945	1.05	1.10	1.40	1.80	
			SMPS Range 1	48	1.35	1.40	1.45	1.50	-	-	-	
				32	1.15	1.15	1.20	1.25	-	-	-	
				16	0.895	0.915	0.950	1.00	-	-	-	
I_{DD}(LPSleep)	Supply current in LPSleep mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled		2	0.068	0.0805	0.130	0.220	0.095	0.330	0.720	
				1	0.044	0.0565	0.105	0.195	0.069	0.310	0.700	
				0.4	0.0225	0.040	0.0885	0.180	0.052	0.290	0.680	
				0.1	0.018	0.032	0.081	0.170	0.045	0.280	0.670	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 43. Current consumption in Sleep and LPSleep modes on CPU1 and CPU2, flash memory ON

Symbol	Parameter	Conditions			Typ	Unit
		-	Voltage scaling	f_{HCLK} (MHz)	25 °C	
I_{DD}(Sleep)	Supply current in Sleep mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled	Range 2	16	0.790	mA
				8	0.585	
				2	0.450	
			Range 1	48	1.75	
				32	1.30	
				16	0.870	
			SMPS Range 1	48	1.40	
				32	1.15	
				16	0.905	
I_{DD}(LPSleep)	Supply current in LPSleep mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled		0.1	0.0165	

Table 44. Current consumption in LPSleep mode on CPU1, flash memory in power-down

Symbol	Parameter	Conditions		Typ				Max(1)			Unit
		-	f_{HCLK} (MHz)	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD} (LPSleep)	Supply current in LPSleep mode	$f_{HCLK} = f_{MS}$ All peripherals disabled	2	58.0	74.5	125	215	86.0	330	710	µA
			1	35.5	50.5	99.0	190	60.0	300	690	
			0.4	18.5	33.5	81.5	170	41.0	280	670	
			0.1	11.0	26.5	74.5	165	36.0	280	660	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 45. Current consumption in LPSleep mode on CPU1 and CPU2, flash memory in power-down

Symbol	Parameter	Conditions		Typ	Unit
		-	f_{HCLK} (MHz)	25 °C	
I_{DD}(LPSleep)	Supply current in LPSleep mode	$f_{HCLK} = f_{MS}$ All peripherals disabled	2	59.5	µA
			1	36.0	
			0.4	21.5	
			0.1	12.5	

Table 46. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions	Typ					Max(1)				Unit
		V_{DD} (V)	0 °C	25 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Stop 2)	Supply current in Stop 2 mode RTC disabled	1.8	0.545	0.830	2.45	8.45	13.5	1.20	2.20	24.0	66.0	µA
		2.4	0.525	0.850	2.60	8.80	14.0	-	-	-	-	
		3.0	0.605	0.885	2.80	9.25	14.5	1.10	2.60	26.0	69.0	
		3.6	0.630	0.935	3.10	9.75	15.5	1.40	2.80	26.0	71.0	
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode RTC enabled, clocked by LSI(2)	1.8	0.650	0.880	2.55	8.25	13.5	1.30	2.30	24.0	66.0	
		2.4	0.630	0.945	2.70	8.85	14.0	-	-	-	-	
		3.0	0.715	1.00	2.90	9.70	15.0	1.40	2.80	26.0	69.0	
		3.6	0.750	1.10	3.15	10.5	15.5	1.50	3.00	26.0	71.0	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. LSI using LSIPRE = 1 configuration.

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Table 47. Current consumption during wakeup from Stop 2 mode

Conditions	Typ at 25 °C				Unit
	V_{DD} = 1.8 V	V_{DD} = 2.4 V	V_{DD} = 3.0 V	V_{DD} = 3.6 V	
Wakeup clock: MSI 4 MHz, voltage range 2	2.93	3.22	3.45	4.79	nAs
Wakeup clock: MSI 2 MHz, voltage range 2	4.44	5.03	5.82	7.36	
Wakeup clock: MSI 4 MHz, voltage range 1	3.03	3.14	3.51	4.66	
Wakeup clock: MSI 16 MHz, voltage range 1	1.75	1.95	2.00	3.06	
Wakeup clock: MSI 48 MHz, voltage range 1	1.75	1.82	1.89	2.80	

Table 48. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions	Typ					Max(1)				Unit
		V_{DD} (V)	0 °C	25 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode RTC disabled	1.8	2.05	4.00	14.0	47.0	74.5	6.10	20.0	200	480	µA
		2.4	2.15	3.95	14.0	47.0	75.0	-	-	-	-	
		3.0	2.15	4.15	14.0	47.5	75.5	5.90	20.0	200	490	
		3.6	2.25	4.20	14.0	48.0	76.5	6.20	20.0	200	490	
I_{DD} (Stop 1with RTC)	Supply current in Stop 1 mode RTC enabled, clocked by LSI(2)	1.8	2.15	4.10	14.0	47.0	75.0	6.30	20.0	200	480	
		2.4	2.15	4.10	14.0	47.5	75.5	-	-	-	-	
		3.0	2.25	4.20	14.0	47.5	76.0	6.40	21.0	200	490	
		3.6	2.30	4.15	14.5	48.5	77.0	6.70	21.0	200	490	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. LSI using LSIPRE = 1 configuration.

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Table 49. Current consumption during wakeup from Stop 1 mode

Conditions	Typ at 25 °C				Unit
	V_{DD} = 1.8 V	V_{DD} = 2.4 V	V_{DD} = 3.0 V	V_{DD} = 3.6 V	
Wakeup clock: MSI 4 MHz, voltage range 2	1.05	1.15	1.09	1.18	nAs
Wakeup clock: MSI 2 MHz, voltage range 2	1.81	1.81	2.12	2.40	
Wakeup clock: MSI 4 MHz, voltage range 1	0.766	1.23	1.34	1.49	
Wakeup clock: MSI 16 MHz, voltage range 1	0.310	0.71	0.935	0.836	
Wakeup clock: MSI 48 MHz, voltage range 1	0.0707	0.461	0.533	0.565	

Table 50. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		Typ					Max(1)				Unit
		-	V_{DD} (V)	0 °C	25 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Stop 0)	Supply current in Stop 0 mode RTC disabled		1.8	335	345	365	415	455	480	500	740	1200	µA
			2.4	360	370	395	445	485	-	-	-	-	
			3.0	390	400	425	475	515	540	570	800	1200	
			3.6	425	435	460	515	550	580	600	840	1300	

1. Guaranteed based on test during characterization, unless otherwise specified.

Table 51. Current consumption during wakeup from Stop 0 mode

Conditions	Typ at 25 °C				Unit
	V_{DD} = 1.8 V	V_{DD} = 2.4 V	V_{DD} = 3.0 V	V_{DD} = 3.6 V	
Wakeup clock: MSI 4 MHz, voltage range 2	3.45	3.76	3.45	4.04	nAs
Wakeup clock: MSI 2 MHz, voltage range 2	3.05	3.20	3.74	3.35	
Wakeup clock: MSI 4 MHz, voltage range 1	3.20	3.25	3.30	4.11	
Wakeup clock: MSI 16 MHz, voltage range 1	1.07	1.25	1.71	1.80	
Wakeup clock: MSI 48 MHz, voltage range 1	0.867	1.13	1.39	0.949	

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Table 52. Current consumption in Standby mode

Symbol	Parameter	Conditions		Typ					Max(1)				Unit
		-	V_{DD} (V)	0 °C	25 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Standby)	Supply current in Standby mode RTC disabled Backup registers retained	No retention	1.8	0.009	0.027	0.245	1.00	2.40	-	-	-	-	µA
			2.4	0.022	0.051	0.340	1.35	2.85	-	-	-	-	
			3.0	0.046	0.071	0.470	1.75	3.40	-	-	-	-	
			3.6	0.075	0.125	0.650	2.30	4.05	-	-	-	-	
		SRAM2 retained	1.8	0.130	0.205	0.820	2.90	5.55	0.200	0.550	8.20	24.0	
			2.4	0.140	0.225	0.915	3.25	6.05	-	-	-	-	
			3.0	0.165	0.255	1.05	3.70	6.60	0.280	0.710	9.40	27.0	
			3.6	0.190	0.300	1.20	4.25	7.25	0.330	0.770	10.0	28.0	
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers and SRAM2 retained) RTC enabled	RTC clocked by LSI (PREDIV = 1)	1.8	0.215	0.295	0.895	3.10	5.30	-	-	-	-	
			2.4	0.230	0.325	0.990	3.45	5.95	-	-	-	-	
			3.0	0.260	0.360	1.15	3.95	6.85	-	-	-	-	
			3.6	0.305	0.425	1.30	4.55	7.85	-	-	-	-	
		RTC clocked by LSE quartz(2) in low drive mode	1.8	0.270	0.350	0.975	3.15	5.80	-	-	-	-	
			2.4	0.295	0.390	1.10	3.50	6.25	-	-	-	-	
			3.0	0.345	0.445	1.25	4.00	6.85	-	-	-	-	
			3.6	0.415	0.535	1.45	4.60	7.55	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 53. Current consumption during wakeup from Standby mode

Symbol	Conditions	Typ at 25 °C				Unit
		V_{DD} = 1.8 V	V_{DD} = 2.4 V	V_{DD} = 3.0 V	V_{DD} = 3.6 V	
I_{DD} (wakeup from Standby)	Wakeup clock: MSI 4 MHz	23.5	81.3	111	114	nAs
	Wakeup clock: MSI 8 MHz	15.2	15.7	17.3	19.6	

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Table 54. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		Typ					Max(1)				Unit
		-	V_{DD} (V)	0 °C	25 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Shutdown)	Supply current in Shutdown mode RTC disabled Backup registers retained		1.8	0.001	0.008	0.105	0.380	0.995	0.001	0.043	1.70	6.40	µA
			2.4	0.008	0.018	0.135	0.445	1.20	-	-	-	-	
			3.0	0.018	0.031	0.180	0.545	1.45	0.078	0.150	2.40	8.50	
			3.6	0.041	0.062	0.260	0.690	1.80	0.110	0.190	2.90	9.90	
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by an external clock	1.8	0.054	0.065	0.145	0.545	1.35	-	-	-	-	
			2.4	0.090	0.105	0.200	0.665	1.60	-	-	-	-	
			3.0	0.160	0.175	0.295	0.860	1.95	-	-	-	-	
			3.6	0.250	0.280	0.440	1.15	2.45	-	-	-	-	
		RTC clocked by LSE quartz (2) in low drive mode	1.8	0.140	0.155	0.270	0.605	1.20	-	-	-	-	
			2.4	0.165	0.185	0.315	0.705	1.40	-	-	-	-	
			3.0	0.205	0.225	0.380	0.855	1.70	-	-	-	-	
			3.6	0.265	0.295	0.500	1.10	2.10	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

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Table 55. Current consumption in VBAT mode

Symbol	Parameter	Conditions		Typ					Max	Unit
		-	V_{BAT} (V)	0 °C	25 °C	55 °C	85 °C	105 °C	105 °C	
I_{DD}(VBAT)	Backup domain supply current	RTC disabled	1.8	1.00	3.00	19.0	95.0	180	1.00	nA
			2.4	1.00	3.00	22.0	110	200	1.00	
			3.0	1.00	5.00	31.0	150	270	1.00	
			3.6	3.00	11.0	50.0	220	380	3.00	
		RTC enabled and clocked by LSE quartz(1)	1.8	140	150	180	275	390	140	
			2.4	155	170	200	310	435	155	
			3.0	185	200	235	375	545	185	
			3.6	230	245	295	485	710	230	

1. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 56. Current under Reset condition

Symbol	Conditions	Typ	Unit
	V_{DD} (V)	25 °C	
I_{DD}(RST)	1.8 V	600	µA
	2.4 V	650	
	3.0 V	700	
	3.6 V	780	

I/O system current consumption

The current consumption of the I/O system has two components: a static and a dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 76: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, these pins must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 57: Peripheral current consumption*, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load.
- V_{DD} is the I/O supply voltage.
- f_{SW} is the I/O switching frequency.
- C is the total capacitance seen by the I/O pin: $C = C_{Io} + C_{EXT}$.
- C_{EXT} is the PCB board capacitance plus any connected external device pin capacitance.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

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On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the table below. The device is placed under the following conditions:

- All I/O pins are in analog mode.
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 22: Voltage characteristics*.
- The power consumption of the digital part of the on-chip peripherals is given in the table below. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 57. Peripheral current consumption

Peripheral		Range 1	Range 2	LPRun and LPSleep	Unit
AHB1	CRC1	0.42	0.38	1.00	µA/MHz
	DMA1	2.29	1.88	1.45	
	DMA2	2.50	1.94	1.50	
	DMAMUX1	3.96	3.38	2.50	
	All AHB1 peripherals	9.17	7.50	9.30	
AHB2	GPIOA	0.01	0.12	0.20	µA/MHz
	GPIOB	0.01	0.12	0.15	
	GPIOC	0.01	0.12	0.15	
	GPIOH	0.01	0.06	0.10	
	All AHB2 peripherals	0.62	0.56	0.40	
AHB3	AES1	2.50	2.13	1.80	µA/MHz
	FLASH	7.92	6.56	11.3	
	PKA	3.33	2.75	2.15	
	RNG1	1.04	N/A	N/A	
	RNG1 independent clock domain	0.62	N/A	N/A	
	SRAM1	0.62	0.38	0.55	
	SRAM2	0.42	0.37	0.50	
	All AHB3 peripherals(1)	16.0	13.4	16.0	
APB1	DAC	0.83	0.69	0.50	µA/MHz
	I2C1	1.67	1.37	1.05	
	I2C1 independent clock domain	2.29	1.94	1.40	
	I2C2	1.67	1.37	1.05	
	I2C2 independent clock domain	2.50	2.00	1.60	
	I2C3	1.67	1.37	0.90	

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Table 57. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	LPRun and LPSleep	Unit
APB1	I2C3 independent clock domain	2.29	1.87	1.30	µA/MHz
	LPTIM1	1.67	1.44	1.50	
	LPTIM1 independent clock domain	2.50	2.19	1.45	
	LPTIM2	1.67	1.37	0.90	
	LPTIM2 independent clock domain	2.50	2.12	1.55	
	LPTIM3	0.83	0.69	0.65	
	LPTIM3 independent clock domain	2.29	1.94	0.65	
	LPUART1	2.08	1.81	3.55	
	LPUART1 independent clock domain	2.50	2.06	1.35	
	RTCAPB	2.08	1.81	1.50	
	SPI2	1.46	1.19	0.90	
	TIM2	4.58	3.81	2.95	
	USART2	1.88	1.56	1.35	
	USART2 independent clock domain	4.58	3.75	3.05	
	WWDG1	0.42	0.31	0.05	
	All APB1 peripherals(1)	19.6	16.1	20.2	
APB2	ADC	1.25	1.00	0.70	µA/MHz
	ADC independent clock domain	0.21	0.13	0.30	
	SPI1	1.25	1.06	0.90	
	TIM1	6.25	5.19	8.30	
	TIM16	2.29	1.94	1.35	
	TIM17	2.29	1.87	1.25	
	USART1	1.67	1.38	1.00	
	USART1 independent clock domain	4.17	3.38	2.90	
	All APB2 peripherals(1)	15.8	13.0	15.8	
APB3	SUBGHZSPI	1.46	1.25	1.10	µA/MHz
	All APB3 peripherals	1.46	1.25	1.10	
All peripherals(1)		62.9	52.3	59.7	

1. Without independent clocks.

5.3.8 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in the table below, are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (wait for event) instruction.

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Table 58. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep to Run mode	-		0.188	0.222	µs
$t_{WULPSLEEP}$	Wakeup time from LPSleep to LPRun mode	Wakeup in flash with memory in power-down during LPSleep mode (FPDS = 1 in PWR_CR1) and with clock MSI = 2 MHz		3.81	4.38	
$t_{WUSTOP0}$	Wakeup time from Stop 0 mode in flash memory(2)	To Run mode (Range 1)	Wakeup clock MSI = 48 MHz	2.14	2.90	µs
			Wakeup clock MSI = 16 MHz	2.78	3.58	
			Wakeup clock HSI16 = 16 MHz	1.99	-	
			Wakeup clock HSI16 = 16 MHz with HSIKERON enabled	1.01	1.13	
			Wakeup clock MSI = 4 MHz	6.79	8.21	
			Wakeup clock MSI = 2 MHz	10.4	12.2	
		To LPRun mode	Wakeup clock MSI = 2 MHz	10.5	12.3	
$t_{WUSTOP1}$	Wakeup time from Stop 1 mode in flash memory(2)	To Run mode (Range 1)	Wakeup clock MSI = 48 MHz	5.15	6.55	µs
			Wakeup clock MSI = 16 MHz	5.73	7.14	
			Wakeup clock HSI16 = 16 MHz	5.71	7.10	
			Wakeup clock HSI16 = 16 MHz with HSIKERON enabled	4.57	6.52	
			Wakeup clock MSI = 4 MHz	8.43	9.93	
			Wakeup clock MSI = 2 MHz	11.9	13.7	
		To LPRun mode	Wakeup clock MSI = 2 MHz	10.6	13.9	
$t_{WUSTOP2}$	Wakeup time from Stop 2 mode in flash memory(2)	To Run mode (Range 1)	Wakeup clock MSI = 48 MHz	5.56	6.85	µs
			Wakeup clock MSI = 16 MHz	6.32	7.59	
			Wakeup clock HSI16 = 16 MHz	6.28	7.51	
			Wakeup clock HSI16 = 16 MHz with HSIKERON enabled	6.26	7.53	
			Wakeup clock MSI = 4 MHz	9.69	10.9	
			Wakeup clock MSI = 2 MHz	14.0	15.4	
t_{WUSTBY}	Wakeup time from Standby to Run mode	Range 1	Wakeup clock MSI = 4 MHz	34.3	39.2	µs
			Wakeup clock MSI = 8 MHz	22.4	25.6	
$t_{WUSHUTD}$	Wakeup time from Shutdown to Run mode	Range 1	Wakeup clock MSI = 4 MHz	264	316	

1. Guaranteed by characterization results (V_{DD} = 3 V, T = 25 °C).
2. Wakeup time is equivalent when code is executed from SRAM1 compared to flash memory. It is also equivalent when going to Range 2 rather than Range 1.

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Table 59. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Transition time from LPRun to Run mode(2)	Code run with MSI = 2 MHz	19.6	-	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1(3)	Code run with HSI16	21.9	32.2	
	Regulator transition time from Range 1 to Range 2(3)		23.1	33.9	

1. Guaranteed by characterization results (V_{DD} = 3 V, T = 25 °C).
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

5.3.9 External clock source characteristics

High-speed external user clock generated from an external source

The high-speed external (HSE32) clock can be supplied with a 32 MHz crystal oscillator or by a TCXO (temperature controlled crystal oscillator).

Crystal oscillator

The devices include internal programmable capacitances that can be used to tune the crystal frequency in order to compensate the PCB parasitic one.

Characteristics in the tables below, are measured over recommended operating conditions, unless otherwise specified. Typical values are referred to T_A = 25 °C and V_{DD} = 3 V.

Table 60. HSE32 crystal requirements(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{nom}	Oscillator frequency	-	-	32	-	MHz
f_{TOL}	Frequency accuracy(2)	Initial(3)	-	-	±10	ppm
		Over temperature(4)	-	-	±30	
		Aging over 10 years	-	-	±10	
C_{Load}	Load capacitance(5)	-	9.5	10	10.5	pF
C_{Shunt}	Crystal shunt capacitance	-	0.3	0.6	2	
C_{motion}	Crystal motional capacitance	-	1.3	1.89	2.5	fF
ESR	Crystal equivalent series resistance	-	-	30	60	Ω
P_D	Drive level	-	-	-	100	µW
G_m	Oscillator transconductance	Startup	11.3	-	-	mA/V

1. 32 MHz XTAL is specified for two specific references: NX2016SA and NX1612SA.
2. Crystal frequency accuracy can also be further restricted by the protocols support by the application.
3. Initial accuracy can be compensated by initial calibration. See the application note AN5646.
4. Frequency over temperature can be partially compensated by firmware.

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5. Load capacitance can be managed by internal programmable capacitances at calibration phase. No need to add external foot capacitances. The values indicated take into account the combination of the two foot capacitances.

Table 61. HSE32 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SUA(HSE)}$	Startup time for 80% amplitude stabilization	V_{DDRF} stabilized, SUBGHZ_HSEINTRIMR = 0x12, -40 to +105 °C temperature range	-	1000	-	µs
$t_{SUR(HSE)}$	Startup time for HSEREADY signal	V_{DDRF} stabilized, SUBGHZ_HSEINTRIMR = 0x12, -40 to +105 °C temperature range	-	180	-	
$I_{DDRF(HSE)}$	HSE32 current consumption	HSEGMC = 000, SUBGHZ_HSEINTRIMR = 0x12	-	50	-	µA
$XOT_{g(HSE)}$	SUBGHZ_HSEINTRIMR granularity	Capacitor bank	-	1	5	ppm
$XOT_{fp(HSE)}$	SUBGHZ_HSEINTRIMR frequency pulling		±15	±30	-	
$XOT_{nb(HSE)}$	SUBGHZ_HSEINTRIMR number of tuning bits		-	6	-	bit
$XOT_{st(HSE)}$	SUBGHZ_HSEINTRIMR setting time		-	-	0.1	ms

For more information about the trimming methodology of the oscillator, refer to the application note *HSE trimming for STM32 wireless MCUs* (AN5042).

For more information about the crystal selection, refer to the application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs* (AN2867).

TCXO regulator

Table 62. HSE32 TCXO regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TCXO}	Regulated voltage range for TCXO voltage supply	$V_{DDOP} > V_{TCXO}$ + 200 mV	1.6	1.7	3.3	V
ILTCXO	Load current for TCXO regulator	-	-	1.5	4	mA
TSVTCXO	Startup time for TCXO regulator	From enable to regulated voltage within 25 mV from target	-	-	50	µs
IDDTCXO	Current consumption for TCXO regulator	Quiescent current	-	-	70	µA
		Relative to load current	-	1.6	2	%
ATCXO	Amplitude voltage for external TCXO applied to OSC_IN pin	Provided through a 220 Ω resistor in series with a capacitance (voltage divider)(1)	0.4	0.6	1.2(2)	Vpk-pk

1. In order to minimize spurious injection, the capacitance value must be calculated such that an amplitude of 0.4 to 0.5 Vpk-pk on OSC_IN is obtained. For TCXO output voltage of 0.8 Vpk-pk, 10 pF can be used.
2. Clipped-sine output TCXO is required, with the output amplitude not exceeding 1.2 V peak-to-peak.

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Low-speed external user clock generated from an external source

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. The information provided in this section is based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time.

Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

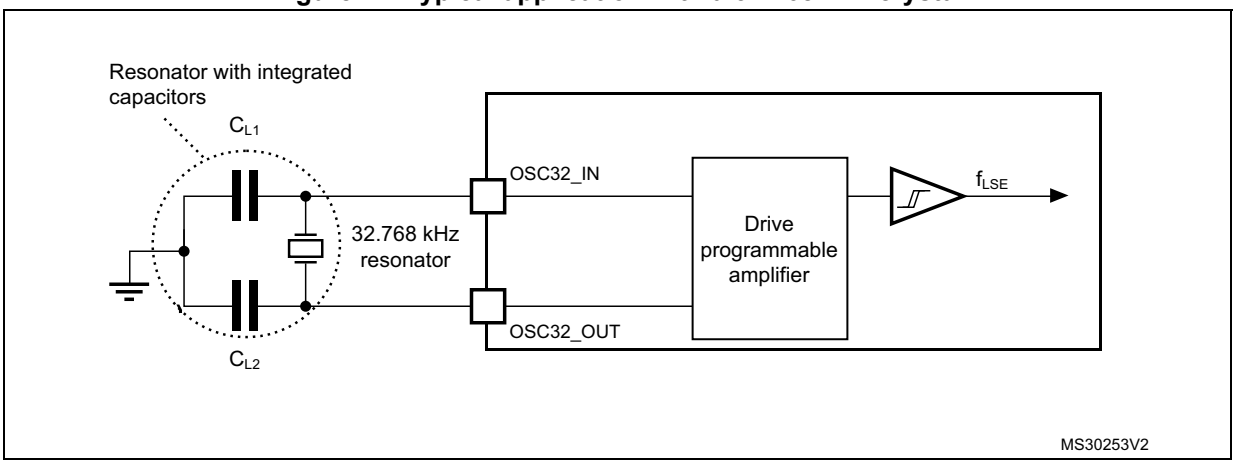
Table 63. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 - Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 - Medium-low drive capability	-	315	-	
		LSEDRV[1:0] = 10 - Medium-high drive capability	-	500	-	
		LSEDRV[1:0] = 11 - High drive capability	-	630	-	
$G_{mcritmax}$	Maximum critical crystal g_m	LSEDRV[1:0] = 00 - Low drive capability	-	-	0.50	µA/V
		LSEDRV[1:0] = 01 - Medium-low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 - Medium-high drive capability	-	-	1.70	
		LSEDRV[1:0] = 11 - High drive capability	-	-	2.70	
$t_{SU(LSE)}$(2)	Startup time	V_{DD} stabilized	-	2	-	s

1. Guaranteed by design.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stable 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

For more information on the crystal selection, refer to application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs* and MPUs (AN2867).

Figure 17. Typical application with a 32.768 kHz crystal



Note: No external resistors are required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

In bypass mode, the LSE oscillator is switched off and the input pin is a standard GPIO.

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The external clock signal has to respect the I/O characteristics detailed in *Section 5.3.16: I/O port characteristics*.The recommend clock input waveform is shown in the figure below.

Figure 18. Low-speed external clock source AC timing diagram

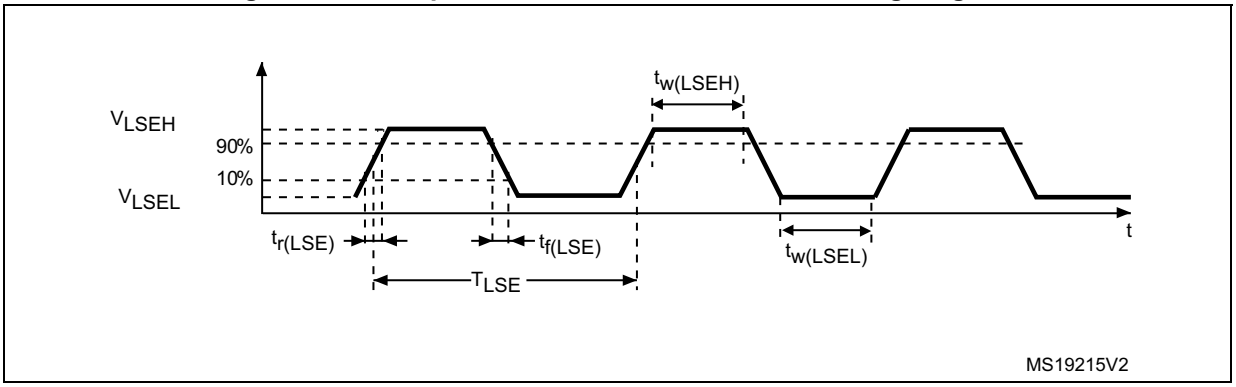


Table 64. Low-speed external user clock characteristics(1) – Bypass mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	21.2	32.768	44.4	kHz
V_{LSEH}	OSC32_IN input pin high-level voltage	-	0.7 x V_{DDx}	-	V_{DDx}	V
V_{LSEL}	OSC32_IN input pin low-level voltage	-	V_{SS}	-	0.3 x V_{DDx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns
f_{tolLSE}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling	–500	-	+500	ppm

1. Guaranteed by design.

5.3.10 Internal clock source characteristics

Parameters given in the table below are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 26: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 65. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 frequency	V_{DD} = 3.0 V, T_A = 30 °C	15.88	-	16.08	MHz

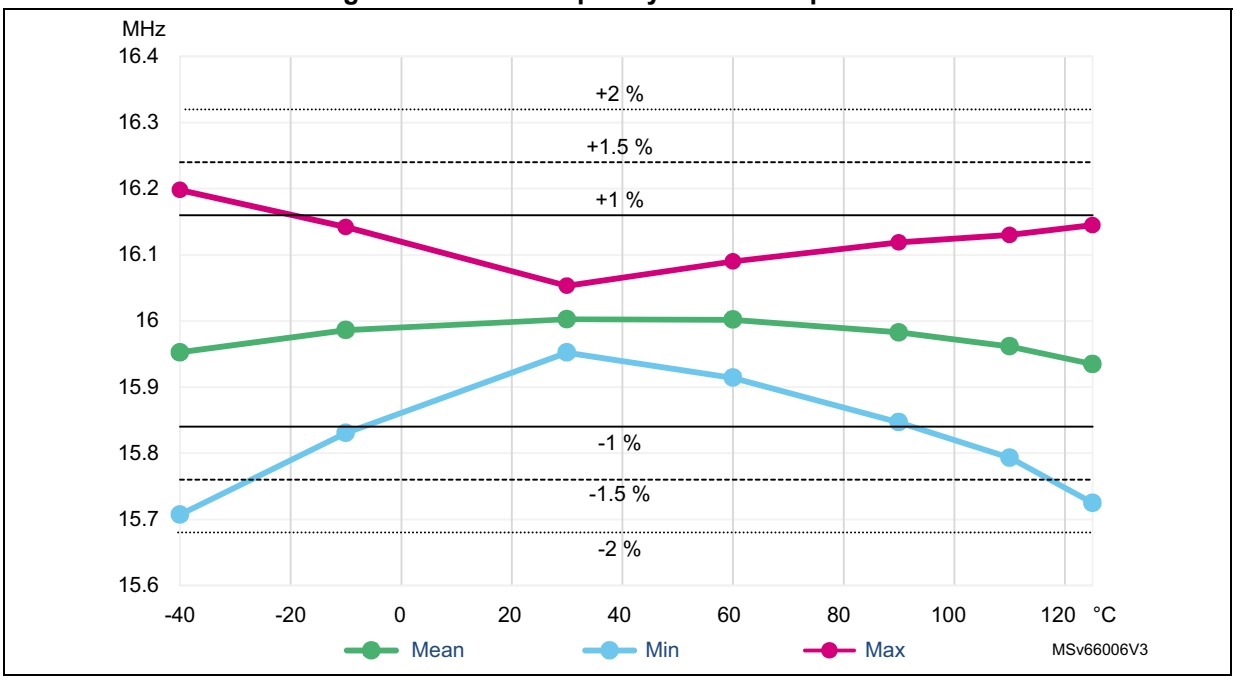
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Table 65. HSI16 oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 48	0.2	0.3	0.4	%
		Trimming code is a multiple of 48	–4	–6	–8	
DuCy(HSI16)(2)	Duty cycle	-	45	-	55	
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift	T_j = 0 to 85 °C	–1	-	1	
		T_j = -40 to 125 °C	–2	-	1.5	
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD} = 1.8 V to 3.6 V	–0.1	-	0.05	
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 19. HSI16 frequency versus temperature



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Multi-speed internal (MSI) RC oscillator

Table 66. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}= 3 V and T_A= 30 °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	789.6	800	810.4	
			Range 4	0.987	1	1.013	MHz
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
Δ_{TEMP}(MSI)(2)	MSI oscillator frequency drift over temperature	MSI mode	T_j = 0 to 85 °C	–3.5	-	3	%
			T_j = -40 to 125 °C	–8	-	6	

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Table 66. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta_{VDD}(MSI)^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD} = 1.8 to 3.6 V	–1.2	-	0.5	%
				V_{DD} = 2.4 to 3.6 V	–0.5	-		
			Range 4 to 7	V_{DD} = 1.8 to 3.6 V	–2.5	-	0.7	
				V_{DD} = 2.4 to 3.6 V	–0.8	-		
			Range 8 to 11	V_{DD} = 1.8 to 3.6 V	–5	-	1	
				V_{DD} = 2.4 to 3.6 V	–1.6	-		
$\Delta F_{SAMPLING}(MSI)^{(2)(4)}$	Frequency variation in sampling mode(3)	MSI mode	T_j = -40 to 85 °C		-	1	2	
			T_j = -40 to 125 °C		-	2	4	
CC jitter(MSI)(4)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)(4)	RMS period jitter	PLL mode Range 11		-	-	50	-	
$t_{SU}(MSI)^{(4)}$	MSI oscillator start-up time	Range 0		-	-	10	20	µs
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)^{(4)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

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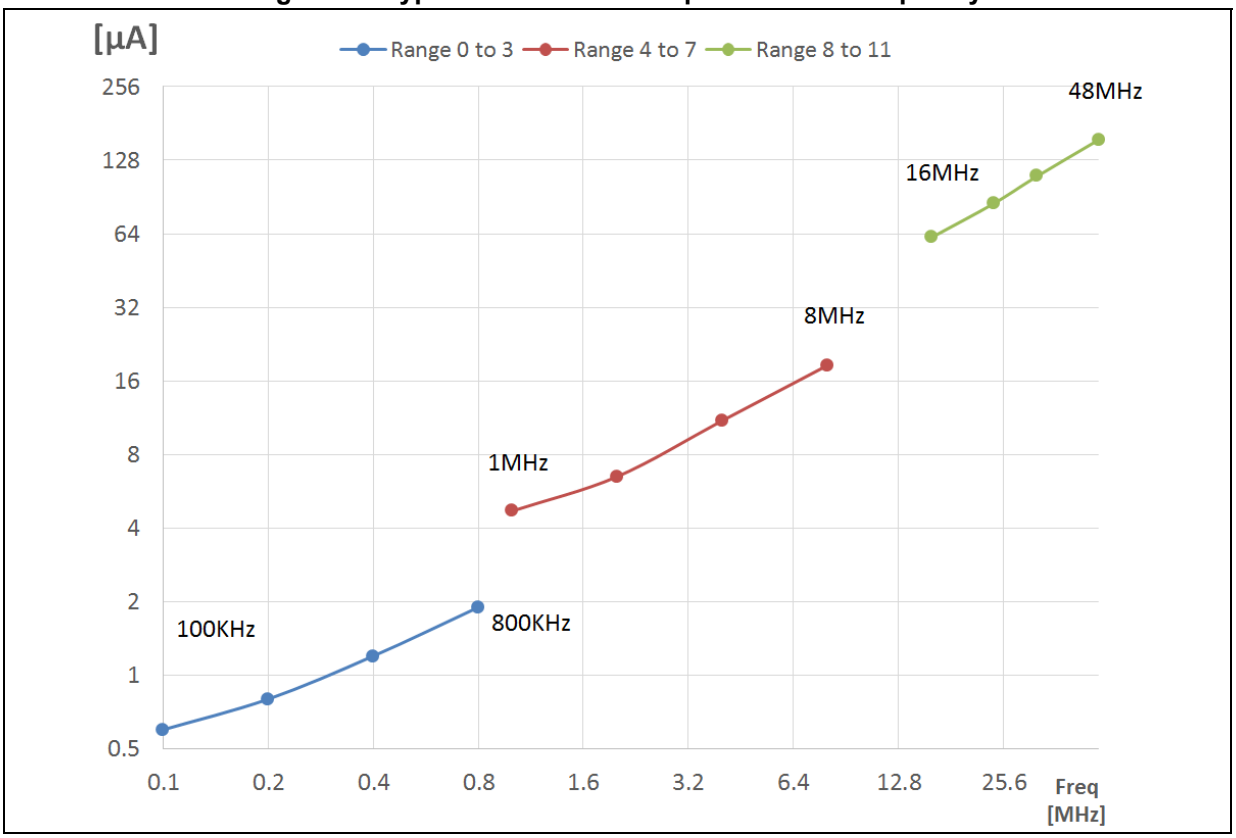
Table 66. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$I_{DD}(MSI)^{(4)}$	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA
			Range 1	-	-	0.8	1.2	
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	
			Range 8	-	-	62	80	
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means LPRun and LPSleep modes with temperature sensor disabled.
4. Guaranteed by design.

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Figure 20. Typical current consumption vs. MSI frequency



Low-speed internal (LSI) RC oscillator

Table 67. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.8 to 3.6 V, T_j = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI)$(2)	LSI oscillator startup time	-	-	80	130	µs
$t_{STAB}(LSI)$(2)	LSI oscillator stabilization time	5 % of final frequency	-	125	180	
$I_{DD}(LSI)$(2)	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

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5.3.11 PLL characteristics

Parameters given in the table below are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions*.

Table 68. PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	2.66	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	3	-	48	MHz
		Voltage scaling Range 2	3	-	16	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	12	-	48	
		Voltage scaling Range 2	12	-	16	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	12	-	48	
		Voltage scaling Range 2	12	-	16	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	
		Voltage scaling Range 2	96	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 48 MHz	-	40	-	ps
	RMS period jitter		-	30	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 96 MHz	-	200	260	µA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the two PLLs.

5.3.12 Flash memory characteristics

Table 69. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.7	90.8	µs
t_{prog_row}	One row (64 double-words) programming time	Normal programming	5.2	5.5	ms
		Fast programming	3.8	4.0	
t_{prog_page}	One 2-Kbyte page programming time	Normal programming	41.8	43.0	
		Fast programming	30.4	31.0	
t_{ERASE}	2-Kbyte page erase time	-	22.0	24.5	
t_{ME}	Mass erase time	-	22.1	25.0	

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Table 69. Flash memory characteristics(1) (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 6 µs)	-	
		Erase mode	7 (for 67 µs)	-	

1. Guaranteed by design.

Table 70. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports). the device is stressed by the following electromagnetic events until a failure occurs (failure indicated by the LEDs):

- **ESD** (electrostatic discharge, positive and negative) applied to all device pins until a functional disturbance occurs (test compliant with IEC 61000-4-2 standard)
- **FTB** (burst of fast transient voltage, positive and negative) applied to VDD and VSS pins, through a 100 pF capacitor, until a functional disturbance occurs (test compliant with IEC 61000-4-4 standard)

A device reset allows normal operations to be resumed.

The test results given in the table below, are based on the EMS levels and classes defined in application note *EMC design guide for STM8, STM32 and Legacy MCUs* (AN1709).

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Table 71. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software.

Note: Good EMC performance is highly dependent on the user application and the software in particular.It is then recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

Software recommendations

The software flow must include the management of runaway conditions such as:

- corrupted program counter
- unexpected reset
- critical data corruption (control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 s.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. For more details, refer to the application note *Software techniques for improving microcontrollers EMC performance (*AN1015).

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with the IEC 61967-2 standard, that specifies the test board and the pin loading.

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Table 72. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Peripheral ON SMPS OFF f_{HSE} = /f_{CPUM4}, f_{CPUM0}]	Unit
				f_{HSE} = 32 MHz f_{CPU1} = f_{CPU2} = 48 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, UFBGA73 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	1	dBµV
			30 MHz to 130 MHz	4	
			130 MHz to 1 GHz	0	
			1 GHz to 2 GHz	7	
			EMI level	2	-

5.3.14 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 s) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 73. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1 JS-002	C2a	500	

1. Guaranteed by characterization results.

Static latch-up

The following complementary static tests are required on three parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 74. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	Level A

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5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3V-capable I/O pins), must be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in case abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating-input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in the table below.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 75. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PB0	–5	N/A(2)	mA
	Injected current on PB0 pin	–5	0	

1. Guaranteed by characterization results.
2. Injection not possible.

5.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the conditions summarized in *Table 26: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Note: For information on GPIO configuration, refer to the application note STM32 GPIO configuration for hardware settings and low-power consumption (AN4899).

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Table 76. I/O static characteristics

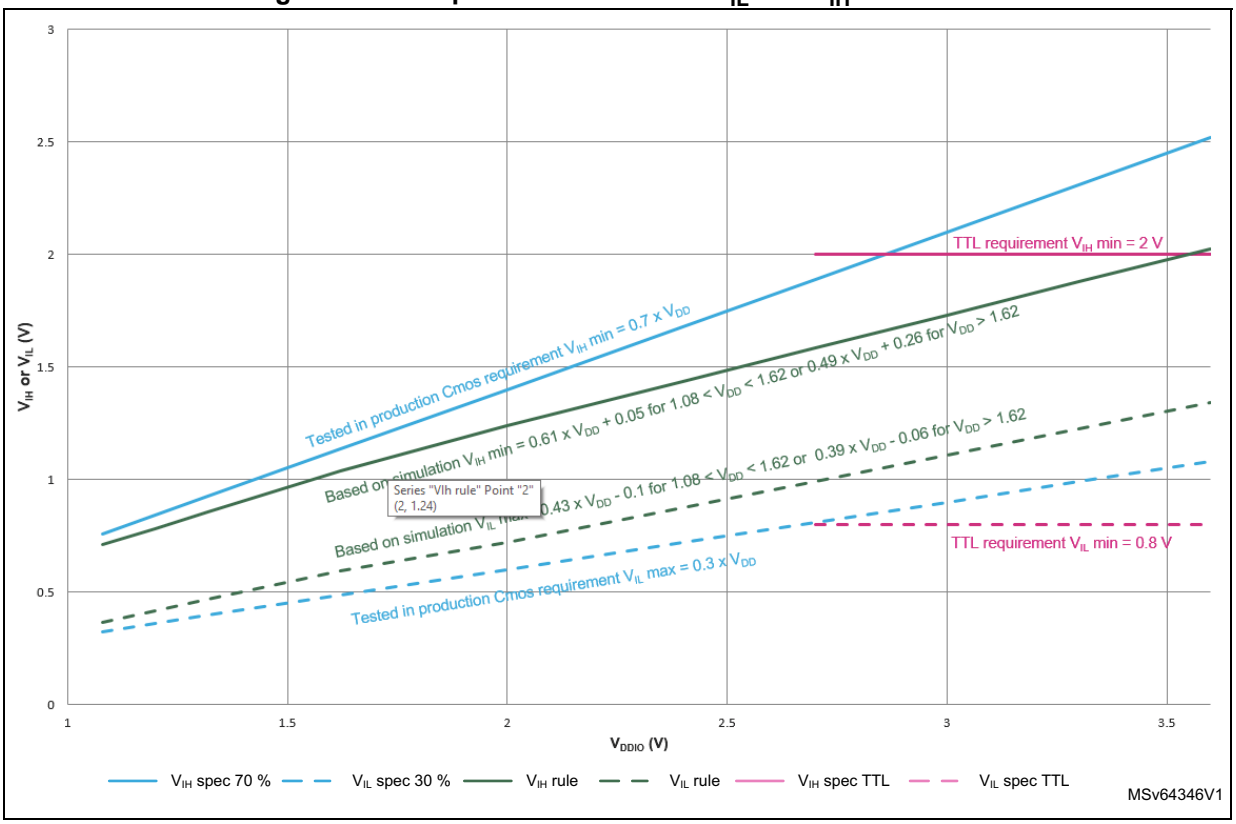
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low-level voltage(1)	1.8 V < V_{DD} < 3.6 V	-	-	0.3 x V_{DD}	V
	I/O input low-level voltage(2)				0.39 x V_{DD} - 0.06	
V_{IH}	I/O input high-level voltage(1)		0.7 x V_{DD}	-	-	
	I/O input high-level voltage(2)		0.49 x V_{DD} + 0.26	-	-	
V_{hys}	TT, FT_xx and NRST I/O input hysteresis		-	200	-	mV
I_{lkg}	FT_xx input leakage current	0 ≤ V_{IN} ≤ Max(V_{DDXXX})(3)(4)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX}) +1 V(2)(3)(4)	-	-	650	
		Max(V_{DDXXX}) +1 V < V_{IN} ≤ 5.5 V(2)(3)(4)(5)(6)	-	-	200(7)	
	TT input leakage current	V_{IN} ≤ Max(V_{DDXXX})(3)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6 V(3)	-	-	2000	
R_{PU}	Weak pull-up equivalent resistor(1)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(1)	V_{IN} = V_{DD}	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Tested in production.
2. Guaranteed by design, not tested in production.
3. Represents the pad leakage of the I/O itself. The total product pad leakage is given by $I_{Total_Ileak_max}$ = 10 µA + number of I/Os where V_{IN} is applied on the pad x $I_{lkg(Max)}$.
4. Max(V_{DDXXX}) is the maximum value among all the I/O supplies.
5. V_{IN} must be lower than [Max(V_{DDXXX}) + 3.6 V].
6. Refer to the figure below.
7. To sustain a voltage higher than [Min(V_{DD}, V_{DDA}) + 0.3 V], the internal pull-up and pull-down resistors must be disabled on all FT_xx I/O.

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All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters, as shown in the figure below.

Figure 21. I/O input characteristics - V_{IL} and V_{IH} on all I/Os



Output driving current

The GPIOs can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2: Absolute maximum ratings*.

The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 22: Voltage characteristics*).

The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 22: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 26: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT or TT unless otherwise specified).

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Table 77. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low-level voltage for an I/O pin	CMOS port(3) $\|I_{IO}\|$ = 8 mA, $V_{DD} \geq 2.7$ V	-	0.4	V
V_{OH}(2)	Output high-level voltage for an I/O pin		V_{DD} - 0.4	-	
V_{OL}(2)	Output low-level voltage for an I/O pin	TTL port(3) $\|I_{IO}\|$ = 8 mA, $V_{DD} \geq 2.7$ V	-	0.4	
V_{OH}(2)	Output high-level voltage for an I/O pin		2.4	-	
V_{OL}(2)	Output low-level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA, $V_{DD} \geq 2.7$ V	-	1.3	
V_{OH}(2)	Output high-level voltage for an I/O pin		V_{DD} - 1.3	-	
V_{OL}(2)	Output low-level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA, $V_{DD} \geq 1.8$ V	-	0.4	
V_{OH}(2)	Output high-level voltage for an I/O pin		V_{DD} - 0.45	-	
V_{OLFM+}(2)	Output low-level voltage for an FT I/O pin in FM+ mode (FT I/O with “f” option)	$\|I_{IO}\|$ = 20 mA, $V_{DD} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA, $V_{DD} \geq 1.8$ V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 22: Voltage characteristics*. The sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. Guaranteed by design.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

Input/output AC characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 26: General operating conditions*.

Table 78. I/O AC characteristics(1)(2)

OSPEEDx[1:0](3)	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5	MHz
			C = 50 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	1	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10	
			C = 10 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	1.5	
	Tr/Tf	Output rise and fall time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	ns
			C = 50 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	52	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17	
			C = 10 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	37	

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Table 78. I/O AC characteristics(1)(2) (continued)

OSPEEDx[1:0](3)	Symbol	Parameter	Conditions	Min	Max	Unit
0b01	Fmax	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	MHz
			C = 50 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	10	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	
			C = 10 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	15	
	Tr/Tf	Output rise and fall time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	9	ns
			C = 50 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	16	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.5	
			C = 10 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	9	
0b10	Fmax	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	MHz
			C = 50 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	25	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100(4)	
			C = 10 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	37.5	
	Tr/Tf	Output rise and fall time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.8	ns
			C = 50 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	11	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.5	
			C = 10 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	5	
0b11	Fmax	Maximum frequency	C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	120(4)	MHz
			C = 30 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	50	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	180(4)	
			C = 10 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	75(4)	
	Tr/Tf	Output rise and fall time	C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C = 30 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	6	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.7	
			C = 10 pF, 1.8 V ≤ V_{DD} ≤ 2.7 V	-	3.3	

1. The maximum frequency is defined with (T_r+ T_f) ≤ 2/3 T, and duty cycle comprised between 45 and 55 %.
2. The fall and rise time are defined, respectively, between 90 and 10 %, and between 10 and 90 % of the output waveform.
3. OSPEED0[1:0] in GPIOA_OSPEEDR, GPIOB_OSPEEDR and GPIOC_OSPEEDR. OSPEED3[1:0] in GPIOH_OSPEEDR
4. This value represents the I/O capability but the maximum system frequency is limited to 48 MHz.

5.3.17 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 26: General operating conditions*.

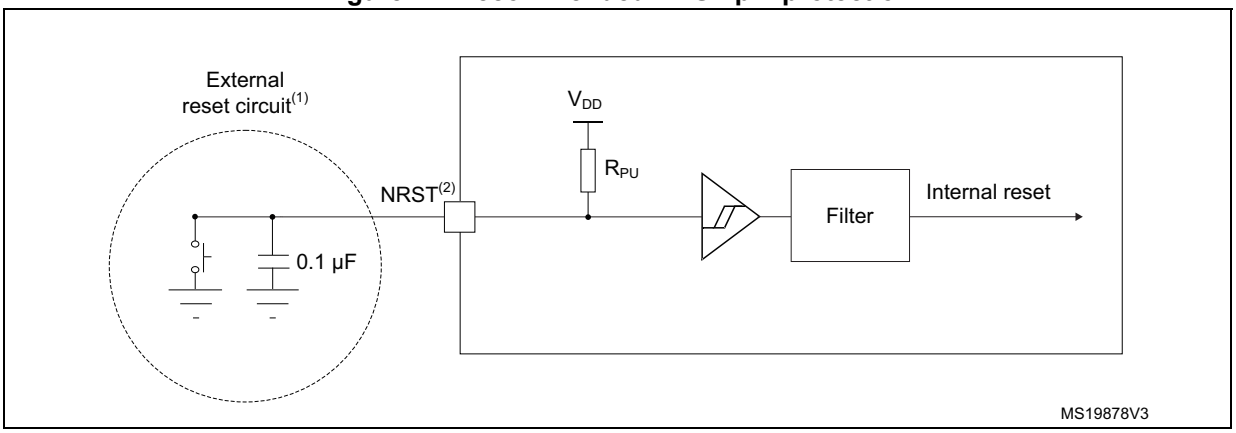
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Table 79. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.7 x V_{DD}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input, filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input, not filtered pulse	1.8 V ≤ V_{DD} ≤ 3.6 V	350	-	-	

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10 %).

Figure 22. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in the above table. Otherwise the reset is not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

5.3.18 Analog switches booster

Table 80. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.8	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.8 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

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5.3.19 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 26: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 81. ADC characteristics(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			
f_{ADC}	ADC clock frequency	Range 1	0.14	-	35	MHz
		Range 2	0.14	-	16	
f_s	Sampling rate	12 bits, $V_{DDA} > 2$ V	-	-	2.50	Msps
		10 bits, $V_{DDA} > 2$ V	-	-	2.92	
		8 bits, $V_{DDA} > 2$ V	-	-	3.50	
		6 bits, $V_{DDA} > 2$ V	-	-	4.38	
		12 bits, $V_{DDA} \leq 2$ V	-	-	2.18	
		10 bits, $V_{DDA} \leq 2$ V	-	-	2.50	
		8 bits, $V_{DDA} \leq 2$ V	-	-	2.92	
		6 bits, $V_{DDA} \leq 2$ V	-	-	3.50	
f_{TRIG}	External trigger frequency	f_{ADC} = 35 MHz, 12 bits, $V_{DDA} > 2$ V	-	-	2.35	MHz
		f_{ADC} = 35 MHz, 12 bits, $V_{DDA} \leq 2$ V	-	-	2.18	
		12 bits, $V_{DDA} > 2$ V	-	-	$f_{ADC}/15$	
		12 bits, $V_{DDA} \leq 2$ V	-	-	$f_{ADC}/17$	
V_{AIN}	Conversion voltage range	-	V_{SS}	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	ADC power-up time	-	2			Conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 35 MHz	2.35			µs
		-	82			$1/f_{ADC}$

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Table 81. ADC characteristics(1) (continued)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency	CKMODE = 00	2	-	3	$1/f_{ADC}$
		CKMODE = 01	6.5			$1/f_{PCLK}$
		CKMODE = 10	12.5			
		CKMODE = 11	3.5			
t_s	Sampling time	f_{ADC} = 35 MHz	0.043	-	4.59	µs
		-	1.5	-	160.5	$1/f_{ADC}$
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 35 MHz Resolution = 12 bits	0.40	-	4.95	µs
		Resolution = 12 bits	t_s + 12.5 cycles for successive approximation = 14 to 173			$1/f_{ADC}$
t_{IDLE}	Laps of time allowed between two conversions without rearm	-	-	-	100	µs
$I_{DDA(ADC)}$	ADC consumption from V_{DDA}	f_s = 2.5 Msps	-	410	-	µA
		f_s = 1 Msps	-	164	-	
		f_s = 10 ksps	-	17	-	
$I_{DDV(ADC)}$	ADC consumption from V_{REF+} single ended mode	f_s = 2.5 Msps	-	65	-	µA
		f_s = 1 Msps	-	26	-	
		f_s = 10 ksps	-	0.26	-	

1. Guaranteed by design
2. I/O analog switch voltage booster must be enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when V_{DDA} ≥ 2.4 V.

Table 82. Maximum ADC R_{AIN} values

Resolution	Sampling cycle at 35 MHz (ns)	Sampling time at 35 MHz (ns)	Max. R_{AIN}(1)(2)(Ω)
12 bits	1.5(3)	43	50
	3.5	100	680
	7.5	214	2200
	12.5	357	4700
	19.5	557	8200
	39.5	1129	15000
	79.5	2271	33000
	160.5	4586	50000

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Table 82. Maximum ADC R_{AIN} values (continued)

Resolution	Sampling cycle at 35 MHz (ns)	Sampling time at 35 MHz (ns)	Max. R_{AIN}(1)(2)(Ω)
10 bits	1.5(3)	43	68
	3.5	100	820
	7.5	214	3300
	12.5	357	5600
	19.5	557	10000
	39.5	1129	22000
	79.5	2271	39000
	160.5	4586	50000
8 bits	1.5(3)	43	82
	3.5	100	1500
	7.5	214	3900
	12.5	357	6800
	19.5	557	12000
	39.5	1129	27000
	79.5	2271	50000
	160.5	4586	50000
6 bits	1.5(3)	43	390
	3.5	100	2200
	7.5	214	5600
	12.5	357	10000
	19.5	557	15000
	39.5	1129	33000
	79.5	2271	50000
	160.5	4586	50000

1. Guaranteed by design.
2. I/O analog switch voltage booster must be enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when V_{DDA} ≥ 2.4 V.
3. Only allowed with V_{DDA} > 2 V

Table 83. ADC accuracy(1)(2)(3)

Symbol	Parameter	Conditions(4)	Min	Typ	Max	Unit
ET	Total unadjusted error	$V_{DDA} = V_{REF+}$ = 3 V, f_{ADC} = 35 MHz, f_s ≤ 2.5 Msps, T_A = 25 °C	-	3	4	LSB
		2 V < V_{DDA}, V_{REF+} < 3.6 V, f_{ADC} = 35 MHz; f_s ≤ 2.5 Msps, T_A = entire range	-	3	6.5	
		1.62 V < $V_{DDA} = V_{REF+}$ < 3.6 V, T_A = entire range Range 1: f_{ADC} = 35 MHz, f_s ≤ 2.2 Msps Range 2: f_{ADC} = 16 MHz, f_s ≤ 1.1 Msps	-	3	7.5	

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Table 83. ADC accuracy(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)	Min	Typ	Max	Unit
EO	Offset error	$V_{DDA} = V_{REF+} = 3$ V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	-	1.5	2	LSB
		2 V < V_{DDA}, V_{REF+} < 3.6 V, $f_{ADC} = 35$ MHz; $f_s \le 2.5$ Msps, T_A = entire range	-	1.5	4.5	
		1.62 V < $V_{DDA} = V_{REF+}$ < 3.6 V, T_A = entire range Range 1: $f_{ADC} = 35$ MHz, $f_s \le 2.2$ Msps Range 2: $f_{ADC} = 16$ MHz, $f_s \le 1.1$ Msps	-	1.5	5.5	
EG	Gain error	$V_{DDA} = V_{REF+} = 3$ V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	-	3	3.5	LSB
		2 V < V_{DDA}, V_{REF+} < 3.6 V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	-	3	5	
		1.62 V < $V_{DDA} = V_{REF+}$ < 3.6 V, T_A = entire range Range 1: $f_{ADC} = 35$ MHz, $f_s \le 2.2$ Msps Range 2: $f_{ADC} = 16$ MHz, $f_s \le 1.1$ Msps	-	3	6.5	
ED	Differential linearity error	$V_{DDA} = V_{REF+} = 3$ V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	-	1.2	1.5	LSB
		2 V < V_{DDA}, V_{REF+} < 3.6 V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	-	1.2	1.5	
		1.62 V < $V_{DDA} = V_{REF+}$ < 3.6 V,T_A = entire range Range 1: $f_{ADC} = 35$ MHz, $f_s \le 2.2$ Msps Range 2: $f_{ADC} = 16$ MHz, $f_s \le 1.1$ Msps	-	1.2	1.5	
EL	Integral linearity error	$V_{DDA} = V_{REF+} = 3$ V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	-	2.5	3	LSB
		2 V < V_{DDA}, V_{REF+} < 3.6 V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	-	2.5	3	
		1.62 V < $V_{DDA} = V_{REF+}$ < 3.6 V, T_A = entire range Range 1: $f_{ADC} = 35$ MHz, $f_s \le 2.2$ Msps Range 2: $f_{ADC} = 16$ MHz, $f_s \le 1.1$ Msps	-	2.5	3.5	
ENOB	Effective number of bits	$V_{DDA} = V_{REF+} = 3$ V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	10.1	10.2	-	bit
		2 V < V_{DDA}, V_{REF+} < 3.6 V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	9.6	10.2	-	
		1.62 V < $V_{DDA} = V_{REF+}$ < 3.6 V, T_A = entire range Range 1: $f_{ADC} = 35$ MHz, $f_s \le 2.2$ Msps Range 2: $f_{ADC} = 16$ MHz, $f_s \le 1.1$ Msps	9.5	10.2	-	
SINAD	Signal-to-noise and distortion ratio	$V_{DDA} = V_{REF+} = 3$ V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	62.5	63	-	dB
		2 V < V_{DDA}, V_{REF+} < 3.6 V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	59.5	63	-	
		1.62 V < $V_{DDA} = V_{REF+}$ < 3.6 V, T_A = entire range Range 1: $f_{ADC} = 35$ MHz, $f_s \le 2.2$ Msps Range 2: $f_{ADC} = 16$ MHz, $f_s \le 1.1$ Msps	59	63	-	
SNR	Signal-to-noise ratio	$V_{DDA} = V_{REF+} = 3$ V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	63	64	-	dB
		2 V < V_{DDA}, V_{REF+} < 3.6 V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	60	64	-	
		1.62 V < $V_{DDA} = V_{REF+}$ < 3.6 V, T_A = entire range Range 1: $f_{ADC} = 35$ MHz, $f_s \le 2.2$ Msps Range 2: $f_{ADC} = 16$ MHz, $f_s \le 1.1$ Msps	60	64	-	

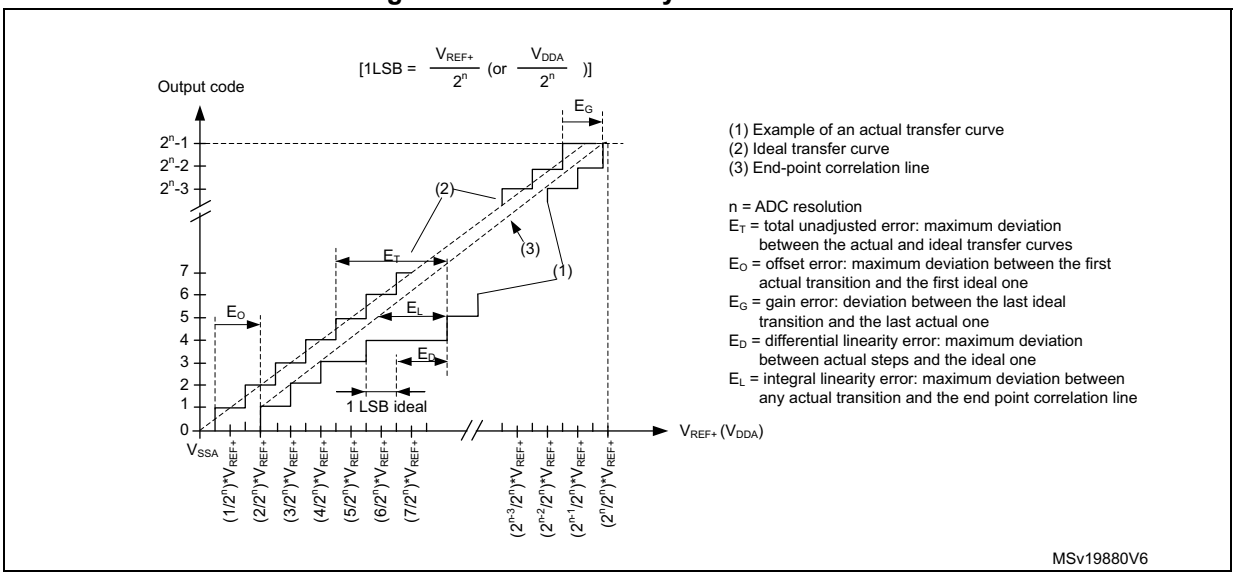
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Table 83. ADC accuracy(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)	Min	Typ	Max	Unit
THD	Total harmonic distortion	$V_{DDA} = V_{REF+} = 3$ V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	-	-74	-73	dB
		2 V < V_{DDA}, V_{REF+} < 3.6 V, $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	-	-74	-70	
		1.62 V < $V_{DDA} = V_{REF+}$ < 3.6 V, T_A = entire range Range 1: $f_{ADC} = 35$ MHz, $f_s \le 2.2$ Msps Range 2: $f_{ADC} = 16$ MHz, $f_s \le 1.1$ Msps	-	-74	-70	

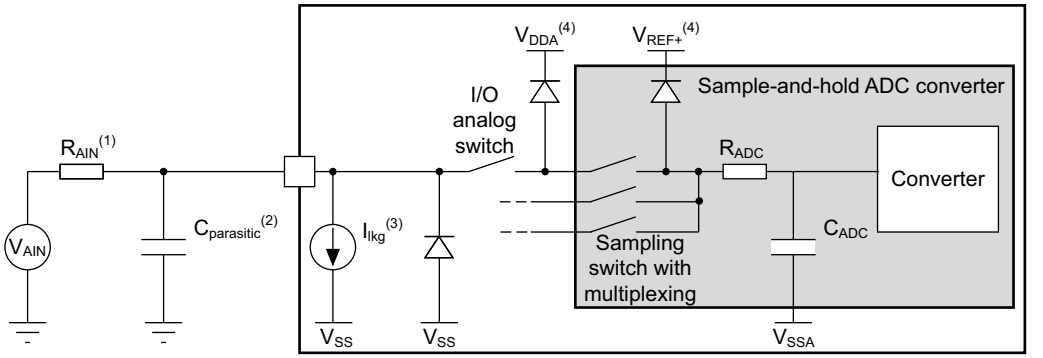
1. Based on characterization results, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. Injecting negative current on any analog input pin significantly reduces the accuracy of A-to-D conversion of signal on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins susceptible to receive negative current.
4. I/O analog switch voltage booster enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when $V_{DDA} \ge 2.4$ V.

Figure 23. ADC accuracy characteristics



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Figure 24. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



1. Refer to *Table 83: ADC accuracy* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 76: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades the conversion accuracy. To remedy this, f_{ADC} must be reduced.
3. Refer to *Table 76: I/O static characteristics* for the values of Ilkg.
4. Refer to *Section 3.10.1: Power supply schemes*.

General PCB design guidelines

Power supply decoupling must be performed as shown in *Figure 14: Power supply scheme*. The 100 nF capacitor must be ceramic (good quality) and must be placed as close as possible to the chip.

5.3.20 Temperature sensor characteristics

Table 84. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30 °C (±5 °C)(3)	0.742	0.76	0.785	V
t_{START} (TS_BUF)(1)	Sensor buffer startup time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Startup time when entering in continuous mode(4)	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by the ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.3 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 13: Temperature sensor calibration values*.
4. Continuous mode means Run and Sleep modes, or temperature sensor enable in LPRun and LPSleep modes.

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5.3.21 V_{BAT} monitoring characteristics

Table 85. V_{BAT} monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}(2)	-	3 * 39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
E_r(3)	Error on Q	-10	-	10	%
t_{S_vbat}(3)	ADC sampling time when reading V_{BAT}	12	-	-	µs

1. 1.55 V < V_{BAT} < 3.6 V.
2. V_{DD} on STM32WL55/4UxYx devices.
3. Guaranteed by design.

Table 86. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

5.3.22 Voltage reference buffer characteristics

Table 87. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V
			V_{RS} = 1	2.8	-	3.6	
		Degraded mode(2)	V_{RS} = 0	1.62	-	2.4	
			V_{RS} = 1	1.62	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode I_{LOAD}=100 µA, T_J = 30 °C	V_{RS} = 0	2.044	2.048	2.052	
			V_{RS} = 1	2.495	2.5	2.505	
		Normal mode I_{LOAD}=100 µA, -40 °C < T_J < 125 °C	V_{RS} = 0	2.030	2.048	2.057	
			V_{RS} = 1	2.478	2.500	2.509	
		Degraded mode(2)	V_{RS} = 0	V_{DDA} - 250 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA} - 250 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent series resistor of C_{load}	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA

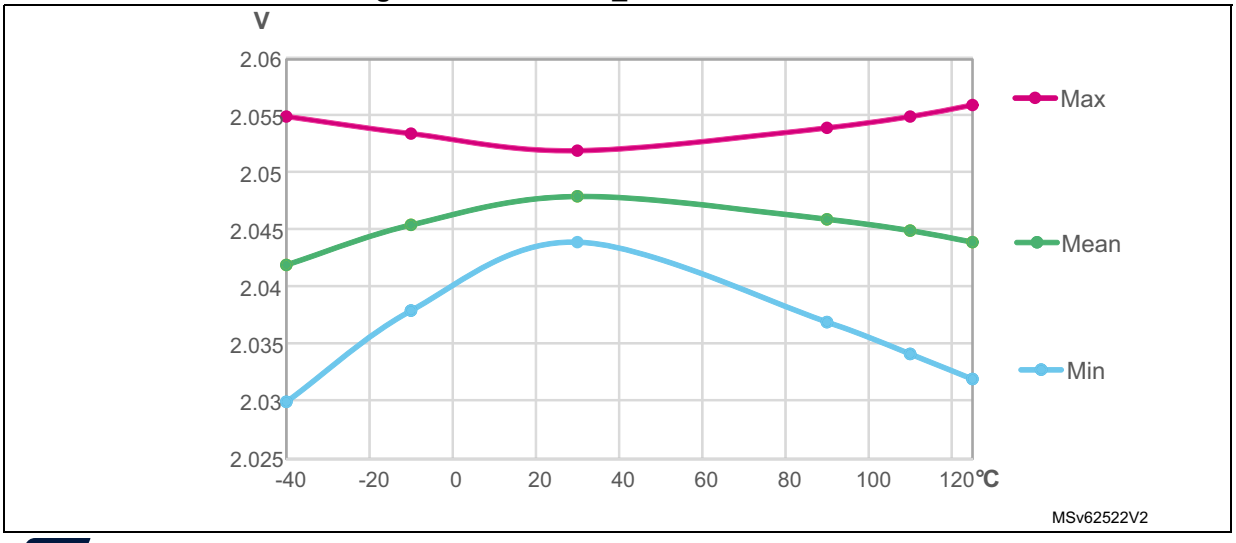
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Table 87. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	Normal mode	-	-	2000	ppm /V
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤ 4 mA	Normal mode	-	50	500	ppm /mA
T_{coeff}	Temperature coefficient	-40 °C < T_J < +105 °C		-	-	±[$T_{coeff_vrefint}$ + 50]	ppm /°C
		0 °C < T_J < +50 °C		-	-	±[$T_{coeff_vrefint}$ + 50]	
PSRR	Power supply rejection	DC		40	55	-	dB
		100 kHz		25	40	-	
t_{START}	Startup time	CL = 0.5 µF(3)		-	300	350	µs
		CL = 1.1 µF(3)		-	500	650	
		CL = 1.5 µF(3)		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (4)	-	-	-	8	-	mA
I_{DDA} (VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA		-	16	25	µA
		I_{load} = 500 µA		-	18	30	
		I_{load} = 4 mA		-	35	50	

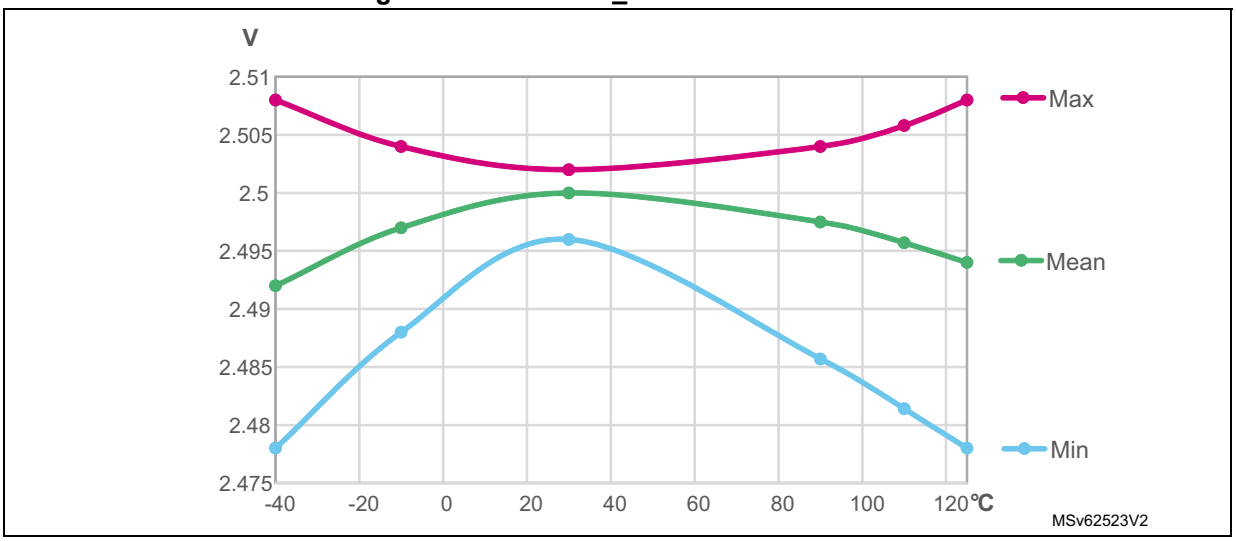
1. Guaranteed by design or characterization. Not tested in production.
2. In degraded mode, VREFBUF cannot maintain accurately the output voltage that follows (V_{DDA} - drop voltage).
3. The capacitive load must include a 100 nF capacitor in order to cut-off the high-frequency noise.
4. To correctly control the VREFBUF in-rush current during start-up phase and scaling change, the V_{DDA} voltage must be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

Figure 25. VREFOUT_TEMP when VRS = 0



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Figure 26. VREFOUT_TEMP when VRS = 1



5.3.23 Digital-to-analog converter characteristics

Table 88. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	3.6	V
		Other modes		1.80	-		
V_{REF+}	Positive reference voltage	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	V_{DDA}	V
		Other modes		1.80	-		
R_L	Resistive load	DAC output buffer ON	Connected to V_{SS}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
R_O	Output impedance	DAC output buffer OFF		9.6	11.7	13.8	
R_{BON}	Output impedance sample-and-hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample-and-hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} - 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	

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Table 88. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes, when DAC_OUT reaches final value ±0.5 LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP} (2)	Wakeup time from off state (setting the ENx bit in the DAC control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, DC		-	-80	-28	dB
$T_{W_to_W}$	Minimum time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB)	DAC_MCR:MODEx[2:0] = 000 or 001 CL ≤ 50 pF, RL ≥ 5 kΩ		1	-	-	µs
		DAC_MCR:MODEx[2:0] = 010 or 011 CL ≤ 10 pF		1.4	-	-	
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	

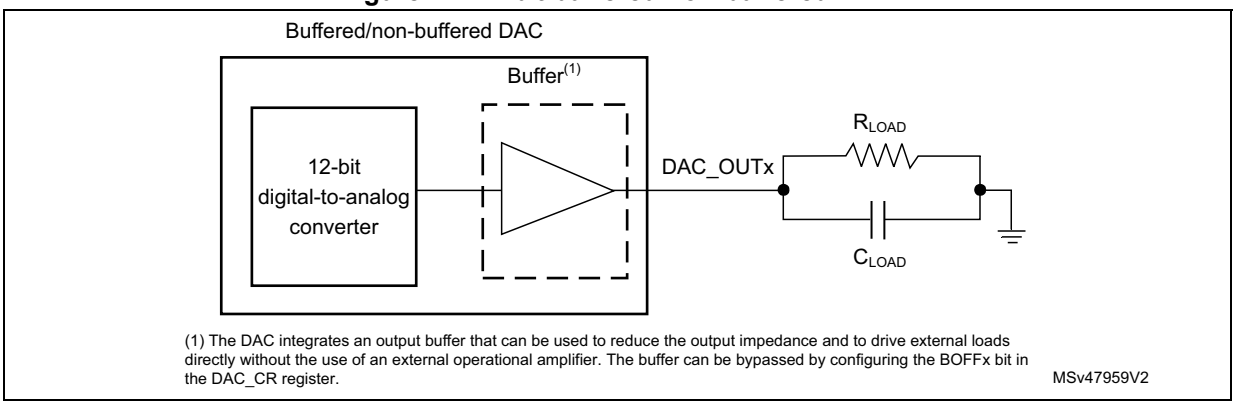
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Table 88. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDA(DAC)}$	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x $T_{on}/(T_{on}+T_{off})$(4)	670 x $T_{on}/(T_{on}+T_{off})$(4)	
$I_{DDV(DAC)}$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x $T_{on}/(T_{on}+T_{off})$(4)	400 x $T_{on}/(T_{on}+T_{off})$(4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x $T_{on}/(T_{on}+T_{off})$(4)	205 x $T_{on}/(T_{on}+T_{off})$(4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to *Table 76: I/O static characteristics*.
4. T_{on} is the Refresh phase duration. T_{off} is the Hold phase duration. Refer to the reference manual for more details.

Figure 27. 12-bit buffered/non-buffered DAC



(1) The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

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Table 89. DAC accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	Monotonicity	10 bits		Guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF, CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF, CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF, CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF, CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF, CL ≤ 50 pF no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF, CL ≤ 50 pF, no RL, 1 kHz, BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF, CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	70.4	-	dB
		DAC output buffer OFF, CL ≤ 50 pF, no RL, 1 kHz		-	71	-	

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Table 89. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF, CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at code i and the value at code i on a line drawn between code 0 and last code 4095.
4. Difference between the value measured at code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

5.3.24 Comparator characteristics

Table 90. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN = 0 (bridge disabled)		-	200	300	nA
		BRG_EN = 1 (bridge enabled)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	V_{DDA} ≥ 2.7 V	-	-	5	µs
			V_{DDA} < 2.7 V	-	-	7	
		Medium mode	V_{DDA} ≥ 2.7 V	-	-	15	
			V_{DDA} < 2.7 V	-	-	25	
		Ultra-low-power mode		-	-	40	
t_D(3)	Propagation delay with 100 mV overdrive	High-speed mode	V_{DDA} ≥ 2.7 V	-	55	80	ns
			V_{DDA} < 2.7 V	-	55	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V_{offset}	Comparator offset error	Full common mode range		-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	

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Table 90. COMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 36: Embedded internal voltage reference*.
3. Guaranteed by characterization results.

5.3.25 Timers characteristics

Parameters given in the following tables are guaranteed by design. Refer to *Section 5.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 91. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	15.625	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	40	
Res_{TIM}	Timer resolution	TIM1, TIM16, TIM17	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.015625	1024	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	67.10	s

1. TIMx is used as a general term where x stands for 1, 2, 16 or 17.

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Table 92. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout (RL[11:0] = 0x000)	Max timeout (RL[11:0] = 0xFFF)	Unit
/4	0x0	0.125	512	ms
/8	0x1	0.250	1024	
/16	0x2	0.500	2048	
/32	0x3	1.0	4096	
/64	0x4	2.0	8192	
/128	0x5	4.0	16384	
/256	0x6 or 0x7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock, hence there is always a full RC period of uncertainty.

5.3.26 Communication interfaces characteristics

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): bitrate up to 100 Kbit/s
- Fast-mode (Fm): bitrate up to 400 Kbit/s
- Fast-mode Plus (Fm+): bitrate up to 1 Mbit/s

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to the reference manual) and when the II2CCLK frequency is greater than the minimum shown in the table below.

Table 93. Minimum I2CCLK frequency in all I2C modes

Symbol	Parameter	Conditions		Min	Unit
$f_{(I2CCLK)}$	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog filter ON, DNF = 0	8	
			Analog filter OFF, DNF = 1	9	
		Fast-mode Plus	Analog filter ON, DNF = 0	18	
			Analog filter OFF, DNF = 1	16	

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.
- The 20 mA output drive requirement in Fast-mode Plus is partially supported. This limits the maximum load C_{load} supported in Fast-mode Plus, given by these formulas:
  - $t_r(SDA/SCL) = 0.8473 \times R_p \times C_{load}$
  - $R_p(min) = [V_{DD} - V_{OL}(max)] / I_{OL}(max)$

    where R_p is the I2C lines pull-up. Refer to *Section 5.3.16: I/O port characteristics* for more details.

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All I2C SDA and SCL I/Os embed an analog filter (refer to the table below for its characteristics).

Table 94. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	100(3)	ns

1. Guaranteed by characterization.
2. Spikes with widths below $t_{AF(min)}$ filtered.
3. Spikes with widths above $t_{AF(max)}$ not filtered.

USART characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- OSPEEDRy[1:0] set to 10 (output speed)
- capacitive load C = 30 pF
- measurement points at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, and RX for USART).

Table 95. USART characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	6	MHz
		Slave mode	-	-	16	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker} + 5	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	
$t_{w(CKH)}$	CK high time	Master mode	1 / f_{CK} / 2 - 1	1 / f_{CK} / 2	1 / f_{CK} / 2 + 1	
$t_{w(CKL)}$	CK low time					
$t_{su(RX)}$	Data input setup time	Master mode	22	-	-	
		Slave mode	3	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0	-	-	
		Slave mode	1	-	-	
$t_{v(TX)}$	Data output valid time	Master mode	-	13	22	
		Slave mode	-	0.5	1	
$t_{h(TX)}$	Data output hold time	Master mode	10	-	-	
		Slave mode	0	-	-	

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SPI characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- output speed set to OSPEEDRy[1:0] = 11
- capacitive load C = 30 pF
- measurements done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 96. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 1.8 < V_{DD} < 3.6 V, Range 1	-	-	24	MHz
		Master transmitter mode 1.8 < V_{DD} < 3.6 V, Range 1			24	
		Slave receiver mode 1.8 < V_{DD} < 3.6 V, Range 1			24	
		Slave mode transmitter/full duplex 2.7 < V_{DD} < 3.6 V, Range 1			24(2)	
		Slave mode transmitter/full duplex 1.8 < V_{DD} < 3.6 V, Range 1			24(2)	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	3 x T_{PCLK}	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	2 x T_{PCLK}	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PCLK} - 1	T_{PCLK}	T_{PCLK} + 1	
$t_{su(MI)}$	Data input setup time	Master mode	1	-	-	ns
$t_{su(SI)}$		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6	-	-	
$t_{h(SI)}$		Slave mode	2	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	12	34	
$t_{dis(SO)}$	Data output disable time		9	10	16	

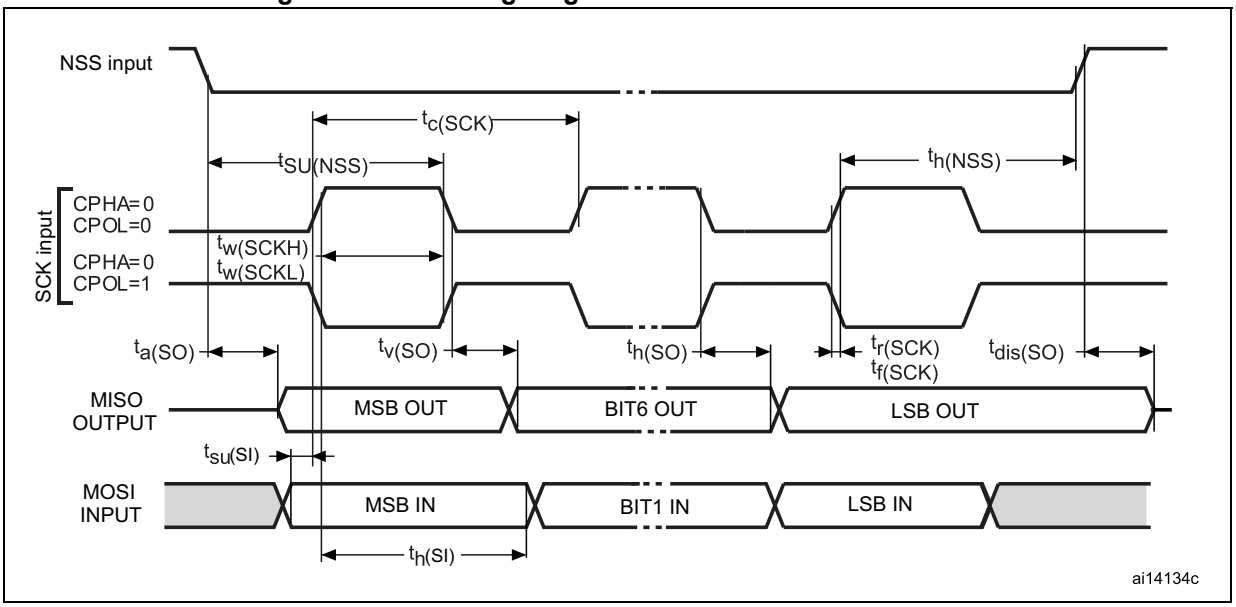
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Table 96. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode, 2.7 < V_{DD} < 3.6 V Range 1	-	10	13.5	ns
		Slave mode, 2.7 < V_{DD} < 3.6 V Range 2	-	17	18	
		Slave mode, 1.8 < V_{DD} < 3.6 V Range 1	-	10	20	
		Slave mode, 1.8 < V_{DD} < 3.6 V Range 2	-	17	24	
$t_{v(MO)}$		Master mode (after enable edge)	-	1	1.5	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	8	-	-	
$t_{h(MO)}$		Master mode (after enable edge)	0	-	-	

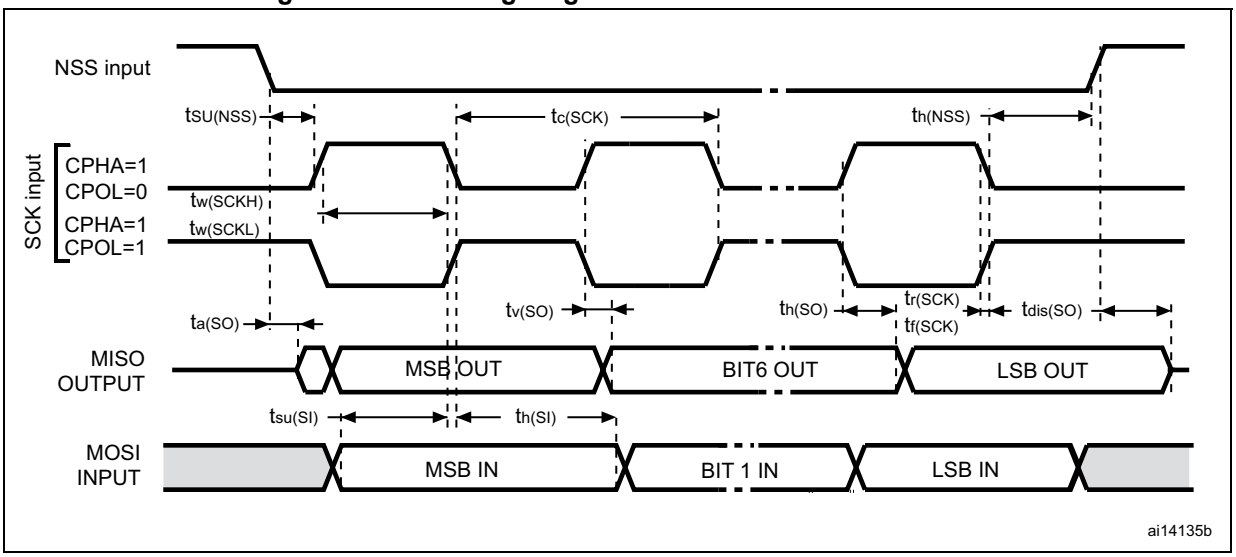
1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$, that has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.

Figure 28. SPI timing diagram - Slave mode and CPHA = 0



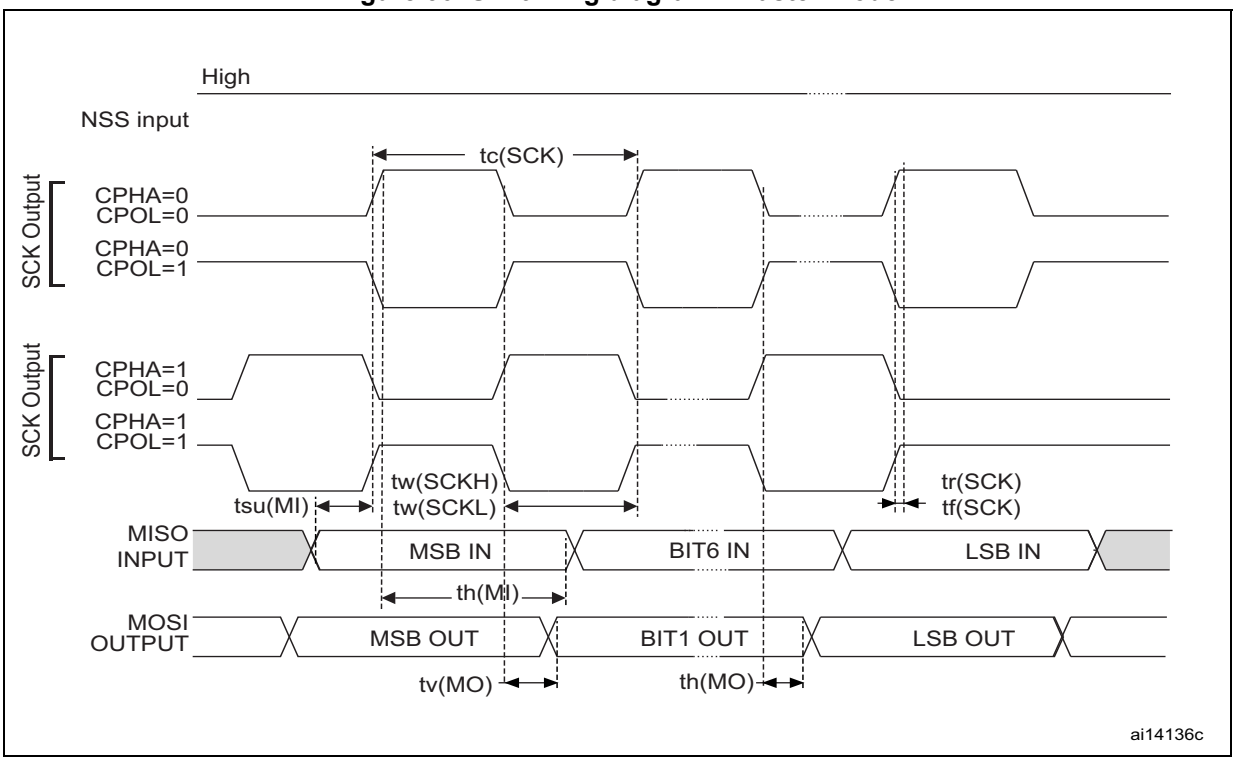
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Figure 29. SPI timing diagram - Slave mode and CPHA = 1



1. Measurement points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 30. SPI timing diagram - Master mode



1. Measurement points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

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JTAG/SWD characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 26: General operating conditions*, with the following configuration:

- capacitive load C = 30 pF
- measurement done at CMOS levels: 0.5 x V_{DD}.

Refer to *Section 5.3.16: I/O port characteristics* for more details.

Table 97. Dynamic JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP} $1/t_{c(TCK)}$	TCK clock frequency	2.7 V < V_{DD} < 3.6 V	-	-	33	MHz
		1.8 V < V_{DD} < 3.6 V	-	-	25	
$ti_{su(TMS)}$	TMS input setup time	-	0.5	-	-	ns
$ti_{h(TMS)}$	TMS input hold time	-	1	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	1	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	2.5	-	-	
$tov_{(TDO)}$	TDO output valid time	2.7 V < V_{DD} < 3.6 V	-	12	15	
		1.8 V< V_{DD} < 3.6 V	-	12	20	
$toh_{(TDO)}$	TDO output hold time	-	10	-	-	

Table 98. Dynamic SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP} $1/t_{c(SWCLK)}$	SWCLK clock frequency	2.7 V < V_{DD} < 3.6 V	-	-	58	MHz
		1.8 < V_{DD} < 3.6 V	-	-	41	
$ti_{su(SWDIO)}$	SWDIO input setup time	-	1	-	-	ns
$ti_{h(SWDIO)}$	SWDIO input hold time	-	2	-	-	
$tov_{(SWDIO)}$	SWDIO output valid time	2.7 V < V_{DD} < 3.6 V	-	15	17	
		1.8 V < V_{DD} < 3.6 V	-	15	24	
$toh_{(SWDIO)}$	SWDIO output hold time	-	9	-	-	

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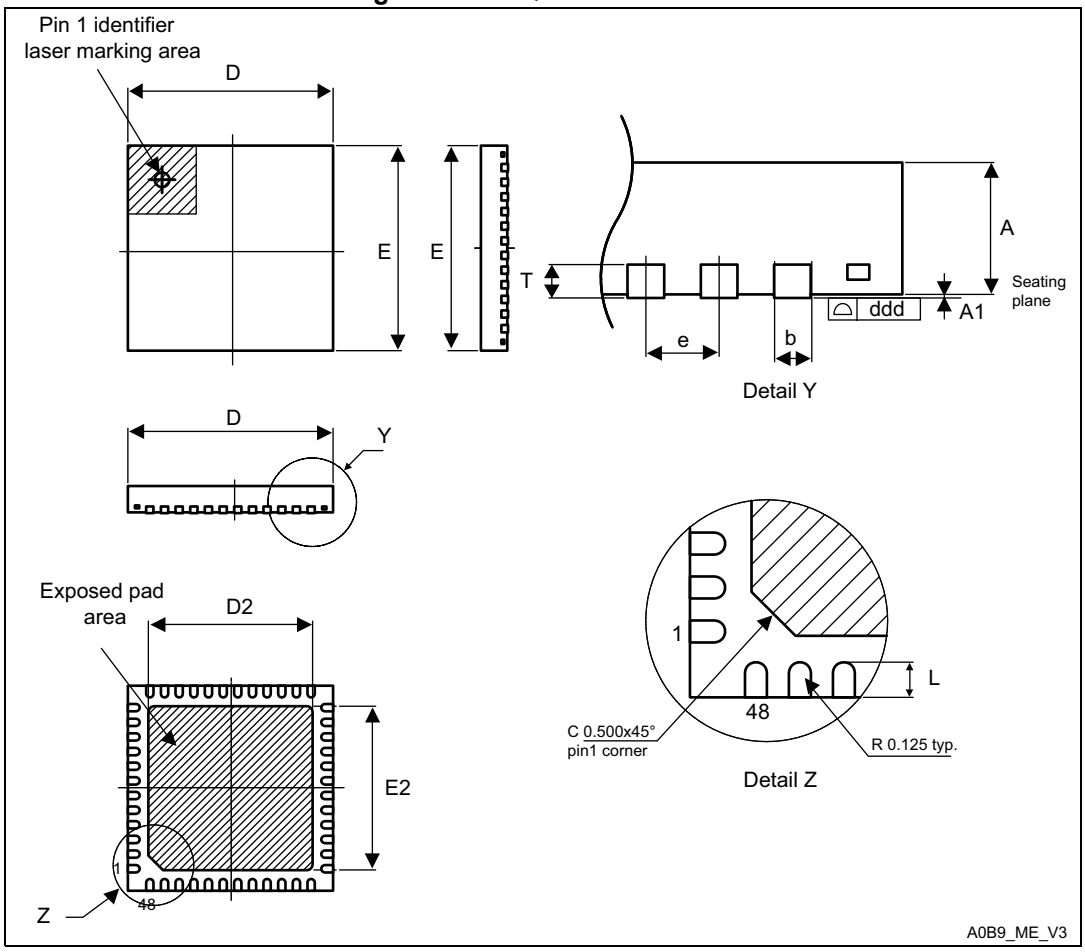
6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at *www.st.com*. ECOPACK is an ST trademark.

6.1 UFQFPN48 package information

This UFQFPN is a 48 leads, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 31. UFQFPN48 - Outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

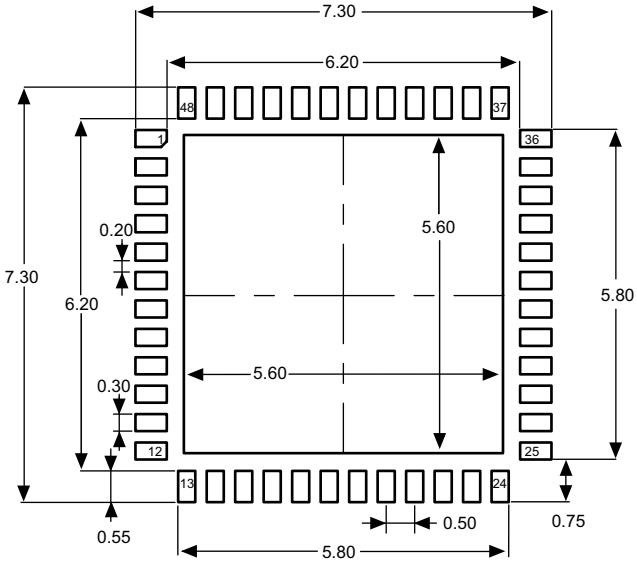
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Table 99. UFQFPN48 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 32. UFQFPN48 - Recommended footprint



1. Dimensions are expressed in millimeters.

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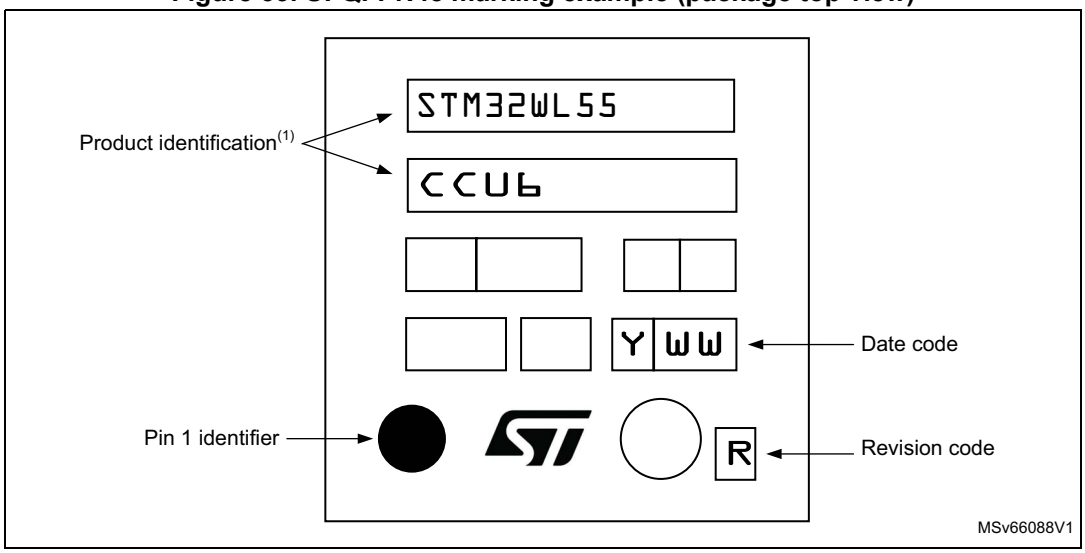
Device marking for UFQFPN48

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 33. UFQFPN48 marking example (package top view)



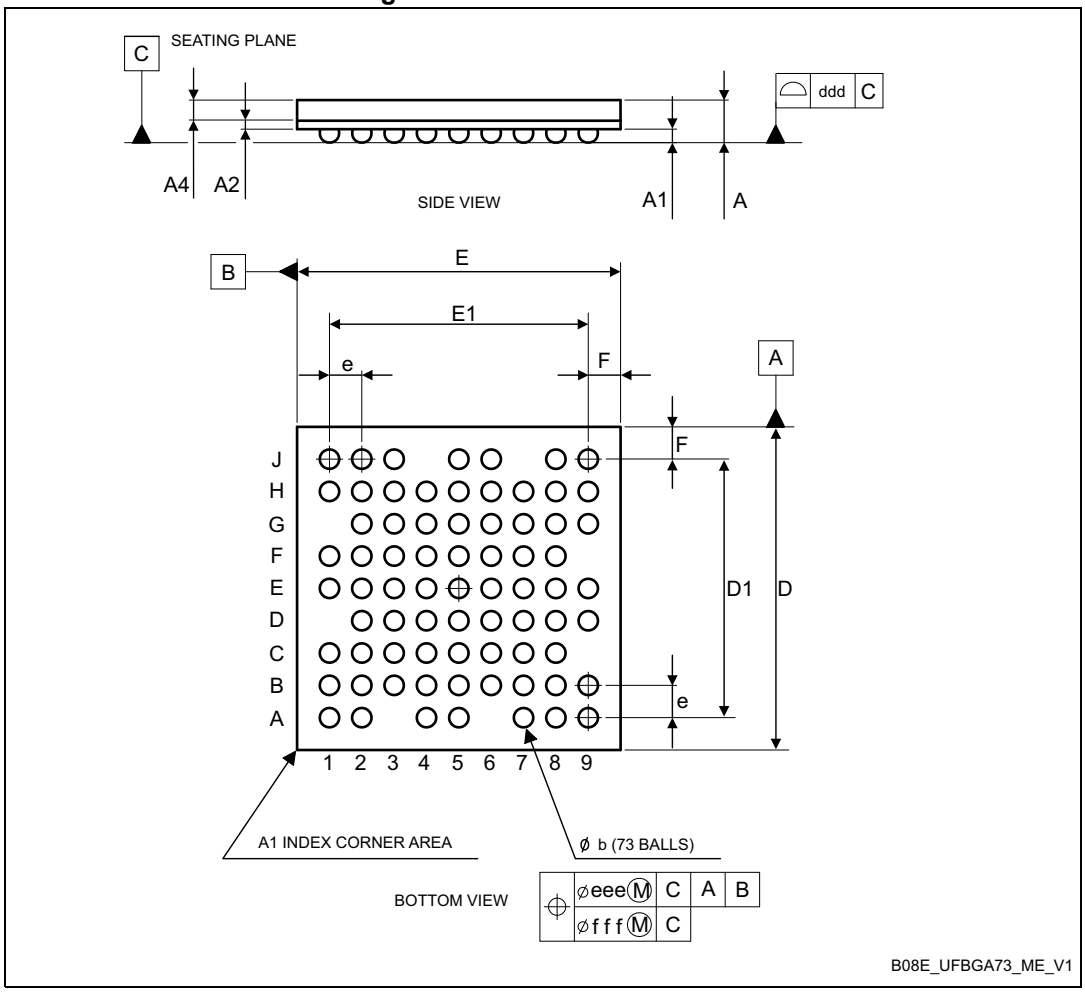
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6.2 UFBGA73 package information

This UFBGA is a 73 balls, 5 × 5 mm, ultra thin fine pitch ball grid array package.

Figure 34. UFBGA73 - Outline



1. Drawing is not to scale.
2. - The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
   - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 100. UFBGA73 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.60	-	-	0.236
A1	-	-	0.11	-	-	0.0043
A2	-	0.13	-	-	0.0051	-
A4	-	0.32	-	-	0.0126	-
b[3]	0.24	0.29	0.34	0.0094	0.0114	0.0134

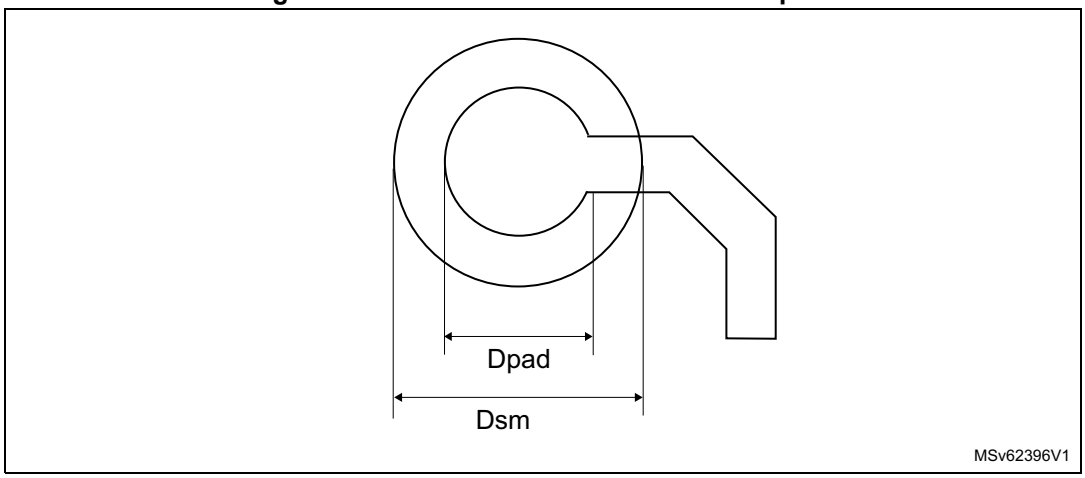
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Table 100. UFBGA73 - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	4.85	5.00	5.15	0.1909	0.1969	0.2028
D1	-	4.00	-	-	0.1575	-
E	4.85	5.00	5.15	0.1909	0.1969	0.2028
E1	-	4.00	-	-	0.1575	-
e	-	0.50	-	-	0.0197	-
F	-	0.50	-	-	0.0197	-
ddd	-	-	0.08	-	-	0.0031
eee[4]	-	-	0.15	-	-	0.0059
fff[5]	-	-	0.05	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. - UFBGA stands for Ultra-Thin Profile Fine Pitch Ball Grid Array.
   - Ultra Thin profile: 0.50 < A ≤ 0.65mm / Fine pitch: e < 1.00mm pitch.
   - The total profile height (Dim A) is measured from the seating plane to the top of the component
   - The maximum total package height is calculated by the following methodology:
   A Max = A1 Typ + A2 Typ + A4 Typ + $\sqrt{}$ (A1²+A2²+A4² tolerance values)
3. The typical balls diameters before mounting is 0.20 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 35. UFBGA73 - Recommended footprint



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Table 101. UFBGA recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.230 mm
Dsm	0.330 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm
Ball diameter	0.280 mm

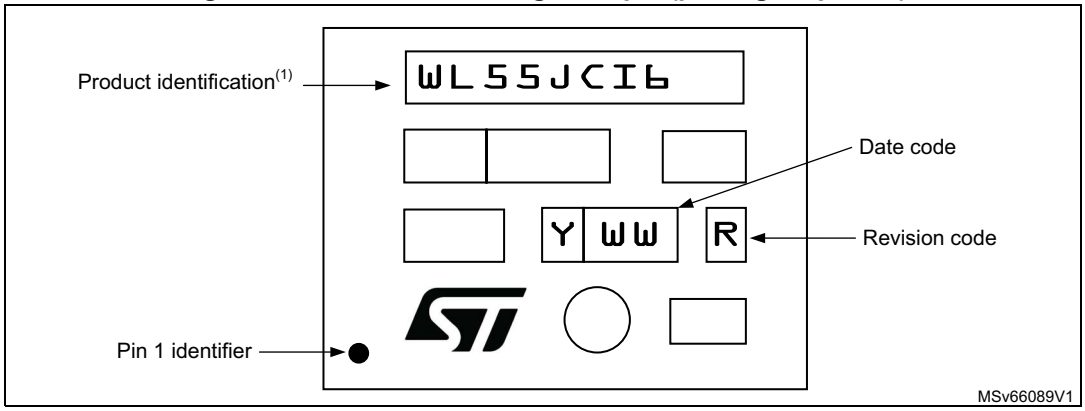
Device marking for UFBGA73

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 36. UFBGA73 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

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6.3 Package thermal characteristics

The maximum chip junction temperature (T_J max) must never exceed the values given in *Table 26: General operating conditions*.

The maximum chip-junction temperature, T_J max (in °C), can be calculated using the equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

where:

- T_A max is the maximum ambient temperature in °C.
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max).
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watt. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH})$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

When the SMPS is used, a portion of the power consumption is dissipated into the external inductor, therefore reducing the device power dissipation. This portion depends mainly on the inductor ESR characteristics.

As the radiated RF power is quite low (< 4 mW), it is not necessary to remove it from the device power consumption.

RF characteristics (such as sensitivity, Tx power consumption) are provided up to 85 °C.

Table 102. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient UFBGA73 - 5 x 5 mm UFQFPN48 - 7 x 7 mm	 43.4 27.4	°C/W
Θ_{JB}	Thermal resistance junction-board UFBGA73 - 5 x 5 mm UFQFPN48 - 7 x 7 mm	 27.2 11.7	
Θ_{JC}	Thermal resistance junction-top case UFBGA73 - 5 x 5 mm UFQFPN48 - 7 x 7 mm	 11 8.5	

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7 Ordering information

Example: STM32 WL 55 J C I 6 TR

Device family

STM32 = Arm based 32-bit microcontroller

Product type

WL = wireless long range

Device subfamily

55 = Cortex-M4, Cortex-M0+, full set of modulations
54 = Cortex-M4, Cortex-M0+, full set of modulations except LoRa

Pin/ball count

C = 48
J = 73

Flash memory size

C = 256 Kbytes

Package

I = UFBGA
U= UFQFPN

Temperature range

6 = -40 to 85 °C (105 °C junction)
7 = -40 to 105 °C (125 °C junction)

Packing

TR = tape and reel

xxx = programmed parts

For a list of available options (such as speed or package) or for further information on any aspect of this device, contact the nearest ST sales office.

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9 Revision history

Table 103. Document revision history

Date	Revision	Changes
9-Nov-2020	1	Initial release.
1-Jul-2021	2	Updated: – One sentence at the beginning of *Features* – *Table 26: Operating range of RF pads* – One sentence at the end of *Section 3.9.3: Transmitter* and *Section 3.9.4: Receiver* – *Section 3.9.1: Sub-GHz radio introduction* – Tx HP values in *Table 24: Main performances at VDD = 3 V* – I_{DD} (868-915MHz, +22 dBm) in *Table 28: Sub-GHz radio power consumption in transmit mode* – 48 MHz, 2.4 V in *Table 46: Current consumption during wakeup from Stop 2 mode* – 16 MHz, 2.4 V in *Table 48: Current consumption during wakeup from Stop 1 mode* – 4 MHz, range 1, 2.4 V in *Table 50: Current consumption during wakeup from Stop 0 mode* – *Table 59: HSE32 crystal requirements* – Reference added after *Table 60: HSE32 oscillator characteristics* – ATCXO in *Table 61: HSE32 TCXO regulator characteristics* – *Figure 22: ADC accuracy characteristics* and *Figure 23: Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function* – *Table 101: Package thermal characteristics*
21-Mar-2022	3	Updated: – *Table 2: Main features and peripheral count* – *Section 3.9.1: Sub-GHz radio introduction* – *Table 26: Operating range of RF pads* – WLCSP59 information removed from the whole document
5-Oct-2022	4	Updated: – *Features* and *Table 1: Device summary* – *Section 2: Description* – *Section 3.5.2: Embedded SRAM* – new *Section 3.9.7: IPDs for STM32WL and reference designs* – *Table 29: Sub-GHz radio power consumption in transmit mode* – *Section 7: Ordering information* – new *Section 8: Important security notice*

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