STM32H503xx

Arm® Cortex®-M33 32-bit MCU+FPU, 375 DMIPS, 250 MHz, 128 Kbytes flash memory, 32 Kbytes RAM, I3C

Datasheet - production data

Features

Includes ST state-of-the-art patented technology

Core

- Arm® Cortex®-M33 CPU with FPU, frequency up to 250 MHz, MPU, 375 DMIPS (Dhrystone 2.1), and DSP instructions

ART Accelerator

- 8-Kbyte instruction cache allowing 0-wait-state execution from flash memory (frequency up to 250 MHz)

Benchmarks

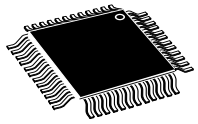
- 1.5 DMIPS/MHz (Drystone 2.1)
- 1023 CoreMark® (4.092 CoreMark®/MHz)

Memories

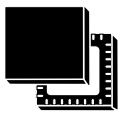
- 128 Kbytes of embedded flash memory with ECC, two banks of read-while-write
- 2-Kbyte OTP (one-time programmable)
- 32-Kbyte SRAM with ECC
- 2 Kbytes of backup SRAM (available in the lowest power modes)

Clock, reset, and supply management

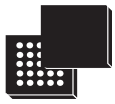
- 1.71 V to 3.6 V application supply and I/O
- POR, PDR, PVD, and BOR
- Embedded regulator (LDO)
- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- Two PLLs for system clock, USB, audio, and ADC
- External oscillators: 4 to 50 MHz HSE, 32.768 kHz LSE



LQFP64 (10 x 10 mm)
LQFP48 (7 x 7 mm)



UFQFPN48
(7 x 7 mm)
UFQFPN32
(5 x 5 mm)



WLCSP25
(2.33 x 2.24 mm)

Low-power modes

- Sleep, Stop and Standby modes
- V_{BAT} supply for RTC, 32 backup registers (32 bits)

General-purpose inputs/outputs

- Up to 49 fast I/Os with interrupt capability (most 5 V tolerant)
- Up to 9 I/Os with independent supply down to 1.08 V

Analog

- One 12-bit ADC, up to 2.5 MSPS
- One 12-bit dual-channel DAC
- One ultra-low-power comparator
- One operational amplifier (7 MHz bandwidth)

One digital temperature sensor

Up to 11 timers

- Six 16-bit (including two low-power 16-bit timer available in Stop mode) and one 32-bit timer
- Two watchdogs
- One SysTick timer
- RTC with hardware calendar, alarms, and calibration

This is information on a product in full production.

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Communication interfaces

- Up to two I2Cs FM + interfaces (SMBus/PMBus®)
- Up to two I3Cs shared with I2C
- Up to three USARTs (ISO7816 interface, LIN, IrDA, modem control) and one LPUART
- Up to three SPIs including three muxed with full-duplex I2S for audio class accuracy via internal audio PLL or external clock and up to three additional SPI from three USART when configured in synchronous mode
- One FDCAN
- One USB 2.0 full-speed host and device

Two DMA controllers to offload the CPU

Security

- HASH (SHA-1, SHA-2), HMAC
- True random generator
- 96-bit unique ID
- Active tamper

Debug

- Authenticated debug
- Serial wire-debug (SWD) and JTAG interfaces

ECOPACK2 compliant packages

Table 1. Device summary

Reference	Part numbers
STM32H503xx	STM32H503EB, STM32H503KB, STM32H503CB, STM32H503RB

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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32H503xx microcontrollers.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32H503xx errata sheet.

For information on the Arm®(a) Cortex®-M33 core, refer to the Cortex®-M33 Technical Reference Manual, available from the www.arm.com website.

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2 Description

The STM32H503xx devices are a high-performance microcontrollers family (STM32H5 series) based on the high-performance Arm® Cortex®-M33 32-bit RISC core. They operate at a frequency of up to 250 MHz.

The Cortex®-M33 core features a single-precision floating-point unit (FPU) that supports all the Arm® single-precision data-processing instructions and all the data types.

The Cortex®-M33 core also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (128 Kbytes of dual bank flash memory and 32 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to three APB buses, three AHB buses, and a 32-bit multi-AHB bus matrix.

The devices feature several protection mechanisms for embedded flash memory and SRAM: secure life cycle management, write protection and hide protection areas.

The devices embed several peripherals reinforcing security: a HASH hardware accelerator and a true random number generator.

The devices offer active tamper detection and protection against transient and environmental perturbation attacks. It is done thanks to several internal monitoring that generate a secret data erase in case of an attack.

The devices offer a fast 12-bit ADC, two DAC channels, an OPAMP, a comparator, a low-power RTC, one 32-bit general-purpose timer, one 16-bit PWM timer dedicated to motor control, one 16-bit general-purpose timer, two 16-bit basic timers and two 16-bit low-power timers.

The devices also feature standard and advanced communication interfaces such as: two I²Cs, two I3Cs shared with I²C, three SPIs with muxed full-duplex I2S, three USARTs and one low-power UART, one FDCAN, and one USB full-speed.

The devices operate in the - 40 to + 85 °C/105 °C, and up to 125 °C at low dissipation (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply.

A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported like an analog independent supply input for ADC, DACs, COMP and OPAMP, and a dedicated supply input for some GPIOs. A VBAT input is available for connecting a backup battery. This battery preserves the RTC functionality and backup 32x 32-bit registers and 2-Kbyte SRAM.

The devices offer five packages from 25-pin to 64-pin.

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Table 2. STM32H503xx features and peripheral counts

Peripherals		STM32H503EB	STM32H503KB	STM32H503CB	STM32H503RB
Flash memory (Kbytes)		128			
SRAM	System (Kbytes)	32 (16 +16)			
	Backup (bytes)	2 Kbytes			
Timers	Advanced control	1 (16 bits)			
	General purpose	1 (32 bits) and 1 (16 bits)			
	Basic	2 (16 bits)			
	Low power	2 (16 bits)			
	SysTick timer	1			
	Watchdog timers (independent, window)	2			
Communication interfaces	SPI/I2S	3 / 3			
	I2C	2			
	I3C(1)	2			
	USART	3			
	LPUART	1			
	FDCAN	1			
	USB	Yes			
Real-time clock (RTC)		Yes			
Tamper pins		1		2	
Active tampers		0		1	
True random number generator		Yes			
HASH (SHA-256)		Yes			
GPIOs Wakeup pins Number of I/Os down to 1.08 V		19 2(2) 9(3)	24 3 0	35 4 0	49 5 0
ADC	12-bit ADC	1			
	Number of channels	10			16
DAC	12-bit DAC controller	1			
	Number of channels	1	2		
Comparator		1			
Operational amplifier		1(4)			
Maximum CPU frequency		250 MHz			

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Table 2. STM32H503xx features and peripheral counts (continued)

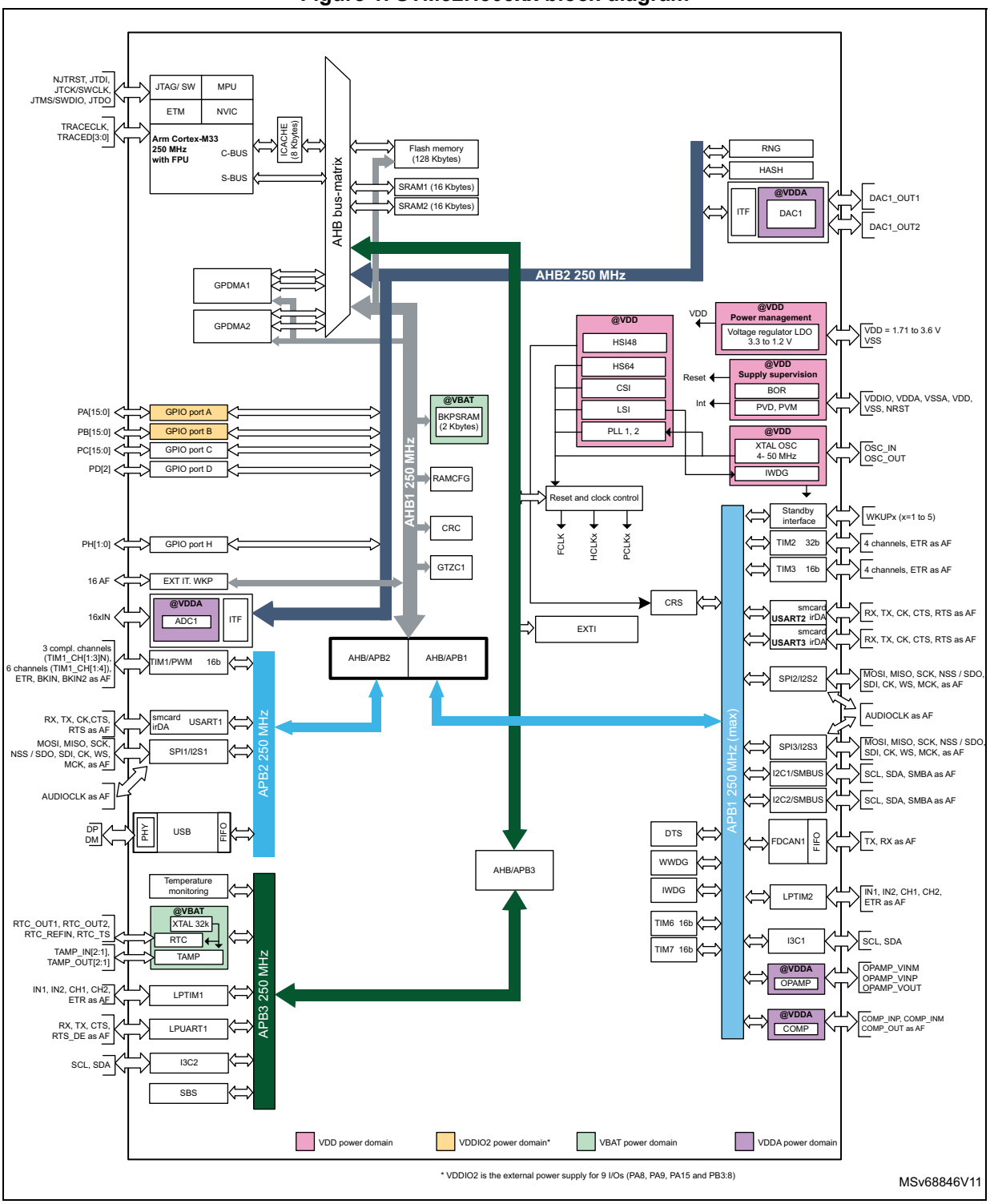
Peripherals	STM32H503EB	STM32H503KB	STM32H503CB	STM32H503RB
Operating voltage	1.71 to 3.6 V			
VDDIO2 separate supply pin(5)	1	-		
Operating temperature	Ambient operating temperature: – -40 to 85 °C/105° C, up to 125 °C at low dissipation Junction temperature: – Voltage range VOS0 (up to 250 MHz): T_j from -40 to 105 °C – Voltage range VOS1 (up to 200 MHz): T_j from -40 to 130 °C			
Package	WLCSP25	UFQFPN32	UFQFPN48 LQFP48	LQFP64

1. I3C1 and I3C2 shares respectively the same IOs than I2C1 and I2C2.
2. Two wakeup pins (PA0 and PB7) from standby are available on the WLCSP25 package. Note that the PB7 pin can only be used when the V_{DDIO2} supply is present.
3. On WLCSP package nine I/Os (PA8, PA9, PA15, and PB[3:8]) have a dedicated supply pin VDDIO2. They can only be used when the VDDIO2 pin is connected to a valid power supply.
4. OPAMP1_VINM is not available on the WLCSP25 package.
5. The dedicated V_{DDIO2} supply is only available on the WLCSP25 package, it represents the external power supply for nine I/Os (PA8, PA9, PA15, and PB[3:8]).

Note: V_{REF+} and V_{DDA} are mapped on the same pin on all packages (no VREF+ separate pin).

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Figure 1. STM32H503xx block diagram



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3 Functional overview

3.1 Arm Cortex-M33 core with FPU

The Cortex-M33 with FPU is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex-M33 processor delivers a high-computational performance with low-power consumption and an advanced response to interrupts. It features:

- Memory protection units (MPUs), supporting eight regions
- Floating-point arithmetic functionality with support for single precision arithmetic

The processor supports a set of DSP instructions that allows an efficient signal processing and a complex algorithm execution.

The Cortex-M33 processor supports the following bus interfaces:

- System AHB bus:

  The system AHB (S-AHB) bus interface is used for any instruction fetch and data access to the memory-mapped SRAM, peripheral, or Vendor_SYS regions of the Armv8-M memory map.
- Code AHB bus:

  The code AHB (C-AHB) bus interface is used for any instruction fetch and data access to the code region of the Armv8-M memory map.

Figure 1 shows the general block diagram of the STM32H503xx devices.

3.2 ART Accelerator (ICACHE)

3.2.1 Instruction cache (ICACHE)

The instruction cache (ICACHE) is introduced on the C-AHB code bus of the Cortex-M33 processor to improve performance when fetching instruction (or data) from internal memories.

ICACHE offers the following features:

- Multibus interface:
  - Slave port receiving the memory requests from the Cortex-M33 C-AHB code execution port
  - Master port performing refill requests to internal memories (flash memory and SRAMs)
  - A second slave port dedicated to ICACHE registers access
- Close to zero wait-states instructions/data access performance:
  - 0 wait-state on cache hit
  - Hit-under-miss capability, allowing to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
  - Critical-word-first refill policy, minimizing processor stalls on cache miss

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  - Hit ratio improved by two-ways set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - Optimal cache line refill thanks to AHB burst transactions (of the cache line size)
  - Performance monitoring by means of a hit counter and a miss counter
- Extension of cacheable region beyond the code memory space, by means of address remapping logic that allows four cacheable external regions to be defined
- Power consumption is reduced intrinsically with more accesses to cache memory rather than to bigger main memories. It is even improved by configuring ICACHE as a direct mapped rather than the default two-ways set-associative mode
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory. It also prevents one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to eight protected areas.

The MPU is especially helpful for applications where some critical or certified code must be protected against the misbehavior of other tasks. An RTOS (real-time operating system) usually manages the MPU.

If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

3.4 Embedded flash memory

The devices feature 128 Kbytes of embedded flash memory that is available for storing programs and data.

The flash memory interface features:

- Dual-bank operating modes
- Read-while-write (RWW)

This allows a read operation to be performed from one bank while an erase or program operation is performed to the other bank. Each bank contains eight pages of 8 Kbytes.

The flash memory embeds 2-Kbytes OTP (one-time programmable) for user data.

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Enhanced flash memory protection mechanisms are available. These mechanisms can be activated by option bytes:

- Different product states for protecting memory content from debug access
- Write protection (WRP) to protect areas against erasing and programming. Two areas per bank can be selected with 8-Kbyte granularity.
- Sector group write-protection (WRPSG), protecting up to 32 groups of four sectors (32 Kbytes) per bank
- One HDP area per bank providing temporal isolation for startup code

The whole nonvolatile memory embeds the error correction code (ECC) feature supporting:

- Single-error detection and correction
- Double-error detection
- ECC fail address report

3.4.1 Flash privilege protection

Each flash memory sector can be programmed on the fly as privileged or unprivileged.

3.5 Embedded SRAMs

Three SRAMs are embedded in the STM32H503xx devices, each with specific features. SRAM1 and SRAM2 are the main SRAMs.

These SRAMs are made of several blocks that can be powered down in Stop mode to reduce consumption:

- SRAM1: 16 Kbytes with ECC
- SRAM2: 16 Kbytes with ECC
- BKPSRAM (backup SRAM): 2 Kbytes with ECC. The BKPSRAM can be retained in all low-power modes and when V_{DD} is off in VBAT mode.

Note: ECC is by default disabled on SRAM1, SRAM2, and BKPSRAM, it can be enabled by clearing the option bit SRAM1_ECC, SRAM2_ECC, and BKPRAM_ECC respectively.

3.5.1 SRAMs privilege protection

The SRAM1 and SRAM2 can be programmed as privileged or nonprivileged by blocks, using the MPCBB. The granularity of SRAM privilege block based is a page of 512 bytes.

Backup SRAM regions can be programmed as privileged or nonprivileged with watermark, using the TZSC (privilege controller) in the GTZC (global privilege controller).

3.6 Boot modes

At startup, the BOOT0 pin allows the system to boot either from the user Flash or from the bootloader.

When boot from user Flash is selected, NSBOOTADD defines the boot address. This address can be locked thanks to NSBOOT_LOCK.

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When boot from bootloader is selected, the bootloader (natively embedded in the flash memory) is launched allowing to reprogram the flash memory by using USART, I2C, I3C, SPI, FDCAN, or USB in device mode through the DFU (device firmware upgrade).

The debug authentication feature can be launched from STMicroelectronics tools (such as STM32CubeProgrammer or IDEs). An authentication password should be used for debug authentication in order to launch a full regression of the product.

For more details about system configuration and boot modes, refer to the product reference manual.

The embedded bootloader is located in the system memory, programmed by STMicroelectronics during production. It is used to reprogram the flash memory by using USART, I2C, I3C, SPI, FDCAN, or USB in device mode through the DFU (device firmware upgrade).

Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more information.

3.7 Global privilege controller (GTZC)

GTZC is used to configure privileged attributes within the full system.

The GTZC includes two different subblocks:

- TZSC: privilege controller
  This subblock defines the privilege state of slave/master peripherals. It also controls the privileged area size for the watermark memory peripheral controller (MPCWM). The TZSC block informs some peripherals (such as RCC or GPIOs) about the privilege status of each privileged peripheral, by sharing with RCC and I/O logic.
- MPCBB: block-based memory protection controller
  This subblock controls the privilege states of all memory blocks (512-byte pages) of the associated SRAM. This peripheral aim at configuring the internal RAM in a privileged system product having segmented SRAM with programmable privilege attributes.

The GTZC main features are:

- Two independent 32-bit AHB interfaces for TZSC and MPCBB
- Privileged and unprivileged access to TZSC and MPCBB
- Set of registers to define product-privileged settings:
  - Privileged blocks for internal SRAMs (with MPCBB)
  - Privileged regions for internal backup SRAM (with MPCWM)
  - Privileged access mode for peripherals
  - Privileged access mode for masters

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3.8 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domains (V_{CORE})
  - VDD domain
  - Backup domain (V_{BAT})
  - Analog domain (V_{DDA})
  - VDDIO2 domain
- System supply voltage regulation
  - Voltage regulator (LDO)
- Power supply supervision
  - POR/PDR monitor
  - BOR monitor
  - PVD monitor
- Power management
  - Operating modes
  - Voltage-scaling control
  - Low-power modes
- VBAT battery charging
- Privilege protection

3.8.1 Power supply schemes

The devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the internal regulator, and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- V_{DDA} = 1.62 V (ADC, COMP) or 1.8 V (DAC) or 2.0 V (OPAMP) to 3.6 V

  V_{DDA} is the external analog power supply for ADCs, DACs, operational amplifier, and comparator. The V_{DDA} voltage level is independent from the V_{DD} voltage and must preferably be connected to V_{DD} when these peripherals are not used.
- V_{DDIO2} = 1.08 V to 3.6 V

  V_{DDIO2} is the external power supply for nine I/Os (PA8, PA9, PA15, PB3:8). The V_{DDIO2} voltage level is independent from the V_{DD} voltage and must preferably be connected to VDD when those pins are not used.
- V_{BAT} = 1.2 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator, and backup registers (through power switch) when V_{DD} is not present.
- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs.

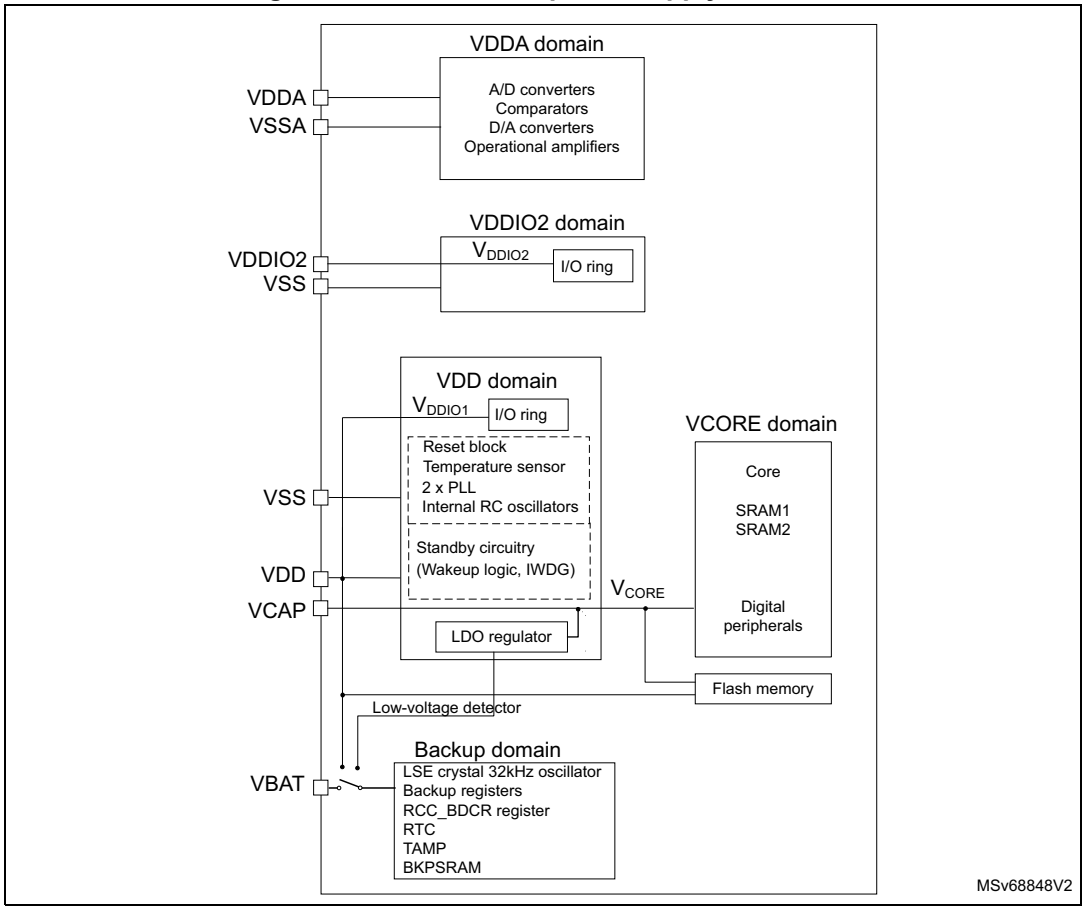
  VREF- and VREF+ pins are not available and they are bonded to VSSA and VDDA, respectively.

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The STM32H503xx devices embed an LDO regulator to provide the V_{CORE} supply for digital peripherals, SRAM1, SRAM2, and embedded flash memory. The LDO generates this voltage on the VCAP pin connected to an external capacitor of 2x 2.2 µF typical.

The LDO regulator can provide four different voltages (voltage scaling) and can operate in Stop modes.

Figure 2. STM32H503xx power supply overview



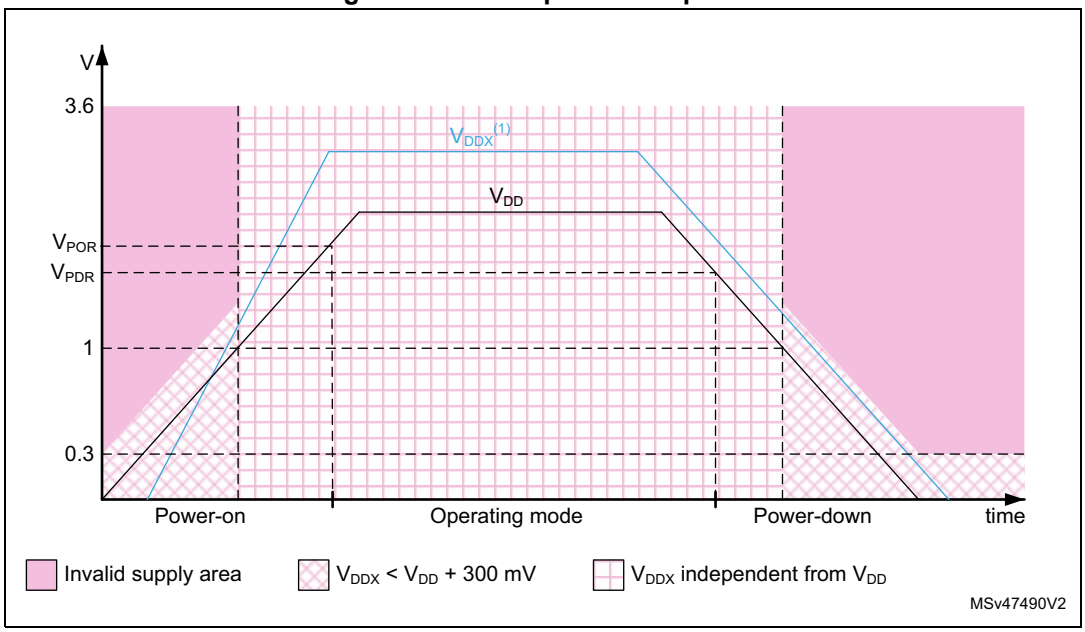
During power-up and power-down phases, the following power sequence requirements must be respected (refer to *Figure 3: Power-up/down sequence*):

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external-decoupling capacitors to be discharged with different time constants during the power-down-transient phase.

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Figure 3. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA} and V_{DDIO2}.

3.8.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a brownout reset (BOR) circuitry:

- Power-on reset (POR)
  The POR supervisor monitors the VDD power supply and compares it to a fixed threshold. The devices remain in reset mode when VDD is below this threshold.
- Power-down reset (PDR)
  The PDR supervisor monitors the VDD power supply. A reset is generated when VDD drops below a fixed threshold.
- Brownout reset (BOR)
  The BOR supervisor monitors VDD power supply. It can be enabled/disabled through BORH_EN option bit. Once enabled, three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when VDD drops below this threshold.
- Programmable voltage detector (PVD)
  The PVD monitors the VDD power supply by comparing it with a threshold selected from a set of predefined values.
  It can also monitor the voltage level of the PVD_IN pin by comparing it with an internal VREFINT voltage reference level.
  An interrupt can be generated when VDD drops below the VPVD threshold and/or when VDD is higher than the VPVD threshold. The interrupt service routine can then

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generate a warning message and/or put the device into a safe state. The PVD is enabled by software

- Analog voltage detector (AVD)
  The AVD monitors the VDDA power supply by comparing it with a threshold selected from a set of predefined values.
- VDDIO2 voltage monitor (IO2VM)
  The IO2VM monitors the independent supply voltage VDDIO2 to ensure that the peripheral is in its functional supply range.
- Backup domain voltage monitoring
  The backup domain voltage level (VBAT battery voltage) can be monitored by comparing it with two thresholds levels.
- Temperature monitoring
  A dedicated temperature sensor monitors the junction temperature and compare it with two threshold levels.

3.8.3 Voltage regulator

The devices support dynamic voltage scaling to optimize power consumption in Run mode.

The voltage regulator output, which supplies the logic (V_{CORE}), can be adjusted according to application needs through the following power supply levels:

- Run mode (VOS0 to VOS3)
  - Scale 0 (VOS0) and scale 1 (VOS1): high performance
  - Scale 2 (VOS2): balanced mode with medium performance and consumption
  - Scale 3 (VOS3): optimized power consumption
- Stop mode (SVOS3 to SVOS5)
  - Scale 3 (SVOS3): peripheral with wakeup from stop mode capabilities (such as UART, SPI, I2C, LPTIM) can be kept operational.
  - Scale 4 and 5 (SVOS4 and SVOS5): reduced set of peripherals (including GPIOs through EXTI) with wakeup from Stop capability.

Regulator bypass (Regulator OFF)

When V_{CORE} is supplied in bypass mode, the V_{CORE} voltage must first settle at a default level higher than 1.1 V.

Due to the LDO default state after power-up (enabled by default), the external V_{CORE} voltage must remain higher than 1.1 V until the LDO is disabled by software.

When the LDO is disabled, the external V_{CORE} voltage can be adjusted according to the user application needs.

Low-power modes

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** modes

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Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the V_{CORE} domain are stopped, the PLL, the CSI, the HSI, the HSI48, and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

The system clock when exiting from Stop mode can be either HSI up to 64 MHz or CSI (4 MHz), depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The PLL, the HSI, the CSI, the HSI48, and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The BOR always remains active in Standby mode.

  The I/Os state during Standby mode can be retained.

  After entering Standby mode, SRAMs and register contents are lost except for registers and backup SRAM in the backup domain and Standby circuitry.

  The device exits Standby mode in the following cases:

  - in an external reset with NRST pin)

  - in an IWDG reset

  - in a WKUP pin event (configurable rising or falling edge)

  - when an RTC event occurs (alarm, periodic wakeup, timestamp),

  - or in a tamper detection. The tamper detection can be raised either due to external pins or due to an internal failure detection.

  The system clock after wakeup is HSI at 32 MHz.

3.8.4 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is “disable”).

3.8.5 VBAT operation

The VBAT pin allows the device VBAT domain to be powered from an external battery or an external super-capacitor.

The VBAT pin supplies the RTC with LSE, antitamper detection (TAMP), backup registers, and 2-Kbyte backup SRAM. Two antitamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from V_{BAT}, the external interrupts nor the RTC alarm/events exit the microcontroller from the VBAT operation.

3.9 Peripheral interconnect matrix

Several peripherals have direct connections between them. These connections allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

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Depending on the peripherals, these interconnections can operate in Run and Sleep modes.

3.10 Reset and clock controller (RCC)

The clock controller distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- **Clock prescaler:** in order to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Clock security system:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals, or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 50 MHz high-speed external crystal or ceramic resonator (HSE) that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 64 MHz high-speed internal RC oscillator (HSI), trimmable by software that can supply a PLL.
  - 4 MHz low-power internal oscillator (CSI), trimmable by software that can supply a PLL.
  - System PLL that can be fed by HSE, HSI, or CSI, with a maximum frequency at 250 MHz.
- **RC48 with clock recovery system (HSI48):** internal 48 MHz clock source (HSI48) can be used to drive the USB.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog.
- **Peripheral clock sources:** several peripherals have their own independent clock whatever the system clock. Two PLLs, each having two independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, USB, RNG and FDCAN1.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 32 MHz clock (HSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If an HSE clock failure occurs, the master clock automatically switches to HSI, and a software interrupt is generated if enabled. LSE failure can also be detected and generates an interrupt.
- Clock-out capability:
  - **MCO (microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

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– **LSCO (low-speed clock output):** it outputs LSI or LSE in all low-power modes (except Standby and VBAT).

Several prescalers allow AHB and APB frequencies configuration. The maximum frequency of the AHB and the APB clock domains is 250 MHz.

3.11 Clock recovery system (CRS)

The devices embed a special block that allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device-operational range. This automatic trimming is based on the external synchronization signal. This signal is either derived from USB SOF signalization, from an LSE oscillator, from an external signal on the CRS_SYNC pin or generated by user software. For faster lock-in during startup, automatic-trimming and manual-trimming action can be combined.

3.12 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

In order to avoid spurious writing to the I/Os registers, if needed, the I/Os alternate function configuration can be locked following a specific sequence

On WLCSP25, nine IOs (PA8, PA9, PA15, PB3:8) can be independently supplied by a dedicated VDDIO2 supply.

The I/O high-speed low-voltage feature (HSLV) should be activated in order to maximize the I/O performance when the device is operating at low voltage.

This is needed to achieve the performance required for communication interface peripherals such SPI. The HSLV feature must be used only when the supply voltage (VDD or VDDIO2) is lower than 2.7 V. To enable it, the corresponding HSLV user option bit (IO_VDD_HSLV or IO_VDDIO2_HSLV) and the HSLVx bits should be set.

3.13 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all the masters (CPU, GPDMA1, GPDMA2) and the slaves (flash memory, SRAMs, AHB, and APB) peripherals. It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

3.14 General-purpose direct memory access controller (GPDMA)

The general-purpose direct memory access (GPDMA) controller is a bus master and system peripheral.

The GPDMA is used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU.

The GPDMA main features are:

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- Dual bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Sleep mode
- Transfers arbitration based on a four-grade-programmed priority at a channel level:
  - One high-priority traffic class, for time-sensitive channels (queue 3)
  - Three low-priority traffic classes, with a weighted round-robin allocation for non-time-sensitive channels (queues 0, 1, 2)
- Per channel event generation, on any of the following events: transfer complete or half transfer complete or data transfer error or user setting error, and/or update linked-list item error or completed suspension
- Per channel interrupt generation, with separately programmed interrupt enable per event
- 8 concurrent DMA channels:
  - Per channel FIFO for queuing source and destination transfers
  - Intra-channel DMA transfers chaining via a programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
  - Intra-channel and interchannel DMA transfers chaining via programmable DMA input triggers connection to DMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - 12 channels with linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - Four channels with 2D source and destination addressing: programmable-signed address offsets between successive burst transfers (noncontiguous addressing

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within a block, combined with programmable-signed address offsets between successive blocks, at a second-2D/repeated block level)
  - Support for scatter-gather (multibuffer transfers), data interleaving and deinterleaving via 2D addressing
  - Programmable DMA request and trigger selection
  - Programmable DMA half-transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the DMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting including FIFO level and event flags
- Privileged/unprivileged support:
  - Support for privileged and unprivileged DMA transfers, independently at a channel level
  - Privileged-aware AHB slave port.

3.15 Interrupts and events

3.15.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller that is able to manage 16 priority levels and to handle up to 134 maskable interrupt channels plus the 16 interrupt lines of the Cortex-M33.

The NVIC benefits are the following:

- Closely coupled NVIC giving low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.15.2 Extended interrupt/event controller (EXTI)

The EXTI handles up to 54 independent event/interrupt lines, it manages the individual CPU, and system wakeup through configurable event inputs. It provides wakeup requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU, an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wakeup requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run modes. The EXTI also includes the EXTI multiplexer IO port selection.

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The EXTI main features are the following:

- All event inputs allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Selectable active trigger edge
  - Interrupt pending status register bit independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wakeup, interrupt, and event generation
  - Software trigger possibility
- EXTI IO port selection

3.16 Cyclic redundancy check calculation unit (CRC)

The CRC is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime that can be ulteriorly compared with a reference signature generated at link time and that can be stored at a given memory location.

3.17 Analog-to-digital converter (ADC1)

The devices embed one successive approximation analog-to-digital converter.

Table 3. ADC features

ADC modes/features[1]	ADC1
Resolution	12 bits
Maximum sampling-speed	2.5 Msps
Hardware-offset calibration	X
Single-ended inputs	X
Differential inputs	X
Injected channel conversion	X
Oversampling	up to x1024
Data register	32 bits
DMA support	X
Offset compensation	X
Gain compensation	X
Number of analog watchdogs	3

1. X = supported.

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3.17.1 Analog temperature sensor

The STM32H503xx embed an analog temperature sensor that generates a voltage V_{SENSE} that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel that is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it must be calibrated to obtain a good accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by STMicroelectronics in the system memory area, accessible in read-only mode.

3.17.2 Digital temperature sensor (DTS)

The STM32H503xx embed a sensor that converts the temperature into a square wave, which frequency is proportional to the temperature. The PCLK or the LSE clock can be used as a reference clock for the measurements. A formula given in the product reference manual (RM0492) allows to calculate the temperature according to the measured frequency stored in the DTS_DR register.

3.17.3 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to the ADC input channel.

The precise voltage of VREFINT is individually measured for each part by STMicroelectronics during production test and stored in the system memory area. It is accessible in read-only mode.

3.17.4 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage by using the ADC input channel. As the V_{BAT} voltage may be higher than the V_{DDA}, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by four. As a consequence, the converted digital value is a quarter of the V_{BAT} voltage.

3.18 Digital to analog converter (DAC)

The DAC module is a 12-bit, voltage output digital-to-analog converter. The DAC can be configured in 8- or 12-bit mode and may be used in conjunction with the DMA controller. In 12-bit mode, the data may be left- or right-aligned.

The DAC features two output channels, each with its own converter. In dual DAC channel mode, conversions can be done independently or simultaneously when both channels are grouped together for synchronous update operations.

The DAC_OUTx pin can be used as a general-purpose input/output (GPIO) when the DAC output is disconnected from the output pad and connected to the on-chip peripheral. The DAC output buffer can be optionally enabled to allow a high drive output current. An

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individual calibration can be applied on each DAC output channel. The DAC output channels support a low-power mode, the sample and hold mode.

The digital interface supports the following features:

- One DAC interface, maximum two output channels
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave and triangular-wave generation
- Sawtooth wave generation
- Dual DAC channel for independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- Double data DMA capability to reduce the bus activity
- External triggers for conversion
- DAC output-channel buffered/unbuffered modes
- Buffer offset calibration
- Each DAC output can be disconnected from the DAC_OUTx output pin
- DAC output connection to on-chip peripherals
- Sample and hold mode for low-power operation in Stop mode.
- Voltage reference input

3.19 Ultra-low-power comparators (COMP)

The STM32H503xx devices embed a comparator COMP1 with a programmable reference voltage (internal or external), hysteresis, and speed (low speed for low-power) as well as selectable output polarity.

The reference voltage can be one of the following:

- An external I/O
- A DAC output channel
- An internal reference voltage or submultiple (1/4, 1/2, 3/4)
- The analog temperature sensor
- The VBAT/4 supply.

The comparator can wake up from Stop mode, generate interrupts and breaks for the timers.

3.20 Operational amplifiers (OPAMP)

The STM32H503xx devices embed an operational amplifier OPAMP1 with external or internal follower routing and PGA capability, and two inputs and one output. These three I/Os can be connected to the external pins, thus enabling any type of external interconnections. The operational amplifier can be configured internally as a follower, as an amplifier with a noninverting gain ranging from 2 to 16 or with an inverting gain ranging from -1 to -15.

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The main features of the operational amplifier are:

- PGA with a noninverting gain ranging of 2, 4, 8 or 16 or inverting gain ranging of -1, -3, -7 or -15
- One positive input connected to the DAC
- Output connected to internal ADC
- Low input bias current down to 1 nA
- Low input offset voltage down to 1.5 mV
- Gain bandwidth up to 7 MHz

3.21 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a nondeterministic random bit generator (NDRBG).

The true random generator:

- delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage
- can be used as an entropy source to construct a nondeterministic random bit generator (NDRBG)
- produces four 32-bit random samples every 412 AHB clock cycles if f_{AHB} < 77 MHz (256 RNG clock cycles otherwise)
- embeds start-up and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration)
- has an AMBA AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored)

3.22 HASH hardware accelerator (HASH)

The HASH is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-224, SHA-256) and the keyed-hash message authentication code (HMAC) algorithm. HMAC is suitable for applications requiring message authentication.

The HASH computes FIPS (federal information processing standards) approved digests of length of 160, 224, 256, 512 bits, for messages of up to (2^{64} – 1).

The HASH main features are:

- Suitable for data authentication applications, compliant with:
  - Federal information processing standards publication FIPS PUB 180-4, *Secure hash standard* (SHA-1 and SHA-2 family)
  - Federal information processing standards publication FIPS PUB 186-4, *Digital* signature standard (DSS)

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  - Internet engineering task force (IETF) Request for comments RFC 2104, *HMAC: keyed-hashing for message authentication* and federal information processing standards publication FIPS PUB 198-1, *The Keyed-Hash message* authentication code (HMAC)
- Fast computation of SHA-1, SHA-224, and SHA-256
  - 82 (respectively 66) clock cycles for processing one 512-bit block of data using the SHA-1 (respectively SHA-256) algorithm
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
  - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit string
  - Word swapping supported: bits, bytes, half-words, and 32-bit words
- Automatic padding to complete the input bit string to fit the digest minimum block size of 512 bits (16 × 32 bits)
- Single 32-bit input register associated to an internal input FIFO of sixteen 32-bit words, corresponding to one block size
- AHB slave peripheral, accessible through 32-bit word accesses only (else an AHB error is generated)
- 8 × 32-bit words (H0 to H7) for output message digest
- Automatic data flow control with support of direct memory access (DMA) using one channel. Single or fixed burst of four supported.
- Interruptible message digest computation, on a per-32-bit word basis
  - Reloadable digest registers
  - Hashing computation suspend/resume mechanism, including using DMA

3.23 Timers and watchdogs

The devices include one advanced control timer, up to two general-purpose timers, two basic timers, two low-power timers, two watchdog timers and one SysTick timer.

The table below compares the features of the advanced control, general-purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16 bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	4
General-purpose	TIM2	32 bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No

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Table 4. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General-purpose	TIM3	16 bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
Basic	TIM6, TIM7	16 bits	Up	Any integer between 1 and 65536	Yes	0	No

3.23.1 Advanced-control timers (TIM1)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 - 100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in the next section) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the *Timer Link* feature for synchronization or event chaining.

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3.23.2 General-purpose timers (TIM2, TIM3)

There are two general-purpose timers that can be synchronized, embedded in the STM32H503xx devices (see *Table 4* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2

  They are full-featured general-purpose timers with 32-bit auto-reload up/downcounter and 32-bit prescaler.

  These timers feature four independent channels for input capture/output compare, PWM, or one-pulse mode output. They can work together, or with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.
- TIM3

  They are full-featured general-purpose timers with 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature four independent channels for input capture/output compare, PWM, or one-pulse mode output.

  They can work together, or with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.

  The counters can be frozen in debug mode. All have independent DMA request generation and support quadrature encoders.

3.23.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebase.

3.23.4 Low-power timers (LPTIM1, LPTIM2)

The devices embed six low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI, or an external clock. They are able to wake up the system from Stop mode.

The low-power timer supports the following features:

- 16-bit up counter with 16-bit auto reload register
- 3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock
  - Internal clock sources: LSE, LSI, HSI, or APB clock
  - External clock source over LPTIM input (working with no LP oscillator running, used by *Pulse Counter* application)
- 16-bit ARR auto reload register
- 16 bit capture/compare register
- Continuous/One-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity

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- Encoder mode
- Repetition counter
- Up to two independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on 10 events
- DMA request generation on the following events:
  - Update event
  - Input capture

3.23.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and, as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.23.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.23.7 SysTick timer

The Cortex-M33 embeds one SysTick timer.

This timer is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.24 Real-time clock (RTC), tamper and backup registers

3.24.1 Real-time clock (RTC)

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year, in BCD (binary-coded decimal) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month

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- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period
- Privilege protection support:
  - Alarm A, alarm B, wakeup timer, and timestamp individual privileged protection

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The RTC clock sources can be one of the following:

- 32.768 kHz external crystal (LSE)
- external resonator or oscillator (LSE)
- internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- high-speed external clock (HSE), divided by a prescaler in the RCC.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes.

All RTC events (alarm, wakeup timer, timestamp) can generate an interrupt and wakeup the device from the low-power modes.

3.24.2 Tamper and backup registers (TAMP)

The antitamper detection circuit is used to protect sensitive data from external attacks. 32 32-bit backup registers are retained in all low-power modes and also in VBAT mode. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with height tamper pins and nine internal tampers. The external tamper pins can be configured for edge detection, or level detection with or without filtering, or active tamper that increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- A tamper detection can erase the backup registers, backup SRAM, SRAM2, and I-cache.
- 32 32-bit backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the backup domain that remains powered-on by V_{BAT} when the V_{DD} power is switched off.
- Up to two tamper pins for two external tamper detection events:
  - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks

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  - Passive tampers: ultra-low power edge or level detection with internal pull-up hardware management
  - Configurable digital filter
- 11 internal tamper events to protect against transient or environmental perturbation attacks:
  - Backup domain voltage monitoring
  - Temperature monitoring
  - LSE monitoring
  - HSE monitoring
  - RTC calendar overflow
  - JTAG/SWD access if product state different from 0
  - Voltage monitoring through ADC analog watchdogs
  - Monotonic counter overflow
  - Fault generation for RNG
  - Independent watchdog reset when tamper flag is already set
  - System fault detection
- Each tamper can be configured in two modes:
  - Hardware mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Software mode: erase of secrets following a tamper detection launched by software
- Any tamper detection can generate an RTC time stamp event.
- Tamper configuration and backup registers privilege protection
- Monotonic counter

3.25 Inter-integrated circuit interface (I2C)

The device embeds two I2C. Refer to *Table 5: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration, and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bit rate up to 100 Kbit/s
  - Fast-mode (Fm), with a bit rate up to 400 Kbit/s
  - Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control

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  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming
- Wakeup from Stop capability
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 5. I2C implementation

I2C features(1)	I2C1	I2C2
Standard-mode (up to 100 Kbit/s)	X	X
Fast-mode (up to 400 Kbit/s)	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	X
Independent clock	X	X
Wakeup capability	X	X

1. X: supported

3.26 Improved inter-integrated circuit (I3C)

The I3C interface handles communication between this device and others, like sensors and host processor(s) that are all connected on an I3C bus.

The I3C peripheral implements all the required features of the MIPI I3C specification v1.1. It can control all I3C bus-specific sequencing, protocol, arbitration and timing, and can be acting as controller (formerly known as master) or as target (formerly known as slave).

The I3C peripheral, acting as controller, improves the features of the I2C interface still preserving some backward compatibility: it allows an I2C target to operate on an I3C bus in legacy I2C fast-mode (Fm) or legacy I2C fast-mode plus (Fm+), provided that this latter does not perform clock stretching.

The I3C peripheral can be used with DMA in order to off-load the CPU.

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Table 6. I3C peripheral controller/target features versus MIPI v1.1

Feature	MIPI I3C v1.1	I3C peripheral when controller	I3C peripheral when target	Comments
I3C SDR message	X	X	X	-
Legacy I^2C message (Fm/Fm+)	X	X	-	Mandatory when controller and the I3C bus is mixed with (external) legacy I^2C target(s). Optional in MIPI v1.1 when target.
HDR DDR message	X	-	-	Optional in MIPI v1.1
HDR-TSL/TSP, HDR-BT	X	-	-	Optional in MIPI v1.1
Dynamic address assignment	X	X	X	-
Static address	X	X	-	No (intended) support of I3C peripheral as a target on an I^2C bus.
Grouped addressing	X	X	-	Optional in MIPI v1.1
CCCs	X	X	X	Mandatory CCCs and some optional CCCs are supported
Error detection and recovery	X	X	X	-
In-band interrupt (with MDB)	X	X	X	-
Secondary controller	X	X	X	-
Hot-join mechanism	X	X	X	-
Target reset	X	X	X	-
Synchronous timing control	X	X	-	Optional in MIPI v1.1
Asynchronous timing control 0	X	X	-	Optional in MIPI v1.1
Asynchronous timing control 1,2, 3	X	-	-	Optional in MIPI v1.1
Device-to-device tunneling	X	X	-	Optional in MIPI v1.1
Multilane data transfer	X	X	-	Optional in MIPI v1.1
Monitoring device early termination	X	-	-	Optional in MIPI v1.1

3.27 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART)

The devices have six embedded universal synchronous receiver transmitters (USART1/USART2/USART3), and one low-power universal asynchronous receiver transmitter (LPUART1).

Table 7. USART, UART, and LPUART features

USART modes/features(1)	USART1/2/3	LPUART1
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X

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Table 7. USART, UART, and LPUART features (continued)

USART modes/features[1]	USART1/2/3	LPUART1
Multiprocessor communication	X	X
Synchronous mode (master/slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual-clock domain and wakeup from Stop mode	X[2]	X[2]
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto-baud rate detection	X	-
Driver enable	X	X
USART data length	7, 8 and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	8 bytes	

1. X = supported.
2. Wakeup supported from Stop mode.

3.27.1 Universal synchronous/asynchronous receiver transmitter (USART/UART)

The USART offers a flexible means to perform full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The USART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications up to 20 Mbauds are possible by using the DMA (direct memory access) for multibuffer configuration.

The USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data
  Each FIFO can be enabled/disabled by software and come with a status flag.
- A common programmable transmit and receive baud rate
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Auto baud rate detection

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- Programmable data word length (7, 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous Master/Slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wakeup from Mute mode by idle line detection or address mark detection
- Wakeup from Stop mode
- LIN master-synchronous break send capability and LIN slave break detection capability
  - 13-bit break generation and 10/11 bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16 bit duration for Normal mode
- Smartcard mode
  - Supports the T=0 and T=1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
  - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

3.27.2 Low-power universal asynchronous receiver transmitter (LPUART)

The LPUART supports bidirectional asynchronous serial communication with minimum power consumption. It also supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher-speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

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The LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 baud/s to 9600 baud/s using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data
  Each FIFO can be enabled/disabled by software and come with status flags for FIFOs states.
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: wakeup from Mute mode by idle line detection or address mark detection
- Wakeup from Stop capability

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3.28 Serial peripheral interface (SPI)/inter-integrated sound interfaces (I2S)

The devices embed three serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex, and simplex synchronous, serial communication with external devices.

The interface can be configured as master or slave and can operate in multislave or multimaster configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to set up communication with a concrete slave and to assure it handles the data flow properly. The Motorola data format is used by default, but some other specific modes are supported as well.

The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4-bit to 32-bit data size selection or fixed to 8-bit and 16-bit only
- Multimaster or multislave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of PCLK
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO x MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI formats support
- Hardware CRC feature can secure communication at the end of a transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun at slave, mode fault at master
- Two 16x or 8x 8-bit embedded Rx and TxFIFOs with DMA capability
- Programmable number of data in transaction
- Configurable FIFO thresholds (data packing)
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Wakeup from Stop capability
- Optional status pin RDY signalizing the slave device ready to handle the data flow.

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Three standard I2S interfaces (multiplexed with SPI1, SPI2, and SPI3) are available. They can be operated in master or slave mode, in full-duplex communication modes, and can be configured to operate with configurable resolutions as an input or output channel.

I2S main features:

- Full duplex communication
- Simplex communication (only transmitter or receiver)
- Master or slave operations
- 8-bit programmable linear prescaler
- Data length may be 16, 24 or 32 bits
- Channel length can be 16 or 32 in master, any value in slave
- Programmable clock polarity
- Error flags signaling for improved reliability: underrun, overrun, and frame error
- Embedded Rx and TxFIFOs
- Supported I2S protocols:
  - I2S Philips standard
  - MSB-Justified standard (left-justified)
  - LSB-Justified standard (right-justified)
  - PCM standard (with short and long frame synchronization)
- Data ordering programmable (LSb or MSb first)
- DMA capability for transmission and reception
- Master clock can be output to drive an external audio component. The ratio is fixed at 256 x FWS (where FWS is the audio sampling frequency)

Table 8. SPI features

SPI feature	SPI1, SPI2, SPI3 (full feature set instances)
Data size	Configurable from 4 to 32-bit
CRC computation	CRC polynomial length configurable from 5 to 33-bit
Size of FIFOs	16x 8-bit
Number of transferred data	Unlimited, expandable
I2S feature	Yes

3.29 Controller area network (FDCAN)

The controller area network (CAN) subsystem consists of one CAN module, a shared message RAM memory, and a configuration block.

The modules (FDCAN) are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 0.8-Kbyte message RAM implements filters, receives FIFOs, transmits event FIFOs, and transmits FIFOs.

The FDCAN main features are:

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- Conform with CAN protocol version 2.0 part A, B, and ISO 11898-1: 2015, -4
- CAN FD with maximum 64 data bytes supported
- CAN error logging
- AUTOSAR and J1939 support
- Improved acceptance filtering
- 2 receive FIFOs of three payloads each (up to 64 bytes per payload)
- Separate signaling on reception of high priority messages
- Configurable transmit FIFO/queue of three payloads (up to 64 bytes per payload)
- Configurable transmit event FIFO
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains: APB bus interface and CAN core kernel clock
- Power-down support

3.30 Universal serial bus full-speed host/device interface (USB)

USB main features

- USB specification version 2.0 full-speed compliant
- Host and device functions
- 2048bytes of dedicated SRAM data buffer memory with 32-bit access
- Configurable number of endpoints from 1 to 8
- Cyclic redundancy check (CRC) generation/checking, non-return-to-zero inverted (NRZI) encoding/decoding, and bit-stuffing
- Isochronous transfers support
- Double-buffered bulk/isochronous endpoint support
- USB suspend/resume operations
- Frame-locked clock pulse generation
- USB 2.0 Link power management support
- Battery charging specification revision 1.2 support in device
- USB connect / disconnect capability (controllable embedded pull-up resistor on USB_DP line)

3.31 Development support

3.31.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be reused as GPIO with an alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

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3.31.2 Embedded Trace Macrocell

The Arm Embedded Trace Macrocell (ETM) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

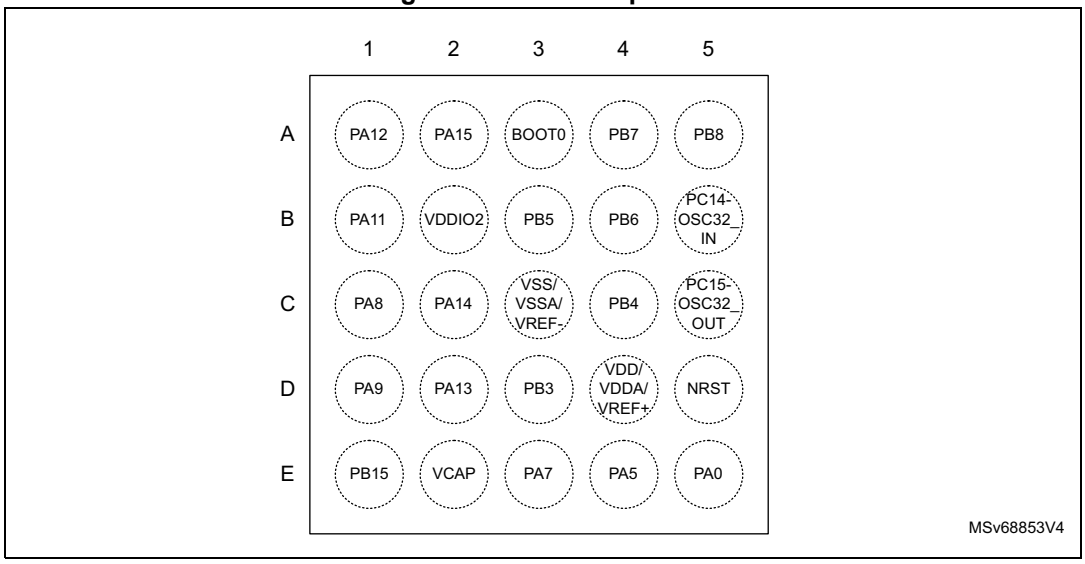
The ETM operates with third-party debugger software tools.

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4 Pinout, pin description, and alternate function

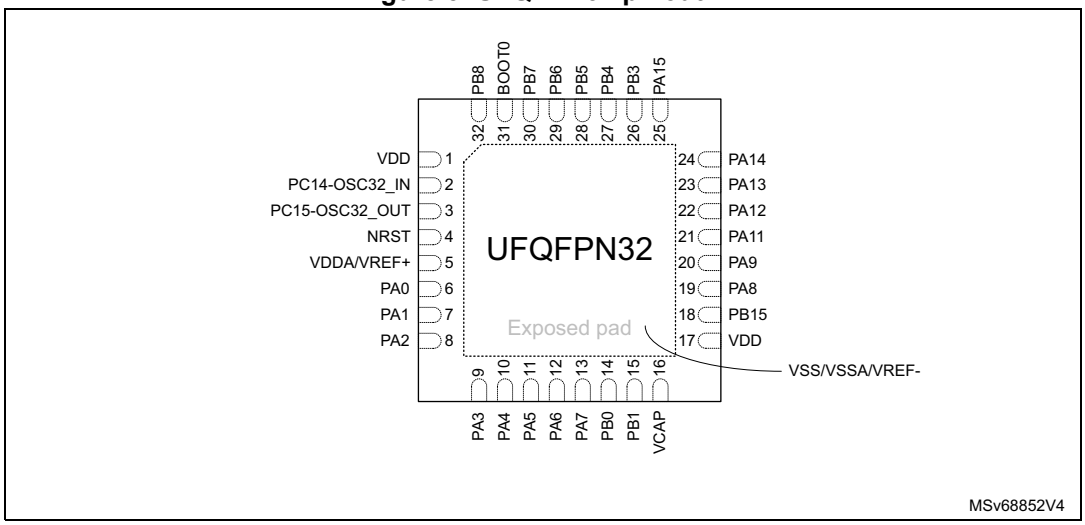
4.1 Pinout/ballout schematics

Figure 4. WLCSP25 pinout



1. The above figure shows the package top view.

Figure 5. UFQFPN32 pinout[a]

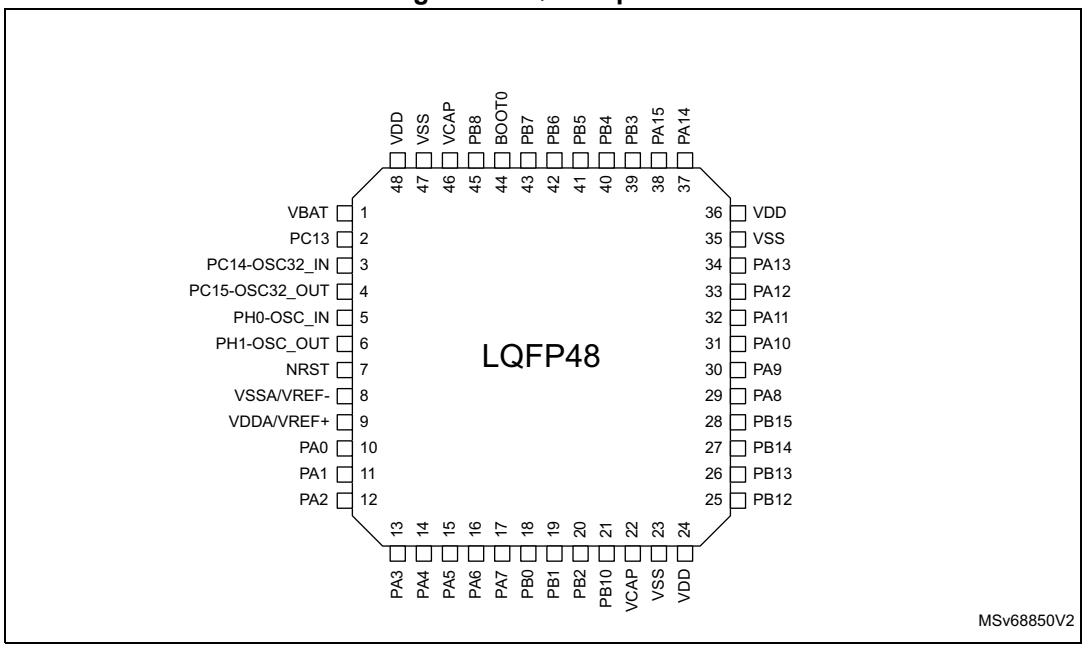


1. The above figure shows the package top view.

a. There is an exposed die pad on the underside of the UFQFPN package. This backside pad must be connected and soldered to PCB ground.

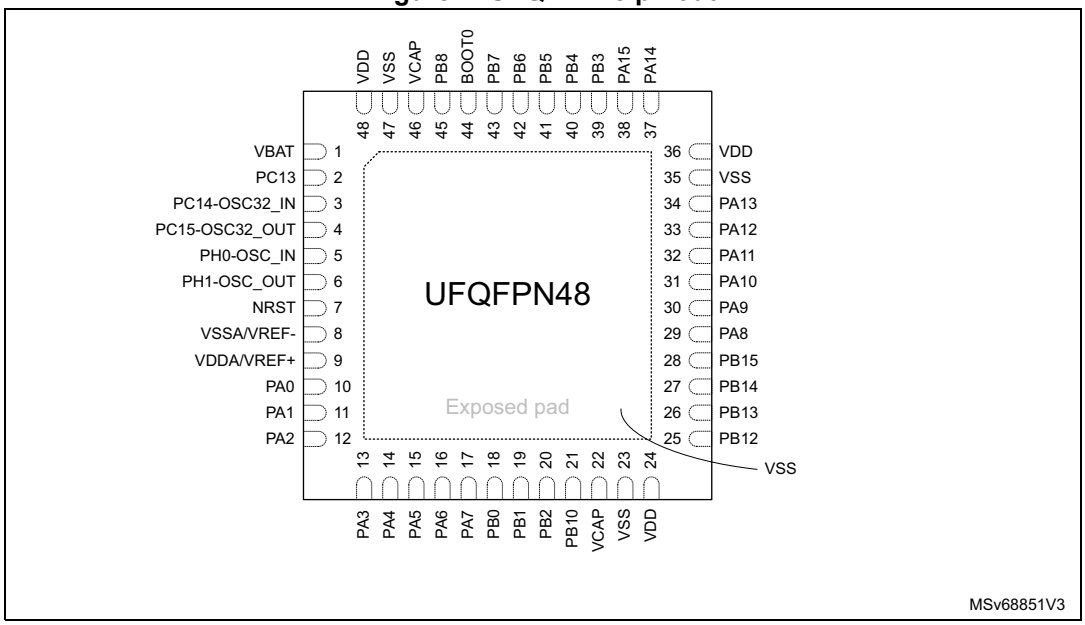
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Figure 6. LQFP48 pinout



1. The above figure shows the package top view.

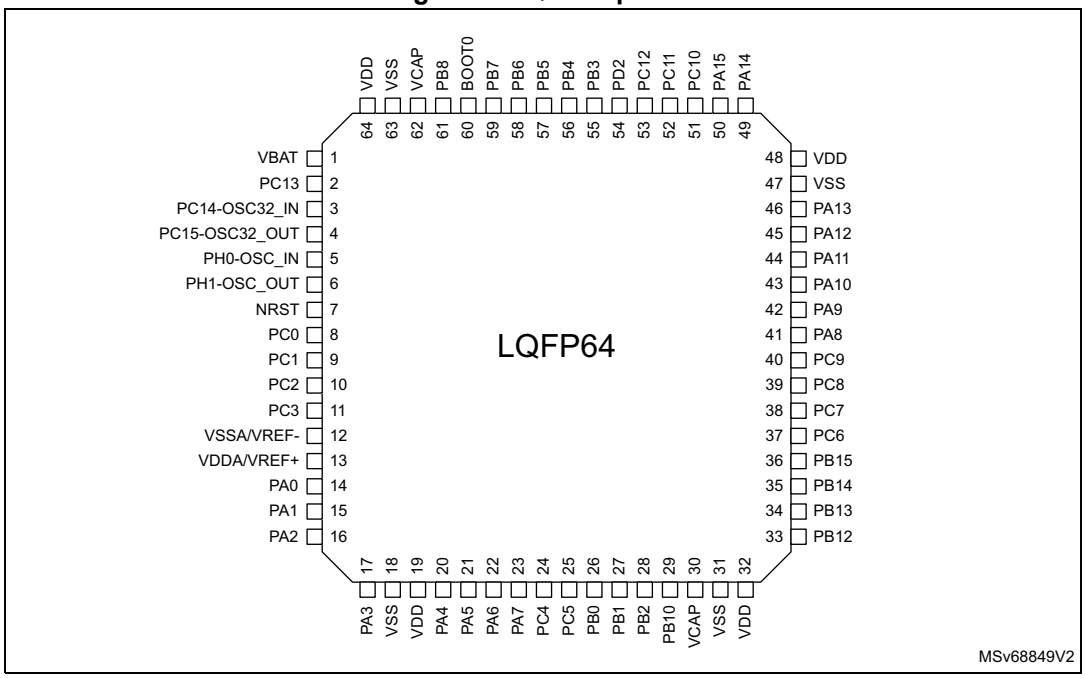
Figure 7. UFQFPN48 pinout



1. The above figure shows the package top view.

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Figure 8. LQFP64 pinout



1. The above figure shows the package top view.

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4.2 Pin description

Table 9. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input/output pin
I/O structure		FT	5V-tolerant I/O
		TT	3.6V-tolerant I/O
		B	Dedicated BOOT pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os(1)	
		_a	I/O, with analog switch function supplied by V_{DDA}
		_f	I/O, Fm+ capable
		_h	I/O with high-speed low-voltage mode (HSLV)
		_s	I/O supplied only by V_{DDIO2}(2)
		_t	I/O with tamper function functional in VBAT mode
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in the table below are a concatenation of various options. Examples: FT_hat, FT_fs, TT_a.
2. Refer to *Table 2: STM32H503xx features and peripheral counts* for the list of packages featuring VDDIO2 separate supply pin.

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Table 10. STM32H503xx pin/ball definition

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP 25	UFQFPN 32	LQFP 48	UFQFPN48	LQFP 64						
-	-	1	1	1	VBAT	S	-	-	-	-
-	-	2	2	2	PC13	I/O	FT_t	(1)(2)	EVENTOUT	TAMP_IN1/TAMP_OUT2, RTC_OUT1/RTC_TS, WKUP4
B5	2	3	3	3	PC14-OSC32_IN(OSC32_IN)	I/O	FT	(1)(2)	EVENTOUT	OSC32_IN
C5	3	4	4	4	PC15-OSC32_OUT(OSC32_OUT)	I/O	FT	(1)(2)	EVENTOUT	OSC32_OUT
-	-	5	5	5	PH0-OSC_IN(PH0)	I/O	FT	-	EVENTOUT	OSC_IN
-	-	6	6	6	PH1-OSC_OUT(PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
D5	4	7	7	7	NRST	I/O	RST	-	-	-
-	-	-	-	8	PC0	I/O	FT_ah	-	TIM1_ETR, LPTIM1_CH2, SPI1_SCK/I2S1_CK, SPI2_RDY, EVENTOUT	ADC1_INP10
-	-	-	-	9	PC1	I/O	FT_ah	-	TRACED0, TIM3_ETR, SPI1_NSS/I2S1_WS, SPI2_MOSI/I2S2_SDO, USART1_CTS/USART1_NSS, LPUART1_CTS, LPTIM2_IN1, EVENTOUT	ADC1_INP11, ADC1_INN10, WKUP3
-	-	-	-	10	PC2	I/O	FT_ah	-	PWR_CSLEEP, SPI1_MISO/I2S1_SDI, SPI2_MISO/I2S2_SDI, USART1_RTS, LPUART1_RTS, EVENTOUT	ADC1_INP12, ADC1_INN11

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
-	-	-	-	11	PC3	I/O	FT_ah	-	PWR_CSTOP, LPUART1_TX, SPI1_MOSI/I2S1_SDO, SPI2_MOSI/I2S2_SDO, USART2_CTS/USART2_NSS, LPTIM2_IN2, EVENTOUT	ADC1_INP13, ADC1_INN12
C3	-	8	8	12	VSSA	S	-	-	-	-
D4	5	9	9	13	VDDA	S	-	-	-	-
E5	6	10	10	14	PA0	I/O	FT_ah	-	RTC_OUT2, TIM2_CH1, TIM3_CH1, LPTIM2_ETR, LPTIM1_ETR, LPTIM1_IN2, SPI3_RDY, USART2_CTS/USART2_NSS, USART1_CTS/USART1_NSS, USART3_CTS/USART3_NSS, SPI3_NSS/I2S3_WS, I2S2_MCK, SPI1_MISO/I2S1_SDI, USART3_CK, TIM2_ETR, EVENTOUT	ADC1_INP0, ADC1_INN1, OPAMP1_VINP, COMP1_INP1, TAMP_IN2/TAMP_OUT1, WKUP1
-	7	11	11	15	PA1	I/O	FT_ah	-	TIM2_CH2, SPI1_NSS/I2S1_WS, LPTIM1_IN1, SPI3_SCK/I2S3_CK, USART2_RTS, USART1_RX, USART2_CK, SPI2_RDY, TIM1_CH3, EVENTOUT	ADC1_INP1

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
-	8	12	12	16	PA2	I/O	FT_ah	-	TIM2_CH3, TIM3_ETR, LPUART1_RX, SPI1_SCK/I2S1_CK, LPTIM1_IN2, SPI3_MISO/I2S3_SDI, USART2_TX, USART1_TX, TIM1_CH4, EVENTOUT	ADC1_INP14, WKUP2
-	9	13	13	17	PA3	I/O	FT_ah	-	TIM2_CH4, LPUART1_TX, SPI1_MISO/I2S1_SDI, SPI2_NSS/I2S2_WS, SPI3_MOSI/I2S3_SDO, USART2_RX, USART1_CK, USART3_RX, TIM1_CH1N, EVENTOUT	ADC1_INP15
-	-	-	-	18	VSS	S	-	-	-	-
-	-	-	-	19	VDD	S	-	-	-	-
-	10	14	14	20	PA4	I/O	TT_ah	-	TIM1_CH2N, LPTIM2_CH1, SPI1_MOSI/I2S1_SDO, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, USART1_RTS, SPI3_MISO/I2S3_SDI, USART3_TX, TIM1_BKIN, EVENTOUT	ADC1_INP18, DAC1_OUT1

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
E4	11	15	15	21	PA5	I/O	TT_ah	-	TIM2_CH1, LPTIM1_ETR, LPTIM2_CH2, LPTIM1_CH1, SPI1_SCK/I2S1_CK, I2S1_MCK, SPI2_SCK/I2S2_CK, LPUART1_RTS, USART2_TX, SPI3_MOSI/I2S3_SDO, USART2_CTS/USART2_NSS, USART3_RX, TIM2_ETR, EVENTOUT	ADC1_INP19, ADC1_INN18, DAC1_OUT2, COMP1_INM3
-	12	16	16	22	PA6	I/O	FT_ah	-	TIM1_BKIN, TIM3_CH1, SPI1_MISO/I2S1_SDI, EVENTOUT	ADC1_INP3
E3	13	17	17	23	PA7	I/O	TT_ah	-	TIM1_CH1N, TIM3_CH2, LPTIM2_ETR, I2S1_MCK, SPI1_MOSI/I2S1_SDO, I2S2_MCK, AUDIOCLK, USART1_RTS, USART3_RTS, I2S3_MCK, SPI2_MISO/I2S2_SDI, USART3_CK, TIM2_CH3, EVENTOUT	ADC1_INP7, ADC1_INN3, OPAMP1_VOUT
-	-	-	-	24	PC4	I/O	FT_ah	-	TIM2_CH4, LPTIM2_ETR, SPI1_RDY, I2S1_MCK, USART3_RX, EVENTOUT	ADC1_INP4, COMP1_INM1
-	-	-	-	25	PC5	I/O	TT_ah	-	TIM1_CH4N, SPI1_SCK/I2S1_CK, COMP1_OUT, LPTIM2_CH1, EVENTOUT	ADC1_INP8, ADC1_INN4, OPAMP1_VINM

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
-	14	18	18	26	PB0	I/O	FT_ah	-	TIM1_CH2N, TIM3_CH3, LPTIM1_IN1, USART2_TX, TIM1_ETR, EVENTOUT	ADC1_INP9, ADC1_INN5, OPAMP1_VINP, COMP1_INP2
-	15	19	19	27	PB1	I/O	FT_ah	-	TIM1_CH3N, TIM3_CH4, LPTIM2_ETR, LPTIM1_IN2, SPI2_MOSI/I2S2_SDO, USART2_RX, COMP1_OUT, TIM1_CH1, EVENTOUT	ADC1_INP5, OPAMP1_VINM, COMP1_INM2
-	-	20	20	28	PB2	I/O	FT_ah	-	RTC_OUT2, TIM1_CH2N, LPTIM1_CH2, SPI1_RDY, LPTIM1_CH1, SPI2_SCK/I2S2_CK, SPI3_MOSI/I2S3_SDO, USART2_CK, TIM2_CH1, EVENTOUT	COMP1_INP3, LSCO
-	-	21	21	29	PB10	I/O	FT_fh	-	TIM2_CH3, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, SPI3_NSS/I2S3_WS, USART3_TX, I3C1_SDA, FDCAN1_TX, I3C2_SCL, I2C1_SDA, USART3_CK, LPTIM2_CH2, EVENTOUT	-
E2	16	22	22	30	VCAP	S	-	-	-	-
-	-	23	23	31	VSS	S	-	-	-	-
-	17	24	24	32	VDD	S	-	-	-	-
-	-	25	25	33	PB12	I/O	FT_h	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, USART1_CK, FDCAN1_RX, EVENTOUT	-

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
-	-	26	26	34	PB13	I/O	FT_fh	-	TIM1_CH1N, LPTIM2_CH1, I2C2_SDA, SPI2_SCK/I2S2_CK, USART3_CTS/USART3_NSS, LPUART1_CTS, FDCAN1_TX, I3C2_SDA, I2C1_SMBA, EVENTOUT	-
-	-	27	27	35	PB14	I/O	FT_h	-	TIM1_CH2N, LPTIM1_ETR, USART1_TX, SPI2_MISO/I2S2_SDI, USART3_RTS, LPUART1_RTS, EVENTOUT	-
E1	18	28	28	36	PB15	I/O	FT_ah	-	RTC_REFIN, TIM1_CH3N, LPTIM1_CH1, LPTIM2_IN2, USART1_RX, SPI2_MOSI/I2S2_SDO, SPI3_MISO/I2S3_SDI, USART3_CTS/USART3_NSS, LPUART1_RX, FDCAN1_TX, I2S3_MCK, USART2_RTS, COMP1_OUT, USART2_RX, TIM3_CH4, EVENTOUT	PVD_IN
-	-	-	-	37	PC6	I/O	FT_fh	-	TIM1_CH1, TIM3_CH1, I3C2_SCL, I2C1_SMBA, I2S2_MCK, I2C2_SCL, FDCAN1_RX, USART2_TX, EVENTOUT	-

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
-	-	-	-	38	PC7	I/O	FT_fh	-	TRGIO, TIM1_CH2, TIM3_CH2, I3C2_SDA, SPI1_MOSI/I2S1_SDO, I2S3_MCK, I2C2_SDA, FDCAN1_TX, USART2_RX, EVENTOUT	-
-	-	-	-	39	PC8	I/O	FT_fh	-	TRACED1, TIM1_CH3, TIM3_CH3, I3C1_SCL, I2C1_SCL, SPI1_NSS/I2S1_WS, I2C2_SMBA, FDCAN1_RX, USART2_CK, EVENTOUT	-
-	-	-	-	40	PC9	I/O	FT_fh	-	MCO2, TIM1_CH4, TIM3_CH4, I3C1_SDA, I2C1_SDA, AUDIOCLK, SPI3_RDY, USART3_RTS, FDCAN1_TX, USART2_CTS/USART2_NSS, EVENTOUT	-
C1	19	29	29	41	PA8	I/O	FT_hs	-	MCO1, TIM1_CH1, TIM3_CH3, LPTIM2_IN1, USART2_TX, SPI1_RDY, SPI2_MOSI/I2S2_SDO, USART1_CK, LPUART1_CTS, FDCAN1_RX, USB_SOF, SPI2_NSS/I2S2_WS, SPI1_SCK/I2S1_CK, USART3_TX, TIM1_CH4N, EVENTOUT	-

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
D1	20	30	30	42	PA9	I/O	FT_hs	-	TRACED2, TIM1_CH2, LPUART1_TX, SPI1_MISO/I2S1_SDI, SPI2_SCK/I2S2_CK, USART1_TX, SPI3_MOSI/I2S3_SDO, USART3_CK, EVENTOUT	-
-	-	31	31	43	PA10	I/O	FT_h	-	TIM1_CH3, LPUART1_RX, LPTIM2_IN2, USART1_RX, EVENTOUT	-
B1	21	32	32	44	PA11	I/O	FT_h	-	TRGIO, TIM1_CH4, TIM3_CH2, LPUART1_CTS, USART2_RX, SPI2_NSS/I2S2_WS, SPI3_RDY, USART1_CTS/USART1_NSS, USART1_RX, FDCAN1_RX, USB_DM, USART3_RTS, LPTIM2_CH2, EVENTOUT	-
A1	22	33	33	45	PA12	I/O	FT_h	-	TRACED3, TIM1_ETR, TIM3_CH4, LPUART1_RTS, USART2_TX, SPI2_SCK/I2S2_CK, SPI2_RDY, USART1_RTS, USART1_TX, FDCAN1_TX, USB_DP, USART3_RX, TIM2_CH4, EVENTOUT	-

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
D2	23	34	34	46	PA13(JTMS/SWDIO)	I/O	FT_h	(3)	JTMS/SWDIO, TIM1_CH1, LPTIM1_CH1, USART1_RX, LPUART1_CTS, USART2_RX, COMP1_OUT, TIM1_ETR, EVENTOUT	-
-	-	35	35	47	VSS	S	-	-	-	-
-	-	36	36	48	VDD	S	-	-	-	-
C2	24	37	37	49	PA14(JTCK/SWCLK)	I/O	FT_h	(3)	JTCK/SWCLK, TIM1_CH2, TIM3_CH1, LPTIM2_CH1, LPTIM1_ETR, USART1_TX, LPUART1_RTS, USART2_TX, TIM1_CH4N, EVENTOUT	-
A2	25	38	38	50	PA15(JTDI)	I/O	FT_hs	(3)	JTDI, TIM2_CH1, LPTIM1_IN2, LPTIM2_CH1, USART2_CK, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI2_MISO/I2S2_SDI, USART1_CTS/USART1_NSS, USART2_RX, SPI3_SCK/I2S3_CK, USART2_RTS, USART3_RX, TIM2_ETR, EVENTOUT	-

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
-	-	-	-	51	PC10	I/O	FT_fh	-	TIM1_BKIN2, I3C2_SCL, SPI1_MISO/I2S1_SDI, SPI3_SCK/I2S3_CK, USART3_TX, I2C2_SCL, FDCAN1_RX, USART2_RTS, EVENTOUT	-
-	-	-	-	52	PC11	I/O	FT_fh	-	TIM2_CH2, I3C2_SDA, I2C1_SMBA, SPI1_RDY, SPI3_MISO/I2S3_SDI, USART3_RX, I2C2_SDA, TIM1_BKIN2, EVENTOUT	-
-	-	-	-	53	PC12	I/O	FT_h	-	TRACED3, TIM2_CH4, LPTIM1_CH1, LPTIM2_CH2, SPI3_MOSI/I2S3_SDO, USART3_CK, I2C2_SMBA, TIM1_CH4, EVENTOUT	-
-	-	-	-	54	PD2	I/O	FT_h	-	TRACED2, TIM2_CH3, TIM3_ETR, SPI3_NSS/I2S3_WS, USART3_CTS/USART3_NSS, USART2_RTS, TIM2_ETR, EVENTOUT	-
D3	26	39	39	55	PB3(JTDO/TRACESWO)	I/O	FT_fhs	(3)	JTDO/TRACESWO, TIM2_CH2, LPTIM1_CH1, I3C2_SCL, I2C2_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, I2S2_MCK, I2C2_SCL, FDCAN1_RX, CRS_SYNC, I2C1_SMBA, USART3_TX, TIM1_BKIN, EVENTOUT	-

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
C4	27	40	40	56	PB4(NJTRST)	I/O	FT_fhs	(3)	NJTRST, TIM1_CH4N, TIM3_CH1, I3C2_SDA, LPTIM1_CH2, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, I2C2_SDA, FDCAN1_TX, I2C1_SMBA, USART2_TX, TIM1_CH2, EVENTOUT	-
B3	28	41	41	57	PB5	I/O	FT_fhs	-	TRACECLK, TIM1_CH3, TIM3_CH2, I3C2_SCL, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, SPI2_MISO/I2S2_SDI, SPI3_MOSI/I2S3_SDO, I2C2_SCL, FDCAN1_RX, I3C1_SDA, I2C1_SDA, USART2_RX, LPTIM1_IN1, EVENTOUT	-
B4	29	42	42	58	PB6	I/O	FT_fhs	-	TRACED0, TIM1_CH3N, TIM3_CH3, I3C1_SCL, I2C1_SCL, I2S1_MCK, SPI3_RDY, USART1_TX, LPUART1_TX, FDCAN1_TX, USART2_CTS/USART2_NSS, USART2_CK, TIM1_CH2, EVENTOUT	-

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Table 10. STM32H503xx pin/ball definition (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP25	UFQFPN32	LQFP48	UFQFPN48	LQFP64						
A4	30	43	43	59	PB7	I/O	FT_fhs	-	TRACED1, TIM1_CH2N, TIM3_ETR, I3C1_SDA, I2C1_SDA, AUDIOCLK, SPI3_SCK/I2S3_CK, USART1_RX, LPUART1_RX, FDCAN1_TX, I2S3_MCK, I2C2_SMBA, USART3_TX, TIM1_CH1, EVENTOUT	WKUP5
A3	31	44	44	60	BOOT0	I	B	-	-	-
A5	32	45	45	61	PB8	I/O	FT_fhs	-	TRACED2, TIM1_BKIN2, LPTIM1_CH2, I3C1_SCL, I2C1_SCL, SPI2_RDY, I2S2_MCK, USART1_CK, I2C2_SDA, FDCAN1_RX, I3C2_SDA, I2C2_SMBA, SPI1_NSS/I2S1_WS, USART3_RX, LPTIM2_CH1, EVENTOUT	-
-	-	46	46	62	VCAP	S	-	-	-	-
-	-	47	47	63	VSS	S	-	-	-	-
-	1	48	48	64	VDD	S	-	-	-	-
B2	-	-	-	-	VDDIO2	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch (by VSW). Since the switch only sinks a limited amount of current, the use of PC13 to PC15 GPIOs in output mode is limited: - The speed must not exceed 2 MHz with a maximum load of 30 pF. These GPIOs must not be used as current sources (for example to drive a LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function depends then on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the product reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions. The internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated too.

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4.3 Alternate functions

Table 11. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2	LPTIM1/TIM3	I3C1/2/LPTIM2/ LPUART1	I2C1/2/LPTIM1/2/SPI 1/I2S1/USART1/2	LPTIM1/SPI1/I2S1/ SPI2/I2S2	SPI1/I2S1/SPI2/I2S 2/SPI3/I2S3	SPI2/I2S2/SPI3/I2S3 /USART1/2/3
Port A	PA0	RTC_OUT2	TIM2_CH1	TIM3_CH1	LPTIM2_ETR	LPTIM1_ETR	LPTIM1_IN2	SPI3_RDY	USART2_CTS/USA RT2_NSS
	PA1	-	TIM2_CH2	-	-	SPI1_NSS/I2S1_WS	LPTIM1_IN1	SPI3_SCK/I2S3_CK	USART2_RTS
	PA2	-	TIM2_CH3	TIM3_ETR	LPUART1_RX	SPI1_SCK/I2S1_CK	LPTIM1_IN2	SPI3_MISO/I2S3_S DI	USART2_TX
	PA3	-	TIM2_CH4	-	LPUART1_TX	SPI1_MISO/I2S1_SDI	SPI2_NSS/I2S2_W S	SPI3_MOSI/I2S3_S DO	USART2_RX
	PA4	-	TIM1_CH2 N	-	LPTIM2_CH1	SPI1_MOSI/I2S1_SD O	SPI1_NSS/I2S1_W S	SPI3_NSS/I2S3_W S	USART2_CK
	PA5	-	TIM2_CH1	LPTIM1_ETR	LPTIM2_CH2	LPTIM1_CH1	SPI1_SCK/I2S1_CK	I2S1_MCK	SPI2_SCK/I2S2_CK
	PA6	-	TIM1_ BKIN	TIM3_CH1	-	-	SPI1_MISO/I2S1_S DI	-	-
	PA7	-	TIM1_ CH1N	TIM3_CH2	LPTIM2_ETR	I2S1_MCK	SPI1_MOSI/I2S1_S DO	I2S2_MCK	AUDIOCLK
	PA8	MCO1	TIM1_CH1	TIM3_CH3	LPTIM2_IN1	USART2_TX	SPI1_RDY	SPI2_MOSI/I2S2_S DO	USART1_CK
	PA9	TRACED2	TIM1_CH2	-	LPUART1_TX	SPI1_MISO/I2S1_SDI	SPI2_SCK/I2S2_CK	-	USART1_TX
	PA10	-	TIM1_CH3	-	LPUART1_RX	LPTIM2_IN2	-	-	USART1_RX
	PA11	TRGIO	TIM1_CH4	TIM3_CH2	LPUART1_CTS	USART2_RX	SPI2_NSS/I2S2_W S	SPI3_RDY	USART1_CTS/USA RT1_NSS
	PA12	TRACED3	TIM1_ETR	TIM3_CH4	LPUART1_RTS	USART2_TX	SPI2_SCK/I2S2_CK	SPI2_RDY	USART1_RTS
	PA13	JTMS/SWDIO	TIM1_CH1	LPTIM1_CH1	-	-	-	-	USART1_RX
	PA14	JTCK/SWCLK	TIM1_CH2	TIM3_CH1	LPTIM2_CH1	LPTIM1_ETR	-	-	USART1_TX
	PA15	JTDI	TIM2_CH1	LPTIM1_IN2	LPTIM2_CH1	USART2_CK	SPI1_NSS/I2S1_W S	SPI3_NSS/I2S3_W S	SPI2_MISO/I2S2_S DI

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Table 11. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2	LPTIM1/TIM3	I3C1/2/LPTIM2/LPUART1	I2C1/2/LPTIM1/2/SPI1/I2S1/USART1/2	LPTIM1/SPI1/I2S1/SPI2/I2S2	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3	SPI2/I2S2/SPI3/I2S3/USART1/2/3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	-	LPTIM1_IN1	-	-	-
	PB1	-	TIM1_CH3N	TIM3_CH4	LPTIM2_ETR	-	LPTIM1_IN2	SPI2_MOSI/I2S2_SDO	-
	PB2	RTC_OUT2	TIM1_CH2N	LPTIM1_CH2	-	SPI1_RDY	LPTIM1_CH1	SPI2_SCK/I2S2_CK	SPI3_MOSI/I2S3_SDO
	PB3	JTDO/TRACESWO	TIM2_CH2	LPTIM1_CH1	I3C2_SCL	I2C2_SDA	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	I2S2_MCK
	PB4	NJTRST	TIM1_CH4N	TIM3_CH1	I3C2_SDA	LPTIM1_CH2	SPI1_MISO/I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_NSS/I2S2_WS
	PB5	TRACECLK	TIM1_CH3	TIM3_CH2	I3C2_SCL	I2C1_SMBA	SPI1_MOSI/I2S1_SDO	SPI2_MISO/I2S2_SDI	SPI3_MOSI/I2S3_SDO
	PB6	TRACED0	TIM1_CH3N	TIM3_CH3	I3C1_SCL	I2C1_SCL	I2S1_MCK	SPI3_RDY	USART1_TX
	PB7	TRACED1	TIM1_CH2N	TIM3_ETR	I3C1_SDA	I2C1_SDA	AUDIOCLK	SPI3_SCK/I2S3_CK	USART1_RX
	PB8	TRACED2	TIM1_BKIN2	LPTIM1_CH2	I3C1_SCL	I2C1_SCL	SPI2_RDY	I2S2_MCK	USART1_CK
	PB10	-	TIM2_CH3	-	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	SPI3_NSS/I2S3_WS	USART3_TX
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	-	USART3_CK
	PB13	-	TIM1_CH1N	-	LPTIM2_CH1	I2C2_SDA	SPI2_SCK/I2S2_CK	-	USART3_CTS/USART3_NSS
	PB14	-	TIM1_CH2N	LPTIM1_ETR	-	USART1_TX	SPI2_MISO/I2S2_SDI	-	USART3_RTS
	PB15	RTC_REFIN	TIM1_CH3N	LPTIM1_CH1	LPTIM2_IN2	USART1_RX	SPI2_MOSI/I2S2_SDO	SPI3_MISO/I2S3_SDI	USART3_CTS/USART3_NSS

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Table 11. Alternate function AF0 to AF7(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2	LPTIM1/TIM3	I3C1/2/LPTIM2/LPUART1	I2C1/2/LPTIM1/2/SPI1/I2S1/USART1/2	LPTIM1/SPI1/I2S1/SPI2/I2S2	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3	SPI2/I2S2/SPI3/I2S3/USART1/2/3
Port C	PC0	-	TIM1_ETR	LPTIM1_CH2	-	-	SPI1_SCK/I2S1_CK	-	SPI2_RDY
	PC1	TRACED0	-	TIM3_ETR	-	SPI1_NSS/I2S1_WS	SPI2_MOSI/I2S2_SDO	-	USART1_CTS/USART1_NSS
	PC2	PWR_CSLEEP	-	-	-	SPI1_MISO/I2S1_SDI	SPI2_MISO/I2S2_SDI	-	USART1_RTS
	PC3	PWR_CSTOP	-	-	LPUART1_TX	SPI1_MOSI/I2S1_SDO	SPI2_MOSI/I2S2_SDO	-	USART2_CTS/USART2_NSS
	PC4	-	TIM2_CH4	-	LPTIM2_ETR	SPI1_RDY	I2S1_MCK	-	USART3_RX
	PC5	-	TIM1_CH4N	-	-	-	SPI1_SCK/I2S1_CK	-	-
	PC6	-	TIM1_CH1	TIM3_CH1	I3C2_SCL	I2C1_SMBA	I2S2_MCK	-	-
	PC7	TRGIO	TIM1_CH2	TIM3_CH2	I3C2_SDA	-	SPI1_MOSI/I2S1_SDO	I2S3_MCK	-
	PC8	TRACED1	TIM1_CH3	TIM3_CH3	I3C1_SCL	I2C1_SCL	SPI1_NSS/I2S1_WS	-	-
	PC9	MCO2	TIM1_CH4	TIM3_CH4	I3C1_SDA	I2C1_SDA	AUDIOCLK	SPI3_RDY	USART3_RTS
	PC10	-	TIM1_BKIN2	-	I3C2_SCL	-	SPI1_MISO/I2S1_SDI	SPI3_SCK/I2S3_CK	USART3_TX
	PC11	-	TIM2_CH2	-	I3C2_SDA	I2C1_SMBA	SPI1_RDY	SPI3_MISO/I2S3_SDI	USART3_RX
	PC12	TRACED3	TIM2_CH4	LPTIM1_CH1	LPTIM2_CH2	-	-	SPI3_MOSI/I2S3_SDO	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-
Port D	PD2	TRACED2	TIM2_CH3	TIM3_ETR	-	-	-	SPI3_NSS/I2S3_WS	USART3_CTS/USART3_NSS

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Table 11. Alternate function AF0 to AF7(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	TIM1/2	LPTIM1/TIM3	I3C1/2/LPTIM2/ LPUART1	I2C1/2/LPTIM1/2/SPI 1/I2S1/USART1/2	LPTIM1/SPI1/I2S1/ SPI2/I2S2	SPI1/I2S1/SPI2/I2S 2/SPI3/I2S3	SPI2/I2S2/SPI3/I2S3 /USART1/2/3
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-

1. Refer to the next table for AF8 to AF15.

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Table 12. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C2/I3C1/LPUART1/USART1	FDCAN1/USART2/3	CRS/I3C1/2/SPI3/I2S3/USB	I2C1/2/SPI2/I2S2/USART2	COMP/SPI1/I2S1	USART2/3	LPTIM1/2/TIM1/2/3	SYS
Port A	PA0	USART1_CTS/USART1_NSS	USART3_CTS/USART3_NSS	SPI3_NSS/I2S3_WS	I2S2_MCK	SPI1_MISO/I2S1_SDI	USART3_CK	TIM2_ETR	EVENTOUT
	PA1	USART1_RX	USART2_CK	-	SPI2_RDY	-	-	TIM1_CH3	EVENTOUT
	PA2	USART1_TX	-	-	-	-	-	TIM1_CH4	EVENTOUT
	PA3	USART1_CK	-	-	-	-	USART3_RX	TIM1_CH1N	EVENTOUT
	PA4	USART1_RTS	-	SPI3_MISO/I2S3_SDI	-	-	USART3_TX	TIM1_BKIN	EVENTOUT
	PA5	LPUART1_RTS	USART2_TX	SPI3_MOSI/I2S3_SDO	USART2_CTS/USART2_NSS	-	USART3_RX	TIM2_ETR	EVENTOUT
	PA6	-	-	-	-	-	-	-	EVENTOUT
	PA7	USART1_RTS	USART3_RTS	I2S3_MCK	SPI2_MISO/I2S2_SDI	-	USART3_CK	TIM2_CH3	EVENTOUT
	PA8	LPUART1_CTS	FDCAN1_RX	USB_SOF	SPI2_NSS/I2S2_WS	SPI1_SCK/I2S1_CK	USART3_TX	TIM1_CH4N	EVENTOUT
	PA9	-	-	SPI3_MOSI/I2S3_SDO	-	-	USART3_CK	-	EVENTOUT
	PA10	-	-	-	-	-	-	-	EVENTOUT
	PA11	USART1_RX	FDCAN1_RX	USB_DM	-	-	USART3_RTS	LPTIM2_CH2	EVENTOUT
	PA12	USART1_TX	FDCAN1_TX	USB_DP	-	-	USART3_RX	TIM2_CH4	EVENTOUT
	PA13	LPUART1_CTS	USART2_RX	-	-	COMP1_OUT	-	TIM1_ETR	EVENTOUT
	PA14	LPUART1_RTS	USART2_TX	-	-	-	-	TIM1_CH4N	EVENTOUT
	PA15	USART1_CTS/USART1_NSS	USART2_RX	SPI3_SCK/I2S3_CK	USART2_RTS	-	USART3_RX	TIM2_ETR	EVENTOUT

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Table 12. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C2/I3C1/LPUART1/USART1	FDCAN1/USART2/3	CRS/I3C1/2/SPI3/I2S3/USB	I2C1/2/SPI2/I2S2/USART2	COMP/SPI1/I2S1	USART2/3	LPTIM1/2/TIM1/2/3	SYS
Port B	PB0	-	USART2_TX	-	-	-	-	TIM1_ETR	EVENTOUT
	PB1	-	USART2_RX	-	-	COMP1_OUT	-	TIM1_CH1	EVENTOUT
	PB2	-	USART2_CK	-	-	-	-	TIM2_CH1	EVENTOUT
	PB3	I2C2_SCL	FDCAN1_RX	CRS_SYNC	I2C1_SMBA	-	USART3_TX	TIM1_BKIN	EVENTOUT
	PB4	I2C2_SDA	FDCAN1_TX	-	I2C1_SMBA	-	USART2_TX	TIM1_CH2	EVENTOUT
	PB5	I2C2_SCL	FDCAN1_RX	I3C1_SDA	I2C1_SDA	-	USART2_RX	LPTIM1_IN1	EVENTOUT
	PB6	LPUART1_TX	FDCAN1_TX	-	USART2_CTS/USART2_NSS	-	USART2_CK	TIM1_CH2	EVENTOUT
	PB7	LPUART1_RX	FDCAN1_TX	I2S3_MCK	I2C2_SMBA	-	USART3_TX	TIM1_CH1	EVENTOUT
	PB8	I2C2_SDA	FDCAN1_RX	I3C2_SDA	I2C2_SMBA	SPI1_NSS/I2S1_WS	USART3_RX	LPTIM2_CH1	EVENTOUT
	PB10	I3C1_SDA	FDCAN1_TX	I3C2_SCL	I2C1_SDA	-	USART3_CK	LPTIM2_CH2	EVENTOUT
	PB12	USART1_CK	FDCAN1_RX	-	-	-	-	-	EVENTOUT
	PB13	LPUART1_CTS	FDCAN1_TX	I3C2_SDA	I2C1_SMBA	-	-	-	EVENTOUT
	PB14	LPUART1_RTS	-	-	-	-	-	-	EVENTOUT
	PB15	LPUART1_RX	FDCAN1_TX	I2S3_MCK	USART2_RTS	COMP1_OUT	USART2_RX	TIM3_CH4	EVENTOUT

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Table 12. Alternate function AF8 to AF15(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C2/I3C1/LPUART1/USART1	FDCAN1/USART2/3	CRS/I3C1/2/SPI3/I2S3/USB	I2C1/2/SPI2/I2S2/USART2	COMP/SPI1/I2S1	USART2/3	LPTIM1/2/TIM1/2/3	SYS
Port C	PC0	-	-	-	-	-	-	-	EVENTOUT
	PC1	LPUART1_CTS	-	-	-	-	-	LPTIM2_IN1	EVENTOUT
	PC2	LPUART1_RTS	-	-	-	-	-	-	EVENTOUT
	PC3	-	-	-	-	-	-	LPTIM2_IN2	EVENTOUT
	PC4	-	-	-	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	COMP1_OUT	-	LPTIM2_CH1	EVENTOUT
	PC6	I2C2_SCL	FDCAN1_RX	-	-	-	USART2_TX	-	EVENTOUT
	PC7	I2C2_SDA	FDCAN1_TX	-	-	-	USART2_RX	-	EVENTOUT
	PC8	I2C2_SMBA	FDCAN1_RX	-	-	-	USART2_CK	-	EVENTOUT
	PC9	-	FDCAN1_TX	-	-	-	USART2_CTS/USART2_NSS	-	EVENTOUT
	PC10	I2C2_SCL	FDCAN1_RX	-	-	-	USART2_RTS	-	EVENTOUT
	PC11	I2C2_SDA	-	-	-	-	-	TIM1_BKIN2	EVENTOUT
	PC12	I2C2_SMBA	-	-	-	-	-	TIM1_CH4	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT
Port D	PD2	-	USART2_RTS	-	-	-	-	TIM2_ETR	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT

1. Refer to the previous table for AF0 to AF7.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with an ambient temperature at T_J = 25 °C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes, and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data is based on T_J = 25 °C, V_{DD} = V_{DDA} = 3.3 V (for the 1.71 ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

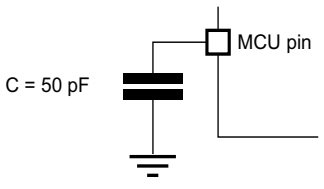
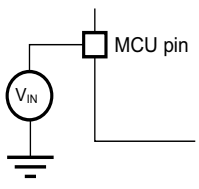


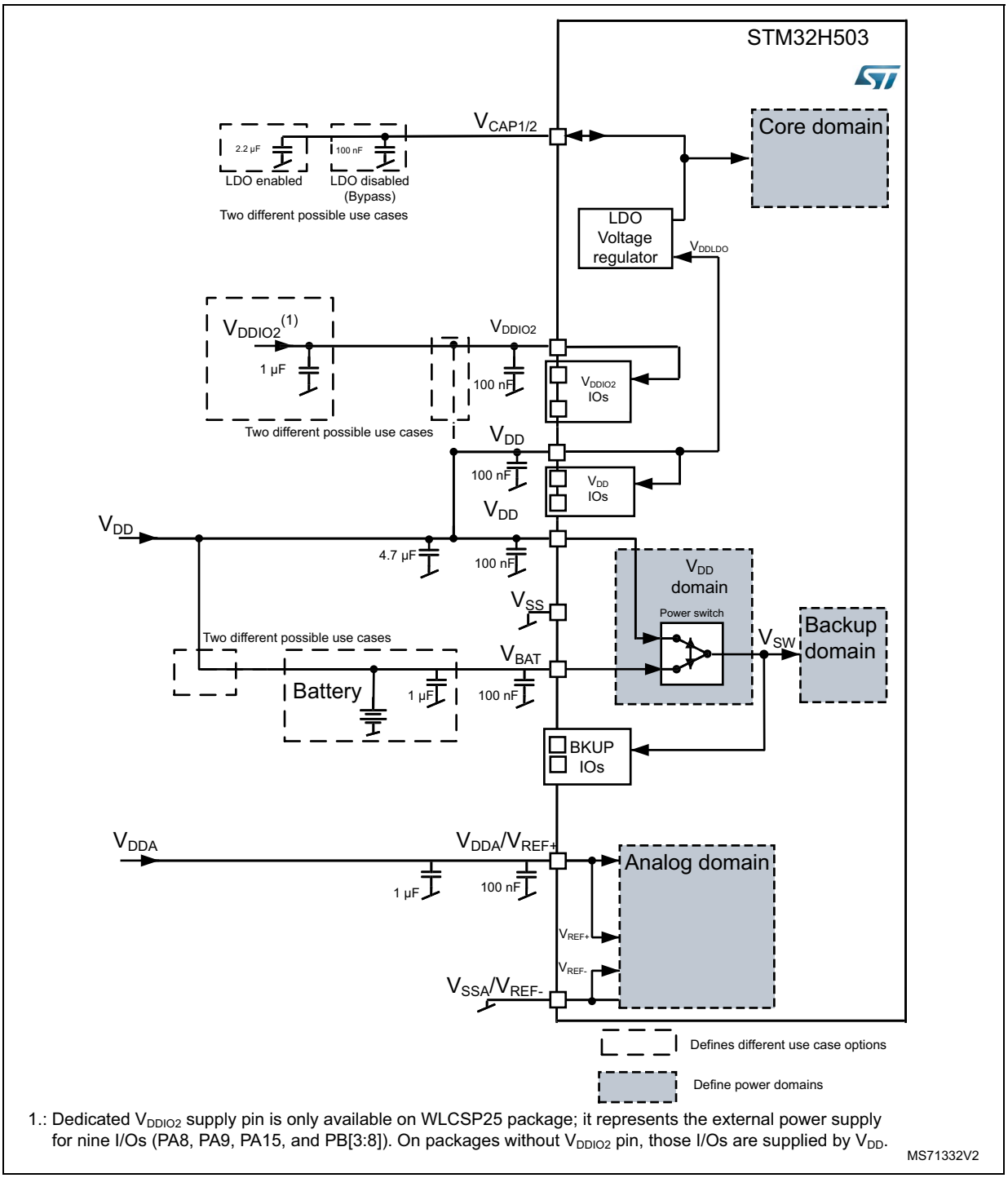
Figure 10. Pin input voltage



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5.1.6 Power supply scheme

Figure 11. Power supply scheme



Caution: If there are two VCAP pins (such as the LQFP64 package), each pin must be connected to a 2.2 µF (typical) capacitor (for a total around 4.4 µF). If only one VCAP pin is available, it must be connected to a 4.7 µF capacitor.

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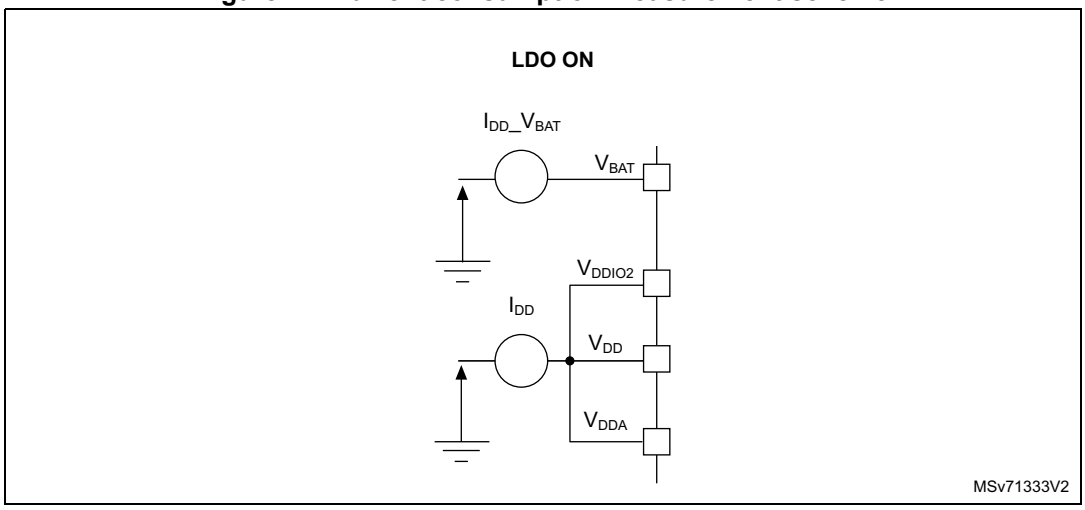
Note: Refer to "Getting started with STM32H5 MCU hardware development" (AN5711) for more details.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA}, and so on) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

5.1.7 Current consumption measurement

The I_{DD} parameters given in various tables in the next sections represent the total MCU consumption including the current supplying V_{DD}, V_{DDIO2}, V_{DDA}, and V_{BAT}.

Figure 12. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics*, and *Table 15: Thermal characteristics* can cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard. Extended mission profiles are available on demand.

Table 13. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	External main supply voltage (including V_{DD}(2)(3)(4), V_{DDA}, and V_{DDIO2}, and V_{BAT})	-0.3	4.0	V
V_{DDIOx}(3)- V_{SS}	I/O supply when HSLV= 0	-0.3	4.0	V
	I/O supply when HSLV = 1	-0.3	2.75	

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Table 13. Voltage characteristics(1) (continued)

Symbol	Ratings	Min	Max	Unit
V_{IN}(5)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (min(V_{DD}, V_{DDA}, V_{DDIO2}) + 4.0, 6.0 V)(6)(7)	V
	Input voltage on FT_t in VBAT mode	V_{SS}-0.3	min (min(V_{BAT}, V_{DDA}, V_{DDIO2}) + 4.0, 6.0 V)(6)(7)	
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on BOOT0 pin	V_{SS}-0.3	min (min(V_{DD}, V_{DDA}, V_{DDIO2}) + 4.0, 6.0 V)(3)(4)	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50.0	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50.0	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, and V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. If HSLV = 0.
3. V_{DDIO1} or V_{DDIO2}. V_{DDIO1} = V_{DD}.
4. HSLV = High-speed low-voltage mode. Refer to “General-purpose I/Os” (GPIO) section of RM0492.
5. V_{IN} maximum must always be respected. Refer to for the maximum allowed injected current values.
6. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
7. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.

Table 14. Current characteristics

Symbol	Ratings	Max	Unit
$\sum I_{VDD}$	Total current into sum of all V_{DD} power lines (source)(1)	200	mA
$\sum I_{VSS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	200	
I_{VDD}	Maximum current into each V_{DD} power pin (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk/sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, NRST pins	-5 / 0	
$\sum\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, and V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection (when V_{IN} > V_{DDIOx}) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by VIN < VSS. IINJ(PIN) must never be exceeded. Refer also to *Table 13: Voltage characteristics* for the minimum allowed input voltage values.

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5. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	130(1)	°C

1. The junction temperature is limited to 105 °C in the VOS0 voltage range.

5.3 Operating condition

5.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	HSLV(1) = 0	1.71(2)	-	3.6	V
		HSLV(1) = 1	1.71(2)	-	2.7	V
V_{DDIO2}(3)	PA8, PA9, PA15 and PB[3:8] I/Os supply voltage	At least one I/O in PA8, PA9, PA15 and PB[3:8] is used, HSLV(1) = 0	1.08	-	3.6	V
		At least one I/O in PA8, PA9, PA15 and PB[3:8] is used, HSLV(1) = 1	1.08	-	2.7	
		PA8, PA9, PA15, and PB[3:8] are not used, HSLV(1) = 0	0	-	3.6	
V_{DDA}	Analog supply voltage	COMP is used	1.62	-	3.6	V
		DAC is used	1.8	-		
		OPAMP is used	2.0	-		
		ADC is used	1.62	-		
		ADC, DAC, OPAMP, and COMP are not used	0	-		
V_{BAT}	Backup operating voltage	-	1.2	-	3.6	V

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Table 16. General operating conditions (continued)

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{IN}	I/O input voltage	All I/O except TT_xx	-0.3	-	min (min (V_{DD}, V_{DDA}, V_{DDIO2}) + 3.6V, 5.5 V)(4)(5)	V
		Input voltage on FT_t in VBAT mode	-0.3	-	min (min (V_{BAT}, V_{DDA}, V_{DDIO2}) + 3.6 V, 5.5 V)(4)(5)	
		TT_xx I/O	-0.3		V_{DDIOx} + 0.3	
V_{CORE}	Internal regulator ON	VOS0(6)	1.30	1.35	1.40	V
		VOS1	1.15	1.20	1.26	
		VOS2	1.05	1.10	1.15	
		VOS3	0.95	1.00	1.05	
	Regulator OFF: external VCORE voltage must be supplied from external regulator on VCAP pins.	VOS0(6)	1.32	1.35	1.40	V
		VOS1	1.17	1.20	1.26	
		VOS2	1.07	1.10	1.15	
		VOS3	0.97	1.00	1.05	
	Stop mode	SVOS3	-	1.0	-	V
		SVOS4	-	0.9	-	
		SVOS5	-	0.74	-	
f_{HCLK}	AHB clock frequency	VOS0(6)	-	-	250	MHz
		VOS1	-	-	200	
		VOS2	-	-	150	
		VOS3	-	-	100	
f_{PCLKx} (x=1,2,3)	APB1, APB2, APB3 clock frequency	VOS0(6)	-	-	250	MHz
		VOS1	-	-	200	
		VOS2	-	-	150	
		VOS3	-	-	100	

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Table 16. General operating conditions (continued)

Symbol	Parameter	Operating conditions		Min	Typ	Max	Unit
P_D(7)	Power dissipation at T_A = 85 °C for suffix 6(8)	WLCSP25		-	-	557.62	mW
		UFQFPN32		-	-	1122.19	
		UFQFPN48		-	-	1525.42	
		LQFP48		-	-	831.79	
		LQFP64		-	-	920.25	
	Power dissipation at T_A = 105 °C for suffix 7(8)	WLCSP25		-	-	309.79	mW
		UFQFPN32		-	-	623.44	
		UFQFPN48		-	-	847.46	
		LQFP48		-	-	462.11	
		LQFP64		-	-	511.25	
	Power dissipation at T_A = 125 °C for suffix 7(8)	WLCSP25		-	-	61.96	mW
		UFQFPN32		-	-	124.69	
		UFQFPN48		-	-	169.49	
		LQFP48		-	-	92.42	
		LQFP64		-	-	102.25	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		-40	-	85	°C
	Ambient temperature for the suffix 7 version	Maximum power dissipation			-	105	
		LDO bypass mode, or in low dissipation at 125 °C (9)			-	125	
T_J	Junction temperature range	Suffix 6 and 7 version	VOS0	-40	-	105	°C
			VOS1, VOS2, and VOS3	-40	-	130	

1. IO_VDD_HSLV option byte to be used for all I/Os, which are supplied by VDD pin except PA8, PA9, PA15, and PB[3:8] I/Os. IO_VDDIO2_HSLV option byte to be used for PA8, PA9, PA15, and PB[3:8] I/Os, which are supplied by the VDDIO2 pin. When the VDDIO2 power supply pin is not available, enabling HSLV on PA8, PA9, PA15, and PB[3:8] pins is still possible via the IO_VDDIO2_HSLV option byte.
2. When RESET is released, the functionality is guaranteed down to VPDR minimum.
3. Dedicated power supply pin VDDIO2 is only available on the WLCSP25 package.
4. This formula has to be applied on power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}, V_{DDIO2}) + 3.6 V and 5.5 V.
5. For operation with voltage higher than min (V_{DD}, V_{DDA}, V_{DDIO2}) +0.3 V, the internal pull-up and pull-down resistors must be disabled.
6. In VOS0 mode, the max T_J is 105 °C.
7. P_{Dmax} is calculated based on relevant Θ_{JA} (characterized in line with JEDEC51-2), for further details, see *Section 6.7: Package thermal characteristics* and the AN5036.
8. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 6.7: Package thermal characteristics*).
9. In the low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 6.7: Package thermal characteristics*).

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Table 17. Maximum allowed clock frequencies

Symbol(1)(2)	Parameter	VOS0	VOS1	VOS2	VOS3	Unit
f_{CPU}	CPU	250	200	150	100	MHz
f_{HCLK}	AHB	250	200	150	100	
f_{PCLK}	APB	250	200	150	100	
$f_{fdcan_ker_ck}$	FDCAN	250	200	150	100	
$f_{I2C_ker_ck}$	I2C[1:2]	250	200	150	100	
$f_{I3C_ker_ck}$	I3C[1:2]	250	200	150	100	
$f_{lptim_ker_ck}$	LPTIM[1:2]	250	200	150	100	
$f_{rcc_tim_ker_ck}$	TIM[1:3],TIM[6:7]	250	200	150	100	
f_{rng_clk}	RNG	50	50	50	50	
$f_{spi_ker_ck}$	SPI[1:3]	250	200	150	100	
$f_{lpuart_ker_ck}$	LPUART1	250	200	150	100	
$f_{usart_ker_ck}$	USART1/2/3	250	200	150	100	
$f_{usb_ker_ck}$	USB	50	50	50	50	
$f_{adc_ker_ck}$	ADC	125	100	75	50	
f_{dac_pclk}	DAC	250	200	150	100	
$f_{rtc_ker_ck}$	RTC	1	1	1	1	

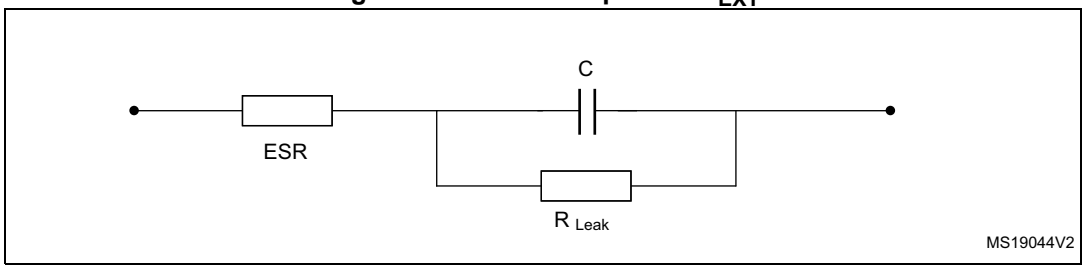
1. Specified by design - Not tested in production.
2. The maximum kernel clock frequencies can be limited by the maximum peripheral clock frequency (refer to each peripheral electrical characteristic).

5.3.2 VCAP external capacitor

Stabilization for the embedded LDO regulator is achieved by connecting an external capacitor C_{EXT} to the VCAPx (one or two pins depending on the packages). C_{EXT} is specified in *Table 18: VCAP operating condition*. Two external capacitors must be connected to VCAP pins (for more information, refer to the AN5711 (Getting started with STM32H5 MCU hardware development).

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Figure 13. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 18. VCAP operating condition

Symbol	Parameter	Conditions
C_{EXT}	External capacitor for LDO enabled	2.2 µF(1)
ESR	ESR of external capacitor	< 100 mΩ

1. This value corresponds to the C_{EXT} typical value. A variation of ±20 % is tolerated.

When the internal LDO voltage regulator is switched OFF, the two 2.2 µF VCAP capacitors are not required. However, all VCAPx package pins must be connected and it is recommended to add a ceramic filtering capacitor of 100 nF as close as possible to each VCAPx pin.

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5.3.3 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Operating conditions at power-up / power-down (regulator ON)

Table 19. Operating conditions at power-up/power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
T_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	
T_{VDDA}	V_{DDA} rise time rate	0	∞	
	V_{DDA} fall time rate	10	∞	
T_{VDDIO2}	T_{VDDIO2} rise time rate	0	∞	
	T_{VDDIO2} fall time rate	10	∞	
T_{VBAT}	T_{VBAT} rise time rate	0	∞	
	T_{VBAT} fall time rate	10	∞	

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5.3.4 Embedded reset and power control block characteristics

The parameters given in *Table 20: Embedded reset and power control block characteristics* are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 16: General operating conditions*.

Table 20. Embedded reset and power control block characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after POR is detected	V_{DD} rising	-	377	550	µs
$V_{POR/PDR}$	Power-on/power-down reset threshold (BORH_EN =0)	Rising edge	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brownout reset threshold 1 (BORH_EN =1)	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brownout reset threshold 2 (BORH_EN =1)	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brownout reset threshold 3 (BORH_EN =1)	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable voltage detector (PVD) threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable voltage detector (PVD) threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable voltage detector (PVD) threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable voltage detector (PVD) threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable voltage detector (PVD) threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable voltage detector (PVD) threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable voltage detector (PVD) threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge	2.69	2.76	2.83	
$V_{POR/PDR}$	Hysteresis for power-on/power-down reset	Hysteresis in run mode	-	43	-	mV
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BOR (unless BORH_EN = 0) and PVD	Hysteresis in run mode	-	100	-	
$I_{DD_BOR_PVD}$(2)	BOR and PVD consumption from V_{DD}	-	-	-	0.630	µA
$I_{DD_POR_PDR}$	POR and PDR consumption from V_{DD}	-	0.8	-	1.2	

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Table 20. Embedded reset and power control block characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVD0}	V_{DDA} voltage monitor 0 threshold	Rising edge	1.66	1.71	1.76	V
		Falling edge	1.56	1.61	1.66	
V_{AVD1}	V_{DDA} voltage monitor 1threshold	Rising edge	2.06	2.12	2.19	
		Falling edge	1.96	2.02	2.08	
V_{AVD2}	V_{DDA} voltage monitor 2 threshold	Rising edge	2.42	2.50	2.58	
		Falling edge	2.35	2.42	2.49	
V_{AVD3}	V_{DDA} voltage monitor 3 threshold	Rising edge	2.74	2.83	2.91	
		Falling edge	2.64	2.72	2.80	
V_{IO2VM}	V_{DDIO2} voltage monitor threshold	-	-	0.9	-	V
V_{hyst_AVD}	Hysteresis of V_{DDA} voltage detector	-	-	100	-	mV
$I_{DD_AVD_IO2VM}$(2)	Power voltage detector consumption from V_{DD} (AVD, IO2VM)	-	-	-	0.25	µA
$I_{DD_AVD_A}$(2)	V_{DDA} analog voltage detector consumption from VDDA (resistor bridge)	-	-	-	0.25	

1. Evaluated by characterization and not tested in production, unless otherwise specified.
2. Specified by design - Not tested in production.

5.3.5 Embedded reference voltage

The parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21*.

Table 21. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}(1)	Internal reference voltage	-40 °C < T_J < +130 °C	1.180	1.216	1.255	V
$t_{S_vrefint}$(2)(3)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat}	V_{BAT} sampling time when reading the internal V_{BAT} voltage		9	-	-	
$t_{start_vrefint}$(3)	Start time of reference voltage buffer when the ADC is enabled	-	-	-	4.4	
I_{refbuf}(3)	Reference buffer consumption for ADC	V_{DD} = 3.3 V	9	13.5	23	µA
ΔV_{REFINT}(3)	Internal reference voltage spread over the temperature range	-40°C < T_J < +130 °C	-	5	15	mV
T_{Coeff}	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	10	1370	ppm/V

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Table 21. Embedded reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT_DIV1} (3)	1/4 reference voltage	-	-	25	-	% V_{REFINT}
V_{REFINT_DIV2} (3)	1/2 reference voltage		-	50	-	
V_{REFINT_DIV3} (3)	3/4 reference voltage		-	75	-	

1. V_{REFINT} does not take into account package and soldering effects.
2. The shortest sampling time for the application can be determined by multiple iterations.
3. Specified by design - Not tested in production.

Table 22. Internal reference voltage calibration value

Symbol	Parameter	Memory address
V_{REFINT_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA} = 3.3 V	0x08FF F810 - 0x08FF F811

5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 12: Current consumption measurement scheme*.

All the run mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait-state number, depending on the f_{HCLK} frequency (refer to the table “FLASH recommended number of wait states and programming delay” available in the reference manual).
- When the peripherals are enabled, f_{PCLK} = $_{HCLK}$.

The parameters given in the below tables are derived from tests performed under supply voltage conditions summarized in *Table 16: General operating conditions* and unless otherwise specified at ambient temperature.

The typical and maximum current consumptions provided in the following tables are given for LDO regulator ON.

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Table 23. Typical and maximum current consumption in run mode, code with data processing running from flash memory, 2-ways instruction cache ON, PREFETCH ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
I_{DD} (Run)	Supply current in run mode	All peripherals disabled	VOS0	250	25.5	27.16	34.76	41.26	-	mA
				215	22.0	23.57	31.24	37.75	-	
				200	20.0	21.63	29.37	35.89	-	
			VOS1	200	17.5	18.67	23.89	28.64	37.39	
				180	16.0	17.19	22.45	27.21	35.94	
				168	14.5	15.83	21.13	25.88	34.60	
				150	13.5	14.25	19.59	24.34	33.04	
			VOS2	150	12.0	13.01	17.12	20.98	28.19	
				100	8.5	9.11	13.34	17.20	24.40	
			VOS3	100	7.8	8.36	11.57	14.70	20.62	
				60	5.0	5.52	8.81	11.92	17.82	
				25	2.5	2.96	6.31	9.41	15.30	
		All peripherals enabled	VOS0	250	43.0	45.89	53.12	59.58	-	
				215	37.0	39.68	47.02	53.51	-	
				200	34.0	36.63	44.04	50.54	-	
			VOS1	200	30.0	31.82	36.69	41.41	50.19	
				180	27.5	29.02	33.97	38.70	47.47	
				150	22.5	24.09	29.17	33.91	42.66	
			VOS2	150	20.5	21.99	25.82	29.66	36.90	
				100	14.0	15.08	19.13	22.99	30.20	
			VOS3	100	13.0	13.77	16.81	19.92	25.84	
				60	8.2	8.73	11.94	15.05	20.96	
				25	3.8	4.28	7.60	10.69	16.59	

1. Evaluated by characterization - Not tested in production.

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Table 24. Typical and maximum current consumption in run mode, code with data processing running from flash memory, 1-way instruction cache ON, PREFETCH ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
I_{DD} (Run)	Supply current in run mode	All peripherals disabled	VOS0	250	22.5	24.26	31.96	38.49	-	mA
				200	17.7	19.32	27.14	33.65	-	
			VOS1	200	15.5	16.67	21.97	26.74	35.48	
				180	14.3	15.40	20.73	25.50	34.24	
				150	11.8	12.76	18.16	22.93	31.65	
			VOS2	150	10.9	11.66	15.83	19.71	26.93	
				100	7.6	8.24	12.51	16.37	23.58	
			VOS3	100	6.9	7.48	10.77	13.89	19.83	
				25	2.3	2.76	6.12	9.23	15.14	
		All peripherals enabled	VOS0	250	40.3	42.96	50.28	56.78	-	
			VOS1	200	28.1	29.79	34.74	39.48	48.27	
				180	25.6	27.20	32.22	36.96	45.75	
			VOS2	150	19.5	20.62	24.52	28.38	35.63	
			VOS3	100	12.1	12.90	15.98	19.10	25.05	

1. Evaluated by characterization - Not tested in production.

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Table 25. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 1-WAY

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
I_{DD} (Run)	Supply current in run mode	All peripherals disabled	VOS0	250	21.5	23.20	30.91	37.44	-	mA
				215	18.6	20.14	27.95	34.46	-	
				200	17.0	18.47	26.29	32.79	-	
			VOS1	200	14.9	15.90	21.21	25.98	34.73	
				180	13.7	14.72	20.06	24.83	33.57	
				150	11.3	12.19	17.61	22.37	31.11	
			VOS2	150	10.4	11.15	15.33	19.20	26.43	
				100	7.2	7.90	12.17	16.04	23.25	
			VOS3	100	6.7	7.20	10.47	13.59	19.53	
				60	4.3	4.81	8.15	11.27	17.20	
				25	2.2	2.69	6.05	9.16	15.07	

1. Evaluated by characterization - Not tested in production.

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Table 26. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 2-WAY

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
I_{DD} (Run)	Supply current in run mode	All peripherals disabled	VOS0	250	24.6	26.30	33.94	40.48	-	mA
				215	21.2	22.80	30.54	37.06	-	
				200	19.4	20.93	28.70	35.19	-	
			VOS1	200	17.0	18.04	23.28	28.05	36.84	
				180	15.6	16.62	21.92	26.70	35.45	
				168	14.3	15.31	20.64	25.43	34.17	
				150	12.8	13.78	19.15	23.92	32.66	
			VOS2	150	11.8	12.57	16.71	20.58	27.82	
				100	8.2	8.83	13.08	16.95	24.18	
			VOS3	100	7.6	8.10	11.33	14.47	20.42	
				60	4.9	5.37	8.67	11.81	17.73	
				25	2.4	2.90	6.26	9.37	15.29	

1. Evaluated by characterization - Not tested in production.

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Table 27. Typical current consumption in run mode with CoreMark

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Unit	Typ LDO	Unit
		Peripheral	Code					
I_{DD} (Run)	Supply current in run mode	All peripherals disabled, instruction cache 2-WAY, prefetch ON	FLASH	250	25.5	mA	102.0	µA/MHz
				200	17.5		87.5	
				168	14.5		86.3	
				150	12.0		80.0	
				100	7.8		78.0	
		All peripherals disabled, instruction cache 1-WAY, prefetch ON	FLASH	250	22.5		90.0	
				200	15.5		77.5	
				150	10.9		72.7	
				100	6.9		69.0	
		All peripherals disabled, instruction cache 2-WAY	SRAM	250	26.1		104.4	
				200	17.0		85.0	
				168	14.3		85.1	
				150	11.8		78.7	
				100	7.6		76.0	
		All peripherals disabled, instruction cache 1-WAY	SRAM	250	21.5		86.0	
				200	14.9		74.5	
				150	10.4		69.3	
				100	6.7		67.0	

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Table 28. Typical current consumption in run mode with SecureMark running from flash memory

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Unit	Typ LDO	Unit
		Peripheral	Code					
I_{DD} (Run)	Supply current in run mode	All peripherals disabled, instruction cache 2-WAY, prefetch ON	FLASH	250	27.2	mA	108.8	µA/MHz
				180	17.3		96.4	
				168	15.9		94.9	
				150	13.3		88.5	
				100	8.5		85.4	
		All peripherals disabled, instruction cache 1-WAY, prefetch ON	FLASH	250	24.6		98.3	
				180	15.7		87.3	
				168	14.4		85.9	
				150	12.1		80.5	
				100	7.8		77.7	

Table 29. Typical and maximum current consumption in sleep mode

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
I_{DD} (sleep)	Supply current in sleep mode	All peripherals disabled	VOS0	250	5.1	6.34	14.19	20.59	-	mA
				200	3.9	5.06	12.91	19.29	-	
			VOS1	200	3.4	4.14	9.65	14.33	22.95	
				180	3.4	4.14	9.65	14.33	22.95	
				168	2.9	3.68	9.19	13.87	22.48	
				150	2.7	3.42	8.94	13.61	22.22	
			VOS2	150	2.5	3.00	7.36	11.17	18.31	
				100	2.0	2.50	6.86	10.67	17.79	
			VOS3	100	1.8	2.20	5.63	8.71	14.59	
				60	1.4	1.83	5.27	8.35	14.21	

1. Evaluated by characterization - Not tested in production.

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Table 30. Typical and maximum current consumption in stop mode

Symbol	Parameter	Conditions		Typ LDO	Max(1)				Unit
					T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 130°C	
I_{DD} (stop)	Supply current in stop	Flash memory in low power mode, SRAM1/2 ON	SVOS3	0.088	0.38	3.05	5.48	10.15	mA
			SVOS4	0.070	0.28	2.33	4.26	8.04	
			SVOS5	0.054	0.18	1.60	3.01	5.82	
		Flash memory in normal mode, SRAM1/2 ON	SVOS3	0.103	0.40	3.07	5.51	10.19	
			SVOS4	0.085	0.29	2.35	4.29	8.08	
		Flash memory in low power mode, SRAM1/2 OFF	SVOS3	0.085	0.37	2.99	5.37	9.95	
			SVOS4	0.068	0.27	2.29	4.18	7.88	
			SVOS5	0.052	0.17	1.56	2.91	5.64	
		Flash memory in normal mode, SRAM1/2 OFF	SVOS3	0.100	0.39	3.02	5.40	9.99	
			SVOS4	0.083	0.29	2.31	4.21	7.93	

1. Evaluated by characterization - Not tested in production.

Table 31. Typical and maximum current consumption in standby mode

Symbol	Parameter	Conditions		Typ				Max(1)				Unit
		Backup RAM	RTC and LSE(2)	1.8 V	2.4 V	3 V	3.3 V	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 130 °C	
I_{DD} (standby)	Supply current in standby mode, IWDG OFF	OFF	OFF	2.47	2.66	2.91	3.05	4.02	8.05	13.86	30.71	µA
		ON	OFF	3.49	3.73	4.01	4.20	5.67	12.90	22.16	48.95	
		OFF	ON	2.84	3.05	3.31	3.49	-	-	-	-	
		ON	ON	3.86	4.12	4.44	4.66	-	-	-	-	

1. Evaluated by characterization - Not tested in production.
2. LSE is in medium low-drive mode.

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Table 32. Typical and maximum current consumption in VBAT mode

Symbol	Parameter	Conditions		Typ (V)				Max(1) (°C)				Unit
		Backup RAM	RTC and LSE(2)	1.62	2	3	3.3	T_J = 25	T_J = 85	T_J = 105	T_J = 130	
I_{DD} (VBAT)	Supply current in V_{BAT} mode	OFF	OFF	0.01	0.01	0.02	0.03	0.10	1.34	3.39	9.76	µA
		ON	OFF	0.73	0.86	1.07	1.16	1.98	8.33	14.91	34.23	
		OFF	ON	0.32	0.35	0.38	0.45	-	-	-	-	
		ON	ON	1.33	1.39	1.52	1.65	-	-	-	-	

1. Evaluated by characterization - Not tested in production.
2. LSE is in medium low-drive mode.

I/O system current consumption

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 53: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins, which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

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Where:

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DDx} is the MCU supply voltage
- f_{SW} is the I/O switching frequency
- C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- f_{HCLK} is the CPU clock.

The given value is calculated by measuring the difference of current consumption:

- With all peripherals clocked off
- With only one peripheral clocked on
- f_{HCLK} = 250 MHz (scale 0), f_{HCLK} = 200 MHz (scale 1), f_{HCLK} = 150 MHz (scale 2), f_{HCLK}= 100 MHz (scale 3)
- The ambient operating temperature and supply voltage conditions are summarized in *Table 16: General operating conditions*

Table 33. Peripheral current consumption in sleep mode

BUS	Peripheral	IDD (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB1	SRAM1	0.69	0.60	0.55	0.51	µA/MHz
	BKPSRAM	1.01	0.89	0.81	0.74	
	GTZC1	1.12	0.98	0.90	0.81	
	ICACHE	0.84	0.75	0.68	0.62	
	RAMCFG	0.48	0.41	0.38	0.35	
	CRC	0.35	0.31	0.28	0.27	
	FLASH	7.88	6.89	6.28	5.71	
	GPDMA2	0.33	0.29	0.26	0.25	
	GPDMA1	0.43	0.38	0.35	0.32	

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Table 33. Peripheral current consumption in sleep mode (continued)

BUS	Peripheral	IDD (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
AHB2	SRAM2	0.95	0.85	0.77	0.70	µA/MHz
	RNG	0.81	0.72	0.66	0.59	
	HASH	0.87	0.77	0.71	0.64	
	DAC1	1.18	1.04	0.95	0.86	
	ADC1	1.30	1.15	1.05	0.95	
	GPIOH	0.08	0.08	0.07	0.06	
	GPIOD	0.05	0.05	0.04	0.03	
	GPIOC	0.06	0.05	0.05	0.04	
	GPIOB	0.09	0.07	0.07	0.06	
	GPIOA	0.06	0.05	0.05	0.04	
APB1	FDCAN SRAM	3.14	2.76	2.51	2.29	µA/MHz
	FDCAN1	3.20	2.82	2.58	2.34	
	LPTIM2	0.91	0.81	0.72	0.67	
	DTS	1.49	1.31	1.20	1.11	
	CRS	0.24	0.22	0.18	0.18	
	I3C1	0.31	0.29	0.25	0.24	
	I2C2	0.63	0.57	0.50	0.47	
	I2C1	0.61	0.54	0.48	0.44	
	USART3	1.35	1.19	1.08	0.99	
	USART2	1.37	1.22	1.10	1.35	
	COMP	0.23	0.21	0.17	0.17	
	SPI3/I2S3	1.08	0.96	0.85	0.78	
	SPI2/I2S2	1.10	0.97	0.87	0.79	
	OPAMP	0.13	0.13	0.10	0.10	
	WWDG	1.18	0.17	0.14	0.13	
	TIM7	0.57	0.51	0.46	0.42	
	TIM6	0.54	0.49	0.44	0.40	
	TIM3	2.44	2.15	1.96	1.78	
	TIM2	2.81	2.49	2.27	2.07	
APB2	USB	2.49	2.17	1.99	1.80	µA/MHz
	USART1	1.34	1.18	1.08	0.97	
	SPI1/I2S1	1.15	1.01	0.93	0.83	
	TIM1	4.39	3.87	3.55	3.23	

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Table 33. Peripheral current consumption in sleep mode (continued)

BUS	Peripheral	IDD (typ)				Unit
		VOS0	VOS1	VOS2	VOS3	
APB3	RTC	1.72	1.51	1.38	1.26	µA/MHz
	LPTIM1	0.92	0.82	0.75	0.68	
	I3C2	0.31	0.28	0.25	0.23	
	SBS	0.45	0.40	0.37	0.34	

Wakeup time from low-power modes

The wakeup times given in *Table 34: Low-power mode wakeup timings* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA1) pin is used to wakeup from Standby, Stop, and Sleep modes.

All timings are derived from tests performed under ambient temperature and VDD=3.0 V.

Table 34. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from sleep	Instruction cache enabled	15	16	CPU clock cycles
		Instruction cache disabled	15	16	
t_{WUSTOP}	Wakeup time from stop mode	SVOS3, HSI 64MHz, flash memory in normal mode	4.0	4.8	µs
		SVOS3, HSI 64MHz, flash memory in low-power mode	7.9	11.5	
		SVOS4, HSI 64MHz, flash memory in normal mode	13.8	16.0	
		SVOS4, HSI 64MHz, flash memory in low-power mode	17.7	21.9	
		SVOS5, HSI 64MHz, flash memory in low-power mode	31.4	36.8	
		SVOS3, CSI 4MHz, flash memory in normal mode	25.5	31.0	
		SVOS3, CSI 4MHz, flash memory in low power mode	27.7	34.2	
		SVOS4, CSI 4MHz, flash memory in normal mode	35.3	40.8	
		SVOS4, CSI 4 MHz, flash memory in low-power mode	37.5	44.0	
		SVOS5, CSI 4 MHz, flash memory in low-power mode	51.2	58.9	
t_{WUSTBY}	Wakeup time from standby mode	VCAP capacitors discharged	506.0	653.6	

1. Evaluated by characterization - Not tested in production.

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5.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the *Table 35: High-speed external user clock characteristics* in addition to *Table 53: I/O static characteristics*. The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0492).

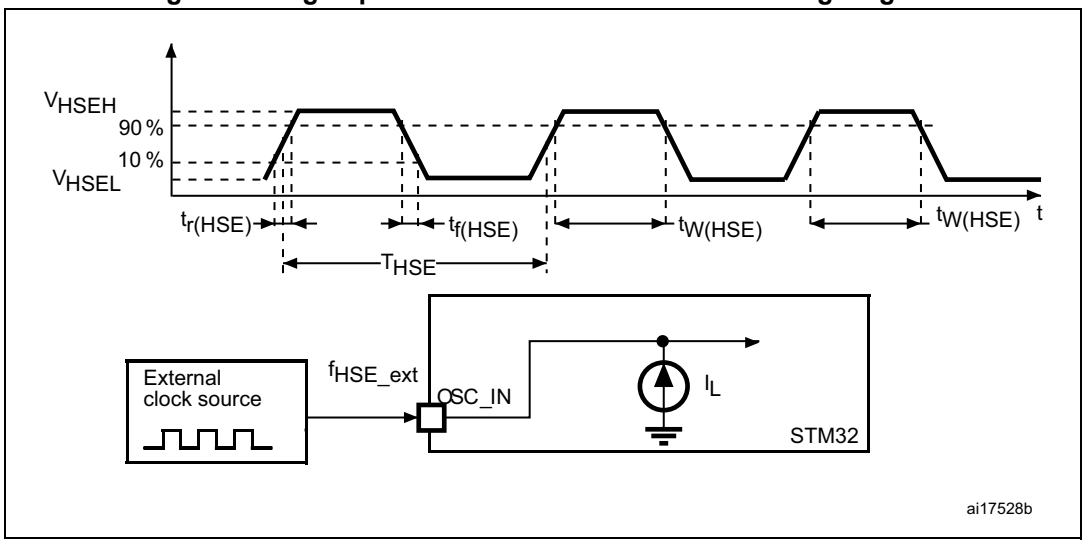
Table 35. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	External digital/analog clock	4	25	50	MHz
V_{HSEH}	Digital OSC_IN input high-level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input low-level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}/t_{w(HSEL)}$ (2)	Digital OSC_IN input high or low time	External digital clock	7	-	-	ns
$V_{isw(HSEH)}$ (V_{HSEH} -V_{HSEH})(3)	Analog low-swing OSC_IN peak-to-peak amplitude	External analog low swing clock	0.2	-	2/3 V_{DD}	V
$DuCy_{HSE}$	Analog low-swing OSC_IN duty cycle		45	50	55	%
$t_{r(HSE)}/t_{f(HSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low swing clock, 10% to 90%	0.05 / f_{HSE_ext}	-	0.3 / f_{HSE_ext}	ns

1. Specified by design - Not tested in production.
2. The rise and fall times for a digital input signal are not specified. However, the V_{HSEH} and V_{HSEL} conditions must be fulfilled.
3. The DC component of the signal must ensure that the signal peaks are located between V_{DD} and V_{SS}.

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Figure 14. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the *Table 36: Low-speed external user clock characteristics* in addition to *Table 53: I/O static characteristics*. The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0492).

Table 36. Low-speed external user clock characteristics(1)

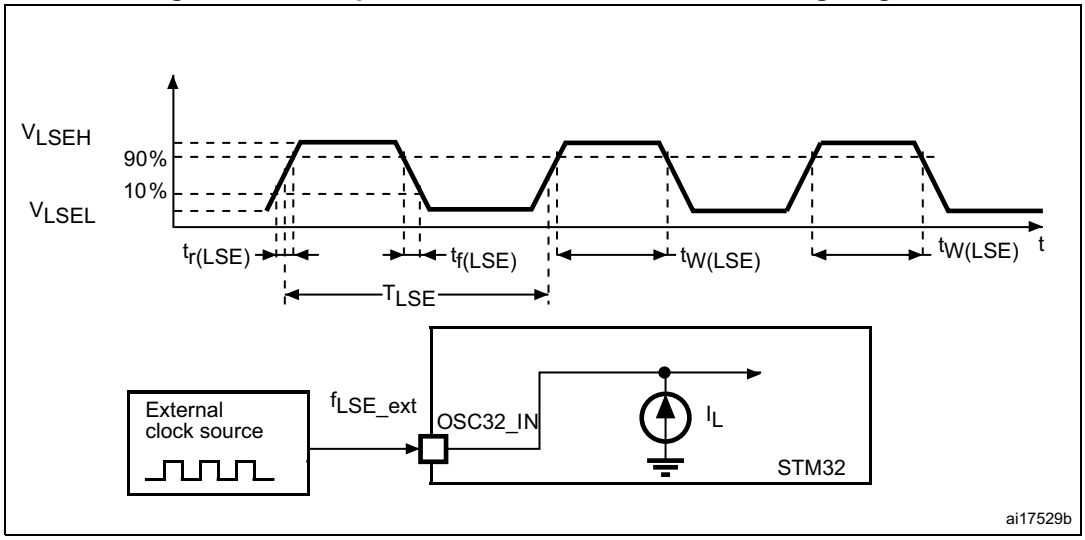
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	External digital/analog clock	-	32.768	1000	kHz
V_{LSEH}	Digital OSC32_IN input high-level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input low-level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(LSEH)}/t_{w(LSEL)}$	OSC32_IN high or low time	External digital clock	250	-	-	ns
V_{lsw_H}	Analog low-swing OSC_IN high-level voltage	External analog low swing clock	0.6	-	1.225	V
V_{lsw_L}	Analog low-swing OSC_IN low-level voltage		0.35	-	0.8	
V_{lswLSE} (V_{LSEH} -V_{LSEL})	Analog low-swing OSC_IN peak-to-peak amplitude		0.2	-	0.875	
$DuCy_{LSE}$	Analog low-swing OSC_IN duty cycle		45	50	55	%
$t_{r(LSE)}/t_{f(LSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low swing clock, 10% to 90%	-	100	200	ns

1. Specified by design - Not tested in production.

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Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 15. Low-speed external clock source AC timing diagram



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High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 50 MHz crystal/ceramic resonator oscillator.

All the information given in this paragraph are based on characterization results obtained with the typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 37. HSE oscillator characteristics(1)

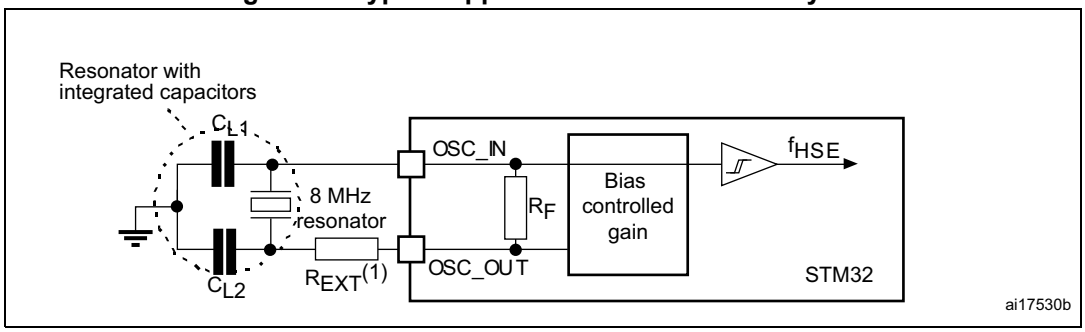
Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	50	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	10	mA
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 4 MHz	-	0	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF@8 MHz	-	0	-	
		V_{DD} = 3 V, Rm = 20 Ω, CL = 10 pF@16 MHz	-	1	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF@32 MHz	-	1	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF@48 MHz	-	1	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Specified by design - Not tested in production.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment that it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

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Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 38*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

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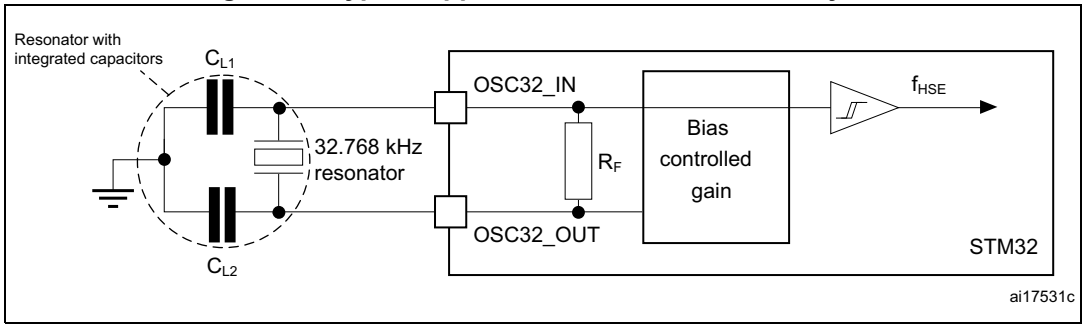
Table 38. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 01 Medium low drive capability	-	333.000	-	nA
		LSEDRV[1:0] = 10 Medium high drive capability	-	462.000	-	
		LSEDRV[1:0] = 11 High drive capability	-	747.000	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	µA/V
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Specified by design - Not tested in production, unless otherwise specified.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment that it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs available from the ST website www.st.com.

Figure 17. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

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5.3.8 Internal clock source characteristics

The parameters given in *Table 39: HSI48 oscillator characteristics* to *Table 42: LSI oscillator characteristics* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*.

48 MHz high-speed internal RC oscillator (HSI48)

Table 39. HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD}=3.3 V, T_J=30 °C	47.5(1)	48	48.5(1)	MHz
TRIM(2)	User trimming step	-	-	0.175	0.250	%
USER TRIM COVERAGE(3)	User trimming coverage	± 32 steps	±4.70	±5.6	-	
DuCy(HSI48)(2)	Duty Cycle	-	45	-	55	%
ACCHSI48_REL(3)(4)	Accuracy of the HSI48 oscillator over temperature (reference is 30 °C)	T_J= -40 to 130 °C	-4.5	-	4	%
Δ_{VDD}(HSI48)(2)	HSI48 oscillator frequency drift with V_{DD} (reference is 3.3 V)	V_{DD}= 3.0 to 3.6 V	-	0.025	0.05	%
		V_{DD}= 1.71 to 3.6 V	-	0.05	0.1	%
t_{su}(HSI48)(2)	HSI48 oscillator start-up time	-	-	2.1	4.0	µs
I_{DD}(HSI48)(2)	HSI48 oscillator power consumption	-	-	350	400	µA
N_T jitter(2)	Next transition jitter accumulated jitter on 28 cycles	-	-	±0.15	-	ns
P_T jitter(2)	Paired transition jitter accumulated jitter on 56 cycles(5)	-	-	±0.25	-	ns

1. Calibrated during manufacturing tests.
2. Specified by design - Not tested in production.
3. Evaluated by characterization - Not tested in production.
4. Δf_{HSI} = ACCHSI48_REL + ΔV_{DD}.
5. Jitter measurements are performed without clock sources activated in parallel.

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64 MHz high-speed internal RC oscillator (HSI)

Table 40. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	V_{DD}=3.3 V, T_J=30 °C	63.7(2)	64(2)	64.3(2)	MHz
TRIM	User trimming step	Trimming is not a multiple of 32(3)	-	0.24	0.32	%
		Trimming is 128, 256 and 384(3)	-5.2	-1.8	-	
		Trimming is 64, 192, 320 and 488(3)	-1.4	-0.8	-	
		Other trimming are a multiple of 32 (not including multiple of 64 and 128)(3)	-0.6	-0.25	-	
DuCy(HSI)	Duty cycle	-	45	-	55	%
Δ_{VDD}(HSI)	HSI oscillator frequency drift with V_{DD} (reference is 3.3 V)	V_{DD}= 1.71 to 3.6 V	-0.12	-	0.03	%
Δ_{TEMP}(HSI)	HSI oscillator frequency drift with V_{DD} (reference is 64 MHz)	T_J= -20 to 105 °C	-1(4)	-	1(4)	%
		T_J= -40 to 130 °C	-2(4)	-	1(4)	%
t_{su}(HSI)	HSI oscillator start-up time	-	-	1.4	2	µs
t_{stab}(HSI)	HSI oscillator stabilization time	at 1% of target frequency	-	4	8	µs
		at 5% of target frequency	-	-	4	
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	450	µA

1. Specified by design - Not tested in production, unless otherwise specified.
2. Calibrated during manufacturing tests.
3. Trimming value of HSICAL[8:0.]
4. Evaluated by characterization. Not tested in production.

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4 MHz low-power internal RC oscillator (CSI)

Table 41. CSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CSI}	CSI frequency	V_{DD}=3.3 V, T_J=30 °C	3.96(2)	4	4.04(2)	MHz
TRIM	User trimming step	Trimming is not a multiple of 16	-	0.40	0.75	%
		Trimming is a multiple of 32	-4.75	-2.75	0.75	
		Other trimming are a multiple of 16 (not including multiple of 32)	-0.43	0.00	0.75	
DuCy(CSI)	Duty Cycle	-	45	-	55	%
Δ_{TEMP}(CSI)	CSI oscillator frequency drift over temperature	T_J= 0 to 85 °C	-3.7(3)	-	4.5(3)	%
		T_J= -40 to 130 °C	-11(3)	-	7.5(3)	%
Δ_{VDD}(CSI)	CSI oscillator frequency drift over V_{DD}	V_{DD}= 1.71 to 3.6 V	-0.06	-	0.06	%
t_{su}(CSI)	CSI oscillator start-up time	-	-	1	2	µs
t_{stab}(CSI)	CSI oscillator stabilization time (to reach ± 3% of f_{CSI})	-	-	-	4	Cycle
I_{DD}(CSI)	CSI oscillator power consumption	-	-	23	30	µA

1. Specified by design - Not tested in production, unless otherwise specified.
2. Calibrated during manufacturing tests.
3. Evaluated by characterization - Not tested in production.

Low-speed internal (LSI) RC oscillator

Table 42. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD}=3.3 V, T_J= 25 °C	31.4(1)	32	32.6(1)	kHz
		T_J= -40 to 110 °C, V_{DD}=1.71 to 3.6 V	29.76 (2)	-	33.6(2)	
		T_J= -40 to 130 °C, V_{DD}=1.71 to 3.6 V	29.4(2)	-	33.6(2)	
t_{su}(LSI)(3)	LSI oscillator start-up time	-	-	80	130	µs
t_{stab}(LSI)(3)	LSI oscillator stabilization time (5% of final value)	-	-	120	170	
I_{DD}(LSI)(3)	LSI oscillator power consumption	-	-	130	280	nA

1. Calibrated during manufacturing tests.
2. Evaluated by characterization - Not tested in production.
3. Specified by design - Not tested in production.

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5.3.9 PLL characteristics

The parameters given in *Table 43* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*.

Table 43. PLL characteristics (wide VCO frequency range)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		2	-	16	MHz
	PLL input clock duty cycle	-		10	-	90	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P, Q, R	VOS0		1	-	250(2)	MHz
		VOS1		1	-	200(2)	
		VOS2		1	-	150(2)	
		VOS3		1	-	100(2)	
f_{VCO_OUT}	PLL VCO output	-		128	-	560(2)	
t_{LOCK}	PLL lock time	Normal mode		-	45	100(3)	µs
		Sigma-delta mode (f_{PLL_IN} ≥ 8 MHz)		-	60	120(3)	
Jitter	Cycle-to-cycle jitter	f_{VCO_OUT} = 128 MHz		-	60	-	±ps
		f_{VCO_OUT} = 200 MHz		-	50	-	
		f_{VCO_OUT} = 400 MHz		-	20	-	
		f_{VCO_OUT} = 560 MHz		-	15	-	
	Long term jitter	Normal mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz		-	±0.2	-	%
		Normal mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz		-	±0.8	-	
		Sigma-delta mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz		-	±0.2	-	
		Sigma-delta mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz		-	±0.8	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}	f_{VCO_OUT} = 560 MHz	V_{DD}	-	330	420	µA
			V_{CORE}	-	630	-	
		f_{VCO_OUT} = 128 MHz	V_{DD}	-	155	230	
			V_{CORE}	-	170	-	

1. Specified by design - Not tested in production, unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.
3. Evaluated by characterization - Not tested in production.

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Table 44. PLL characteristics (medium VCO frequency range)

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
f_{PLL_IN}	PLL input clock	-		1	-	2	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS0		1.17	-	210	MHz
		VOS1		1.17	-	210	
		VOS2		1.17	-	160(2)	
		VOS3		1.17	-	88(2)	
f_{VCO_OUT}	PLL VCO output	-		150	-	420	
t_{LOCK}	PLL lock time	Normal mode		-	45	80(3)	µs
		Sigma-delta mode		forbidden			
Jitter	Cycle-to-cycle jitter	f_{VCO_OUT} = 150 MHz	-	-	60	-	±ps
		f_{VCO_OUT} = 200 MHz	-	-	40	-	
		f_{VCO_OUT} = 400 MHz	-	-	18	-	
		f_{VCO_OUT} = 420 MHz	-	-	15	-	
	Period jitter	f_{VCO_OUT} = 150 MHz	f_{PLL_OUT} = 50 MHz	-	75	-	
		f_{VCO_OUT} = 400 MHz		-	25	-	
	Long term jitter	Normal mode f_{VCO_OUT} = 400 MHz		-	±0.2	-	%
I_{DD}(PLL)	PLL power consumption on V_{DD}	f_{VCO_OUT} = 420 MHz	V_{DD}	-	275	360	µA
			V_{CORE}	-	450	-	
		f_{VCO_OUT} = 150 MHz	V_{DD}	-	160	240	
			V_{CORE}	-	165	-	

1. Specified by design - Not tested in production, unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation.
3. Evaluated by characterization - Not tested in production.

5.3.10 Memory characteristics

Flash memory

The characteristics are given at T_J = -40 to 130 °C unless otherwise specified.

The devices are shipped to customers with the flash memory erased.

Table 45. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Word program (50% of bits at 0)	-	2.7	-	mA
		Sector erase	-	1.7	-	
		Mass erase	-	1.7	-	

1. Specified by design - Not tested in production.

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Table 46. Flash memory programming(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	Word program time	128 bits (user area)	-	31	-	µs
		16 bits (OTP area)	-	31	-	
t_{ERASE}	Sector erase time (8 Kbytes)	-	-	2	-	ms
t_{ME}	Bank erase time		-	16	-	ms
	Mass erase time		-	32	-	
V_{prog}	Programming voltage		1.71	-	3.6	V

1. Specified by design - Not tested in production.

Table 47. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_J = -40 to +130 °C	10	kcycles
t_{RET}	Data retention	1 kcycle at T_A = 85 °C	30	Years
		10 kcycles at T_A = 55 °C	30	

1. Evaluated by characterization - Not tested in production.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 48*. They are based on the EMS levels and classes defined in application note AN1709 "*EMC design guide for STM8, STM32 and legacy MCUs*".

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Table 48. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, LQFP64, f_{HCLK} = 250 MHz, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on the PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015 *"Software techniques for improving microcontrollers EMC performance").*

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application, executing the EEMBC code, is running. This emission test is compliant with the SAE IEC61967-2 standard, which specifies the test board and the pin loading.

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Table 49. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/250 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	13	dBµV
			30 MHz to 130 MHz	6	
			130 MHz to 1 GHz	23	
			1 GHz to 2 GHz	10	
			EMI level	3.5	-

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C conforming to ANSI/ESDA/JEDEC JS-001	All packages	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All packages	C2a	500	V

1. Evaluated by characterization - Not tested in production.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output, and configurable I/O pin

These tests are compliant with the JESD78 IC latchup standard.

Table 51. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_J = 130 °C, conforming to JESD78,	II level A

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5.3.13 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of -5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 52. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on pins PA4, PA5, and PB1	0	0	mA
	Injected current on pins PB10, and PC6	0	N/A(2)	
	Injected current on all other I/Os	5	N/A	

1. Evaluated by characterization - Not tested in production.
2. Not applicable.

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 53: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 16: General operating conditions*. All I/Os are CMOS and TTL compliant (except for BOOT0).

Note: For information on GPIO configuration, refer to application note AN4899 "STM32 GPIO configuration for hardware settings and low-power consumption", available from the ST website www.st.com.

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Table 53. I/O static characteristics(1)

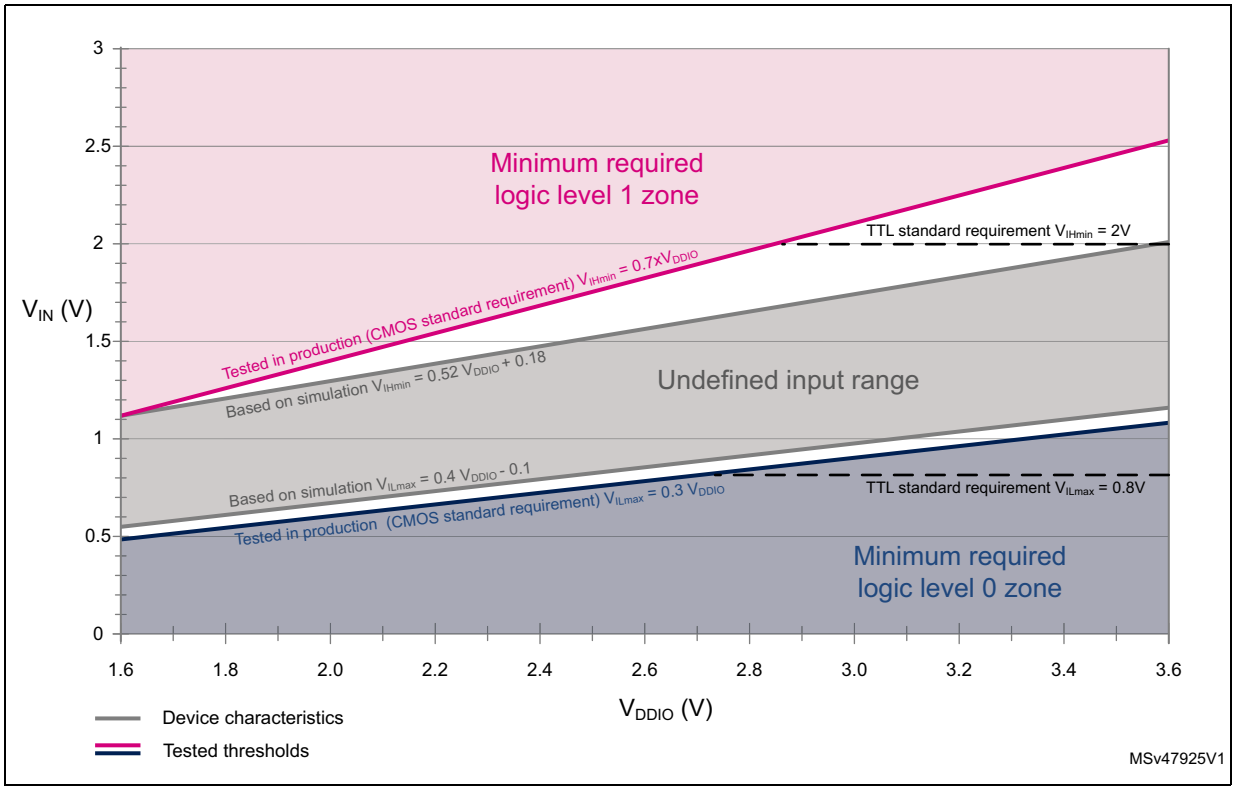
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage except BOOT0	1.08 V<V_{DDIOx}<3.6 V	-		$0.3V_{DDIOx}$(2)	V
	I/O input low level voltage except BOOT0		-		$0.4V_{DDIOx}$-0.1(3)	
	BOOT0 I/O input low level voltage		-		$0.19V_{DDIOx}$ + 0.1(3)	
V_{IH}	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<3.6 V	$0.7V_{DDIOx}$(2)			V
	I/O input high level voltage except BOOT0		$0.52V_{DDIOx}$+0.18(3)			
	BOOT0 I/O input high level voltage		$0.17V_{DDIOx}$+0.6(3)			
V_{HYS}(3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.08 V< V_{DDIOx} <3.6 V	-	250		mV
	BOOT0 I/O input hysteresis	1.71 V< V_{DD} <3.6 V	-	200		
I_{leak}(4)	FT_xx Input leakage current(3)	0< V_{IN} ≤ Max(V_{DDXXX})(7)	-	-	±200	nA
		Max(V_{DDXXX}) < V_{IN} ≤ Max(V_{DDXXX})+ 1 V) (5)(7)	-	-	2500	
		Max(V_{DDXXX}) < V_{IN} ≤ 5.5 V (5)(7)	-	-	750	
	TT_xx Input leakage current	0< V_{IN} ≤ Max(V_{DDXXX}) (7)	-	-	±200	
	BOOT0	0< V_{IN} ≤ V_{DDIOx}	-	-	15	
R_{PU}	Weak pull-up equivalent resistor(6)	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	V_{IN}=V_{DD}(7)	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DDIOx} represents V_{DD} or V_{DDIO2}.
2. Compliant with CMOS requirements.
3. Specified by design - Not tested in production.
4. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total_leak_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x $I_{lkg(Max)}$.
5. V_{IN} must be less than Max(VDDXXX) + 3.6 V.
6. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).
7. Max(V_{DDXXX}) is the maximum value of all the I/O supplies.

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All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 18*.

Figure 18. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general-purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins, which can drive current, must be limited to respect the absolute maximum rating specified in *Table 5.2: Absolute maximum ratings*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 14: Current characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 14: Current characteristics*).

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Output voltage levels

Unless otherwise specified, the parameters given in *Table 54: Output voltage characteristics for all I/Os except PC13, PC14 and PC15* and *Table 55: Output voltage characteristics for PC13* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 54. Output voltage characteristics for all I/Os except PC13, PC14 and PC15

Symbol	Parameter	Conditions(1)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 8 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -8 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 8 mA 2.7 V≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = -8 mA 2.7 V≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 20 mA 2.7 V≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}(3)	Output high level voltage	I_{IO} = -20 mA 2.7 V≤ V_{DD} ≤ 3.6 V	V_{DD} - 1.3	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 4 mA 1.71 V≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage	I_{IO} = -4 mA 1.71 V≤V_{DD} <3.6 V	V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 2 mA 1.08 V≤ V_{DDIO2} ≤ 1.32 V	-	0.3 x V_{DDIO2} 0.3	
V_{OH} (3)	Output high level voltage	I_{IO} = -2 mA 1.08 V≤V_{DDIO2} < 1.32 V	0.7 x V_{DDIO2}	-	
V_{OLFM+}(3)	Output low level voltage for an FTf I/O pin in (FT I/O with “f” option)	I_{IO} = 20 mA 2.3 V≤ V_{DD} ≤3.6 V	-	0.4	
		I_{IO} = 10 mA 1.71 V≤ V_{DD} ≤ 3.6 V	-	0.4	
		I_{IO} = 4.5 mA 1.08 V≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 13: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

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Table 55. Output voltage characteristics for PC13(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -3 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = -3 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 1.5 mA 1.71 V≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	I_{IO} = −1.5 mA 1.71 V≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 13: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Table 56. Output voltage characteristics for PC14 and PC15(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 0.5 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -0.5 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 0.5 mA 2.7 V ≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = -0.5 mA 2.7 V ≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 0.25 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	I_{IO} = -0.25 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 13: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

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Output buffer timing characteristics (HSLV option disabled)

The HSLV feature (can be enabled over option bytes IO_VDDIO2_HSLV and IO_VDD_HSLV) can be used to optimize the I/O speed when the product voltage is below 2.7 V.

Table 57. Output timing characteristics (HSLV OFF)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)(3)	Maximum frequency	C = 50 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	8	MHz
			C = 50 pF, 1.71 V≤V_{DD} ≤ 2 V	-	5	
			C = 40 pF, 2.7 V≤V_{DD} ≤ 3.6 V	-	10	
			C = 40 pF, 1.71 V≤V_{DD}≤ 2 V	-	5	
			C = 30 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	12	
			C = 30 pF, 1.71 V≤V_{DD}≤ 2 V	-	5	
			C = 20 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	14	
			C = 20 pF, 1.71 V≤V_{DD}≤ 2 V	-	5	
			C = 10 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	16	
			C = 10 pF, 1.71 V≤V_{DD}≤ 2 V	-	5	
	t_r/t_f(4)(5)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	18.0	ns
			C = 50 pF, 1.71 V≤V_{DD} ≤ 2 V	-	36.0	
			C = 40 pF, 2.7 V≤V_{DD} ≤ 3.6 V	-	17.0	
			C = 40 pF, 1.71 V≤V_{DD}≤ 2 V	-	34.0	
			C = 30 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	15.5	
			C = 30 pF, 1.71 V≤V_{DD}≤ 2 V	-	32.0	
			C = 20 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	14.2	
			C = 20 pF, 1.71 V≤V_{DD}≤ 2 V	-	30.0	
			C = 10 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	12.2	
			C = 10 pF, 1.71 V≤V_{DD}≤ 2 V	-	27	

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Table 57. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
01	F_{max}(2)(3)	Maximum frequency	C =50 pF, 2.7 V≤ V_{DD}≤3.6		40	MHz
			C = 50 pF, 1.71 V≤V_{DD} ≤ 2 V	-	12	
			C = 40 pF, 2.7 V≤V_{DD} ≤ 3.6 V	-	45	
			C = 40 pF, 1.71 V≤V_{DD}≤ 2 V	-	14	
			C = 30 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	50	
			C = 30 pF, 1.71 V≤V_{DD}≤ 2 V	-	16	
			C = 20 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	55	
			C = 20 pF, 1.71 V≤V_{DD}≤ 2 V	-	18	
			C = 10 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	60	
			C = 10 pF, 1.71 V≤V_{DD}≤ 2 V	-	20	
	t_r/t_f(4)(5)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	6.2	ns
			C = 50 pF, 1.71 V≤V_{DD} ≤ 2 V	-	11.4	
			C = 40 pF, 2.7 V≤V_{DD} ≤ 3.6 V	-	5.7	
			C = 40 pF, 1.71 V≤V_{DD}≤ 2 V	-	10.5	
			C = 30 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	5.1	
			C = 30 pF, 1.71 V≤V_{DD}≤ 2 V	-	9.5	
			C = 20 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	4.5	
			C = 20 pF, 1.71 V≤V_{DD}≤ 2 V		8.4	
			C = 10 pF, 2.7 V≤V_{DD}≤ 3.6 V		3.7	
			C = 10 pF, 1.71 V≤V_{DD}≤ 2 V		7.0	

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Table 57. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
10	F_{max}(2)(3) (6)	Maximum frequency	C =50 pF, 2.7 V≤ V_{DD}≤3.6	-	80	MHz
			C = 50 pF, 1.71 V≤V_{DD} ≤ 2 V	-	30	
			C = 40 pF, 2.7 V≤V_{DD} ≤ 3.6 V	-	90	
			C = 40 pF, 1.71 V≤V_{DD}≤ 2 V	-	35	
			C = 30 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	100	
			C = 30 pF, 1.71 V≤V_{DD}≤ 2 V	-	40	
			C = 20 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	110	
			C = 20 pF, 1.71 V≤V_{DD}≤ 2 V	-	45	
			C = 10 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	133	
			C = 10 pF, 1.71 V≤V_{DD}≤ 2 V	-	50	
	t_r/t_f(4)(5)(6)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	3.8	ns
			C = 50 pF, 1.71 V≤V_{DD} ≤ 2 V	-	7.5	
			C = 40 pF, 2.7 V≤V_{DD} ≤ 3.6 V	-	3.4	
			C = 40 pF, 1.71 V≤V_{DD}≤ 2 V	-	6.6	
			C = 30 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	2.9	
			C = 30 pF, 1.71 V≤V_{DD}≤ 2 V	-	5.7	
			C = 20 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	2.5	
			C = 20 pF, 1.71 V≤V_{DD}≤ 2 V	-	4.7	
			C = 10 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	1.9	
			C = 10 pF, 1.71 V≤V_{DD}≤ 2 V	-	3.7	

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Table 57. Output timing characteristics (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
11	F_{max}(2)(3)(6)	Maximum frequency	C =50 pF, 2.7 V≤ V_{DD}≤3.6	-	100	MHz
			C = 50 pF, 1.71 V≤V_{DD} ≤ 2 V	-	40	
			C = 40 pF, 2.7 V≤V_{DD} ≤ 3.6 V	-	120	
			C = 40 pF, 1.71 V≤V_{DD}≤ 2 V	-	50	
			C = 30 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	140	
			C = 30 pF, 1.71 V≤V_{DD}≤ 2 V	-	60	
			C = 20 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	166	
			C = 20 pF, 1.71 V≤V_{DD}≤ 2 V	-	70	
			C = 10 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	200	
			C = 10 pF, 1.71 V≤V_{DD}≤ 2 V	-	80	
	t_r/t_f(4)(5)(6)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	3.3	ns
			C = 50 pF, 1.71 V≤V_{DD} ≤ 2 V	-	6.3	
			C = 40 pF, 2.7 V≤V_{DD} ≤ 3.6 V	-	2.8	
			C = 40 pF, 1.71 V≤V_{DD}≤ 2 V	-	5.5	
			C = 30 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	2.3	
			C = 30 pF, 1.71 V≤V_{DD}≤ 2 V	-	4.6	
			C = 20 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	1.9	
			C = 20 pF, 1.71 V≤V_{DD}≤ 2 V	-	3.7	
			C = 10 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	1.4	
			C = 10 pF, 1.71 V≤V_{DD}≤ 2 V	-	3	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45% < Duty cycle < 55%
3. When 2 V < V_{DD} < 2.7 V maximum frequency is between values given for V_{DD} =1.98 V and V_{DD} =2.7 V
4. The fall and rise times are defined between 90% and 10% and between 10 % and 90 % of the output waveform, respectively.
5. When 2 V < V_{DD} < 2.7 V maximum tr/tf is between values given for V_{DD} = 1.98 V and V_{DD} = 2.7 V
6. Compensation cell enabled.

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Output buffer timing characteristics (HSLV option enabled)

Table 58. Output timing characteristics (HSLV ON)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C =50 pF, 1.71 V≤V_{DD}≤2 V	-	8	MHz
			C =40 pF, 1.71 V≤V_{DD}≤2 V	-	10	
			C =30 pF, 1.71 V≤V_{DD}≤2 V	-	12	
			C =20 pF, 1.71 V≤V_{DD}≤2 V	-	14	
			C =10 pF, 1.71 V≤V_{DD}≤2 V	-	16	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C =50 pF, 1.71 V≤V_{DD}≤2 V	-	17.8	ns
			C =40 pF, 1.71 V≤V_{DD}≤2 V	-	15.8	
			C =30 pF, 1.71 V≤V_{DD}≤2 V	-	14.4	
			C =20 pF, 1.71 V≤V_{DD}≤2 V	-	13.1	
			C =10 pF, 1.71 V≤V_{DD}≤2 V	-	11.4	
01	F_{max}(2)	Maximum frequency	C = 50 pF, 1.71 V≤V_{DD}≤2 V	-	40	MHz
			C = 40 pF, 1.71 V≤V_{DD}≤2 V	-	45	
			C = 30 pF, 1.71 V≤V_{DD}≤2 V	-	50	
			C = 20 pF, 1.71 V≤V_{DD}≤2 V	-	55	
			C =10 pF, 1.71 V≤V_{DD}≤2 V	-	60	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V≤V_{DD}≤2 V	-	7.2	ns
			C = 40 pF, 1.71 V≤V_{DD}≤2 V	-	6.5	
			C = 30 pF, 1.71 V≤V_{DD}≤2 V	-	5.6	
			C = 20 pF, 1.71 V≤V_{DD}≤2 V	-	4.8	
			C =10 pF, 1.71 V≤V_{DD}≤2 V	-	3.8	
10	F_{max}(2)(4)	Maximum frequency	C = 50 pF, 1.71 V≤V_{DD}≤2 V	-	60	MHz
			C = 40 pF, 1.71 V≤V_{DD}≤2 V	-	70	
			C = 30 pF, 1.71 V≤V_{DD}≤2 V	-	90	
			C = 20 pF, 1.71 V≤V_{DD}≤2 V	-	110	
			C =10 pF, 1.71 V≤V_{DD}≤2 V	-	140	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V≤V_{DD}≤2 V	-	5.3	ns
			C = 40 pF, 1.71 V≤V_{DD}≤2 V	-	4.6	
			C = 30 pF, 1.71 V≤V_{DD}≤2 V	-	3.8	
			C = 20 pF, 1.71 V≤V_{DD}≤2 V	-	3.0	
			C =10 pF, 1.71 V≤V_{DD}≤2 V	-	2.2	

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Table 58. Output timing characteristics (HSLV ON)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
11	F_{max}(2)(4)	Maximum frequency	C=50 pF, 1.71 V≤V_{DD}≤2 V	-	67	MHz
			C = 40 pF, 1.71 V≤V_{DD}≤2 V	-	100	
			C = 30 pF, 1.71 V≤V_{DD}≤2 V	-	120	
			C = 20 pF, 1.71 V≤V_{DD}≤2 V	-	155	
			C=10 pF, 1.71 V≤V_{DD}≤2 V	-	200	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.71 V≤V_{DD}≤2 V	-	5.0	ns
			C = 40 pF, 1.71 V≤V_{DD}≤2 V	-	4.1	
			C = 30 pF, 1.71 V≤V_{DD}≤2 V	-	3.3	
			C = 20 pF, 1.71 V≤V_{DD}≤2 V	-	2.5	
			C=10 pF, 1.71 V≤V_{DD}≤2 V	-	1.8	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45% < Duty cycle < 55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation cell enabled.

Table 59. Output timing characteristics VDDIO2 1.2 V range (HSLV OFF)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	1	MHz
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	1	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	1	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	1	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	1	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	83.0	ns
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	79.0	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	46.0	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	72.0	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	68.0	

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Table 59. Output timing characteristics VDDIO2 1.2 V range (HSLV OFF)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
01	F_{max}(2)	Maximum frequency	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5	MHz
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	24.5	ns
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	22.2	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	20.0	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	17.8	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	15.0	
10	F_{max}(2)	Maximum frequency	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	10	MHz
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	10	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	10	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	10	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	10	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	16.2	ns
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	14.3	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	12.2	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	10.0	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	7.9	
11	F_{max}(2)(4)	Maximum frequency	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	20	MHz
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	23	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	25	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	28	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	30	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	14.0	ns
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	12.0	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	10.0	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	8.0	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	6.0	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation cell enabled.

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Table 60. Output timing characteristics VDDIO2 1.2 V (HSLV ON)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5	MHz
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	32.5	ns
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	30.0	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	27.5	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	25.0	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	22.5	
01	F_{max}(2)	Maximum frequency	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	15.0	MHz
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	17.5	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	20.0	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	22.5	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	25.0	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	14.6	ns
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	12.9	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	11.2	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	9.3	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	7.3	
10	F_{max}(2)(4)	Maximum frequency	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	25	MHz
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	30	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	33	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	44	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	55	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	11.6	ns
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	9.7	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	7.8	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	6.1	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	4.3	

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Table 60. Output timing characteristics VDDIO2 1.2 V (HSLV ON)(1) (continued)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
11	F_{max}(2)(4)	Maximum frequency	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	30	MHz
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	35	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	44	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	55	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	77	
	t_r/t_f(3)(4)	Output high to low level fall time and output low to high level rise time	C =50 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	11.1	ns
			C =40 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	9.2	
			C =30 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	7.2	
			C =20 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	5.4	
			C =10 pF, 1.08 V≤V_{DDIO2}≤1.32 V	-	3.6	

1. Specified by design - Not tested in production.
2. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45% < Duty cycle < 55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation cell enabled.

5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 53: I/O static characteristics*).

Unless otherwise specified, the parameters given in *Table 61* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*.

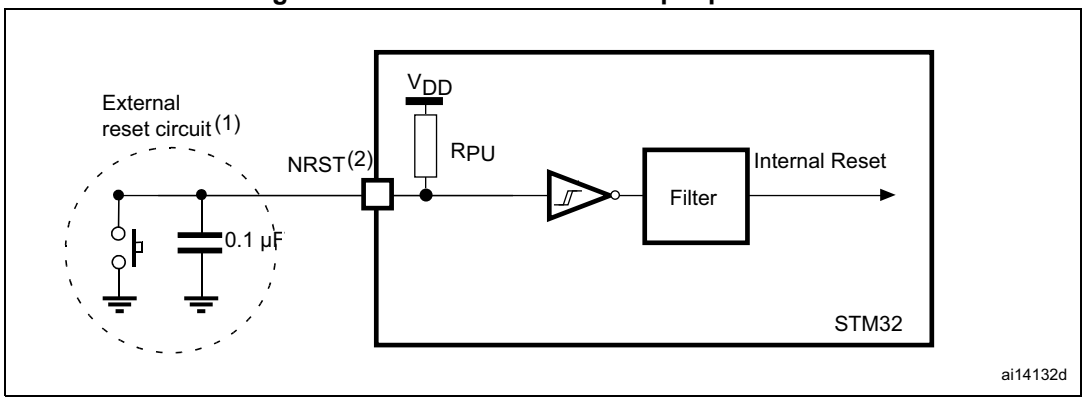
Table 61. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	V_{IN} = V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	1.71 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	1.71 V < V_{DD} < 3.6 V	350	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10 % order).
2. Specified by design - Not tested in production.

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Figure 19. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53*. Otherwise, the reset is not taken into account by the device.

5.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 62. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Specified by design - Not tested in production.

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 63* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 16: General operating conditions*.

Table 63. 12-bit ADC characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.62	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}			
f_{ADC}	ADC clock frequency	1.62 V ≤ V_{DDA} ≤ 3.6 V	1.5	-	37.5	MHz

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Table 63. 12-bit ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions						Min	Typ	Max	Unit
f_s with RAIN=47 Ω and C_{PCB}=22 pF	Sampling rate for direct channels (VIN[0:5])	Resolution = 12 bits	All modes	1.6 V ≤ V_{DDA} ≤ 3.6 V	-40 ≤ T_J ≤ 130 °C	f_{ADC} = 37.5 MHz	SMP = 2.5	-	2.50	-	MSps
		Resolution = 10 bits						-	2.88	-	
		Resolution = 8 bits						-	3.41	-	
		Resolution = 6 bits						-	4.17	-	
	Sampling rate for slow channels	Resolution = 12 bits	All modes	1.6 V ≤ V_{DDA} ≤ 3.6 V	-40 ≤ T_J ≤ 130 °C	f_{ADC} = 30 MHz	SMP = 2.5	-	2.00	-	
		Resolution = 10 bits						-	2.31	-	
		Resolution = 8 bits						-	2.73	-	
		Resolution = 6 bits						-	3.33	-	
t_{TRIG}	External trigger period	Resolution = 12 bits						-	-	15	1/ f_{ADC}
V_{AIN}(3)	Conversion voltage range	-						0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	-						V_{REF}/2 -10%	V_{REF}/2	V_{REF}/2 +10%	V
R_{AIN}(4)	External input impedance	Resolution = 12 bits, T_J = 130 °C (tolerance 4 LSBs						-	-	321	Ω
		Resolution = 12 bits, T_J = 125 °C						-	-	220	
		Resolution = 10 bits, T_J =130 °C						-	-	1039	
		Resolution = 10 bits, T_J = 125 °C						-	-	2100	
		Resolution = 8 bits, T_J =130 °C						-	-	6327	
		Resolution = 8 bits, T_J = 125 °C						-	-	12000	
		Resolution = 6 bits, T_J =130 °C						-	-	47620	
		Resolution = 6 bits, T_J = 125 °C						-	-	80000	
C_{ADC}	Internal sample and hold capacitor	-						-	3	-	pF
$t_{ADCVREG_STUP}$	ADC LDO startup time	-						-	5	-	µs
t_{STAB}	ADC power-up time	LDO already started						1	-	-	Conversion cycle
t_{OFF_CAL}	Offset calibration time	-						1335			1/ f_{ADC}
t_{LATR}	Trigger conversion latency regular and injected channels without conversion abort	CKMODE = 00						1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01						-	-	2.5	
		CKMODE = 10						-	-	2.5	
		CKMODE = 11						-	-	2.25	
$t_{LATRINJ}$	Trigger conversion latency regular injected channels aborting a regular conversion	CKMODE = 00						2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01						-	-	3.5	
		CKMODE = 10						-	-	3.5	
		CKMODE = 11						-	-	3.25	
t_S	Sampling time	-						2.5	-	640.5	$1/f_{ADC}$

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Table 63. 12-bit ADC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CONV}	Total conversion time (including sampling time)	N bits resolution	t_S + 0.5 + N	-	-	$1/f_{ADC}$
$I_{DDA_D(ADC)}$	ADC consumption on V_{DDA} and V_{REF+} Differential mode	f_S = 2.5 MSPS	-	320	-	µA
		f_S = 1 MSPS	-	190	-	
		f_S = 0.1 MSPS	-	50	-	
$I_{DDA_SE(ADC)}$	ADC consumption on V_{DDA} and V_{REF+} Single-ended mode	f_S = 2.5 MSPS	-	240	-	µA
		f_S = 1 MSPS	-	150	-	
		f_S = 0.1 MSPS	-	50	-	
I_{DD} (ADC)	ADC consumption on V_{DD}	f_{ADC}= 37.5 MHz	-	135	-	µA
		f_{ADC}= 30 MHz	-	110	-	
		f_{ADC}= 25 MHz	-	90	-	
		f_{ADC}= 12.5 MHz	-	45	-	
		f_{ADC}= 6.25 MHz	-	22	-	
		f_{ADC}= 3.125 MHz	-	11	-	

1. Evaluated by characterization - Not tested in production.
2. The voltage booster on ADC switches must be used for V_{DDA} < 2.7 V (embedded I/O switches).
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} to V_{SSA}.
4. The tolerance is 2 LSBs, otherwise it is specified.

Table 64. Minimum sampling time versus R_{AIN}(1)(2)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channel	Slow channel(3)
12 bits	47	3.75E-08	6.12E-08
	68	3.94E-08	6.25E-08
	100	4.36E-08	6.51E-08
	150	5.11E-08	7.00E-08
	220	6.54E-08	7.86E-08
	330	8.80E-08	9.57E-08
	470	1.17E-07	1.23E-07
	680	1.60E-07	1.65E-07

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Table 64. Minimum sampling time versus R_{AIN}(1)(2) (continued)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channel	Slow channel(3)
10 bits	47	3.19E-08	5.17E-08
	68	3.35E-08	5.28E-08
	100	3.66E-08	5.45E-08
	150	4.35E-08	5.83E-08
	220	5.43E-08	6.50E-08
	330	7.18E-08	7.89E-08
	470	9.46E-08	1.00E-07
	680	1.28E-07	1.33E-07
	1000	1.81E-07	1.83E-07
	1500	2.63E-07	2.63E-07
	2200	3.79E-07	3.76E-07
	3300	5.57E-07	5.52E-07
8 bits	47	2.64E-08	4.17E-08
	68	2.76E-08	4.24E-08
	100	3.02E-08	4.39E-08
	150	3.51E-08	4.66E-08
	220	4.27E-08	5.13E-08
	330	5.52E-08	6.19E-08
	470	7.17E-08	7.72E-08
	680	9.68E-08	1.00E-07
	1000	1.34E-07	1.37E-07
	1500	1.93E-07	1.94E-07
	2200	2.76E-07	2.74E-07
	3300	4.06E-07	4.01E-07
	4700	5.73E-07	5.62E-07
	6800	8.21E-07	7.99E-07
	10000	1.20E-06	1.17E-06
	15000	1.79E-06	1.74E-06

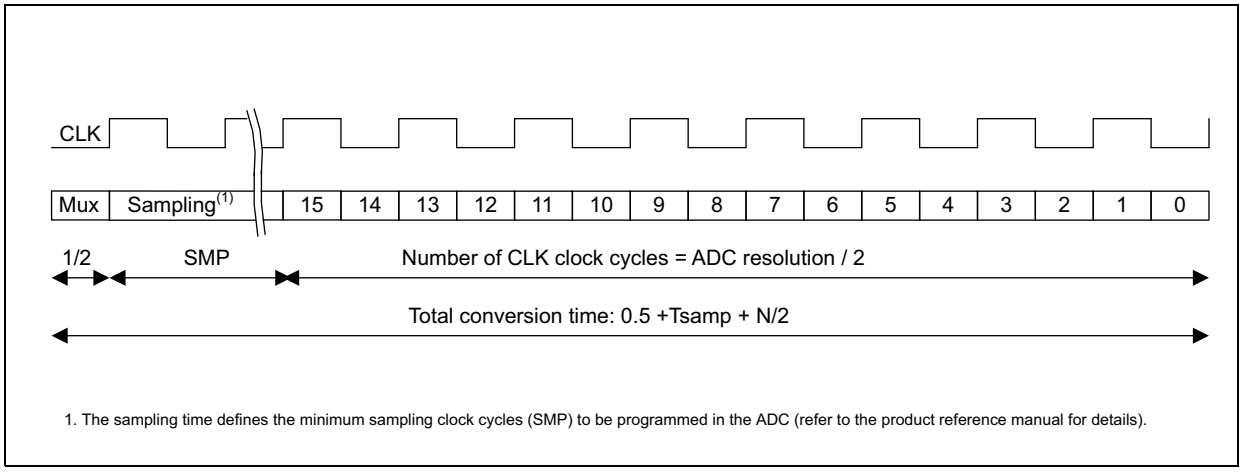
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Table 64. Minimum sampling time versus R_{AIN}(1)(2) (continued)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channel	Slow channel(3)
6 bits	47	2.14E-08	3.16E-08
	68	2.23E-08	3.21E-08
	100	2.40E-08	3.31E-08
	150	2.68E-08	3.52E-08
	220	3.13E-08	3.87E-08
	330	3.89E-08	4.51E-08
	470	4.88E-08	5.39E-08
	680	6.38E-08	6.79E-08
	1000	8.70E-08	8.97E-08
	1500	1.23E-07	1.24E-07
	2200	1.73E-07	1.73E-07
	3300	2.53E-07	2.49E-07
	4700	3.53E-07	3.45E-07
	6800	5.04E-07	4.90E-07
	10000	7.34E-07	7.11E-07
	15000	1.09E-06	1.05E-06

1. Specified by design - Not tested in production.
2. Data valid up to 130 °C, with a 22 pF PCB capacitor, and V_{DDA} = 1.6 V.
3. Slow channels correspond to all ADC inputs except for the fast channels.

Figure 20. ADC conversion timing diagram



1. The sampling time defines the minimum sampling clock cycles (SMP) to be programmed in the ADC (refer to the product reference manual for details).

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Table 65. ADC accuracy(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	Fast and slow channels	Single ended	-	±3.5	±12	LSB
			Differential	-	±2.5	±7.5	
EO	Offset error	-	Single ended	-	±3	±5.5	
		-	Differential	-	±2	±3.5	
EG	Gain error	-	Single ended	-	±3.5	±11	
		-	Differential		±2.5	±7	
ED	Differential linearity error	-	Single ended	-	±0.75	+2/-1	
		-	Differential	-	±0.75	+2/-1	
EL	Integral linearity error	Fast and slow channels	Single ended	-	±2	±6.5	
			Differential	-	±1	±4	
ENOB	Effective number of bits	Single ended		-	10.8	-	Bits
		Differential		-	11.5	-	
SINAD	Signal-to-noise and distortion ratio	Single ended		-	68	-	dB
		Differential		-	71	-	
SNR	Signal-to-noise ratio	Single ended		-	70	-	
		Differential		-	72	-	
THD	Total harmonic distortion	Single ended		-	-70	-	
		Differential		-	-80	-	

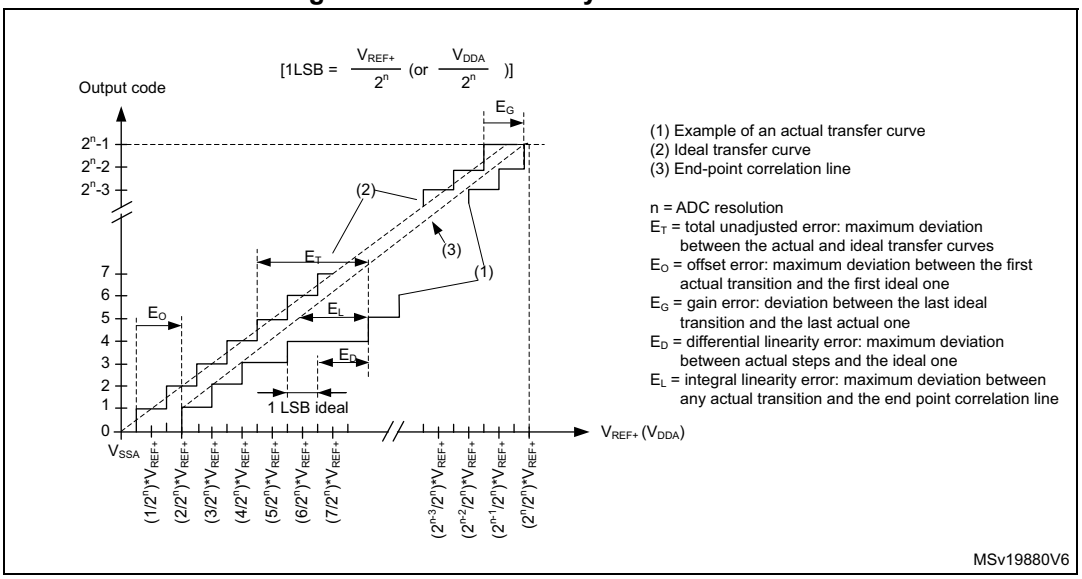
1. Evaluated by characterization - Not tested in production.
2. ADC DC accuracy values are measured after internal calibration in continuous mode.

Note: ADC accuracy versus negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to the ground) to analog pins, which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13: I/O current injection characteristics* does not affect the ADC accuracy.

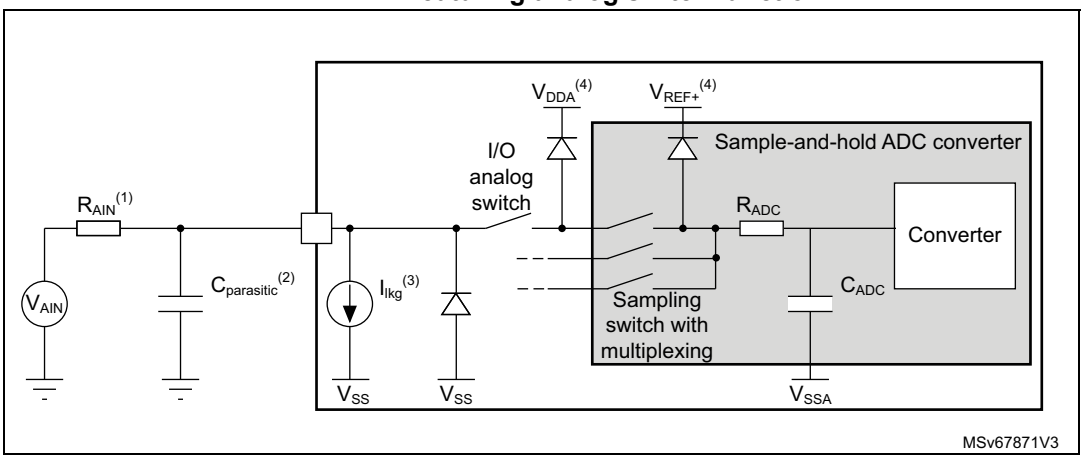
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Figure 21. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
5. EO = Offset error: deviation between the first actual transition and the first ideal one.
6. EG = Gain error: deviation between the last ideal transition and the last actual one.
7. ED = Differential linearity error: maximum deviation between actual steps and the ideal one.
8. EL = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 22. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



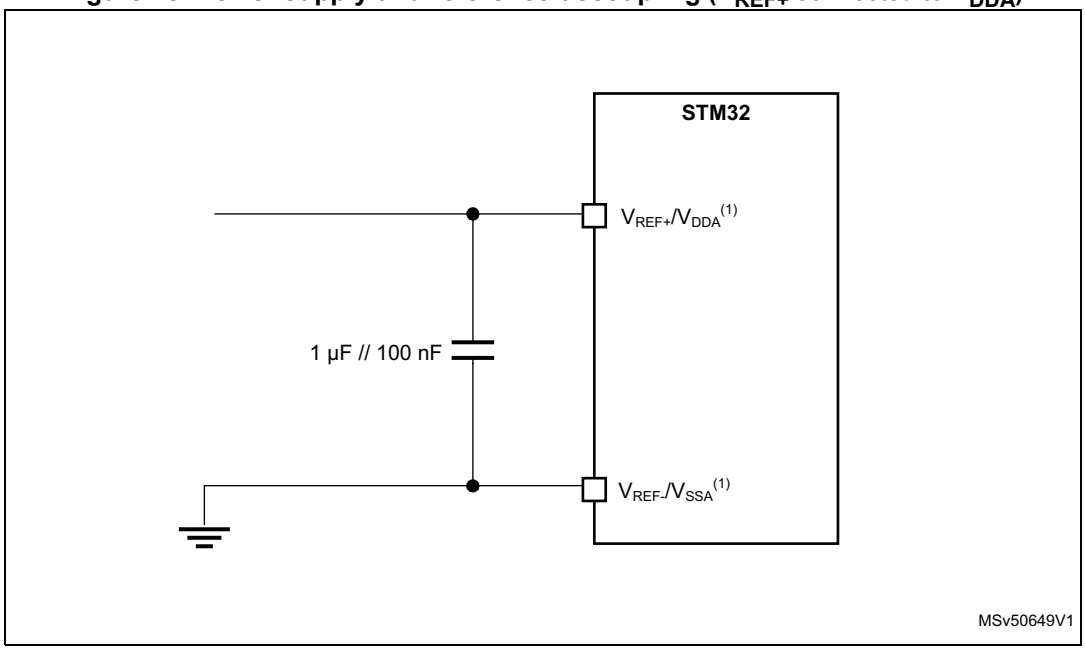
1. Refer to *Table 63: 12-bit ADC characteristics* for the values of R_{AIN}, and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 53: I/O static characteristics*). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 53: I/O static characteristics* for the value of I_{lkg}.
4. Refer to *Figure 11: Power supply scheme*.

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General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 23*. The 100 nF capacitors should be ceramic (good quality). They should be placed as close to the chip as possible.

Figure 23. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is internally connected to V_{DDA} while V_{REF-} is internally connected to V_{SSA} (refer to *Table 2: STM32H503xx features and peripheral counts*).

5.3.18 DAC characteristics

Table 66. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	3.3	3.6	V
V_{REF+}	Positive reference voltage	-		1.80	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	V
R_L	Resistive Load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	kΩ
R_O	Output Impedance	DAC output buffer OFF		10.3	13	16	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	kΩ
			V_{DD} = 2.0 V	-	-	2.6	kΩ
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	kΩ
			V_{DD} = 2.0 V	-	-	18.7	kΩ

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Table 66. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_L	Capacitive Load	DAC output buffer OFF		-	-	50	pF
C_{SH}		Sample and Hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} −0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB)	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ	±0.5 LSB	-	2.05	3	µs
			±1 LSB	-	1.97	2.87	
			±2 LSB	-	1.67	2.84	
			±4 LSB	-	1.66	2.78	
			±8 LSB	-	1.65	2.7	
		Normal mode, DAC output buffer OFF, ±1LSB C_L=10 pF		-	1.7	2	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until the final value of ±1LSB is reached	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, R_L = 5 kΩ		-	5	7.5	µs
		Normal mode, DAC output buffer OFF, $C_L \leq 10$ pF		-	2	5	
PSRR	DC V_{DDA} supply rejection ratio	Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, R_L = 5 kΩ		-	-80	-28	dB
t_{SAMP}	Sampling time in Sample and Hold mode C_L=100 nF (code transition between the lowest input code and the highest input code when DAC_OUT reaches the ±1LSB final value)	MODE<2:0>_V12=100/101 (BUFFER ON)		-	0.7	2.6	ms
		MODE<2:0>_V12=110 (BUFFER OFF)		-	11.5	18.7	
		MODE<2:0>_V12=111(3) (INTERNAL BUFFER OFF)		-	0.3	0.6	µs
I_{leak}	Output leakage current	-		-	-	(4)	nA
C_{lint}	Internal sample and hold capacitor	-		1.8	2.2	2.6	pF
t_{TRIM}	Middle code offset trim time	Minimum time to verify the each code		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	850	-	µV
		V_{REF+} = 1.8 V		-	425	-	

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Table 66. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDA(DAC)}$	DAC quiescent consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	360	-	µA
			No load, worst code (0xF1C)	-	490	-	
		DAC output buffer OFF	No load, middle/ worst code (0x800)	-	20	-	
		Sample and Hold mode, C_{SH}=100 nF		-	$360*T_{ON}/(T_{ON}+T_{OFF})$ (5)	-	
$I_{DDV}(DAC)$	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	170	-	
			No load, worst code (0xF1C)	-	170	-	
		DAC output buffer OFF	No load, middle/ worst code (0x800)	-	160	-	
		Sample and Hold mode, Buffer ON, C_{SH}=100 nF (worst code)		-	$170*T_{ON}/(T_{ON}+T_{OFF})$ (5)	-	
		Sample and Hold mode, Buffer OFF, C_{SH}=100 nF (worst code)		-	$160*T_{ON}/(T_{ON}+T_{OFF})$ (5)	-	

1. Specified by design - Not tested in production, unless otherwise specified.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).
3. DACx_OUT pin is not connected externally (internal connection only).
4. Refer to *Table 53: I/O static characteristics*.
5. T_{ON} is the refresh phase duration, while T_{OFF} is the hold phase duration. Refer to the product reference manual for more details.

Table 67. DAC accuracy(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential non linearity(2)	DAC output buffer ON	−2	-	2	LSB
		DAC output buffer OFF	−2	-	2	
-	Monotonicity	10 bits	-	-	-	-

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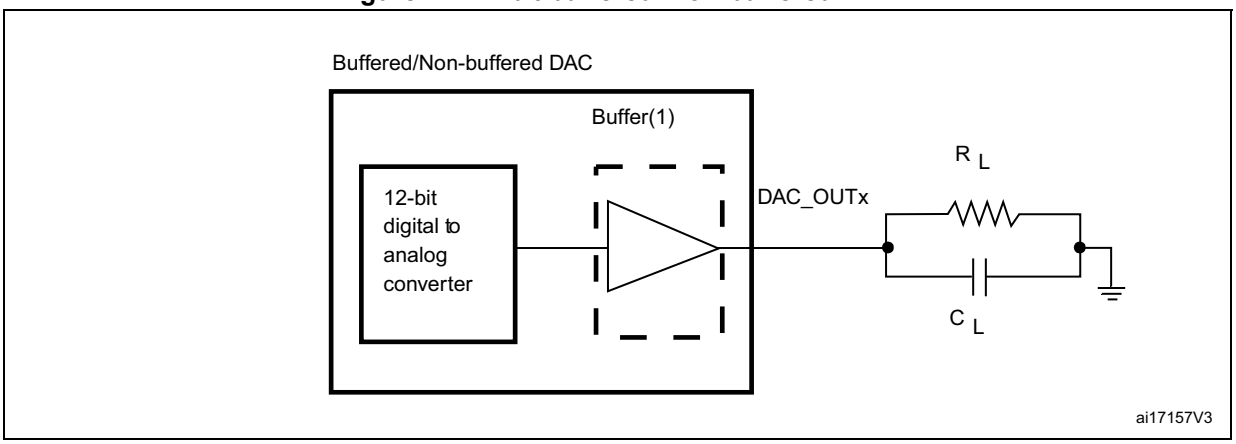
Table 67. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
INL	Integral non linearity(3)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		−4	-	4	LSB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		−4	-	4	
Offset	Offset error at code 0x800 (3)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	V_{REF+} = 3.6 V	-	-	±12	LSB
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±5	LSB
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	V_{REF+} = 3.6 V	-	-	±5	LSB
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON,$C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	-	±1	%
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±1	
TUE	Total unadjusted error	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	-	±30	LSB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L				±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	-	±23	
SNR	Signal-to-noise ratio(6)	DAC output buffer ON,$C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 kHz, BW = 500 KHz		-	67.8	-	dB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L,1 kHz, BW = 500 KHz		-	67.8	-	
THD	Total harmonic distortion(6)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 kHz		-	−78.6	-	dB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L, 1 kHz		-	−78.6	-	
SINAD	Signal-to-noise and distortion ratio(6)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 kHz		-	67.5	-	dB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L, 1 kHz		-	67.5	-	
ENOB	Effective number of bits	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 kHz		-	10.9	-	bits
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L, 1 kHz		-	10.9	-	

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1. Evaluated by characterization - Not tested in production.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2 V) when the buffer is ON.
6. Signal is -0.5 dBFS with $F_{sampling}$=1 MHz.

Figure 24. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.19 Analog temperature sensor characteristics

Table 68. Analog temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature (from V_{SENSOR} voltage)	-	-	3	°C
	V_{SENSE} linearity with temperature (from ADC counter)	-	-	3	
Avg_Slope(2)	Average slope (from V_{SENSOR} voltage)	-	2	-	mV/°C
	Average slope (from ADC counter)	-	2	-	
V_{30}(3)	Voltage at 30°C ± 5 °C	-	0.62	-	V
t_{start_run}	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

1. Specified by design - Not tested in production.
2. Evaluated by characterization - Not tested in production.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

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Table 69. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA}=3.3 V	0x08FF F814 -0x08FF F815
TS_CAL2	Temperature sensor raw data acquired value at 130 °C, V_{DDA}=3.3 V	0x08FF F818 - 0x08FF F819

5.3.20 Digital temperature sensor characteristics

Table 70. Digital temperature sensor characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}(2)	Output Clock frequency	-	500	750	1150	kHz
T_{LC}(2)	Temperature linearity coefficient	VOS2	1660	2100	2750	Hz/°C
T_{TOTAL_ERROR}(2)	Temperature offset measurement, all VOS	T_J = −40°C to 30°C	-13	-	4	°C
		T_J = 30°C to Tjmax	-7	-	2	
T_{VDD_CORE}	Additional error due to supply variation	VOS2	0	-	0	°C
		VOS0, VOS1, VOS3	-1	-	1	
t_{TRIM}	Calibration time	-	-	-	2	ms
t_{WAKE_UP}	Wake-up time from off state until DTS ready bit is set	-	-	67	116.00	µs
I_{DDCORE_DTS}	DTS consumption on VDD_CORE	-	8.5	30	70.0	µA

1. Specified by design - Not tested in production, unless otherwise specified.
2. Evaluated by characterization - Not tested in production.

5.3.21 V_{CORE} monitoring characteristics

Table 71. V_{CORE} monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_{S_VCORE}	ADC sampling time when reading the V_{CORE} voltage	1	-	-	µs

1. Specified by design - Not tested in production.

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5.3.22 Temperature and V_{BAT} monitoring

Table 72. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	4 x 26	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	-10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9	-	-	µs
$V_{BAThigh}$	High supply monitoring	3.5	3.575	3.63	V
V_{BATlow}	Low supply monitoring	-	1.36	-	
$I_{VBATbuf}$	Sensor buffer consumption	-	3.8	6.5	µA

1. Specified by design - Not tested in production.

Table 73. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_BDCR = 0	-	5	-	KΩ
		VBRS in PWR_BDCR = 1		1.5	-	

Table 74. Temperature monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	-	126	-	°C
$TEMP_{low}$	Low temperature monitoring	-	-37	-	

5.3.23 Voltage booster for analog switch

Table 75. Voltage booster for analog switch characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.71	2.6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.71 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

1. Evaluated by characterization - Not tested in production.

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5.3.24 Comparator characteristics

Table 76. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	3.3	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		-			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	0.2	0.3	µA
		BRG_EN=1 (bridge enable)		-	0.8	1	
t_{START_SCALER}	Scaler startup time	-		-	140	250	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode		-	2	5	µs
		Medium mode		-	5	20	
		Ultra-low-power mode		-	15	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode		-	50	80	ns
		Medium mode		-	0.5	0.9	µs
		Ultra-low-power mode		-	2.5	7	
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	High-speed mode		-	50	120	ns
		Medium mode		-	0.5	1.2	µs
		Ultra-low-power mode		-	2.5	7	
V_{offset}	Comparator offset error	Full common mode range		-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		4	10	22	
		Medium hysteresis		8	20	37	
		High hysteresis		16	30	52	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	800	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. Specified by design - Not tested in production, unless otherwise specified.
2. Refer to *Section 5.3.5: Embedded reference voltage*.

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3. Evaluated by characterization - Not tested in production.

5.3.25 Operational amplifier characteristics

Table 77. Operational amplifier characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage Range	-	2	3.3	3.6	V
CMIR	Common Mode Input Range	-	0	-	V_{DDA}	
VI_{OFFSET}	Input offset voltage	25°C, no load on output	-	-	±1.5	mV
		All voltages and temperature, no load	-	-	±2.5	
ΔVI_{OFFSET}	Input offset voltage drift	-	-	±3.0	-	µV/°C
TRIMOFFSETP, TRIMLPOFFSETP	Offset trim step at low common input voltage ($0.1*V_{DDA}$)	-	-	1.1	1.5	mV
TRIMOFFSETN, TRIMLPOFFSETN	Offset trim step at high common input voltage ($0.9*V_{DDA}$)	-	-	1.1	1.5	
I_{LOAD}	Drive current	-	-	-	500	µA
I_{LOAD_PGA}	Drive current in PGA mode	-	-	-	270	
C_{LOAD}	Capacitive load	-	-	-	50	pF
CMRR	Common mode rejection ratio	-	-	80	-	dB
PSRR	Power supply rejection ratio	C_{LOAD} ≤ 50pf / R_{LOAD} ≥ 4 kΩ(2) at 1 kHz, $V_{com}=V_{DDA}/2$	50	66	-	dB
GBW	Gain bandwidth for high supply range	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV	4	7.3	12.3	MHz
SR	Slew rate (from 10% and 90% of output voltage)	Normal mode	-	3	-	V/µs
		High-speed mode	-	24	-	
AO	Open loop gain	200 mV ≤ Output dynamic range ≤ V_{DDA} - 200 mV	59	90	129	dB
φm	Phase margin	-	-	55	-	°
GM	Gain margin	-	-	12	-	dB
V_{OHSAT}	High saturation voltage	I_{load}=max or R_{LOAD}=min, Input at V_{DDA}	V_{DDA} −100 mV	-	-	mV
V_{OLSAT}	Low saturation voltage	I_{load}=max or R_{LOAD}=min, Input at 0 V	-	-	100	

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Table 77. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WAKEUP}	Wake up time from OFF state	Normal mode	C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ, follower configuration	-	0.8	3.2	µs
		High speed mode	C_{LOAD} ≤ 50pf, R_{LOAD} ≥ 4 kΩ, follower configuration	-	0.9	2.8	
PGA gain	Non inverting gain error value	PGA gain = 2		-1	-	1	%
		PGA gain = 4		-2	-	2	
		PGA gain = 8		-2.5	-	2.5	
		PGA gain = 16		-3	-	3	
	Inverting gain error value	PGA gain = 2		-1	-	1	
		PGA gain = 4		-1	-	1	
		PGA gain = 8		-2	-	2	
		PGA gain = 16		-3	-	3	
	External non-inverting gain error value	PGA gain = 2		-1	-	1	
		PGA gain = 4		-3	-	3	
		PGA gain = 8		-3.5	-	3.5	
		PGA gain = 16		-4	-	4	
$R_{network}$	R2/R1 internal resistance values in non-inverting PGA mode(3)	PGA Gain=2		-	10/10	-	kΩ/ kΩ
		PGA Gain=4		-	30/10	-	
		PGA Gain=8		-	70/10	-	
		PGA Gain=16		-	150/10	-	
	R2/R1 internal resistance values in inverting PGA mode(3)	PGA Gain = -1		-	10/10	-	
		PGA Gain = -3		-	30/10	-	
		PGA Gain = -7		-	70/10	-	
		PGA Gain = -15		-	150/10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%

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Table 77. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PGA BW	PGA bandwidth for different non inverting gain	Gain=2		-	GBW/2	-	MHz
		Gain=4		-	GBW/4	-	
		Gain=8		-	GBW/8	-	
		Gain=16		-	GBW/16	-	
	PGA bandwidth for different inverting gain	Gain = -1		-	5.00	-	MHz
		Gain = -3		-	3.00	-	
		Gain = -7		-	1.50	-	
		Gain = -15		-	0.80	-	
en	Voltage noise density	at 1 KHz	output loaded with 4 kΩ	-	140	-	nV/√Hz
		at 10 KHz		-	55	-	
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode, follower	-	570	1000	µA
		High-speed mode		-	610	1200	

1. Specified by design - Not tested in production, unless otherwise specified.
2. R_{LOAD} is the resistive load connected to V_{SSA} or to V_{DDA}.
3. R2 is the internal resistance between the OPAMP output and the OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.

5.3.26 Timer characteristics

The parameters given in *Table 78* are specified by design, not tested in production.

Refer to *Section 5.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 78. TIMx characteristics(1)(2)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 250 MHz	1	-	$t_{TIMxCLK}$
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 125 MHz	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 250 MHz	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$

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1. TIMx is used as a general term to refer to the TIM1 to TIM3 and TIM6/7 timers.
2. Specified by design - Not tested in production.
3. The maximum timer frequency on APB1 or APB2 is up to 250 MHz, by setting the TIMPRE bit in the RCC_CFGR register, if APBx prescaler is 1, 2, or 4, then TIMxCLK = f_{HCLK}, otherwise TIMxCLK = 4x f_{PCLKx} or TIMxCLK = 4x f_{PCLKx}.

5.3.27 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 Kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are specified by design, not tested in production, when the I²C peripheral is properly configured (refer to RM0492 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but still present.
- Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 5.3.14: I/O port characteristics* for the I²C I/Os characteristics

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 79. I²C analog filter characteristics(1)(2)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by analog filter	50(3)	160(4)	ns

1. Evaluated by characterization results - Not tested in production.
2. Measurement points are done at 50 % V_{DD}.
3. Spikes with widths below $t_{AF(min)}$ are filtered.
4. Spikes with widths above $t_{AF(max)}$ are not filtered.

I3C interface characteristics

The I3C interface meets the timings requirements of the MIPI® I3C specification v1.1.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

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The parameters given in *Table 80: I3C open-drain measured timing* and *Table 81: I3C push-pull measured timing* are obtained with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- I/O compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS 0

The I3C timings are in line with the MIPI specification except for the ones given in *Table 80: I3C open-drain measured timing* and *Table 81: I3C push-pull measured timing*. For t_{SU_OD} and t_{SU_PP} this can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register. For t_{SCO} this can be mitigated by enabling and adjusting the clock stall time both on the address ACK phase and on the data read T_{bit} phase in the I3C_TIMINGR2 register. This can also be mitigated by increasing the SCL low duration in the I3C_TIMINGR0 register. For further details, refer to I3C application note AN5879.

Table 80. I3C open-drain measured timing

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements	Unit
			Min	Max		
t_{SU_OD}	SDA data setup time during open drain mode	Controller 1.08 V ≤ V_{DDIO2} (1) ≤ 1.32 V	3	-	23	ns
		Controller 1.71 V ≤ V_{DD} ≤ 3.6 V			16.5	

1. On WLCSP25, the I3C is mapped on port A/B I/Os, which is supplied by VDDIO2 with specification down to 1.08 V. The I3C is tested at this value.

Table 81. I3C push-pull measured timing

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements	Unit
			Min	Max		
t_{SCO}	Clock in to data out for target	Target 1.08 V ≤ V_{DDIO2} (1) ≤ 1.32 V	-	12	18	ns
t_{SU_PP}	SDA signal data setup in push-pull mode	Controller 1.08 V ≤ V_{DDIO2} (1) ≤ 1.32 V	3	-	21	ns
		Controller 1.71 V ≤ V_{DD} ≤ 3.6 V			12	

1. On WLCSP25, the I3C is mapped on port A/B I/Os, which is supplied by VDDIO2 with specification down to 1.08V. The I3C is tested at this value.

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USART interface characteristics

Unless otherwise specified, the parameters given in *Table 82* for USART are derived from tests performed under the ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*, and *Section 5.3.1: General operating conditions* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO compensation cell activated
- VOS level set to VOS0
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 82. USART characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master receiver	-	-	31	MHz
		Slave receiver			83	
		Slave transmitter, 1.71 V < V_{DD} < 3.6 V			32	
		Slave transmitter, 2.7 V < V_{DD} < 3.6 V			35	
		Slave transmitter, 1.08 V < V_{DDIO2} < 1.32 V			22	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker} + 3.5(3)	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2.5	-	-	
$t_{w(CKH)}$, $t_{w(CKL)}$	CK high and low time	Master mode	$1/f_{ck}/2-1$	$1/f_{ck}/2$	$1/f_{ck}/2+1$	
$t_{su(RX)}$	Data input setup time	Master mode	13/22(4)	-	-	
		Slave mode	3.5	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0.5	-	-	
		Slave mode	1.5	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode 1.71 V < V_{DD} < 3.6 V	-	11.5	15.5	ns
		Slave mode 2.7 V < V_{DD} < 3.6 V	-		14	
		Slave mode 1.08 V < V_{DDIO2} < 1.32 V	-	16	22.5	
		Master mode 1.71 V < V_{DD} < 3.6 V	-	2.5	3	
		Master mode 2.7 V < V_{DD} < 3.6 V	-		3	

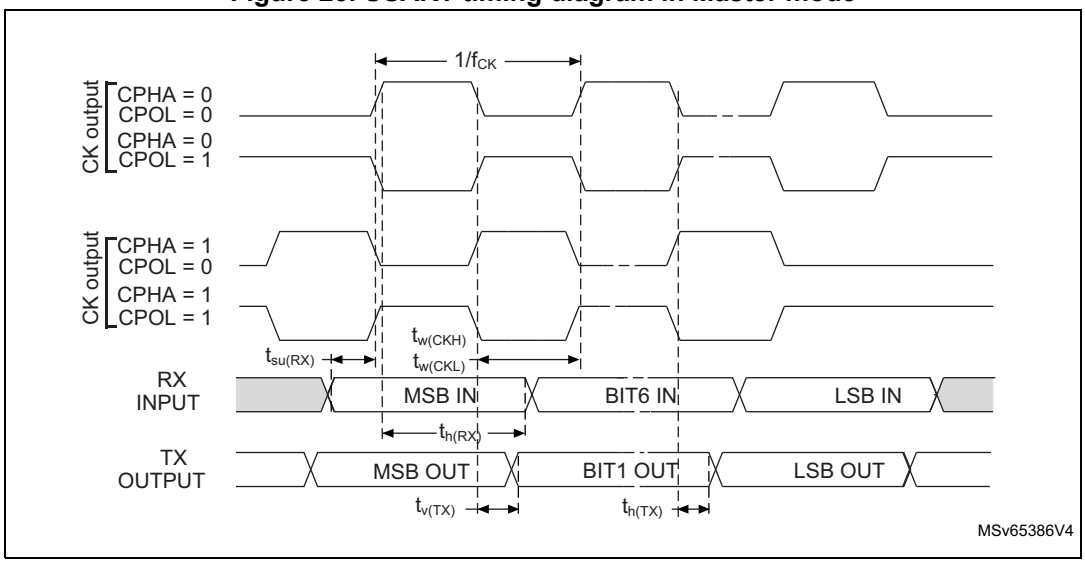
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Table 82. USART characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(TX)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	7.5	-	-	ns
		Slave mode 1.08 V < V_{DDIO2} < 1.32 V	10.5	-	-	
		Master mode	0	-	-	

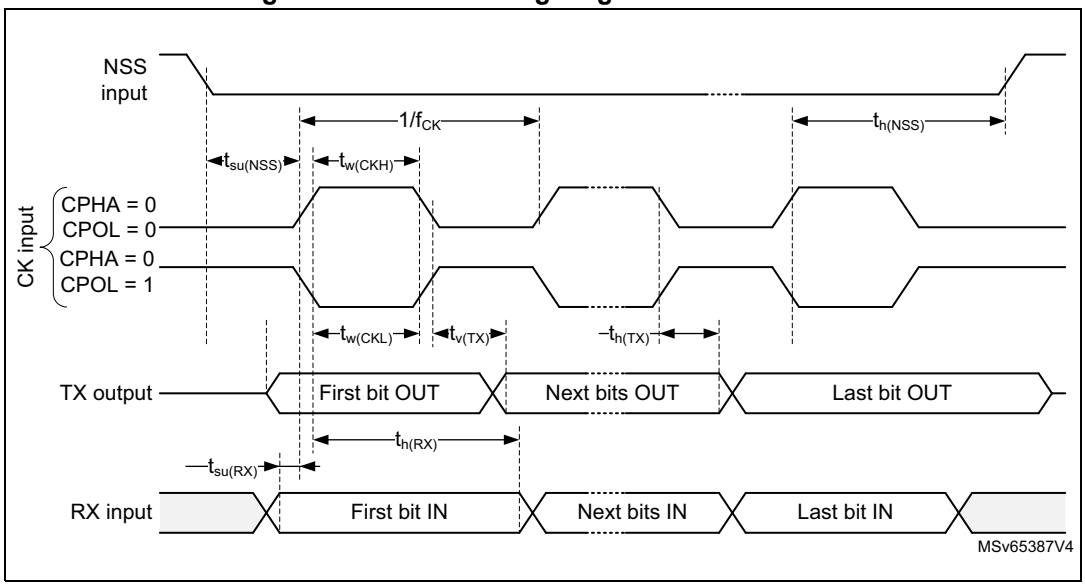
1. Evaluated by characterization - Not tested in production.
2. For VDDIO2 OSPEEDRy[1:0] = 11.
3. t_{ker} is the usart_ker_ck_pres clock period.
4. For V_{DDIO2}.

Figure 25. USART timing diagram in Master mode



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Figure 26. USART timing diagram in Slave mode



SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 83* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions* and *Section 5.3.1: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS0

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

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Table 83. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{SCK}$	SPI clock frequency	Master receiver mode 2.7 V < V_{DD} < 3.6 V	-	-	135	MHz
		Master receiver mode 1.71 V < V_{DD} < 2.7 V	-	-	120	
		Master receiver mode 1.08 V <V_{DDIO2}< 1.32 V	-	-	50	
		Master transmitter mode 2.7 <V_{DD}< 3.6V	-	-	135	
		Master transmitter mode 1.71 V < V_{DD}< 2.7 V	-	-	120	
		Master transmitter mode 1.08 V < V_{DDIO2} < 1.32 V	-	-	50	
		Slave receiver mode 1.71 V < V_{DD} < 3.6 V	-	-	120	
		Slave receiver mode 1.08 V < V_{DDIO2} < 1.32 V	-	-	120	
		Slave transmitter 2.7 V < V_{DD} < 3.6V	-	-	43	
		Slave transmitter 1.71V < V_{DD} < 2.7 V	-	-	41	
		Slave transmitter 1.08 V <V_{DDIO2}<1.32 V	-	-	23	
$t_{su(NSS)}$	NSS setup time	Slave mode	3.5	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	4.5	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	(t_{SCK}/2) - 1	(t_{SCK}/2)	(t_{SCK}/2) + 1	

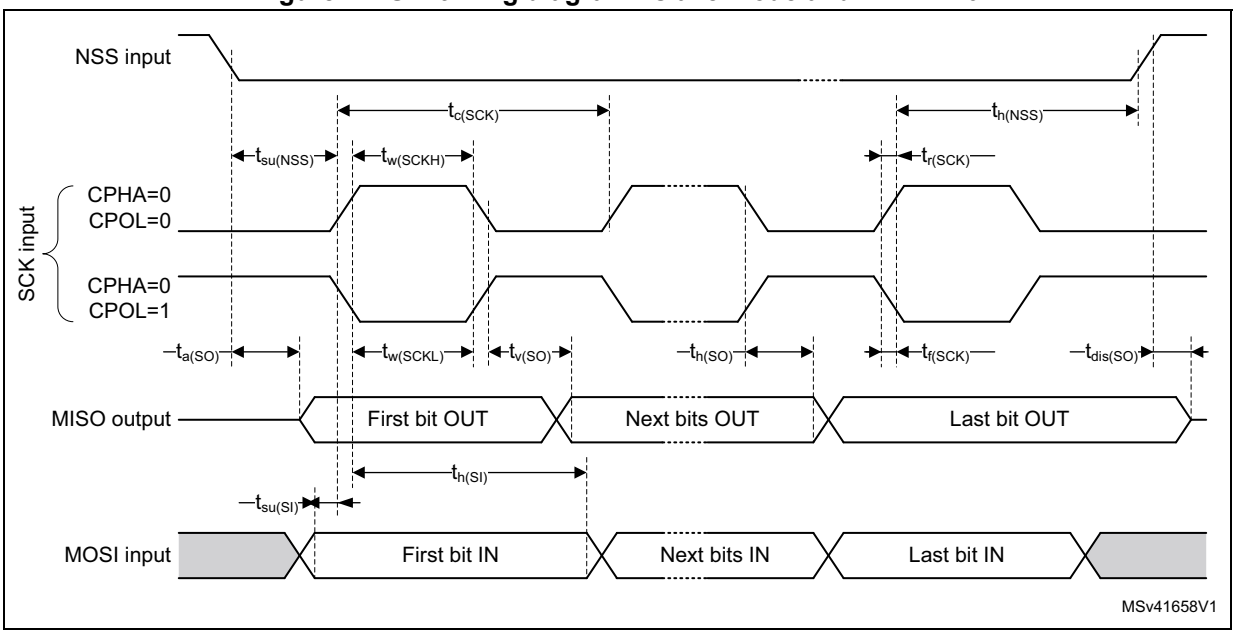
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Table 83. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(MI)}$	Data input setup time	Master mode	3.5	-	-	ns
$t_{su(SI)}$		Slave mode	2	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	1	-	-	
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	6.5	-	15	
$t_{dis(SO)}$	Data output disable time	Slave mode	7.5	-	18	
$t_{v(SO)}$	Data output valid time	Slave mode, $2.7\ V \le V_{DD} \le 3.6\ V$	-	8.5	11.5	
		Slave mode, $1.71\ V \le V_{DD} \le 2.7\ V$	-	10	12	
		Slave mode, $1.08\ V \le V_{DDIO2} \le 1.32\ V$	-	18	21.5	
$t_{v(MO)}$		Master mode	-	1.5	2	
$t_{h(SO)}$	Data output hold time	Slave mode, $1.71\ V \le V_{DD} \le 3.6\ V$	6.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

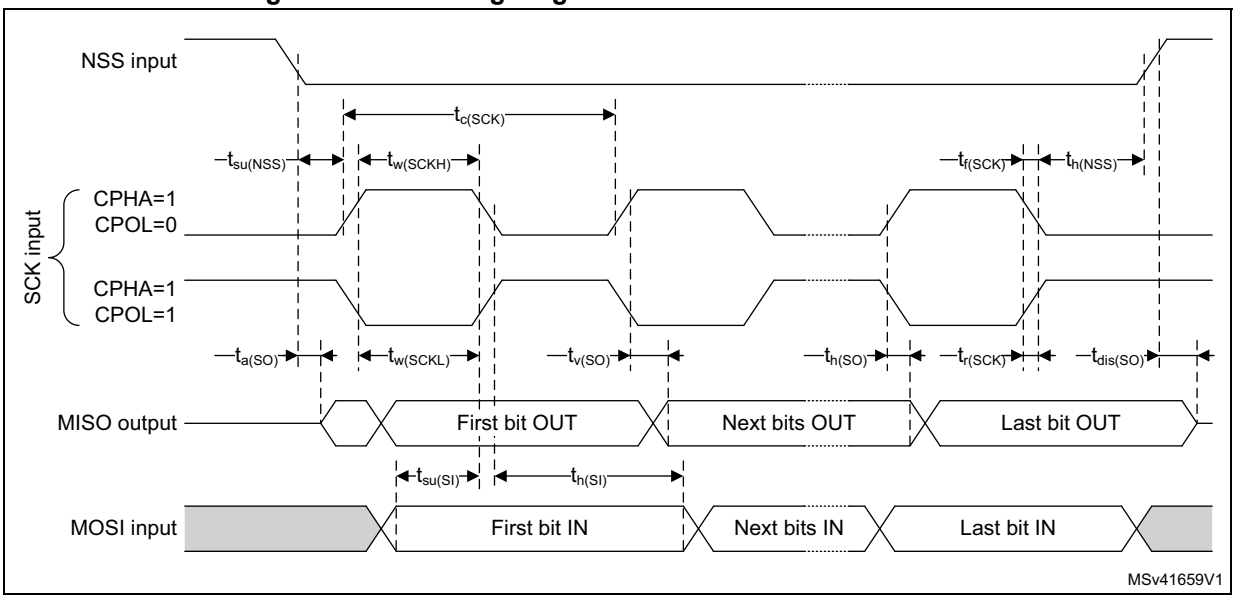
1. Evaluated by characterization - Not tested in production.

Figure 27. SPI timing diagram - slave mode and CPHA = 0



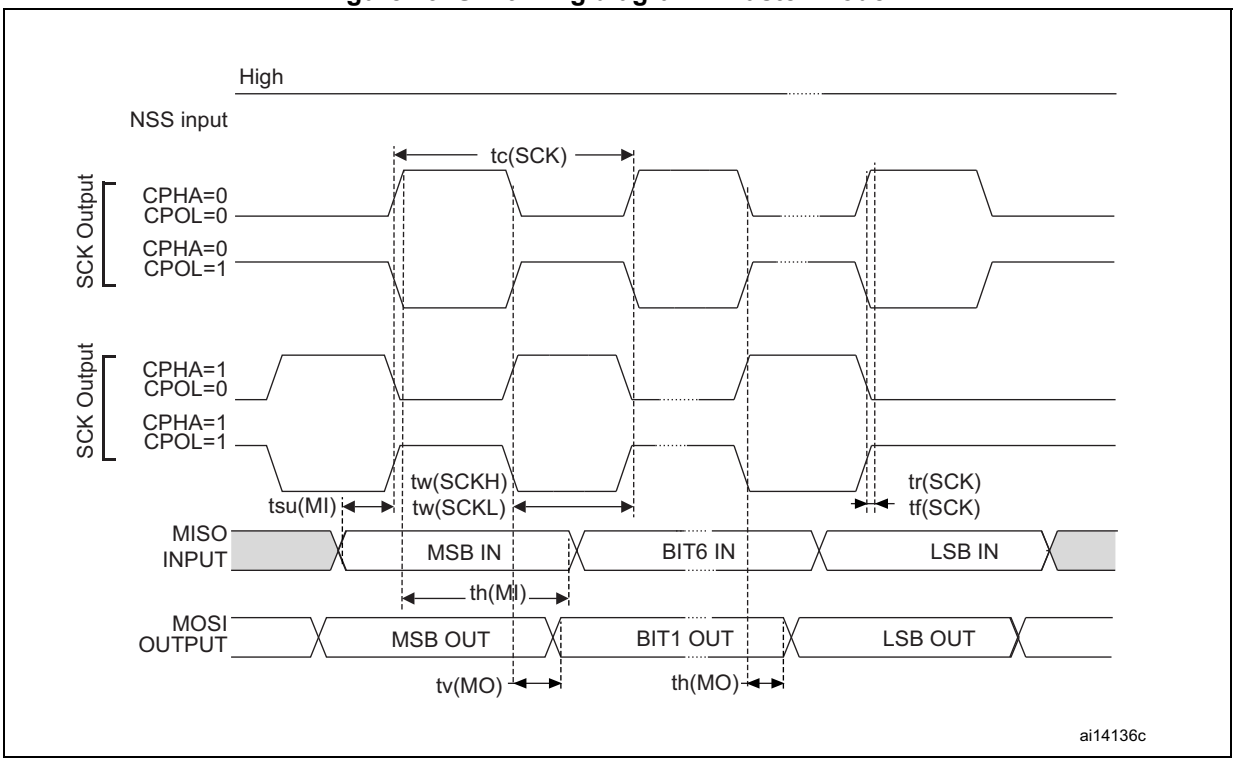
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Figure 28. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 29. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

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I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 84* for I2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS0

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD0,SDI, WS).

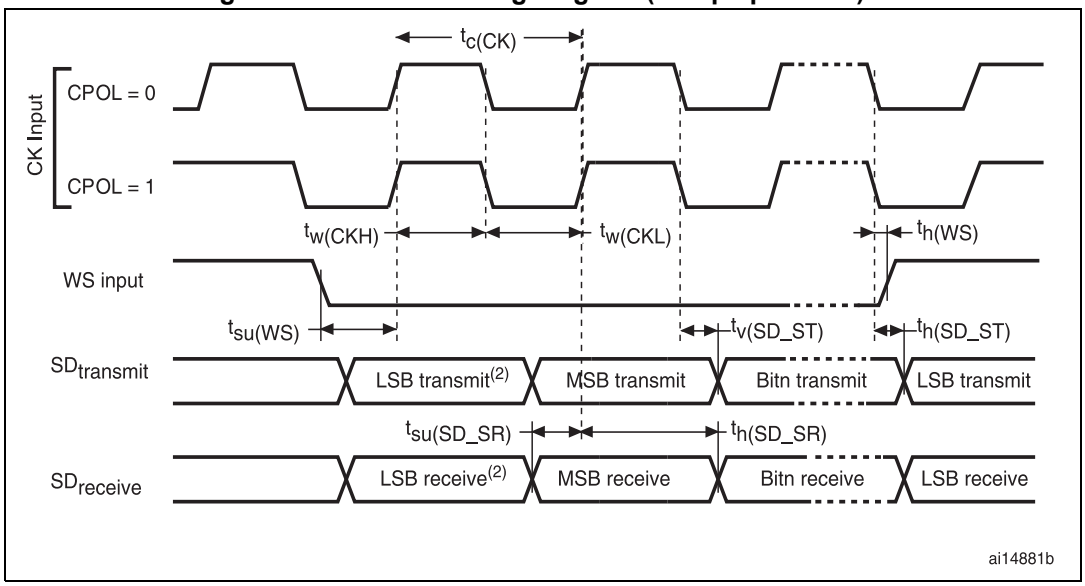
Table 84. I²S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I²S main clock output	-	-	50	MHz
f_{CK}	I²S clock frequency	Master	-	50	
		Slave TX	-	21	
		Slave RX	-	50	
$t_{v(WS)}$	WS valid time	Master mode	-	2	ns
$t_{h(WS)}$	WS hold time		0.5	-	
$t_{su(WS)}$	WS setup time	Slave mode	3	-	
$t_{h(WS)}$	WS hold time		1.5	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	4	-	
$t_{su(SD_SR)}$		Slave receiver	2	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	1	-	
$t_{h(SD_SR)}$		Slave receiver	1.5	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	14	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	1	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5.5	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	

1. Evaluated by characterization. - Not tested in production.

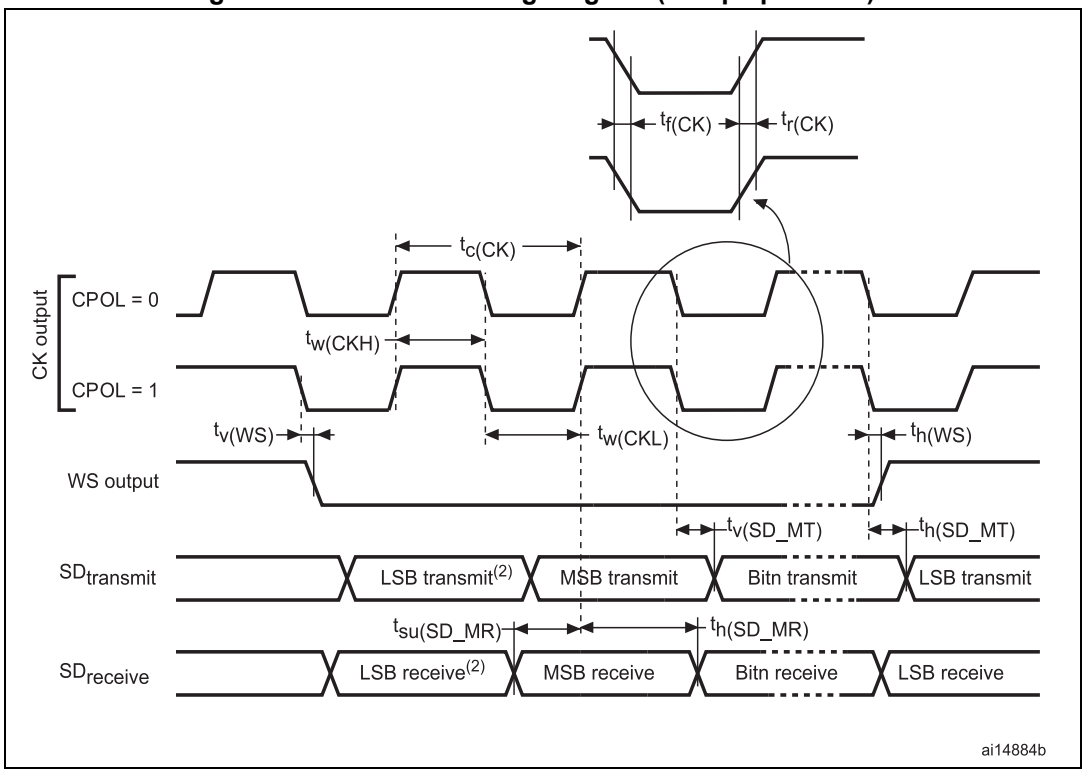
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Figure 30. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 31. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

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USB full speed (FS) characteristics

The USB interface is fully compliant with the USB specification version 2.0.

Table 85. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	USB full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
V_{DI}(3)	Differential input sensitivity	Over VCM range	0.2	-	-	V
V_{CM}(3)	Differential input common mode range	Includes V_{DI} range	0.8	-	2.5	
V_{SE}(3)	Single ended receiver input threshold	-	0.8	-	2.0	
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}(3)	Pull down resistor on PA11, PA12 (USB_DP/DM)	V_{IN} = V_{DD}	14.25	-	24.8	kΩ
R_{PU}(3)	Pull Up Resistor on PA12 (USB_DP)	V_{IN} = V_{SS}, during idle	0.9	1.25	1.575	kΩ
	Pull Up Resistor on PA12 (USB_DP)	V_{IN} = V_{SS} during reception	1.425	2.25	3.09	kΩ

1. All the voltages are measured from the local ground potential.
2. The USB full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics, which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Specified by design - Not tested in production.
4. R_L is the load connected on the USB full speed drivers.

Figure 32. USB timings - definition of data signal rise and fall time

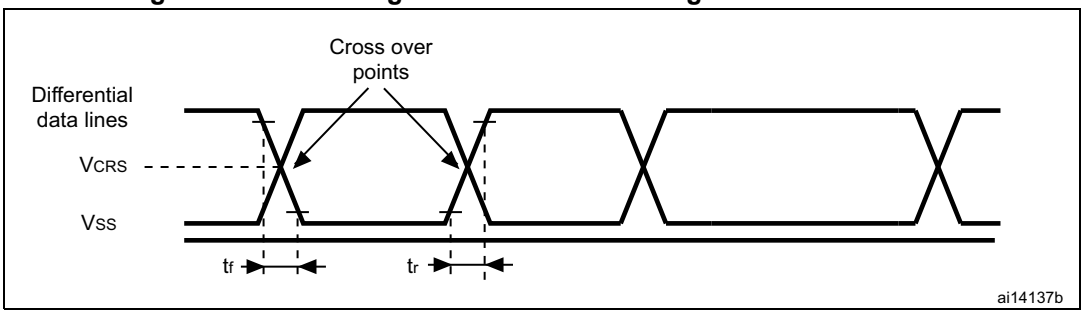


Table 86. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Specified by design - Not tested in production.

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Table 87. USB electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rLS}	Rise time in LS(2)	C_L = 200 to 600 pF	75	300	ns
t_{fLS}	Fall time in LS(2)	C_L = 200 to 600 pF	75	300	ns
t_{rfmLS}	Rise/ fall time matching in LS	t_r/t_f	80	125	%
t_{rFS}	Rise time in FS(2)	C_L = 50 pF	4	20	ns
t_{fFS}	Fall time in FS(2)	C_L = 50 pF	4	20	ns
t_{rfmFS}	Rise/ fall time matching in FS	t_r/t_f	90	111	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

1. Specified by design - Not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed information, refer to USB specification - chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 88. USB BCD DC electrical characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	-	-	300	µA
	Secondary detection mode consumption	-	-	-	300	µA
RDAT_LKG	Data line leakage resistance	-	300	-	-	kΩ
VDAT_LKG	Data line leakage voltage	-	0.0	-	3.6	V
RDCP_DAT	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
VLGC_HI	Logic high	-	2.0	-	3.6	V
VLGC_LOW	Logic low	-	-	-	0.8	V
VLGC	Logic threshold	-	0.8	-	2.0	V
VDAT_REF	Data detect voltage	-	0.25	-	0.4	V
VDP_SRC	D+ source voltage	-	0.5	-	0.7	V
VDM_SRC	D- source voltage	-	0.5	-	0.7	V
IDP_SINK	D+ sink current	-	25	-	175	µA
IDM_SINK	D- sink current	-	25	-	175	µA

1. Specified by design - Not tested in production.

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JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 89* and *Table 90* for JTAG/SWD are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage summarized in *Table 16: General operating conditions* and *Section 5.3.1: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load CL=30 pF
- Measurement points are done at CMOS levels: 0.5VDD
- VOS level set to VOS0

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output characteristics:

Table 89. Dynamic JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{pp}	T_{CK} clock frequency	2.7 V < V_{DD} < 3.6 V	-	-	50	MHz
$1/t_{c(TCK)}$		1.71 V < V_{DD} < 3.6 V	-	-	45	
$t_{isu(TMS)}$	TMS input setup time	-	2	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	1.5	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	1.5	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	1.5	-	-	
$t_{ov(TDO)}$	TDO output valid time	2.7 V < V_{DD} < 3.6 V	-	8	10	
		1.71 V < V_{DD} < 3.6 V	-	8	11	
$t_{oh(TDO)}$	TDO output hold time	-	6.5	-	-	

Table 90. Dynamic SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{pp}	SWCLK clock frequency	2.7 V < V_{DD} < 3.6 V	-	-	80	MHz
$1/t_{c(TCK)}$		1.71 V < V_{DD} < 3.6 V	-	-	71	
$t_{isu(SWDIO)}$	SWDIO input setup time	-	1.5	-	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time	-	1.5	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	2.7 V < V_{DD} < 3.6 V	-	10.5	12.5	
		1.71 V < V_{DD} < 3.6 V	-	10.5	14	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8.5	-	-	

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Figure 33. JTAG timing diagram

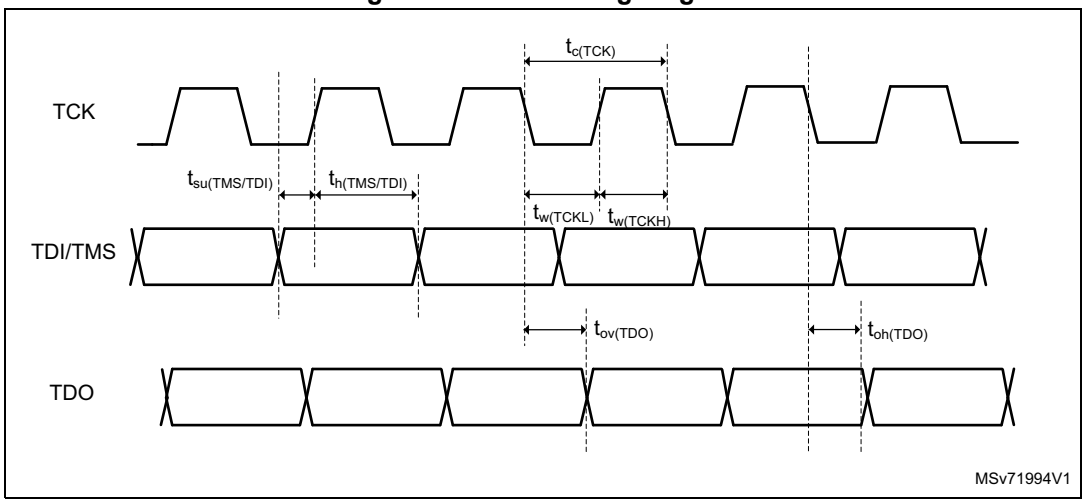
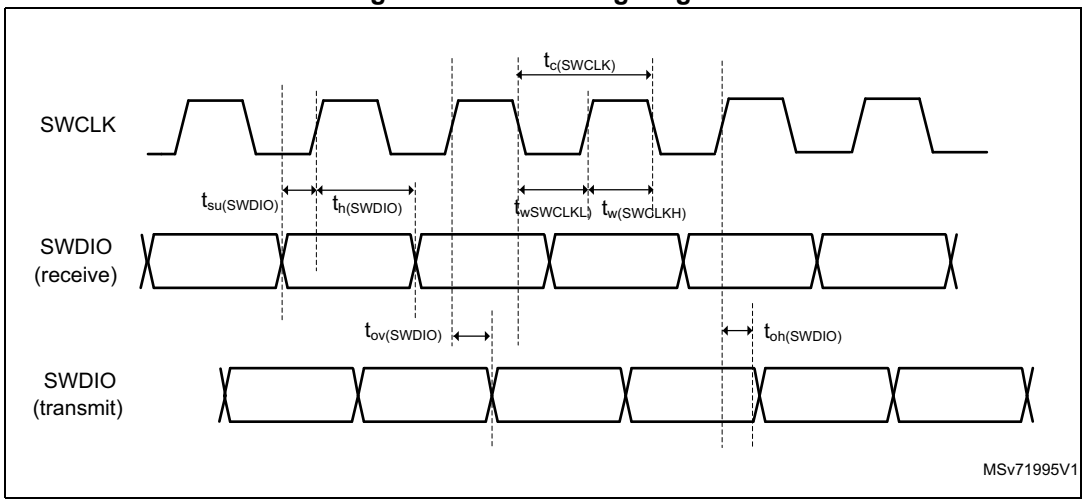


Figure 34. SWD timing diagram



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6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 Device marking

Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

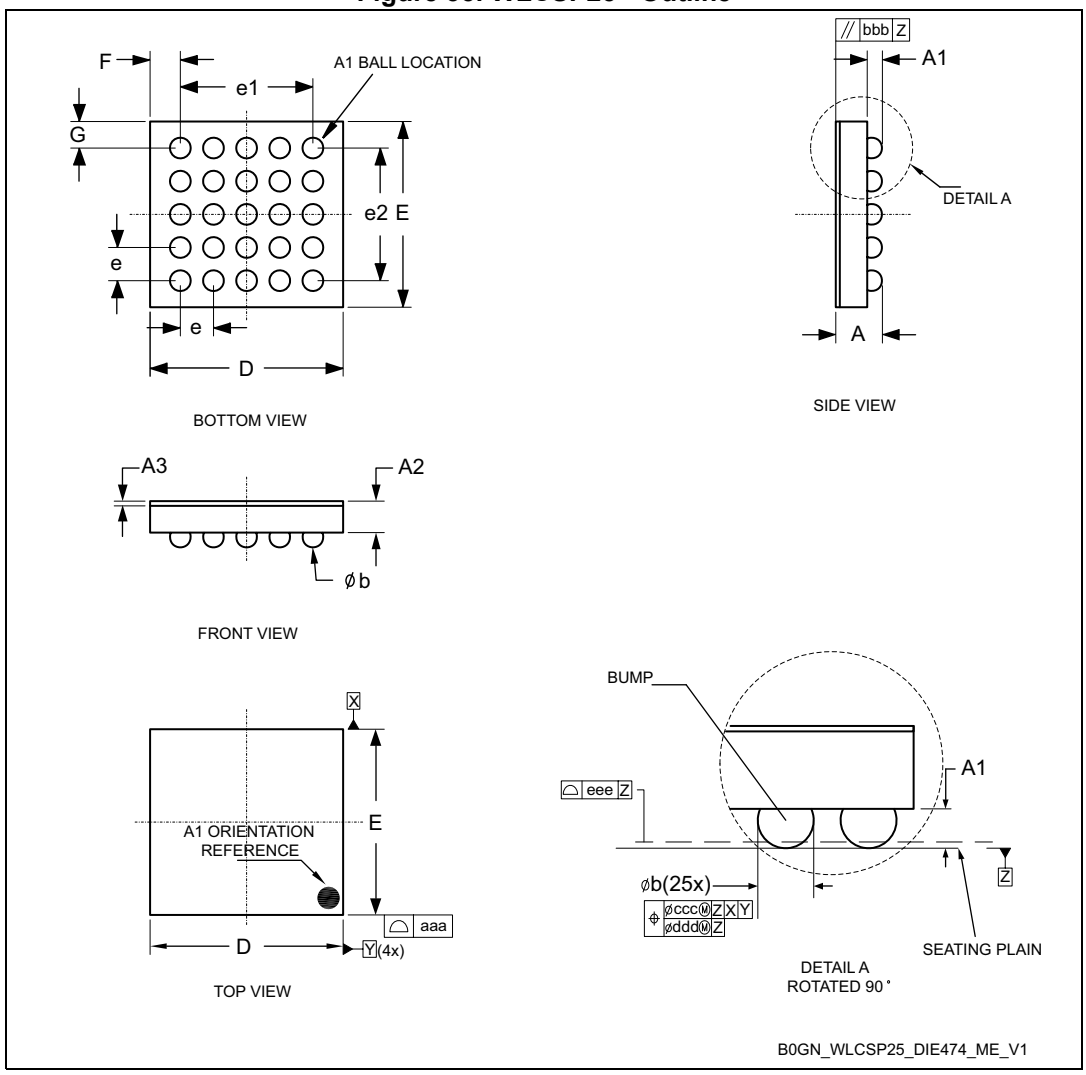
A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

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6.2 WLCSP25 package information (B0GN)

This WLCSP is a 25 ball, 2.33 x 2.24 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 35. WLCSP25 - Outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.

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Table 91. WLCSP25 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.58	-	-	0.0228
A1	-	0.17	-	-	0.0067	-
A2	-	0.38	-	-	0.0149	-
A3[3]	-	0.025	-	-	0.0010	-
b[4]	0.23	0.26	0.28	0.0090	0.0102	0.0110
D	2.31	2.33	2.35	0.0909	0.0917	0.0925
E	2.22	2.24	2.26	0.0874	0.0882	0.0890
e	-	0.40	-	-	0.0157	-
e1	-	1.60	-	-	0.0630	-
e2	-	1.60	-	-	0.0630	-
F[5]	-	0.365	-	-	0.0144	-
G[5]	-	0.320	-	-	0.0126	-
aaa	-	-	0.10	-	-	0.0039
bbb	-	-	0.10	-	-	0.0039
ccc[6]	-	-	0.10	-	-	0.0039
ddd[7]	-	-	0.05	-	-	0.0020
eee	-	-	0.05	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Back side coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
5. Calculated dimensions are rounded to the 3rd decimal place
6. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.
7. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
   The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone ddd perpendicular to datum Z and located on true position as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone. Each tolerance zone ddd in the array is contained entirely in the respective zone ccc above. The axis of each ball must lie simultaneously in both tolerance zones.

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Figure 36. WLCSP25 - Footprint example

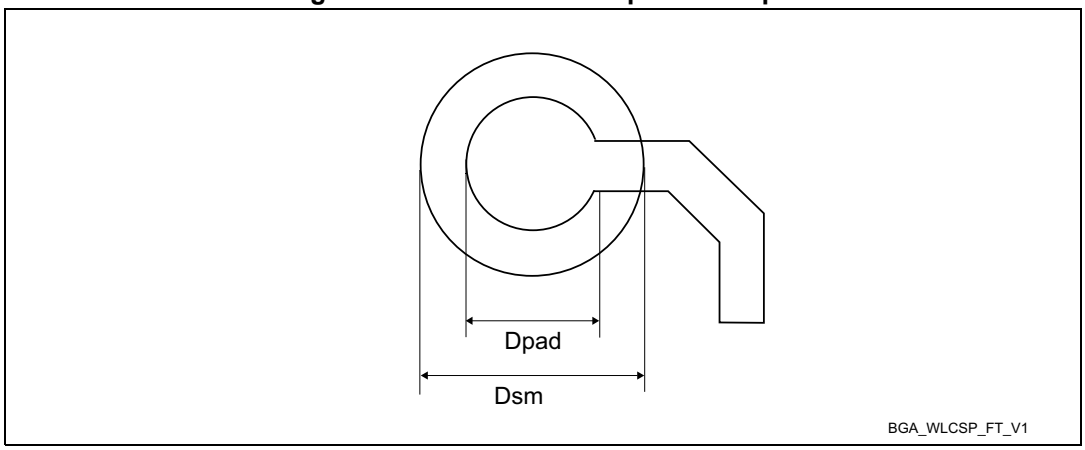
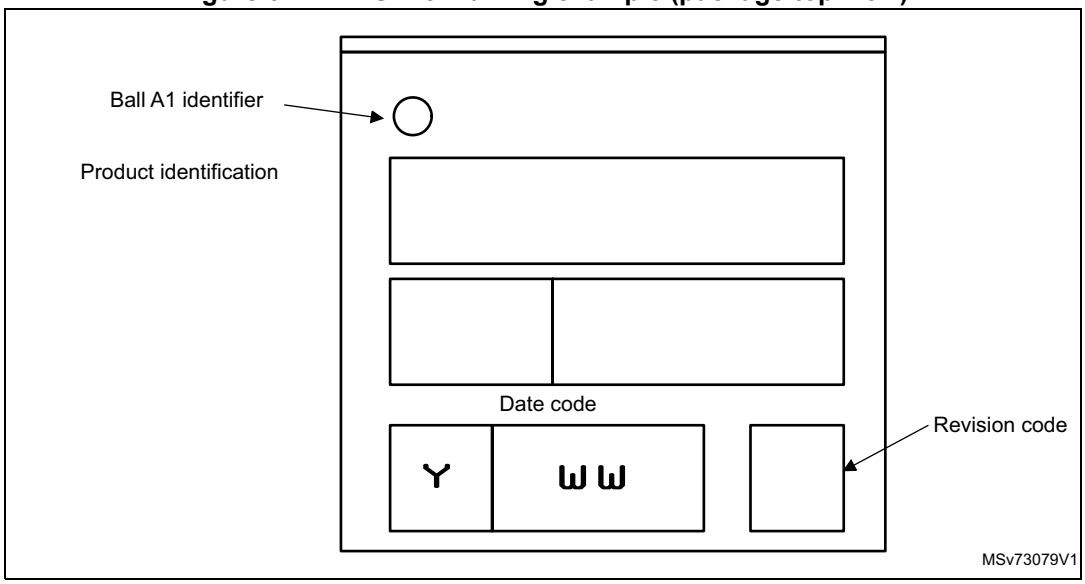


Table 92. WLCSP25 - Example of PCB design rules

Dimension	Values
Pitch	0.4 mm
Dpad	0,225 mm
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Figure 37. WLCSP25 marking example (package top view)

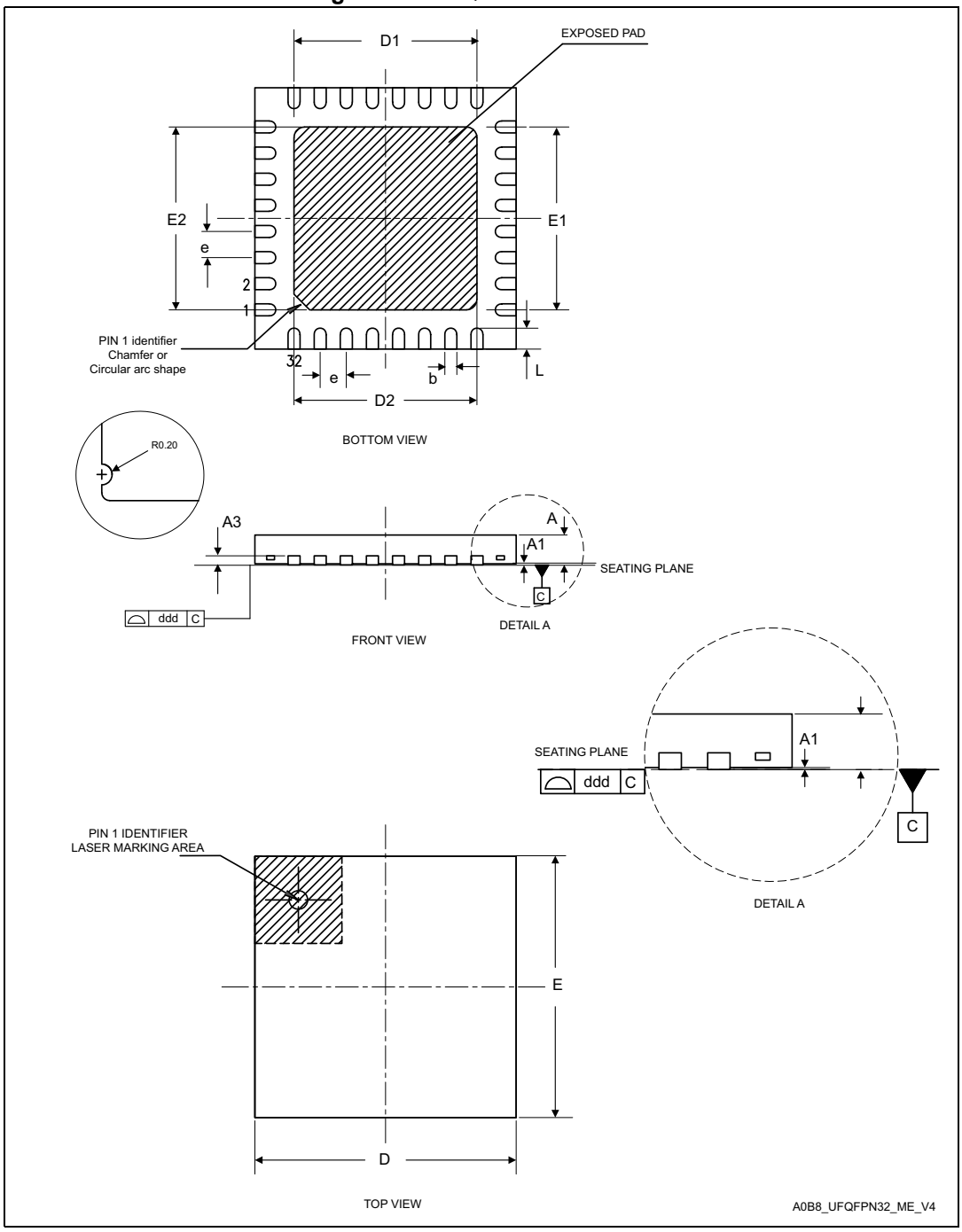


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6.3 UFQFPN32 package information (A0B8)

This UFQFPN is a 32 pins, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package

Figure 38. UFQFPN32 - Outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This backside pad must be connected and soldered to PCB ground.

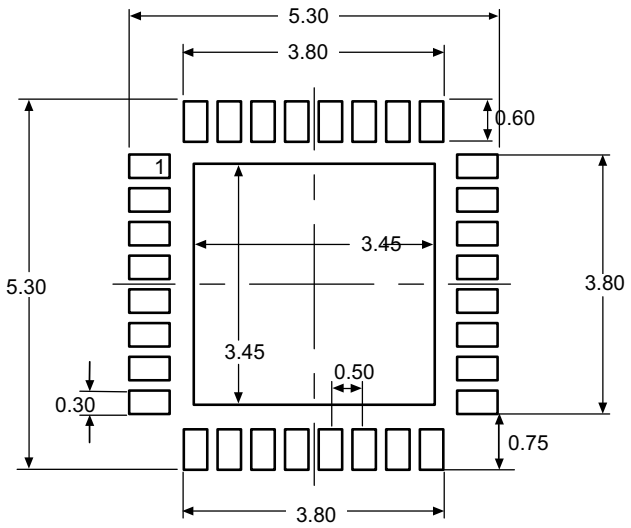
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Table 93. UFQFPN32 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.000	0.0007	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	-	0.300	0.0071	-	0.0118
D[2]	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E[2]	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D and E do not include mold protrusion, not to exceed 0,15mm.

Figure 39. UFQFPN32 - Footprint example



1. Dimensions are expressed in millimeters.

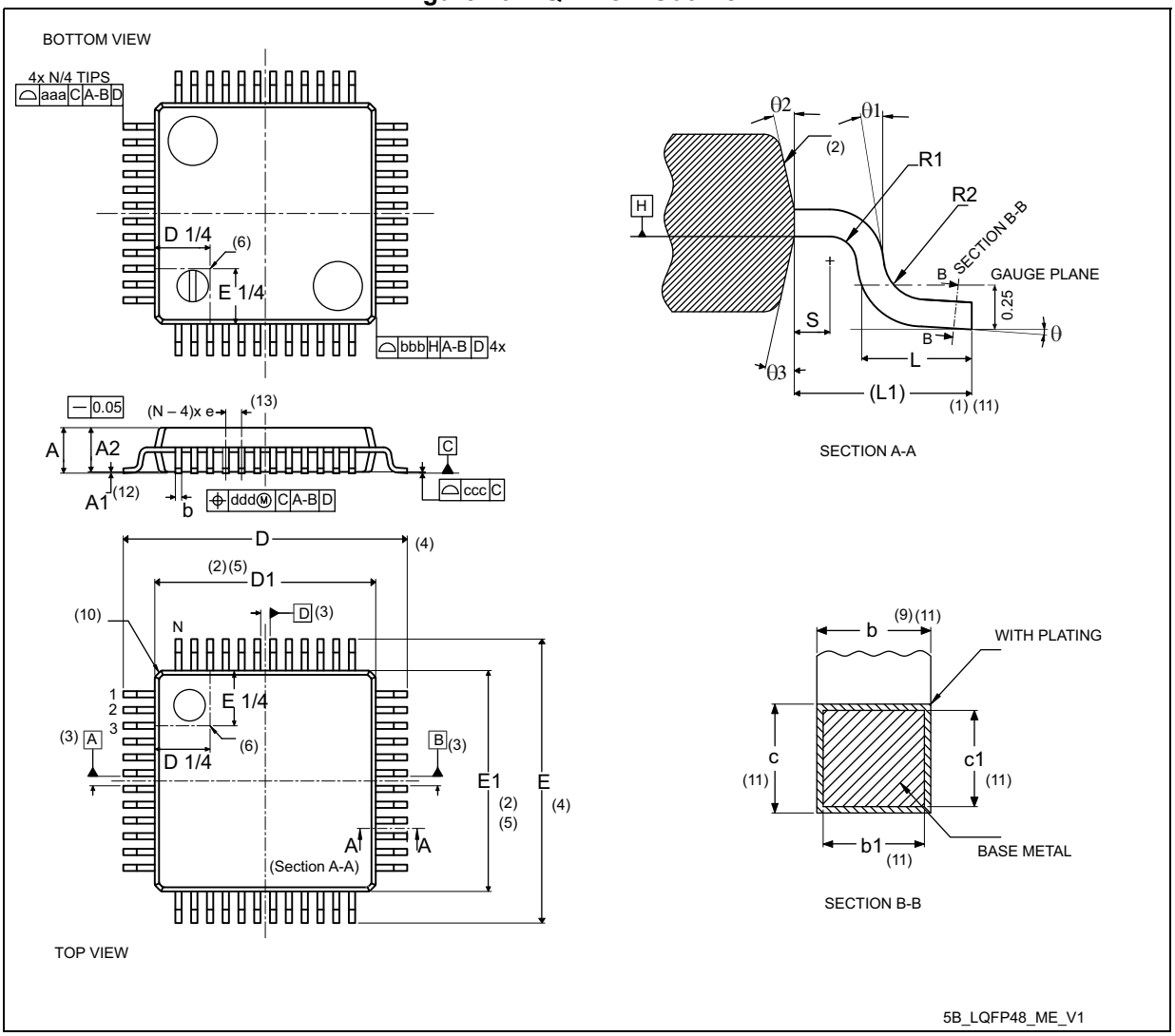
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6.4 LQFP48 package information (5B)

This LQFP is a 48-pin, 7 x 7 mm low-profile quad flat package

Note: See list of notes in the notes section.

Figure 40. LQFP48 – Outline(15)



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Table 94. LQFP48 – Mechanical data

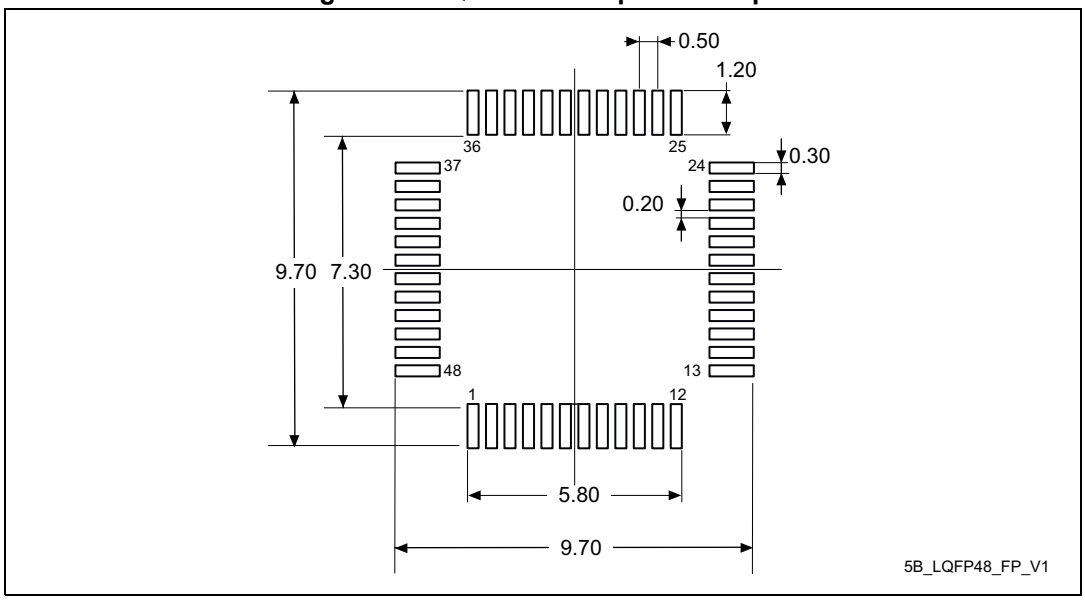
Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	9.00 BSC			0.3543 BSC		
D1[2][5]	7.00 BSC			0.2756 BSC		
E[4]	9.00 BSC			0.3543 BSC		
E1[2][5]	7.00 BSC			0.2756 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	48					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1][7]	0.20			0.0079		
bbb[1][7]	0.20			0.0079		
ccc[1][7]	0.08			0.0031		
ddd[1][7]	0.08			0.0031		

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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 41. LQFP48 – Footprint example



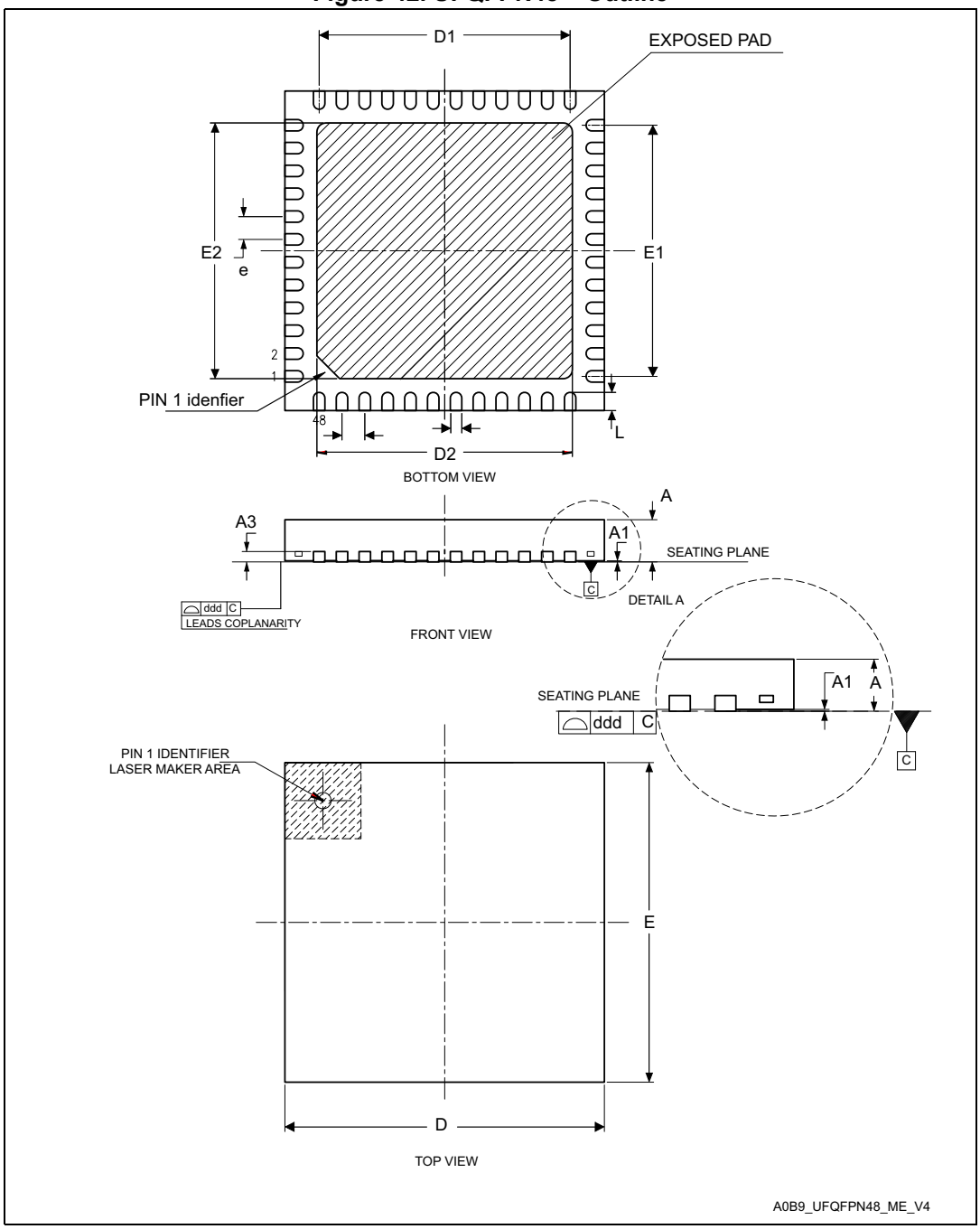
1. Dimensions are expressed in millimeters.

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6.5 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 42. UFQFPN48 – Outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.

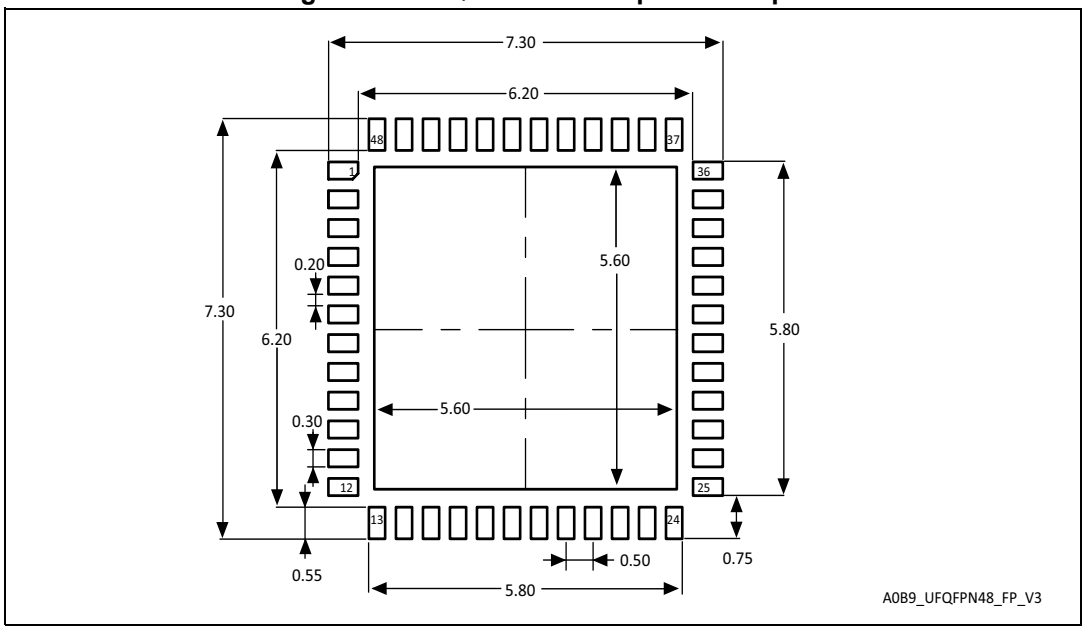
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Table 95. UFQFPN48 – Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D[2]	6.900	7.000	7.100	0.2717	0.2756	0.2795
D1	5.400	5.500	5.600	0.2126	0.2165	0.2205
D2[3]	5.500	5.600	5.700	0.2165	0.2205	0.2244
E[2]	6.900	7.000	7.100	0.2717	0.2756	0.2795
E1	5.400	5.500	5.600	0.2126	0.2165	0.2205
E2[3]	5.500	5.600	5.700	0.2165	0.2205	0.2244
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.
3. Dimensions D2 and E2 are not in accordance with JEDEC.

Figure 43. UFQFPN48 – Footprint example



1. Dimensions are expressed in millimeters.

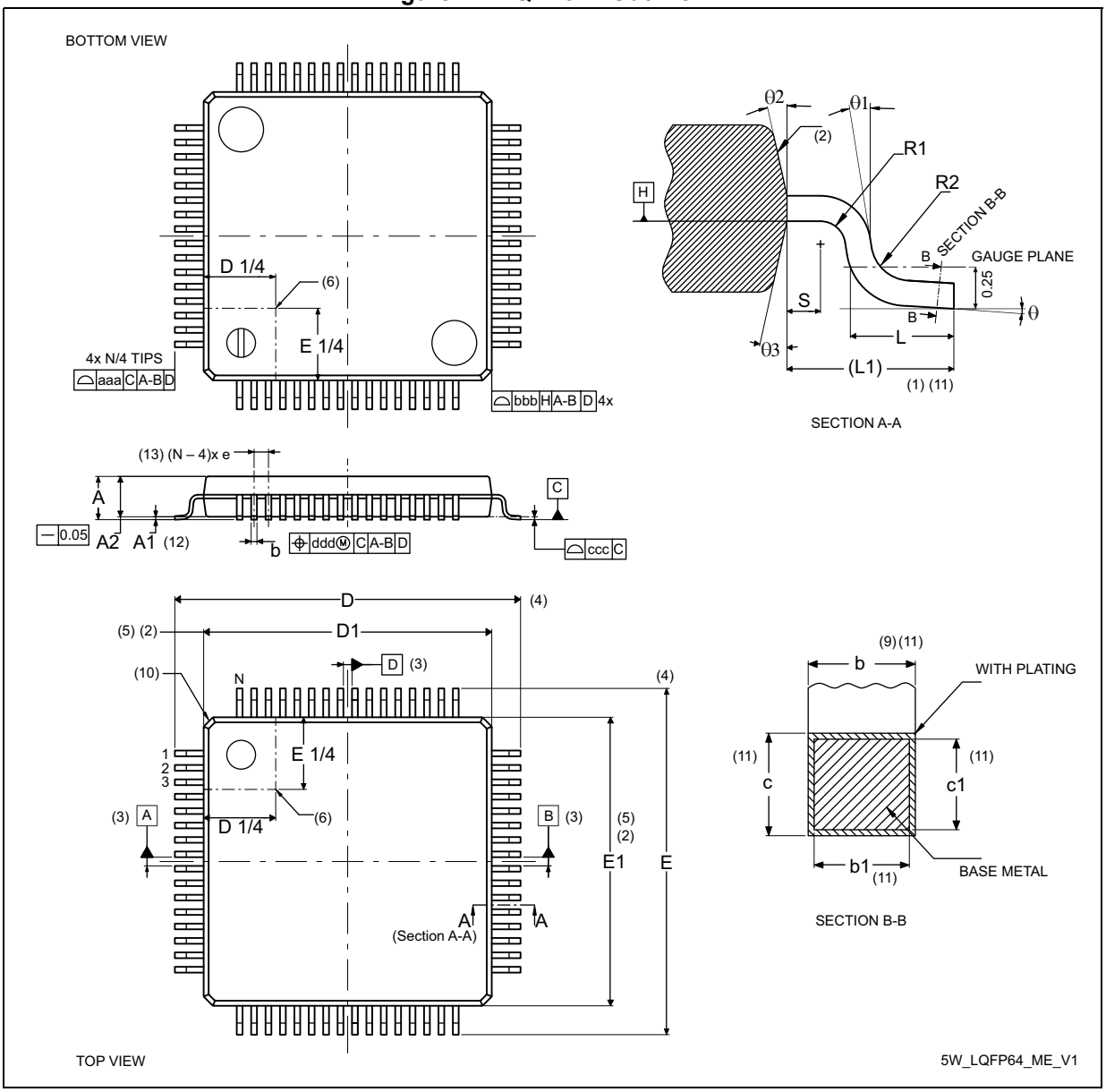
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6.6 LQFP64 package information (5W)

This LQFP is 64-pin, 10 x 10 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 44. LQFP64 - Outline(15)



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Table 96. LQFP64 - Mechanical data

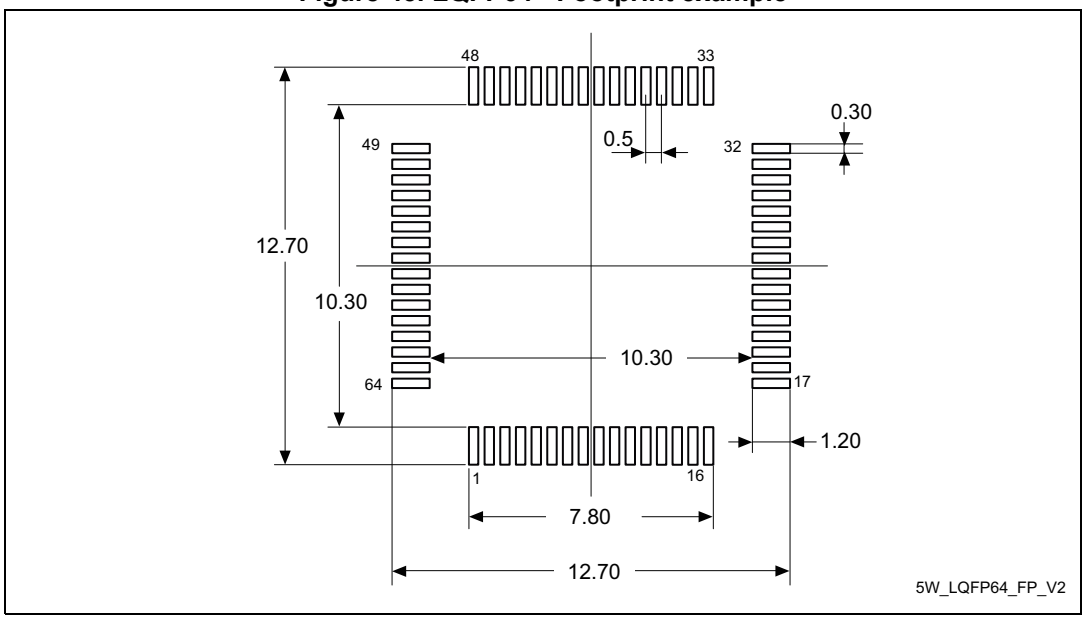
Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	12.00 BSC			0.4724 BSC		
D1[2][5]	10.00 BSC			0.3937 BSC		
E[4]	12.00 BSC			0.4724 BSC		
E1[2][5]	10.00 BSC			0.3937 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	64					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1]	0.20			0.0079		
bbb[1]	0.20			0.0079		
ccc[1]	0.08			0.0031		
ddd[1]	0.08			0.0031		

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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 45. LQFP64 - Footprint example



1. Dimensions are expressed in millimeters.

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6.7 Package thermal characteristics

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_J max = T_A max + (P_D max \times \Theta_{JA})$

Where:

- $T_A max$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D max$ is the sum of $P_{INT} max$ and $P_{I/O} max$ ($P_D max = P_{INT} max + P_{I/O} max$),
- $P_{INT} max$ is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O} max$ represents the maximum power dissipation on output pins where:

- $P_{I/O} max = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$, taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 97. Package thermal characteristics

Symbol	Definition	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	Thermal resistance junction-ambient WLCSP25 - 2.33 x 2.24 mm /0.4 mm pitch	80.7	°C/W
		Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm /0.5 mm pitch	40.1	
		Thermal resistance junction-ambient LQFP48 - 7 x 7 mm /0.5 mm pitch	54.1	
		Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm /0.5 mm pitch	29.5	
		Thermal resistance junction-ambient LQFP64 - 10 x 10 mm /0.5 mm pitch	48.9	
Θ_{JB}	Thermal resistance junction-board	Thermal resistance junction-ambient WLCSP25 - 2.33 x 2.24 mm /0.4 mm pitch	51.9	°C/W
		Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm /0.5 mm pitch	22.1	
		Thermal resistance junction-ambient LQFP48 - 7 x 7 mm /0.5 mm pitch	31.6	
		Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm /0.5 mm pitch	13.9	
		Thermal resistance junction-ambient LQFP64 - 10 x 10 mm /0.5 mm pitch	31.2	

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Table 97. Package thermal characteristics (continued)

Symbol	Definition	Parameter	Value	Unit
Θ_{JC}	Thermal resistance junction-case	Thermal resistance junction-ambient WLCSP25 - 2.33 x 2.24 mm /0.4 mm pitch	5	°C/W
		Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm /0.5 mm pitch	19.4	
		Thermal resistance junction-ambient LQFP48 - 7 x 7 mm /0.5 mm pitch	16.4	
		Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm /0.5 mm pitch	11.3	
		Thermal resistance junction-ambient LQFP64 - 10 x 10 mm /0.5 mm pitch	15.1	

6.7.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.
- For information on thermal management, refer to application note “Thermal management guidelines for STM32 32-bit Arm Cortex MCUs applications” (AN5036) available from *www.st.com*.

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7 Ordering information

Example: STM32 H 503 R B T 6 TR

Device family

STM32 = Arm based 32-bit microcontroller

Product type

H = high performance

Device subfamily

503 = STM32H503xx

Pin count

E = 25 pins
K = 32 pins
C = 48 pins
R = 64 pins

Flash memory size

B = 128 Kbytes

Package

U = UFQFPN
Y = WLCSP
T = LQFP

Temperature range

6 = Temperature range, -40 to 85 °C
7 = Temperature range, -40 to 105 °C, and up to 125 °C at low dissipation

Packing

TR = tape and reel

xxx = programmed parts

For a list of available options (such as speed or package) or for further information on any aspect of this device, contact the nearest ST sales office.

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9 Revision history

Table 98. Document revision history

Date	Revision	Changes
03-Mar-2023	1	Initial release.
28-Aug-2023	2	Updated: – *Section 3.10: Reset and clock controller (RCC)* – *Table 41: CSI oscillator characteristics* – *Figure 18: VIL/VIH for all I/Os except BOOT0* – *Table 54: Output voltage characteristics for all I/Os except PC13, PC14 and PC15* – *Table 58: Output timing characteristics (HSLV ON)* – *Section 6.3: UFQFPN32 package information (A0B8)* – *Section 6.4: LQFP48 package information (5B)* – *Section 6.5: UFQFPN48 package information (A0B9)*
26-Sep-2023	3	Updated: – *Table 2: STM32H503xx features and peripheral counts* – Tables from *Table 23: Typical and maximum current consumption in run mode, code with data processing running from flash memory, 2-ways instruction cache ON, PREFETCH ON* to *Table 26: Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 2-WAY*. – *Table 29: Typical and maximum current consumption in sleep mode* – *Table 30: Typical and maximum current consumption in stop mode* – *Section 5.3.7: External clock source characteristics* – *Section 7: Ordering information* Added: – *Section 6.1: Device marking* – *Figure 37: WLCSP25 marking example (package top view)*

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