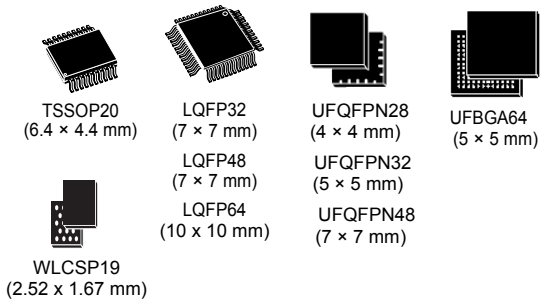
STM32C071x8/xB

Arm®Cortex®-M0+ 32-bit MCU, 128 KB flash, 24 KB RAM, 2 x USART, timers, ADC, USB FS, comm. I/Fs, 2-3.6V

Datasheet - production data

Features

- Includes ST state-of-the-art patented technology
- Core: Arm® 32-bit Cortex®-M0+ CPU, frequency up to 48 MHz
- -40°C to 85°C/105°C/125°C operating temperature
- Memories
  - Up to 128 Kbytes of flash memory with protection and securable area
  - 24 Kbytes of SRAM with hardware parity check
- CRC calculation unit
- Reset and power management
  - Voltage range: 2.0 V to 3.6 V
  - Separate I/O supply pin (1.65 V to 3.6 V)
  - Power-on / power-down reset (POR/PDR)
  - Programmable brownout reset (BOR)
  - Low-power modes: Sleep, Stop, Standby, Shutdown
- Clock management
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator with calibration
  - Internal 48 MHz RC oscillator (±1 %)
  - Internal 48 MHz RC oscillator with clock recovery system
  - Internal 32 kHz RC oscillator (±5 %)
- Up to 61 fast I/Os
  - All mappable on external interrupt vectors
  - All 5 V-tolerant
- 5-channel DMA controller with flexible mapping
- 12-bit, 0.4 µs ADC (up to 19 ext. channels)
  - Conversion range: 0 to 3.6 V
- 9 timers: 16-bit for advanced motor control, one 32-bit timer and four 16-bit general-purpose, two watchdogs, SysTick timer
- Calendar RTC with alarm



- Communication interfaces
  - Two I^2C-bus interface supporting Fast-mode Plus (1 Mbit/s) with extra current sink; one supporting SMBus/PMBus™ and wake-up from Stop mode
  - Two USARTs with master/slave synchronous SPI; one supporting ISO7816 interface, LIN, IrDA capability, auto baud rate detection and wake-up feature
  - Two SPIs (24 Mbit/s) with 4- to 16-bit programmable bitframe, one multiplexed with I²S interface; two extra SPIs through USARTs
- USB 2.0 FS device (crystal-less) and host controller
- Development support: serial wire debug (SWD)
- 96-bit unique ID
- All packages ECOPACK 2 compliant

Table 1. Device summary

Reference	Part number
STM32C071x8	STM32C071F8, STM32C071G8, STM32C071K8, STM32C071C8, STM32C071R8
STM32C071xB	STM32C071FB, STM32C071GB, STM32C071KB, STM32C071CB, STM32C071RB

This is information on a product in full production.

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1 Introduction

This document provides information on STM32C071x8/xB microcontrollers, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging, and ordering codes.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32C071x8/xB errata sheet ES0618.

Information on memory mapping and control registers is the subject of the reference manual RM0490.

Information on Arm®(a) Cortex®-M0+ core is available from the www.arm.com website.

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2 Description

The STM32C071x8/xB mainstream microcontrollers are based on high-performance Arm® Cortex®-M0+ 32-bit RISC core operating at up to 48 MHz frequency. Offering a high level of integration, they are suitable for a wide range of applications in consumer, industrial and appliance domains and ready for the Internet of Things (IoT) solutions.

The devices incorporate a memory protection unit (MPU), high-speed embedded memories (24 Kbytes of SRAM and up to 128 Kbytes of flash program memory with read and write protection, proprietary code protection, and securable area), DMA, an extensive range of system functions, enhanced I/Os, and peripherals. The devices offer standard communication interfaces (two I^2Cs, two SPI / one I^2S, one full-speed USB, and two USARTs), one 12-bit ADC (2.5 MSps) with up to 19 channels, a low-power RTC, an advanced control PWM timer, four general-purpose 16-bit timers, a 32-bit general-purpose timer, two watchdog timers, and a SysTick timer.

The devices operate within ambient temperatures from -40 to 125°C and with supply voltages from 2.0 V to 3.6 V. Optimized dynamic consumption combined with power-saving modes allows the design of low-power applications.

The devices are housed in packages with 19 to 64 pins.

Table 2. STM32C071x8/xB family device features and peripheral counts

Peripheral		STM32C071_									
		_F8 / _FB	_F8xxN / _FBxxN	_G8 / _GB	_G8xxN / _GBxxN	_K8 / _KB	_K8xxN / _KBxxN	_C8 / _CB	_C8xxN / _CBxxN	_R8 / _RB	_R8xxN / _RBxxN
Flash memory (Kbyte)		64/128(1)	64/128								64/128(2)
SRAM (Kbyte)		24 with parity									
Timers	Advanced control	1 (16-bit)									
	General-purpose	1 (32-bit)									
		4 (16-bit)									
	SysTick	1									
	Watchdog	2									
Communication	SPI [I2S](3)	2 [1] + 2 extra through USARTs									
	I2C	2									
	USART	2									
	USB	1									
RTC		Yes									
VDDIO2 pin		No	Yes	No	Yes	No	Yes	No	Yes	No	Yes
GPIOs (all 5V-tolerant)		18 or 17(4)	17	26	25	30	29	45	43	61	59
DMA channels		5									
Wakeup pins		4		5		5		5		6	

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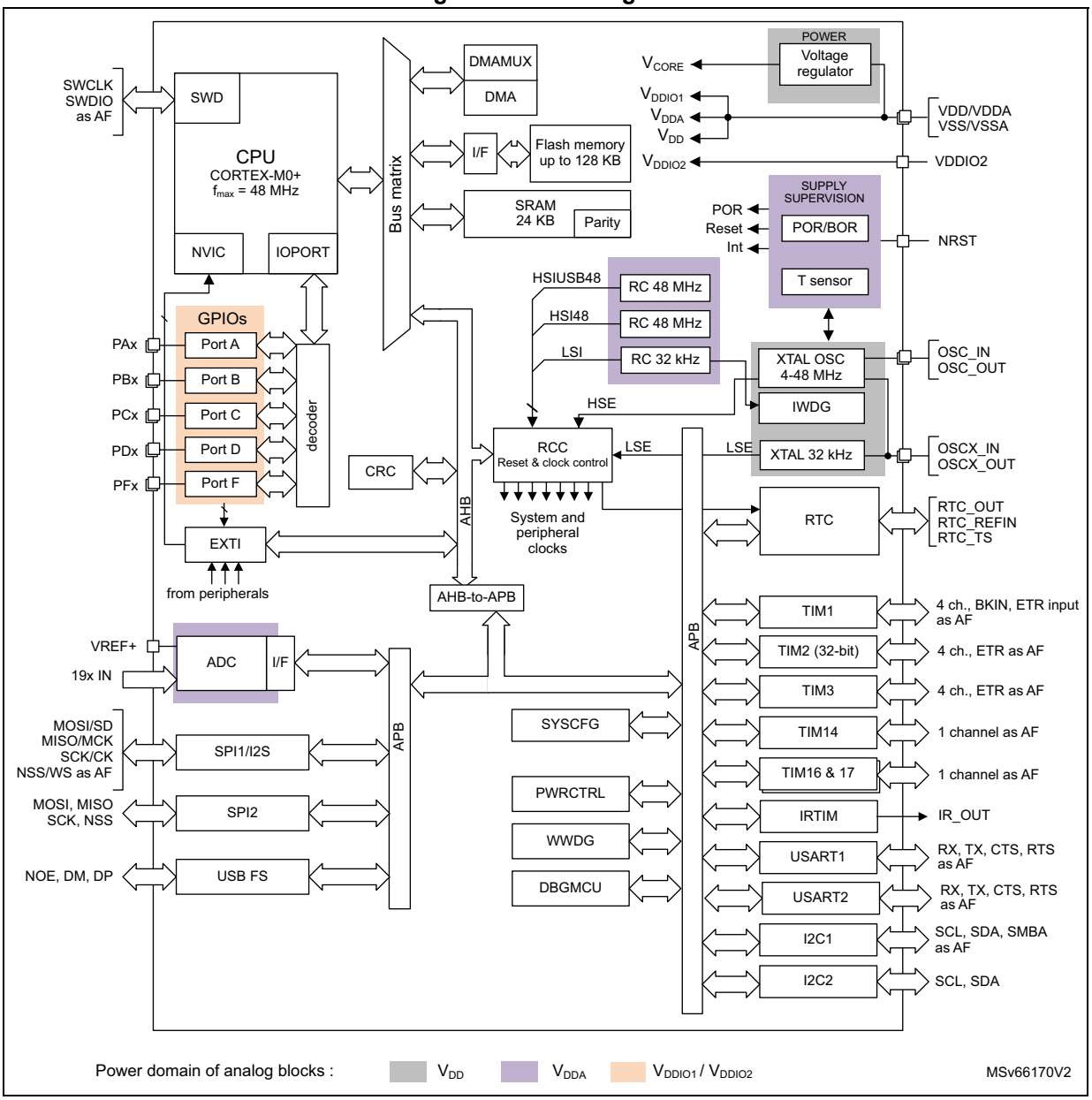
Table 2. STM32C071x8/xB family device features and peripheral counts (continued)

Peripheral	STM32C071_									
	_F8 / _FB	_F8xxN / _FBxxN	_G8 / _GB	_G8xxN / _GBxxN	_K8 / _KB	_K8xxN / _KBxxN	_C8 / _CB	_C8xxN / _CBxxN	_R8 / _RB	_R8xxN / _RBxxN
12-bit ADC channels (ext. + int.)	11 + 2		13 + 2		14 + 2		17 + 2		19 + 2	
Max. CPU frequency	48 MHz									
Operating voltage	2.0 to 3.6 V									
Operating temperature(5)	Ambient: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C									
Packages	WLCSP19 TSSOP20	TSSOP 20	UFQPN28		UFQFPN32 LQFP32		UFQFPN48 LQFP48		LQFP 64	UFBGA64 LQFP64
Bootloader	USART1, USART2, I2C1, I2C2, SPI1, SPI2, and USB DFU									

1. Only 128 KB version is available for parts in WLCSP19 package.
2. Only 128 KB version is available for parts in UFBGA64 package.
3. The numbers in brackets denote the count of SPI interfaces configurable as I^2S interface.
4. For WLCSP19 package
5. Depends on order code. Refer to *Section 7: Ordering information* for details.

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Figure 1. Block diagram



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3 Functional overview

3.1 Arm® Cortex®-M0+ core with MPU

The Cortex-M0+ is an entry-level 32-bit Arm Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture, easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area- and power-optimized 32-bit core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to embedded Arm core, the STM32C071x8/xB devices are compatible with Arm tools and software.

The Cortex-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC) described in *Section 3.13.1*.

3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3 Embedded flash memory

STM32C071x8/xB devices feature up to 128 Kbytes of embedded flash memory available for storing code and data.

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Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M0+ serial wire), boot in RAM and bootloader selection are disabled. This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU as instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. An additional option bit (PCROP_RDP) determines whether the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

3.3.1 Securable area

A part of the Flash memory can be hidden from the application once the code it contains is executed. As soon as the write-once SEC_PROT bit is set, the securable memory cannot be accessed until the system resets. The securable area generally contains the secure boot code to execute only once at boot. This helps to isolate secret code from untrusted application code.

3.4 Embedded SRAM

STM32C071x8/xB devices have 24 Kbytes of embedded SRAM with parity. Hardware parity check allows memory data errors to be detected, which contributes to increasing functional safety of applications.

The memory can be read/write-accessed at CPU clock speed, with 0 wait states.

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3.5 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from main flash memory
- boot from system memory
- boot from embedded SRAM

The boot pin is shared with a standard GPIO and can be enabled through the boot selector option bit. If the BOOT0 pin selects the boot from the main flash memory of which the first location is empty, the flash memory empty checker forces the boot from the system memory.

The system memory contains an embedded boot loader. It manages the flash memory reprogramming through one of the following interfaces:

- USART on pins PA9/PA10 or PA3/PA2
- I^2C-bus on pins PB6/PB7 or PB10/PB11
- SPI on pins PA4/PA5/PA6/PA7 (PA2/PA4/PA5/PA6 on TSSOP20 N package) or PB12/PB13/PB14/PB15
- USB on pins PA11/PA12

When boot loader is executed, it configures some of the GPIOs out of their by-default high-Z state. Refer to AN2606 for more details on the boot loader and on the GPIO configuration when booting from the system memory.

3.6 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

3.7 Power supply management

3.7.1 Power supply schemes

The STM32C071x8/xB devices require 2.0 V to 3.6 V operating supply voltage (V_{DD}). Several different power supplies are provided to specific peripherals:

- V_{DD} = 2.0 V (1.96 V) to 3.6 V

  V_{DD} is the external power supply for the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD/VDDA pin.

  The minimum voltage of 2.0 V corresponds to power-on reset release threshold V_{POR}(max). Once this threshold is crossed and power-on reset is released, the functionality is guaranteed down to power-down reset threshold V_{PDR}(min) of 1.96 V.

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- V_{DDA} = 2.0 V (1.96 V) to 3.6 V

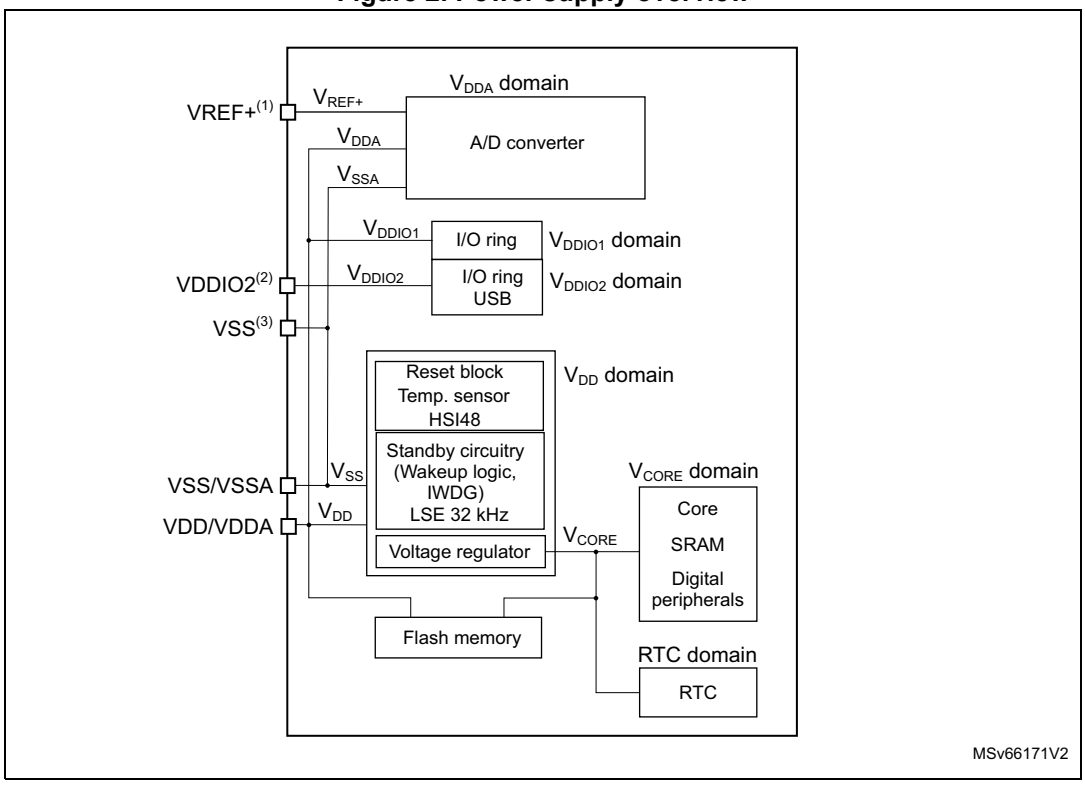
  V_{DDA} is the analog power supply for the A/D converter. V_{DDA} voltage level is identical to V_{DD} voltage as it is provided externally through VDD/VDDA pin.
- V_{DDIO1} = V_{DD}

  V_{DDIO1} is the power supply for the I/Os. V_{DDIO1} voltage level is identical to V_{DD} voltage as it is provided externally through VDD/VDDA pin.
- V_{DDIO2} = 1.65 V to 3.6 V

  V_{DDIO2} is the power supply from VDDIO2 pin for certain I/Os and the USB peripheral. On packages without VDDIO2 pin, V_{DDIO2} is internally connected with V_{DD}. Although V_{DDIO2} is independent of V_{DD} and V_{DDA}, it must not be applied without valid V_{DD}.
- V_{REF+} is the analog peripheral input reference voltage.

  V_{REF+} is delivered through VREF+ pin. On packages without VREF+ pin, V_{REF+} is internally connected with V_{DD}.
- V_{CORE} is an internal supply for digital peripherals, SRAM and flash memory. It is produced by an embedded linear voltage regulator. On top of V_{CORE}, the flash memory is also powered from V_{DD}.

Figure 2. Power supply overview



1. Internally connected to VDD/VDDA pin on packages without VREF+ pin.
2. Internally connected to VDD/VDDA pin on packages without VDDIO2 pin.
3. Internally connected to VSS/VSSA pin on packages without VSS pin.

3.7.2 Power supply supervisor

The device has an integrated power-on/power-down (POR/PDR) reset active in all power modes except Shutdown and ensuring proper operation upon power-on and power-down. It

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maintains the device in reset when the supply voltage is below $V_{POR/PDR}$ threshold, without the need for an external reset circuit. Brownout reset (BOR) function allows extra flexibility. It can be enabled and configured through option bytes, by selecting one of four thresholds for rising V_{DD} and other four for falling V_{DD}.

3.7.3 Voltage regulator

An embedded linear voltage regulator supplies most of the digital circuitry in the device.

In Standby and Shutdown modes, the regulator is powered down and its output set in high-impedance state, such as to bring its current consumption close to zero.

3.7.4 Low-power modes

By default, the device is in Run mode after system or power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode

  In Stop mode, the device achieves the lowest power consumption while retaining the SRAM and register contents. All clocks in the V_{CORE} are stopped. The HSE and HSI48 oscillators stop. The HSIUSB48 oscillator is powered down. The HSI48 can be restarted by a peripheral with wake-up capability requiring HSI48.
  The LSE and LSI can be kept running. The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  The event of exiting Stop mode enables the HSI48 oscillator and select HSISYS as system clock.
- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption, with POR/PDR always active in this mode. The regulator is switched off to power down V_{CORE} domain. The HSI48 and HSIUSB48 RC oscillators and the HSE crystal oscillator are also powered down. The RTC is switched off.

  For each I/O, the software can determine whether a pull-up, a pull-down or no resistor shall be applied to that I/O during Standby mode.

  Upon entering Standby mode, register contents are lost, except for 16-bit backup registers whose contents are kept.

  The device exits Standby mode upon external reset event (NRST pin), IWDG reset event, wake-up event (WKUP pin, configurable rising or falling edge), or when a failure is detected on LSE (CSS on LSE).
- **Shutdown** mode

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The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off to power down the V_{CORE} domain. The HSI48, HSIUSB48 and LSI RC-oscillators and HSE crystal oscillator are also powered down. The RTC is off.

The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode.

SRAM and register contents are lost.

The device exits Shutdown mode upon external reset event (NRST pin), or wake-up event (WKUP pin, configurable rising or falling edge).

3.7.5 Reset mode

During and upon exiting reset, the Schmitt triggers of I/Os are disabled so as to reduce power consumption. In addition, when the reset source is internal, the built-in pull-up resistor on NRST pin is deactivated.

3.8 Interconnect of peripherals

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.

Table 4. Interconnect of peripherals

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Stop
TIMx	TIMx	Timer synchronization or chaining	Y	Y	-
	ADCx	Conversion triggers	Y	Y	-
	DMA	Memory-to-memory transfer trigger	Y	Y	-
ADCx	TIM1	Timer triggered by analog watchdog	Y	Y	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	-
All clock sources (internal and external)	TIM14,16,17	Clock source used as input channel for RC measurement and trimming	Y	Y	-
CSS RAM (parity error)	TIM1,16,17	Timer break	Y	Y	-
CPU (hard fault)	TIM1,16,17	Timer break	Y	-	-

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Table 4. Interconnect of peripherals (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Stop
GPIO	TIM1,2,3	External trigger	Y	Y	-
	ADC	Conversion external trigger	Y	Y	-

3.9 Clocks and startup

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** the following clock sources can deliver SYSCLK system clock:
  - 4-48 MHz high-speed oscillator with external crystal or ceramic resonator (HSE). The HSE can also be configured in bypass mode for an external clock.
  - 48 MHz high-speed internal RC oscillators (HSI48 and HSIUSB48), trimmable by software.
  - 32.768 kHz low-speed oscillator with external crystal (LSE), supporting two drive capability modes. The LSE can also be configured in bypass mode for using an external clock.
  - 32 kHz low-speed internal RC oscillator (LSI) with ±5% accuracy, also used to clock an independent watchdog.
- **Peripheral clock sources:** several peripherals (I2S, USART1, I2C1, ADC, USB FS) can operate with a clock source independent of the system clock. The HSIUSB48 RC oscillator associated with CRS allows the USB FS peripheral to operate without requiring an external resonator, as a USB device.
- **Clock security system (CSS):** in the event of HSE or LSE clock failure, the system clock is automatically switched to HSI48 or LSI, respectively. If enabled, a software interrupt is generated. The CCS feature can be enabled by software.
- **Clock output:**
  - **MCO and MCO2 (microcontroller clock output)** provides one of the internal clocks for external use by the application.
  - **LSCO (low speed clock output)** provides LSI or LSE in all low-power modes.

Several prescalers allow the application to configure AHB and APB domain clock frequencies, 48 MHz at maximum.

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3.10 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function (AF). Most of the GPIO pins are shared with special digital or analog functions.

Through a specific sequence, this special function configuration of I/Os can be locked, such as to avoid spurious writing to I/O control registers.

3.11 Direct memory access controller (DMA)

The direct memory access (DMA) controller is a bus master and system peripheral with single-AHB architecture.

With 5 channels, it performs data transfers between memory-mapped peripherals and/or memories, to offload the CPU.

Each channel is dedicated to managing memory access requests from one or more peripherals. The unit includes an arbiter for handling the priority between DMA requests.

Main features of the DMA controller:

- Single-AHB master
- Peripheral-to-memory, memory-to-peripheral, memory-to-memory and peripheral-to-peripheral data transfers
- Access, as source and destination, to on-chip memory-mapped devices such as flash memory, SRAM, and AHB and APB peripherals
- All DMA channels independently configurable:
  - Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
  - Priority between the requests is programmable by software (four levels per channel: very high, high, medium, low) and by hardware in case of equality (such as request to channel 1 has priority over request to channel 2).
  - Transfer size of source and destination are independent (byte, half-word, word), emulating packing and unpacking. Source and destination addresses must be aligned on the data size.
  - Support of transfers from/to peripherals to/from memory with circular buffer management
  - Programmable number of data to be transferred: 0 to 2^{16} - 1
- Generation of an interrupt request per channel. Each interrupt request originates from any of the three DMA events: transfer complete, half transfer, or transfer error.

3.12 DMA request multiplexer (DMAMUX)

The DMAMUX request multiplexer enables routing a DMA request line between the peripherals and the DMA controller. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. DMAMUX may also be used as a DMA request generator from programmable events on its input trigger signals.

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3.13 Interrupts and events

The device flexibly manages events causing interrupts of linear program execution, called exceptions. The Cortex-M0+ processor core, a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI) are the assets contributing to handling the exceptions. Exceptions include core-internal events such as, for example, a division by zero and, core-external events such as logical level changes on physical lines. Exceptions result in interrupting the program flow, executing an interrupt service routine (ISR) then resuming the original program flow.

The processor context (contents of program pointer and status registers) is stacked upon program interrupt and unstacked upon program resume, by hardware. This avoids context stacking and unstacking in the interrupt service routines (ISRs) by software, thus saving time, code and power. The ability to abandon and restart load-multiple and store-multiple operations significantly increases the device's responsiveness in processing exceptions.

3.13.1 Nested vectored interrupt controller (NVIC)

The configurable nested vectored interrupt controller is tightly coupled with the core. It handles physical line events associated with a non-maskable interrupt (NMI) and maskable interrupts, and Cortex-M0+ exceptions. It provides flexible priority management.

The tight coupling of the processor core with NVIC significantly reduces the latency between interrupt events and start of corresponding interrupt service routines (ISRs). The ISR vectors are listed in a vector table, stored in the NVIC at a base address. The vector address of an ISR to execute is hardware-built from the vector table base address and the ISR order number used as offset.

If a higher-priority interrupt event happens while a lower-priority interrupt event occurring just before is waiting for being served, the later-arriving higher-priority interrupt event is served first. Another optimization is called tail-chaining. Upon a return from a higher-priority ISR then start of a pending lower-priority ISR, the unnecessary processor context unstacking and stacking is skipped. This reduces latency and contributes to power efficiency.

Features of the NVIC:

- Low-latency interrupt processing
- 4 priority levels
- Handling of a non-maskable interrupt (NMI)
- Handling of 32 maskable interrupt lines
- Handling of 10 Cortex-M0+ exceptions
- Later-arriving higher-priority interrupt processed first
- Tail-chaining
- Interrupt vector retrieval by hardware

3.13.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller adds flexibility in handling physical line events and allows identifying wake-up events at processor wake-up from Stop mode.

The EXTI controller has a number of channels, of which some with rising, falling or rising, and falling edge detector capability. Any GPIO and a few peripheral signals can be connected to these channels.

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The channels can be independently masked.

The EXTI controller can capture pulses shorter than the internal clock period.

A register in the EXTI controller latches every event even in Stop mode, which allows the software to identify the origin of the processor's wake-up from Stop mode or, to identify the GPIO and the edge event having caused an interrupt.

3.14 Analog-to-digital converter (ADC)

A native 12-bit analog-to-digital converter is embedded into STM32C071x8/xB devices. The ADC has up to 19 external channels and 2 internal channels (temperature sensor, voltage reference). It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 2.5 MSps even with a low CPU speed. An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate in the whole V_{DD} supply range.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions with timers.

3.14.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to an ADC input to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor may vary from part to part due to process variation, the uncalibrated internal temperature sensor is suitable only for relative temperature measurements.

To improve the accuracy of the temperature sensor, each part is individually factory-calibrated by ST. The resulting calibration data are stored in the part’s engineering bytes, accessible in read-only mode.

Table 5. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF7568-0x1FFF7569

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3.14.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to an ADC input. The V_{REFINT} voltage is individually precisely measured for each part by ST during production test and stored in the part's engineering bytes. It is accessible in read-only mode.

Table 6. Internal voltage reference calibration values

Calibration value name	Description	Memory address
V_{REFINT}	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF756A-0x1FFF756B

3.15 Timers and watchdogs

The device includes an advanced-control timer, five general-purpose timers, two watchdog timers and a SysTick timer. *Table 7* compares features of the advanced-control and general-purpose timers.

Table 7. Timer feature comparison

Timer	Timer type	Counter resolution	Counter type	Maximum operating frequency	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary outputs
TIM1	Advanced-control	16-bit	Up, down, up/down	48 MHz	Integer from 1 to 2^{16}	Yes	4 +2 internal	3
TIM2	General-purpose	32-bit	Up, down, up/down	48 MHz	Integer from 1 to 2^{16}	Yes	4	-
TIM3	General-purpose	16-bit	Up, down, up/down	48 MHz	Integer from 1 to 2^{16}	Yes	4	-
TIM14	General-purpose	16-bit	Up	48 MHz	Integer from 1 to 2^{16}	No	1	-
TIM16 TIM17	General-purpose	16-bit	Up	48 MHz	Integer from 1 to 2^{16}	Yes	1	1

3.15.1 Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM unit multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM output (edge or center-aligned modes) with full modulation capability (0-100%)
- one-pulse mode output

On top of these, there are two internal channels that can be used.

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In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled, so as to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.15.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.15.2 General-purpose timers (TIM2, 3, 14, 16, 17)

There are five synchronizable general-purpose timers embedded in the device (refer to *Table 7* for comparison). Each general-purpose timer can be used to generate PWM outputs or act as a simple timebase.

- TIM2, TIM3

  These are full-featured general-purpose timers:

  – TIM2 with 32-bit auto-reload up/downcounter and 16-bit prescaler

  – TIM3 with 16-bit auto-reload up/downcounter and 16-bit prescaler

  They have four independent channels for input capture/output compare, PWM or one-pulse mode output. They can operate in combination with other general-purpose timers via the Timer Link feature for synchronization or event chaining. They can generate independent DMA request and support quadrature encoders. Their counter can be frozen in debug mode.

- TIM14

  This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. It has one channel for input capture/output compare, PWM output or one-pulse mode output. Its counter can be frozen in debug mode.

- TIM16, TIM17

  These are general-purpose timers featuring:

  – 16-bit auto-reload upcounter and 16-bit prescaler

  – 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output. The timers can operate together via the Timer Link feature for synchronization or event chaining. They can generate independent DMA request. Their counters can be frozen in debug mode.

3.15.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 32 kHz internal RC (LSI). Independent of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. Its counter can be frozen in debug mode.

3.15.4 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked by the system clock. It has an early-warning interrupt capability. Its counter can be frozen in debug mode.

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3.15.5 SysTick timer

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter.

Features of SysTick timer:

- 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.16 Real-time clock (RTC)

The devices embed an RTC located in the RTC domain and supplied from V_{CORE}.

The RTC is an independent BCD timer/counter.

Features of the RTC:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Programmable alarm
- On-the-fly correction from 1 to 32767 RTC clock pulses, usable for synchronization with a master clock
- Reference clock detection - a more precise second-source clock (50 or 60 Hz) can be used to improve the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature to save a calendar snapshot, triggered by an event on the timestamp pin
- Multiple clock sources and references:
  - a 32.768 kHz external crystal (LSE)
  - an external resonator or oscillator (LSE)
  - the internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
  - the high-speed external clock (HSE) divided by 32

The RTC operates in Run, Sleep, and Stop mode.

RTC events (Alarm, Timestamp) can generate an interrupt and wake the device up from the low-power modes.

3.17 Inter-integrated circuit interface (I2C)

The devices embed two I2C peripheral. Refer to *Table 8* for the features.

The I2C peripheral handles communication between the microcontroller and the serial I^2C-bus. It controls all I^2C-bus-specific sequencing, protocol, arbitration and timing.

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Features of the I2C peripheral:

- I²C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and extra output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Clock stretching
- SMBus specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Command and data acknowledge control
  - Address resolution protocol (ARP) support
  - Host and device support
  - SMBus alert
  - Timeouts and idle condition detection
- PMBus rev 1.3 standard compatibility
- Independent clock: a choice of independent clock sources allowing the I²C-bus communication speed to be independent of the PCLK reprogramming
- Wake-up from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 8. I²C implementation

I²C features(1)	I2C1	I2C2
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus (up to 1 Mbit/s) with extra output drive I/Os	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	-
Independent clock	X	-
Wakeup from Stop mode on address match	X	-

1. X: supported

3.18 Universal synchronous/asynchronous receiver transmitter (USART)

The devices embed two universal synchronous/asynchronous receivers/transmitters that communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, synchronous SPI communication and single-wire half-

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duplex communication mode. Some can also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and have a clock domain independent of the CPU clock, which allows them to wake up the MCU from Stop mode. The wake-up events from Stop mode are programmable and can be:

- start bit detection
- any received data frame
- a specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 9. USART implementation

USART modes/features(1)	USART1	USART2
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
SPI emulation master/slave (synchronous mode)	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wake-up from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X: supported

3.19 Serial peripheral interface (SPI)

The devices contain two SPI running at up to 24 Mbits/s in master and slave modes. It supports half-duplex, full-duplex and simplex communications. A 3-bit prescaler gives eight master mode frequencies. The frame size is configurable from 4 bits to 16 bits. The SPI peripherals support NSS pulse mode, TI mode and hardware CRC calculation.

The SPI peripherals can be served by the DMA controller.

The I^2S interface mode of the SPI peripheral (if supported, see the following table) supports four different audio standards can operate as master or slave, in half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

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Table 10. SPI/I2S implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I^2S mode	X	-
TI mode	X	X

1. X = supported.

3.20 Universal serial bus device (USB) and host (USBH)

The devices embed a USB controller with full-speed USB device and host functionality, compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory of 2 KB and suspend/resume support. It requires a precise 48 MHz clock that is generated from the internal high-speed external clock source or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization), which allows crystal-less operation in USB device mode.

3.21 Development support

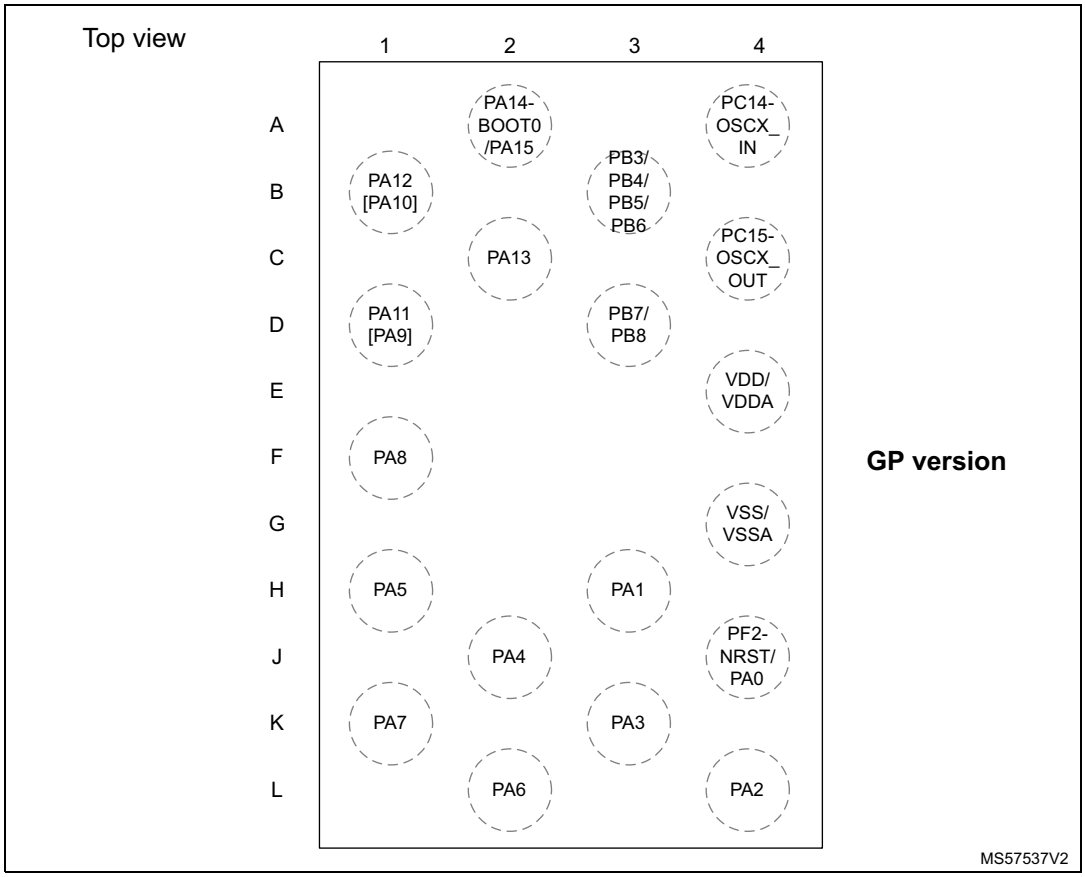
3.21.1 Serial wire debug port (SW-DP)

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

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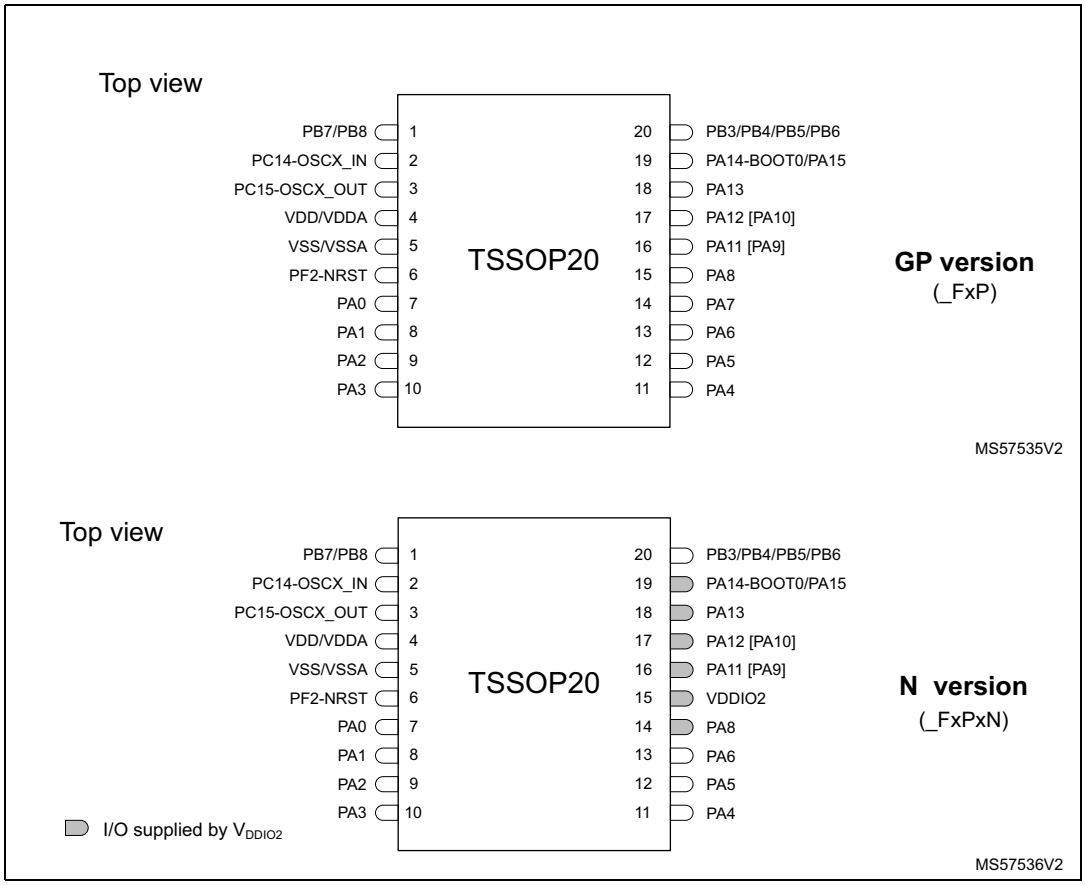
4 Pinouts, pin description and alternate functions

Figure 3. STM32C071FxY WLCSP19 ballout



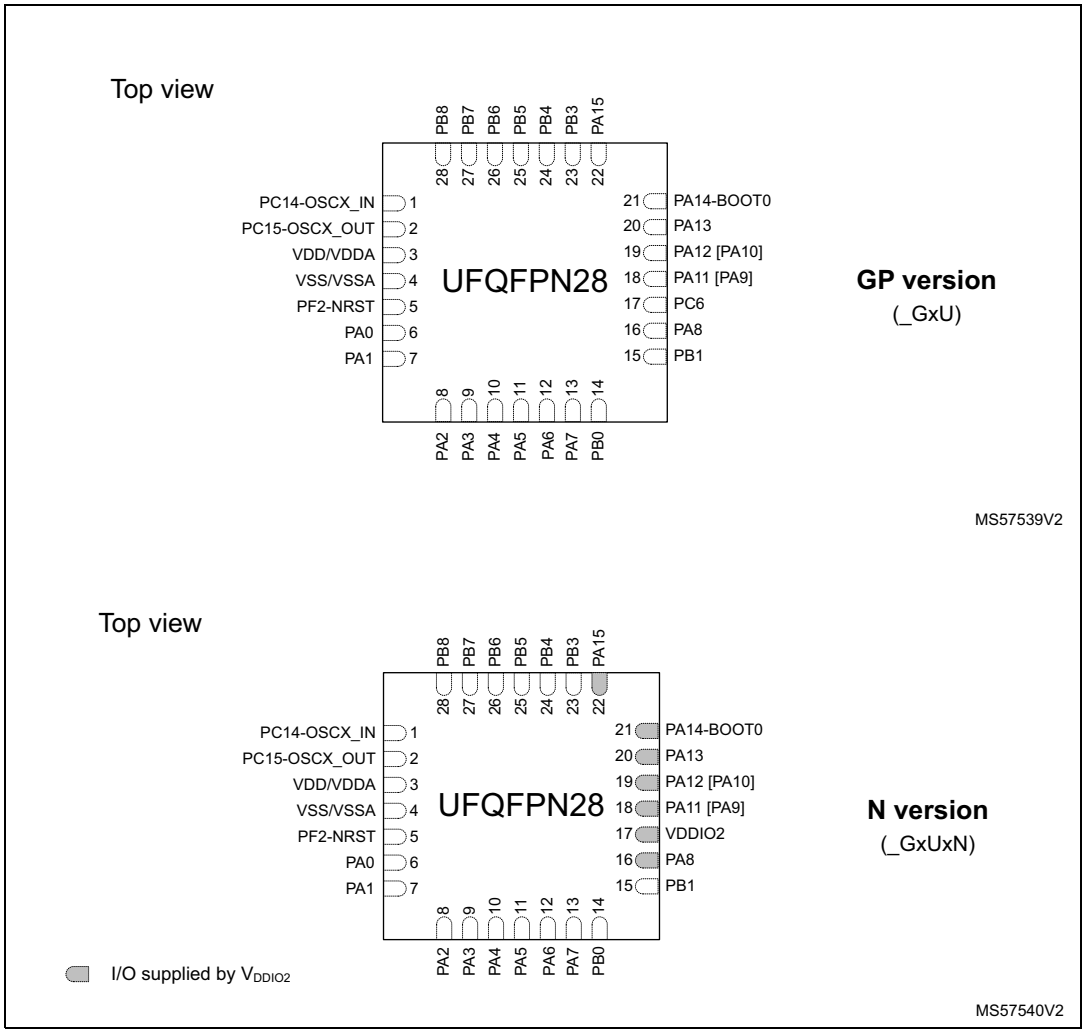
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Figure 4. STM32C071FxP TSSOP20 pinout



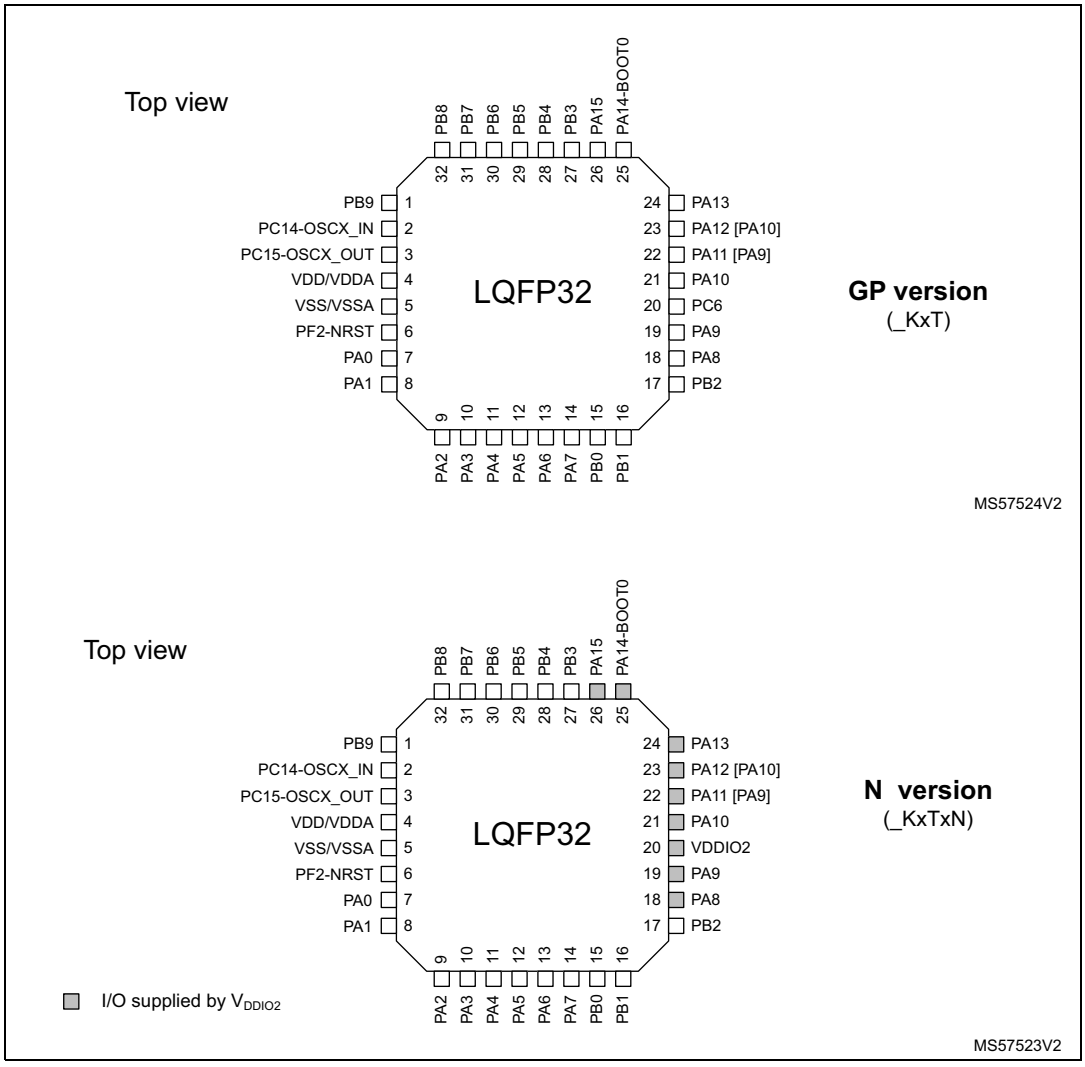
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Figure 5. STM32C071GxU UFQFPN28 pinout



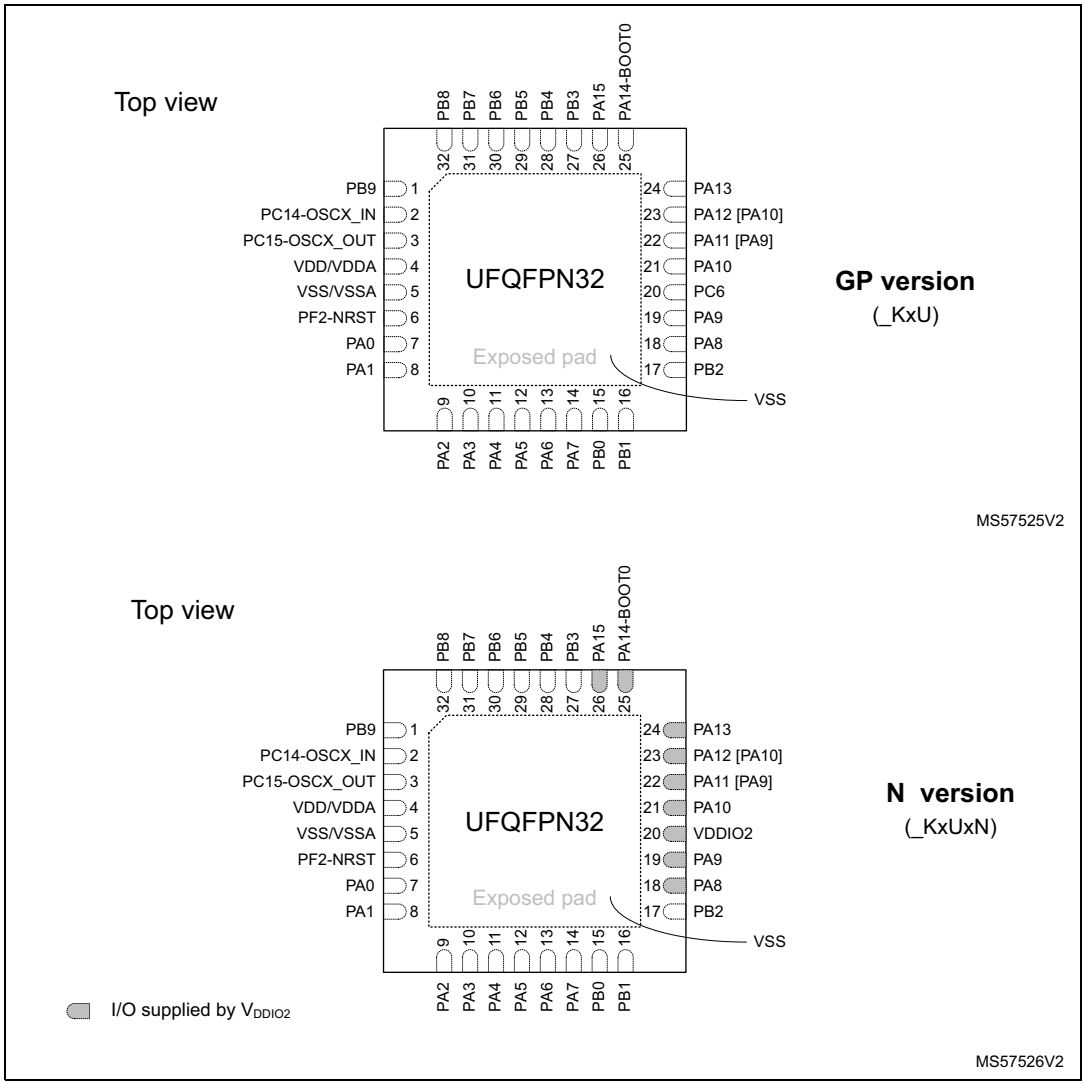
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Figure 6. STM32C071KxT LQFP32 pinout



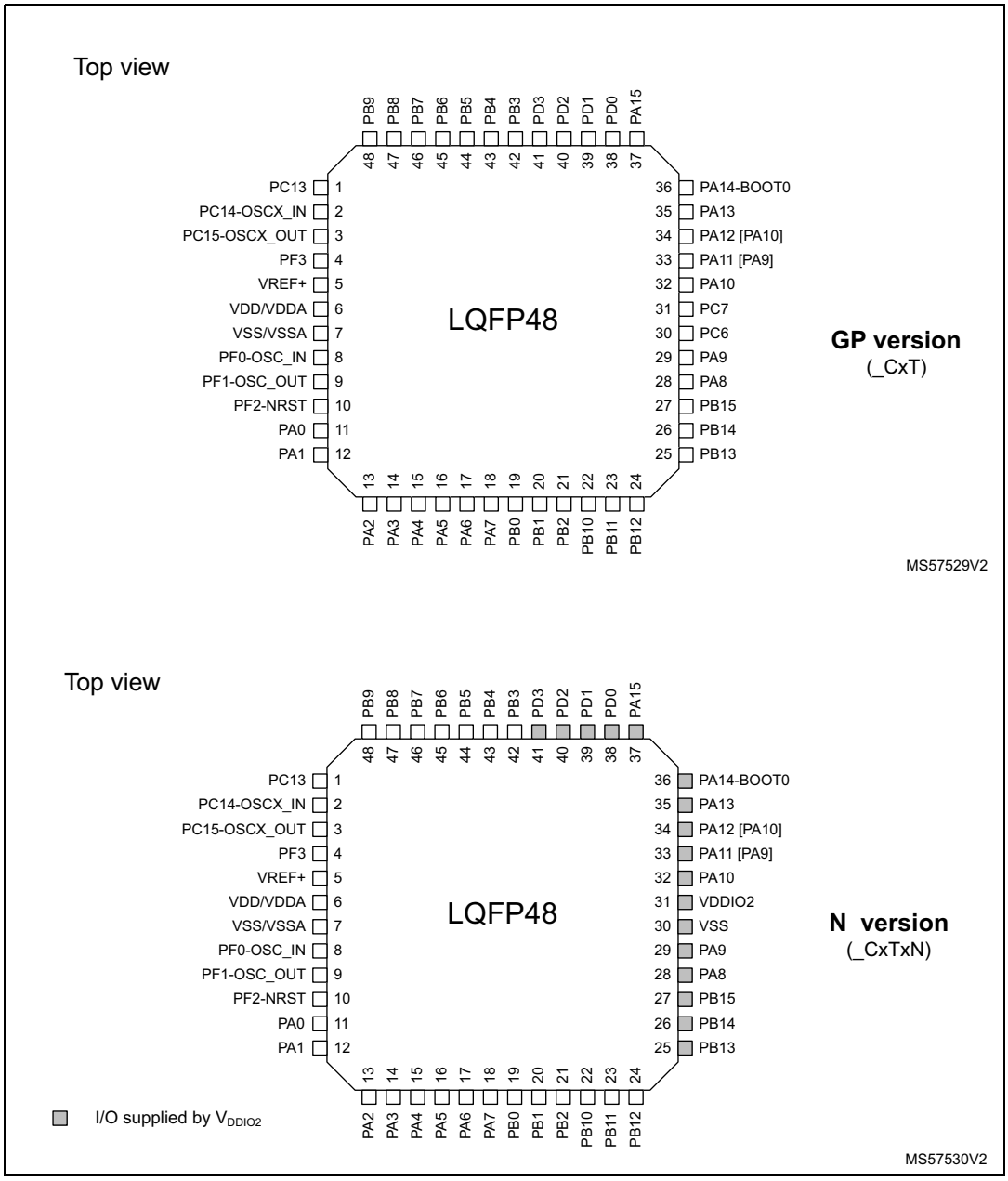
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Figure 7. STM32C071KxU UFQFPN32 pinout



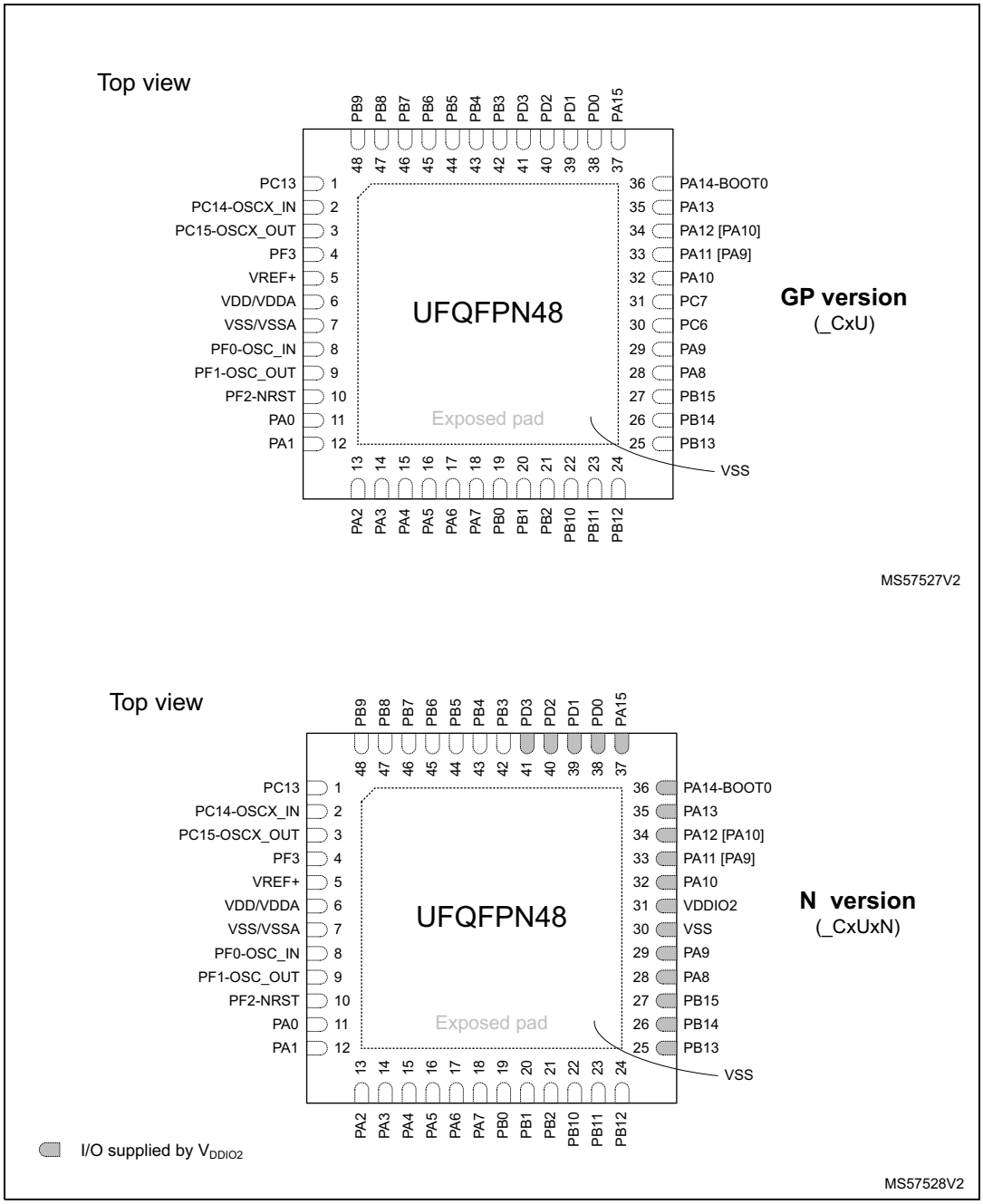
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Figure 8. STM32C071CxT LQFP48 pinout



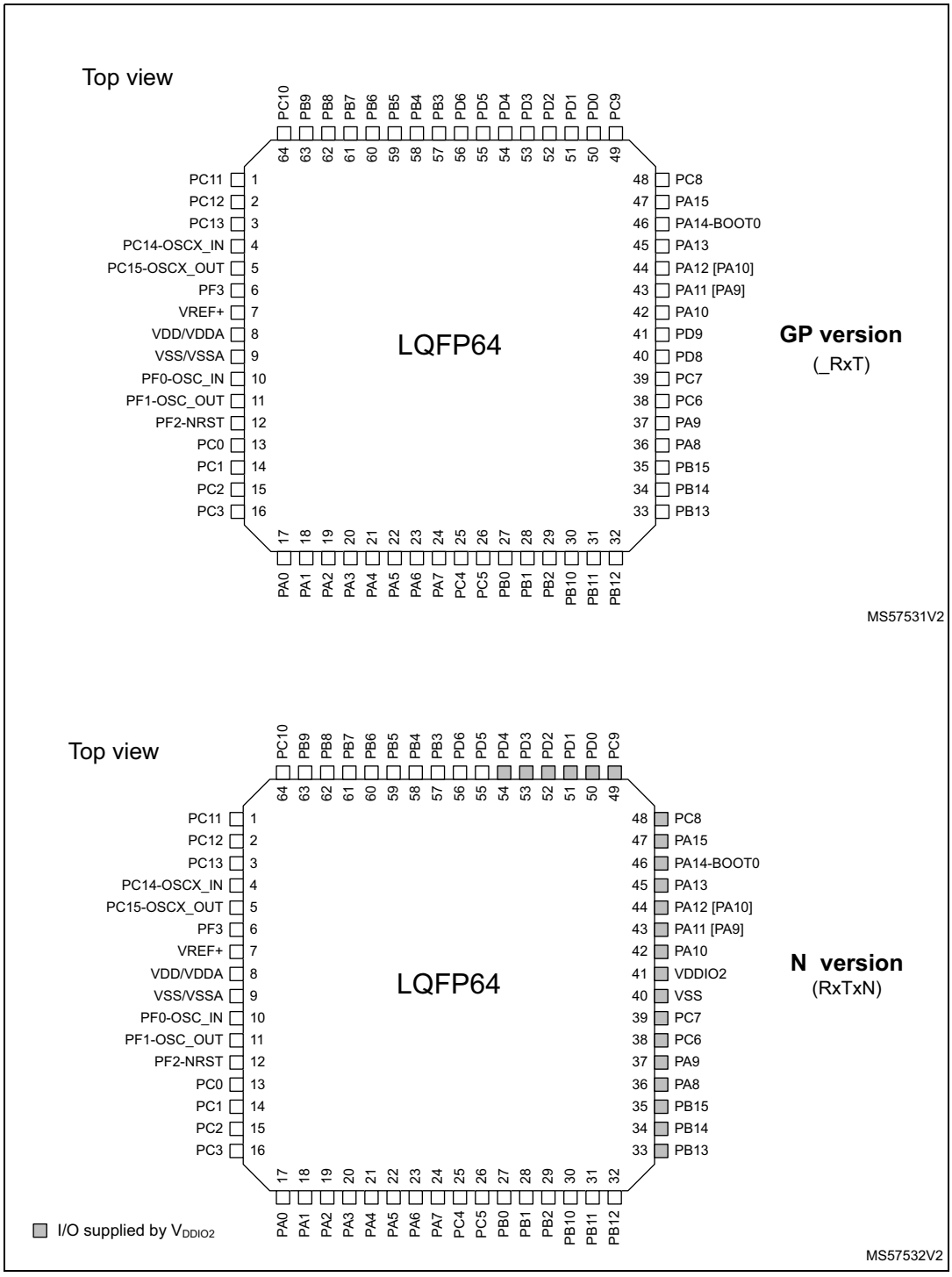
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Figure 9. STM32C071CxU UFQFPN48 pinout



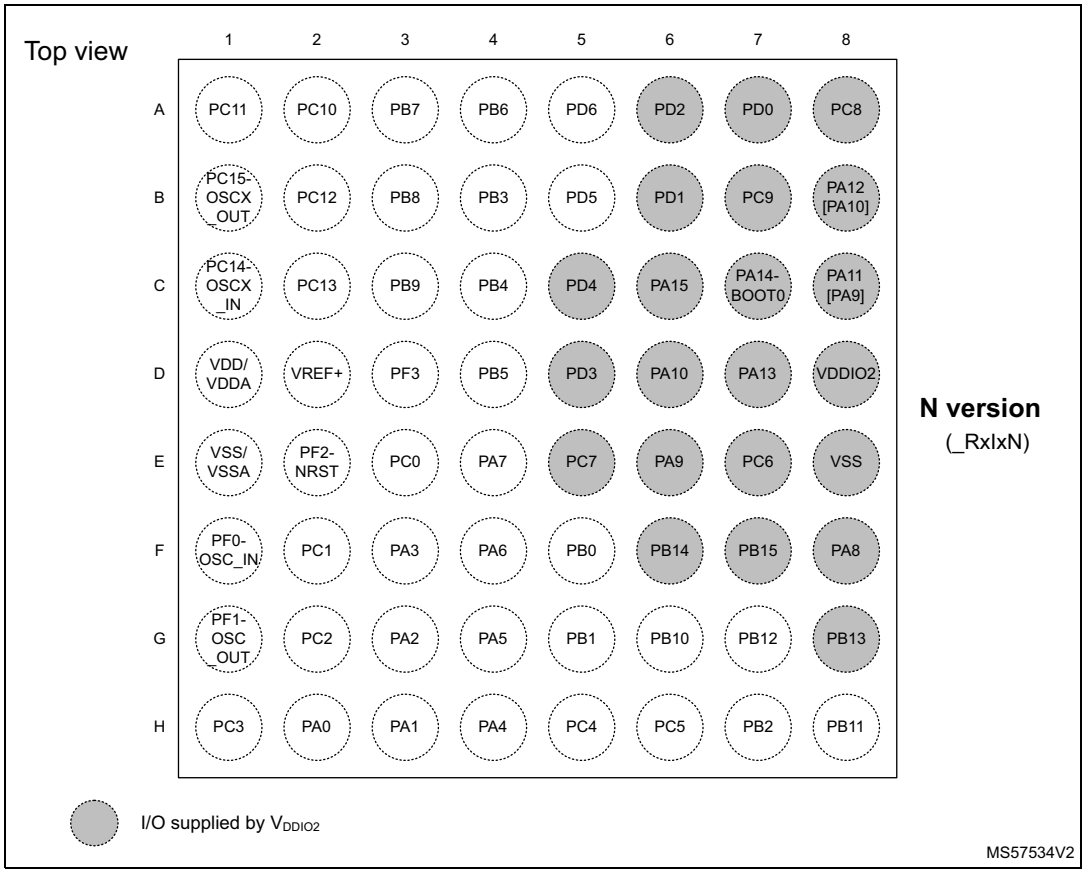
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Figure 10. STM32C071RxT LQFP64 pinout



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Figure 11. STM32C071RxI UFBGA64 pinout



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Table 11. Terms and symbols used in the pin assignment table

Column		Symbol	Definition
Pin name		Terminal name corresponds to its by-default function at reset, unless otherwise specified in parenthesis under the pin name.	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		RST	Reset pin with embedded weak pull-up resistor
		Options for FT I/Os	
		_f	I/O, Fm+ capable
		_a	I/O, with analog switch function
		_s	I/O only supplied by V_{DDIO2}
		_u	I/O, with USB function
Note		Upon reset, all I/Os are set as analog inputs, unless otherwise specified.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 12. Pin assignment and description

Pin Number[1]							Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP19 GP	TSSOP20 GP/N	UFQFPN28 GP/N	LQFP32, UFQFPN32 GP/N	LQFP48, UFQFPN48 GP/N	LQFP64 GP/N	UFBGA64 N						
-	-	-	-	-	1	A1	PC11	I/O	FT	-	TIM1_CH4	-
-	-	-	-	-	2	B2	PC12	I/O	FT	-	TIM14_CH1	-
-	-	-	-	1	3	C2	PC13	I/O	FT	-	TIM1_ETR, TIM1_BKIN	RTC_TS, RTC_OUT1, WKUP2
A4	2	1	2	2	4	C1	PC14-OSCX_IN (PC14)	I/O	FT_f	-	USART1_TX, TIM1_ETR, TIM1_BKIN2, IR_OUT, USART2_RTS/USART2_DE/USART2_CK, TIM17_CH1, TIM3_CH2, SPI2_NSS, I2C1_SDA, EVENTOUT	OSCX_IN
C4	3	2	3	3	5	B1	PC15-OSCX_OUT (PC15)	I/O	FT	-	OSC32_EN, OSC_EN, TIM1_ETR, TIM3_CH3	OSCX_OUT
-	-	-	-	4	6	D3	PF3	I/O	FT	-	-	-
-	-	-	-	5	7	D2	VREF+	S	-	-	-	-

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Table 12. Pin assignment and description (continued)

Pin Number[1]							Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP19 GP	TSSOP20 GP/N	UFQFPN28 GP/N	LQFP32, UFQFPN32 GP/N	LQFP48, UFQFPN48 GP/N	LQFP64 GP/N	UFBGA64 N						
E4	4	3	4	6	8	D1	VDD/VDDA	S	-	-	-	-
G4	5	4	5	7	9	E1	VSS/VSSA	S	-	-	-	-
-	-	-	-	8	10	F1	PF0-OSC_IN (PF0)	I/O	FT	-	CRS_SYNC, TIM14_CH1	OSC_IN
-	-	-	-	9	11	G1	PF1-OSC_OUT (PF1)	I/O	FT	-	OSC_EN	OSC_OUT
J4	6	5	6	10	12	E2	PF2-NRST	I/O	RST, FT	(2)	MCO, TIM1_CH4	NRST
-	-	-	-	-	13	E3	PC0	I/O	FT	-	-	-
-	-	-	-	-	14	F2	PC1	I/O	FT	-	-	-
-	-	-	-	-	15	G2	PC2	I/O	FT	-	SPI2_MISO	-
-	-	-	-	-	16	H1	PC3	I/O	FT	-	SPI2_MOSI	-
J4	7	6	7	11	17	H2	PA0	I/O	FT_a	-	SPI2_SCK, USART2_CTS/USART2_NSS, TIM16_CH1, TIM2_ETR/TIM2_CH1, USART1_TX, TIM1_CH1	ADC_IN0, WKUP1
H3	8	7	8	12	18	H3	PA1	I/O	FT_a	-	SPI1_SCK/I2S1_CK, USART2_RTS/USART2_DE/ USART2_CK, TIM17_CH1, TIM2_CH2, USART1_RX, TIM1_CH2, I2C1_SMBA, EVENTOUT	ADC_IN1
L4	9	8	9	13	19	G3	PA2	I/O	FT_a	-	SPI1_MOSI/I2S1_SD, USART2_TX, TIM16_CH1N, TIM3_ETR, TIM1_CH3, TIM2_CH3	ADC_IN2, WKUP4, LSCO
K3	10	9	10	14	20	F3	PA3	I/O	FT_a	-	SPI2_MISO, USART2_RX, TIM1_CH1N, TIM2_CH4, TIM1_CH4, EVENTOUT	ADC_IN3
-	-	-	-	15	21	H4	PA4	I/O	FT_a	-	SPI1_NSS/I2S1_WS, USART2_TX, TIM1_CH2N, SPI2_MOSI, TIM14_CH1, TIM17_CH1N, USB_NOE, EVENTOUT	ADC_IN4, RTC_OUT2
J2	11	10	11	-	-	-	PA4	I/O	FT_a	-	SPI1_NSS/I2S1_WS, USART2_TX, TIM1_CH2N, SPI2_MOSI, TIM14_CH1, TIM17_CH1N, USB_NOE, EVENTOUT	ADC_IN4, RTC_TS, RTC_OUT1, WKUP2
H1	12	11	12	16	22	G4	PA5	I/O	FT_a	-	SPI1_SCK/I2S1_CK, USART2_RX, TIM1_CH3N, TIM2_ETR/TIM2_CH1, TIM1_CH1, EVENTOUT	ADC_IN5
L2	13	12	13	17	23	F4	PA6	I/O	FT_fa	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, I2C2_SDA	ADC_IN6
K1	14/-	13	14	18	24	E4	PA7	I/O	FT_fa	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1, I2C2_SCL	ADC_IN7
-	-	-	-	-	25	H5	PC4	I/O	FT_a	-	USART1_TX, TIM2_ETR/TIM2_CH1	ADC_IN11
-	-	-	-	-	26	H6	PC5	I/O	FT_a	-	USART1_RX, TIM2_CH2	ADC_IN12, WKUP5
-	-	14	15	19	27	F5	PB0	I/O	FT_a	-	SPI1_NSS/I2S1_WS, TIM3_CH3, TIM1_CH2N	ADC_IN17
-	-	15	16	20	28	G5	PB1	I/O	FT_a	-	TIM14_CH1, TIM3_CH4, TIM1_CH3N, TIM1_CH2N, EVENTOUT	ADC_IN18

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Table 12. Pin assignment and description (continued)

Pin Number[1]							Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP19 GP	TSSOP20 GP/N	UFQFPN28 GP/N	LQFP32, UFQFPN32 GP/N	LQFP48, UFQFPN48 GP/N	LQFP64 GP/N	UFBGA64 N						
-	-	-	17	21	29	H7	PB2	I/O	FT_a	-	USART1_RX, MCO2, SPI2_MISO, EVENTOUT	ADC_IN19
-	-	-	-	22	30	G6	PB10	I/O	FT_fa	-	TIM2_CH3, SPI2_SCK, I2C2_SCL	ADC_IN20
-	-	-	-	23	31	H8	PB11	I/O	FT_fa	-	SPI2_MOSI, TIM2_CH4, I2C2_SDA	ADC_IN21
-	-	-	-	24	32	G7	PB12	I/O	FT_a	-	SPI2_NSS, TIM1_BKIN2, TIM1_BKIN, EVENTOUT	ADC_IN22
-	-	-	-	25	33	G8	PB13	I/O	FT_sfa	-	SPI2_SCK, TIM1_CH1N, I2C2_SCL, EVENTOUT	-
-	-	-	-	26	34	F6	PB14	I/O	FT_s	-	SPI2_MISO, TIM1_CH2N, I2C2_SDA, EVENTOUT	-
-	-	-	-	27	35	F7	PB15	I/O	FT_s	-	SPI2_MOSI, TIM1_CH3N, EVENTOUT	RTC_REFIN
F1	15/14	16	18	28	36	F8	PA8	I/O	FT_sa	-	MCO, USART2_TX, TIM1_CH1, SPI2_NSS, CRS_SYNC, SPI2_MISO, EVENTOUT, SPI1_NSS/I2S1_WS, TIM1_CH2N, TIM1_CH3N, TIM3_CH3, TIM3_CH4, TIM14_CH1, USART1_RX, MCO2	ADC_IN8
-	-	-	19	29	37	E6	PA9	I/O	FT_sf	(3)	MCO, USART1_TX, TIM1_CH2, TIM3_ETR, SPI2_MISO, I2C1_SCL, EVENTOUT, I2C2_SCL	-
-	-	17/-	20/-	30/-	38	E7	PC6	I/O	FT_s	-	TIM3_CH1, TIM2_CH3	-
-	-	-	-	31/-	39	E5	PC7	I/O	FT_s	-	TIM3_CH2, TIM2_CH4	-
-	-	-	-	-	40/-	-	PD8	I/O	FT_s	-	SPI1_SCK/I2S1_CK	-
-	-	-	-	-	41/-	-	PD9	I/O	FT_s	-	SPI1_NSS/I2S1_WS, TIM1_BKIN2	-
-	-	-	-	-/30	-/40	E8	VSS	S	-	-	-	-
-	-/15	-/17	-/20	-/31	-/41	D8	VDDIO2	S	-	(4)	-	-
-	-	-	21	32	42	D6	PA10	I/O	FT_sf	(3)	SPI2_MOSI, USART1_RX, TIM1_CH3, MCO2, TIM17_BKIN, I2C1_SDA, EVENTOUT, I2C2_SDA	-
D1	16	18	22	33	43	C8	PA11 [PA9]	I/O	FT_usf	(3)	SPI1_MISO/I2S1_MCK, USART1_CTS/USART1_NSS, TIM1_CH4, TIM1_BKIN2, I2C2_SCL	USB_DM
B1	17	19	23	34	44	B8	PA12 [PA10]	I/O	FT_usf	(3)	SPI1_MOSI/I2S1_SD, USART1_RTS/USART1_DE/USART1_CK, TIM1_ETR, I2S_CKIN, I2C2_SDA	USB_DP
C2	18	20	24	35	45	D7	PA13	I/O	FT_sa	(5)	SWDIO, IR_OUT, USB_NOE, TIM3_ETR, USART2_RX, EVENTOUT	ADC_IN13
A2	19	21	25	36	46	C7	PA14-BOOT0	I/O	FT_sa	(5)	SWCLK, USART2_TX, EVENTOUT, SPI1_NSS/I2S1_WS, USART2_RX, TIM1_CH1, MCO2, USART1_RTS/USART1_DE/USART1_CK	ADC_IN14, BOOT0
A2	19	22	26	37	47	C6	PA15	I/O	FT_s	-	SPI1_NSS/I2S1_WS, USART2_RX, TIM1_CH1, MCO2, USART1_RTS/USART1_DE/USART1_CK, TIM2_ETR/TIM2_CH1, USB_NOE, EVENTOUT	-
-	-	-	-	-	48	A8	PC8	I/O	FT_s	-	TIM3_CH3, TIM1_CH1	-
-	-	-	-	-	49	B7	PC9	I/O	FT_s	-	TIM3_CH4, TIM1_CH2, I2S_CKIN, USB_NOE	-
-	-	-	-	38	50	A7	PD0	I/O	FT_s	-	EVENTOUT, TIM16_CH1, SPI2_NSS	-
-	-	-	-	39	51	B6	PD1	I/O	FT_s	-	EVENTOUT, TIM17_CH1, SPI2_SCK	-

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Table 12. Pin assignment and description (continued)

Pin Number[1]							Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP19 GP	TSSOP20 GP/N	UFQFPN28 GP/N	LQFP32, UFQFPN32 GP/N	LQFP48, UFQFPN48 GP/N	LQFP64 GP/N	UFBGA64 N						
-	-	-	-	40	52	A6	PD2	I/O	FT_s	-	TIM3_ETR, TIM1_CH1N	-
-	-	-	-	41	53	D5	PD3	I/O	FT_s	-	USART2_CTS/USART2_NSS, TIM1_CH2N, SPI2_MISO	-
-	-	-	-	-	54	C5	PD4	I/O	FT	-	SPI2_MOSI, USART2_RTS/USART2_DE/USART2_CK, TIM1_CH3N	-
-	-	-	-	-	55	B5	PD5	I/O	FT	-	SPI1_MISO/I2S1_MCK, USART2_TX, TIM1_BKIN	-
-	-	-	-	-	56	A5	PD6	I/O	FT	-	SPI1_MOSI/I2S1_SD, USART2_RX	-
B3	20	23	27	42	57	B4	PB3	I/O	FT_f	-	SPI1_SCK/I2S1_CK, TIM1_CH2, TIM3_CH2, USART1_RTS/USART1_DE/USART1_CK, I2C2_SCL, TIM2_CH2, EVENTOUT	-
B3	20	24	28	43	58	C4	PB4	I/O	FT_f	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, USART1_CTS/USART1_NSS, TIM17_BKIN, I2C2_SDA, EVENTOUT	-
B3	20	25	29	44	59	D4	PB5	I/O	FT	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM16_BKIN, TIM3_CH3, I2C1_SMBA	WKUP6
B3	20	26	30	45	60	A4	PB6	I/O	FT_f	-	USART1_TX, TIM1_CH3, TIM16_CH1N, TIM3_CH3, SPI2_MISO, USART1_NSS/ USART1_CTS, I2C1_SCL, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI1_MISO/I2S1_MCK, SPI1_SCK/I2S1_CK, TIM1_CH2, TIM3_CH1, TIM3_CH2, TIM16_BKIN, TIM17_BKIN	WKUP3
-	-	-	-	46	61	A3	PB7	I/O	FT_f	-	USART1_RX, TIM1_CH4, TIM17_CH1N, TIM3_CH4, SPI2_MOSI, I2C1_SDA, EVENTOUT, USART2_CTS/USART2_NSS, TIM16_CH1, TIM3_CH1, I2C1_SCL	-
D3	1	27	31	-	-	-	PB7	I/O	FT_f	-	USART1_RX, TIM1_CH4, TIM17_CH1N, TIM3_CH4, SPI2_MOSI, I2C1_SDA, EVENTOUT, USART2_CTS/USART2_NSS, TIM16_CH1, TIM3_CH1, I2C1_SCL	RTC_REFIN
D3	1	28	32	47	62	B3	PB8	I/O	FT_f	-	USART2_CTS/USART2_NSS, TIM16_CH1, TIM3_CH1, SPI2_SCK, I2C1_SCL, EVENTOUT	-
-	-	-	1	48	63	C3	PB9	I/O	FT_f	-	IR_OUT, USART2_RTS/USART2_DE/USART2_CK, TIM17_CH1, TIM3_CH2, SPI2_NSS, I2C1_SDA, EVENTOUT	-
-	-	-	-	-	64	A2	PC10	I/O	FT	-	TIM1_CH3	-

1. If a cell contains the slash separator, the information before the slash applies to the GP and the information after the slash to the N package variant.
2. RST I/O structure when the PF2-NRST pin is configured as reset (input or input/output mode), FT I/O structure when the PF2-NRST pin is configured as GPIO
3. Pins PA9 and PA10 can be remapped in place of pins PA11 and PA12 (default mapping), using SYSCFG_CFGR1 register.
4. On GP package types, the V_{DDIO2} supply line is internally connected to the VDD/VDDA pin.
5. Upon reset, this pin is configured as SWD alternate function, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.

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Table 13. Port A alternate function mapping (AF0 to AF7)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI2_SCK	USART2_CTS/ USART2_NSS	TIM16_CH1	TIM2_ETR/ TIM2_CH1	USART1_TX	TIM1_CH1	-	-
PA1	SPI1_SCK/ I2S1_CK	USART2_RTS/ USART2_DE/ USART2_CK	TIM17_CH1	TIM2_CH2	USART1_RX	TIM1_CH2	I2C1_SMBA	EVENTOUT
PA2	SPI1_MOSI/ I2S1_SD	USART2_TX	TIM16_CH1N	TIM3_ETR	-	TIM1_CH3	TIM2_CH3	-
PA3	SPI2_MISO	USART2_RX	TIM1_CH1N	TIM2_CH4	-	TIM1_CH4	-	EVENTOUT
PA4	SPI1_NSS/ I2S1_WS	USART2_TX	TIM1_CH2N	SPI2_MOSI	TIM14_CH1	TIM17_CH1N	USB_NOE	EVENTOUT
PA5	SPI1_SCK/ I2S1_CK	USART2_RX	TIM1_CH3N	TIM2_ETR/ TIM2_CH1	-	TIM1_CH1	-	EVENTOUT
PA6	SPI1_MISO/ I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	I2C2_SDA	-
PA7	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	I2C2_SCL	-
PA8	MCO	USART2_TX	TIM1_CH1	SPI2_NSS	CRS_SYNC	-	SPI2_MISO	EVENTOUT
PA9	MCO	USART1_TX	TIM1_CH2	TIM3_ETR	SPI2_MISO	-	I2C1_SCL	EVENTOUT
PA10	SPI2_MOSI	USART1_RX	TIM1_CH3	MCO2	-	TIM17_BKIN	I2C1_SDA	EVENTOUT
PA11	SPI1_MISO/ I2S1_MCK	USART1_CTS/ USART1_NSS	TIM1_CH4	-	-	TIM1_BKIN2	I2C2_SCL	-
PA12	SPI1_MOSI/ I2S1_SD	USART1_RTS/ USART1_DE/ USART1_CK	TIM1_ETR	-	-	I2S_CKIN	I2C2_SDA	-
PA13	SWDIO	IR_OUT	USB_NOE	TIM3_ETR	USART2_RX	-	-	EVENTOUT
PA14	SWCLK	USART2_TX	-	-	-	-	-	EVENTOUT
PA15	SPI1_NSS/ I2S1_WS	USART2_RX	TIM1_CH1	MCO2	USART1_RTS/ USART1_DE/ USART1_CK	TIM2_ETR/ TIM2_CH1	USB_NOE	EVENTOUT

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Table 14. Port A alternate function mapping (AF8 to AF15)

Port	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	-	-	-	-	-	-	-
PA1	-	-	-	-	-	-	-	-
PA2	-	-	-	-	-	-	-	-
PA3	-	-	-	-	-	-	-	-
PA4	-	-	-	-	-	-	-	-
PA5	-	-	-	-	-	-	-	-
PA6	-	-	-	-	-	-	-	-
PA7	-	-	-	-	-	-	-	-
PA8	SPI1_NSS/ I2S1_WS	TIM1_CH2N	TIM1_CH3N	TIM3_CH3	TIM3_CH4	TIM14_CH1	USART1_RX	MCO2
PA9	I2C2_SCL	-	-	-	-	-	-	-
PA10	I2C2_SDA	-	-	-	-	-	-	-
PA11	-	-	-	-	-	-	-	-
PA12	-	-	-	-	-	-	-	-
PA13	-	-	-	-	-	-	-	-
PA14	SPI1_NSS/ I2S1_WS	USART2_RX	TIM1_CH1	MCO2	USART1_RTS/ USART1_DE/ USART1_CK	-	-	-
PA15	-	-	-	-	-	-	-	-

Table 15. Port B alternate function mapping (AF0 to AF7)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI1_NSS/ I2S1_WS	TIM3_CH3	TIM1_CH2N	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	TIM1_CH2N	-	EVENTOUT
PB2	USART1_RX	-	-	MCO2	SPI2_MISO	-	-	EVENTOUT

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Table 15. Port B alternate function mapping (AF0 to AF7) (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB3	SPI1_SCK/ I2S1_CK	TIM1_CH2	-	TIM3_CH2	USART1_RTS/ USART1_DE/ USART1_CK	I2C2_SCL	TIM2_CH2	EVENTOUT
PB4	SPI1_MISO/ I2S1_MCK	TIM3_CH1	-	-	USART1_CTS/ USART1_NSS	TIM17_BKIN	I2C2_SDA	EVENTOUT
PB5	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM16_BKIN	TIM3_CH3	-	-	I2C1_SMBA	-
PB6	USART1_TX	TIM1_CH3	TIM16_CH1N	TIM3_CH3	SPI2_MISO	USART1_NSS/ USART1_CTS	I2C1_SCL	I2C1_SMBA
PB7	USART1_RX	TIM1_CH4	TIM17_CH1N	TIM3_CH4	SPI2_MOSI	-	I2C1_SDA	EVENTOUT
PB8	-	USART2_CTS/ USART2_NSS	TIM16_CH1	TIM3_CH1	SPI2_SCK	-	I2C1_SCL	EVENTOUT
PB9	IR_OUT	USART2_RTS/ USART2_DE/ USART2_CK	TIM17_CH1	TIM3_CH2	-	SPI2_NSS	I2C1_SDA	EVENTOUT
PB10	-	-	-	TIM2_CH3	-	SPI2_SCK	I2C2_SCL	-
PB11	SPI2_MOSI	-	-	TIM2_CH4	-	-	I2C2_SDA	-
PB12	SPI2_NSS	TIM1_BKIN2	TIM1_BKIN	-	-	-	-	EVENTOUT
PB13	SPI2_SCK	-	TIM1_CH1N	-	-	-	I2C2_SCL	EVENTOUT
PB14	SPI2_MISO	-	TIM1_CH2N	-	-	-	I2C2_SDA	EVENTOUT
PB15	SPI2_MOSI	-	TIM1_CH3N	-	-	-	-	EVENTOUT

Table 16. Port B alternate function mapping (AF8 to AF15)

Port	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	-	-	-	-	-	-	-	-
PB1	-	-	-	-	-	-	-	-
PB2	-	-	-	-	-	-	-	-

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Table 16. Port B alternate function mapping (AF8 to AF15) (continued)

Port	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB3	-	-	-	-	-	-	-	-
PB4	-	-	-	-	-	-	-	-
PB5	-	-	-	-	-	-	-	-
PB6	SPI1_MOSI/ I2S1_SD	SPI1_MISO/ I2S1_MCK	SPI1_SCK/ I2S1_CK	TIM1_CH2	TIM3_CH1	TIM3_CH2	TIM16_BKIN	TIM17_BKIN
PB7	-	USART2_CTS/ USART2_NSS	TIM16_CH1	TIM3_CH1	-	-	I2C1_SCL	-
PB8	-	-	-	-	-	-	-	-
PB9	-	-	-	-	-	-	-	-
PB10	-	-	-	-	-	-	-	-
PB11	-	-	-	-	-	-	-	-
PB12	-	-	-	-	-	-	-	-
PB13	-	-	-	-	-	-	-	-
PB14	-	-	-	-	-	-	-	-
PB15	-	-	-	-	-	-	-	-

Table 17. Port C alternate function mapping (AF0 to AF7)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	-	-	-	-	-	-	-	-
PC1	-	-	-	-	-	-	-	-
PC2	SPI2_MISO	-	-	-	-	-	-	-
PC3	SPI2_MOSI	-	-	-	-	-	-	-
PC4	-	USART1_TX	-	TIM2_ETR/ TIM2_CH1	-	-	-	-
PC5	-	USART1_RX	-	TIM2_CH2	-	-	-	-
PC6	-	TIM3_CH1	-	TIM2_CH3	-	-	-	-

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Table 17. Port C alternate function mapping (AF0 to AF7) (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC7	-	TIM3_CH2	-	TIM2_CH4	-	-	-	-
PC8	-	TIM3_CH3	TIM1_CH1	-	-	-	-	-
PC9	-	TIM3_CH4	TIM1_CH2	-	-	I2S_CKIN	USB_NOE	-
PC10	-	-	TIM1_CH3	-	-	-	-	-
PC11	-	-	TIM1_CH4	-	-	-	-	-
PC12	TIM14_CH1	-	-	-	-	-	-	-
PC13	-	TIM1_ETR	TIM1_BKIN	-	-	-	-	-
PC14	USART1_TX	TIM1_ETR	TIM1_BKIN2	-	-	-	-	-
PC15	OSC32_EN	OSC_EN	TIM1_ETR	TIM3_CH3	-	-	-	-

Table 18. Port C alternate function mapping (AF8 to AF15)

Port	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	-	-	-	-	-	-	-	-
PC1	-	-	-	-	-	-	-	-
PC2	-	-	-	-	-	-	-	-
PC3	-	-	-	-	-	-	-	-
PC4	-	-	-	-	-	-	-	-
PC5	-	-	-	-	-	-	-	-
PC6	-	-	-	-	-	-	-	-
PC7	-	-	-	-	-	-	-	-
PC8	-	-	-	-	-	-	-	-
PC9	-	-	-	-	-	-	-	-
PC10	-	-	-	-	-	-	-	-
PC11	-	-	-	-	-	-	-	-
PC12	-	-	-	-	-	-	-	-

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Table 18. Port C alternate function mapping (AF8 to AF15) (continued)

Port	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC13	-	-	-	-	-	-	-	-
PC14	IR_OUT	USART2_RTS/ USART2_DE/ USART2_CK	TIM17_CH1	TIM3_CH2	SPI2_NSS	-	I2C1_SDA	EVENTOUT
PC15	-	-	-	-	-	-	-	-

Table 19. Port D alternate function mapping (AF0 to AF7)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	EVENTOUT	-	TIM16_CH1	SPI2_NSS	-	-	-	-
PD1	EVENTOUT	-	TIM17_CH1	SPI2_SCK	-	-	-	-
PD2	-	TIM3_ETR	TIM1_CH1N	-	-	-	-	-
PD3	USART2_CTS/ USART2_NSS	-	TIM1_CH2N	SPI2_MISO	-	-	-	-
PD4	SPI2_MOSI	USART2_RTS/ USART2_DE/ USART2_CK	TIM1_CH3N	-	-	-	-	-
PD5	SPI1_MISO/ I2S1_MCK	USART2_TX	TIM1_BKIN	-	-	-	-	-
PD6	SPI1_MOSI/ I2S1_SD	USART2_RX	-	-	-	-	-	-
PD8	SPI1_SCK/ I2S1_CK	-	-	-	-	-	-	-
PD9	SPI1_NSS/ I2S1_WS	-	TIM1_BKIN2	-	-	-	-	-

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Table 20. Port F alternate function mapping (AF0 to AF7)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	CRS_SYNC	-	TIM14_CH1	-	-	-	-	-
PF1	OSC_EN	-	-	-	-	-	-	-
PF2	MCO	TIM1_CH4	-	-	-	-	-	-
PF3	-	-	-	-	-	-	-	-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

Parameter values defined at temperatures or in temperature ranges out of the ordering information scope are to be ignored.

Packages used for characterizing certain electrical parameters may differ from the commercial packages as per the ordering information.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A(max) (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = V_{DDIO2} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 12*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 13*.

Figure 12. Pin loading conditions

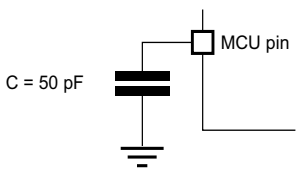
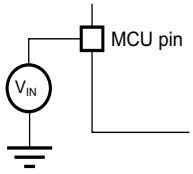


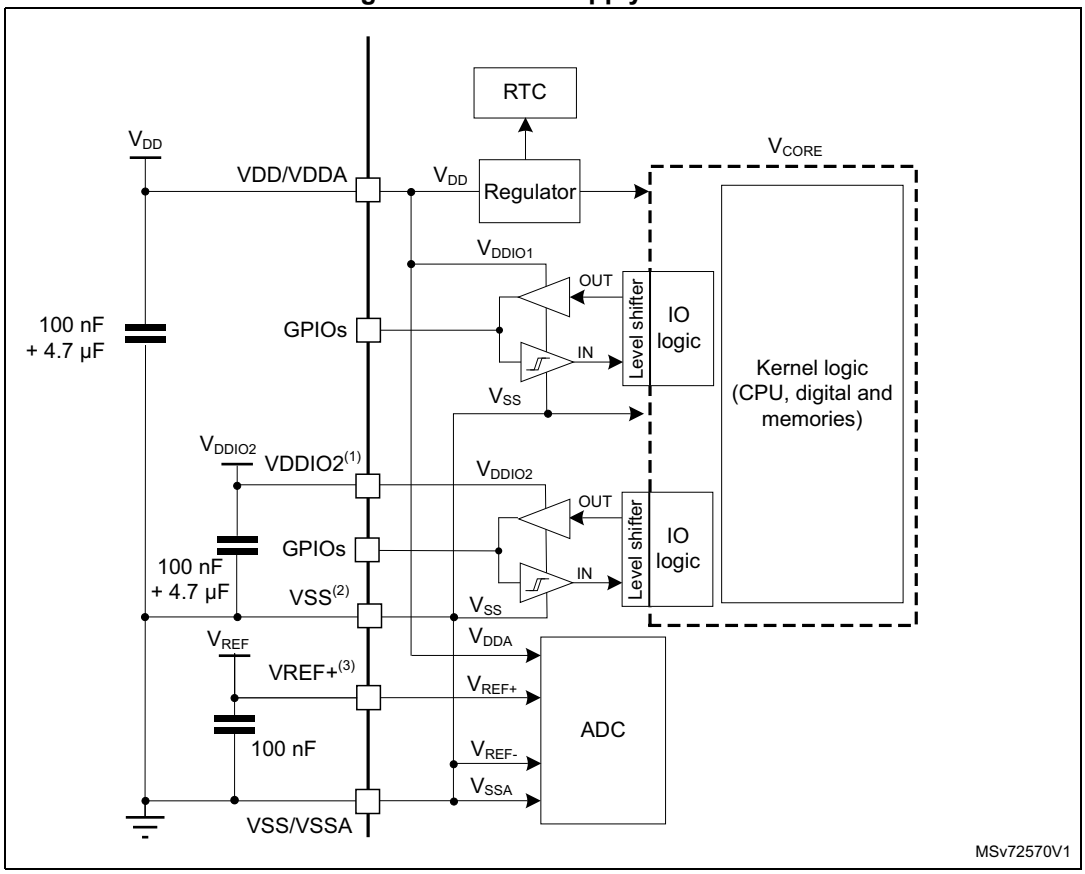
Figure 13. Pin input voltage



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5.1.6 Power supply scheme

Figure 14. Power supply scheme



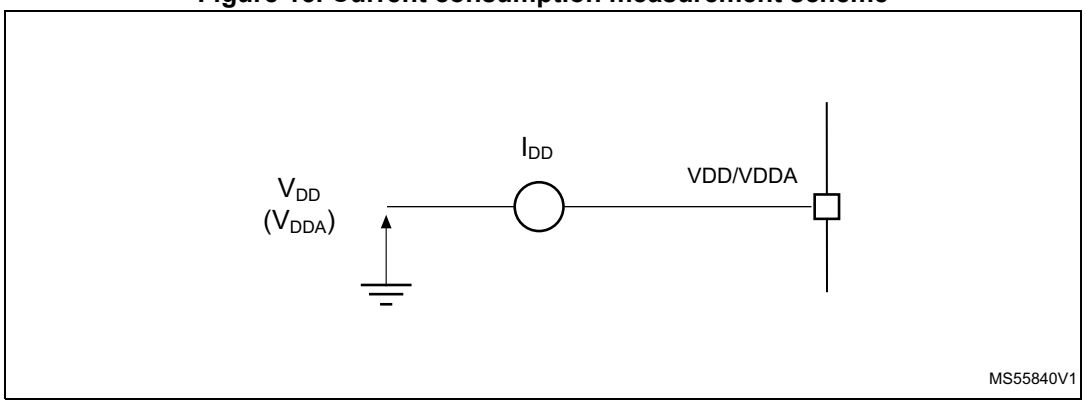
1. Internally connected to V_{DD} in devices without the VDDIO2 pin
2. Internally connected to V_{SS} in devices without the VSS pin
3. Internally connected to V_{DDA} in devices without the VREF+ pin

Caution: Power supply pin pairs (VDD/VDDA and VDDIO2 versus VSS/VSSA and VSS) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

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5.1.7 Current consumption measurement

Figure 15. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 21*, *Table 22* and *Table 23* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard.

All voltages are defined with respect to V_{SS}.

Table 21. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}	External supply voltage	- 0.3	4.0	V
V_{DDIO2}	External supply voltage for selected I/Os	- 0.3	4.0	V
V_{REF+}	External voltage on VREF+ pin	- 0.3	Min(V_{DD} + 0.4, 4.0)	V
V_{IN}(1)	Input voltage on pin	- 0.3	V_{DDIOx} + 4.0(2)(3)	V

1. V_{IN} maximum must always be respected. Refer to *Table 22* for the maximum allowed injected current values.
2. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
3. When an FT_a pin is used by an analog peripheral such as ADC, the maximum V_{IN} is 4 V.

Table 22. Current characteristics

Symbol	Ratings	Max	Unit
$I_{VDD/VDDA,VDDIO2}$	Current into VDD/VDDA and VDDIO2 power pins (source)	100	mA
$I_{VSS/VSSA}$	Current out of VSS/VSSA ground pin (sink)	100	mA
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	20	mA
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(1)	80	mA
	Total output current sourced by sum of all I/Os and control pins(1)	80	

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Table 22. Current characteristics (continued)

Symbol	Ratings	Max	Unit
$I_{INJ(PIN)}$(1)(2)	Injected current on a FT_xx pin	-5 / NA	mA
$\sum I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(3)	-25	mA

1. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
2. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	130	°C

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5.3 Operating conditions

5.3.1 General operating conditions

Table 24. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	2.0(1)	3.6	V
V_{DDIO2}	External supply voltage for selected I/Os	-	1.65	3.6	V
V_{IN}	I/O input voltage	-	-0.3	Min (V_{DDIOx} + 3.6, 5.5)(2)(3)	V
f_{HCLK}	AHB clock frequency	-	-	48	MHz
f_{PCLK}	APB clock frequency	-	-	48	MHz
T_A	Ambient temperature(4)	Suffix 6(5)	-40	85	°C
		Suffix 7(5)	-40	105	
		Suffix 3(5)	-40	125	
T_J	Junction temperature	Suffix 6(5)	-40	105	°C
		Suffix 7(5)	-40	125	
		Suffix 3(5)	-40	130	

1. When RESET is released, functionality is guaranteed down to V_{PDR}.
2. For operation with voltage higher than VDD +0.3 V, the internal pull-up and pull-down resistors must be disabled.
3. When V_{DDIO2}>V_{DD} and an FT_sa pin is used by an analog peripheral such as ADC, the maximum V_{IN} is V_{DD}+0.3V.
4. The T_A(max) applies to P_D(max). At P_D < P_D(max) the ambient temperature is allowed to go higher than T_A(max) provided that the junction temperature T_J does not exceed T_J(max). Refer to *Section 6.11: Thermal characteristics*.
5. Temperature range digit in the order code. See *Section 7: Ordering information*.

5.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 25* are derived from tests performed under the ambient temperature condition summarized in *Table 24*.

Table 25. Operating conditions at power-up / power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 26* are derived from tests performed under the ambient temperature conditions summarized in *Table 24*.

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Table 26. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$ (1)	POR temporization when V_{DD} crosses V_{POR}	V_{DD} rising	-	270	500	µs
V_{POR} (1)	Power-on reset threshold	-	1.9	1.94	1.98	V
V_{PDR} (1)	Power-down reset threshold	-	1.88	1.92	1.96	V
V_{BOR1}	Brownout reset threshold 1	V_{DD} rising	2.05	2.10	2.18	V
		V_{DD} falling	1.95	2.00	2.08	
V_{BOR2}	Brownout reset threshold 2	V_{DD} rising	2.20	2.31	2.38	V
		V_{DD} falling	2.10	2.21	2.28	
V_{BOR3}	Brownout reset threshold 3	V_{DD} rising	2.50	2.62	2.68	V
		V_{DD} falling	2.40	2.52	2.58	
V_{BOR4}	Brownout reset threshold 4	V_{DD} rising	2.80	2.91	3.00	V
		V_{DD} falling	2.70	2.81	2.90	
$V_{hyst_POR_PDR}$	Hysteresis of V_{POR} and V_{PDR}	-	-	20	-	mV
V_{hyst_BOR}	Hysteresis of V_{BORx}	-	-	100	-	mV
$I_{DD(BOR)}$ (1)	BOR consumption from V_{DD}	-	-	2.2	2.5	µA

1. Specified by design. Not tested in production.

5.3.4 Embedded voltage reference

The parameters given in *Table 27* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

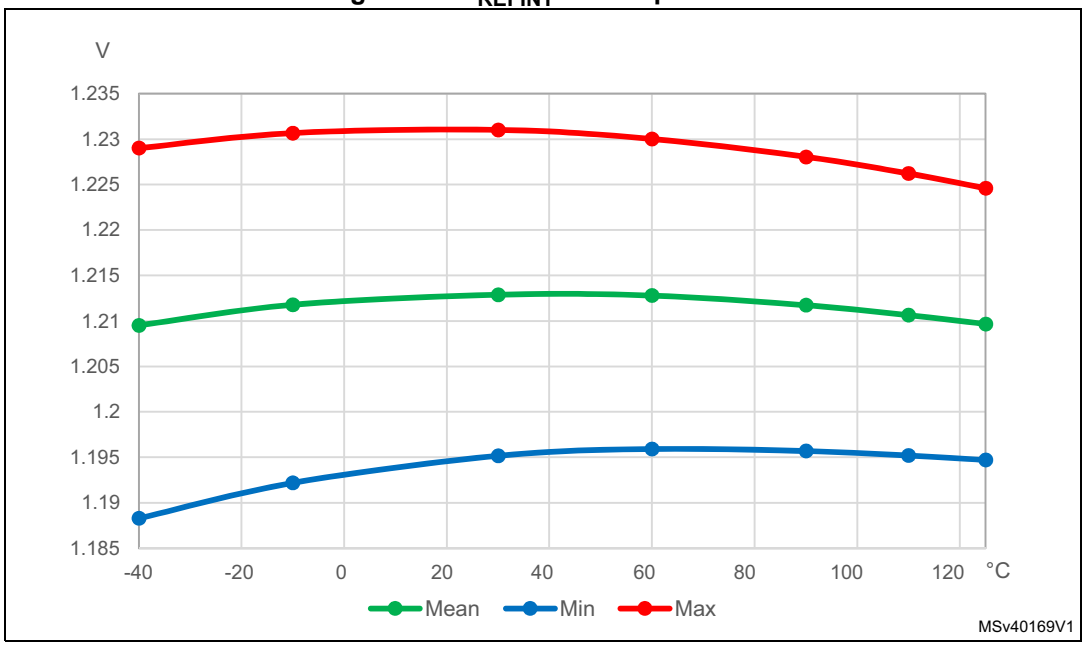
Table 27. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-	1.182	1.212	1.232	V
$t_{S_vrefint}$ (1)(2)	ADC sampling time when reading the internal reference voltage	-	4	-	-	µs
$t_{start_vrefint}$ (2)	Start time of reference voltage buffer when ADC is enable	-	-	8	12	µs
$I_{DD(VREFINTBUF)}$ (2)	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	9	13.5	23	µA
ΔV_{REFINT} (2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	30	50	mV
T_{Coeff}	Averange temperature coefficient	-	-	20	70	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25 °C	-	300	1000	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200	ppm/V

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Specified by design. Not tested in production.

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Figure 16. V_{REFINT} vs. temperature



5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 15: Current consumption measurement scheme*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0490 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- For flash memory and shared peripherals $f_{PCLK} = f_{HCLK} = f_{HCLKS}$

Unless otherwise stated, values given in *Table 28* through *Table 35* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

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Table 28. Current consumption in Run mode from flash memory at different die temperatures

Symbol	Parameter	Conditions			Typ				Max(1)				Unit
		General(2)	f_{HCLK}	Fetch from(3)	25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE_bypass}$ (> 32.768 kHz), $f_{HCLK} = f_{LSE_bypass}$ (= 32.768 kHz)	48 MHz	Flash memory	3.70	3.85	3.95	4.20	4.000	4.200	4.500	5.000	mA
			32 MHz		2.50	2.65	2.75	2.95	2.700	2.900	3.200	3.800	
			24 MHz		2.20	2.35	2.45	2.65	2.400	2.600	2.900	3.400	
			16 MHz		1.50	1.60	1.75	1.95	1.700	1.900	2.200	2.700	
			8 MHz		0.800	0.900	1.000	1.250	0.880	0.990	1.500	2.000	
			4 MHz		0.440	0.535	0.645	0.855	0.500	0.750	1.100	1.600	
			2 MHz		0.265	0.355	0.460	0.675	0.310	0.570	0.860	1.500	
			1 MHz		0.175	0.265	0.370	0.580	0.210	0.470	0.770	1.400	
			500 kHz		0.130	0.220	0.325	0.535	0.160	0.420	0.720	1.300	
			125 kHz		0.097	0.185	0.290	0.500	0.130	0.390	0.690	1.300	
			32.768 kHz		0.089	0.175	0.285	0.495	0.260	0.380	0.680	1.300	
		$f_{HCLK} = f_{HSI48/HSIDIV}$ (> 32 kHz), $f_{HCLK} = f_{LSI}$ (= 32 kHz)	48 MHz		3.90	4.00	4.10	4.30	4.200	4.300	4.500	5.000	
			24 MHz		2.50	2.60	2.70	2.90	2.700	2.800	3.100	3.600	
			12 MHz		1.50	1.60	1.70	1.90	1.600	1.800	2.100	2.600	
			6 MHz		1.00	1.05	1.15	1.35	1.000	1.300	1.600	2.100	
			3 MHz		0.740	0.800	0.900	1.10	0.770	0.990	1.300	1.900	
			1.5 MHz		0.610	0.670	0.770	0.970	0.640	0.870	1.200	1.700	
			750 kHz		0.545	0.605	0.705	0.905	0.570	0.800	1.100	1.700	
			375 kHz		0.515	0.575	0.675	0.875	0.540	0.770	1.100	1.600	
			32 kHz		0.089	0.175	0.285	0.495	0.120	0.380	0.680	1.300	
		$f_{HCLK} = f_{HSIUSB48/SYSDIV}$	48 MHz		3.900	4.050	4.200	4.400	4.200	4.300	4.600	5.100	
			24 MHz		2.000	2.100	2.250	2.450	2.100	2.300	2.600	3.200	

1. Evaluated by characterization. Not tested in production.
2. V_{DD} = 3.0 V for values in Typ columns and 3.6 V for values in Max columns, all peripherals disabled.
3. Prefetch disabled and cache enabled when fetching from flash memory.

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Table 29. Current consumption in Run mode from SRAM at different die temperatures

Symbol	Parameter	Conditions			Typ				Max[1]				Unit
		General[2]	f_{HCLK}	Fetch from[3]	25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE_bypass}$ (>32.768 kHz), $f_{HCLK} = f_{LSE_bypass}$ (=32.768 kHz)	48 MHz	SRAM	3.10	3.20	3.35	3.55	3.40	3.60	3.80	4.30	mA
			32 MHz		2.10	2.20	2.30	2.55	2.30	2.50	2.80	3.30	
			24 MHz		1.60	1.70	1.80	2.00	1.80	2.00	2.20	2.80	
			16 MHz		1.100	1.20	1.30	1.50	1.20	1.40	1.70	2.30	
			8 MHz		0.590	0.680	0.790	1.000	0.65	0.89	1.20	1.80	
			4 MHz		0.340	0.425	0.535	0.745	0.39	0.64	0.94	1.50	
			2 MHz		0.210	0.300	0.405	0.615	0.25	0.51	0.81	1.40	
			1 MHz		0.150	0.235	0.345	0.555	0.18	0.44	0.74	1.30	
			500 kHz		0.115	0.205	0.310	0.520	0.15	0.41	0.71	1.30	
			125 kHz		0.094	0.180	0.290	0.495	0.120	0.39	0.68	1.30	
			32.768 kHz		0.088	0.175	0.285	0.490	0.120	0.38	0.68	1.30	
		$f_{HCLK} = f_{HSI48/HSIDIV}$ (> 32 kHz), $f_{HCLK} = f_{LSI}$ (= 32 kHz)	48 MHz		3.35	3.40	3.45	3.65	3.600	3.60	3.90	4.40	
			24 MHz		1.90	1.95	2.05	2.25	2.000	2.20	2.50	3.00	
			12 MHz		1.20	1.25	1.35	1.55	1.300	1.50	1.80	2.30	
			6 MHz		0.840	0.895	1.00	1.20	0.870	0.96	1.40	2.00	
			3 MHz		0.660	0.720	0.815	1.000	0.690	0.90	1.20	1.80	
			1.5 MHz		0.570	0.630	0.730	0.930	0.600	0.82	1.20	1.70	
			750 kHz		0.525	0.585	0.685	0.885	0.550	0.78	1.10	1.70	
			375 kHz		0.505	0.565	0.665	0.865	0.530	0.76	1.10	1.60	
			32 kHz		0.088	0.175	0.285	0.490	0.120	0.38	0.68	1.30	
		$f_{HCLK} = f_{HSIUSB48/SYSDIV}$	48 MHz		3.350	3.450	3.550	3.750	3.600	3.70	3.90	4.40	
			24 MHz		1.600	1.700	1.800	2.000	1.700	1.90	2.20	2.70	

1. Evaluated by characterization. Not tested in production.
2. V_{DD} = 3.0 V for values in Typ columns and 3.6 V for values in Max columns, all peripherals disabled.
3. Code compiled with high optimization for space in SRAM.

Table 30. Typical current consumption in Run depending on code executed

Symbol	Parameter	Conditions			Typ	Unit	Typ	Unit
		General(1)	Code	Fetch from(2)	25 °C		25 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE_bypass}$ = 48 MHz	Reduced code	Flash memory	4.00	mA	83.3	µA/MHz
			Coremark		3.70		77.1	
			Dhrystone		3.80		79.2	
			Fibonacci		3.00		62.5	
			WhileLoop		1.90		39.6	
			Reduced code	SRAM	3.10		64.6	
			Coremark		3.00		62.5	
			Dhrystone		2.95		61.5	
			Fibonacci		3.20		66.7	
			WhileLoop		2.30		47.9	
		$f_{HCLK} = f_{HSE_bypass}$ = 16 MHz	Reduced code	Flash memory	1.50		93.8	
			Coremark		1.35		84.4	
			Dhrystone		1.40		87.5	
			Fibonacci		1.050		65.6	
			WhileLoop		0.685		42.8	
			Reduced code	SRAM	1.100		68.8	
			Coremark		1.050		65.6	
			Dhrystone		1.050		65.6	
			Fibonacci		1.10		68.8	
			WhileLoop		0.815		50.9	
		$f_{HCLK} = f_{HSE_bypass}$ = 2 MHz	Reduced code	Flash memory	0.265		132.5	
			Coremark		0.245		122.5	
			Dhrystone		0.245		122.5	
			Fibonacci		0.205		102.5	
			WhileLoop		0.160		80.0	
			Reduced code	SRAM	0.210		105.0	
			Coremark		0.205		102.5	
			Dhrystone		0.205		102.5	
			Fibonacci		0.215		107.5	
			WhileLoop		0.175		87.5	

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Table 30. Typical current consumption in Run depending on code executed (continued)

Symbol	Parameter	Conditions			Typ	Unit	Typ	Unit
		General(1)	Code	Fetch from(2)	25 °C		25 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSI48/HSIDIV}$ = 48 MHz (HSIDIV = 1)	Reduced code	Flash memory	4.25	mA	88.5	µA/MHz
			Coremark		3.90		81.3	
			Dhrystone		4.00		83.3	
			Fibonacci		3.20		66.7	
			WhileLoop		2.15		44.8	
			Reduced code	SRAM	3.35		69.8	
			Coremark		3.20		66.7	
			Dhrystone		3.20		66.7	
			Fibonacci		3.40		70.8	
			WhileLoop		2.50		52.1	
		$f_{HCLK} = f_{HSI48/HSIDIV}$ = 12 MHz (HSIDIV = 4)	Reduced code	Flash memory	1.50		125.0	
			Coremark		1.40		116.7	
			Dhrystone		1.40		116.7	
			Fibonacci		1.15		95.8	
			WhileLoop		0.89		73.8	
			Reduced code	SRAM	1.20		100.0	
			Coremark		1.15		95.8	
			Dhrystone		1.15		95.8	
			Fibonacci		1.20		100.0	
			WhileLoop		0.99		82.1	
		$f_{HCLK} = f_{HSI48/HSIDIV}$ = 3 MHz (HSIDIV = 16)	Reduced code	Flash memory	0.735		245.0	
			Coremark		0.710		236.7	
			Dhrystone		0.710		236.7	
			Fibonacci		0.650		216.7	
			WhileLoop		0.585		195.0	
			Reduced code	SRAM	0.660		220.0	
			Coremark		0.650		216.7	
			Dhrystone		0.650		216.7	
			Fibonacci		0.665		221.7	
			WhileLoop		0.610		203.3	

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Table 30. Typical current consumption in Run depending on code executed (continued)

Symbol	Parameter	Conditions			Typ	Unit	Typ	Unit
		General(1)	Code	Fetch from(2)	25 °C		25 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSIUSB48}$	Reduced code	Flash memory	4.250	mA	88.5	µA/MHz
			Coremark		3.900		81.3	
			Dhrystone		4.000		83.3	
			Fibonacci		3.200		66.7	
			WhileLoop		2.100		43.8	
			Reduced code	SRAM	3.350		69.8	
			Coremark		3.200		66.7	
			Dhrystone		3.200		66.7	
			Fibonacci		3.400		70.8	
			WhileLoop		2.500		52.1	

1. V_{DD} = 3.0 V, all peripherals disabled
2. Prefetch and cache enabled when fetching from flash

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Table 31. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ				Max(1)				Unit
		General			25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	All peripherals disabled, $f_{HCLK} = f_{HSE_bypass}$ (> 32.768 kHz), $f_{HCLK} = f_{LSE_bypass}$ (= 32.768 kHz)	Flash memory enabled	48 MHz	0.770	0.865	0.975	1.20	0.97	1.30	1.60	2.1	mA
				32 MHz	0.540	0.635	0.745	0.960	0.73	0.96	1.30	1.8	
				24 MHz	0.425	0.520	0.630	0.840	0.58	0.81	1.20	1.7	
				16 MHz	0.315	0.405	0.510	0.725	0.42	0.67	0.96	1.6	
				8 MHz	0.200	0.290	0.395	0.605	0.27	0.52	0.82	1.4	
				4 MHz	0.145	0.230	0.340	0.550	0.20	0.46	0.76	1.3	
				2 MHz	0.115	0.200	0.310	0.520	0.16	0.42	0.72	1.3	
				1 MHz	0.1	0.190	0.295	0.505	0.14	0.40	0.69	1.3	
				500 kHz	0.093	0.180	0.285	0.495	0.13	0.39	0.68	1.3	
				125 kHz	0.088	0.175	0.280	0.490	0.12	0.38	0.68	1.3	
				32,768 Hz	0.086	0.175	0.280	0.490	0.12	0.38	0.67	1.3	
			Flash memory disabled (flash memory power-down sleep mode)	48 MHz	0.765	0.860	0.970	1.20	0.96	1.30	1.60	2.1	
				32 MHz	0.535	0.630	0.740	0.955	0.72	0.95	1.30	1.8	
				24 MHz	0.420	0.515	0.620	0.835	0.57	0.81	1.10	1.7	
				16 MHz	0.305	0.395	0.505	0.715	0.42	0.66	0.96	1.5	
				8 MHz	0.195	0.280	0.390	0.600	0.27	0.52	0.81	1.4	
				4 MHz	0.135	0.225	0.330	0.540	0.19	0.45	0.75	1.3	
				2 MHz	0.110	0.195	0.300	0.510	0.15	0.41	0.71	1.3	
				1 MHz	0.094	0.180	0.285	0.495	0.13	0.40	0.69	1.3	
				500 kHz	0.087	0.175	0.280	0.490	0.12	0.38	0.68	1.3	
				125 kHz	0.081	0.170	0.275	0.485	0.11	0.37	0.67	1.3	
				32,768 Hz	0.08	0.165	0.275	0.485	0.11	0.37	0.67	1.3	

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Table 31. Current consumption in Sleep mode (continued)

Symbol	Parameter	Conditions			Typ				Max(1)				Unit
		General		f_{HCLK}	25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	All peripherals disabled, $f_{HCLK} = f_{HSI48/HSIDIV}$ (> 32 kHz), $f_{HCLK} = f_{LSI}$ (= 32 kHz)	Flash memory enabled	48 MHz	1.00	1.05	1.15	1.35	1.20	1.40	1.70	2.2	mA
				24 MHz	0.74	0.80	0.90	1.10	0.83	1.10	1.40	1.9	
				12 MHz	0.61	0.67	0.77	0.97	0.67	0.90	1.20	1.8	
				6 MHz	0.55	0.61	0.71	0.91	0.59	0.81	1.10	1.7	
				3 MHz	0.52	0.58	0.67	0.88	0.55	0.78	1.10	1.6	
				1.5 MHz	0.50	0.56	0.66	0.86	0.53	0.76	1.10	1.6	
				750 kHz	0.50	0.55	0.65	0.85	0.52	0.75	1.10	1.6	
				375 kHz	0.49	0.55	0.65	0.85	0.51	0.74	1.10	1.6	
				32 kHz	0.09	0.18	0.28	0.49	0.12	0.38	0.67	1.3	
		$f_{HCLK} = f_{HSIUSB48/SYSDIV}$		48MHz	0.98	1.10	1.20	1.40	1.20	1.40	1.70	2.2	
				16MHz	0.80	0.90	1.00	1.20	0.87	1.20	1.40	2.0	

1. Evaluated by characterization. Not tested in production.

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Table 32. Current consumption in Stop mode

Symbol	Parameter	Conditions	V_{DD}	Typ				Max(1)				Unit
				25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Stop)}$	Supply current in Stop mode	All clocks off	2 V	82.5	170	275	485	110	360	650	1200	µA
			2.4 V	84.0	170	275	485	120	360	650	1200	
			3 V	85.5	175	280	490	120	360	650	1200	
			3.6 V	87.5	175	285	495	120	360	650	1200	
		All clocks off Flash memory in power-down stop mode	2 V	76.5	165	265	480	110	360	640	1200	
			2.4 V	78.0	165	265	480	110	360	640	1200	
			3 V	79.5	165	270	480	110	360	640	1200	
			3.6 V	81.0	170	275	485	110	360	640	1200	
		RTC enabled and supplied with LSE bypass (32.768 kHz)	2 V	83.0	170	275	485	110	360	650	1200	
			2.4 V	84.5	170	275	485	120	360	650	1200	
			3 V	86.0	175	280	490	120	360	650	1200	
			3.6 V	89.0	180	285	500	120	360	650	1200	
		RTC enabled and supplied with LSE bypass (32.768 kHz) Flash memory in power-down stop mode	2 V	76.5	165	265	480	110	360	650	1200	
			2.4 V	78.0	165	270	480	110	360	650	1200	
			3 V	79.5	165	275	485	110	360	650	1200	
			3.6 V	83.0	170	280	490	110	360	650	1200	
		HSI Kernel on	2 V	455	515	615	815	480	710	980	1500	
			2.4 V	455	515	615	815	490	710	980	1500	
			3 V	460	520	615	820	490	710	980	1500	
			3.6 V	460	520	620	825	490	710	980	1500	

1. Evaluated by characterization. Not tested in production.

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Table 33. Current consumption in Standby mode

Symbol	Parameter	Conditions	V_{DD}	Typ				Max(1)				Unit
				25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Standby)}$	Supply current in Standby mode	All clocks off	2 V	6.65	8.00	9.40	13.5	7.7	9.4	11.8	18.2	µA
			2.4 V	6.95	8.40	9.90	14.0	8.0	9.8	12.3	18.9	
			3 V	7.35	8.75	10.50	15.5	8.4	10.2	12.9	19.9	
			3.6 V	7.75	9.50	12.0	18.5	9.5	11.6	14.6	22.5	
		IWDG enabled and clocked by LSI	2 V	7.20	8.70	10.00	14.0	8.3	10.1	12.8	19.6	
			2.4 V	7.50	9.05	10.50	14.5	8.5	10.4	13.1	20.1	
			3 V	7.90	9.45	11.5	16.5	9.0	11.0	13.8	21.3	
			3.6 V	8.40	10.50	12.5	19.0	11.0	13.4	16.9	26.0	

1. Evaluated by characterization. Not tested in production.

Table 34. Current consumption in Shutdown mode

Symbol	Parameter	Conditions	V_{DD}	Typ				Max(1)				Unit
				25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Shutdown)}$	Supply current in Shutdown mode	All clocks off	2 V	12.00	515	1650	5250	82.0	1300	4100	11500	nA
			2.4 V	16.0	580	1850	5800	89.0	1350	4300	11700	
			3.0 V	23.0	720	2250	6950	91.0	1500	4600	12400	
			3.6 V	41.0	1000	3100	9300	130.0	1900	5800	16700	

1. Evaluated by characterization. Not tested in production.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up or pull-down resistor generate current consumption when the pin is externally held low or high, respectively. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 51: I/O static characteristics*.

For the output pins, any pull-up or pull-down device (internal and external) and external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 35: Current consumption of peripherals*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal and external) of the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

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On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 21: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 35. Current consumption of peripherals

Peripheral	Bus	Consumption in µA/MHz
IOPORT bus	IOPORT	0.1
GPIOA		1.5
GPIOB		1.5
GPIOC		1.5
GPIOD		1.5
GPIOF		0.7
Bus matrix	AHB	0.3
All AHB peripherals		8.5
DMA1		3.2
FLASH		4.4
SRAM1		0.5
CRC1		0.5

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Table 35. Current consumption of peripherals (continued)

Peripheral	Bus	Consumption in µA/MHz
All APB peripherals	APB	39.1
AHB to APB bridge (2)		0.3
TIM3		3.6
RTCAPB		1.2
CRS		0.5
WWDG1		0.4
USART2		1.9
I2C1		0.9
I2C1 independent clock domain		2.5
I2C2		0.8
DBGMCU1		0.1
PWR		0.3
SYSCFG		0.5
TIM1		6.0
TIM2		4.8
SPI1		2.2
SPI1 independent clock domain		0.7
SPI2		1.7
USART1		2.4
USART1 independent clock domain		5.2
TIM14		1.4
TIM16		2.8
TIM17		2.7
ADC1		1.4
ADC1 independent clock domain		0.1
USB		4.0
All peripherals		65.4

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5.3.6 Wake-up time from low-power modes

The wake-up times given in *Table 36* are the latency between the event and the execution of the first user instruction.

Table 36. Low-power mode wake-up times

Symbol	Parameter[1]	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up time from Sleep to Run mode	HCLK = HSI48/4 = 12 MHz	Transiting to Run-mode execution in flash memory powered during Sleep mode	10	12	CPU clock cycles
			Transiting to Run-mode execution in flash memory not powered during Sleep mode	4.74	5.02	µs
$t_{WULPSTOP}$	Wake-up time from Stop mode	Clock after wake-up is HCLK = HSI48/4 = 12 MHz	Transiting to Run-mode execution in flash memory powered during Stop mode	2.7	3.1	µs
			Transiting to Run-mode execution in flash memory not powered during Stop mode	5.9	6.4	
			Transiting to Run-mode execution in SRAM	2.5	2.9	
t_{WUSTBY}	Wake-up time from Standby mode	Clock after wake-up is HCLK = HSI48/4 = 12 MHz	Transiting to Run mode	23.0	35.0	
t_{WUSHDN}	Wake-up time from Shutdown mode	Clock after wake-up is HCLK = HSI48/4 = 12 MHz	Transiting to Run mode	385.0	466.0	

1. Evaluated by characterization. Not tested in production.

5.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 5.3.13*. See *Figure 17* for recommended clock input waveform.

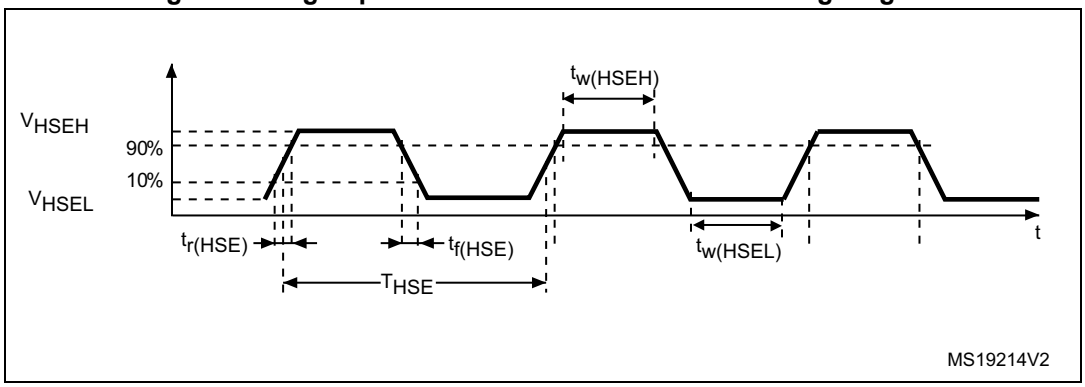
Table 37. High-speed external user clock characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	-	8	48	MHz
V_{HSEH}	Digital OSC_IN input pin high level voltage	-	$0.7 \times V_{DD}$	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3 \times V_{DD}$	
$t_{w(HSEH)}$/ $t_{w(HSEL)}$	Digital OSC_IN high or low time	-	7	-	-	ns

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1. Specified by design. Not tested in production.

Figure 17. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

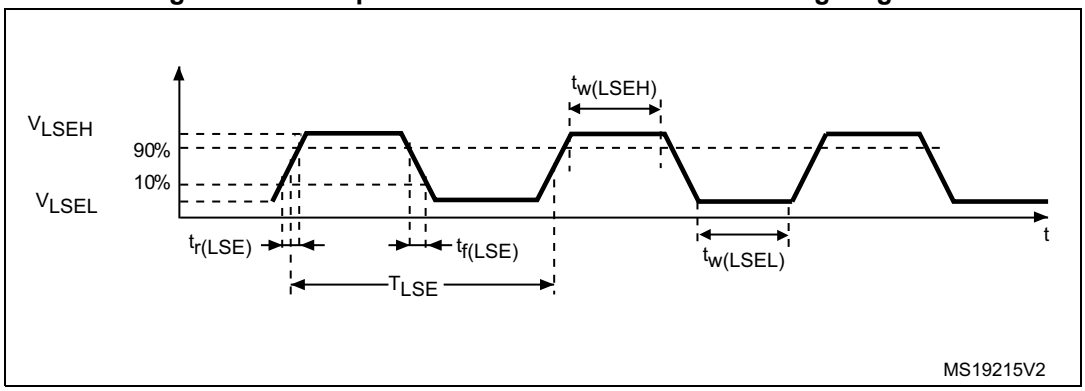
The external clock signal has to respect the I/O characteristics in *Section 5.3.13*. See *Figure 18* for recommended clock input waveform.

Table 38. Low-speed external user clock characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 × V_{DDIO1}	-	V_{DDIO1}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 × V_{DDIO1}	
$t_{w(LSEH)}$/ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Specified by design. Not tested in production.

Figure 18. Low-speed external clock source AC timing diagram



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High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 39. HSE oscillator characteristics

Symbol	Parameter[1]	Conditions[2]	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup[3]	-	-	13	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.62	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.67	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	1.15	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	1.75	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	5.0	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$[4]	Startup time	V_{DD} is stabilized	-	2	-	ms

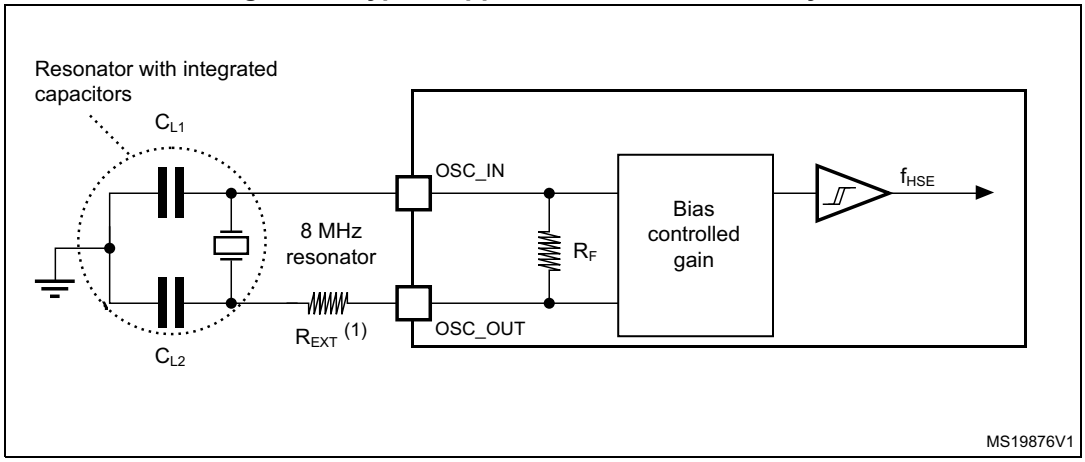
1. Specified by design. Not tested in production.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 19*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

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Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 19. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

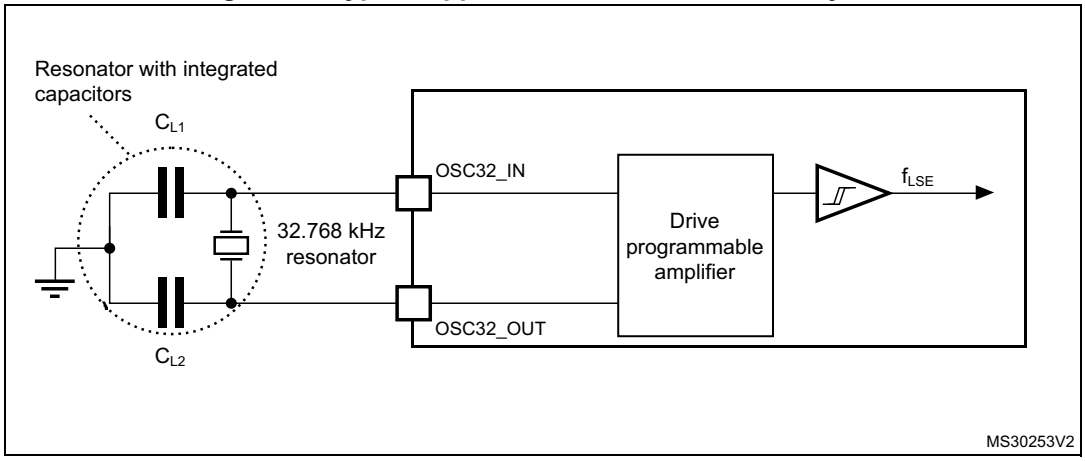
Symbol	Parameter	Conditions(1)	Min(2)	Typ(2)	Max(2)	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV = 0 Medium high drive capability	-	500	-	nA
		LSEDRV = 1 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV = 0 Medium high drive capability	-	-	1.7	µA/V
		LSEDRV = 1 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
2. Specified by design. Not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

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Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 20. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

5.3.8 Internal clock source characteristics

The parameters given in *Table 41* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI48) RC oscillator

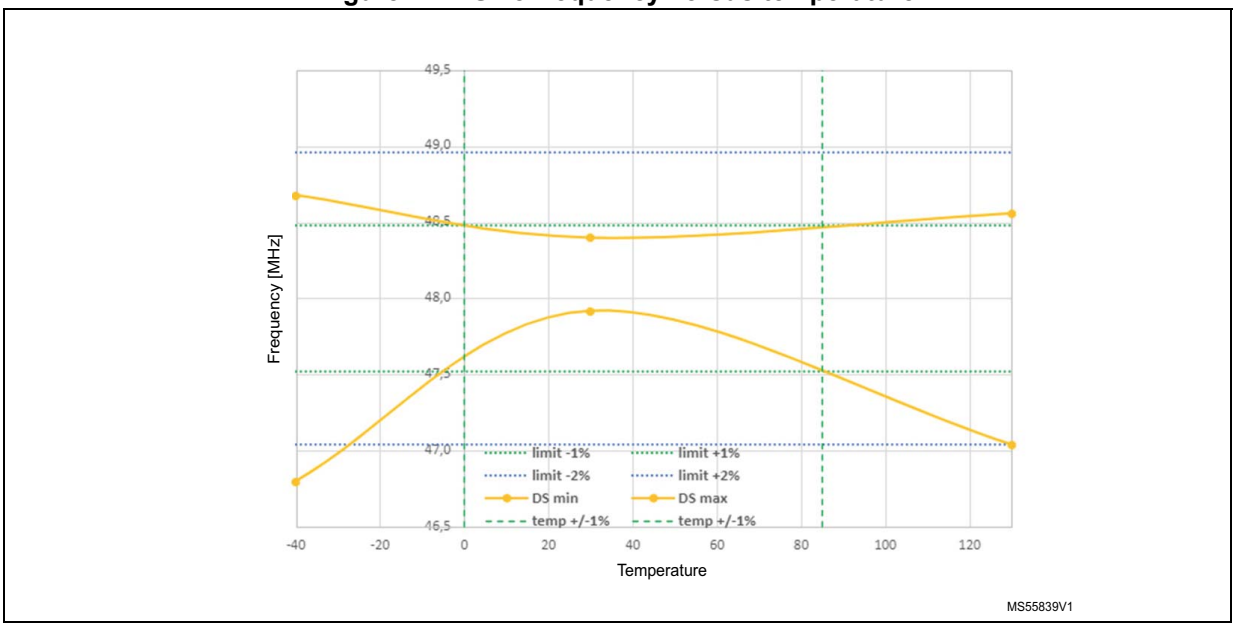
Table 41. HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0 V, T_A=30 °C	47.92	-	48.40	MHz
$\Delta_{Temp(HSI)}$(1)	HSI48 oscillator frequency drift over temperature and V_{DD} full voltage range	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2.5	-	2	%
TRIM(1)	HSI48 oscillator frequency user trimming step	From code 127 to 128	-8	-6	-4	%
		From code 63 to 64 From code 191 to 192	-5.8	-3.8	-1.8	
		For all other code increments	0.2	0.3	0.4	
D_{HSI48}(2)	Duty cycle	-	45	-	55	%
$t_{su(HSI48)}$(2)	HSI48 oscillator start-up time	-	-	1.4	1.8	µs
$t_{stab(HSI48)}$(2)	HSI48 oscillator stabilization time	at 1% of target frequency	-	1.5	3.6	µs
$I_{DD(HSI48)}$(1)	HSI48 oscillator power consumption	-	-	525	570	µA

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1. Based on characterization results, not tested in production
2. Specified by design. Not tested in production.

Figure 21. HSI48 frequency versus temperature



High-speed internal USB (HSIUSB48) oscillator

Table 42. HSIUSB48 oscillator characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$f_{HSIUSB48}$	HSIUSB48 frequency	V_{DD} = 3.0 V, T_A = 30 °C	-	48	-	MHz
TRIM	HSIUSB48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSIUSB48 user trimming coverage	±64 steps	±6(3)	±7(3)	-	%
$DuCy_{(HSIUSB48)}$	Duty cycle	-	45(2)	-	55(2)	%
$ACC_{HSIUSB48_REL}$	Accuracy of the HSIUSB48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V T_A = -15 to 85 °C	-	-	±3	%
		V_{DD} = 2.0 V to 3.6 V T_A = -40 to 125 °C	-	-	±4.5(3)	
$DV_{DD(HSIUSB48)}$	HSIUSB48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 2.0 V to 3.6 V	-	0.05(3)	0.1(3)	
$t_{su(HSIUSB48)}$	HSIUSB48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
$I_{DD(HSIUSB48)}$	HSIUSB48 oscillator power consumption	-	-	340(2)	380(2)	µA

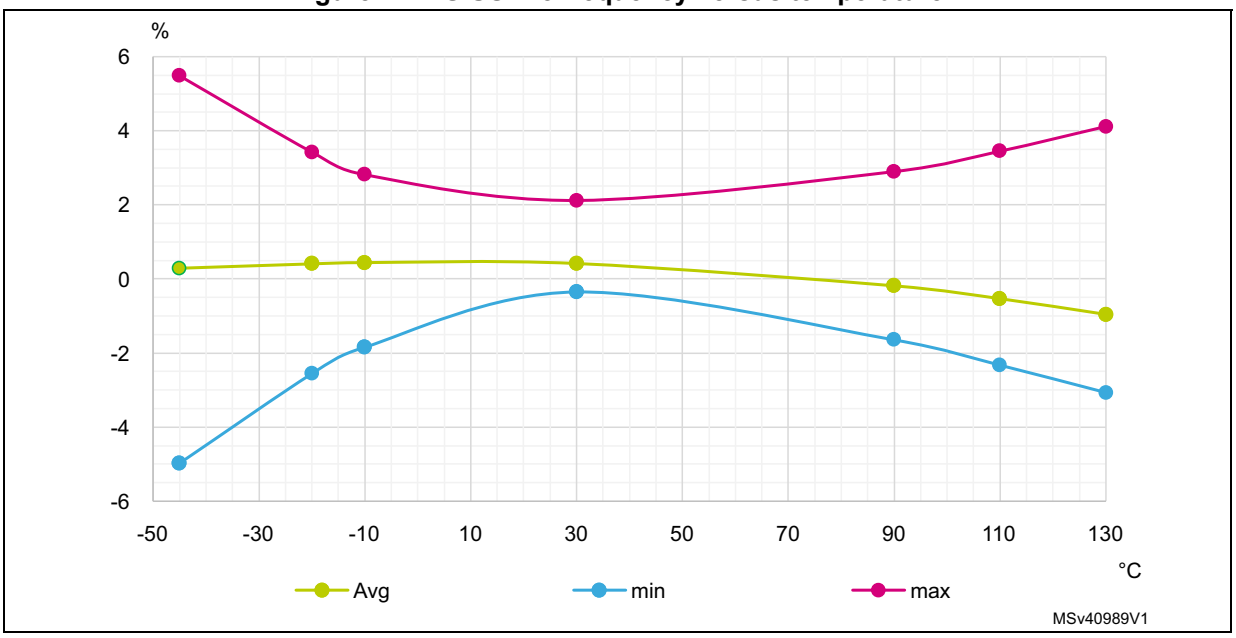
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Table 42. HSIUSB48 oscillator characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
NT jitter	Next transition jitter Accumulated jitter on 28 cycles[4]	-	-	±0.15[2]	-	ns
PT jitter	Paired transition jitter Accumulated jitter on 56 cycles[4]	-	-	±0.25[2]	-	ns

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C, unless otherwise specified.
2. Specified by design. Not tested in production.
3. Evaluated by characterization. Not tested in production.
4. Jitter measurement is performed without clock source activated in parallel.

Figure 22. HSIUSB48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.3 V, T_A = 25 °C	31.04	32	32.96	kHz
		V_{DD} = 2 V to 3.6 V, T_A = -40 to 125 °C	29.5[1]	-	34[1]	
$t_{SU(LSI)}$[2]	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB(LSI)}$[2]	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD(LSI)}$[2]	LSI oscillator power consumption	-	-	110	180	nA

1. Evaluated by characterization. Not tested in production.
2. Specified by design. Not tested in production.

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5.3.9 Flash memory characteristics

Table 44. Flash memory characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
t_{prog}	Word programming time	64 bits	-	85.0	125.0	µs
t_{prog_row}	Row (32 double word) programming time	Normal programming	-	2.7	4.6	ms
		Fast programming	-	1.7	2.8	
t_{prog_page}	Page (2 Kbyte) programming time	Normal programming	-	21.8	36.6	
		Fast programming	-	13.7	22.4	
t_{ERASE}	Page (2 Kbyte) erase time	-	-	22.0	40.0	
t_{prog_bank}	Bank (128 Kbyte[2]) programming time	Normal programming	-	1.4	2.4	s
		Fast programming	-	0.9	1.4	
t_{ME}	Mass erase time	-	-	22.1	40.1	ms
$I_{DD(FlashA)}$	Average consumption from V_{DD}	Programming	-	3.0	-	mA
		Page erase	-	3.0	-	
		Mass erase	-	5.0	-	
$I_{DD(FlashP)}$	Maximum current (peak)	Programming, 2 µs peak duration	-	7.0	-	mA
		Erase, 41 µs peak duration	-	7.0	-	

1. Specified by design. Not tested in production.
2. Values provided also apply to devices with less flash memory than one 128 Kbyte bank

Table 45. Flash memory endurance and data retention

Symbol	Parameter[1]	Conditions	Min	Unit
N_{END}	Endurance	T_J = -40 to +130 °C	10	kcycles
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	30	Years
		1 kcycle[2] at T_A = 105 °C	15	
		1 kcycle[2] at T_A = 125 °C	7	
		10 kcycles[2] at T_A = 55 °C	30	
		10 kcycles[2] at T_A = 85 °C	15	
		10 kcycles[2] at T_A = 105 °C	10	

1. Evaluated by characterization. Not tested in production..
2. Cycling performed over the whole temperature range.

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5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 46*. They are based on the EMS levels and classes defined in application note AN1709.

Table 46. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HSE} = f_{HCLK} = 48 MHz, LQFP64, conforming to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HSE} = f_{HCLK} = 48 MHz, LQFP64, conforming to IEC 61000-4-2	4B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- corrupted program counter
- unexpected reset
- critical data corruption (for example control registers)

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Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

The following table gives the EMI characteristics for f_{HSI48} and f_{HCLK} of 48 MHz.

Table 47. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				48 MHz / 48 MHz	
S_{EMI}	Peak(1)	V_{DD} = 3.6 V, T_A = 25 °C, LQFP48 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	1	dBµV
			30 MHz to 130 MHz	5	
			130 MHz to 1 GHz	10	
			1 GHz to 2 GHz	7	
	Level(2)		0.1 MHz to 2 GHz	2	-

1. Refer to AN1709, section *EMI radiated test*
2. Refer to AN1709, section *EMI level classification*

5.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

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Table 48. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-002	C2a	500	

1. Evaluated by characterization. Not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current is injected to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 49. Electrical sensitivity

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78	II Level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter: ADC error above a certain limit (higher than 5 LSB TUE), induced leakage current on adjacent pins out of conventional limits (-5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

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Table 50. I/O current injection susceptibility

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}	Injected current on pin	Any IO	5(1)	NA	mA

1. Evaluated by characterization. Not tested in production.

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under the conditions summarized in *Table 24: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

For information on GPIO configuration, refer to the application note AN4899 *STM32 GPIO configuration for hardware settings and low-power consumption*, available on the ST website www.st.com.

Table 51. I/O static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage	All	1.65 V < V_{DDIOx} < 3.6 V	-	-	0.3 × V_{DDIOx}	V
V_{IH}(1)	I/O input high level voltage	All	1.65 V < V_{DDIOx} < 3.6 V	0.7 × V_{DDIOx}	-	-	V
V_{hys}(2)	I/O input hysteresis	-		-	200	-	mV
I_{lkg}(3)	Input leakage current(3)	FT_u	0 < V_{IN} ≤ V_{DDIOx}	-	-	±150	nA
			V_{DDIOx} ≤ V_{IN} ≤ V_{DDIOx} +1 V	-	-	2500	
			V_{DDIOx} + 1 V ≤ V_{IN}	-	-	250	
		Other FT_xx	0 < V_{IN} ≤ V_{DDIOx}	-	-	±70	
			V_{DDIOx} ≤ V_{IN} ≤ V_{DDIOx} +1 V	-	-	600	
			V_{DDIOx} + 1 V ≤ V_{IN}	-	-	150	
R_{PU}	Weak pull-up equivalent resistor (4)	V_{IN} = V_{SS}		25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	V_{IN} = V_{DDIOx}		25	40	55	kΩ
C_{IO}	I/O pin capacitance	-		-	5	-	pF

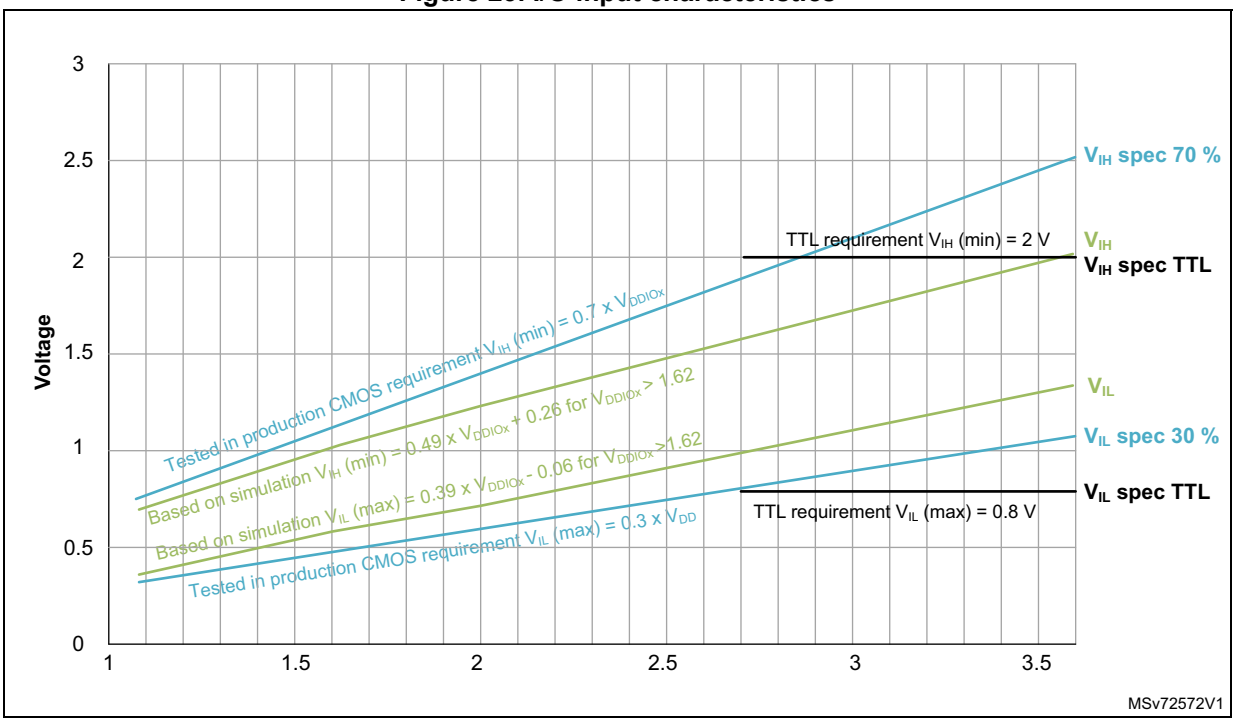
1. Refer to *Figure 23: I/O input characteristics*.
2. Specified by design. Not tested in production.
3. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: ITotal_Ileak_max = 10 µA + [number of I/Os where VIN is applied on the pad] × Ilkg(Max).

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4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters, as shown in *Figure 23*.

Figure 23. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±6 mA, and up to ±15 mA with relaxed V_{OL}/V_{OH}.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIO1}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 21: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 21: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

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Table 52. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage		V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage		2.4	-	
V_{OL}(3)	Output low level voltage	All I/Os $\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage		V_{DD}- 1.3	-	
V_{OL}(3)	Output low level voltage	$\|I_{IO}\|$ = 4 mA $V_{DDIOx} \geq 1.65$ V	-	0.45	
V_{OH}(3)	Output high level voltage		V_{DD} - 0.45	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.65$ V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 21: Voltage characteristics*. The sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\sum I_{IO}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design. Not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 53*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

Table 53. I/O AC characteristics

Speed	Symbol	Parameter(1)(2)	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	2	MHz
			C=50 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	0.35	
			C=10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	3.00	
			C=10 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	0.45	
	Tr/Tf	Output rise and fall time(3)	C=50 pF,2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	100.00	ns
			C=50 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	225.00	
			C=10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	75.00	
			C=10 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	150.00	

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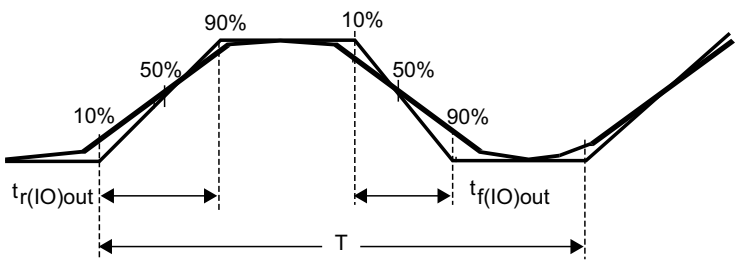
Table 53. I/O AC characteristics (continued)

Speed	Symbol	Parameter[1][2]	Conditions	Min	Max	Unit
01	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	10.00	MHz
			C=50 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	2.00	
			C=10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	15.00	
			C=10 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	2.50	
	Tr/Tf	Output rise and fall time[3]	C=50 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	30.00	ns
			C=50 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	60.00	
			C=10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	15.00	
			C=10 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	30.00	
10	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	30.00	MHz
			C=50 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	15.00	
			C=10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	60.00[4]	
			C=10 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	30.00	
	Tr/Tf	Output rise and fall time[3]	C=50 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	11.00	ns
			C=50 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	22.00	
			C=10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	4.00	
			C=10 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	8.00	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	60.00[4]	MHz
			C=30 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	30.00	
			C=10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	80.00[4]	
			C=10 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	40.00	
	Tr/Tf	Output rise and fall time[3]	C=30 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	5.50	ns
			C=30 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	11.00	
			C=10 pF, 2.7 V ≤ V_{DDIOx} ≤ 3.6 V	-	2.50	
			C=10 pF, 1.65 V ≤ V_{DDIOx} ≤ 2.7 V	-	5.00	

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0490 reference manual for a description of GPIO Port configuration register.
2. Specified by design. Not tested in production.
3. The fall time is defined between 70% and 30% of the output waveform, according to I^2C specification.
4. This value represents the I/O capability but the maximum system frequency is limited to 48 MHz.

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Figure 24. I/O AC characteristics definition(1)



Maximum frequency is achieved with a duty cycle at (45 - 55%) when loaded by the specified capacitance.

1. Refer to *Table 53: I/O AC characteristics*.

5.3.14 NRST input characteristics

The NRST input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 24: General operating conditions*.

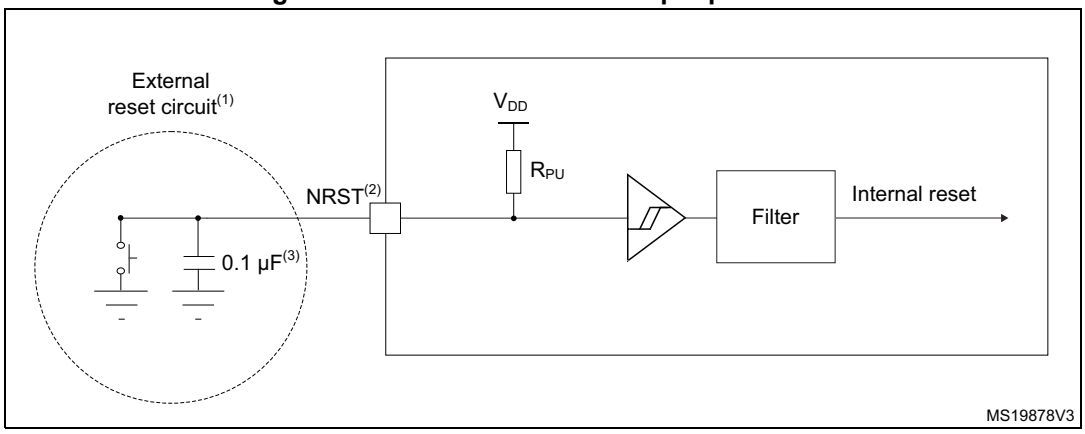
Table 54. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3 \times V_{DD}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7 \times V_{DD}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}(1)	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse	$2.0\ V < V_{DD} < 3.6\ V$	-	-	70	ns
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	$2.0\ V < V_{DD} < 3.6\ V$	350	-	-	ns

1. Specified by design. Not tested in production..
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

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Figure 25. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that, upon power-on, the level on the NRST pin can exceed the minimum $V_{IH(NRST)}$ level specified in *Table 54: NRST pin characteristics*. Otherwise, the device does not exit the power-on reset. This applies to any NRST configuration set through the NRST_MODE[1:0] bitfield, the GPIO mode inclusive.
3. The external capacitor on NRST must be placed as close as possible to the device.

5.3.15 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 55* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 24: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 55. ADC characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.0	-	3.6	V
V_{REF+}	Positive reference voltage	-	2	-	V_{DD}	V
f_{ADC}	ADC clock frequency	-	0.14	-	35	MHz
f_s	Sampling rate	12 bits	-	-	2.50	MSps
		10 bits	-	-	2.92	
		8 bits	-	-	3.50	
		6 bits	-	-	4.38	
f_{TRIG}	External trigger frequency	f_{ADC} = 35 MHz; 12 bits	-	-	2.33	MHz
		12 bits	-	-	f_{ADC}/15	
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}(2)	V
R_{AIN}	External input impedance	-	-	-	50	kΩ

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Table 55. ADC characteristics (continued)

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	ADC power-up time	LDO already started	2			Conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 35 MHz	2.35			µs
		-	82			$1/f_{ADC}$
t_{WLAT}	ADC_DR register write latency	CKMODE = 00	$1.5/f_{ADC_CK} + 2/f_{PCLK}$	-	$1.5/f_{ADC_CK} + 3/f_{PCLK}$	-
		CKMODE = 01	4.5			$1/f_{PCLK}$
		CKMODE = 10	8.5			
		CKMODE = 11	2.5			
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	2	-	3	$1/f_{ADC}$
		CKMODE = 01	6.5			$1/f_{PCLK}$
		CKMODE = 10	12.5			
		CKMODE = 11	3.5			
t_s	Sampling time	f_{ADC} = 35 MHz	0.043	-	4.59	µs
			1.5	-	160.5	$1/f_{ADC}$
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 35 MHz Resolution = 12 bits	0.40	-	4.95	µs
		Resolution = 12 bits	t_s + 12.5 cycles for successive approximation = 14 to 173			$1/f_{ADC}$
t_{IDLE}	Laps of time allowed between two conversions without rearm	-	-	-	100	µs
$I_{DDA(ADC)}$	ADC consumption from V_{DDA}	f_s = 2.5 MSps	-	410	-	µA
		f_s = 1 MSps	-	164	-	
		f_s = 10 kSps	-	17	-	
$I_{DDV(ADC)}$	ADC consumption from V_{REF+}	f_s = 2.5 MSps	-	65	-	µA
		f_s = 1 MSps	-	26	-	
		f_s = 10 kSps	-	0.26	-	

1. Specified by design. Not tested in production.
2. V_{REF+} is internally connected to V_{DDA} on some packages.Refer to *Section 4: Pinouts, pin description and alternate functions* for further details.

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Table 56. Maximum ADC R_{AIN}

Resolution	Sampling cycle at 35 MHz	Sampling time at 35 MHz [ns]	Max. R_{AIN}(1) (Ω)
12 bits	1.5	43	50
	3.5	100	680
	7.5	214	2200
	12.5	357	4700
	19.5	557	8200
	39.5	1129	15000
	79.5	2271	33000
	160.5	4586	50000
10 bits	1.5	43	68
	3.5	100	820
	7.5	214	3300
	12.5	357	5600
	19.5	557	10000
	39.5	1129	22000
	79.5	2271	39000
	160.5	4586	50000
8 bits	1.5	43	82
	3.5	100	1500
	7.5	214	3900
	12.5	357	6800
	19.5	557	12000
	39.5	1129	27000
	79.5	2271	50000
	160.5	4586	50000
6 bits	1.5	43	390
	3.5	100	2200
	7.5	214	5600
	12.5	357	10000
	19.5	557	15000
	39.5	1129	33000
	79.5	2271	50000
	160.5	4586	50000

1. Specified by design. Not tested in production.

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Table 57. ADC accuracy

Symbol	Parameter[1][2]	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25°C$	-	±3	±4	LSB
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	-	±3	±6.5	
EO	Offset error	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25°C$	-	±1.5	±2	
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	-	±1.5	±4.5	
EG	Gain error	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	-	±3	±3.5	
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	-	±3	±5	
ED	Differential linearity error	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	-	±1.2	±1.5	
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	-	±1.2	±1.5	
EL	Integral linearity error	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	-	±2.5	±3	
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	-	±2.5	±3	
ENOB	Effective number of bits	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	10.1	10.2	-	bit
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	9.6	10.2	-	
SINAD	Signal-to-noise and distortion ratio	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	62.5	63	-	dB
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	59.5	63	-	
SNR	Signal-to-noise ratio	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	63	64	-	dB
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	60	64	-	
THD	Total harmonic distortion	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, $T_A = 25$ °C	-	-74	-73	dB
		$2\ V < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \le 2.5$ Msps, T_A = entire range	-	-74	-70	

1. Evaluated by characterization. Not tested in production.
2. ADC DC accuracy values are measured after internal calibration.

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Figure 26. ADC accuracy characteristics

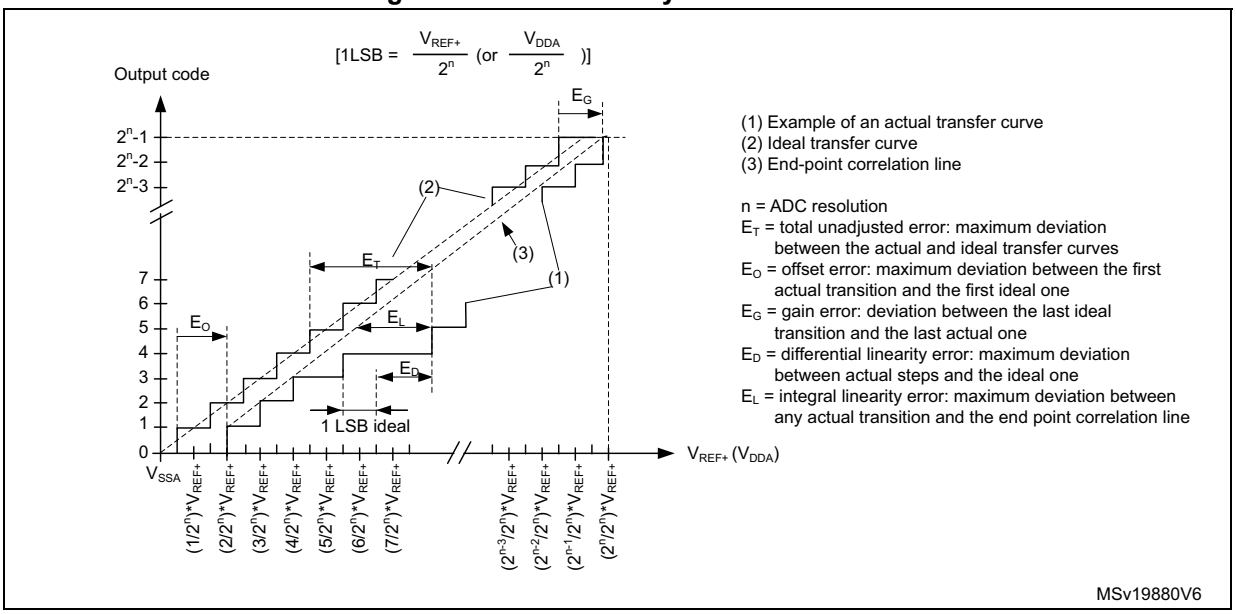
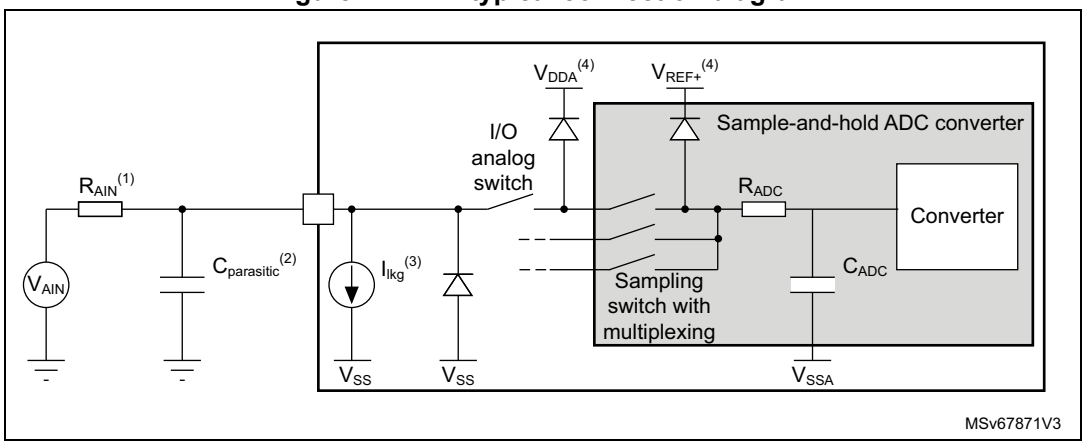


Figure 27. ADC typical connection diagram



1. Refer to *Table 55: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 51: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 51: I/O static characteristics* for the values of I_{lkg}.
4. Refer to *Figure 2: Power supply overview*.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 14: Power supply scheme*. The 100 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

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5.3.16 Temperature sensor characteristics

Table 58. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±5	°C
Avg_Slope(2)	Average slope from V_{SENSE} voltage	2.4	2.53	2.65	mV/°C
V_{30} (3)	Voltage at 30°C (±5 °C)	0.742	0.76	0.786	V
$t_{START(TS_BUF)}$ (1)	Sensor Buffer Start-up time in continuous mode	-	8	15	µs
t_{START} (1)	Start-up time when entering in continuous mode	-	8	120	
t_{S_temp} (1)	ADC sampling time when reading the temperature	5	-	-	
i_{sens} (1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7.0	µA

1. Specified by design. Not tested in production.
2. Evaluated by characterization. Not tested in production.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

5.3.17 Timer characteristics

The parameters given in the following tables are specified by design.

Note: TIMx is used as a general term to refer to a timer (for example, TIM1).

Refer to *Section 5.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 59. TIMx characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.833	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/4$	MHz
Res_{TIM}	Timer resolution	TIMx other than TIM2	-	16	bit
		TIM2	-	32	bit
$t_{COUNTER}$	Counter clock period	TIMx other than TIM2	1	2^{16}	$t_{TIMxCLK}$
		TIM2	1	2^{32}	$t_{TIMxCLK}$

1. Specified by design. Not tested in production.

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Table 60. IWDG min/max timeout period at 32 kHz LSI clock

Prescaler divider	PR[2:0] bits	Min timeout(1) RL[11:0]= 0x000	Max timeout(1) RL[11:0] = 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings further depend on the phase of the APB interface clock versus the LSI clock, which causes an uncertainty of one RC period.

5.3.18 Characteristics of communication interfaces

I²C-bus interface characteristics

The I²C-bus interface meets timing requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The timings are specified by design as long as the I2C peripheral is properly configured (refer to the reference manual RM0490) and when the I2CCLK frequency is greater than the minimum shown in the following table.

Table 61. Minimum I2CCLK frequency

Symbol	Parameter	Condition		Typ	Unit
$f_{I2CCLK(min)}$	Minimum I2CCLK frequency for correct operation of I2C peripheral	Standard-mode		2	MHz
		Fast-mode	Analog filter enabled	9	
			DNF = 0		
			Analog filter disabled	9	
			DNF = 1		
		Fast-mode Plus	Analog filter enabled	19	
			DNF = 0		
			Analog filter disabled	16	
			DNF = 1		

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIO1} is disabled, but is still present. Only FT_f I/O pins

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support Fm+ low-level output current maximum requirement. Refer to *Section 5.3.13: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the following table for its characteristics:

Table 62. I2C analog filter characteristics

Symbol	Parameter(1)	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	100(3)	ns

1. Evaluated by characterization. Not tested in production.
2. Spikes with widths below t_{AF} (min) are filtered.
3. Spikes with widths above t_{AF} (max) are not filtered.

USART (SPI mode) characteristics

Unless otherwise specified, the parameters given in *Table 63* for USART are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 24: General operating conditions*. The additional general conditions are:

- OSPEEDRy[1:0] set to 10 (output speed)
- capacitive load C = 30 pF
- measurement points at CMOS levels: 0.5 × V_{DD}

Refer to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, and RX for USART).

Table 63. USART (SPI mode) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode 2.0 V < V_{DD} < 3.6 V 1.65 V < V_{DDIO2} < 3.6 V	-	-	6.0	MHz
		Slave receiver mode 2.0 V < V_{DD} < 3.6 V 1.65 V < V_{DDIO2} < 3.6 V	-	-	16.0	
		Slave transmitter mode 2.0 V < V_{DD} < 3.6 V 1.65 V < V_{DDIO2} < 3.6 V	-	-	16.0	
$t_{su(NSS)}$	NSS setup time	Slave mode	T_{ker}(1) + 1	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	ns
$t_{w(CKH)}$	CK high time	Master mode	1 / f_{CK} / 2 - 1.5	1 / f_{CK} / 2	1 / f_{CK} / 2 + 1.5	ns
$t_{w(CKL)}$	CK low time					

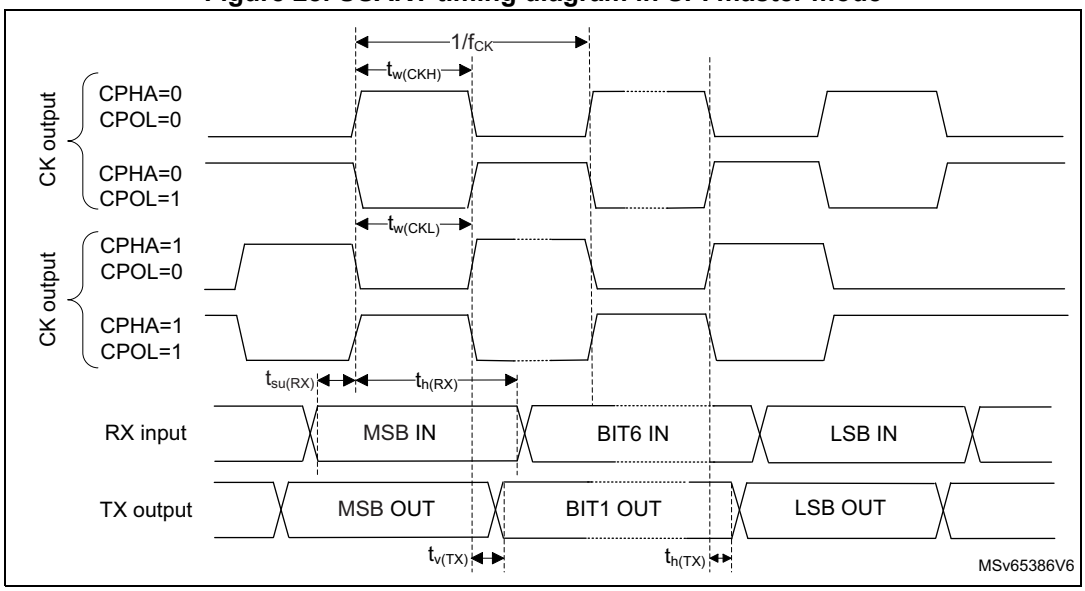
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Table 63. USART (SPI mode) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(RX)}$	Data input setup time	Master mode 2.0 V < V_{DD} < 3.6 V 1.65 V < V_{DDIO2} < 3.6 V	19	-	-	ns
		Master mode 2.0 V < V_{DD} < 3.6 V 2.0 V < V_{DDIO2} < 3.6 V	16	-	-	
		Slave mode	1.5	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0	-	-	ns
		Slave mode	0	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode 2.0 V < V_{DD} < 3.6 V 1.65 V < V_{DDIO2} < 3.6 V	-	13.5	25.5	ns
		Slave mode 2.0 V < V_{DD} < 3.6 V 2.0 V < V_{DDIO2} < 3.6 V			22	
		Slave mode 2.7 V < V_{DD} < 3.6 V 2.7 V < V_{DDIO2} < 3.6 V	-		17.5	
		Master mode	-	2.0	4	
$t_{h(TX)}$	Data output hold time	Slave mode	11.5	-	-	ns
		Master mode	0.5	-	-	

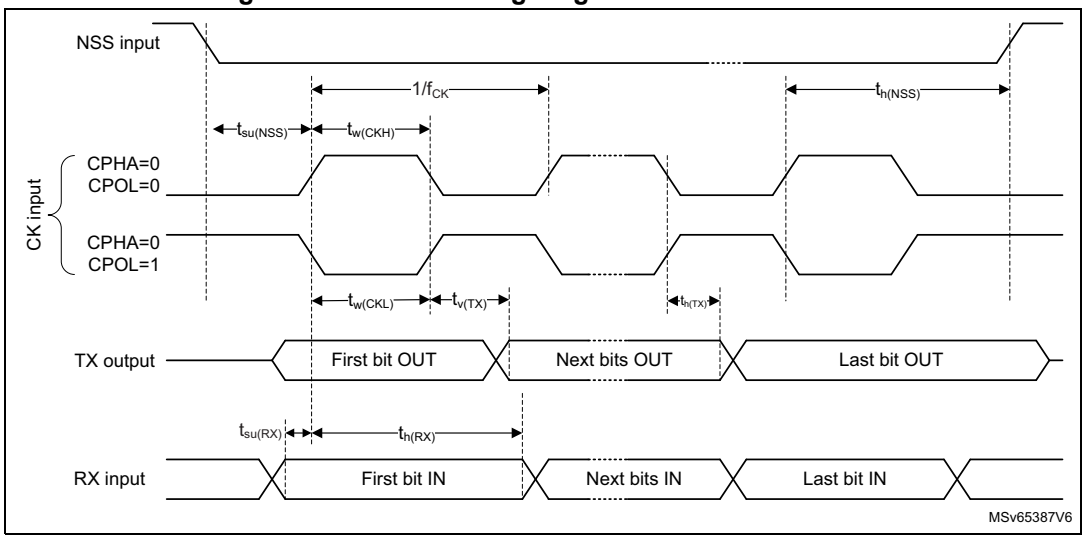
1. T_{ker} is the *usart_ker_ck_pres* clock period

Figure 28. USART timing diagram in SPI master mode



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Figure 29. USART timing diagram in SPI slave mode



SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 64* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 24: General operating conditions*. The additional general conditions are:

- OSPEEDRy[1:0] set to 11 (output speed)
- capacitive load C = 30 pF
- measurement points at CMOS levels: 0.5 × V_{DD}

Refer to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 64. SPI characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2 V < V_{DD} < 3.6 V 1.65 V < V_{DDIO2} < 3.6 V	-	-	24	MHz
		Slave receiver mode 1.65 V < V_{DDIO2} < 3.6 V			24	
		Slave transmitter mode/full duplex(2) 2.7 V < V_{DD} < 3.6 V			24	
		Slave transmitter mode/full duplex(2) 2 V < V_{DD} < 3.6 V			22	
		Slave transmitter mode/full duplex(2) 1.65 V < V_{DDIO2} < 3.6 V			19	
$t_{su(NSS)}$	NSS setup time	Slave mode	4 * T_{PCLK}	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 * T_{PCLK}	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low times	Master mode	T_{SCK2}(3) - 1	T_{PCLK}	T_{SCK2}(3) + 1	ns

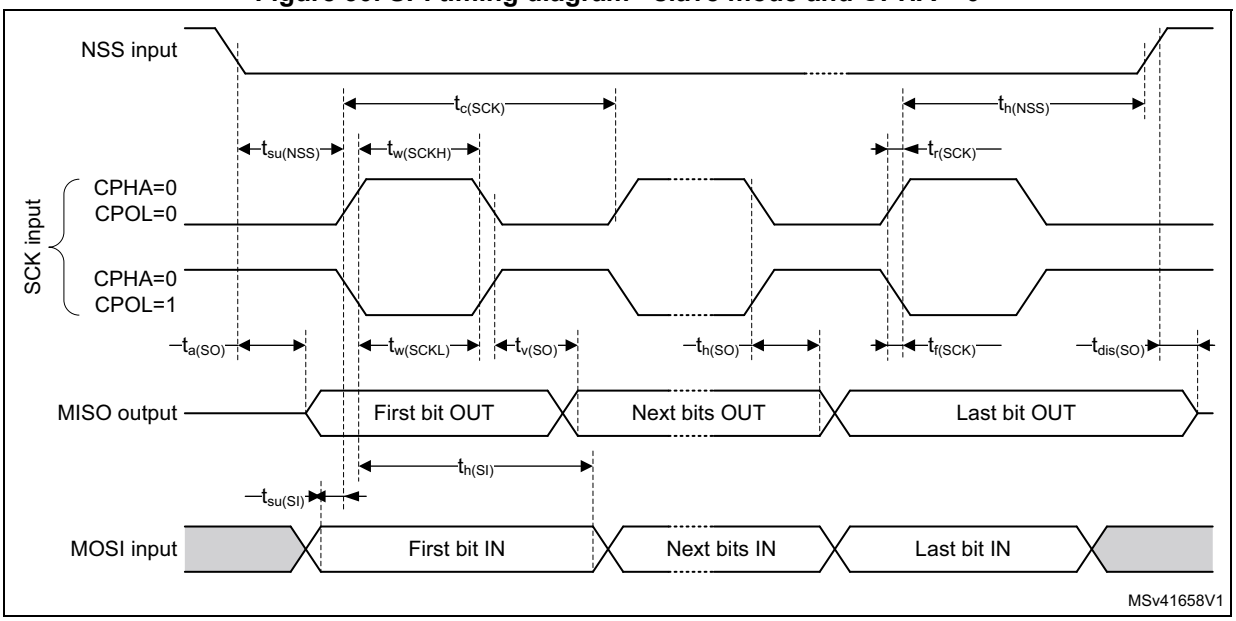
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Table 64. SPI characteristics (continued)

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
$t_{su(MI)}$	Data input setup time in master mode	-	4.5	-	-	ns
$t_{su(SI)}$	Data input setup time in slave mode	-	2.5	-	-	ns
$t_{h(MI)}$	Data input hold time in master mode	-	2	-	-	ns
$t_{h(SI)}$	Data input hold time in slave mode	-	3	-	-	ns
$t_{a(SO)}$	Data output access time in slave mode	-	6	-	34	ns
$t_{dis(SO)}$	Data output disable time in slave mode	-	5	-	16	ns
$t_{v(SO)}$	Data output valid time in slave mode	$2.7\ V < V_{DD} < 3.6\ V$	-	12	16	ns
		$2\ V < V_{DD} < 3.6\ V$	-	12	22.5	
		$1.65\ V < V_{DDIO2} < 3.6\ V$		12	26	
$t_{v(MO)}$	Data output valid time in master mode	-	-	3	5.5	ns
$t_{h(SO)}$	Data output hold time in slave mode	-	8	-	-	ns
$t_{h(MO)}$	Data output hold time in master mode	-	0.5	-	-	ns

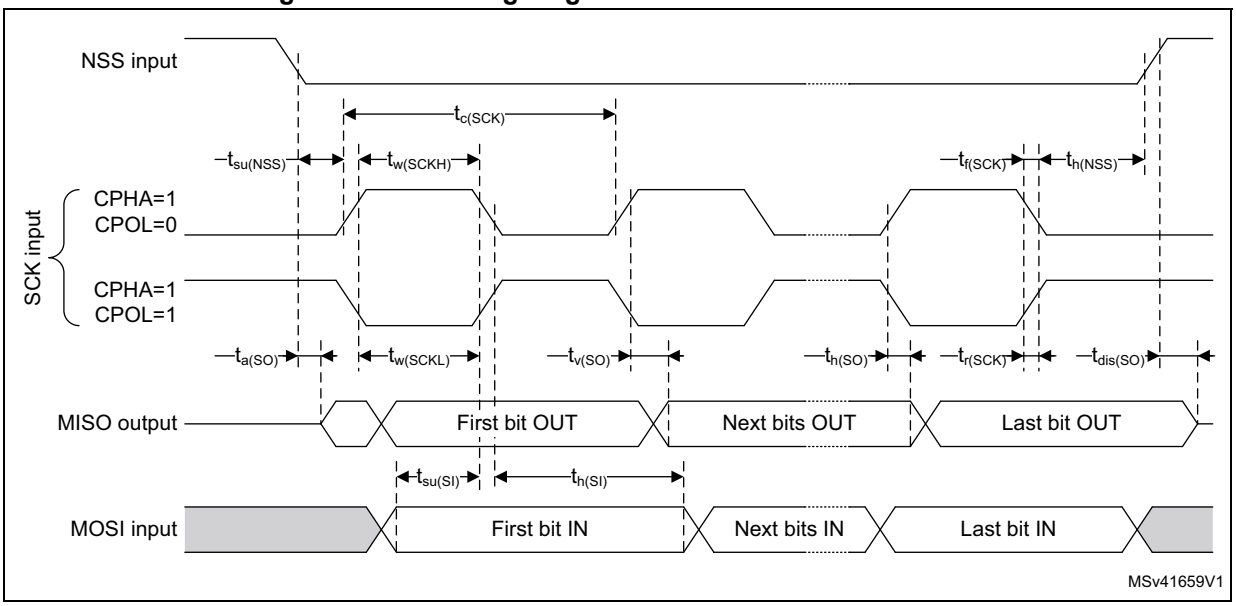
1. Evaluated by characterization. Not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%
3. $T_{SCK2} = T_{PCLK}$ * prescaler / 2

Figure 30. SPI timing diagram - slave mode and CPHA = 0



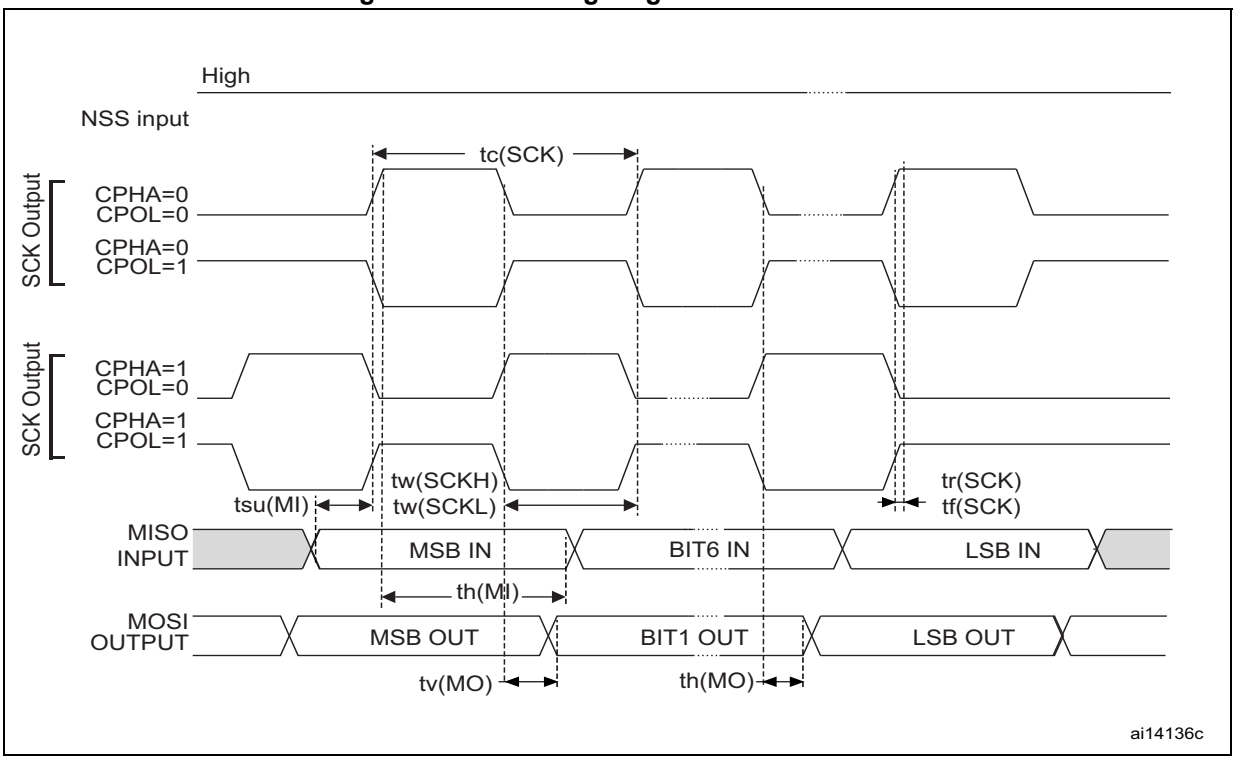
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Figure 31. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at 0.5 V_{DD} and with external C_L = 30 pF.

Figure 32. SPI timing diagram - master mode



1. Measurement points are done at 0.5 V_{DD} and with external C_L = 30 pF.

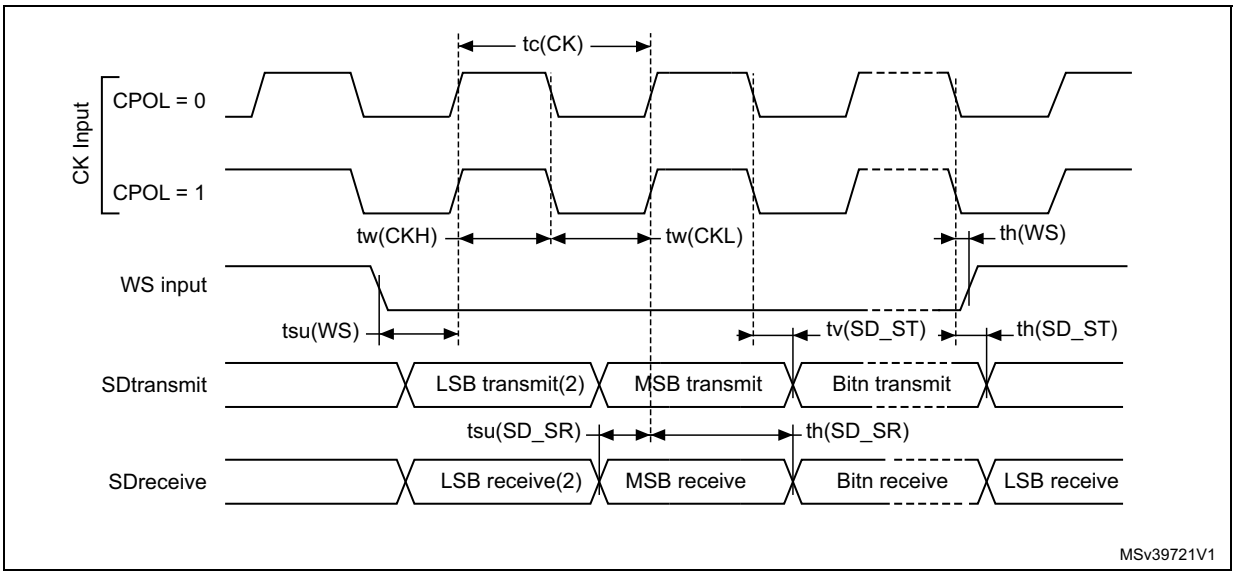
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Table 65. I²S characteristics

Symbol	Parameter(1)	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	-	-	48	MHz
f_{CK}	I2S clock frequency	Master TX	-	12	MHz
		Master RX	-	12	
		Slave TX	-	13	
		Slave RX	-	48	
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	3.5	-	
$t_{h(WS)}$	WS hold time	Slave mode	1	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	3.5	-	
$t_{su(SD_SR)}$		Slave receiver	2.5	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	2.5	-	ns
$t_{h(SD_SR)}$		Slave receiver	1	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	23	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10.5	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0.5	-	

1. Evaluated by characterization. Not tested in production.

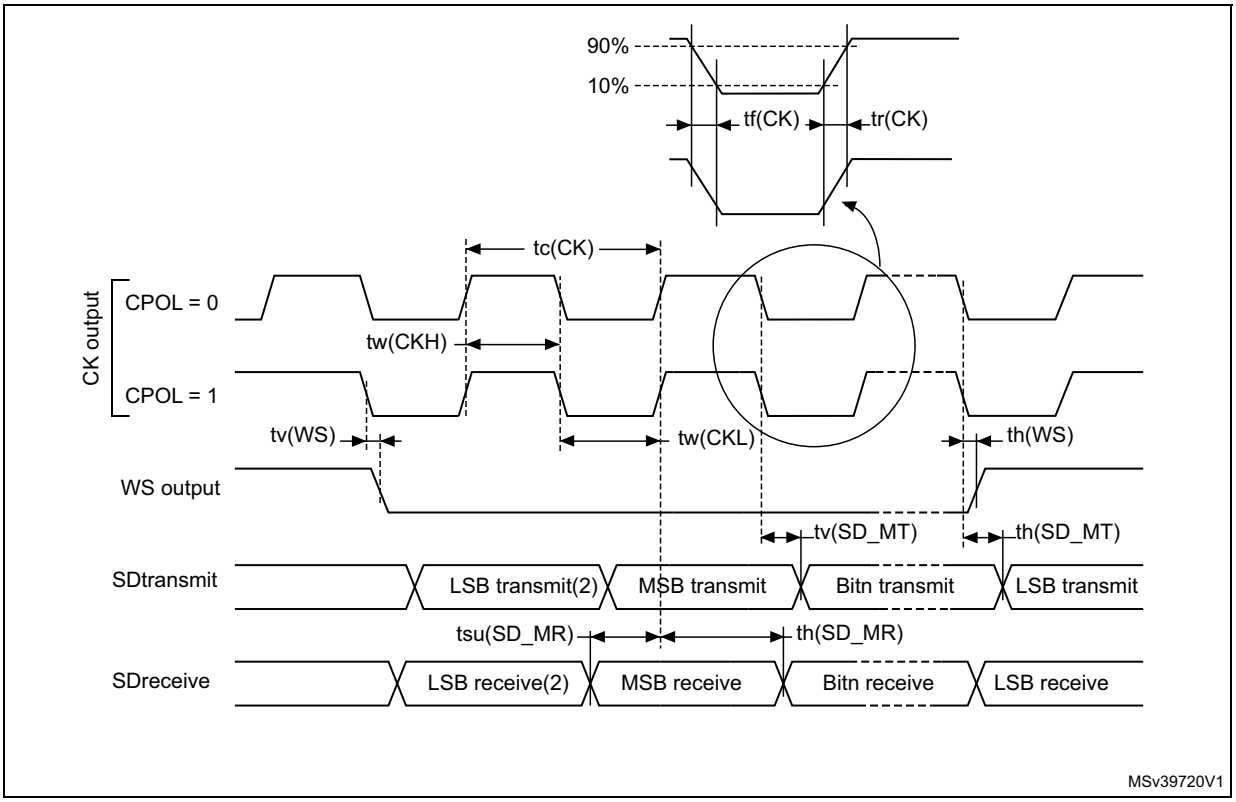
Figure 33. I²S slave timing diagram (Philips protocol)



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1. Measurement points are done at CMOS levels: 0.3 × V_{DDIOx} and 0.7 × V_{DDIOx}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 34. I^2S master timing diagram (Philips protocol)



1. Evaluated by characterization. Not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB characteristics

The following table provides the electrical characteristics of the USB peripheral.

Table 66. USB electrical characteristics

Symbol	Parameter[1][2]	Conditions	Min	Typ	Max	Unit
V_{DDIO2}	USB full speed transceiver operating voltage	-	3.0[3]	-	3.6	V
$t_{STARTUP}$	USB transceiver startup time	-	-	-	1	µs
R_{PD}	Pull down resistor on PA11 (USB_DM), PA12 (USB_DP)	$V_{IN} = V_{DD}$	14.25	-	24.8	kΩ
R_{PU}	Pull Up Resistor on PA12 (USB_DP)	$V_{IN} = V_{SS}$, during idle	0.9	1.25	1.575	kΩ
		$V_{IN} = V_{SS}$, during reception	1.425	2.25	3.09	

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Table 66. USB electrical characteristics (continued)

Symbol	Parameter[1][2]	Conditions	Min	Typ	Max	Unit
VCRS	Output signal crossover voltage	-	1.3	-	2	V
ZDRV	Output driver impedance[4]	Driving high or low	28	36	44	Ω

1. Specified by design. Not tested in production.
2. All voltages are with respect to the local ground potential.
3. The USB full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics. These are degraded in the V_{DDIO2} voltage range from 2.7 V to 3.0 V.
4. No external termination series resistors are required on DP (D+) and DM (D-) pins as the matching impedance is included in the embedded driver

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6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 Device marking

Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

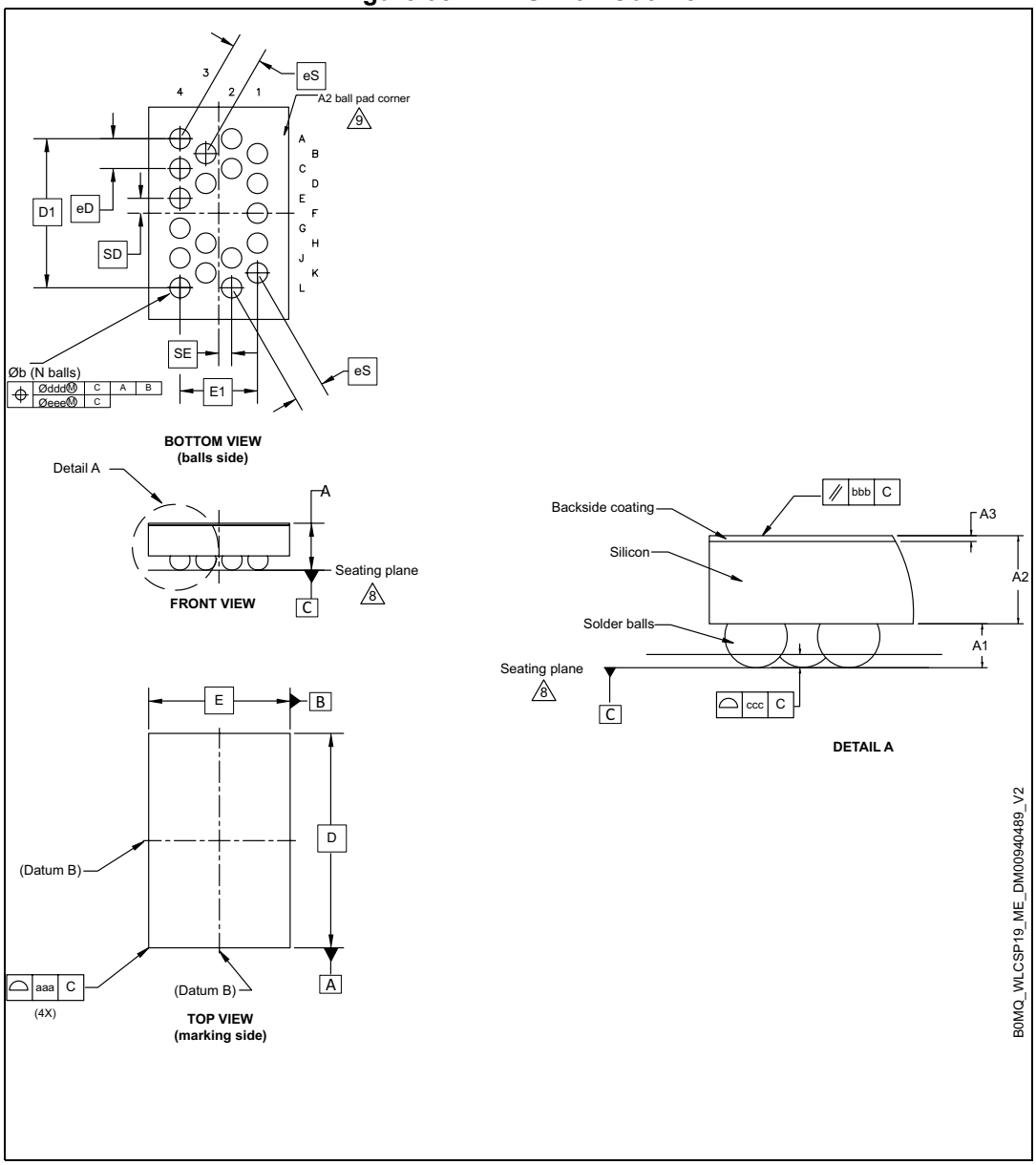
A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

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6.2 WLCSP19 package information (B0MQ)

This WLCSP is a 19-ball, 2.492 x 1.643 mm, 0.350 mm pitch, wafer level chip scale package.

Figure 35. WLCSP19 - Outline



1. Drawing is not to scale.

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Table 67. WLCSP19 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.577	-	-	0.0227
A1[3]	0.152	-	-	0.0060	-	-
A2	-	0.380	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b[4]	0.215	0.240	0.265	0.0085	0.0094	0.0104
D[5]	2.492 BSC			0.0981 BSC		
D1[5]	1.750 BSC			0.0689 BSC		
E[5]	1.643 BSC			0.0647 BSC		
E1[5]	0.909 BSC			0.0358 BSC		
eD[5][6]	0.350 BSC			0.0138 BSC		
eS[5][6]	0.350 BSC			0.0138 BSC		
N[7]	19					
SD[5][8]	0.175 BSC			0.0069 BSC		
SE[5][8]	0.152 BSC			0.0060 BSC		
aaa[9]	0.100			0.0039		
bbb[9]	0.100			0.0039		
ccc[9]	0.100			0.0039		
ddd[9]	0.050			0.0020		
eee[9]	0.050			0.0020		

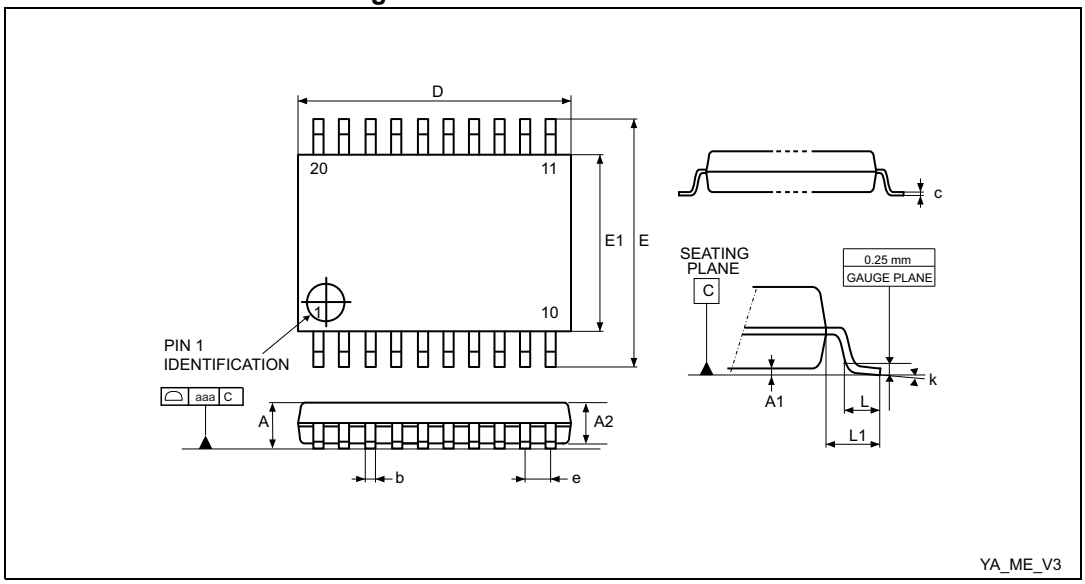
1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The profile height A is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to Datum C.
5. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances, refer to form and position table. On the drawing, these dimensions are framed. For the tolerances, refer to form and position values.
6. e represents the solder balls grid pitch(es).
7. N represents the total number of balls.
8. Basic dimensions SD & SE are defining the ball matrix position with respect to datums A and B.
9. Tolerance of form and position drawing.

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6.3 TSSOP20 package information (YA)

TSSOP20 is a 20-lead, 6.5 x 4.4 mm thin small-outline package with 0.65 mm pitch.

Figure 36. TSSOP20 – Outline



1. Drawing is not to scale.

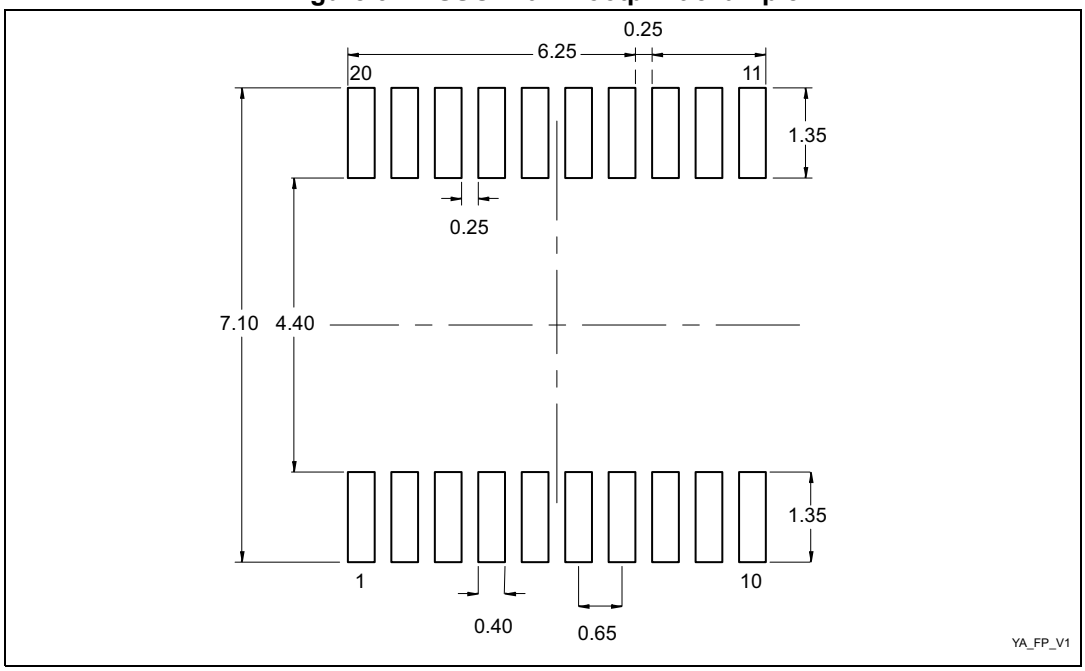
Table 68. TSSOP20 – Mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

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Figure 37. TSSOP20 – Footprint example



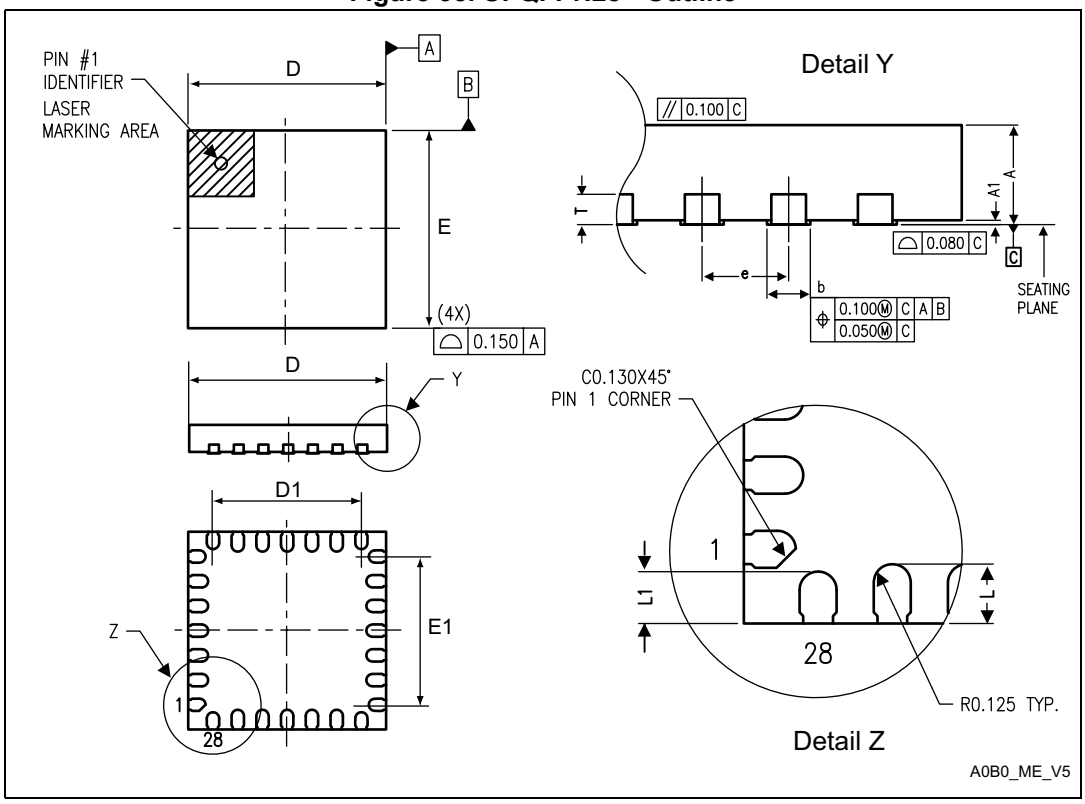
1. Dimensions are expressed in millimeters.

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6.4 UFQFPN28 package information (A0B0)

UFQFPN28 is a 28-lead, 4 x 4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 38. UFQFPN28 - Outline



1. Drawing is not to scale.

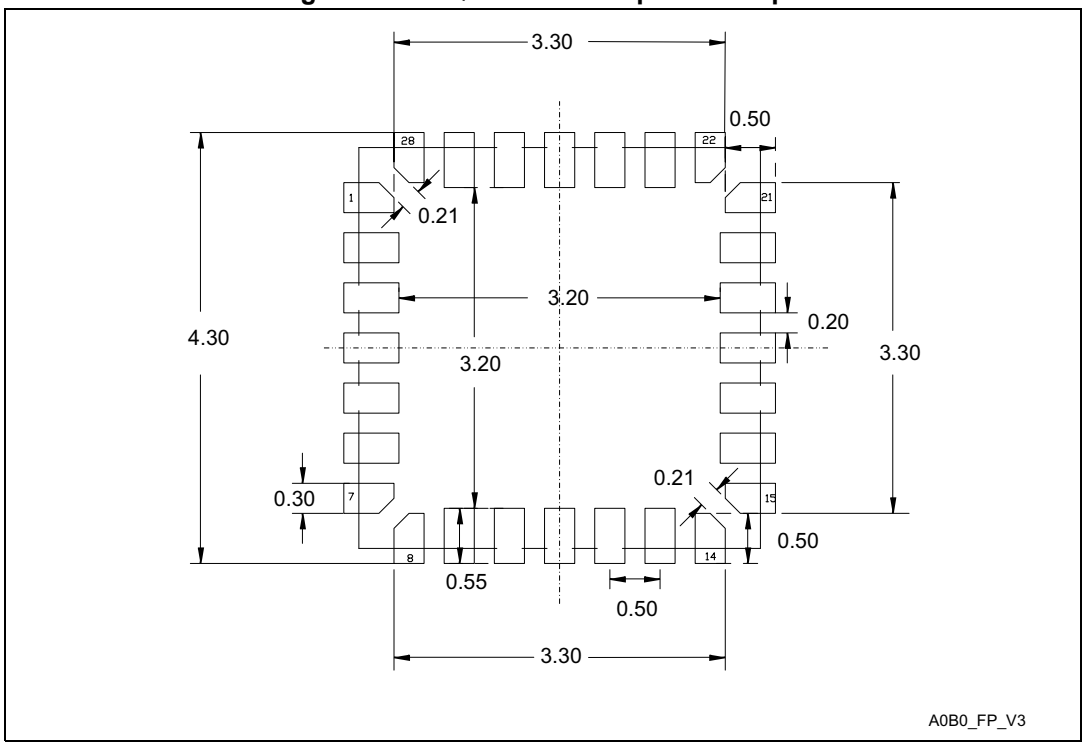
Table 69. UFQFPN28 – Mechanical data(1)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

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Figure 39. UFQFPN28 – Footprint example



1. Dimensions are expressed in millimeters.

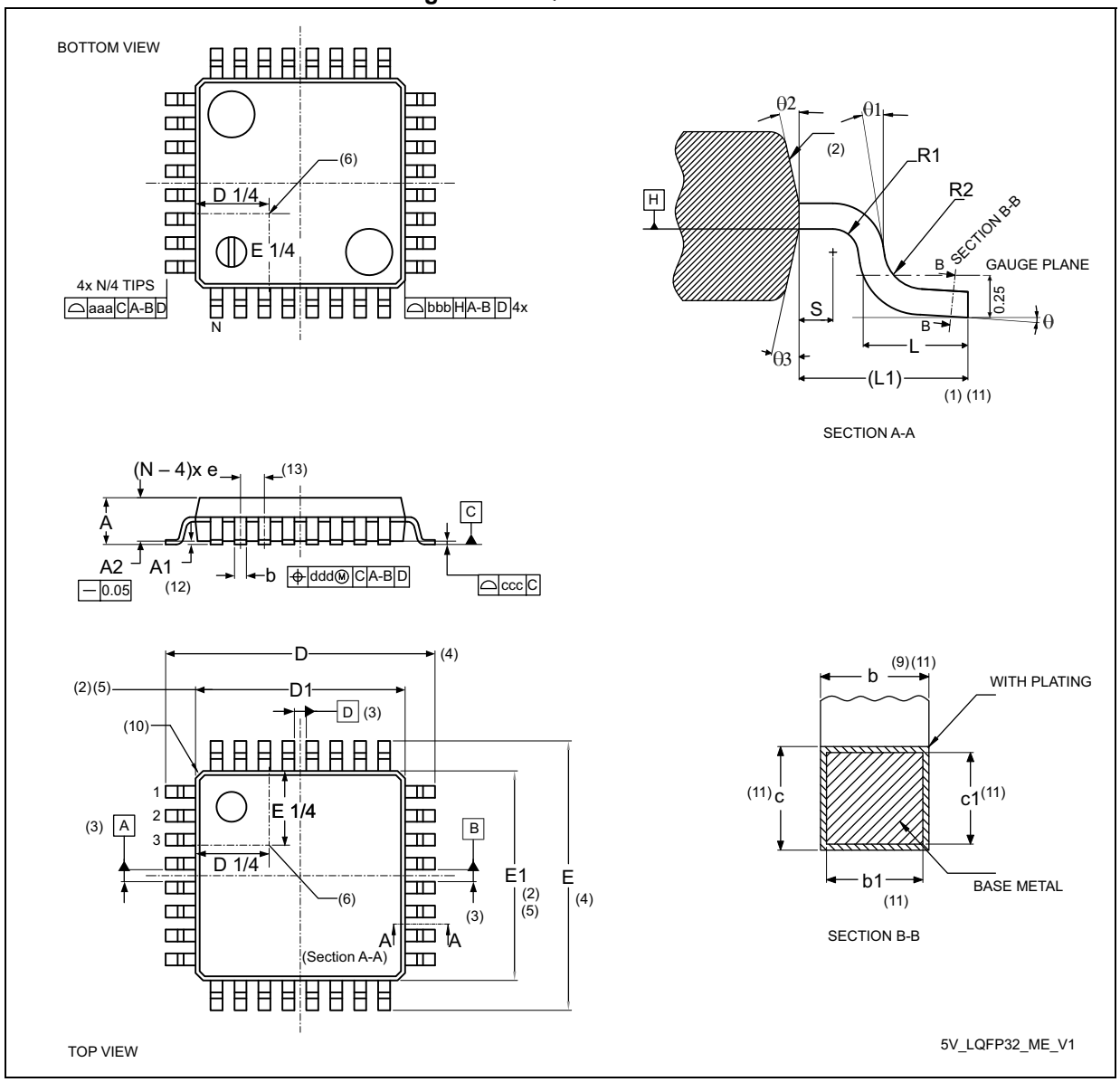
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6.5 LQFP32 package information (5V)

This LQFP is a 32-pin, 7 x 7 mm, low-profile quad flat package.

Note: Figure 40 is not to scale.
Refer to the notes section for the list of notes on Figure 40 and Table 70.

Figure 40. LQFP32 - Outline



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Table 70. LQFP32 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.30	0.37	0.45	0.0118	0.0146	0.0177
b1[11]	0.30	0.35	0.40	0.0118	0.0128	0.0157
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	9.00 BSC			0.3543 BSC		
D1[2][5]	7.00 BSC			0.2756 BSC		
e	0.80 BSC			0.0315 BSC		
E[4]	9.00 BSC			0.3543 BSC		
E1[2][5]	7.00 BSC			0.2756 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	32					
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1][7][15]	0.20			0.0079		
bbb[1][7][15]	0.20			0.0079		
ccc[1][7][15]	0.10			0.0039		
ddd[1][7][15]	0.20			0.0079		

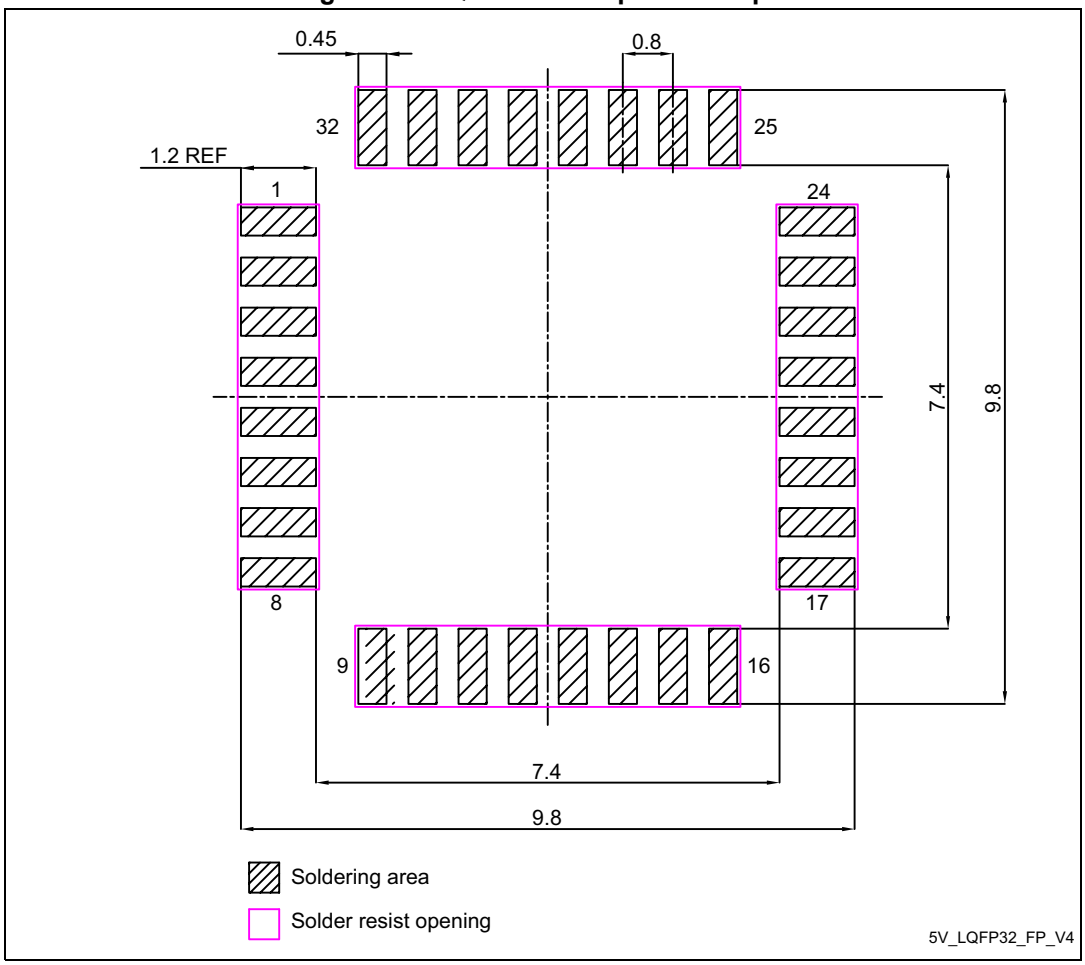
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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at the seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion is allowed inwards the leads.
9. Dimension b does not include a dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. The exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. N is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to four decimal digits.
15. Recommended values and tolerances.

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Figure 41. LQFP32 – Footprint example



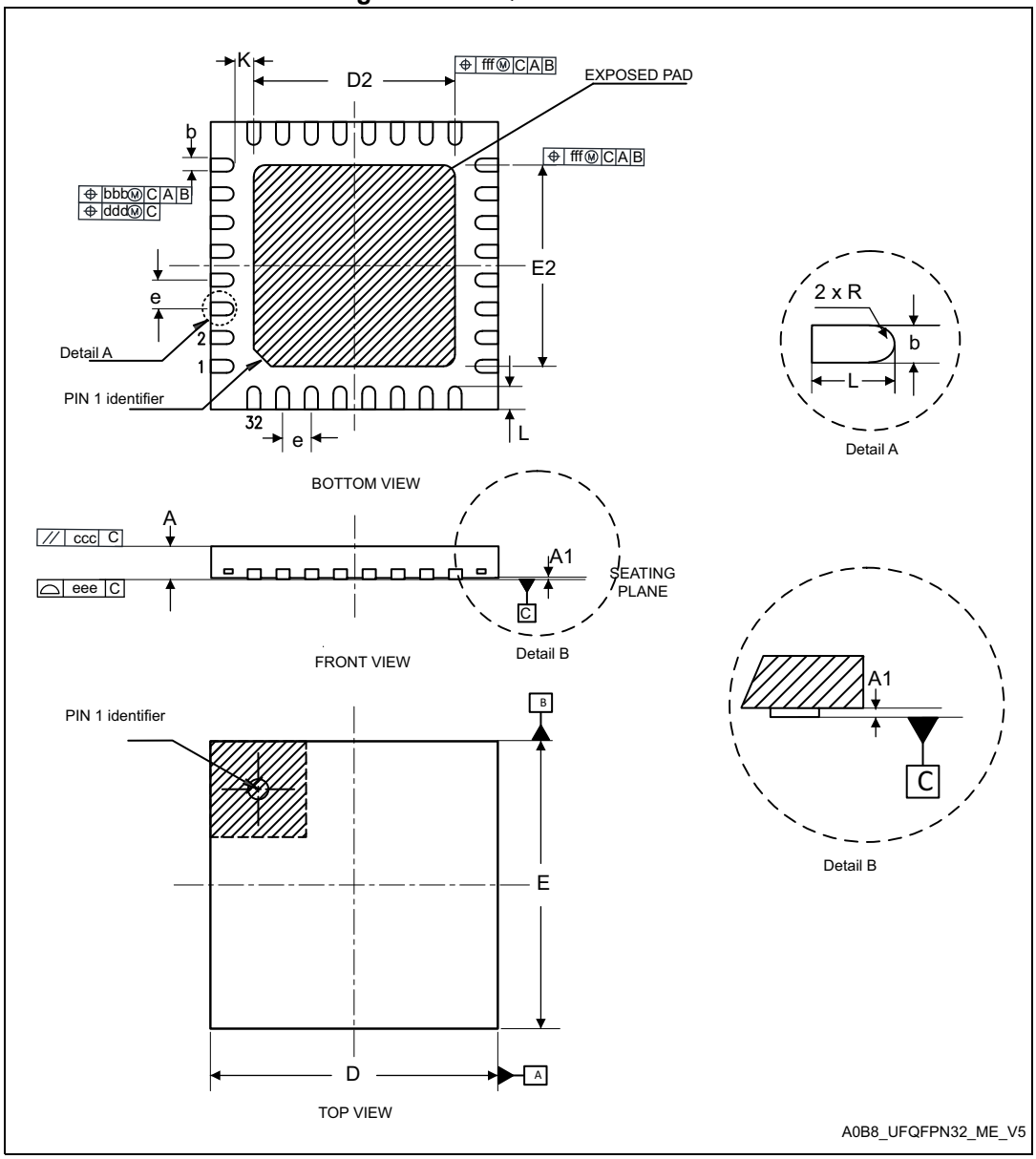
1. Dimensions are expressed in millimeters.

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6.6 UFQFPN32 package information (A0B8)

This UFQFPN is a 32-pin, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package.

Figure 42. UFQFPN32 - Outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.

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Table 71. UFQFPN32 - Mechanical data

Symbol	millimeters[1]			inches[2]		
	Min	Typ	Max	Min	Typ	Max
A[3][4]	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1[5]	0.00	-	0.05	0.000	-	0.0020
b[6]	0.18	0.25	0.30	0.0071	0.0098	0.0118
D[7]	5.00 BSC			0.1969 BSC		
D2[8]	See *Table 73: Exposed pad variation*					
E[7]	5.00 BSC			0.1969 BSC		
E2[8]	See *Table 73: Exposed pad variation*					
e	0.50 BSC			0.0197 BSC		
N[9]	32					
L	0.30	-	0.50	0.0118	-	0.0197
R	0.09	-	-	0.0035	-	-

1. All dimensions are in millimeters. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2018 except European.
2. Values in inches are converted from mm and rounded to four decimal digits.
3. UFQFPN stands for ultra thin fine pitch quad flat package no lead: A ≤ 0.60 mm / Fine pitch e ≤ 1.00 mm.
4. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
5. A1 is the vertical distance from the bottom surface of the plastic body to the nearest metalized package feature.
6. Dimension b applies to metalized terminal. If the terminal has the optional radius on the other end of the terminal, the dimension b must not be measured in that radius area.
7. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances, refer to *Table 72*.
8. Dimensions D2 and E2 refer to the exposed pad. For variance, refer to *Table 73*.
9. N represents the total number of terminals.

Table 72. Tolerance of form and position

Symbol	Millimeters[1]	Inches[2]
aaa	0.15	0.0059
bbb	0.10	0.0039
ccc	0.10	0.0039
ddd	0.05	0.0020
eee	0.08	0.0315
fff	0.10	0.0039

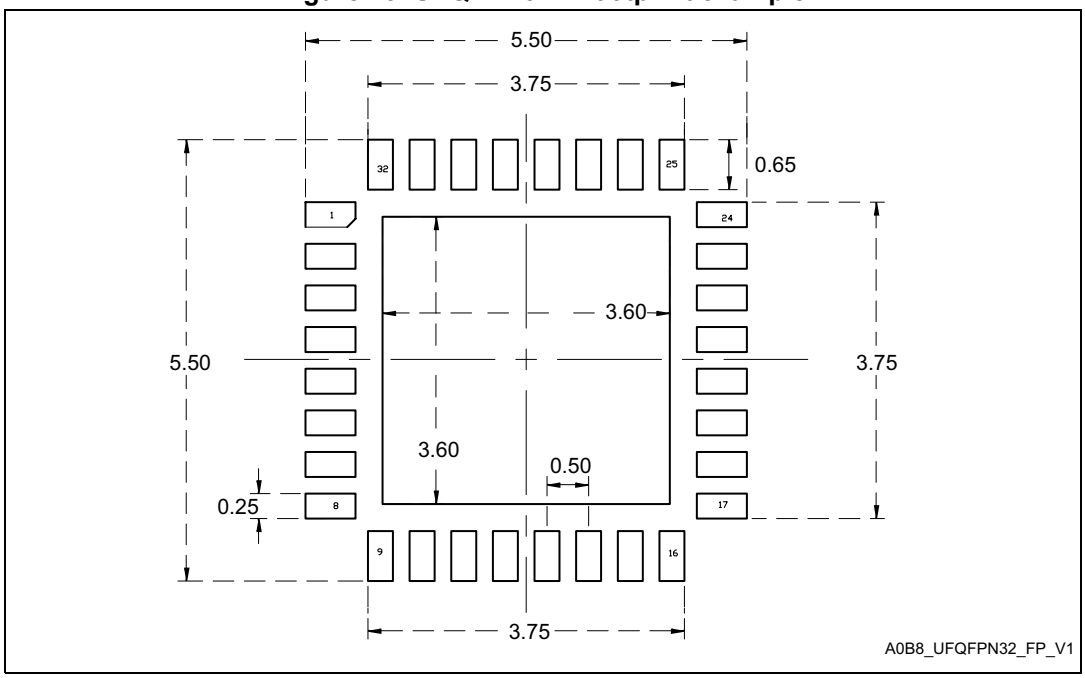
1. All dimensions are in millimeters. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2018 except European.
2. Values in inches are converted from mm and rounded to four decimal digits.

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Table 73. Exposed pad variation

Option	D2			E2		
	Min	Typ	Max	Min	Typ	Max
1	3.40	3.50	3.60	3.40	3.50	3.60
2	3.50	3.60	3.70	3.50	3.60	3.70
3	3.60	3.70	3.80	3.60	3.70	3.80

Figure 43. UFQFPN32 - Footprint example



1. Dimensions are expressed in millimeters.

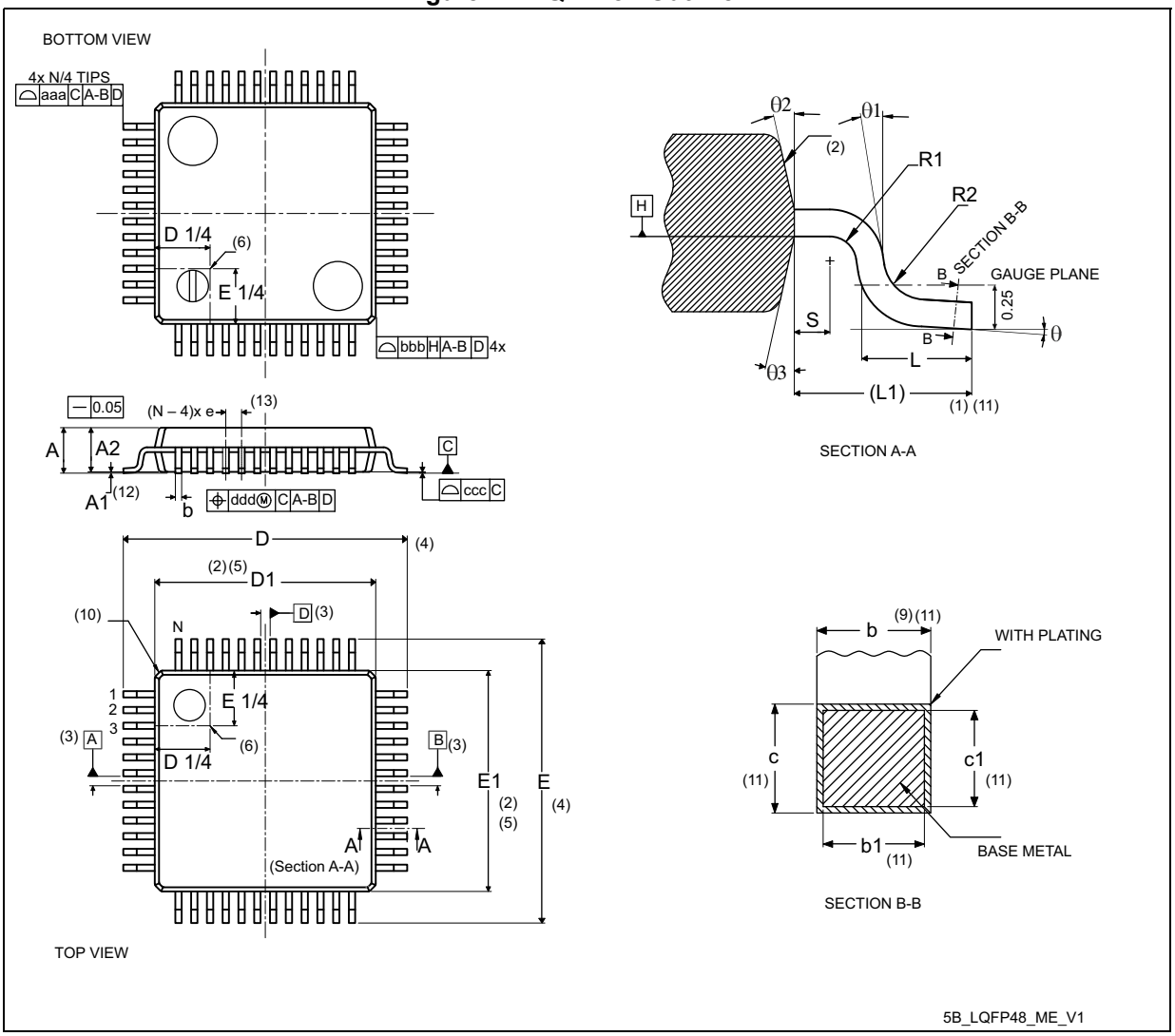
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6.7 LQFP48 package information (5B)

This LQFP is a 48-pin, 7 x 7 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 44. LQFP48 - Outline(15)



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Table 74. LQFP48 - Mechanical data

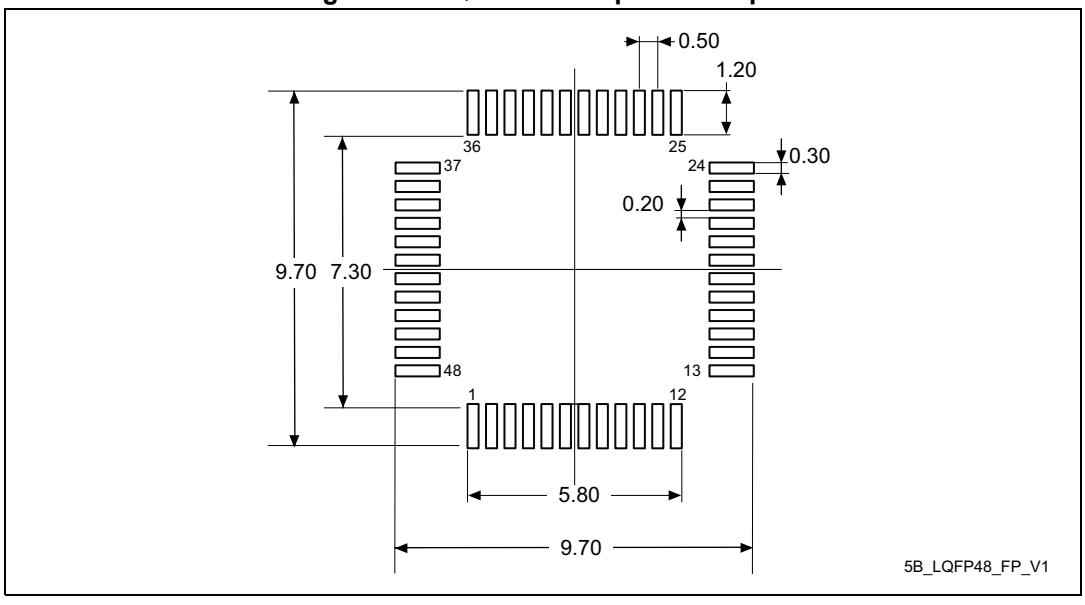
Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	9.00 BSC			0.3543 BSC		
D1[2][5]	7.00 BSC			0.2756 BSC		
E[4]	9.00 BSC			0.3543 BSC		
E1[2][5]	7.00 BSC			0.2756 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	48					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1][7]	0.20			0.0079		
bbb[1][7]	0.20			0.0079		
ccc[1][7]	0.08			0.0031		
ddd[1][7]	0.08			0.0031		

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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 45. LQFP48 - Footprint example



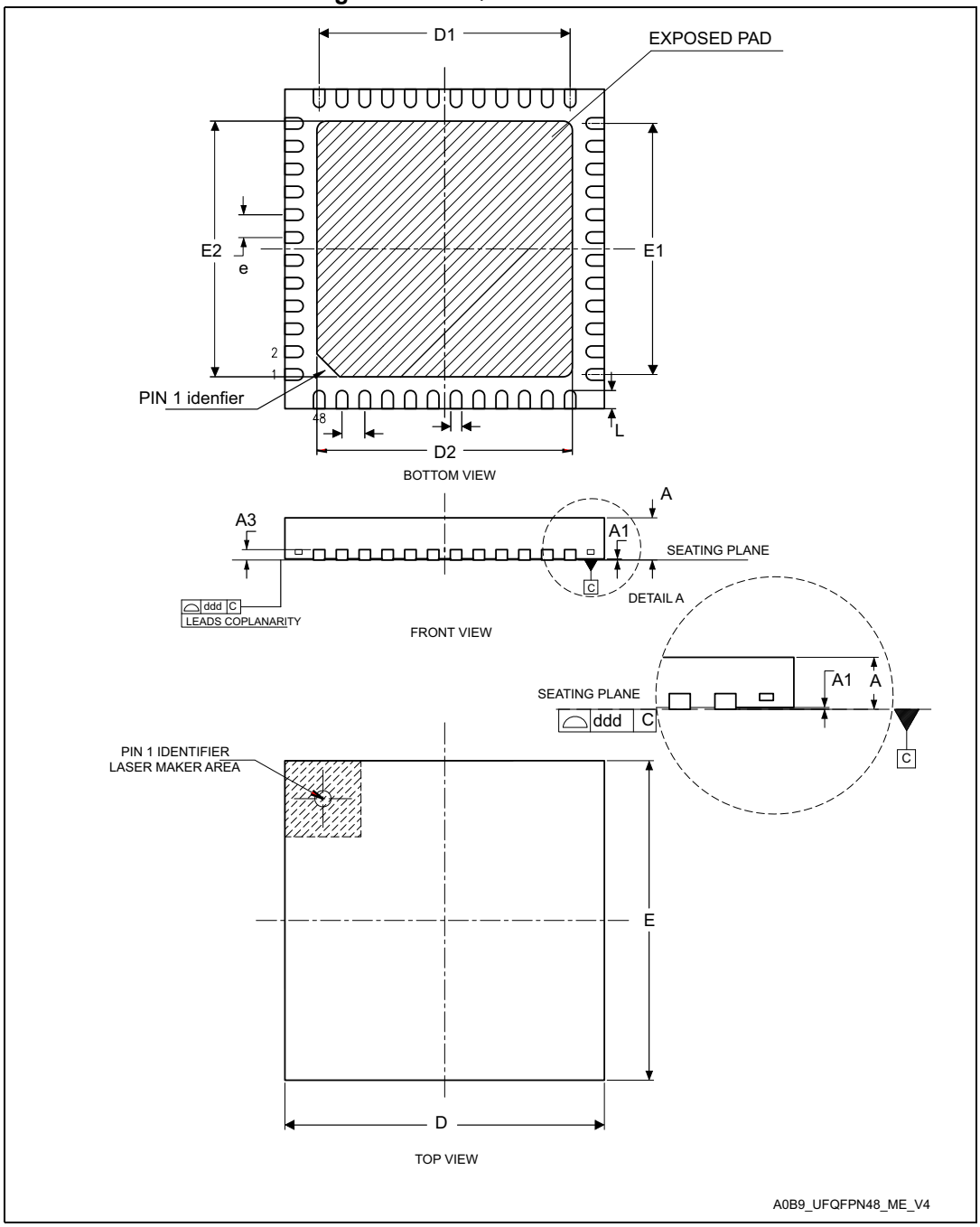
1. Dimensions are expressed in millimeters.

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6.8 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 46. UFQFPN48 – Outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.

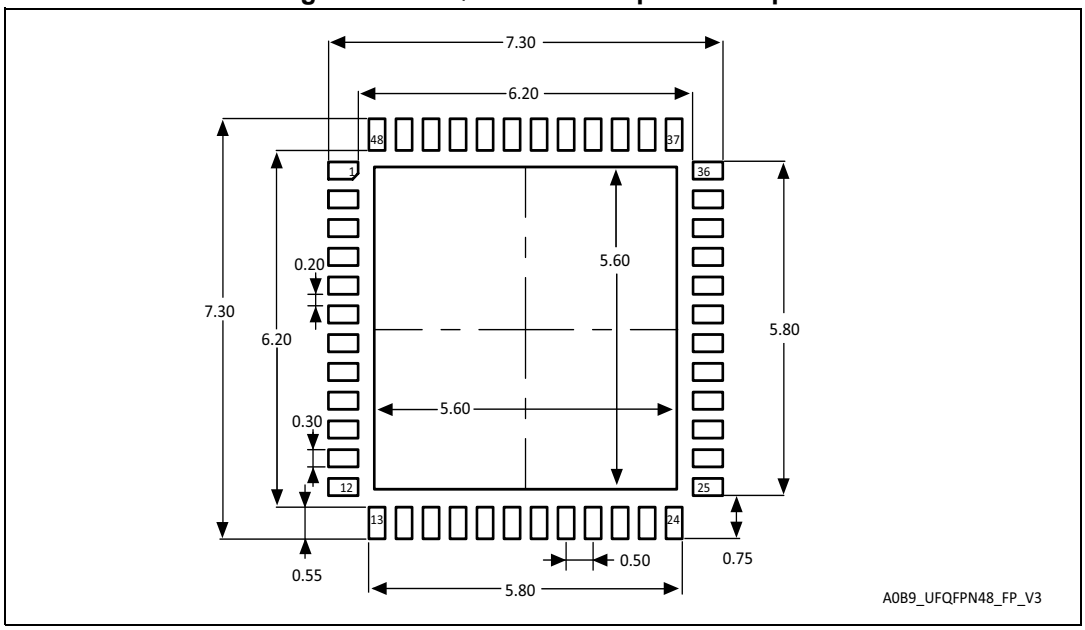
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Table 75. UFQFPN48 – Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D[2]	6.900	7.000	7.100	0.2717	0.2756	0.2795
D1	5.400	5.500	5.600	0.2126	0.2165	0.2205
D2[3]	5.500	5.600	5.700	0.2165	0.2205	0.2244
E[2]	6.900	7.000	7.100	0.2717	0.2756	0.2795
E1	5.400	5.500	5.600	0.2126	0.2165	0.2205
E2[3]	5.500	5.600	5.700	0.2165	0.2205	0.2244
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.
3. Dimensions D2 and E2 are not in accordance with JEDEC.

Figure 47. UFQFPN48 – Footprint example



1. Dimensions are expressed in millimeters.

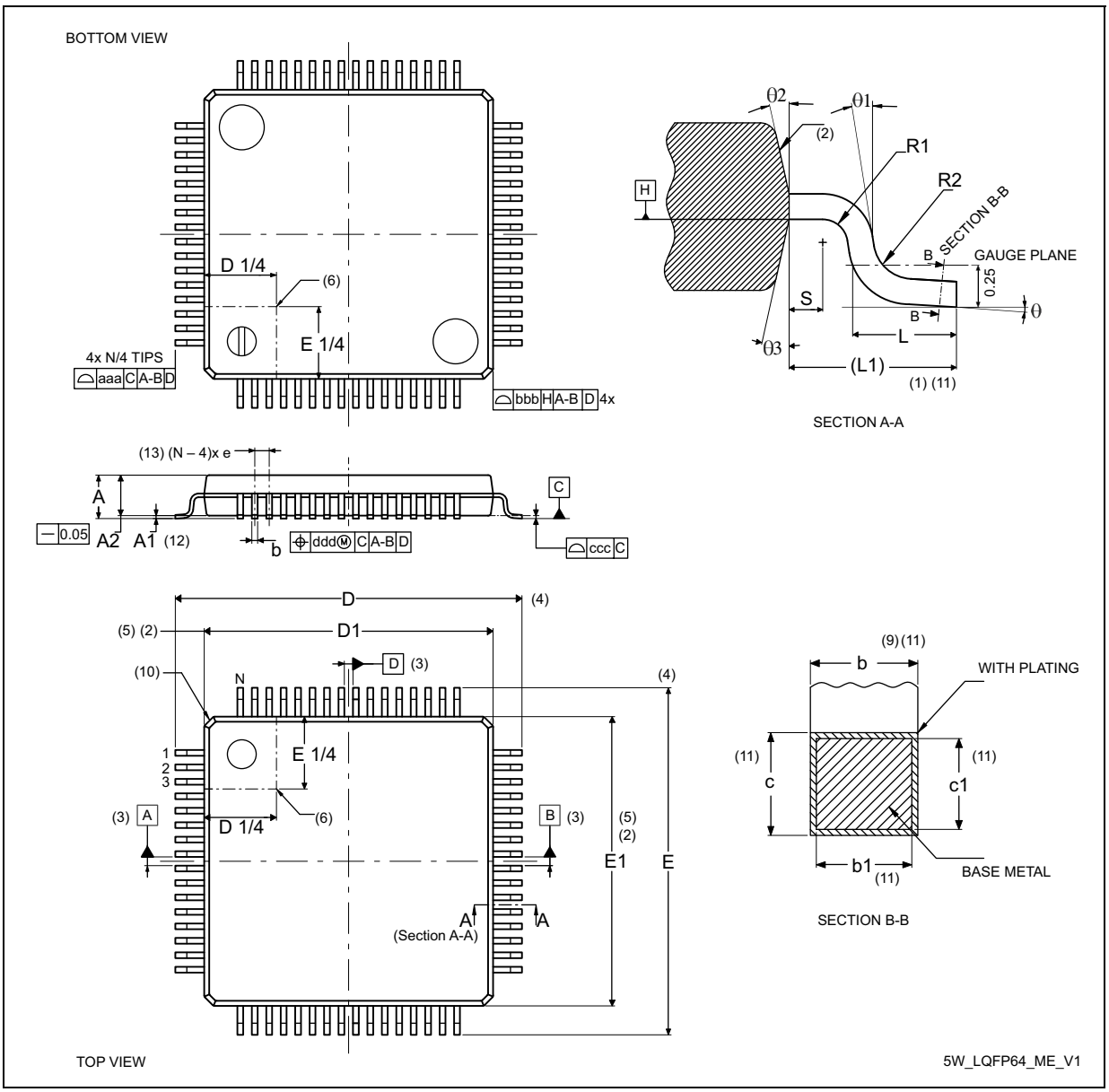
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6.9 LQFP64 package information (5W)

This LQFP is 64-pin, 10 x 10 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 48. LQFP64 - Outline(15)



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Table 76. LQFP64 - Mechanical data

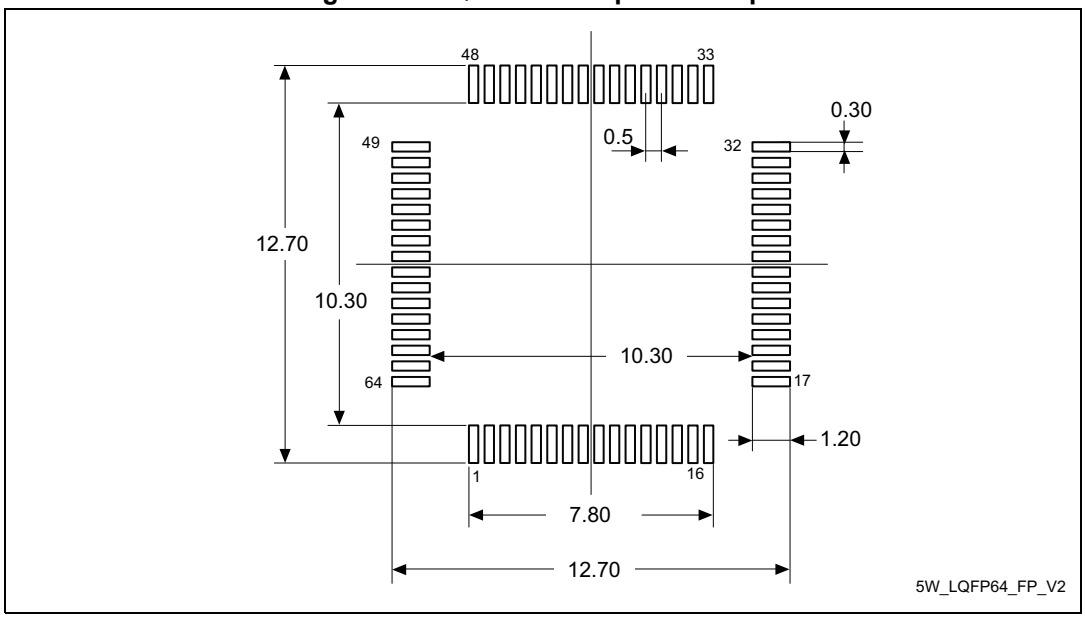
Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	12.00 BSC			0.4724 BSC		
D1[2][5]	10.00 BSC			0.3937 BSC		
E[4]	12.00 BSC			0.4724 BSC		
E1[2][5]	10.00 BSC			0.3937 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	64					
q	0°	3.5°	7°	0°	3.5°	7°
q1	0°	-	-	0°	-	-
q2	10°	12°	14°	10°	12°	14°
q3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1]	0.20			0.0079		
bbb[1]	0.20			0.0079		
ccc[1]	0.08			0.0031		
ddd[1]	0.08			0.0031		

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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 49. LQFP64 - Footprint example



1. Dimensions are expressed in millimeters.

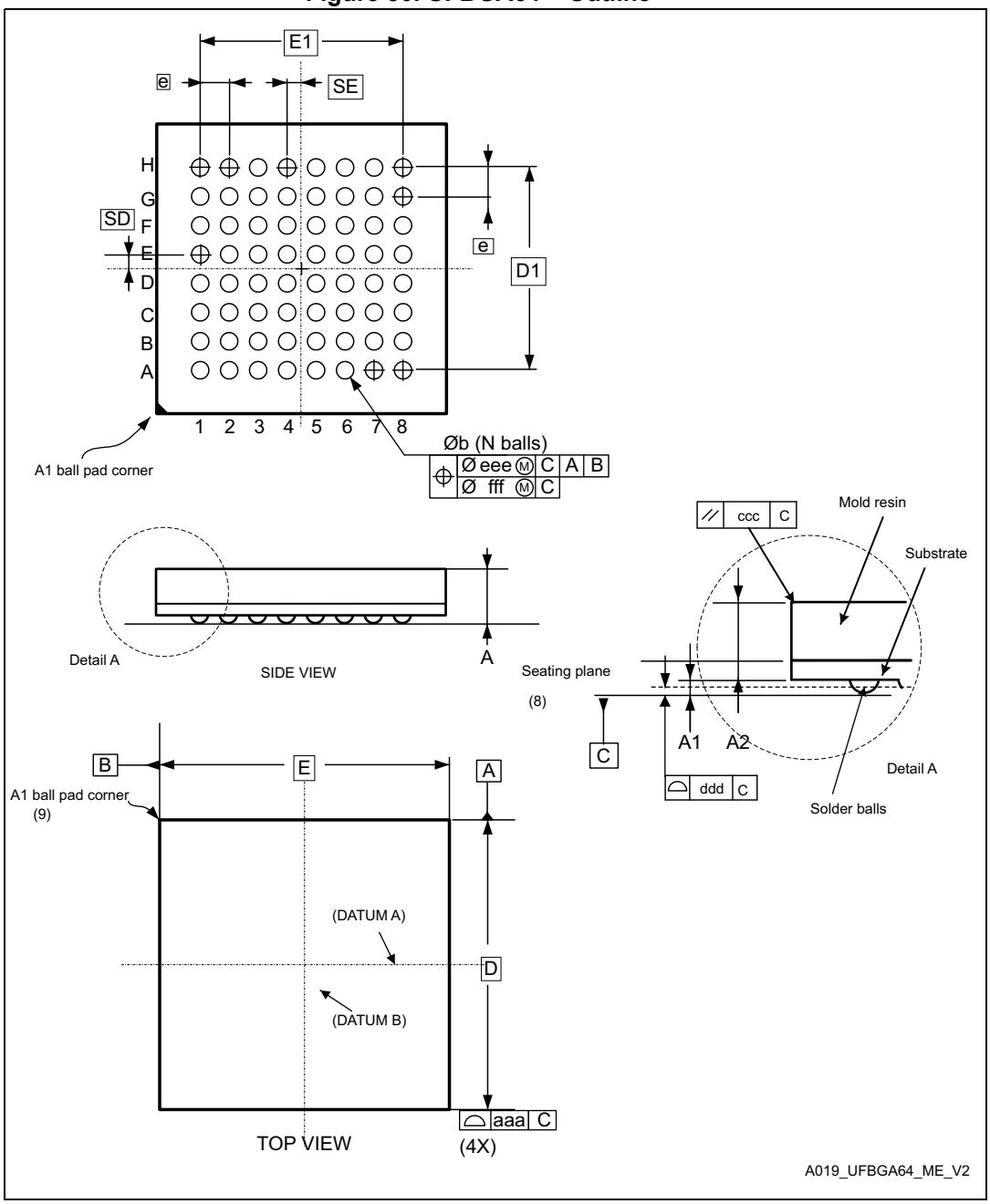
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6.10 UFBGA64 package information (A019)

This UFBGA is a 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package.

Note: See list of notes in the notes section.

Figure 50. UFBGA64 – Outline(13)



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Table 77. UFBGA64 – Mechanical data

Symbol	millimeters[1]			inches[12]		
	Min	Typ	Max	Min	Typ	Max
A[2][3]	-	-	0.60	-	-	0.0236
A1[4]	0.05	-	-	0.0020	-	-
A2	-	0.43	-	-	0.0169	-
b[5]	0.23	0.28	0.33	0.0090	0.0110	0.0130
D[6]	5.00 BSC			0.1969 BSC		
D1	3.50 BSC			0.1378 BSC		
E	5.00 BSC			0.1969 BSC		
E1	3.50 BSC			0.1378 BSC		
e[9]	0.50 BSC			0.0197 BSC		
N[11]	64					
SD[12]	0.25 BSC			0.0098 BSC		
SE[12]	0.25 BSC			0.0098 BSC		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.08			0.0031		
eee	0.15			0.0059		
fff	0.05			0.0020		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. UFBGA stands for ultra profile fine pitch ball grid array: 0.5 mm < A ≤ 0.65 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metalized markings, or other feature of package body or

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integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

Figure 51. UFBGA64 – Footprint example

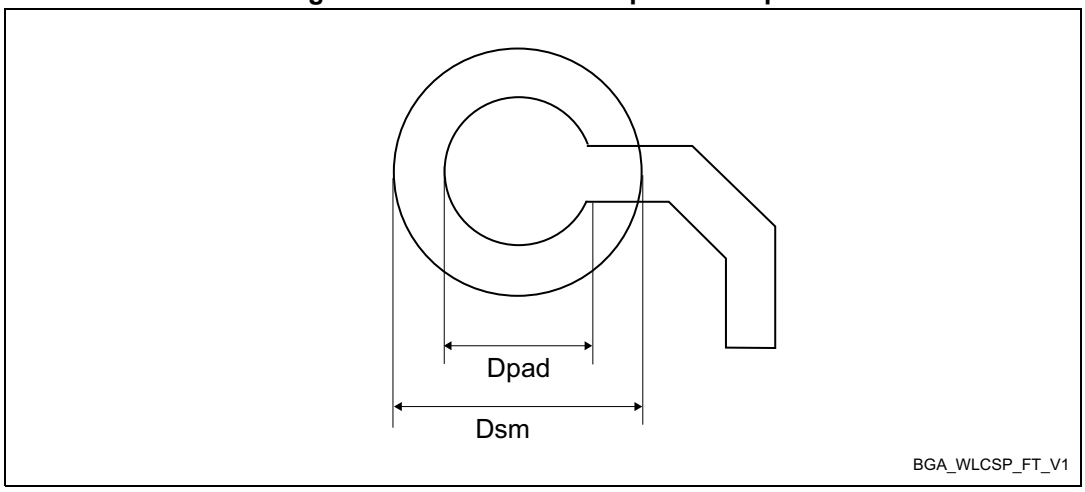


Table 78. UFBGA64 - Example of PCB design rules (0.5 mm pitch BGA)

Dimension	Values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

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6.11 Thermal characteristics

The operating junction temperature T_J must never exceed the maximum given in *Table 24: General operating conditions*.

The maximum junction temperature in °C that the device can reach if respecting the operating conditions, is:

$$T_J(max) = T_A(max) + P_D(max) \times \Theta_{JA}$$

where:

- $T_A(max)$ is the maximum operating ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D = P_{INT} + P_{I/O}$,
  - P_{INT} is power dissipation contribution from product of I_{DD} and V_{DD}
  - $P_{I/O}$ is power dissipation contribution from output ports where
    $P_{I/O} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH})$, taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 79. Thermal resistance

Symbol	Parameter	Package[1]	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	WLCSP19	101.9	°C/W
		TSSOP20	81.4	
		UFQFPN28	TBD[2]	
		UFQFPN32	42.9	
		LQFP32	54.3	
		UFQFPN48	32.4	
		LQFP48	54.3	
		LQFP64	47.2	
		UFBGA64	69.1	
Θ_{JB}	Thermal resistance junction-board	WLCSP19	74.6	°C/W
		TSSOP20	52.2	
		UFQFPN28	TBD[2]	
		UFQFPN32	24.8	
		LQFP32	31.6	
		UFQFPN48	16.7	
		LQFP48	31.6	
		LQFP64	29.6	
		UFBGA64	52	

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Table 79. Thermal resistance

Symbol	Parameter	Package[1]	Value	Unit
Θ_{JC}	Thermal resistance junction-case	WLCSP19	7.7	°C/W
		TSSOP20	26	
		UFQFPN28	TBD[2]	
		UFQFPN32	21.3	
		LQFP32	20.4	
		UFQFPN48	13.3	
		LQFP48	20.4	
		LQFP64	17.4	
		UFBGA64	24.7	

1. Refer to *Section 6: Package information* for package dimensions
2. Value not yet defined. TBD stands for *to be defined*.

6.11.1 Reference documents

[1] *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)* (JESD51-2A), JEDEC, January 2008. Available from www.jedec.org.

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7 Ordering information

Example STM32 C 071 F B P 6 xyy

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

C = general-purpose

Device subfamily

071 = STM32C071

Pin count

F = 19 or/and 20
G = 28
K = 32
C = 48
R = 64

Flash memory size

8 = 64 Kbytes
B = 128 Kbytes

Package type

I = UFBGA
T = LQFP
U = UFQFPN
Y = WLCSP
P = TSSOP

Temperature range

6 = -40 to 85°C (105°C junction)
7 = -40 to 105°C (125°C junction)
3 = -40 to 125°C (130°C junction)

Options

xTR = tape and reel packing; x = N (“N” product version), otherwise blank
x = tray packing; x = N (“N” product version) or blank
other = 3-character ID incl. custom flash memory code and packing information; the leading character is N for “N” product version

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact your nearest ST sales office.

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9 Revision history

Table 80. Document revision history

Date	Revision	Changes
09-Sep-2024	1	Initial release.

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