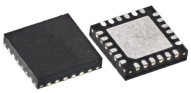
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ST25R100

Datasheet

NFC/HF RFID reader IC



UFQFPN24

(4x4 mm)

Product status link
ST25R100

Features

Operating modes

- Reader/Writer

RF communication

- ISO14443A/NFC-A at 106 kbit/s
- ISO14443B/NFC-B at 106 kbit/s
- ISO15693/NFC-V up to 53 kbit/s
- NFC Forum T1T, T2T, T4T, and T5T tag types
- Proprietary protocols, such as Kovio, CTS, B'
- Low level modes to implement MIFARE Classic® compliant or other custom protocols

Key features

- Improved low power card detection based on inductive wake-up
- High output power with dynamic power output (DPO)
- Option to connect two independent single-ended antennas
- Adjustable ASK modulation depth
- Automatic gain control and squelch feature to maximize SNR (signal-to-noise ratio)
- Integrated regulators to boost system PSRR
- Measurement of antenna characteristics (I/Q channels)
- 256-byte FIFO

External communication interfaces

- Serial peripheral interface (SPI) up to 6 Mbit/s

Electrical characteristics

- Supply voltage range, from 2.7 to 5.5 V
- Peripheral communication supply range, from 2.7 to 5.5 V
- Antenna driver voltage range, up to $6V_P$
- Quartz oscillator capable of operating with 27.12 MHz crystal with fast startup

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Applications

The ST25R100 is suitable for a wide range of NFC and HF RFID applications in the consumer and industrial segment, among them:

- Healthcare
- Access control
- Beauty and lifestyle
- Kitchen and home appliances
- Gaming and education
- Home automation and entertainment
- Industrial and tools
- IoT

Enabled by the extensive feature set, the ST25R100 can be used to implement use cases like:

- Brand protection
- Accessory recognition
- Automatic parameter setting
- Identification
- Metering
- Transportation and ticketing
- User interaction and consumer engagement

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1 Description

Delivering high-end performance in a small 4x4 mm package, the ST25R100 multipurpose NFC transceiver brings the convenience of contactless interaction and features to a variety of end applications. It is especially optimized for end products in consumer and industrial segments.

The ST25R100 supports NFC reader/writer mode. The high output power allows easy integration into applications with small antennas. The reader has an excellent read range and comes with an improved low power card detection (LPCD), increasing detection range in inductive wake-up mode. During this low power wake-up mode, the system is capable of detecting the approach or the removal of tags. The IC contains an RC oscillator and programmable timer to automatically scan for cards or other NFC-enabled devices like a smartwatch or a phone when in WU mode.

The high sensitivity of the ST25R100, supported by ST's noise suppression receiver (NSR) technology, allows successful reads even in noisy environments.

The device includes an advanced analog front end (AFE) and a highly integrated data framing system for NFC-A/B (ISO 14443A/B) and NFC-V (ISO 15693) to read cards. The transparent mode of the AFE can be used to implement other custom protocols in reader mode.

The ST25R100 comes in a compact 4x4mm 24-pin TQFN package, allowing the integration of NFC technology in small devices.

The ST25R100 is designed to operate from a wide power supply range (2.7 to 5.5 V) and a wide peripheral IO voltage range (from 2.7 to 5.5 V), within a broad ambient temperature range from -25 °C up to +85 °C.

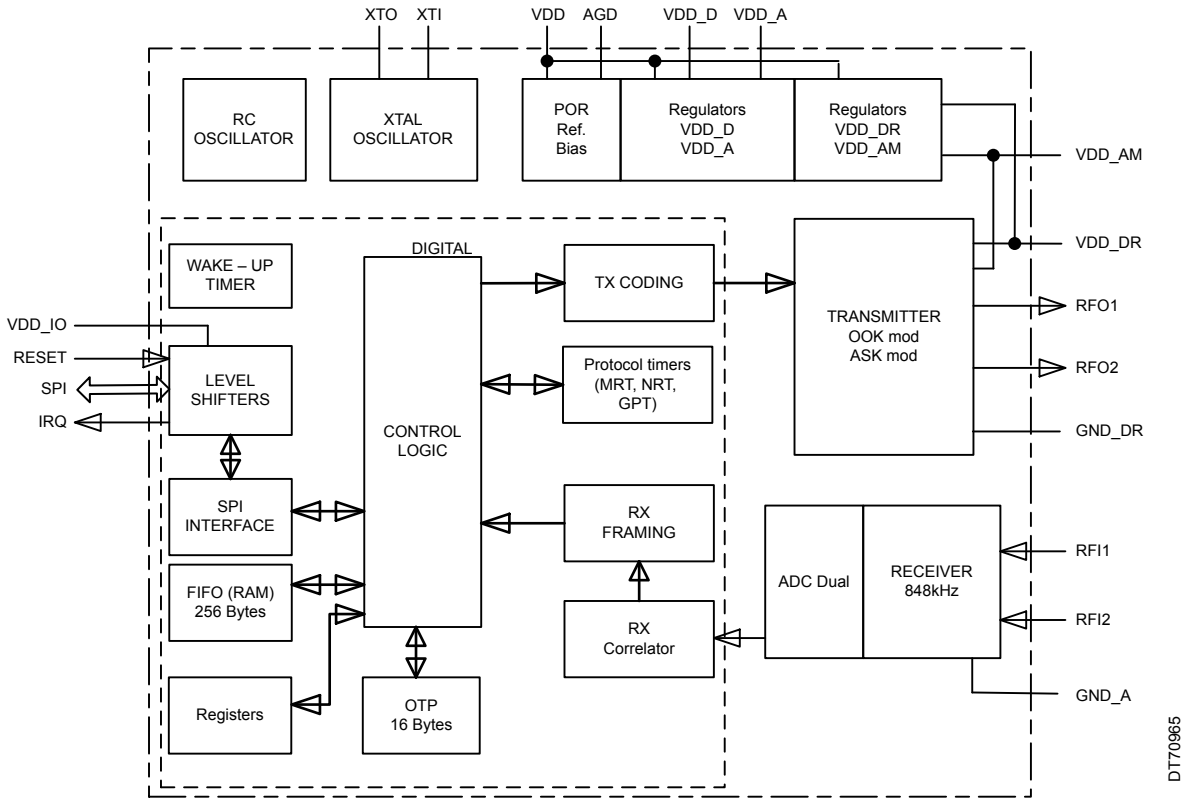
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2 Functional overview

2.1 Block diagram

The ST25R100 block diagram is shown in Figure 1.

Figure 1. Block diagram



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2.1.1 Transmitter

The transmitter incorporates the drivers, which drive the external antenna through pins RFO1 and RFO2. Both single-ended and differential antenna configurations are supported. The transmitter block also generates the OOK or AM modulation of the transmitted RF signal.

The transmitter can either operate RFO1 and RFO2 independently to drive up to two antennas in single ended configuration or operate RFO1 and RFO2 combined to drive one antenna in differential configuration. The drivers are designed to directly drive antenna(s) integrated on the PCB as well as antennas connected with 50 Ω cables.

2.1.2 Receiver

The receiver detects card modulation superimposed on the 13.56 MHz carrier signal. The receiver chain incorporates several features that enable reliable operation in challenging and noisy conditions.

The receiver is connected to the antenna via the pins RFI1 and RFI2. The output of the receiver is connected to the framing block that decodes the demodulated and digitized subcarrier signal.

2.1.3 Quartz crystal oscillator

The quartz crystal oscillator operates with 27.12 MHz crystals. At startup, the transconductance of the oscillator is increased to achieve a fast startup. Since the startup time varies with crystal type, temperature and other parameters, the oscillator amplitude is observed and an interrupt is sent when stable oscillator operation is reached.

2.1.4 Power supply regulators

Integrated power supply regulators ensure a high power supply rejection ratio for the complete reader system. Different voltage regulators supply separate blocks in order to decouple from noise sources.

2.1.5 POR and bias

This block provides bias currents and reference voltages to all other blocks. It also incorporates a power on reset (POR) circuit, which provides a reset at power-up and at low supply levels.

2.1.6 RC oscillator and wake-up timer

The RC oscillator allows the wake-up timer to run and periodically trigger a measurement of its surroundings during wake-up mode.

2.1.7 Tx coding

This block encodes the transmit frames according to the selected RF communication mode and bit rate. It generates the SOF (start of frame), EOF (end of frame), CRC, and parity bits automatically. The data to be transmitted is taken from the FIFO.

2.1.8 Rx framing

This block decodes received frames according to the selected RF communication mode and bit rate. The SOF (start of frame), EOF (end of frame), CRC, and parity bits are automatically checked and removed by this block. The received data is then placed in the FIFO.

2.1.9 Control logic

This block drives all activity of the device based on the commands received via the serial interface and the configurations present on the registers.

2.1.10 FIFO

A 256-byte FIFO is available for exchanging data via the transmitter and receiver. Depending on the mode, it contains either data that has been received or data to be transmitted.

2.1.11 SPI

A 4-wire serial peripheral interface (SPI) is available for communication between the device and the host/ microcontroller.

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3 Pin and signal description

Figure 2. **UFQFPN24 pinout (top view)**

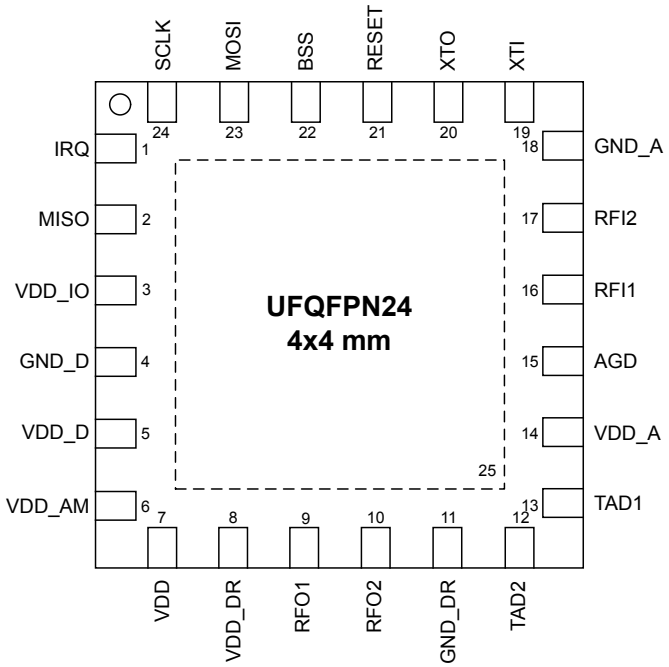


Table 1. **UFQFPN24 pin assignment**

UFQFPN24	Name	Type(1)	Description
1	IRQ	DO	Interrupt request output
2	MISO	DO_T	Serial peripheral interface data output
3	VDD_IO	P	External peripheral communication supply (5 V domain)
4	GND_D	P	Digital ground
5	VDD_D	AOS	Regulated supply for digital (1 V domain)
6	VDD_AM	AOS	Regulated driver supply for AM modulation (5 V domain)
7	VDD	P	External main positive supply (5 V domain)
8	VDD_DR	AOS	Regulated driver supply for antenna driver (5 V domain)
9	RFO1	AO	Antenna driver output
10	RFO2	AO	Antenna driver output
11	GND_DR	P	Antenna driver ground (it must be connected as short as possible to pin 25 (VSS) that is the exposed pad)
12	TAD2	AIO	Analog/Digital test pin (connect to test point or unconnected if not used)
13	TAD1	AO	Analog/Digital test pin (connect to test point or unconnected if not used)
14	VDD_A	AOS	Regulated supply for analog (3 V domain)
15	AGD	AIO	Analog reference voltage
16	RFI1	AI	Receiver input
17	RFI2	AI	Receiver input
18	GND_A	P	Analog ground
19	XTI	AI/DI	Crystal oscillator input

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UFQFPN24	Name	Type(1)	Description
20	XTO	AO	Crystal oscillator output
21	RESET	DI	Reset input
22	BSS	DI	Serial peripheral interface enable (active low)
23	MOSI	DI	Serial peripheral interface data input
24	SCLK	DI	Serial peripheral interface clock
25	VSS	P	Ground, die substrate potential, via exposed die pad

1.
- *AI: analog input*
- *AIO: analog I/O*
- *AO: analog output*
- *DI: digital input*
- *DIO: digital bidirectional*
- *DO: digital output*
- *DO_T: digital output/tri-state*
- *P: power supply pin*

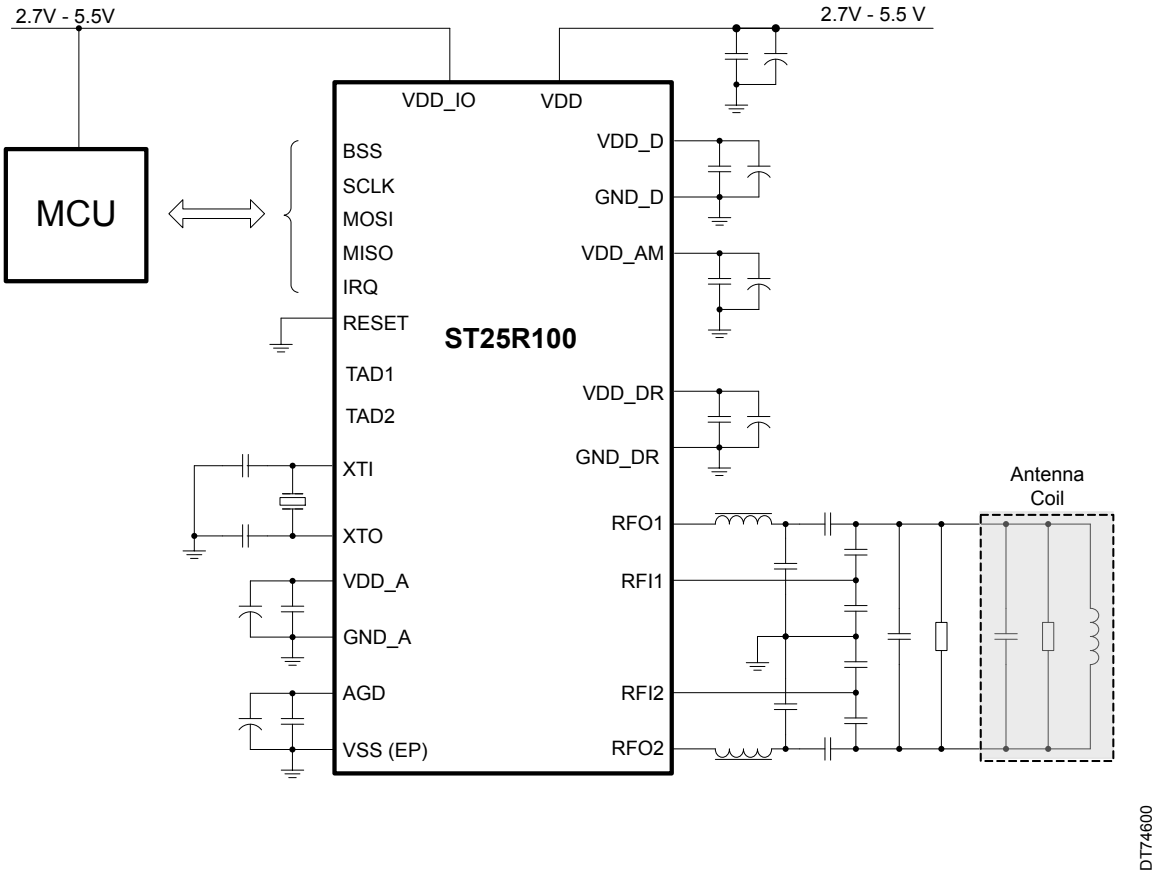
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4 Device description

4.1 System diagram

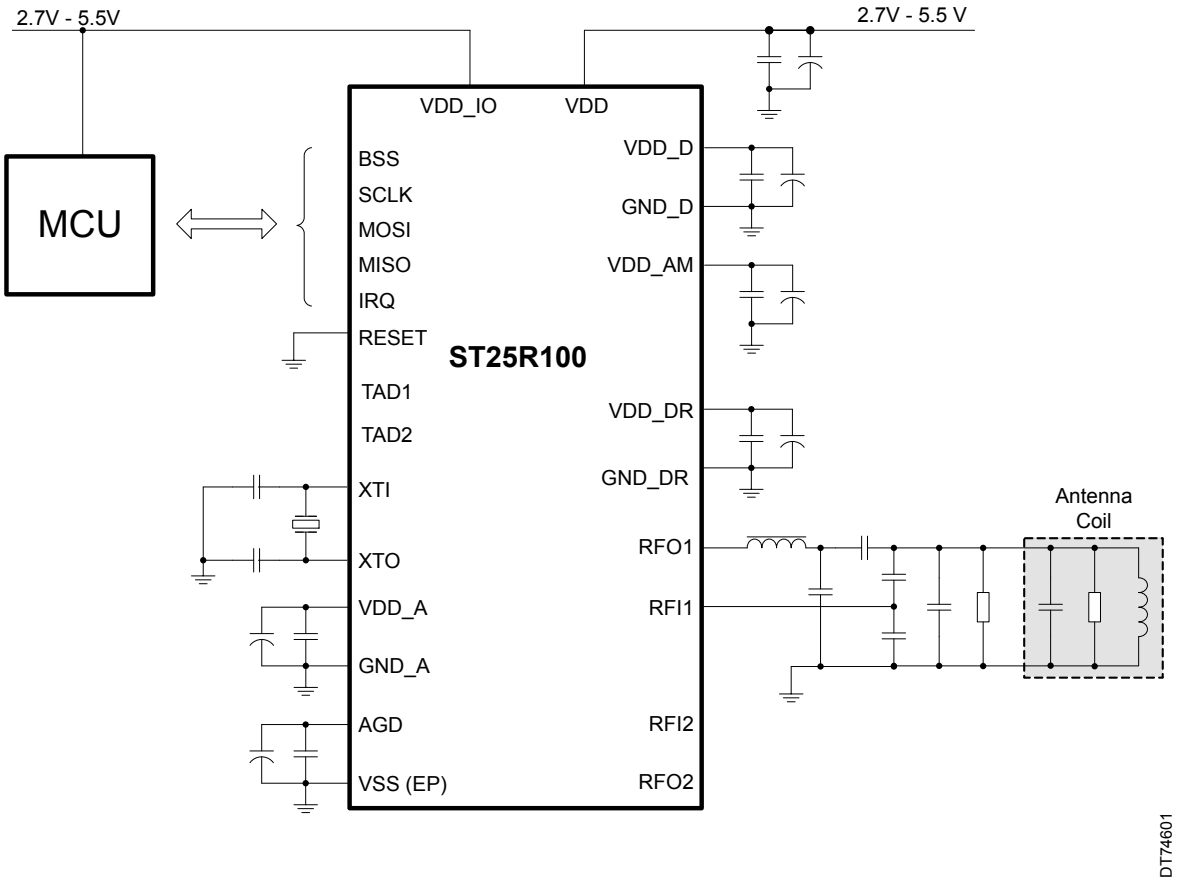
The minimum system configuration is shown below. Figure 3 and Figure 4 show the minimum system configuration for, respectively, differential and single ended antenna configurations. Both include the EMC filter.

Figure 3. System diagram - differential antenna driving



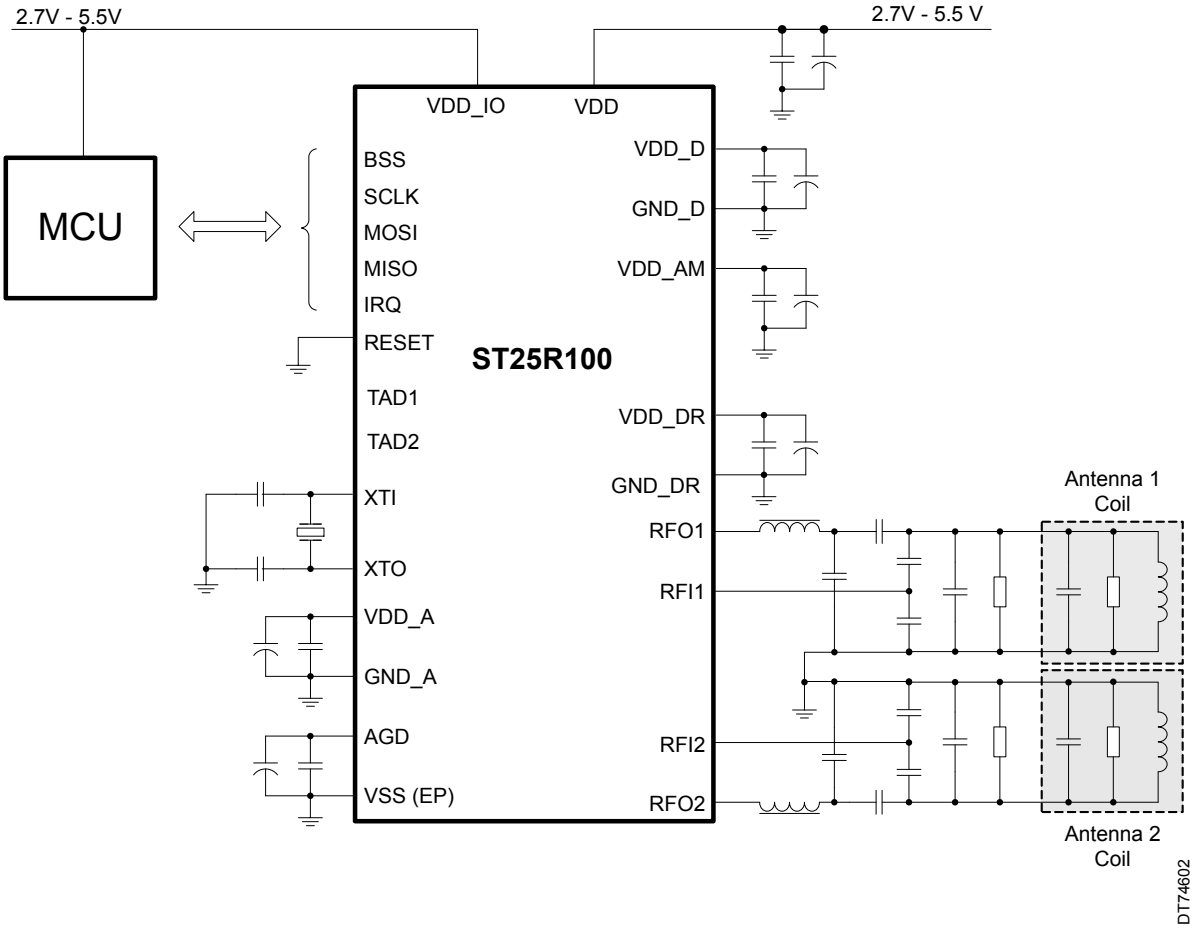
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Figure 4. **System diagram - single-ended antenna driving**



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Figure 5. **System diagram – two single-ended antenna driving**



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5 Application information

5.1 Operating modes

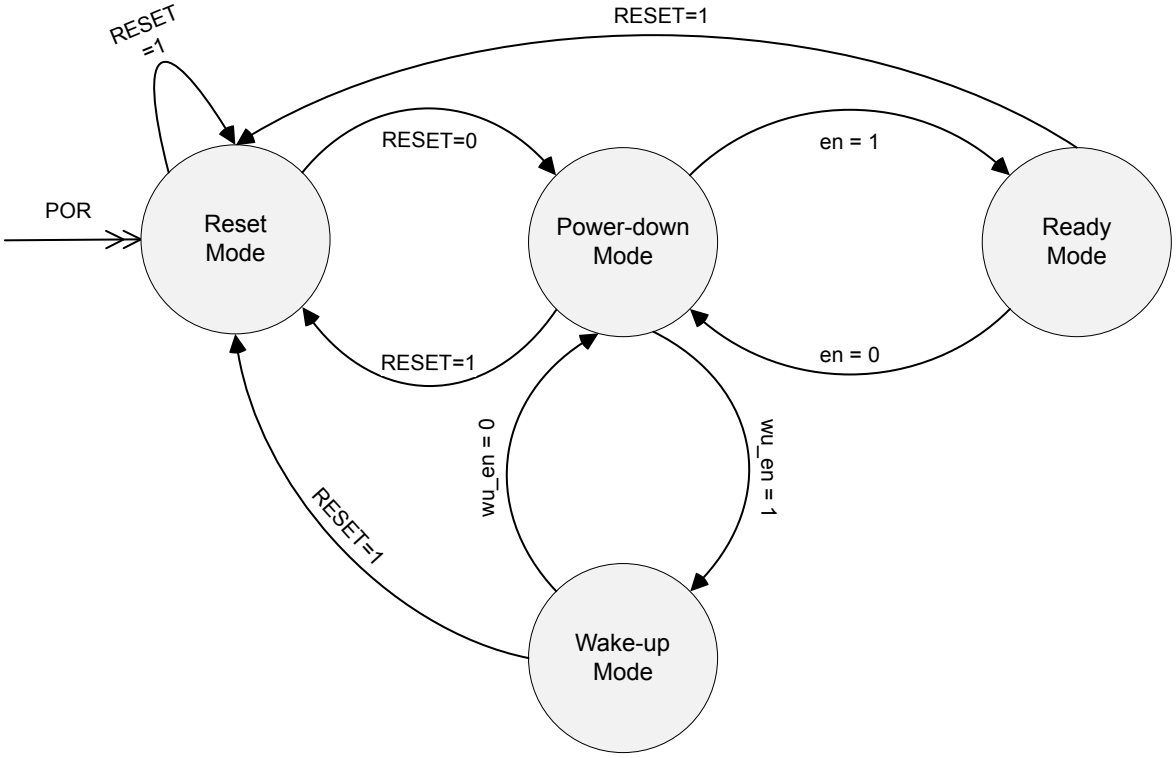
The device supports four operating modes:

- **Reset mode (RESET)**
  When the device is supplied and the RESET pin is high, the device is in reset mode. All blocks are deactivated, no clock is present, and consumption is minimized.
- **Power-down mode (PD)**
  At power-up and RESET pin is low, the device goes to power-down mode. In this mode, the AFE static power consumption is very low, but SPI communication is possible as well as register access to those in the PD domain.
  Blocks that are active in PD mode:
  – VDD_D regulator (1V) in low power mode
  – Registers in PD domain
- **Wake-up mode (WU)**
  Wake-up mode is controlled via the wu_en bit. In this mode, the device checks for a change in antenna properties in regular time intervals and triggers an IRQ in case a change was detected.
  Blocks that are active in WU mode:
  – VDD_D regulator (1V) in low power mode
  – Registers in PD domain
  – RC oscillator
  – WU timer
  – IRQ
- **Ready mode (RD)**
  Ready mode is controlled by en bit. In this mode, the regulators and crystal oscillator are enabled and the device is ready to transmit/receive. Blocks that are active in RD mode:
  – VDD_D regulator (1V) in normal power mode
  – All registers (both in PD and RD domain)
  – Main logic
  – VDD_A, VDD_DR, VDD_AM (depending on am_en bit) regulators
  – Crystal oscillator
  – IRQ

  When RD mode is reached (by enabling en bit) the devices issues an IRQ I_osc.

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Figure 6. **State diagram**



5.2 Power-on sequence

Once powered, the device enters the PD mode. The content of all registers is set to its default state.

One can set the device into any other operation mode by changing the configuration on the Operation register.

Transiting the device to RD mode and prepared for communication comprises on:

- Applying appropriate configuration on registers: Operation and General
- Setting en = 1 and waiting for the device to get ready and with oscillator stable (I_osc/osc_ok)
- The internal voltage regulators must be configured.

Once completed the device is ready for communication.

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5.3 Supply system

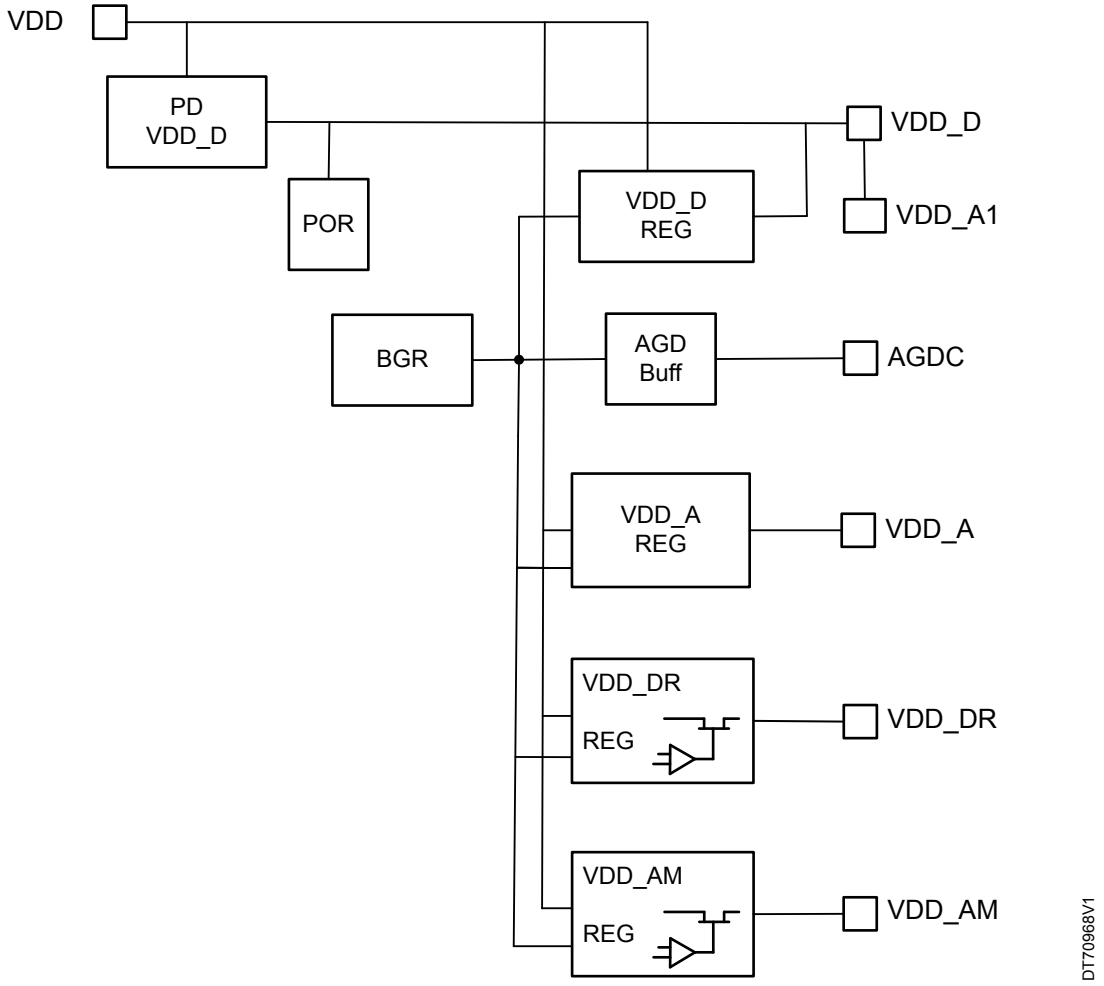
The ST25R100 features two positive supply pins:

- VDD_IO is used to define the supply level for digital communication pins (MISO, MOSI, SCLK, BSS, and IRQ). Digital communication pins interface with ST25R100 logic through level shifters, therefore the internal supply voltage can be either higher or lower than VDD_IO.
- VDD is the main power supply pin. It supplies the ST25R100 blocks through the following:
  - Regulator VDD_D
  - Regulator VDD_A
  - Regulator VDD_DR
  - Regulator VDD_AM

The recommended blocking capacitors for supply pins are as following:

- 2.2 µF in parallel with 10 nF for: VDD, VDD_DR, VDD_D, and VDD_AM (pin 5, 6, 7, and 8)
- 1 µF in parallel with 10 nF for AGD and VDD_IO (pin 3 and 15)

Figure 7. Supply system



Note:

- *BGR: Bandgap reference*

Figure 7 details the building blocks of the ST25R100 power supply system. It contains three regulators, a power-down support block, a block generating analog reference voltage (AGDC). The three regulators are providing supply to analog blocks (VDD_A), logic (VDD_D), and transmitter (VDD_DR).

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VDD_A and VDD_D regulators

VDD_A and VDD_D regulators are used to supply the ST25R100 analog and digital blocks respectively.

In power-down and wake-up modes, the VDD_D is in low power and is maintained by the power-down support block. In ready mode, the VDD_D is in normal mode and is supplied by the VDD_D regulator.

VDD_A is available in RD mode through the VDD_A regulator.

VDD_DR regulator

The purpose of this regulator is to improve the PSRR (power supply rejection ratio) of the transmitter (the noise of the transmitter power supply is emitted and fed back to the receiver).

The VDD_DR regulator operation is controlled and observed by accessing three regulator registers: general configuration, regulator configuration, and display register1.

Bit reg_s must be set to 1 so that the regulated voltage is defined by the bits rege<4:0>.

The VDD_DR regulator includes a current limiter that limits the regulator current to 250 mA in normal operation. The bit i_lim is set when the VDD_DR regulator is in current limiting mode.

In power-down mode, the VDD_DR regulator is not operating. Output is connected to VDD through the 1 kΩ resistor.

VDD_AM regulator

This regulator is used to support the transmitter AM modulation. Its output voltage is used as a transmitter supply during the modulation phase. The output is internally connected to the transmitter. It requires decoupling capacitors at the VDD_AM pin.

VDD_DR is used as a reference voltage, resulting in the correct VDD_AM voltage and modulation index across the supply voltage range.

The output voltage and therefore the modulation setting is controlled by the am_mod<3:0> option bits from 8 to 55 % in 16 steps.

In PD mode, the VDD_AM regulator is not operating. The VDD_AM pin is connected to the V_{DD} through a 1 kΩ resistor.

Note: The actual modulation index may deviate from the target set by am_mod<3:0> when considerable RFO driver resistance is added via d_res<3:0>.

5.4 Power-down support block

In PD mode the regulators are disabled in order to save current. In this mode a low power power-down support block maintains the VDD_D.

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5.5 Crystal oscillator

The crystal oscillator operates with 27.12 MHz crystals. The operation of the quartz crystal oscillator is enabled when the option bit en is set to one.

The oscillator is based on an inverter stage supplied by the controlled current source. A feedback loop is controlling the bias current in order to regulate the amplitude on XTI/XTO pins to approximately 1Vpp.

Division by two assures that the 13.56 MHz signal has a duty cycle of 50%, which is better for the transmitter performance (no PW distortion).

The ADC and preprocessing block are clocked directly with 27.12 MHz. All other blocks operate at 13.56 MHz or lower, generated in the main logic. An interrupt (I_osc) is sent to inform the host that stable oscillator operation is reached.

The status of the oscillator can be observed by checking the osc_ok display bit. This bit is set to one when the oscillator frequency is stable.

5.6 RC oscillator

RC oscillator is used to support the low power WU mode, and it runs at the frequency of 26.48 kHz nominal. It is enabled when the device enters the WU mode, and is disabled when the device goes to PD or RD mode. Additionally, it may be enabled by execution of the direct command start wake-up timer.

5.7 Communication with an external host

The ST25R100 communicates with a host via an SPI interface where it acts as a slave device, relying on the host to initiate all communication.

To notify the host of completed commands or external events that the ST25R100 signals an interrupt on the IRQ pin.

A RESET pin is also available in order to reset the device logic.

5.7.1 Interrupt interface

There are three interrupt registers implemented in the ST25R100.

When an interrupt condition is met, the source of the interrupt bit is set and the IRQ pin transitions to high.

In order to distinguish between different interrupt sources the host reads the interrupt registers. After a particular interrupt register is read, its content is reset to 0.

The IRQ pin transitions to low after the interrupt bit(s) that caused its transition to high has(have) been read.

Note: There may be more than one interrupt bit set if the host does not immediately read the interrupt registers after the IRQ signal is set and another event causing an interrupt occurs. In this case, the IRQ pin transitions to low after the last bit causing the interrupt is read.

If an interrupt from a certain source is not required, it can be disabled by setting the corresponding bit in the mask interrupt registers. In the case of masking a certain interrupt source the IRQ line is not set high, but the interrupt status bit is still set in the IRQ status registers.

By reading the IRQ status registers, the masked interrupt bits are also retrieved and cleared.

In case an interrupt is masked and its bit set to high due to a previous IRQ event, and then the host unmasked this particular IRQ source, the IRQ line is immediately set to high. This notifies the host system that there are some interrupt events not yet read out.

5.7.2 Serial peripheral interface (SPI)

The ST25R100 has a standard serial peripheral interface with clock polarity of 0, a clock phase of 1, and an active low slave select signal. The SPI speed up to 10 Mbit/s is available. The communication starts with the master pulling BSS low. The MOSI pin is sampled on the falling edge of SCLK, and the state of the MISO pin is updated on the rising edge of the SCLK signal. The data is transferred byte-wise, the most significant bit first. The read and write commands support an address auto increment to reduce communication time.

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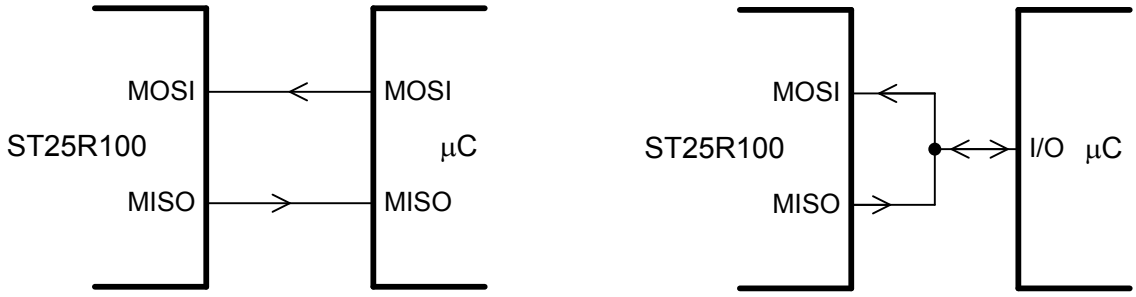
Table 2. SPI signal lines

Name	Signal	Signal level	Description
BSS	Digital input	CMOS	SPI enable (active low)
MOSI	Digital input	CMOS	Serial data input
SCLK	Digital input	CMOS	Clock for serial communication
MISO	Digital output with tristate	CMOS	Serial data output

MISO output is usually in tristate. It is only driven when output data is available. Due to this the MOSI and the MISO can be externally shorted to create a bidirectional signal.

During the time the MISO output is in tristate, it is possible to switch on a 10 kΩ pull down by activating option bits miso_pd1 and miso_pd2.

Figure 8. SPI data signals with a host



The following addressing scheme is used:

- Bit 7 indicates the direction of the operation (0-Write / 1-Read)
- 95 addressable registers (0x00 - 0x5E)
- 64 command codes (0x60 - 0x7F and 0xE0 - 0xFF)
- FIFO access (0x5F)
- Test/OTP registers access (0xFC)

For specific details on ST25R100 registers and commands, refer to the Registers and Direct commands.

Table 3. SPI operation modes

MODE	MODE pattern (com. bits)								Related data
	R/W	B6	B5	B4	B3	B2	B1	B0	
Register write	0	A6	A5	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto-incrementing) A<6,0>=0x5E max
Register read	1	A6	A5	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto-incrementing) A<6,0>=0x5E max
Commands	C7	1	1	C4	C3	C2	C1	C0	-
Test	1	1	1	1	1	1	0	0	Enable access to test registers
FIFO write	0	1	0	1	1	1	1	1	One or more bytes of FIFO data
FIFO read	1	1	0	1	1	1	1	1	One or more bytes of FIFO data

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Writing of data to addressable registers (write mode)

The following figures show cases of writing a single byte and writing multiple bytes with auto-incrementing address. After the SPI operation direction bit, the address of the register to be written is provided. Then one or more data bytes are transferred from the SPI, always from the MSB to the LSB. The data byte is written in the register on the falling edge of its last clock. In the event that the communication is terminated by setting BSS high before an 8-bit packet composing one byte is sent, the writing of this register is not performed. In case the register on the defined address does not exist or it is a read only register no write is performed.

Figure 9. SPI communication: writing of single byte

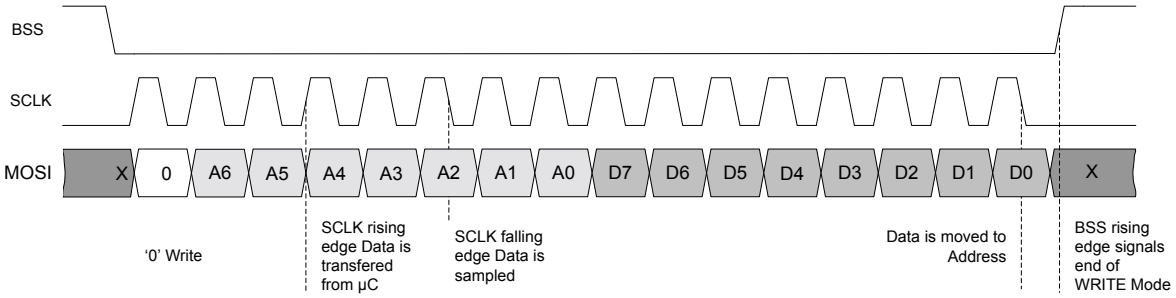
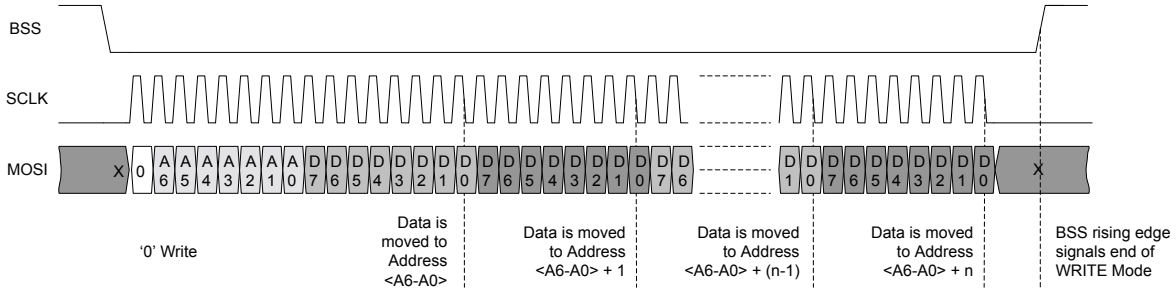


Figure 10. SPI communication: writing of multiple bytes



Reading of data from addressable registers (read mode)

After the SPI operation direction bit, the address of the register to be read has to be provided from the MSB to the LSB. Then one or more data bytes are transferred to the MISO output, always from the MSB to the LSB. Analogous to the write mode, also the read mode supports auto-incrementing address.

MOSI is sampled at the falling edge of SCLK (like shown in the following diagrams), data to be read from the device internal register is driven to the MISO pin on the rising edge of SCLK and is sampled by the master at the falling edge of SCLK.

In case the register on the defined address does not exist, all 0 data is sent to MISO.

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Figure 11. **SPI communication: reading of single byte**

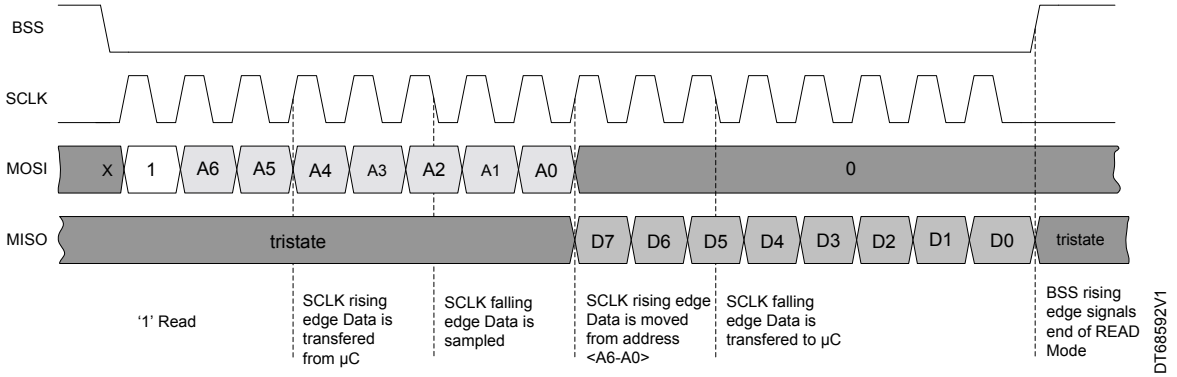
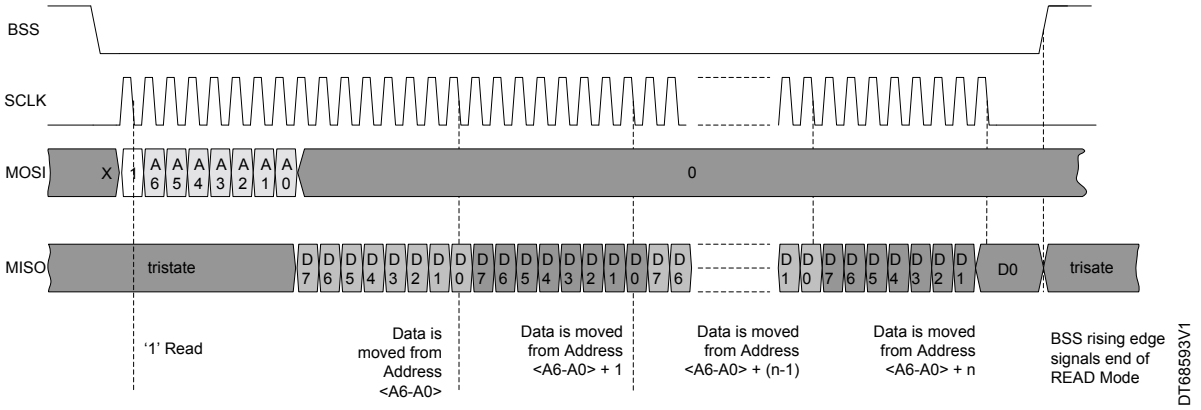


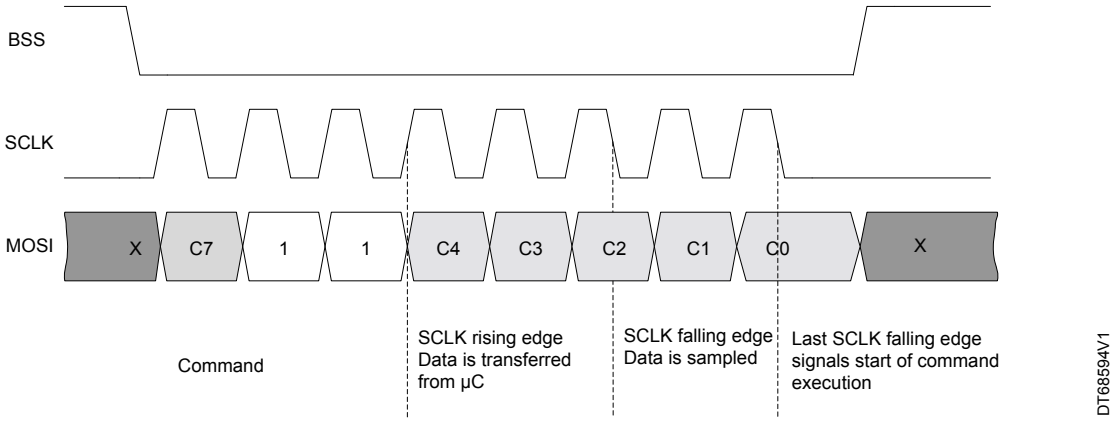
Figure 12. **SPI communication: reading of multiple bytes**



Direct command mode

The direct command mode has no additional data apart from the command code itself, therefore a single byte is sent MSB first. Execution of the direct command starts after the last clock.

Figure 13. **SPI communication: direct command**

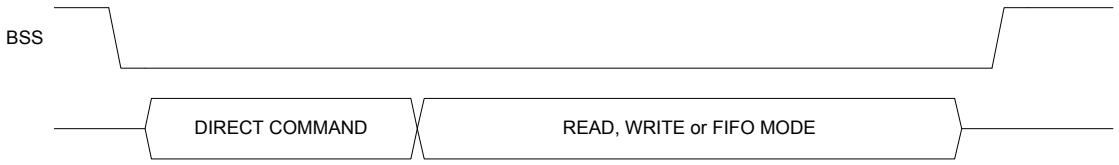


While the execution of some direct commands is immediate, there are others that start a process of certain duration (for instance calibration, and measurements). During the execution of such commands it is not allowed to start another activity over the SPI interface, an IRQ is sent when the execution has terminated.

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Direct commands with immediate execution can be followed by another SPI mode (read, write, or FIFO) without deactivating the BSS signal in between.

Figure 14. SPI communication: direct command chaining



FIFO mode

Reading received data from the FIFO is similar to reading data from the addressable registers. Read and write operations are performed by accessing the address 0x5F, resulting in 0x5F for a write operation and 0xDF for a read operation.

Figure 15. SPI communication: writing bytes into FIFO

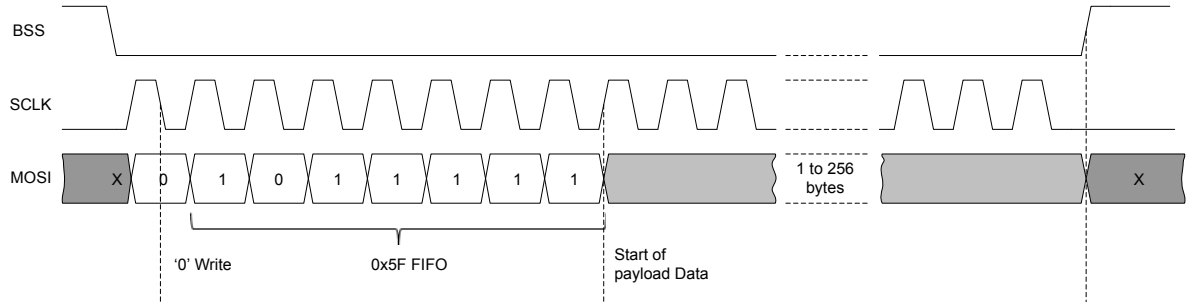
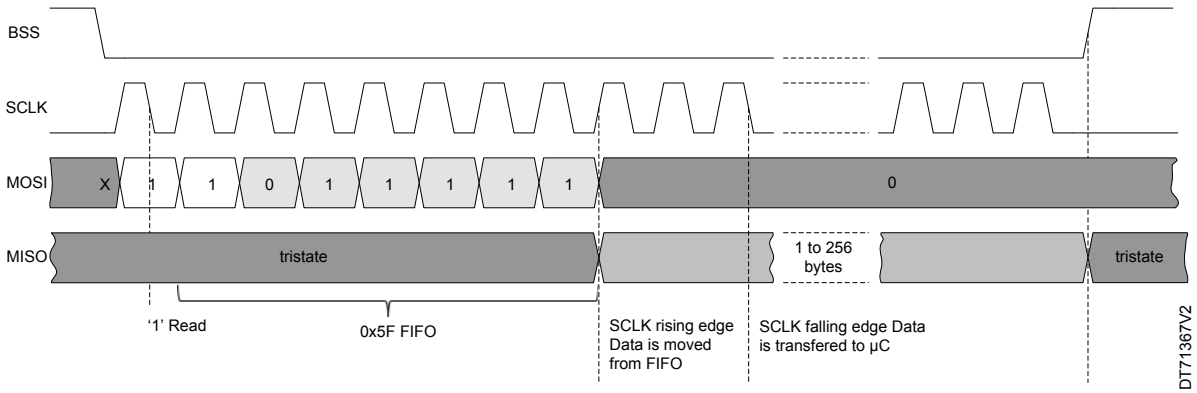


Figure 16. SPI communication: reading bytes from FIFO



5.7.3 FIFO block

The ST25R100 features a 256 bytes FIFO. The control logic shifts the data during transmission, which was previously loaded by the external host to the framing block and further to the transmitter. During reception, the demodulated data is stored in the FIFO and the host can receive data at a later moment.

The FIFO status register 2 also contains two bits that indicate that the FIFO was not correctly served during the transmission or reception process (FIFO overflow and FIFO underflow).

A FIFO overflow is set when too much data is written into the FIFO.

When this bit is set during Rx, the external controller did not react on time on the water level IRQ and more than 256 bytes were written into the FIFO. Consequently, the received data is corrupted.

When an overflow happens during transmission, it means that the controller has written more data than the FIFO size. The data to be transmitted is corrupted.

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A FIFO underflow is set when data was read from an empty FIFO.

When this bit is set during reception, the host read more data than was actually received.

When an underflow happens during transmission, it means that the controller has failed to provide the quantity of data defined in the number of transmitted bytes registers on time.

FIFO pointers and FIFO status are reset at the start of each data reception (I_rxs). They are also reset at power-up and by commands set default and clear FIFO. Reading out data from empty/cleared FIFO shows data as zeros.

5.8 Timers

Several timers are integrated in the device in order to eliminate the need to runtime critical tasks with counters/timers on the host side, sampling system integration and improve its portability.

Each timer has one or more associated configuration registers in which the timeout duration and different operating modes are defined. These configuration registers have to be set while the corresponding timer is not running. Any modification of timer configuration while the timer is active may result in unpredictable behavior.

All timers can be stopped by the direct command stop all activities.

Mask receive timer (MRT)

This timer blocks the receiver and reception process in framing logic by keeping the rx_on signal low after the end of transmission during the time that the tag reply is not expected.

While the mask receive timer is running the squelch can be automatically turned on.

The MRT does not produce an IRQ.

The MRT timeout is configured in the MRT SQT configuration register and MRT registers. It is automatically started at the end of data transmission (at the end of EOF). In case MRT = 0 the timer does not run at the end of transmission and the receiver remains blocked.

Additionally, the MRT can be triggered by starting the MRT direct command.

No-response timer (NRT)

The NRT is intended to observe whether a Tag/Listener response was detected within a configured time frame, starting from the end of data transmission.

The IRQ with I_nre flag is triggered at the NRT timeout.

The NRT is configured by writing the NRT1/2 and NRT GPT configuration registers.

The NRT is started at the end of data transmission (at the end of EOF).

Bit nrt_step configures the time step of the no-response timer. Two steps are available, 64/fc (4.72 µs), which covers range up to 309 ms and 4096/fc, which covers range up to 19.8 s.

NRT supports two operating modes controlled by bit nrt_emd:

- When nrt_emd=0 (default mode), the IRQ is produced in case the NRT expires before a start of a Tag/Listener reply is detected. Additionally, the rx_on is set low to disable the receiver.
  In the opposite case, when the start of a tag reply is detected before the timeout, the timer is stopped, and no IRQ is produced.
- When nrt_emd=1 the NRT unconditionally produces an IRQ when it expires. This means that IRQ is independent from whether or not a tag reply was detected.
  When a tag reply is being processed during a timeout, no other action is taken and the reply is normally received.
  In the opposite case, when no tag response is being processed additionally the receiver is disabled.

Additionally, the NRT can be started using the direct command start NRT. The intention of this command is to extend the NRT timeout. In case this command is sent while the timer is running, it is reset and restarted.

The NRT can be terminated using the direct command stop NRT or stop all activities. The timer is terminated and no IRQ is sent. It is expected to be used when nrt_emd=1, where an incoming reception does not stop the NRT.

General purpose timer (GPT)

The GPT can be used for multiple purposes, as it allows it to be triggered manually or by several other trigger sources. It can be used to measure the duration of the reception process (triggering by start of reception, after SOF), or to time out the reader frame after the tag's reception (triggered by end of reception, after EOF).

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The GPT can be started by sending the direct command start GPT. If this command is sent while the timer is running, it is reset and restarted.

The GPT can be terminated using the direct command stop all activities.

Wake-up timer (WUT)

This timer is primarily used in the wake-up mode.

It can also be triggered by sending the direct command start WUT. When this command is sent, the RC oscillator, which is used as the clock source for the wake-up timer, is started. When the timer expires, an IRQ with the I_wut flag is sent.

As the RC oscillator is the clock source for the WUT, it can run during PD mode. The other timers, which are based on the crystal oscillator, cannot be used in PD or WU mode.

Note: The tolerance of WUT is defined by the tolerance of the RC oscillator.

5.9 Reader operation

To perform the function of the reader, the ST25R100 must be placed in RD mode as detailed on Section 5.2: Power-on sequence. Once in RD mode, the mode (om<3:0>) and bitrates (tx_rate<1:0>, rx_rate<1:0>) to be used must be defined, as well as all the needed configurations for the transmitter and receiver paths. Both the transmitter (tx_en) and receiver (rx_en) shall be enabled.

Several NFC standards define a guard time, which requires that the reader field must be turned on for a certain duration (for instance 5 ms for ISO14443A/B) before the first command is sent.

Recommended preparation and execution of a transceiver operation:

- Execute the direct command stop all activities
- Execute the direct command reset Rx gain
- Configure the timers accordingly
- Define the length of data to be transmitted (ntx<12:0> and nbtx<2:0>)
- Write the bytes to be transmitted in the FIFO
- Send the direct command transmit data
- When all the data is transmitted, an IRQ is sent to inform the host that the transmission is finished (I_txe)

After the transmission is completed, the receiver automatically starts to observe the RFI inputs to detect a tag response. In case it is enabled (sq_en, agc_en) the squelch and AGC are started, the framing block processes the subcarrier signal from the receiver and fills the FIFO with data. When the reception is started an IRQ with the flag I_rxs is signaled, and the data is placed in the FIFO. When reception is completed an IRQ is sent to the host (I_rxe), and the FIFO status register 1 and FIFO status register 1 display the amount of data in the FIFO and further information so the host can process it. When data frames longer than the FIFO are to be transmitted or received an additional step is needed.

During transmission, when the remaining number of bytes is lower than the FIFO water level, an IRQ due to the FIFO water level (I_wl) is signaled. The host then shall add more data in the FIFO. This step shall be repeated the number of times needed to transmit the full frame. When all the data is transmitted, an IRQ (I_txe) is sent to inform the host that the transmission has finished.

Similarly during reception, when the FIFO is loaded with more data than the FIFO water level, an IRQ (I_wl) is sent and the host shall retrieve the data from the FIFO. This step shall be repeated the number of times needed to receive the full frame. When the reception is finished, an IRQ (I_rxe) is sent to the host and the remainder of the data could be retrieved from the FIFO. FIFO water level is 128 bytes on both directions (transmission and reception).

The diagrams below depict a few examples of transceiver operations.

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Figure 17. **Transceiver operation with timeout**

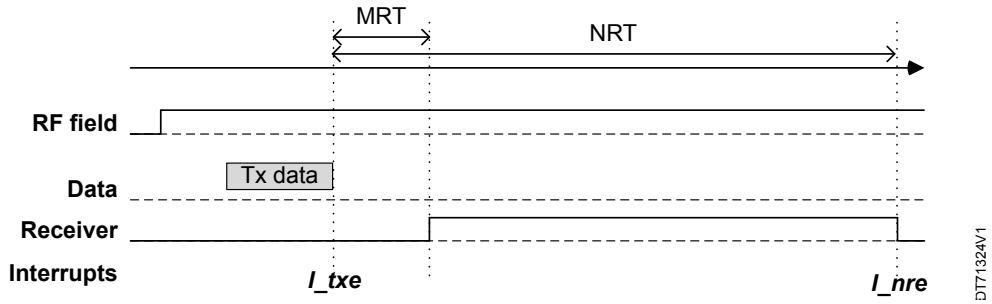


Figure 18. **Transceiver operation with nrt_emd=0**

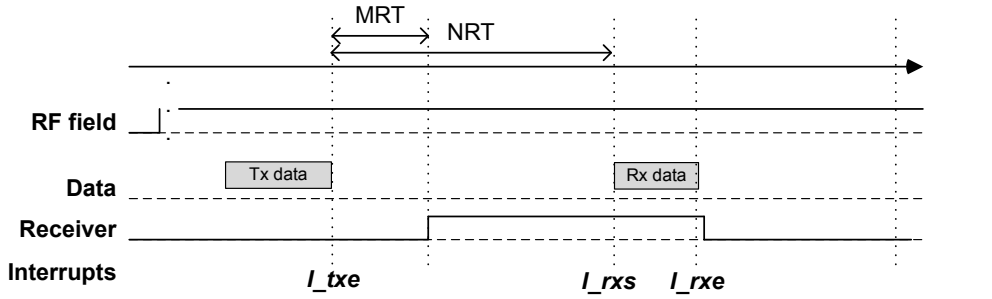
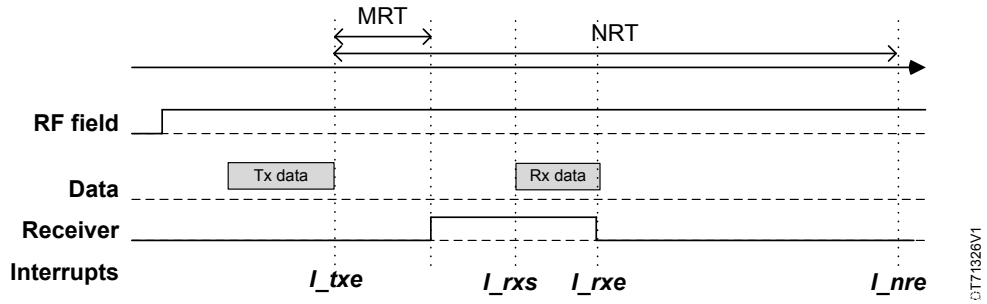


Figure 19. **Transceiver operation with nrt_emd=1**



5.9.1 ISO14443A/NFC-A short frames

ISO14443A/NFC-A short frames (REQA/SENS_REQ and WUPA/ALL_REQ) are transmitted in the same manner via the FIFO. The number of data to be sent shall be defined to zero bytes and seven bits. As the response to these requests (ATQA/SENS_RES), does not contain CRC, the bit rx_crc shall be cleared.

5.9.2 Bit oriented anti-collision

In order to receive bit oriented anti-collision frames, the bit antcl has to be set.

For ISO14443A/NFC_A bit oriented anti-collision, the bit rx_nbtx shall be set so that nbtx<2:0> define the position of the first bit in the first byte in consecutive reception.

Bit oriented anti-collision can be performed for both ISO14443A/NFC-A and ISO15693/NFC-V. When bit antcl is set:

- Level coll_lvl is used to detect colliding bits
- Detected collision is signaled via IRQ with the flag I_col
- The position of the first bit collision detected is available in the collision register
- The first parity bit is ignored in case the split happens within the byte

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5.10 Wake-up mode

Once in PD mode, the bit wu_en sets the ST25R100 into wake-up mode (WU), which is used to perform low power card detection. An integrated low power 26.48 kHz RC oscillator and configurable wake-up timer (WUT) are used to trigger periodic measurements.

Usually the presence of a card is detected by RF/NFC polling. In this process, the reader field is periodically turned on and the host checks whether a card is present using RF commands. This procedure consumes considerable energy since the reader emits a field for long periods before a command can be issued, due to guard time fulfillment.

Low power detection of card presence is performed by detecting a change in the reader environment, produced by an approaching detuning element. When a change is detected, an interrupt is sent to the host. The host can then perform the regular RF/NFC polling afterwards.

In wake-up mode the ST25R100 performs periodic measurements and sends an IRQ to the host when a difference to the configured reference value is detected.

The ST25R100 monitors the I and Q channels to assess a variation on the antenna surroundings.

The latest measurement value is shown in i_adc<7:0> and q_adc<7:0>, and the current reference is defined on i_ref<7:0> and q_ref<7:0>. ADC values are provided in 8-bit signed values using two's complement representation. The delta/difference to the reference that triggers a wake-up interrupt is defined in i_diff<5:0> and q_diff<5:0>.

Card detection

The presence of a card close to the reader antenna coil produces a change of the antenna LC tank signal. The reader field activation time required to perform the measurement is extremely short, compared to the activation time required to send a protocol activation command.

The power level during the measurement can be lower than that during normal operation as the card does not have to be powered to produce a coupling effect. The emitted power can be configured by changing the RFO driver resistance.

An IRQ is sent when the difference between a measured value and reference value is larger than the configured delta/diff value. There are two possibilities how to define the reference value, controlled by the bit iq_aaref:

- The ST25R100 can automatically calculate the reference based on previous measurements (auto-averaging)
- The host determines the reference value(s) and sets it on i_ref<7:0> and q_ref<7:0>

Auto-averaging

In case auto-averaging is enabled (iq_aaref = 1) the reference value is recalculated after every measurement. The last measurement value, the old reference value, and the weight are used in this calculation.

The following formula is used to calculate the new reference value:

```
new_reference = old_reference - (old_reference - measured_value) / weight
```

The bits i_iirqm and q_iirqm define whether a measurement that causes an interrupt is taken into account for the average value calculation.

The influence that the new measurement has over the reference can be configured by a weight defined in bits i_aaw<1:0> and q_aaw<1:0>

Calibration

The wake-up mode has an additional calibration step that can be executed manually or automatically. Bits skip_cal and skip_recal control the automatic calibration behavior.

When starting the wake-up mode, if skip_cal = 0 a calibration step is performed automatically on the first WUT timeout.

While the wake-up mode is running and skip_recal = 0, in case the reference ± delta/diff is larger than 63, a recalibration is performed.

Wake-up IRQ

ST25R100 allows to configure the conditions when a wake-up IRQ is sent to the host.

This behavior is defined by bits i_tdi_en<2:0> and q_tdi_en<2:0> and the following three conditions can be used:

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- IRQ when the latest measurement is above the upper limit: i/q_adc > i/q_ref + i/q_diff
- IRQ when the latest measurement is in between the upper and lower limit: i/q_ref – i/q_diff ≤ i/q_adc ≤ i/q_ref + i/q_diff
- IRQ when the latest measurement is below the lower limit: i/q_adc < i/q_ref - i/q_diff

In case the bits i_tdi_en<2:0> = 0, the I channel is not used during WU, and the same applies for the Q channel when q_tdi_en<2:0> = 0.

5.11 Transparent mode

Standard or custom 13.56 MHz RFID reader protocols that are not supported by the ST25R100 framing system can be implemented using directly the AFE via the transparent mode, where the framing is implemented on the host side.

After sending the direct command transparent mode the external host directly controls the transmission modulator and gets the receiver output (control logic becomes “transparent”).

The transparent mode is entered on the rising edge of signal BSS after sending the command transparent mode.

Before executing the direct command transparent mode the transmitter and receiver must be turned on and the AFE configured properly.

While in transparent mode the AFE is controlled directly through the SPI interface:

Table 4. Signals in Transparent mode

Pin	Description
MOSI	Transmitter modulation - high is modulator on
SCLK	Enable reception (rx_on) - high enables reception chain and AGC
MISO	In case dis_corr=0, correlator data output (sum of I+Q) In case dis_corr=1, output of receiver I reception chain (digitized subcarrier signal)
IRQ	In case dis_corr=0, correlator start signal (subcarrier detected) In case dis_corr=1, output of receiver Q reception chain (digitized subcarrier signal)

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5.12 Registers

The 7-bit register addresses below are defined in hexadecimal notation. The possible addresses range from 00h to 3Fh.

There are two types of registers available in the ST25R100:

- Configuration registers
- Display registers

Configuration registers can be read and written (RW) through the SPI and hold the devices configuration.

Display registers are read only (R) and contain information about the device's internal state.

Additionally, registers are grouped in two different power domains:

- Power down (PD)
- Ready (RD)

When the device is not in ready mode, only register belonging to the PD domain can be accessed. In Ready mode all registers can be accessed.

Registers are set to their default state at power-up, reset and after execution of the direct command set default. The bits set as RFU must be kept at their default values unless otherwise specified.

Table 5. Registers overview

Type	Address(hex)	Register name	Power domain
Operation	0	Operation	PD
Configuration	1	General	PD
	2	Regulator	PD
	3	Driver	PD
	4	Tx mod 1	PD
	5	Tx mod 2	PD
	6	Rx path analog 1	PD
	7	Rx path analog 2	PD
	8	Rx path digital	RD
	9	Correlator 1	RD
	A	Correlator 2	RD
	B	Correlator 3	RD
	C	Correlator 4	RD
	D	Correlator 5	RD
	E	Correlator 6	RD
Display	F	Display 1	PD
	10	Display 2	RD
	11	Status	RD
Protocol	12	Protocol	RD
	13	Protocol Tx 1	RD
	14	Protocol Tx 2	RD
	15	Protocol Tx 3	RD
	16	Protocol Rx 1	RD
	17	Protocol Rx 2	RD
	18	Protocol Rx 3	RD
Reserved	19	Reserved	RD
	1A	Reserved	RD

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Type	Address(hex)	Register name	Power domain
Timers	1B	MRT SQT Config	RD
	1C	MRT	RD
	1D	SQT	RD
	1E	NRT GPT Config	RD
	1F	NRT1	RD
	20	NRT2	RD
	21	GPT1	RD
	22	GPT2	RD
Display	23	Display 3	PD
	24	Display 4	PD
Reserved	25	Reserved	RD
	26	Reserved	RD
	27	Reserved	RD
Wake-up	28	WU control	PD
	29	WU control 2	PD
	2A	I-Channel WU configuration	PD
	2B	I-channel WU difference	PD
	2C	I-channel WU display ADC part	PD
	2D	I-channel WU display auto average Ref.	PD
	2E	I-channel WU display calibration	PD
	2F	Q-Channel WU Config.	PD
	30	Q-channel WU difference	PD
	31	Q-channel WU display ADC part	PD
	32	Q-channel WU display auto average Ref.	PD
	33	Q-channel WU display calibration	PD
Tx/Rx Frame	34	Tx Frame 1	RD
	35	Tx Frame 2	RD
	36	FIFO status 1	RD
	37	FIFO status 2	RD
	38	Collision	RD
IRQ mask	39	IRQ mask 1	RD
	3A	IRQ mask 2	RD
	3B	IRQ mask 3	PD
IRQ status	3C	IRQ status 1	RD
	3D	IRQ status 2	RD
	3E	IRQ status 3	PD
Identity	3F	IC identity	PD

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5.12.1 Operation register

Address: 00h
Type: RW
Domain: PD

Table 6. Operation register

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	tx_en	0	1: Enables Tx operation	Enables field transmission
4	rx_en	0	1: Enables Rx operation	-
3	am_en	0	1: Enables AM regulator	-
2	RFU	0	-	-
1	en(1)	0	1: Enables ready mode (RD)	-
0	wu_en(1)	0	1: Enables wake-up mode (WU)	-

1. *The transition between modes follows the sequence described in Operating modes.*

5.12.2 General configuration register

Address: 01h
Type: RW
Domain: PD

Table 7. General configuration register

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	sink_mode	0	0: AM sink via main loop 1: AM sink via separate loop	-
5	single	0	0: Differential antenna driving 1: Single ended antenna driving	In the single ended, only one RFO driver is used.
4	rfo2	0	0: RFO1, RFI1 1: RFO2, RFI2	When singe=1, defines the RFO/RFI pair to use.
3	miso_pd2	0	1: Pull down on MISO, when BSS is low and MISO is not driven by the device	-
2	miso_pd1	0	1: Pull down on MISO when BSS is high	-
1	RFU	0	-	-
0	reg_s	0	0: RFU 1: Regulated voltages are defined by rege<4:0> bits	-

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5.12.3 Regulator configuration register

Address: 02h
Type: RW
Domain: PD

Table 8. Regulator configuration register

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	1		
5	RFU	0		
4	rege4	1	Regulator target voltage Used when manual voltage setting is used (reg_s=1)	External definition of regulated voltage in 80mV steps (see Table 9)
3	rege3	1		
2	rege2	1		
1	rege1	1		
0	rege0	1		

Table 9. Regulated voltages

rege<4:0>	rege4	rege3	rege2	rege1	rege0	VDD_A (V)	VDD_DR (V)
9	0	1	0	0	1	3.34	3.34
8	0	1	0	0	0	3.26	3.26
7	0	0	1	1	1	3.18	3.18
6	0	0	1	1	0	3.1	3.1
5	0	0	1	0	1	3.02	3.02
4	0	0	1	0	0	2.94	2.94
3	0	0	0	1	1	2.86	2.86
2	0	0	0	1	0	2.78	2.78
1	0	0	0	0	1	2.7	2.7
0	0	0	0	0	0	2.62	2.62
All other combinations						RFU	

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5.12.4 Tx driver register

Address: 03h
Type: RW
Domain: PD

Table 10. Tx driver register

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	d_res3	0	RFO driver resistance	-
2	d_res2	0		-
1	d_res1	0		-
0	d_res0	0		-

Table 11. RFO driver resistance

d_res3:0	d_res3	d_res2	d_res1	d_res0	Driver output resistance (normalized)(1)
0	0	0	0	0	1
1	0	0	0	1	1.19
2	0	0	1	0	1.4
3	0	0	1	1	1.61
4	0	1	0	0	1.79
5	0	1	0	1	2.02
6	0	1	1	0	2.49
7	0	1	1	1	2.94
8	1	0	0	0	3.41
9	1	0	0	1	4.06
10	1	0	1	0	5.95
11	1	0	1	1	8.26
12	1	1	0	0	17.1
13	1	1	0	1	36.6
14	1	1	1	0	51.2
15	1	1	1	1	High Z

1. *The value must be multiplied by the RFO resistance from Electrical characteristics to obtain the driver output resistance for the corresponding d_res setting.*

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5.12.5 Tx modulation register 1

Address: 04h
Type: RW
Domain: PD

Table 12. Tx modulation register 1

Bit	Name	Default	Function	Comment
7	am_mod3	0	AM modulation index (see Table 13)	-
6	am_mod2	1		-
5	am_mod1	1		-
4	am_mod0	1		-
3	mod_state	0	Modulation state	It enables to switch the modulation/unmodulated state manually
2	RFU	0	-	-
1	res_am	0	1: Resistive AM modulation enable	-
0	reg_am	0	1: Regulator AM enable	-

Table 13. AM modulation index

am_mod<3:0>	am_mod3	am_mod2	am_mod1	am_mod0	Modulation (%)
0	0	0	0	0	8
1	0	0	0	1	9
2	0	0	1	0	10
3	0	0	1	1	11
4	0	1	0	0	12
5	0	1	0	1	13
6	0	1	1	0	14
7	0	1	1	1	15
8	1	0	0	0	17
9	1	0	0	1	19
10	1	0	1	0	22
11	1	0	1	1	26
12	1	1	0	0	30
13	1	1	0	1	35
14	1	1	1	0	45
15	1	1	1	1	55

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5.12.6 Tx modulation register 2

Address: 05h
Type: RW
Domain: PD

Table 14. Tx modulation register 2

Bit	Name	Default	Function	Comment
7	am_ref_sel	0	0: AM reg. reference internally generated 1: AM reg. reference from VDD_DR	-
6	md_res6	0	Resistive modulation (see Table 15)	-
5	md_res5	0		
4	md_res4	0		
3	md_res3	0		
2	md_res2	0		
1	md_res1	0		
0	md_res0	0		

Table 15. Resistive AM modulated state driver output resistance

md_res<6:0>	md_res6	md_res5	md_res4	md_res3	md_res2	md_res1	md_res0	Driver output resistance RRFO (normalized)(1)
0	0	0	0	0	0	0	0	1.004
1	0	0	0	0	0	0	1	1.02
2	0	0	0	0	0	1	0	1.036
3	0	0	0	0	0	1	1	1.053
4	0	0	0	0	1	0	0	1.071
5	0	0	0	0	1	0	1	1.089
6	0	0	0	0	1	1	0	1.108
7	0	0	0	0	1	1	1	1.128
8	0	0	0	1	0	0	0	1.148
9	0	0	0	1	0	0	1	1.169
10	0	0	0	1	0	1	0	1.191
11	0	0	0	1	0	1	1	1.213
12	0	0	0	1	1	0	0	1.237
13	0	0	0	1	1	0	1	1.261
14	0	0	0	1	1	1	0	1.286
15	0	0	0	1	1	1	1	1.313
16	0	0	1	0	0	0	0	1.34
17	0	0	1	0	0	0	1	1.369
18	0	0	1	0	0	1	0	1.399
19	0	0	1	0	0	1	1	1.43
20	0	0	1	0	1	0	0	1.463
21	0	0	1	0	1	0	1	1.497
22	0	0	1	0	1	1	0	1.533

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md_res<6:0>	md_res6	md_res5	md_res4	md_res3	md_res2	md_res1	md_res0	Driver output resistance RRFO (normalized)(1)
23	0	0	1	0	1	1	1	1.571
24	0	0	1	1	0	0	0	1.61
25	0	0	1	1	0	0	1	1.652
26	0	0	1	1	0	1	0	1.695
27	0	0	1	1	0	1	1	1.741
28	0	0	1	1	1	0	0	1.79
29	0	0	1	1	1	0	1	1.842
30	0	0	1	1	1	1	0	1.896
31	0	0	1	1	1	1	1	1.954
32	0	1	0	0	0	0	0	2.016
33	0	1	0	0	0	0	1	2.081
34	0	1	0	0	0	1	0	2.151
35	0	1	0	0	0	1	1	2.226
36	0	1	0	0	1	0	0	2.306
37	0	1	0	0	1	0	1	2.349
38	0	1	0	0	1	1	0	2.393
39	0	1	0	0	1	1	1	2.438
40	0	1	0	1	0	0	0	2.485
41	0	1	0	1	0	0	1	2.535
42	0	1	0	1	0	1	0	2.586
43	0	1	0	1	0	1	1	2.639
44	0	1	0	1	1	0	0	2.695
45	0	1	0	1	1	0	1	2.753
46	0	1	0	1	1	1	0	2.813
47	0	1	0	1	1	1	1	2.876
48	0	1	1	0	0	0	0	2.943
49	0	1	1	0	0	0	1	3.012
50	0	1	1	0	0	1	0	3.084
51	0	1	1	0	0	1	1	3.16
52	0	1	1	0	1	0	0	3.241
53	0	1	1	0	1	0	1	3.325
54	0	1	1	0	1	1	0	3.413
55	0	1	1	0	1	1	1	3.507
56	0	1	1	1	0	0	0	3.606
57	0	1	1	1	0	0	1	3.657
58	0	1	1	1	0	1	0	3.71
59	0	1	1	1	0	1	1	3.765
60	0	1	1	1	1	0	0	3.821
61	0	1	1	1	1	0	1	3.879
62	0	1	1	1	1	1	0	3.938
63	0	1	1	1	1	1	1	4

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md_res<6:0>	md_res6	md_res5	md_res4	md_res3	md_res2	md_res1	md_res0	Driver output resistance RRFO (normalized)(1)
64	1	0	0	0	0	0	0	4.063
65	1	0	0	0	0	0	1	4.129
66	1	0	0	0	0	1	0	4.197
67	1	0	0	0	0	1	1	4.267
68	1	0	0	0	1	0	0	4.339
69	1	0	0	0	1	0	1	4.414
70	1	0	0	0	1	1	0	4.491
71	1	0	0	0	1	1	1	4.571
72	1	0	0	1	0	0	0	4.655
73	1	0	0	1	0	0	1	4.741
74	1	0	0	1	0	1	0	4.83
75	1	0	0	1	0	1	1	4.923
76	1	0	0	1	1	0	0	5.02
77	1	0	0	1	1	0	1	5.12
78	1	0	0	1	1	1	0	5.224
79	1	0	0	1	1	1	1	5.333
80	1	0	1	0	0	0	0	5.447
81	1	0	1	0	0	0	1	5.565
82	1	0	1	0	0	1	0	5.689
83	1	0	1	0	0	1	1	5.818
84	1	0	1	0	1	0	0	5.953
85	1	0	1	0	1	0	1	6.095
86	1	0	1	0	1	1	0	6.244
87	1	0	1	0	1	1	1	6.4
88	1	0	1	1	0	0	0	6.564
89	1	0	1	1	0	0	1	6.737
90	1	0	1	1	0	1	0	6.919
91	1	0	1	1	0	1	1	7.111
92	1	0	1	1	1	0	0	7.314
93	1	0	1	1	1	0	1	7.529
94	1	0	1	1	1	1	0	7.758
95	1	0	1	1	1	1	1	8
96	1	1	0	0	0	0	0	8.258
97	1	1	0	0	0	0	1	8.533
98	1	1	0	0	0	1	0	8.828
99	1	1	0	0	0	1	1	9.143
100	1	1	0	0	1	0	0	9.481
101	1	1	0	0	1	0	1	9.846
102	1	1	0	0	1	1	0	10.24
103	1	1	0	0	1	1	1	10.667
104	1	1	0	1	0	0	0	11.13

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md_res<6:0>	md_res6	md_res5	md_res4	md_res3	md_res2	md_res1	md_res0	Driver output resistance RRFO (normalized)(1)
105	1	1	0	1	0	0	1	11.636
106	1	1	0	1	0	1	0	12.19
107	1	1	0	1	0	1	1	12.8
108	1	1	0	1	1	0	0	13.474
109	1	1	0	1	1	0	1	14.222
110	1	1	0	1	1	1	0	15.059
111	1	1	0	1	1	1	1	16
112	1	1	1	0	0	0	0	17.067
113	1	1	1	0	0	0	1	18.286
114	1	1	1	0	0	1	0	19.692
115	1	1	1	0	0	1	1	21.333
116	1	1	1	0	1	0	0	23.273
117	1	1	1	0	1	0	1	25.6
118	1	1	1	0	1	1	0	28.444
119	1	1	1	0	1	1	1	32
120	1	1	1	1	0	0	0	36.571
121	1	1	1	1	0	0	1	42.667
122	1	1	1	1	0	1	0	51.2
123	1	1	1	1	0	1	1	64
124	1	1	1	1	1	0	0	85.333
125	1	1	1	1	1	0	1	128
126	1	1	1	1	1	1	0	256
127	1	1	1	1	1	1	1	High Z

1. *The value must be multiplied by the RFO resistance from Electrical characteristics to obtain the driver output resistance for the corresponding md_res setting.*

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5.12.7 Rx analog register 1

Address: 06h
Type: RW
Domain: PD

Table 16. Rx analog register 1

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	1		-
5	RFU	0		-
4	RFU	1		-
3	RFU	0	-	-
2	RFU	0	-	-
1	hpf_ctrl1	1	00: 80 kHz 01: 160 kHz 10: 240 kHz 11: 380 kHz	Analogue 1st and 3rd stage HPF setting (2nd stage: LPF, 2nd order, 2 MHz)
0	hpf_ctrl0	1		

5.12.8 Rx analog register 2

Address: 07h
Type: RW
Domain: PD

Table 17. Rx analog register 2

Bit	Name	Default	Function	Comment
7	afe_gain_rw3	0	Start gain in RW mode	-
6	afe_gain_rw2	0		
5	afe_gain_rw1	0		
4	afe_gain_rw0	0		
3	afe_gain_td3	1	Gain in WU mode/measurements	-
2	afe_gain_td2	0		
1	afe_gain_td1	0		
0	afe_gain_td0	0		

Table 18. Gain in RW mode

afe_gain_rw<3:0>	afe_gain_rw3	afe_gain_rw2	afe_gain_rw1	afe_gain_rw0	Total gain (dB)
0	0	0	0	0	46
1	0	0	0	1	43
2	0	0	1	0	40
3	0	0	1	1	37
4	0	1	0	0	34
5	0	1	0	1	31
6	0	1	1	0	28

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afe_gain_rw<3:0>	afe_gain_rw3	afe_gain_rw2	afe_gain_rw1	afe_gain_rw0	Total gain (dB)
7	0	1	1	1	25
8	1	0	0	0	22
9	1	0	0	1	19
10	1	0	1	0	16
11	1	0	1	1	13
12	1	1	0	0	10
13	1	1	0	1	7
14	1	1	1	0	4
15	1	1	1	1	1

Table 19. Gain in WU mode

afe_gain_td<3:0>	afe_gain_td3	afe_gain_td2	afe_gain_td1	afe_gain_td0	Total gain (dB)
0	0	0	0	0	26
1	0	0	0	1	23
2	0	0	1	0	20
3	0	0	1	1	17
4	0	1	0	0	14
5	0	1	0	1	11
6	0	1	1	0	8
7	0	1	1	1	5
8	1	0	0	0	2
9	1	0	0	1	-1
10	1	0	1	0	-4
11	1	0	1	1	-
12	1	1	0	0	-
13	1	1	0	1	-
14	1	1	1	0	-
15	1	1	1	1	-

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5.12.9 Rx digital register

Address: 08h
Type: RW
Domain: RD

Table 20. Rx digital register

Bit	Name	Default	Function	Comment
7	agc_en	1	0: AGC disabled 1: AGC enabled	-
6	lpf_coef2	1	Digital IIR high pass filter 4th stage	-
5	lpf_coef1	0		
4	lpf_coef0	0		
3	hpf_coef1	1	Digital IIR high pass filter 5th stage	-
2	hpf_coef0	1		
1	RFU	0	-	-
0	dis_corr	0	1: Disable correlator	-

5.12.10 Correlator register 1

Address: 09h
Type: RW
Domain: RD

Table 21. Correlator register 1

Bit	Name	Default	Function	Comment
7	iir_coef2_3	1	1st order IIR coefficient	Filter after decimation
6	iir_coef2_2	0		
5	iir_coef2_1	0		
4	iir_coef2_0	1		
3	iir_coef1_3	0	1st order IIR coefficient	Filter after down conversion
2	iir_coef1_2	0		
1	iir_coef1_1	0		
0	iir_coef1_0	1		

5.12.11 Correlator register 2

Address: 0Ah
Type: RW
Domain: RD

Table 22. Correlator register 2

Bit	Name	Default	Function	Comment
7	agc_thr_squelch3	0	Squelch threshold	-
6	agc_thr_squelch2	1		
5	agc_thr_squelch1	0		
4	agc_thr_squelch0	0		

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Bit	Name	Default	Function	Comment
3	agc_thr3	1	AGC threshold	-
2	agc_thr2	0		
1	agc_thr1	1		
0	agc_thr0	0		

5.12.12 Correlator register 3

Address: 0Bh
Type: RW
Domain: RD

Table 23. Correlator register 3

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	start_wait5	0	Wait time for subcarrier detection	-
4	start_wait4	0		
3	start_wait3	0		
2	start_wait2	1		
1	start_wait1	1		
0	start_wait0	1		

5.12.13 Correlator register 4

Address: 0Ch
Type: RW
Domain: RD

Table 24. Correlator register 4

Bit	Name	Default	Function	Comment
7	coll_lvl3	1	Manchester: collision level ratio	-
6	coll_lvl2	0		
5	coll_lvl1	1		
4	coll_lvl0	0		
3	data_lvl3	1	Manchester: data level ratio BPSK: Subcarrier end detection level	-
2	data_lvl2	0		
1	data_lvl1	1		
0	data_lvl0	0		

5.12.14 Correlator register 5

Address: 0Dh
Type: RW
Domain: RD

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Table 25. **Correlator register 5**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	dis_soft_sq	0	0: Enables soft squelch with noise measurement when the receiver is enabled 1: Disables soft squelch	-
4	en_subc_end	0	BPSK only 0: No subcarrier end detection (reception stops with valid EoF or timeout) 1: Fast subcarrier end detection	-
3	no_phase	0	BPSK only 0: Enables phase correction after signal start detection 1: Disables phase correction after signal start detection	-
2	dec_f2	0	Decimation factor for IIR filters	-
1	dec_f1	1		
0	dec_f0	1		

5.12.15 Correlator register 6

Address: 0Eh
Type: RW
Domain: RD

Table 26. **Correlator register 6**

Bit	Name	Default	Function	Comment
7	init_noise_lvl3	0	Correlator initial noise level	Higher levels increase robustness to noise, where lower levels lead to higher sensitivity
6	init_noise_lvl2	0		
5	init_noise_lvl1	1		
4	init_noise_lvl0	1		
3	RFU	0	-	-
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

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5.12.16 Display register 1

Address: 0Fh
Type: RO
Domain: PD

Table 27. **Display register 1**

Bit	Name	Default	Function	Comment
7	i_lim	0	1: VDD_DR regulator in current limit mode	-
6	agd_ok	0	1: AGD stable	-
5	osc_ok	0	1: Oscillator stable	-
4	RFU	1	-	-
3	RFU	1		
2	RFU	1		
1	RFU	1		
0	RFU	1		

5.12.17 Display register 2

Address: 10h
Type: RO
Domain: RD

Table 28. **Display register 2**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	afe_gain3	0	Actual gain used during reception (after Squelch and AGC operation)	Valid until a following reception is started (rx_on)
2	afe_gain2	0		
1	afe_gain1	0		
0	afe_gain0	0		

5.12.18 Status register 2

Address: 11h
Type: RO
Domain: RD

Table 29. **Status register 2**

Bit	Name	Default	Function	Comment
7	subc_on	0	1: Subcarrier detected	-
6	gpt_on	0	1: General Purpose timer is running	-
5	nrt_on	0	1: No-response timer is running	-
4	mrt_on	0	1: Mask Receive timer is running	-
3	rx_act	0	1: Receive decoder is receiving a message	-

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Bit	Name	Default	Function	Comment
2	rx_on	0	1: Receive decoder is enabled	-
1	tx_on	0	1: Transmission is active	-
0	RFU	0	-	-

5.12.19 Protocol register

Address: 12h
Type: RW
Domain: RD

Table 30. Protocol register

Bit	Name	Default	Function	Comment
7	rx_rate1	0	00: 106 kbit/s ISO14443A/B 26 kbit/s ISO15693 01: - 10: 53 kbit/s ISO15693 11: -	Receiver bit rate definition
6	rx_rate0	0		
5	tx_rate1	0	00: 106 kbit/s ISO14443A/B 26 kbit/s 1 of 4 ISO15693 01: - 10: - 11: -	Transmitter bit rate definition
4	tx_rate0	0		
3	om3	0	Operation mode/protocol (see Table 31)	-
2	om2	0		-
1	om1	0		-
0	om0	1		-

Table 31. Operating modes

om<3:0>	om3	om2	om1	om0	Mode
1	0	0	0	1	ISO14443A/NFC-A
2	0	0	1	0	ISO14443B/NFC-B
4	0	1	0	0	Topaz/T1T
5	0	1	0	1	ISO15693/NFC-V
Other combinations					RFU

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5.12.20 Protocol transmission register 1

Address: 13h
Type: RW
Domain: RD

Table 32. Protocol transmission register 1

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	a_tx_par	1	0: Parity is not transmitted during transmission 1: Parity is generated and transmitted during transmission	-
5	tx_crc	1	0: CRC is not transmitted during transmission 1: CRC is generated and transmitted during transmission	-
4	tr_am	0	0: OOK 1: AM	Transmitter modulation type
3	p_len3	0	ISO14443A/ISO15693 modulation pulse width defined in 13.56 MHz clock periods (see Table 33 and Table 34)	-
2	p_len2	0		
1	p_len1	0		
0	p_len0	0		

Table 33. ISO14443A modulation pulse width

p_len<3:0>	p_len3	p_len2	p_len1	p_len0	Pulse width in number of 1/fc
7	0	1	1	1	42
6	0	1	1	0	41
5	0	1	0	1	40
4	0	1	0	0	39
3	0	0	1	1	38
2	0	0	1	0	37
1	0	0	0	1	36
0	0	0	0	0	35
15	1	1	1	1	34
14	1	1	1	0	33
13	1	1	0	1	32
12	1	1	0	0	31
11	1	0	1	1	30
10	1	0	1	0	29
9	1	0	0	1	28
8	1	0	0	0	27

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Table 34. **ISO15693 modulation pulse width**

p_len<3:0>	p_len3	p_len2	p_len1	p_len0	Pulse width in number of 1/fc
7	0	1	1	1	128
6	0	1	1	0	124
5	0	1	0	1	120
4	0	1	0	0	116
3	0	0	1	1	112
2	0	0	1	0	108
1	0	0	0	1	104
0	0	0	0	0	100
15	1	1	1	1	96
14	1	1	1	0	92
13	1	1	0	1	88
12	1	1	0	0	84
11	1	0	1	1	80
10	1	0	1	0	76
9	1	0	0	1	72
8	1	0	0	0	68

5.12.21 Protocol transmission register 2

Address: 14h
Type: RW
Domain: RD

Table 35. **Protocol transmission register 2**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	b_tx_sof_0	0	0: 10 etu 1: 11 etu	SOF, number of etu with logic 0
2	b_tx_sof_1	0	0: 2 etu 1: 3 etu	SOF, number of etu with logic 1
1	b_tx_eof	0	0: 10 etu 1: 11 etu	EOF, number of etu with logic 0
0	b_tx_half	0	1: SOF 10.5, 2.5, EOF: 10.5	Sets SOF and EOF settings in middle of specification

5.12.22 Protocol transmission register 3

Address: 15h
Type: RW
Domain: RD

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Table 36. **Protocol transmission register 3**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	RFU	0	-	-
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

5.12.23 Protocol reception register 1

Address: 16h
Type: RW
Domain: RD

Table 37. **Protocol reception register 1**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	b_rx_sof	1	1: SOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3 Support of B' (no SOF)
4	b_rx_eof	1	1: EOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3
3	a_rx_par	1	1: Receive with parity check	-
2	rx_crc	1	1: Receive with CRC check	-
1	rx_nbtx	0	0: Received bits are positioned normally 1: Received bits are positioned according to nbtx<2:0> setting (ISO14443A)	nbtx<2:0> bits define the position of the first bit in the first byte in consecutive reception
0	antcl	0	1: ISO14443A/ISO15693 bit oriented anticollision frame	Shall be set to 1 when ISO14443A/ISO15693 bit-oriented anticollision frame is expected. When enabled: coll_lvl is used to detect colliding bits the first parity bit is ignored in case the split happens within the byte

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5.12.24 Protocol reception register 2

Address: 17h
Type: RW
Domain: RD

Table 38. Protocol reception register 2

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	tr1_min_len6	0	-	-
5	tr1_min_len5	1	Minimum remaining TR1 length defined in subcarrier periods (0-127)	If TR1 is shorter than the minimum, a soft framing error is reported. start_wait<5:0> needs to be taken into account.
4	tr1_min_len4	1		
3	tr1_min_len3	1		
2	tr1_min_len2	0		
1	tr1_min_len1	1		
0	tr1_min_len0	0		

5.12.25 Protocol reception register 3

Address: 18h
Type: RW
Domain: RD

Table 39. Protocol reception register 3

Bit	Name	Default	Function	Comment
7	tr1_max_len7	1	Maximum remaining TR1 length defined in subcarrier periods (0-255)	If TR1 is longer than the maximum, a soft framing error is reported. start_wait<5:0> needs to be taken into account.
6	tr1_max_len6	1		
5	tr1_max_len5	0		
4	tr1_max_len4	0		
3	tr1_max_len3	0		
2	tr1_max_len2	0		
1	tr1_max_len1	0		
0	tr1_max_len0	0		

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5.12.26 Reserved

Address: 19h
Type: RW
Domain: RD

Table 40. **Reserved**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	1		
5	RFU	0		
4	RFU	0		
3	RFU	1	-	-
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

5.12.27 Reserved

Address: 1Ah
Type: RW
Domain: RD

Table 41. **Reserved**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	RFU	0	-	-
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

5.12.28 MRT SQT configuration register

Address: 1Bh
Type: RW
Domain: RD

Table 42. **MRT SQT configuration register**

Bit	Name	Default	Function	Comment
7	sq_del1	0	00: 18.88 µs 01: 37.76 µs 10: 75.52 µs 11: 151.04 µs	Defines the delay, in 18.88µs steps, of the squelch enable, with respect to end of transmission
6	sq_del0	0		
5	mrt_step1	1	00: 16/fc (1.18 µs)	Selects the mask-receive timer step

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Bit	Name	Default	Function	Comment
4	mrt_step0	0	01: 32/fc (2.36 µs) 10: 64/fc (4.72 µs) 11: 512/fc (37.8 µs)	Selects the mask-receive timer step
3	RFU	0	-	-
2	RFU	0	-	-
1	RFU	0	-	-
0	sq_en	1	1: Automatic squelch activation after end of transmission	Activated 18.88 µs after end of transmission, terminated with mask receive timer expiration

5.12.29 Mask receive timer register

Address: 1Ch
Type: RW
Domain: RD

Table 43. Mask receive timer register

Bit	Name	Default	Function	Comment
7	mrt7	0	mrt_step = 00: • Step: 16 / fc (1.18 µs) • Range: 16 / fc (~1.18 µs) to 4080 / fc (~300.1 µs) mrt_step = 01: • Step: 32 / fc (2.36 µs) • Range: 32 / fc (~2.36 µs) to 8260 / fc (~601.77 ms) mrt_step = 10: • Step: 64 / fc (4.72 µs) • Range: 256 / fc (~4.72 µs) to 16320 / fc (~1.2 ms) mrt_step = 11: • Step: 512 / fc (37.78 µs) • Range: 512 / fc (37.78 µs) to 130560 / fc (9.62 ms)	Defines time after end of transmission during which receiver output is masked (ignored).
6	mrt6	0		
5	mrt5	0		
4	mrt4	0		
3	mrt3	1		
2	mrt2	0		
1	mrt1	1		
0	mrt0	1		

5.12.30 Squelch timer register

Address: 1Dh
Type: RW
Domain: RD

Table 44. Squelch timer register

Bit	Name	Default	Function	Comment
7	sqt7	0	Steps defined by MRT configuration mrt_step<1:0>	Squelch is enabled 18.88µs -151µs after the end of transmission, as defined in sq_del<1:0>. Squelch is enabled until the time defined on sqt<7:0>. In case sqt < sq_del, there is no squelch period (and Gain reduction from previous reception are used as starting point for AGC). In case sqt > mrt, Squelch is enabled until the MRT expires.
6	sqt6	0		
5	sqt5	0		
4	sqt4	0		
3	sqt3	1		
2	sqt2	0		
1	sqt1	1		
0	sqt0	1		

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5.12.31 NRT GPT configuration register

Address: 1Eh
Type: RW
Domain: RD

Table 45. NRT GPT configuration register

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	gptc2	0	Defines the GPT trigger source (see Table 46)	-
5	gptc1	0		
4	gptc0	0		
3	RFU	0	-	-
2	RFU	0	-	-
1	nrt_emd	0	0: Normal mode of NRT 1: EMD mode of NRT	When enabled, NRT produces an IRQ when it expires independent of the reception.
0	nrt_step	0	0: 64/fc (4.72 µs) 1: 4096/fc (~302 µs)	-

Table 46. GPT trigger sources

gptc<2:0>	gptc2	gptc1	gptc0	Trigger source
0	0	0	0	No trigger source
1	0	0	1	Starts at the end of reception (RXE)
2	0	1	0	Starts at start of reception (RXS)
3	0	1	1	Starts at end of transmission (TXE)
Other combinations				RFU

Note: The GPT timer can always be started manually by execution of the direct command start GPT.

5.12.32 No-response timer register 1

Address: 1Fh
Type: RW
Domain: RD

Table 47. No-response timer register 1

Bit	Name	Default	Function	Comment
7	nrt15	0	No-response timer definition MSB nrt_step = 0: • Step: 64 / fc (4.72 µs) • Range: 64 / fc (~4.72 µs) to 16320 / fc (~309.3 ms) nrt_step = 1: • Step: 4096 / fc (302 µs) • Range: 4096 / fc (~302 µs) to 268431360 / fc (~19.8 s)	Defines the timeout after the end of transmission until when the reception may start. In case this timeout expires without detecting a response, a I_nre IRQ is produced. When nrt_emd=1 the IRQ is produced regardless of the reception. In case nrt<15:0>=0 the NRT is not started.
6	nrt14	0		
5	nrt13	0		
4	nrt12	0		
3	nrt11	0		
2	nrt10	0		
1	nrt9	0		
0	nrt8	0		

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5.12.33 No-response timer register 2

Address: 20h
Type: RW
Domain: RD

Table 48. **No-response timer register 2**

Bit	Name	Default	Function	Comment
7	nrt7	0	No-response timer definition LSB	-
6	nrt6	0		
5	nrt5	0		
4	nrt4	0		
3	nrt3	0		
2	nrt2	0		
1	nrt1	0		
0	nrt0	0		

5.12.34 General purpose timer register 1

Address: 21h
Type: RW
Domain: RD

Table 49. **General purpose timer register 1**

Bit	Name	Default	Function	Comment
7	gpt15	0	General Purpose Timer definition MSB • Step: 8/fc steps (~590 ns) • Range: 8 / fc (~590 ns) to 524280 / fc (~38.7 ms)	-
6	gpt14	0		
5	grt13	0		
4	gpt12	0		
3	gpt11	0		
2	gpt10	0		
1	gpt9	0		
0	gpt8	0		

5.12.35 General purpose timer register 2

Address: 22h
Type: RW
Domain: RD

Table 50. **General purpose timer register 2**

Bit	Name	Default	Function	Comment
7	gpt7	0	General purpose timer definition LSB	-
6	gpt6	0		
5	gpt5	0		
4	gpt4	0		
3	gpt3	0		

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Bit	Name	Default	Function	Comment
2	gpt2	0	General purpose timer definition LSB	-
1	gpt1	0		
0	gpt0	0		

5.12.36 Display register 3

Address: 23h
Type: RO
Domain: PD

Table 51. Display register 3

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	rf_ind6	0	Result of the sense RF measurement command	-
5	rf_ind5	0		
4	rf_ind4	0		
3	rf_ind3	0		
2	rf_ind2	0		
1	rf_ind1	0		
0	rf_ind0	0		

5.12.37 Display register 4

Address: 24h
Type: RO
Domain: PD

Table 52. Display register 4

Bit	Name	Default	Function	Comment
7	RFU	1	-	-
6	q_tdi2	0	1: q_adc >> q_ref + q_diff	Above upper threshold
5	q_tdi1	0	1: q_ref - q_diff ≤ q_adc ≤ q_ref + q_diff	Between lower and upper threshold
4	q_tdi0	0	1: q_adc < q_ref - q_diff	Below lower threshold
3	RFU	0	-	-
2	i_tdi2	0	1: i_adc > i_ref + i_diff	Above upper threshold
1	i_tdi1	0	1: i_ref - i_diff ≤ i_adc ≤ i_ref + i_diff	Between lower and upper threshold
0	i_tdi0	0	1: i_adc < i_ref - i_diff	Below lower threshold

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5.12.38 Reserved

Address: 25h
Type: RW
Domain: RD

Table 53. **Reserved**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	RFU	0	-	-
2	RFU	0		
1	RFU	0	-	-
0	RFU	0		

5.12.39 Reserved

Address: 26h
Type: RW
Domain: RD

Table 54. **Reserved**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	RFU	0	-	-
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

5.12.40 Reserved

Address: 27h
Type: RW
Domain: RD

Table 55. **Reserved**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	RFU	0	-	-

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Bit	Name	Default	Function	Comment
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

5.12.41 Wake-up configuration register 1

Address: 28h
Type: RW
Domain: PD

Table 56. Wake-up configuration register 1

Bit	Name	Default	Function	Comment
7	wut3	0	Wake-up timer period/timeout value (See Table 57)	-
6	wut2	0		
5	wut1	0		
4	wut0	0		
3	wuti	0	1: I_wut IRQ at every WU timeout	-
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

Table 57. Typical wake-up period/time

wut<3:0>	wut3	wut2	wut1	wut0	Timeout (ms)(1)
0	0	0	0	0	9.7
1	0	0	0	1	13.3
2	0	0	1	0	19.3
3	0	0	1	1	26.6
4	0	1	0	0	38.7
5	0	1	0	1	53.2
6	0	1	1	0	77.3
7	0	1	1	1	106.3
8	1	0	0	0	154.7
9	1	0	0	1	212.7
10	1	0	1	0	309.3
11	1	0	1	1	425.3
12	1	1	0	0	618.6
13	1	1	0	1	850.6
14	1	1	1	0	1237.3
15	1	1	1	1	1701.2

1. *RC oscillator nominal values, PVT variation up to ±30%.*

5.12.42 Wake-up configuration register 2

Address: 29h

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Domain: PD

Table 58. Wake-up configuration register 2

Bit	Name	Default	Function	Comment
7	skip_recal	0	1: Disable automatic recalibration	-
6	skip_cal	0	1: Disable automatic calibration at start	-
5	skip_twcal	0	1: Disable calibration deferment at start	-
4	skip_twref	0	1: Disable reference deferment at start	-
3	iq_aaref	0	1: Enable Auto Average reference for both I and Q channel 0: Manually defined reference for both I and Q channel	When iq_aaref = 1 the reference is automatically obtained and registers 0x2D and 0x32 are read-only.
2	td_mf	0	Wake-up Measurement pulse length (see Table 59)	-
1	td_mt1	0		
0	td_mt0	0		

Table 59. Measurement pulse length

td_mf	td_mt1	td_mt0	Measurement pulse (µs)
0	0	0	26.0
0	0	1	29.5
0	1	0	34.2
0	1	1	43.7
1	0	0	10.6
1	0	1	14.2
1	1	0	18.9
1	1	1	28.3

5.12.43 I-Channel WU configuration register

Address: 2Ah
Type: RW
Domain: PD

Table 60. I-Channel WU configuration register

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	i_iirqm	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Includes/excludes the measurement that causes IRQ when auto-averaging is enabled
5	i_aaw1	0	00: 4 01: 8 10: 16 11: 32	Defines the weight of last measurement result for auto-averaging
4	i_aaw0	0		
3	RFU	0	-	-
2	i_tdi_en2	0	1: IRQ if i_adc > i_ref + i_diff	i_tdi_en<2:0> = 0 Wake-up I-channel disabled
1	i_tdi_en1	0	1: IRQ if i_ref - i_diff ≤ i_adc ≤ i_ref + i_diff	

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Bit	Name	Default	Function	Comment
0	i_tdi_en0	0	1: IRQ if i_adc < i_ref - i_diff	i_tdi_en<2:0> = 0 Wake-up I-channel disabled

5.12.44 I-Channel WU difference register

Address: 2Bh
Type: RW
Domain: PD

Table 61. I-Channel WU difference register

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	i_diff5	0	Defines the difference/delta from the reference that triggers an IRQ (unsigned) Range: 0 to 63	-
4	i_diff4	0		
3	i_diff3	0		
2	i_diff2	0		
1	i_diff1	0		
0	i_diff0	0		

5.12.45 I-Channel WU display ADC register

Address: 2Ch
Type: RO
Domain: PD

Table 62. I-Channel WU display ADC register

Bit	Name	Default	Function	Comment
7	i_adc7	0	8bit signed ADC part Range: -128 to 127	-
6	i_adc6	0		
5	i_adc5	0		
4	i_adc4	0		
3	i_adc3	0		
2	i_adc2	0		
1	i_adc1	0		
0	i_adc0	0		

5.12.46 I-Channel WU reference register

Address: 2Dh
Type: RO
Domain: PD

Table 63. I-Channel WU reference register

Bit	Name	Default	Function	Comment
7	i_ref7	0	8-bit signed reference Range: -128 to 127	If iq_aaref = 1 the reference is automatically calculated, and this register is RO. When iq_aaref = 0 the reference shall be set manually, and this register becomes RW
6	i_ref6	0		

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Bit	Name	Default	Function	Comment
5	i_ref5	0	8-bit signed reference Range: -128 to 127	If iq_aaref = 1 the reference is automatically calculated, and this register is RO. When iq_aaref = 0 the reference shall be set manually, and this register becomes RW
4	i_ref4	0		
3	i_ref3	0		
2	i_ref2	0		
1	i_ref1	0		
0	i_ref0	0		

5.12.47 I-Channel WU display calibration register

Address: 2Eh
Type: RO
Domain: PD

Table 64. I-Channel WU display calibration register

Bit	Name	Default	Function	Comment
7	i_cal7	1	8-bit unsigned calibration result	-
6	i_cal6	0		
5	i_cal5	0		
4	i_cal4	0		
3	i_cal3	0		
2	i_cal2	0		
1	i_cal1	0		
0	i_cal0	0		

5.12.48 Q-Channel WU configuration register

Address: 2Fh
Type: RW
Domain: PD

Table 65. Q-Channel WU configuration register

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	q_iirqm	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Includes/excludes the measurement that causes IRQ when auto-averaging is enabled
5	q_aaw1	0	00: 4 01: 8 10: 16 11: 32	Defines the weight of last measurement result for auto-averaging
4	q_aaw0	0		
3	RFU	0	-	-
2	q_tdi_en2	0	1: IRQ if q_adc > q_ref + q_diff	q_tdi_en<2:0> = 0 Wake-up Q-channel disabled
1	q_tdi_en1	0	1: IRQ if q_ref - q_diff ≤ q_adc ≤ q_ref + q_diff	
0	q_tdi_en0	0	1: IRQ if q_adc < q_ref - i_diff	

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5.12.49 Q-Channel WU difference register

Address: 30h
Type: RW
Domain: PD

Table 66. Channel WU difference register

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	q_diff5	0	Defines the difference/delta from the reference that triggers an IRQ (unsigned) Range: 0 to 63	-
4	q_diff4	0		
3	q_diff3	0		
2	q_diff2	0		
1	q_diff1	0		
0	q_diff0	0		

5.12.50 Q-Channel WU display ADC register

Address: 31h
Type: RO
Domain: PD

Table 67. Q-Channel WU display ADC register

Bit	Name	Default	Function	Comment
7	q_adc7	0	8-bit signed ADC part Range: -128 to 127	-
6	q_adc6	0		
5	q_adc5	0		
4	q_adc4	0		
3	q_adc3	0		
2	q_adc2	0		
1	q_adc1	0		
0	q_adc0	0		

5.12.51 Q-Channel WU reference register

Address: 32h
Type: RO
Domain: PD

Table 68. Q-Channel WU reference register

Bit	Name	Default	Function	Comment
7	q_ref7	0	8-bit signed reference Range: -128 to 127	If iq_aaref = 1 the reference is automatically calculated, and this register is RO. When iq_aaref = 0 the reference shall be set manually, and this register becomes RW
6	q_ref6	0		
5	q_ref5	0		
4	q_ref4	0		
3	q_ref3	0		

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Bit	Name	Default	Function	Comment
2	q_ref2	0	8-bit signed reference Range: -128 to 127	If iq_aaref = 1 the reference is automatically calculated, and this register is RO. When iq_aaref = 0 the reference shall be set manually, and this register becomes RW
1	q_ref1	0		
0	q_ref0	0		

5.12.52 Q-Channel WU display calibration register

Address: 33h
Type: RO
Domain: PD

Table 69. Q-Channel WU display calibration register

Bit	Name	Default	Function	Comment
7	q_cal7	1	8-bit unsigned calibration result	-
6	q_cal6	0		
5	q_cal5	0		
4	q_cal4	0		
3	q_cal3	0		
2	q_cal2	0		
1	q_cal1	0		
0	q_cal0	0		

5.12.53 TX frame register 1

Address: 34h
Type: RW
Domain: RD

Table 70. TX frame register 1

Bit	Name	Default	Function	Comment
7	ntx12	0	Number of full bytes to be transmitted (msb)	-
6	ntx11	0		
5	ntx10	0		
4	ntx9	0		
3	ntx8	0		
2	ntx7	0		
1	ntx6	0		
0	ntx5	0		

5.12.54 Tx frame register 2

Address: 35h
Type: RW
Domain: RD

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Table 71. **Tx frame register 2**

Bit	Name	Default	Function	Comment
7	ntx4	0	Number of full bytes to be transmitted (lsb)	-
6	ntx3	0		
5	ntx2	0		
4	ntx1	0		
3	ntx0	0		
2	nbtx2	0	Number of bits to transmit after the last full byte. nbtx<2:0>=0 only full bytes to be transmitted.	Bit transmission starts from LSB. Applicable for ISO14443A: • bit oriented anticollision frame in case the last byte is a split byte • Tx is done without parity bit generation
1	nbtx1	0		
0	nbtx0	0		

5.12.55 FIFO status register 1

Address: 36h
Type: RO
Domain: RD

Table 72. **FIFO status register 1**

Bit	Name	Default	Function	Comment
7	fifo_b7	0	Number of bytes in the FIFO (LSB)	fifo_b<8:0> valid range is from 0 to 256
6	fifo_b6	0		
5	fifo_b5	0		
4	fifo_b4	0		
3	fifo_b3	0		
2	fifo_b2	0		
1	fifo_b1	0		
0	fifo_b0	0		

5.12.56 FIFO status register 2

Address: 37h
Type: RO
Domain: RD

Table 73. **FIFO status register 2**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	fifo_b8	0	Number of bytes in the FIFO (msb)	-
5	fifo_unf	0	FIFO underflow	-
4	fifo_ovr	0	FIFO overflow	-
3	fifo_lb2	0	Number of bits in the last FIFO byte if it was not complete	The received bits are stored in the LSB part of the last byte in the FIFO. In case of I_hfe, fifo_lb<2:0> shall be disregarded.
2	fifo_lb1	0		
1	fifo_lb0	0		
0	np_lb	0	Parity bit is missing in last byte	Set if the last byte was complete with 8 data bits and only the parity bit is missing.

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Bit	Name	Default	Function	Comment
				In case of I_hfe, np_lb bit shall be disregarded.

5.12.57 Collision display register

Address: 38h
Type: RO
Domain: RD

Table 74. **Collision display register**

Bit	Name	Default	Function	Comment
7	c_byte3	0	Number of full bytes before the bit collision was detected	Covers ISO14443A anticollision command. If collision (or framing error interpreted as collision) happens in a longer frame, these are not set. In the case of I_hfe, c_byte<3:0> and c_bit<2:0> shall be disregarded.
6	c_byte2	0		
5	c_byte1	0		
4	c_byte0	0		
3	c_bit2	0	Number of bits before the collision in the byte where the collision was detected	
2	c_bit1	0		
1	c_bit0	0		
0	c_pb	0	Collision in parity bit	This error is reported if the first detected collision is in a parity bit. In the case of I_hfe, c_pb bit shall be disregarded.

5.12.58 IRQ mask register 1

Address: 39h
Type: RW
Domain: RD

Table 75. **IRQ mask register 1**

Bit	Name	Default	Function	Comment
7	M_subc_start	1	Mask IRQ due to subcarrier start	-
6	M_col	0	Mask IRQ due to bit collision	-
5	M_wl	0	Mask IRQ due FIFO water level	-
4	M_rx_rest	0	Mask IRQ due to automatic reception restart	-
3	M_rxe	0	Mask IRQ due to end of reception	-
2	M_rxs	0	Mask IRQ due to start of reception	-
1	M_txe	0	Mask IRQ due to end of transmission	-
0	RFU	0	-	-

5.12.59 IRQ mask register 2

Address: 3Ah
Type: RW
Domain: RD

Table 76. **IRQ mask register 2**

Bit	Name	Default	Function	Comment
7	M_gpe	0	Mask IRQ due to general purpose timer expire	-

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Bit	Name	Default	Function	Comment
6	M_nre	0	Mask IRQ due to No-response timer expire	-
5	RFU	0	-	-
4	RFU	0	-	-
3	M_crc	0	Mask IRQ due to CRC error	-
2	M_par	0	Mask IRQ due to parity error	-
1	M_hfe	0	Mask IRQ due to hard framing error	-
0	M_sfe	0	Mask IRQ due to soft framing error	-

5.12.60 IRQ mask register 3

Address: 3Bh
Type: RW
Domain: PD

Table 77. **IRQ mask register 3**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	M_dct	0	Mask IRQ due to termination of direct command	-
3	M_wuq	0	Mask IRQ due to wake-up Q-channel measurement	-
2	M_wui	0	Mask IRQ due to wake-up I-channel measurement	-
1	M_wut	0	Mask IRQ due to wake-up timer	-
0	M_osc	0	Mask IRQ due to oscillator ready	-

5.12.61 IRQ status register 1

Address: 3Ch
Type: RO
Domain: RD

Table 78. **IRQ status register 1**

Bit	Name	Default	Function	Comment
7	I_subc_start	1	IRQ due to subcarrier start	-
6	I_col	0	IRQ due to bit collision	-
5	I_wl	0	IRQ due FIFO water level	-
4	I_rx_rest	0	IRQ due to automatic reception restart	-
3	I_rxe	0	IRQ due to end of reception	-
2	I_rxs	0	IRQ due to start of reception	-
1	I_txe	0	IRQ due to end of transmission	-
0	RFU	0	-	-

5.12.62 IRQ status register 2

Address: 3Dh
Type: RO

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Domain: RD

Table 79. **IRQ status register 2**

Bit	Name	Default	Function	Comment
7	I_gpe	0	IRQ due to general purpose timer expire	-
6	I_nre	0	IRQ due to No-response timer expire	-
5	RFU	0	-	-
4	RFU	0	-	-
3	I_crc	0	IRQ due to CRC error	-
2	I_par	0	IRQ due to parity error	-
1	I_hfe	0	IRQ due to hard framing error	-
0	I_sfe	0	IRQ due to soft framing error	-

5.12.63 IRQ status register 3

Address: 3Eh
Type: RO
Domain: PD

Table 80. **IRQ status register 3**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	I_dct	0	IRQ due to termination of direct command	-
3	I_wuq	0	IRQ due to Wake-up Q-channel Measurement	-
2	I_wui	0	IRQ due to Wake-up I-channel Measurement	-
1	I_wut	0	IRQ due to Wake-up timer	-
0	I_osc	0	IRQ due to oscillator ready	-

5.12.64 IC identity register

Address: 3Fh
Type: RO
Domain: PD

Table 81. **IC identity register**

Bit	Name	Default	Function	Comment
7	ic_type4	1	IC type code 10101: ST25R100	5-bit IC type code
6	ic_type3	0		
5	ic_type2	1		
4	ic_type1	0		
3	ic_type0	1		
2	ic_rev2	0	IC revision code 000: rev 1.0 001: rev 1.1	3-bit IC revision code
1	ic_rev1	0		

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Bit	Name	Default	Function	Comment
0	ic_rev0	0	IC revision code 000: rev 1.0 001: rev 1.1	3-bit IC revision code

5.13 Direct commands

Table 82. **Direct commands**

Code (hex) [1]	Command	Comments	Chaining	I_dct	Operation mode
60, 61	Set default	Puts the ST25R100 into the power-up state	No	No	RD or PD
62, 63	Stop all activities	Stops all activities: transmission, reception, direct commands execution, timers, clear FIFO, collision, and IRQ status	Yes	No	RD
64, 65	Clear FIFO	Clears FIFO and collision status	Yes	No	RD
66, 67	Clear Rx gain	Clears the current squelch setting and loads the manual gain reduction from the register	Yes	No	RD
6A, 6B	Transmit data	Starts a data transmit sequence	No	No	RD
6C, 6D	Transmit EOF	Transmits an ISO15693 EOF (single modulation pulse)	No	No	RD
70, 71	Mask receive data	Masks the receiver (incoming data after this command is ignored)	Yes	No	RD
72, 73	Unmask receive data	Unmasks the receiver (incoming data after this command is normally processed)	Yes	No	RD
74, 75	Calibrate WU measurement	Calibrate the WU measurement	No	Yes	RD or PD
76, 77	Clear WU calibration	Clears previous calibration data	No	No	RD or PD
78, 79	WU measurement	I and Q components of the RFI signal are measured similarly as in WU mode	No	Yes	RD or PD
7A, 7B	I/Q measurement	I and Q components of the RFI signal are measured (with or without transmitter enabled)	No	Yes	RD
7C, 7D	Sense RF	Senses RF signal presence on RFI inputs (with or without transmitter enabled)	No	Yes	RD
E0, E1	Transparent mode	Enter in Transparent mode	No	No	RD
E2, E3	Start GPT	Manually starts the General purpose timer	No	No	RD
E4, E5	Start WUT	Manually starts the wake up timer	No	No	PD or RD
E6, E7	Start MRT	Manually starts the Mask receive timer	No	No	RD
E8, E9	Start NRT	Manually starts the No Response timer	No	No	RD
EA, EB	Stop NRT	Manually stops the No response timer	No	No	RD
FC	Test Register access	Enable access to test registers	No	No	PD or RD

1. *The command codes not explicitly listed shall not be used.*

5.13.1 Set default

This direct command sets the device in the same state as power-up initialization:

- Performs stop all activities command
- Sets all registers to default state
- Clears IRQ line and IRQ status bits
- Clears collision bits

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Results of the calibration and adjust commands are cleared.

5.13.2 Stop all activities

This direct command stops any ongoing activity:

- Performs clear FIFO command
- Stops data transmission and reception
- Stops all timers
- Clears IRQ line and IRQ status bits

This command does not update any register apart from the FIFO status registers. Therefore, it does not disable the field in case it was enabled.

5.13.3 Clear FIFO

This direct command clears FIFO pointers and FIFO status registers. It does not clear the IRQ line or IRQ status bits.

Ahead of a transmission it sends this command before writing data into the FIFO. If a clear FIFO command is sent during an ongoing data transmission, then the data transmission is aborted and the FIFO status registers are cleared.

5.13.4 Clear RX Gain

This command initializes both the AGC and Squelch blocks and it resets the gain reduction to the value set in afe_gain_rw<3:0>.

Sending this command also stops any ongoing squelch process.

5.13.5 Transmit commands

The transmit commands (Transmit data and transmit EOF) are used to start a data transmission from the ST25R100.

They switch the device to reception mode after the transmission is completed.

Prior to executing the command transmit data, the direct command

Clear FIFO shall be sent, followed by the definition of the number of transmitted bytes/bits, the data to be transmitted written into FIFO, as well as all configuration parameters (for example, protocol mode, bitrate, CRC, parity, framing, etc.) set.

For the direct command transmit EOF, the ISO15693 mode shall be set and it is not necessary to send the direct command clear FIFO before as the FIFO is not used.

At the end of the transmission an I_txe is produced, and the device moves into reception mode.

5.13.6 Mask receive data and unmask receive data

The direct command mask receive data disables processing of the receiver output by the Rx decoders, and AGC operation.

The direct command unmask receive data enables processing of the received data by the Rx decoders and AGC operation.

A common use of this command is to re-enable the receiver operation after it was masked by the command mask receive data. If the mask receive timer is still running while the direct command unmask receive data is received, reception is enabled, and the mask receive timer is reset.

5.13.7 Calibrate WU measurement

The command calibrates the WU measurement.

The command is triggered manually and may also be automatically executed during WU mode (depending on skip_cal and skip_recal configuration bits).

When executed from PD mode it first triggers transition to RD mode, waits for the oscillator to become stable, enables the field and then performs the measurement.

In RD mode, it enables the field and then performs the measurement itself.

Calibration result available in the I/Q channel WU display calibration registers.

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5.13.8 Clear WU calibration

The command clears the WU calibration to its default value.

Calibration result is available in the I/Q channel WU display calibration registers.

5.13.9 I/Q measurement and sense RF

These commands allow the user to measure the I and Q components of the RFI signal, whether it is an external or self-emitted field.

The measurements are similar to the WU measurement but they can only be triggered once in RD mode and the state of the transmitter is kept. Depending on tx_en it measures its own field, or check for the presence of an external one.

Before executing the measurement, a clear WU calibration command shall be executed.

The measurement result is available at:

- I/Q measurement: i_adc<7:0> and q_adc<7:0>
- Sense RF: rf_ind<6:0> as a combination of I and Q

Note: Both measurements take into account the configured gain, and calibration configuration. In the absence of the self-emitted field, the external signal is not synchronous and may lead to uneven results. It may be used to check for the presence of an external field, but not to accurately assess its intensity.

5.13.10 Transparent mode

This command sets the receiver and transmitter into the transparent mode. The device enters the transparent mode on the rising edge of the BSS signal of the SPI frame used to send the direct command. The transparent mode is maintained as long as the signal BSS is kept high, that is, the following SPI command sent from the host is automatically stopped the transparent mode.

5.13.11 Start GPT

This command manually starts the general purpose timer.

5.13.12 Start WUT

This command manually starts the wake-up timer.

5.13.13 Start MRT

This command manually starts the mark receive timer. Along with MRT, Start MRT command starts the NRT in case nrt<15:0> ≠ 0.

5.13.14 Start NRT

This command manually starts the no response timer.

5.13.15 Stop NRT

This command manually stops the no response timer.

5.13.16 Test register access

This command allows access to the device's test registers.

Test registers are not part of the normal register address space. After sending the direct command, test registers can be accessed using the normal Read/Write register operation.

The access to test registers is possible in a chained command sequence where command test register access is sent first, followed by read/write operation to test registers. The test registers are set to the default state at power-up.

Test and observation register 1

Address: 02h

Type: RW

Domain: PD

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Table 83. **Observation access 1**

Bit	Name	Default	Function	Comment
7	tm_rxwu_tad2_3	0	TAD2 test mode	Table 84
6	tm_rxwu_tad2_2	0		
5	tm_rxwu_tad2_1	0		
4	tm_rxwu_tad2_0	0		
3	tm_rxwu_tad1_3	0	TAD1 test mode	
2	tm_rxwu_tad1_2	0		
1	tm_rxwu_tad1_1	0		
0	tm_rxwu_tad1_0	0		

Table 84. **TAD1/TAD2 test mode**

tm_rxwu_tad<3:0>	tm_rxwu_tad3	tm_rxwu_tad2	tm_rxwu_tad1	tm_rxwu_tad0	Mode
3	0	0	1	1	Digital
6	0	1	1	0	Digital
Other combinations					RFU

Test and observation register 2

Address: 03h
Type: RW
Domain: PD

Table 85. **Observation register 2**

Bit	Name	Default	Function	Comment
7	tm_sigsel_tad2_3	0	TAD2 test signal	Table 86 and Table 87
6	tm_sigsel_tad2_2	0		
5	tm_sigsel_tad2_1	0		
4	tm_sigsel_tad2_0	0		
3	tm_sigsel_tad1_3	0	TAD1 test signal	
2	tm_sigsel_tad1_2	0		
1	tm_sigsel_tad1_1	0		
0	tm_sigsel_tad1_0	0		

Table 86. **TAD1/TAD2 test signal (tm_rxwu_tad=3)**

tm_sigsel_tad<3:0>	tm_sigsel _tad3	tm_sigsel _tad2	tm_sigsel _tad1	tm_sigsel _tad0	Type	Functionality
1	0	0	0	1	DO	AGD stable (agd_ok)
2	0	0	1	0	DO	Oscillator stable (osc_ok)
Other combinations					RFU	

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Table 87. **TAD1/TAD2 test signal (tm_rxwu_tad=6)**

tm_sigsel_tad<3:0>	tm_sigsel_tad3	tm_sigsel_tad2	tm_sigsel_tad1	tm_sigsel_tad0	Type	Functionality
0	0	0	0	0	DO	Tx modulation signal
1	0	0	0	1	DO	Receive decoder is enabled (rx_on)
2	0	0	1	0	DO	Correlation data signal
3	0	0	1	1	DO	Correlation collision/start detection signal
Other combinations					RFU	

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6 Electrical characteristics

6.1 Absolute maximum ratings

Any stress beyond the limits listed in Table 88, Table 89, and Table 90 may cause permanent damage to the device. These are stress ratings only.

Functional operation of the device at these or any other conditions beyond those indicated in Table 88 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 88. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}(1)	Positive supply voltage	-0.3	6	V
V_{DD_IO}(1)	Peripheral communication supply voltage	-0.3	6	
V_{GND}(1)	Negative supply voltage	-0.3	0.3	
V_{RFO}(2)	Maximum voltage on RFO1 and RFO2	-	6	V_P
I_{SCR}	Input current (latch-up immunity) according to JESD78	-100	100	mA
I_{VDD_LDO}	Maximum driver current using internal voltage regulator	-	165(3)	
ESD voltage	Electrostatic discharge voltage according to JS-001, human body model	-	2000	V
T_{strg}	Storage temperature	-65	150	°C
T_{body}	Package body temperature according to IPC/JEDEC J-STD-020(4)	-	260	
T_{Jun}	Junction temperature	-25	125	
-	Humidity non-condensing	5	85	%

1. *Referenced to V_{SS}.*
2. *Implementation of the ST25R100 must be done such whatever the condition (loaded or unloaded) the voltage does not exceed this value.*
3. *Provide good thermal management to ensure that junction temperature remains below the specified value.*
4. *Reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”.*

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6.2 Operating conditions

Table 89. Operating conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}[1]	Positive supply voltage	2.7	5.5	V
V_{DD_IO}[1]	Peripheral communication supply voltage (pin 3)	2.7	5.5	
V_{PIO}[1]	Voltage for peripheral IO communication (pins: 1, 2, 21, 22, 23, and 24)	2.7	5.5	
V_{P5V}[1]	Pin voltage (pins: 6, 8, 9, 10, 12, and 13) in the 5 V domain	0	5.5	
V_{P3V}[1]	Pin voltage (pins: 14, 15, 16, 17, 19, and 20) in the 3 V domain	0	3.6	
V_{P1V}[1]	Pin voltage (pin 5) in the 1 V domain	0	1.4	
V_{RFI_A}	RFI input amplitude[2]	0.15	3	V_{PP}
T_{Jun}	Junction temperature	-25	125	°C
T_{Amb}	Ambient temperature range	-25	85	°C

1. *Referenced to V_{SS}.*
2. *In NFC/HF reader mode the recommended signal level is 2.5 V_{PP}.*

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6.3 DC/AC characteristics for digital inputs and outputs

Table 90. Characteristics of CMOS I/Os

Type	Symbol	Parameter	Condition	Min(1)	Typ(2)	Max(1)	Unit
Input(3)	V_{IH}	High level input	V_{DD} = 2.7 - 5.5 V V_{DD_IO} = 2.7 - 5.5 V	0.8 * VDD_IO	-	-	V
	V_{IL}	Low level input voltage	V_{DD} = 2.7 - 5.5 V_{DD_IO} = 2.7-5.5 V	-	-	0.2 * VDD_IO	
	I_{LEAK}	Input leakage current	V_{DD_IO} = 2.7-5.5 V	-	-	10	µA
Output	V_{OH}	High level output voltage	V_{DD_IO} = 3.3 V I_{SOURCE} = 1 mA	0.9 * VDD_IO	-	-	V
	V_{OL}	Low level output voltage	V_{DD_IO} = 3.3 V I_{SOURCE} = 1 mA	-	-	0.1 * VDD_IO	
	C_L	Capacitive load(2)	V_{DD} = 2.7-5.5 V V_{DD_IO} = 2.7-5.5 V	-	-	50	pF
	R_O	Output resistance	V_{DD} = 2.7 - 5.5 V V_{DD_IO} = 2.7-5.5 V	-	60	160	Ω
	R_{PD}	Pull-down resistance pin MISO	V_{DD} = 2.7 - 5.5 V V_{DD_IO} = 2.7 - 5.5 V	-	10	-	kΩ

1. *Tested in production at 25 °C.*
2. *Evaluated by characterization - not tested in production.*
3. *Pins BSS, MOSI, SCLK, and RESET.*

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6.4 Electrical specifications

Table 91. Electrical characteristics (V_{DD} = 2.7 V, V_{DD_IO} = 2.7 V)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
I_{RESET}	Supply current in reset mode	T_{jun} = -25 °C to 25 °C [2]	-	0.12	1.2	µA
		T_{jun} = 85 °C[2][7]	-	0.4	5	
		T_{jun} = 125 °C[2]	-	4	20	
I_{PD}	Supply current in Power-down mode	T_{jun} = -25 °C to 25 °C [3]	-	1.2	2.2	µA
		T_{jun} = 85 °C[3][7]	-	3.5	15	
		T_{jun} = 125 °C[3]	-	20	62	
I_{WU}	Supply current in Wake-up mode	T_{jun} = -25 °C to 25 °C[4]	-	1.7	4.2	µA
		T_{jun} = 85 °C[4][7]	-	4	15	
		T_{jun} = 125 °C [4]	-	20	62	
I_{RD}	Supply current in Ready mode	[5]	-	4.2	9.5	mA
I_{ALL}	Supply current all active	[6]	-	12	23	mA
R_{RFO}	RFO1 and RFO2 driver output resistance	V_{RFO}=150 mV[7]	-	2	4	Ω
R_{RFI}	RFI input resistance	[7]	8	11	15	kΩ
V_{POR}	Power on reset voltage	[7]	0.3	0.75	1.3	V
V_{AGD}	AGD voltage	[5]	1.4	1.5	1.6	V
t_{RESET}	Time between RESET pin in high state to device reset	[7]	10	-	-	µs
t_{BOOT}	Time between power On/RESET high-to-low transition and first SPI operation	[7]	1000	-	-	µs

1. *The minimum and maximum values are tested in production at 25 °C, values at different temperatures are evaluated by characterization.*
2. *The registers are in the default state.*
3. *The register 01h is set to 04h (miso_pd1 enabled), and the other registers are in the default state.*
4. *The register 00h is set to 01h (wake-up enabled), register 01h is set to 04h (miso_pd1 enabled), and the other registers are in default state.*
5. *The register 00h is set to 02h (Enabled), and the other registers are in the default state.*
6. *The register 00h is set to 3Ah (Enabled, VDD_AM enabled, Tx enabled, Rx enabled), the register 03h is set to 0Fh (RFO segments disabled), and the other registers are in default state.*
7. *Evaluated by characterization - not tested in production.*

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Table 92. Electrical characteristics (V_{DD} = 3.3 V, V_{DD_IO} = 3.3 V)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
I_{RESET}	Supply current in reset mode	T_{jun} = -25 °C to 25 °C [2]	-	0.15	1.2	µA
		T_{jun} = 85°C [2][7]	-	0.6	5	
		T_{jun} = 125 °C[2]	-	5	24	
I_{PD}	Supply current in power-down mode	T_{jun} = -25 °C to 25 °C [3]	-	1.4	2.7	µA
		T_{jun} = 85 °C[3][7]	-	4.1	16	
		T_{jun} = 125 °C[3]	-	21	67	
I_{WU}	Supply current in wake up mode	T_{jun} = -25 °C to 25 °C[4]	-	2.0	4.5	µA
		T_{jun} = 85 °C[4][7]	-	4.5	17	
		T_{jun} = 125 °C [4]	-	21	68	
I_{RD}	Supply current in Ready mode	[5]	-	4.8	11	mA
I_{ALL}	Supply current all active	[6]	-	13	25	mA
R_{RFO}	RFO1 and RFO2 driver output resistance	V_{RFO}=150 mV[7]	-	1.5	3	Ω
R_{RFI}	RFI input resistance	[7]	8	11	15	kΩ
V_{POR}	Power on reset voltage	[7]	0.3	0.75	1.3	V
V_{AGD}	AGD voltage	[5]	1.4	1.5	1.6	V
t_{RESET}	Time between RESET pin in high state to device reset	[7]	10	-	-	µs
t_{BOOT}	Time between power On/RESET high-to-low transition and first SPI operation	[7]	500	-	-	µs

1. *The minimum and maximum values are tested in production at 25°C, and other temperature values are evaluated by characterization.*
2. *The registers are in the default state.*
3. *The register 01h is set to 04h (miso_pd1 enabled), and the other registers are in the default state.*
4. *The register 00h is set to 01h (wake-up enabled), register 01h is set to 04h (miso_pd1 enabled), and the other registers are in default state.*
5. *The register 00h is set to 02h (Enabled), and the other registers are in the default state.*
6. *The register 00h is set to 3Ah (Enabled, VDD_AM enabled, Tx enabled, Rx enabled), the register 03h is set to 0Fh (RFO segments disabled), and the other registers are in default state.*
7. *Evaluated by characterization - not tested in production.*

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Table 93. Electrical characteristics (V_{DD} = 5.5 V, V_{DD_IO} = 5.5 V)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
I_{RESET}	Supply current in reset mode	T_{jun} = -25 °C to 25 °C [2]	-	0.27	3	µA
		T_{jun} = 85°C [2][7]	-	0.53	11	
		T_{jun} = 125 °C[2]	-	9	45	
I_{PD}	Supply current in Power-down mode	T_{jun} = -25 °C to 25 °C [3]	-	2.3	4.2	µA
		T_{jun} = 85 °C[3][7]	-	3.6	22	
		T_{jun} = 125 °C[3]	-	25	89	
I_{WU}	Supply current in Wake-up mode	T_{jun} = -25 °C to 25 °C[4]	-	2.9	5.2	µA
		T_{jun} = 85 °C[4][7]	-	4.1	23	
		T_{jun} = 125 °C [4]	-	25	90	
I_{RD}	Supply current in Ready mode	[5]	-	6	12	mA
I_{ALL}	Supply current all active	[6]	-	15	27	mA
R_{RFO}	RFO1 and RFO2 driver output resistance	V_{RFO}=150 mV[7]	-	1	2.5	Ω
R_{RFI}	RFI input resistance	-	8	11	15	kΩ
V_{POR}	Power on reset voltage	[7]	0.3	0.75	1.3	V
V_{AGD}	AGD voltage	[5]	1.4	1.5	1.6	V
t_{RESET}	Time between RESET pin in high state to device reset	-	10	-	-	µs
t_{BOOT}	Time between Power On/RESET high-to-low transition and first SPI operation	-	350	-	-	µs

1. *The minimum and maximum values are tested in production at 25°C, and other temperature values are evaluated by characterization.*
2. *The registers are in the default state.*
3. *The register 01h is set to 04h (miso_pd1 enabled), and the other registers are in the default state.*
4. *The register 00h is set to 01h (wake-up enabled), register 01h is set to 04h (miso_pd1 enabled), and the other registers are in default state.*
5. *The register 00h is set to 02h (Enabled), and the other registers are in the default state.*
6. *The register 00h is set to 3Ah (Enabled, VDD_AM enabled, Tx enabled, Rx enabled), the register 03h is set to 0Fh (RFO segments disabled), and the other registers are in default state.*
7. *Evaluated by characterization - not tested in production.*

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6.5 SPI interface characteristics

Table 94. SPI interface characteristics(up to 6 MHz)

Operation	Symbol	Parameter	Conditions (1)	Min	Typ	Max	Unit
General	T_{SCLK}	SCLK period	$T_{SCLK}=T_{SCLKL} + T_{SCLKH}$	165	-	-	ns
	T_{SCLKL}	SCLK low	-	80	-	-	
	T_{SCLKH}	SCLK high	-	80	-	-	
	T_{SSH}	SPI reset (BSS high)	-	100	-	-	
	T_{NCSL}	BSS falling to SCLK rising	First SCLK pulse	25	-	-	
	T_{NCSH}	SCLK falling to BSS rising	Last SCLK pulse	25	-	-	
	T_{DIS}	Data in setup time	-	10	-	-	
	T_{DIH}	Data in hold time	-	10	-	-	
	T_{DOD}	Data out delay	C_{load} < 50 pF	-	20	45	
	T_{DOHZ}	Data out to high impedance delay	C_{load} < 50 pF	-	20	-	
Read	T_{DOD}	Data out delay	C_{load} < 50 pF	-	20	45	
	T_{DOHZ}	Data out to high impedance delay	C_{load} < 50 pF	-	20	-	

1. *Evaluated by characterization - not tested in production.*

Figure 20. SPI timing diagram - General operation

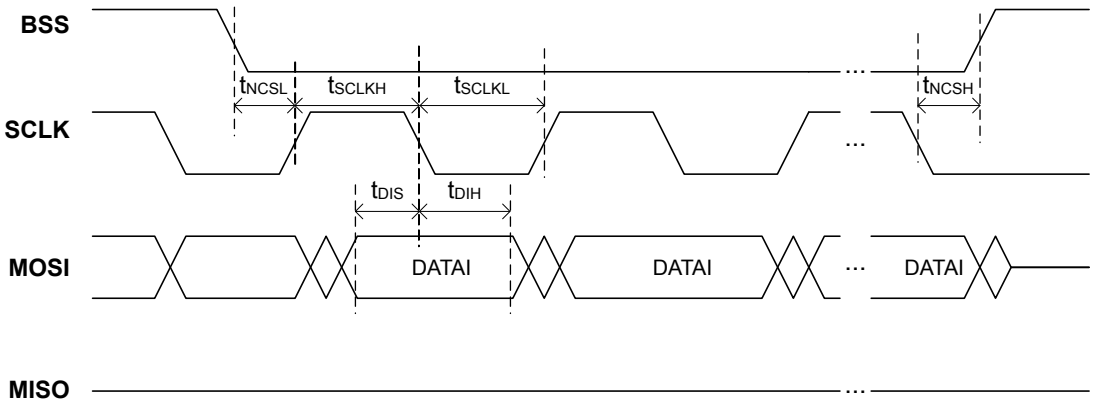
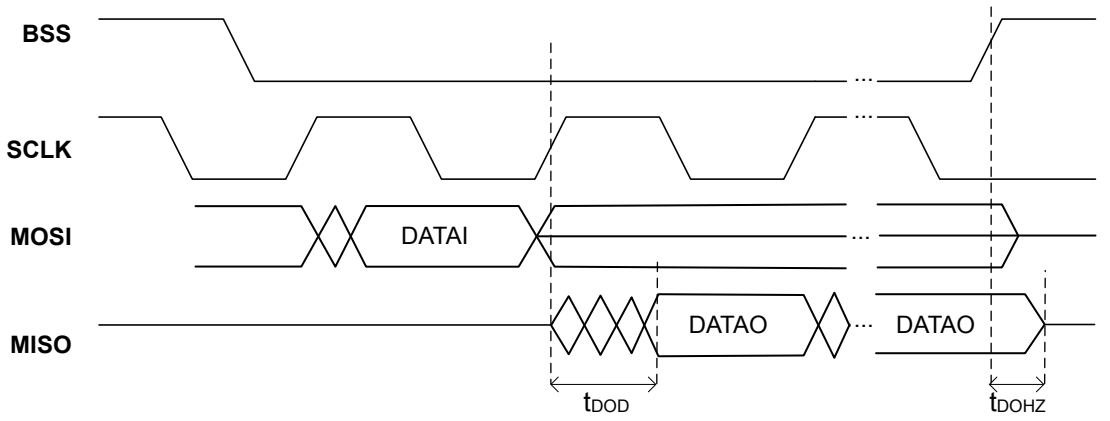


Figure 21. SPI timing diagram - Read operation



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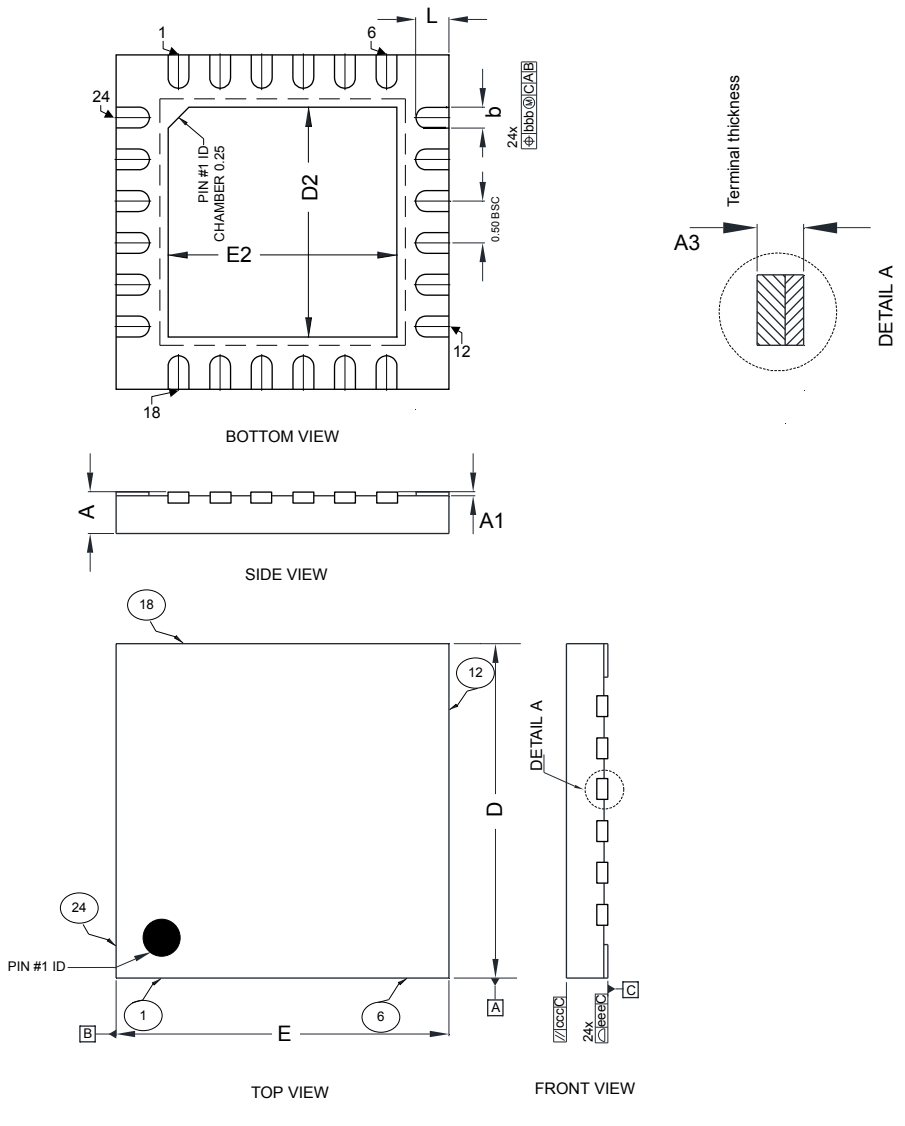
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 UFQFPN24 package information

This UFQFPN is a 24 pins, 4 x 4 mm, 0.5 mm pitch, thermally enhanced ultra-thin fine pitch quad flat no lead package.

Figure 22. UFQFPN24 - Outline



1. *Drawing is not to scale.*
2. *Co-planarity applies to the exposed pad as well as the terminal.*

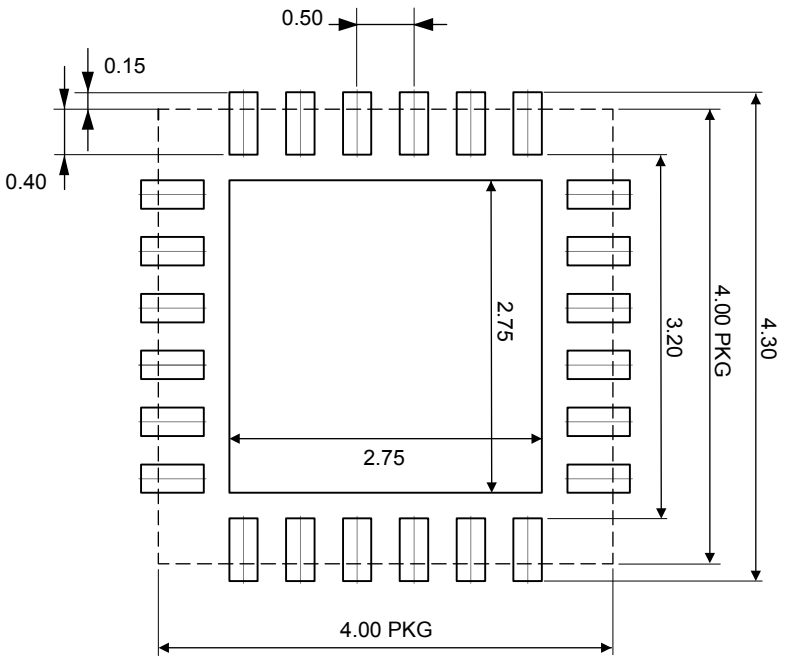
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Table 95. **UFQFPN24 - Mechanical data**

Symbol	Millimetres			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.45	-	0.60	0.0177	-	0.0236
A1	0	-	0.05	0	-	0.0020
A3[2]		0.152 REF			0.0060 REF	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D[3]		4.00 BSC			0.1575 BSC	
E[3]		4.00 BSC			0.1575 BSC	
e[3]		0.50 BSC			0.0197 BSC	
D2	2.60	-	2.85	0.1024	-	0.1122
E2	2.60	-	2.85	0.1024	-	0.1122
bbb	-	0.10	-	-	0.0039	-
ccc	-	0.10	-	-	0.0039	-
eee	-	0.08	-	-	0.0031	-
N[4]		24			24	

1. *Values in inches are converted from mm and rounded to 3 decimal digits.*
2. *REF stands for REFERENCE.*
3. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table*
4. *Total number of terminals*

Figure 23. **UFQFPN24 - Footprint example**



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1. *Dimensions are expressed in millimetres.*

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8 Ordering information

Table 96. Ordering information scheme

Example: ST25 R 100 -C ME T

Device type

ST25 = NFC/RFID tags and readers

Product type

R = NFC/HF reader

Product feature

100 = Entry-level NFC reader for consumer and industrial

Ambient temperature range

C = -25 °C to 85 °C

Package/Packaging

ME = 24-pin UFQFPN (4 x 4 mm) with no wettable flanks

Tape and reel

T = 5000 pcs/reel

Note: For a list of available options (speed, package, etc.) or for further information on any aspect of this device, contact your nearest ST sales office.

Note: Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

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Revision history

Table 97. **Document revision history**

Date	Version	Changes
01-Dec-2023	1	Initial release.
02-Feb-2024	2	Updated: • Section Features • Figure 3. System diagram - differential antenna driving • Figure 4. System diagram - single-ended antenna driving • Figure 5. System diagram – two single-ended antenna driving
20-Mar-2024	3	Updated Section 7: Package information
04-Apr-2024	4	Changed the document scope from ST restricted to public.

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