# SiT8924
## Automotive AEC-Q100 Oscillator

The Smart Timing Choice™

## Features

- AEC-Q100 with extended temperature range (-55°C to 125°C)
- Frequencies between 1 MHz and 110 MHz accurate to 6 decimal places
- Supply voltage of 1.8V or 2.25V to 3.63V
- Excellent total frequency stability as low as ±25 ppm
- Industry best G-sensitivity of 0.1 PPB/G
- Low power consumption of 3.8 mA typical at 1.8V
- LVCMOS/LVTTL compatible output
- Industry-standard packages: 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

## Applications

- Automotive, extreme temperature and other high-rel electronics
- Infotainment systems, collision detection devices, and in-vehicle networking
- Power train control




## Electrical Specifications

### Table 1. Electrical Characteristics[1, 2]

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency Range** | | | | | | |
| **Output Frequency Range** | f | 1 | – | 110 | MHz | Refer to Table 13 and Table 14 for a list supported frequencies |
| **Frequency Stability and Aging** | | | | | | |
| **Frequency Stability** | F_stab | -25 | – | +25 | ppm | Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load (15 pF ± 10%). |
| | | -30 | – | +30 | ppm | |
| | | -50 | – | +50 | ppm | |
| **Operating Temperature Range** | | | | | | |
| **Operating Temperature Range (ambient)** | T_use | -40 | – | +105 | °C | Extended Industrial, AEC-Q100 Grade 2 |
| | | -40 | – | +125 | °C | Automotive, AEC-Q100 Grade 1 |
| | | -55 | – | +125 | °C | Extended Temperature, AEC-Q100 |
| **Supply Voltage and Current Consumption** | | | | | | |
| **Supply Voltage** | Vdd | 1.62 | 1.8 | 1.98 | V | All voltages between 2.25V and 3.63V including 2.5V, 2.8V, 3.0V and 3.3V are supported. |
| | | 2.25 | – | 3.63 | V | |
| **Current Consumption** | Idd | – | 4.0 | 4.8 | mA | No load condition, f = 20 MHz, Vdd = 2.25V to 3.63V |
| | | – | 3.8 | 4.5 | mA | No load condition, f = 20 MHz, Vdd = 1.8V |
| **LVCMOS Output Characteristics** | | | | | | |
| **Duty Cycle** | DC | 45 | – | 55 | % | All Vdds |
| **Rise/Fall Time** | Tr, Tf | – | 1.5 | 3 | ns | Vdd = 2.25V - 3.63V, 20% - 80% |
| | | – | 1.3 | 2.5 | ns | Vdd = 1.8V, 20% - 80% |
| **Output High Voltage** | VOH | 90% | – | – | Vdd | IOH = -4 mA (Vdd = 3.0V or 3.3V)<br>IOH = -3 mA (Vdd = 2.8V and Vdd = 2.5V)<br>IOH = -2 mA (Vdd = 1.8V) |
| **Output Low Voltage** | VOL | – | – | 10% | Vdd | IOL = 4 mA (Vdd = 3.0V or 3.3V)<br>IOL = 3 mA (Vdd = 2.8V and Vdd = 2.5V)<br>IOL = 2 mA (Vdd = 1.8V) |
| **Input Characteristics** | | | | | | |
| **Input High Voltage** | VIH | 70% | – | – | Vdd | Pin 1, OE |
| **Input Low Voltage** | VIL | – | – | 30% | Vdd | Pin 1, OE |
| **Input Pull-up Impedence** | Z_in | – | 100 | – | kΩ | Pin 1, OE logic high or logic low |
| **Startup and Resume Timing** | | | | | | |
| **Startup Time** | T_start | – | – | 10 | ms | Measured from the time Vdd reaches 90% of final value |
| **Enable/Disable Time** | T_oe | – | – | 130 | ns | f = 110 MHz. For other frequencies, T_oe = 100 ns + 3 * cycles |
| **Jitter** | | | | | | |
| **RMS Period Jitter** | T_jitt | – | 1.6 | 2.5 | ps | f = 75 MHz, 2.25V to 3.63V |
| | | – | 1.9 | 3.0 | ps | f = 75 MHz, 1.8V |
| **RMS Phase Jitter (random)** | T_phj | – | 0.5 | – | ps | f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz |
| | | – | 1.3 | – | ps | f = 75 MHz, Integration bandwidth = 12 kHz to 20 MHz |

**Notes:**

1. All electrical specifications in the above table are specified with 15 pF output load and for all Vdd(s) unless otherwise stated.
2. The typical value of any parameter in the Electrical Characteristics table is specified for the nominal value of the highest voltage option for that parameter and at 25 °C temperature.

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## Table 2. Pin Description

| Pin | Symbol | | Functionality |
|---|---|---|---|
| 1 | OE/NC | Output Enable | H[3]: specified frequency output<br>L: output is high impedance. Only output driver is disabled. |
| | | No Connect | Any voltage between 0 and Vdd or Open[3]: Specified frequency output. Pin 1 has no function. |
| 2 | GND | Power | Electrical ground[4] |
| 3 | OUT | Output | Oscillator output |
| 4 | VDD | Power | Power supply voltage[4] |

**Notes:**

3. In OE mode, a pull-up resistor of 10kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
4. A capacitor of value 0.1 µF or higher between Vdd and GND is required.

**Top View**

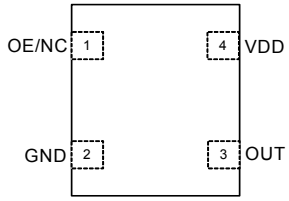



**Figure 1. Pin Assignments**

## Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| **Storage Temperature** | -65 | 150 | °C |
| **Vdd** | -0.5 | 4 | V |
| **Electrostatic Discharge** | – | 2000 | V |
| **Soldering Temperature (follow standard Pb free soldering guidelines)** | – | 260 | °C |
| **Junction Temperature[5]** | – | 150 | °C |

**Note:**

5.Exceeding this temperature for extended period of time may damage the device.

## Table 4. Thermal Consideration[6]

| Package | θJA, 4 Layer Board (°C/W) | θJA, 2 Layer Board (°C/W) | θJC, Bottom (°C/W) |
|---|---|---|---|
| **7050** | 142 | 273 | 30 |
| **5032** | 97 | 199 | 24 |
| **3225** | 109 | 212 | 27 |
| **2520** | 117 | 222 | 26 |
| **2016** | 152 | 252 | 36 |

**Note:**

6. Refer to JESD51 for θJA and θJC definitions, and reference layout used to determine the θJA and θJC values in the above table.

## Table 5. Maximum Operating Junction Temperature[7]

| Max Operating Temperature (ambient) | Maximum Operating Junction Temperature |
|---|---|
| 105°C | 115°C |
| 125°C | 135°C |

**Note:**

7. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

## Table 6. Environmental Compliance

| Parameter | Condition/Test Method |
|---|---|
| **Mechanical Shock** | **MIL-STD-883F, Method 2002** |
| **Mechanical Vibration** | **MIL-STD-883F, Method 2007** |
| **Temperature Cycle** | **JESD22, Method A104** |
| **Solderability** | **MIL-STD-883F, Method 2003** |
| **Moisture Sensitivity Level** | **MSL1 @ 260°C** |


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## Test Circuit and Waveform[8]

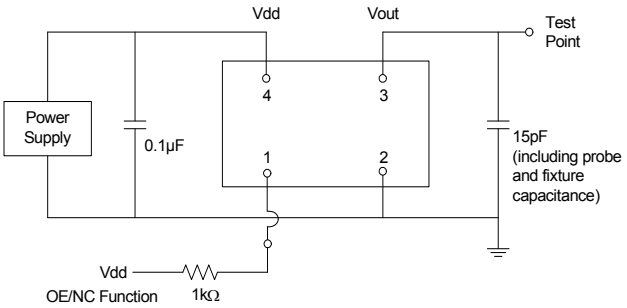



**Figure 2. Test Circuit**

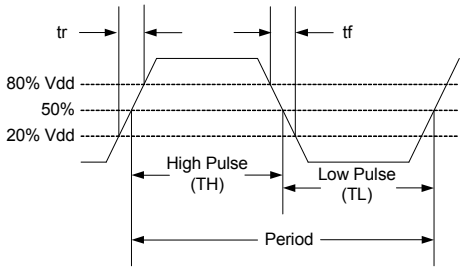
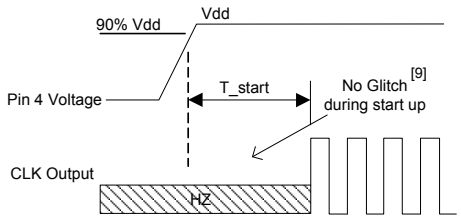



**Figure 3. Waveform**

**Note:**

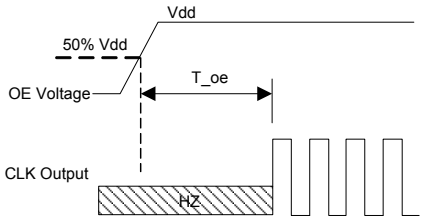
8. Duty Cycle is computed as Duty Cycle = TH/Period.

## Timing Diagrams



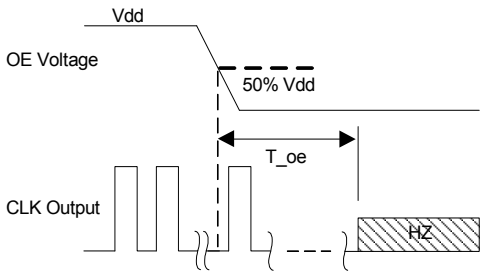

T_start: Time to start from power-off

**Figure 4. Startup Timing (OE Mode)**




T_oe: Time to re-enable the clock output

**Figure 5. OE Enable Timing (OE Mode Only)**




T_oe: Time to put the output in High Z mode

**Figure 6. OE Disable Timing (OE Mode Only)**

**Note:**

9 SiT8924 has “no runt” pulses and “no glitch” output during startup or resume.


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## Performance Plots[10]

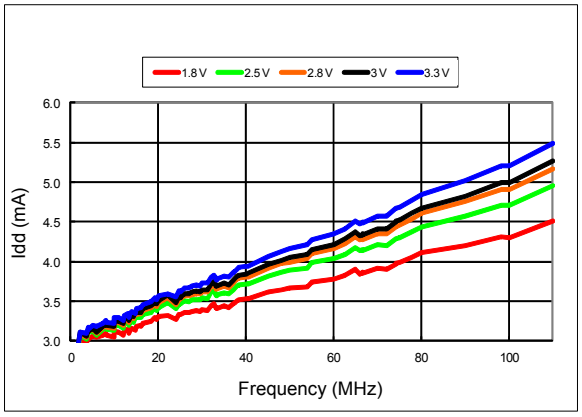



**Figure 7. Idd vs Frequency**

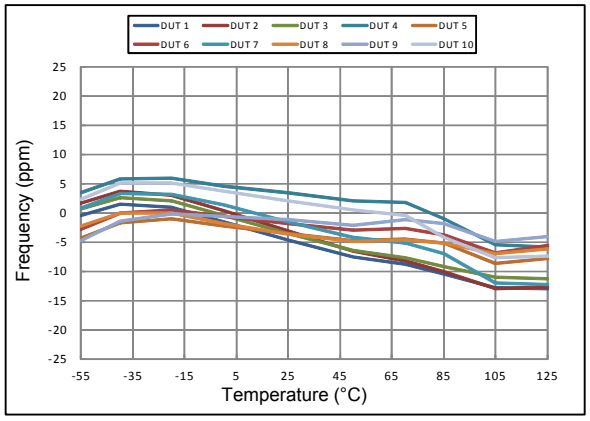



**Figure 8. Frequency vs Temperature**

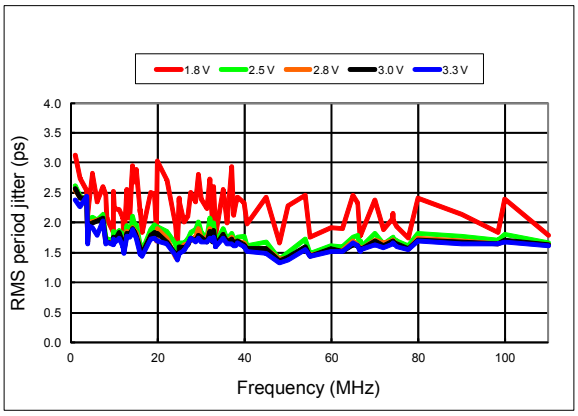



**Figure 9. RMS Period Jitter vs Frequency**

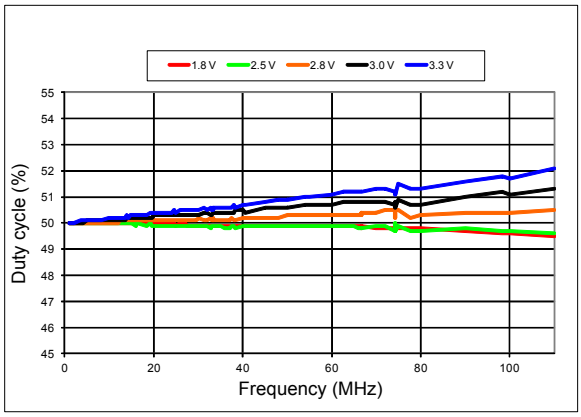



**Figure 10. Duty Cycle vs Frequency**

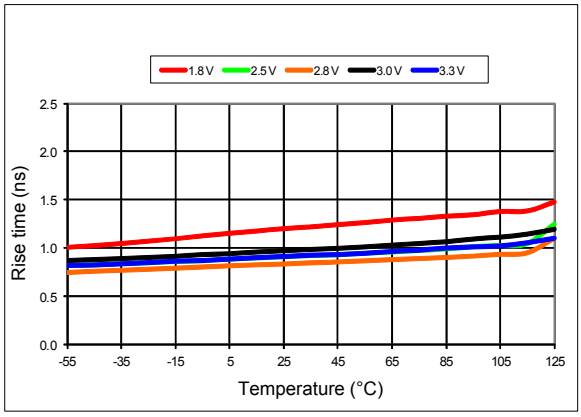



**Figure 11. 20%-80% Rise Time vs Temperature**

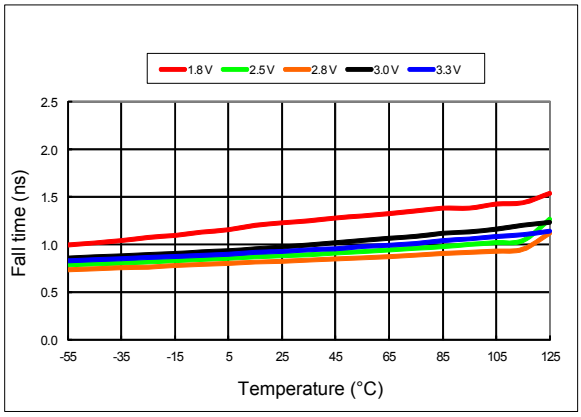



**Figure 12. 20%-80% Fall Time vs Temperature**


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## Performance Plots[10]

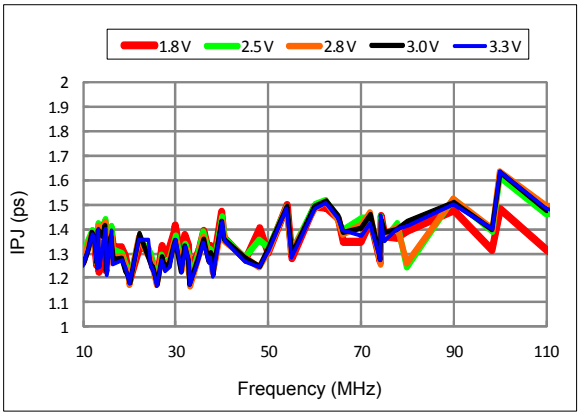



**Figure 13. RMS Integrated Phase Jitter Random (12 kHz to 20 MHz) vs Frequency[11]**

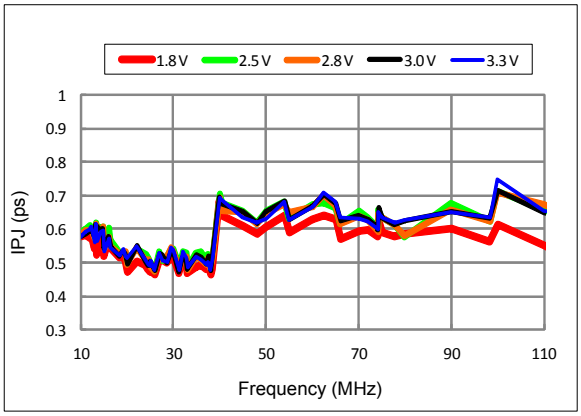



**Figure 14. RMS Integrated Phase Jitter Random (900 kHz to 7.5 MHz) vs Frequency[11]**

**Notes:**

10. All plots are measured with 15 pF load at room temperature, unless otherwise stated.
11. Phase noise plots are measured with Agilent E5052B signal source analyzer. Integration range is up to 5 MHz for carrier frequencies up to 40 MHz.


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## Programmable Drive Strength

The SiT8924 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time.
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Application Notes section: http://www.sitime.com/support/application-notes.

### EMI Reduction by Slowing Rise/Fall Time

Figure 15 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

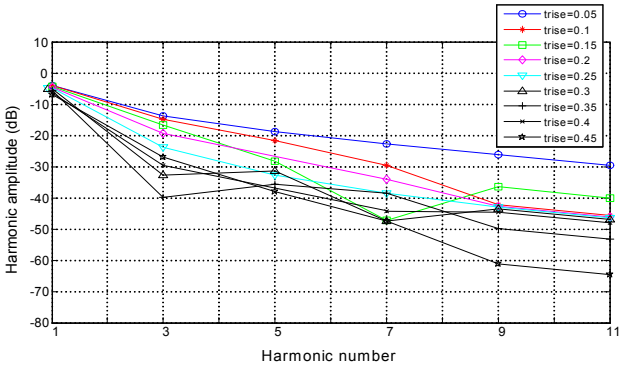



**Figure 15. Harmonic EMI reduction as a Function of Slower Rise/Fall Time**

### Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 11) to determine the proper drive strength.

### High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V SiT8924 device with default drive strength setting, the typical rise/fall time is 1ns for 15 pF output load. The typical rise/fall time slows down to 2.6 ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.83 ns by then increasing the drive strength setting on the SiT8924.

The SiT8924 can support up to 60 pF in maximum capacitive loads with drive strength settings. Refer to the Rise/Tall Time Tables (Table 7 to 11) to determine the proper drive strength for the desired combination of output load vs. rise/fall time

### SiT8924 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the SiT8924 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

### Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 7 through 11, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature can be calculated as follows:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf_20/80}}$$

where Trf_20/80 is the typical value for 20%-80% rise/fall time.

***Example 1***

Calculate $f_{MAX}$ for the following condition:

- Vdd = 1.8V (Table 7)
- Capacitive Load: 30 pF
- Desired Tr/f time = 3 ns (rise/fall time part number code = E)

Part number for the above example:

SiT8924AI**E**12-18E-66.666660

Drive strength code is inserted here. Default setting is "-"


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## Rise/Fall Time (20% to 80%) vs $C_{LOAD}$ Tables

**Table 7. Vdd = 1.8V Rise/Fall Times for Specific $C_{LOAD}$**

| Rise/Fall Time Typ (ns) | | | | | |
|---|---|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 6.16 | 11.61 | 22.00 | 31.27 | 39.91 |
| A | 3.19 | 6.35 | 11.00 | 16.01 | 21.52 |
| R | 2.11 | 4.31 | 7.65 | 10.77 | 14.47 |
| B | 1.65 | 3.23 | 5.79 | 8.18 | 11.08 |
| T | 0.93 | 1.91 | 3.32 | 4.66 | 6.48 |
| E | 0.78 | 1.66 | 2.94 | 4.09 | 5.74 |
| U | 0.70 | 1.48 | 2.64 | 3.68 | 5.09 |
| F or "-": default | 0.65 | 1.30 | 2.40 | 3.35 | 4.56 |

**Table 8. Vdd = 2.5V Rise/Fall Times for Specific $C_{LOAD}$**

| Rise/Fall Time Typ (ns) | | | | | |
|---|---|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 4.13 | 8.25 | 12.82 | 21.45 | 27.79 |
| A | 2.11 | 4.27 | 7.64 | 11.20 | 14.49 |
| R | 1.45 | 2.81 | 5.16 | 7.65 | 9.88 |
| B | 1.09 | 2.20 | 3.88 | 5.86 | 7.57 |
| T | 0.62 | 1.28 | 2.27 | 3.51 | 4.45 |
| E or "-": default | 0.54 | 1.00 | 2.01 | 3.10 | 4.01 |
| U | 0.43 | 0.96 | 1.81 | 2.79 | 3.65 |
| F | 0.34 | 0.88 | 1.64 | 2.54 | 3.32 |

**Table 9. Vdd = 2.8V Rise/Fall Times for Specific $C_{LOAD}$**

| Rise/Fall Time Typ (ns) | | | | | |
|---|---|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 3.77 | 7.54 | 12.28 | 19.57 | 25.27 |
| A | 1.94 | 3.90 | 7.03 | 10.24 | 13.34 |
| R | 1.29 | 2.57 | 4.72 | 7.01 | 9.06 |
| B | 0.97 | 2.00 | 3.54 | 5.43 | 6.93 |
| T | 0.55 | 1.12 | 2.08 | 3.22 | 4.08 |
| E or "-": default | 0.44 | 1.00 | 1.83 | 2.82 | 3.67 |
| U | 0.34 | 0.88 | 1.64 | 2.52 | 3.30 |
| F | 0.29 | 0.81 | 1.48 | 2.29 | 2.99 |

**Table 10. Vdd = 3.0V Rise/Fall Times for Specific $C_{LOAD}$**

| Rise/Fall Time Typ (ns) | | | | | |
|---|---|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 3.60 | 7.21 | 11.97 | 18.74 | 24.30 |
| A | 1.84 | 3.71 | 6.72 | 9.86 | 12.68 |
| R | 1.22 | 2.46 | 4.54 | 6.76 | 8.62 |
| B | 0.89 | 1.92 | 3.39 | 5.20 | 6.64 |
| T or "-": default | 0.51 | 1.00 | 1.97 | 3.07 | 3.90 |
| E | 0.38 | 0.92 | 1.72 | 2.71 | 3.51 |
| U | 0.30 | 0.83 | 1.55 | 2.40 | 3.13 |
| F | 0.27 | 0.76 | 1.39 | 2.16 | 2.85 |

**Table 11. Vdd = 3.3V Rise/Fall Times for Specific $C_{LOAD}$**

| Rise/Fall Time Typ (ns) | | | | | |
|---|---|---|---|---|---|
| Drive Strength \ $C_{LOAD}$ | 5 pF | 15 pF | 30 pF | 45 pF | 60 pF |
| L | 3.39 | 6.88 | 11.63 | 17.56 | 23.59 |
| A | 1.74 | 3.50 | 6.38 | 8.98 | 12.19 |
| R | 1.16 | 2.33 | 4.29 | 6.04 | 8.34 |
| B | 0.81 | 1.82 | 3.22 | 4.52 | 6.33 |
| T or "-": default | 0.46 | 1.00 | 1.86 | 2.60 | 3.84 |
| E | 0.33 | 0.87 | 1.64 | 2.30 | 3.35 |
| U | 0.28 | 0.79 | 1.46 | 2.05 | 2.93 |
| F | 0.25 | 0.72 | 1.31 | 1.83 | 2.61 |


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## Pin 1 Configuration Options (OE or NC)

Pin 1 of the SiT8924 can be factory-programmed to support two modes: Output Enable (OE) or No Connect (NC).

### Output Enable (OE) Mode

In the OE mode, applying logic low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in <1µs.

### No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and output the specified frequency regardless of the logic level on pin 1.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE or NC mode.

**Table 12. OE vs. NC**

| | OE | NC |
|---|---|---|
| Active current 20 MHz (max, 1.8V) | 4.5 mA | 4.5 mA |
| OE disable current (max. 1.8V) | 3.8 mA | N/A |
| OE enable time at 110 MHz (max) | 130 ns | N/A |
| Output driver in OE disable | High Z | N/A |

## Output on Startup and OE Enable

The SiT8924 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or when the output driver is enabled.

In addition, the SiT8924 supports “no runt” pulses and “no glitch” output during startup or when the device output driver is enabled as shown in the waveform captures in Figure 16 and Figure 17.

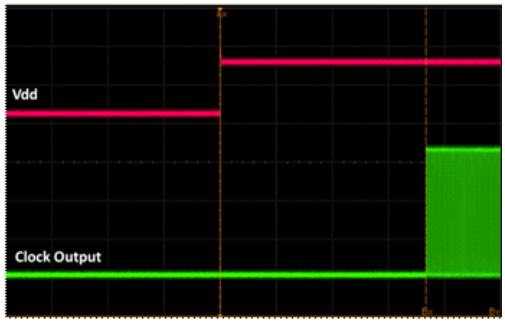



**Figure 16. Startup Waveform vs. Vdd**

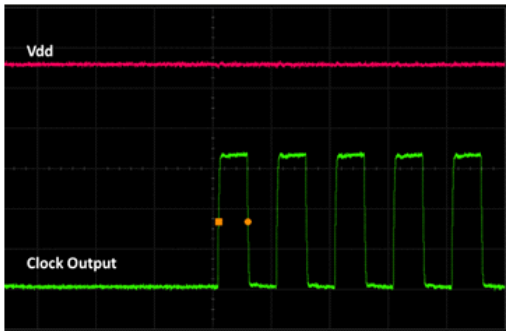
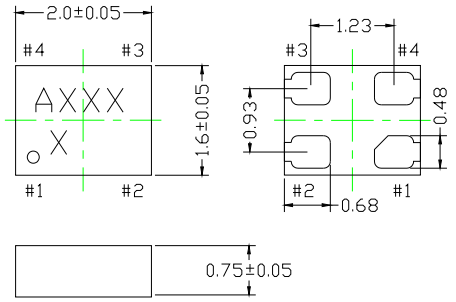
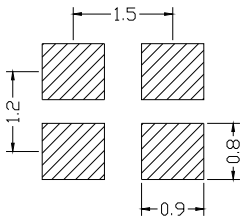
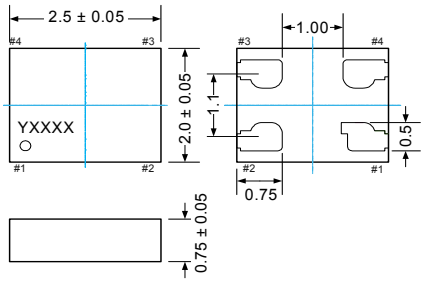
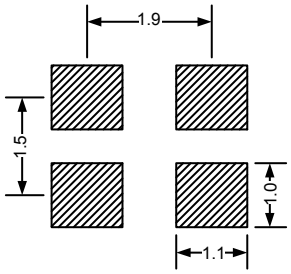
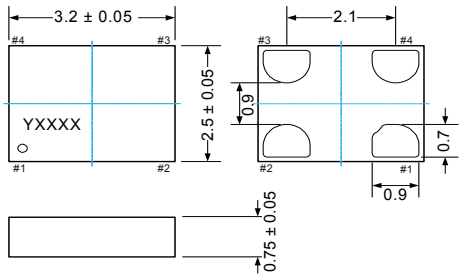
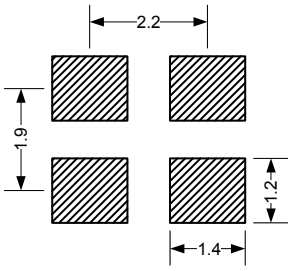
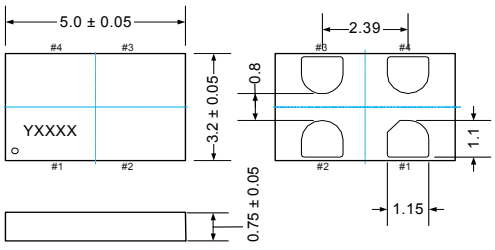
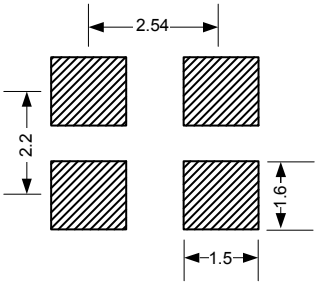



**Figure 17. Startup Waveform vs. Vdd (Zoomed-in View of Figure 16)**

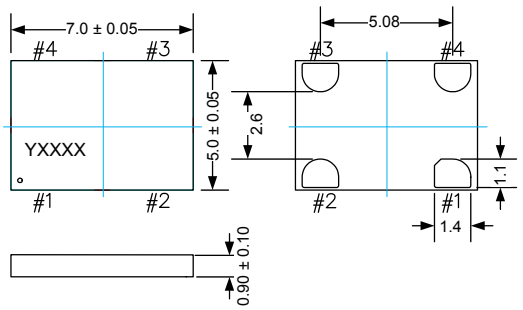
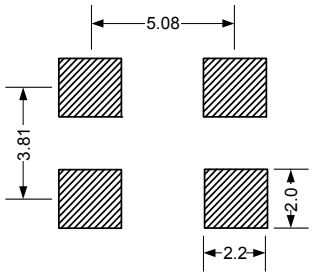

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## Dimensions and Patterns

| Package Size – Dimensions (Unit: mm)[12] | Recommended Land Pattern (Unit: mm)[13] |
|---|---|
| **2.0 x 1.6 x 0.75 mm**   |   |
| **2.5 x 2.0 x 0.75 mm**   |   |
| **3.2 x 2.5 x 0.75 mm**   |   |
| **5.0 x 3.2 x 0.75 mm**   |   |


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## Dimensions and Patterns

| Package Size – Dimensions (Unit: mm)[12] | Recommended Land Pattern (Unit: mm)[13] |
|---|---|
| **7.0 x 5.0 x 0.90 mm**  |  |





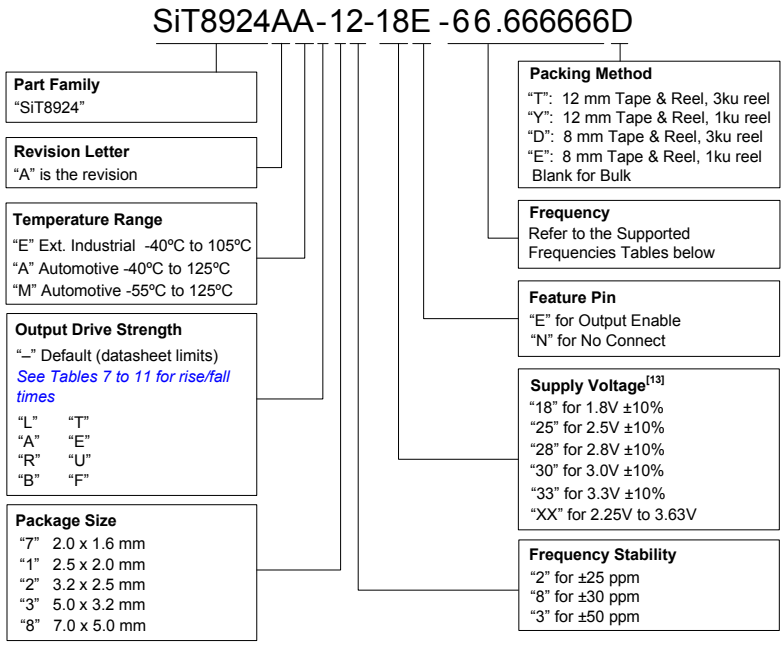
**Notes:**

12. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
13. A capacitor of value 0.1 µF or higher between Vdd and GND is required.


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## Ordering Information

**The Part No. Guide is for reference only. To customize and build an exact part number, use the SiTime Part Number Generator.**




**Note:**

13. The voltage portion of the SiT8924 part number consists of two characters that denote the specific supply voltage of the device. The SiT8924 supports either 1.8V ±10% or any voltage between 2.25V and 3.62V. In the 1.8V mode, one can simply insert 18 in the part number. In the 2.5V to 3.3V mode, two digits such as 18, 25 or 33 can be used in the part number to reflect the desired voltage. Alternatively, "XX" can be used to indicate the entire operating voltage range from 2.25V to 3.63V.

### Table 13. Supported Frequencies (-40°C to ±105°C or -40°C to ±125°C)[14, 15]

| Frequency Range | |
|---|---|
| Min. | Max. |
| 1.000000 MHz | 61.222999 MHz |
| 61.674001 MHz | 69.795999 MHz |
| 70.485001 MHz | 79.062999 MHz |
| 79.162001 MHz | 81.427999 MHz |
| 82.232001 MHz | 91.833999 MHz |
| 92.155001 MHz | 94.248999 MHz |
| 94.430001 MHz | 94.874999 MHz |
| 94.994001 MHz | 97.713999 MHz |
| 98.679001 MHz | 110.000000 MHz |

### Table 14. Supported Frequencies (-55°C to ±125°C)[14, 15]

| Frequency Range | |
|---|---|
| Min. | Max. |
| 1.000000 MHz | 61.222999 MHz |
| 61.674001 MHz | 69.239999 MHz |
| 70.827001 MHz | 78.714999 MHz |
| 79.561001 MHz | 80.159999 MHz |
| 80.174001 MHz | 80.779999 MHz |
| 82.632001 MHz | 91.833999 MHz |
| 95.474001 MHz | 96.191999 MHz |
| 96.209001 MHz | 96.935999 MHz |
| 99.158001 MHz | 110.000000 MHz |

**Notes:**

14. Any frequency within the min and max values in the above tables are supported with 6 decimal places of accuracy.
15. Please contact SiTime for frequencies that are not listed in the tables above.

### Table 15. Ordering Codes for Supported Tape & Reel Packing Method

| Device Size (mm x mm) | 16 mm T&R (3ku) | 16 mm T&R (1ku) | 12 mm T&R (3ku) | 12 mm T&R (1ku) | 8 mm T&R (3ku) | 8 mm T&R (1ku) |
|---|---|---|---|---|---|---|
| 2.0 x 1.6 | – | – | – | – | D | E |
| 2.5 x 2.0 | – | – | – | – | D | E |
| 3.2 x 2.5 | – | – | – | – | D | E |
| 5.0 x 3.2 | – | – | T | Y | – | – |
| 7.0 x 5.0 | T | Y | – | – | – | – |


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### Table 16. Additional Information

| Document | Description | Download Link |
|---|---|---|
| **Time Machine II** | MEMS oscillator programmer | http://www.sitime.com/support/time-machine-oscillator-programmer |
| **Field Programmable Oscillators** | Devices that can be programmable in the field by Time Machine II | http://www.sitime.com/products/field-programmable-oscillators |
| **Manufacturing Notes** | Tape & Reel dimension, reflow profile and other manufacturing related info | http://www.sitime.com/component/docman/doc_download/243-manufacturing-notes-for-sitime-oscillators |
| **Qualification Reports** | RoHS report, reliability reports, composition reports | http://www.sitime.com/support/quality-and-reliability |
| **Performance Reports** | Additional performance data such as phase noise, current consumption and jitter for selected frequencies | http://www.sitime.com/support/performance-measurement-report |
| **Termination Techniques** | Termination design recommendations | http://www.sitime.com/support/application-notes |
| **Layout Techniques** | Layout recommendations | http://www.sitime.com/support/application-notes |

## Revision History

### Table 17. Datasheet Version and Change Log

| Version | Release Date | Change Summary |
|---|---|---|
| 0.9 | 1/24/2013 | Preliminary |
| 0.95 | 11/28/13 | • Added supported frequency table<br>• Added ±20 ppm option<br>• Added No Connect (NC) option for pin 1<br>• Updated thermal consideration table<br>• Added Maximum Operating Junction Temperature table<br>• Added timing diagram, test circuits and waveform diagrams<br>• Added performance plots<br>• Added programmable drive strength options<br>• Added pin 1 option section (OE vs NC)<br>• Updated order info section<br>• Added revision history<br>• Added LifeTime Warranty icon in the feature section |
| 0.96 | 1/24/14 | • Added ±30 ppm<br>• Additional corrections in spelling and grammar. |
| 0.97 | 1/28/14 | • Added support for -55°C to 125°C |
| 1.0 | 5/28/15 | • Final production release<br>• Revised Timing Diagrams<br>• Fixed error link<br>• Revised 2016 package diagram |
| 1.01 | 6/18/15 | • Added 16 mm T&R information to Table 15<br>• Revised 12 mm T&R information to Table 15 |

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# Supplemental Information

The Supplemental Information section is not part of the datasheet and is for informational purposes only.



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# Silicon MEMS Outperforms Quartz


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# Silicon MEMS Outperforms Quartz

The Smart Timing Choice™

## Best Reliability

Silicon is inherently more reliable than quartz. Unlike quartz suppliers, SiTime has in-house MEMS and analog CMOS expertise, which allows SiTime to develop the most reliable products. Figure 1 shows a comparison with quartz technology.

**Why is SiTime Best in Class:**

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal™ process, which eliminates foreign particles and improves long term aging and reliability
- World-class MEMS and CMOS design expertise

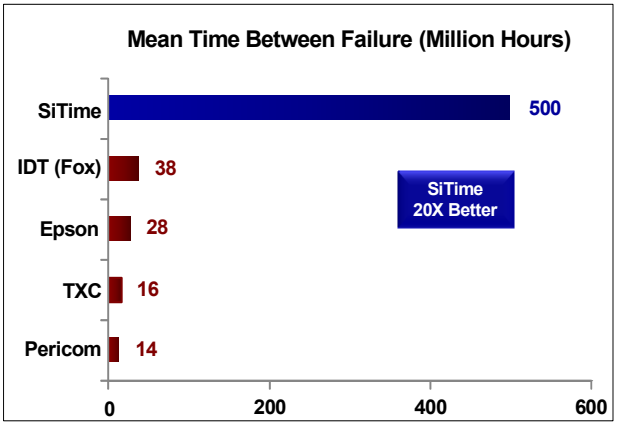



**Figure 1. Reliability Comparison[1]**

## Best Aging

Unlike quartz, MEMS oscillators have excellent long term aging performance which is why every new SiTime product specifies 10-year aging. A comparison is shown in Figure 2.

**Why is SiTime Best in Class:**

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal process, which eliminates foreign particles and improves long term aging and reliability
- Inherently better immunity of electrostatically driven MEMS resonator

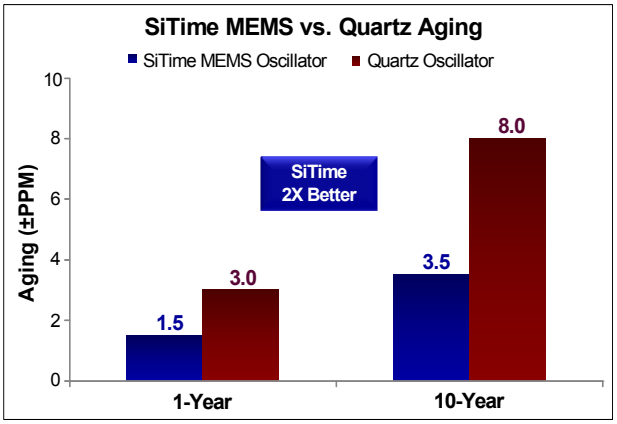



**Figure 2. Aging Comparison[2]**

## Best Electro Magnetic Susceptibility (EMS)

SiTime's oscillators in plastic packages are up to 54 times more immune to external electromagnetic fields than quartz oscillators as shown in Figure 3.

**Why is SiTime Best in Class:**

- Internal differential architecture for best common mode noise rejection
- Electrostatically driven MEMS resonator is more immune to EMS

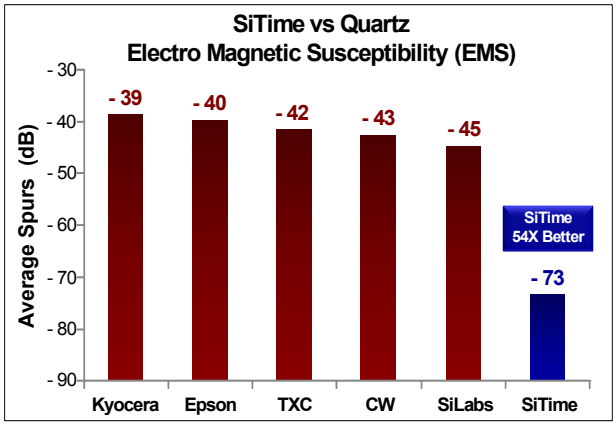



**Figure 3. Electro Magnetic Susceptibility (EMS)[3]**

## Best Power Supply Noise Rejection

SiTime's MEMS oscillators are more resilient against noise on the power supply. A comparison is shown in Figure 4.

**Why is SiTime Best in Class:**

- On-chip regulators and internal differential architecture for common mode noise rejection
- Best analog CMOS design expertise

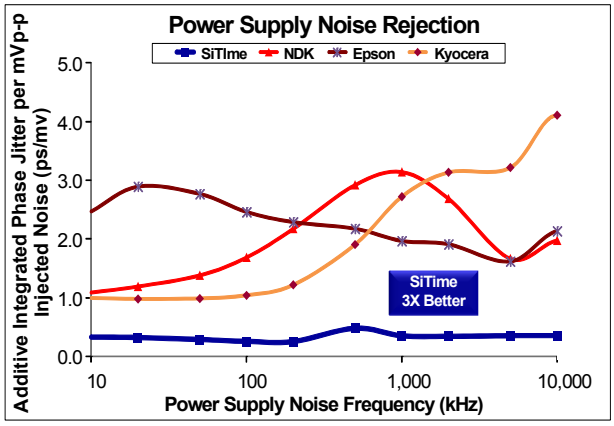



**Figure 4. Power Supply Noise Rejection[4]**



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# Silicon MEMS Outperforms Quartz

## Best Vibration Robustness

High-vibration environments are all around us. All electronics, from handheld devices to enterprise servers and storage systems are subject to vibration. Figure 5 shows a comparison of vibration robustness.

**Why is SiTime Best in Class:**

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

## Best Shock Robustness

SiTime's oscillators can withstand at least 50,000 *g* shock. They all maintain their electrical performance in operation during shock events. A comparison with quartz devices is shown in Figure 6.

**Why is SiTime Best in Class:**

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

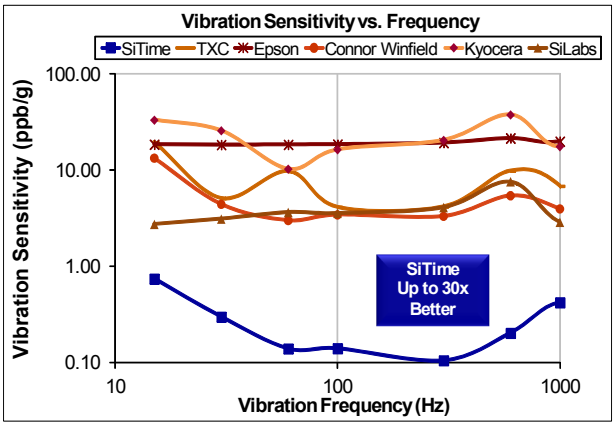



**Figure 5. Vibration Robustness[5]**

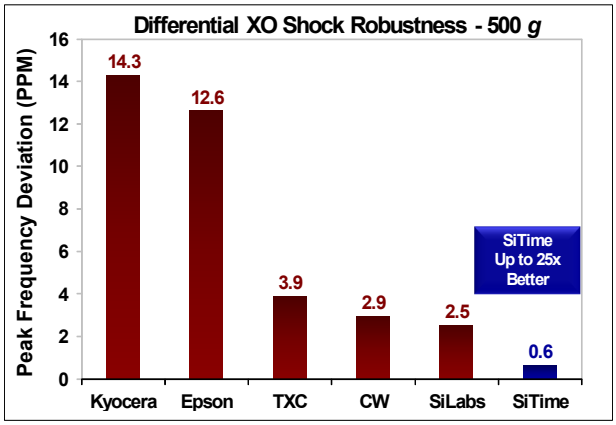



**Figure 6. Shock Robustness[6]**

**Notes:**

1. Data Source: Reliability documents of named companies.
2. Data source: SiTime and quartz oscillator devices datasheets.
3. Test conditions for Electro Magnetic Susceptibility (EMS):
   - According to IEC EN61000-4.3 (Electromagnetic compatibility standard)
   - Field strength: 3V/m
   - Radiated signal modulation: AM 1 kHz at 80% depth
   - Carrier frequency scan: 80 MHz – 1 GHz in 1% steps
   - Antenna polarization: Vertical
   - DUT position: Center aligned to antenna

   **Devices used in this test:**
   SiTime, SiT9120AC-1D2-33E156.250000 - MEMS based - 156.25 MHz
   Epson, EG-2102CA 156.2500M-PHPAL3 - SAW based - 156.25 MHz
   TXC, BB-156.250MBE-T - 3rd Overtone quartz based - 156.25 MHz
   Kyocera, KC7050T156.250P30E00 - SAW based - 156.25 MHz
   Connor Winfield (CW), P123-156.25M - 3rd overtone quartz based - 156.25 MHz
   SiLabs, Si590AB-BDG - 3rd overtone quartz based - 156.25 MHz
4. 50 mV pk-pk Sinusoidal voltage.
   **Devices used in this test:**
   SiTime, SiT8208AI-33-33E-25.000000, MEMS based - 25 MHz
   NDK, NZ2523SB-25.6M - quartz based - 25.6 MHz
   Kyocera, KC2016B25M0C1GE00 - quartz based - 25 MHz
   Epson, SG-310SCF-25M0-MB3 - quartz based - 25 MHz
5. **Devices used in this test:** same as EMS test stated in Note 3.
6. Test conditions for shock test:
   - MIL-STD-883F Method 2002
   - Condition A: half sine wave shock pulse, 500-g, 1ms
   - Continuous frequency measurement in 100 µs gate time for 10 seconds

   **Devices used in this test:** same as EMS test stated in Note 3
7. Additional data, including setup and detailed results, is available upon request to qualified customers. Please contact productsupport@sitime.com.



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