eMMC Product Family（Industrial）

eMMC5.1 Specification Compatibility

SGM8000I-S21BAG

SGM8000I-S21BBG

SGM8000I-S21DCG

Datasheet

V1.1

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Revision History

Revision No.	Date	History	Remark
0.1	2021-09-02	Initial Issue	Draft
1.0	2022-01-12	Customer version for 16GB Product	Final
1.1	2022-03-15	Added 32GB/64GB Product	Final

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1 Introduction

1.1 General Description

SiliconGo e•MMC is an embedded storage solution designed in a BGA package form. The operation of e•MMC is a simple read and write to memory using e•MMC protocol v5.1 which is an industry standard.

The e•MMC consists of NAND flash and a MMC controller. 3.3V supply voltage is required for the NAND area (V_{CC}), whereas 1.8V or 3.3V dual supply voltage (V_{CC} or V_{CCQ}) is supported for MMC controller.

There are several advantages of e•MMC. It is easy to be used on the standard interface, which allows the easy and widely used integration with general CPU. Any revision or amendment of NAND is invisible to the host as the embedded e•MMC controller insulates NAND technology from the host. It means that the host can support the newest processing flash without updating its hardware or software.

SiliconGo e•MMC has high performance at a competitive-cost, high quality and low power consumption. e•MMC provides capacities from 16GB to 64GB.

1.2 Product List

Capacity	Part Number	NAND Flash Type	Package Size	Package Type
16 GB	SGM8000I-S21BAG	128Gb x1	11.5x13.0x1.0 (mm)	153 FBGA
32 GB	SGM8000I-S21BBG	128Gb x 2	11.5x13.0x1.0 (mm)	153 FBGA
64 GB	SGM8000I-S21DCG	128Gb x 4	11.5x13.0x1.2 (mm)	153 FBGA

1.3 Key Feature

- **e•MMC v5.1 compatible. Detail description is referenced by JEDEC Standard**
  - (Backward compatible to e•MMC v4.41/v4.5/v5.0)
- **Bus mode**
  - Data bus width: 1bit(default), 4bit and 8bit
  - Data transfer rate: up to 400MB/s (HS400) @ 200MHz DDR with 8bit bus width
  - MMC I/F Clock Frequency: 0~200MHz
  - MMC I/F Boot Frequency: 0~52MHz
- **Operating Voltage Range**
  - V_{CC} (NAND/Core): 2.7V ~ 3.6V
  - V_{CCQ} (CTRL/IO): 1.7V ~ 1.95V / 2.7V ~ 3.6V
- **Temperature**
  - Operation (-40℃ ~ 85℃)
  - Storage without operation (-40℃ ~ 85℃)

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- **Supports Features**
  - HS400, HS200, DDR52, SDR52
  - High Priority Interrupt (HPI)
  - Background Operation, **BKOPS Control**
  - Packed CMD, **Command Queuing**
  - Cache, **Cache Flushing Report, Cache Barrier** (Optional)
  - Partitioning, Partition types, RPMB, **RPMB Throughput Improve**
  - Discard, Trim, Erase, Sanitize
  - Write Protect, **Secure Write Protection** (Optional)
  - Lock/Unlock
  - Power Off Notification(PON), Sleep/Awake
  - Enhance Reliable Write
  - Boot feature, Boot partition
  - Context IDs, Data Tag, Real Time Clock
  - HW/SW Reset
  - Configurable driver strength
  - Field Firmware Update
  - Secure Removal Type (Optional)
  - Device Health Report (Optional)
  - Production State Awareness (Optional)
  - Data Strobe pin, **Enhanced Strobe** (Optional)

  (Bold features are added in eMMC5.1)

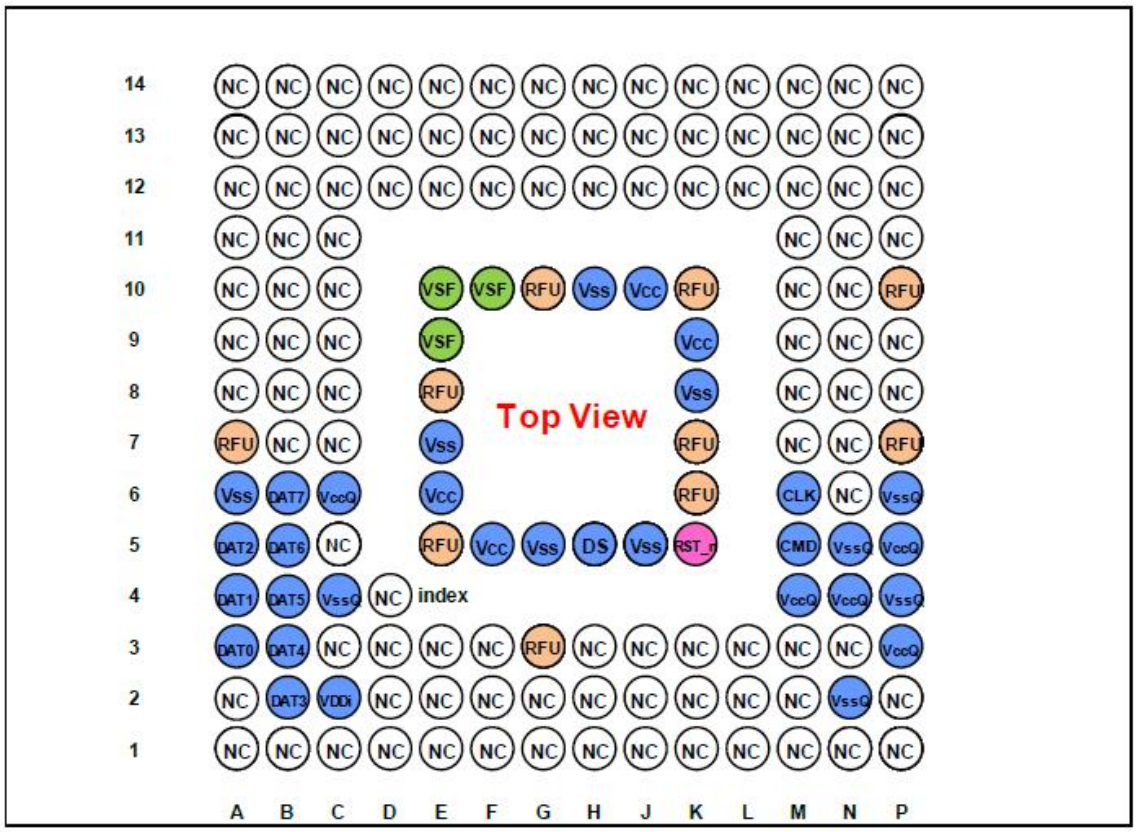
- **Others**
  - This product is compliance with the RoHS directive.

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2 Package Configurations

2.1 153-FBGA Ball Array View



Ball Side down View

Ball No.	Name	Ball No.	Name	Ball No.	Name	Ball No.	Name
A3	DAT0	C2	VDDi	J5	V_{SS}	N4	V_{CCQ}
A4	DAT1	C4	V_{SSQ}	J10	V_{CC}	N5	V_{SSQ}
A5	DAT2	C6	V_{CCQ}	K5	RST_n	P3	V_{CCQ}
A6	V_{SS}	E6	V_{CC}	K8	V_{SS}	P4	V_{SSQ}
B2	DAT3	E7	V_{SS}	K9	V_{CC}	P5	V_{CCQ}
B3	DAT4	F5	V_{CC}	M4	V_{CCQ}	P6	V_{SSQ}
B4	DAT5	G5	V_{SS}	M5	CMD	--	--
B5	DAT6	H5	DS	M6	CLK	--	--
B6	DAT7	H10	V_{SS}	N2	V_{SSQ}	--	--

Note：

NC: No Connect, can be connected to ground or left floating.

RFU: Reserved for Future Use, should be left floating for future use.

VSF: Vendor Specific Function, shall be left floating.

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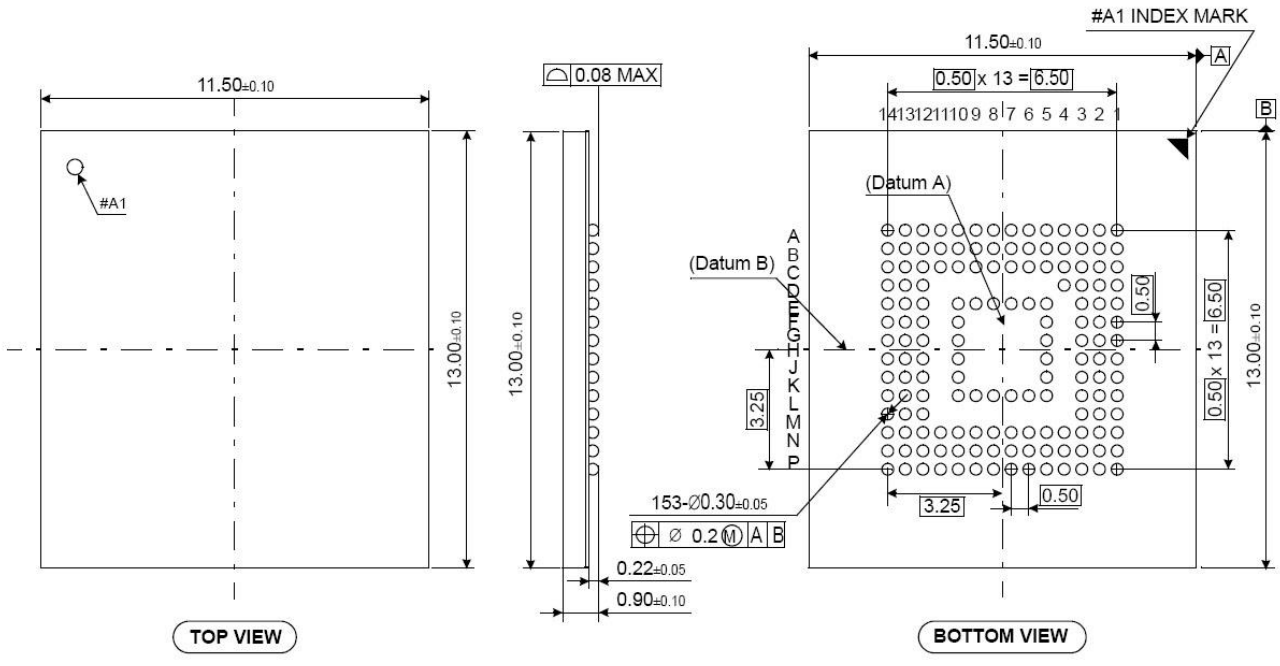
2.2 Ball Assignment

Signal	Ball No.	Description
CLOCK (CLK)	M6	Each cycle of the clock directs a transfer on the command line and on the data lines.
COMMAND (CMD)	M5	This signal is a bidirectional command channel used for device initialization and command transfer. The CMD Signal has 2 operation modes: open drain for initialization, and push-pull for fast command transfer.
DATA (DAT0-DAT7)	A3~A5 B2~B6	These are bidirectional data channels. The DAT signals operate in push-pull mode.
RST_n	K5	Hardware Reset Input
DS	H5	Data Strobe: Return Clock signal used in HS400 mode
V_{CCQ}	C6,M4,N4,P3,P5	Power supply for MMC interface and Controller, have two power mode: High power mode:2.7V~3.6V; Lower power mode:1.7V~1.95V
V_{CC}	E6,F5,J10,K9	Power supply for NAND flash memory, its power voltage range is: 2.7V~3.6V
VDDi	C2	VDDi is internal power mode. Connect 0.1uF or 2.2uF capacitor from VDDi to ground
V_{SS},V_{SSQ}	A6, E7, G5, H10, J5, K8, C4, N2, N5, P4, P6	Ground lines

Note： All other pins are not connected [NC] and can be connected to GND or left floating.

2.3 Package Dimensions

For 16GB/32GB

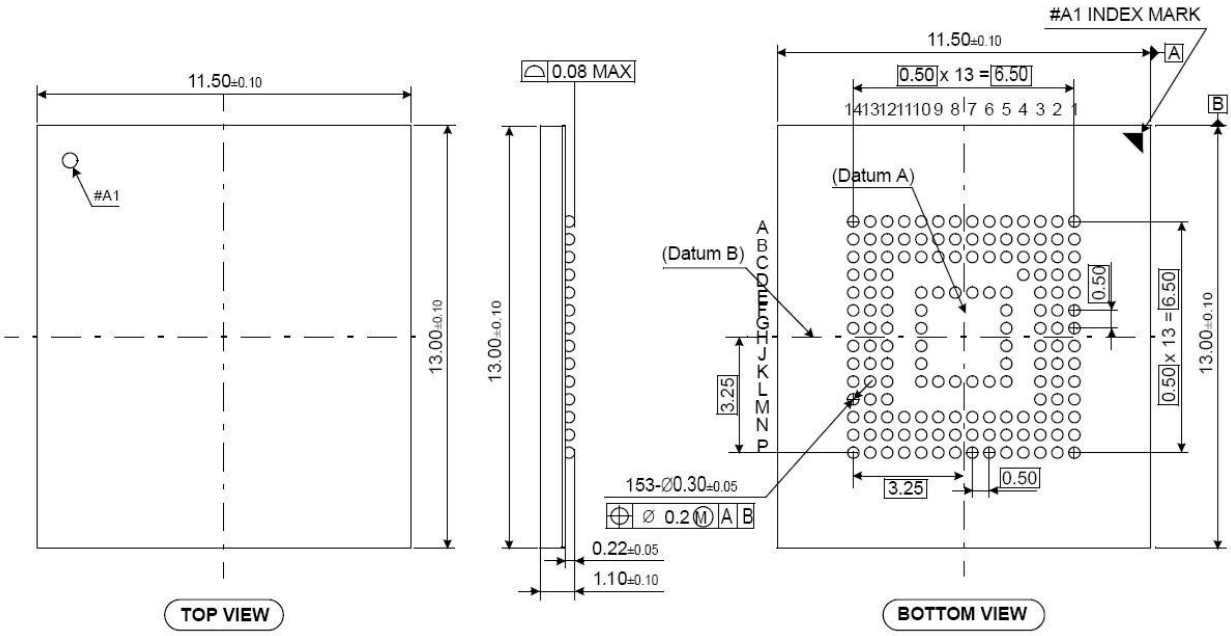


Unit: mm

11.5mm×13mm×1.0mm Package Dimensions

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For 64GB

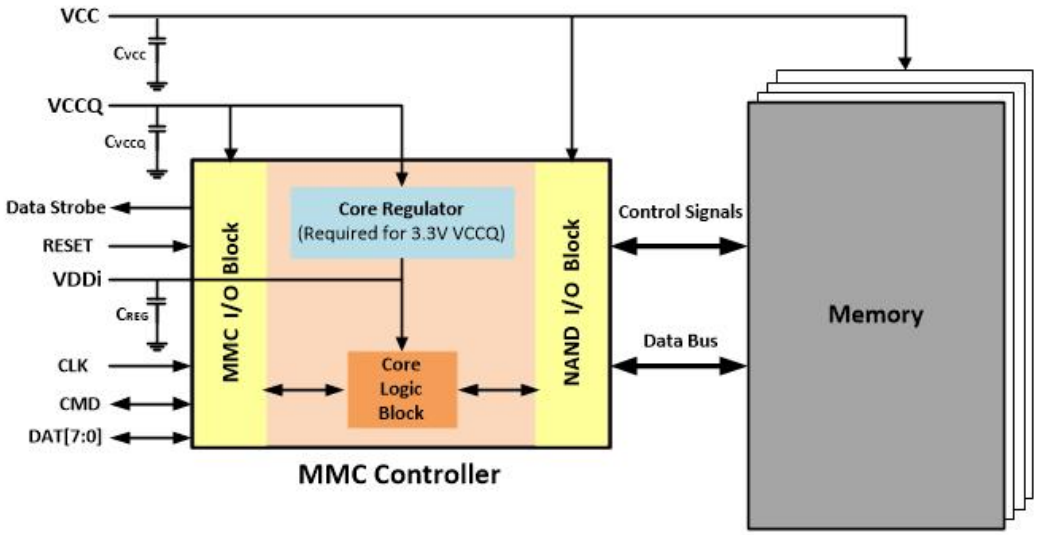


Unit: mm

11.5mm×13mm×1.2mm Package Dimensions

2.4 Product Architecture

e•MMC consists of NAND Flash and Controller. V_{CCQ} is for Controller power and V_{CC} is for flash power.



Parameter	Symbol	Unit	Min.	Typ.	Max.
VDDi capacitor value	C_{REG}	uF	0.1	1.0+0.1	2.2
VCC capacitor value	C_{VCC}	uF	-	2.2+0.1	-
VCCQ capacitor value	C_{VCCQ}	uF	-	2.2+0.1	-

Note：

e•MMC recommends that the minimum value should be usually applied as the value of C_{REG}; C_{REG} shall be compliant with X5R/X7R of EIA standard or B of JIS standard.

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3 e•MMC Features

3.1 HS400 mode

■ **The HS400 mode has the following features**

- DDR Data sampling method
- CLK frequency up to 200 MHz DDR – up to 400 MB/s
- Only 8-bits bus width supported
- Signaling levels of 1.8 V
- Support up to 5 Drive Strengths
- Data strobe signal is toggled only for Data out, CRC response and CMD Response

■ **I/O driver strength types**

Driver Type Values	Support	Nominal Impedance	Approximated driving capability compared to Type-0	Remark
0x0	Mandatory	50 Ω	x1	Default Driver Type. Supports up to 200 MHz operation
0x1	Optional	33 Ω	x1.5	Supports up to 200 MHz operation.
0x2	Optional	66 Ω	x0.75	The weakest driver that supports up to 200 MHz operation.
0x3	Optional	100 Ω	x0.5	For low noise and low EMI systems. Maximal operating frequency is decided by Host design
0x4	Optional	40 Ω	x1.2	

Note： Support of Driver Type-0 is mandatory for HS200 and HS400 device.

■ **Device type values (EXT_CSD Register: DEVICE_TYPE [196])**

Bit	Device Type	Supportability
7	HS400 Dual Data Rate e•MMC @ 200 MHz - 1.2V I/O	Not support
6	HS400 Dual Data Rate e•MMC @ 200 MHz - 1.8V I/O	Support
5	HS200 Single Data Rate e•MMC @ 200 MHz - 1.2V I/O	Not support
4	HS200 Single Data Rate e•MMC @ 200 MHz - 1.8V I/O	Support
3	High-Speed Dual Data Rate e•MMC @ 52MHz - 1.2V I/O	Not support
2	High-Speed Dual Data Rate e•MMC @ 52MHz - 1.8V or 3V I/O	Support
1	High-Speed e•MMC @ 52MHz - at rated device voltage(s)	Support
0	High-Speed e•MMC @ 26MHz - at rated device voltage(s)	Support

Note： It is being discussed in JEDEC and is not confirmed yet. It can be modified according to JEDEC standard in the future.

■ **Extended CSD revisions (EXT_CSD Register: EXT_CSD_REV [192])**

Value	Timing Interface	EXT_CSD Register Value
255–9	Reserved	-
8	Revision 1.8 (for MMC v5.1)	0x08
7	Revision 1.7 (for MMC V5.0)	-
6	Revision 1.6 (for MMC V4.5, V4.51)	-
5	Revision 1.5 (for MMC V4.41)	-
4	Revision 1.4 (Obsolete)	-

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3	Revision 1.3 (for MMC V4.3)	-
2	Revision 1.2 (for MMC V4.2)	-
1	Revision 1.1 (for MMC V4.1)	-
0	Revision 1.0 (for MMC V4.0)	-

Note： Current e•MMC standard defined by JEDEC supports up to 0x08 for EXT_CSD_REV value.

■ **High Speed timing values (EXT_CSD Register: HS_TIMING [185])**

Value	Timing Interface	Supportability
0x0	Selecting backwards compatibility interface timing	Support
0x1	High Speed	Support
0x2	HS200	Support
0x3	HS400	Support

4 e•MMC 5.1 Features

4.1 Overview

New Feature	JEDEC	Support
Cache Flushing Report	Mandatory	Yes
Background operation control	Mandatory	Yes
Command Queuing	Optional	Yes
Enhanced Strobe	Optional	Yes
RPMB Throughput improve	Optional	Yes

4.2 Command Queuing

To facilitate command queuing in eMMC, the device manages an internal task queue that the host can queue during data transfer tasks.
Every task is issued by the host and initially queued as pending. The device works to prepare pending tasks for execution. When a task is ready for execution, its state changes to “ready for execution”.
The host tracks the state of all queued tasks and may order the execution of any task, marked as “ready for execution”, by sending a command indicating its task ID. The device executes the data transfer transaction after receiving the execute command (CMD46/CMD47).

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4.2.1 CMD Set Description

■ CMD Set Description and Details

CMD	Type	Argument	Abbreviation	Purpose
CMD44	ac/R1	[31] Reliable Write Request [30] DAT_DIR - "0" write / "1" read [29] tag request [28:25] context ID [24] forced programming [23] Priority: “0” simple / “1” high [20:16] TASK ID [15:0] number of blocks	QUEUED_TASK _PARAMS	Define direction of operation (Read or Write) and Set high priority CMD Queue with task ID
CMD45	ac/R1	[31:0] Start block address	QUEUED_TASK_ADDRESS	Indicate data address for Queued CMD
CMD46	adtc/R1	[20:16] TASK ID	EXECUTE_READ_TASK	(Read) Transmit the requested number of data blocks
CMD47	adtc/R1	[20:16] TASK ID	EXECUTE_WRITE_TASK	(Write) Transmit the requested number of data blocks
CMD48	ac/R1b	[20:16] Task ID [3:0] TM op-code	CMDQ_TASK _MGMT	Reset a specific task or entire queue. [20:16] when TM op-code = 2h these bits represent TaskID. When TM op-code = 1h these bits are reserved."

4.2.2 New Response: QSR (Queue Status Register)

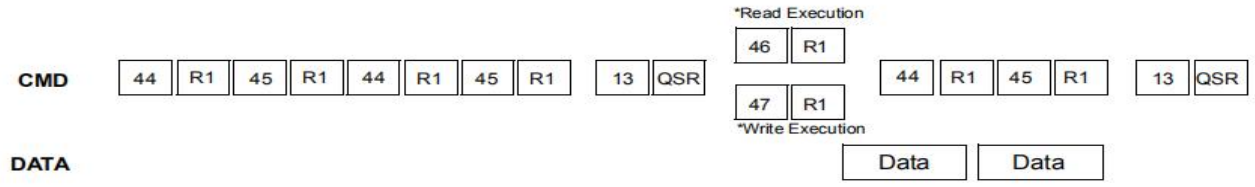
The 32-bit Queue Status Register (QSR) carries the state of tasks in the queue at a specific point in time. The host has read access to this register through device response to SEND_STATUS command (CMD13 with bit[15]=”1”), R1’s argument will be the 32- bit Queue Status Register (QSR). Every bit in the QSR represents the task who’s ID corresponds to the bit index. If bit QSR[i] = “0”, then the queued task with a Task ID i is not ready for execution. The task may be queued and pending, or the Task ID is unused. If bit QSR[i] = “1”, then the queued task with Task ID i is ready for execution.

4.2.3 Send Status: CMD13

CMD13 for reading the Queue Status Register (QSR) by the host. If bit[15] in CMD13’s argument is set to 1, then the device shall send an R1 Response with the QSR instead of the Device Status. * There is still legacy CMD13 with R` response.

4.2.4 Mechanism of CMD Queue operation

Host issues CMD44 with Task ID number, Sector, Count, Direction, Priority to the device followed by CMD45 and host checks the Queue Status check with CMD13 [15]bits to 1 . After that host issues CMD46 for Read or CMD47 for write During CMD queue operation, CMD44/CMD45 is able to be issued at anytime when the CMD line is not in use



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4.2.5 CMD Queue Register description

Configuration and capability structures shall be added to the EXT_CSD register, as described below

■ CMD Queuing Support (EXT_CSD register : CMDQ_SUPPORT [308])

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							CMD Queue supportability

This field indicates whether the device supports command queuing or not

0x0: CMD Queue function is not supported
0x1: CMD Queue function is supported

■ Command Queue Mode Enable(EXT_CSD register : CMDQ_MODE_EN [15])

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							CMD Queue supportability

This field is used by the host enable command queuing

0x0: Queue function is not enabled
0x1: Queue function is enabled

■ CMD Queuing Depth(EXT_CSD register : CMDQ_DEPTH [307])

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved							CMD Queue supportability

This field is used to calculate the depth of the queue supported by the device

Bit encoding:
[7:5]: Reserved
[4:0]: N,a parameter used to calculate the Queue Depth of task queue in the device.
Queue Depth = N+1.

4.3 Enhanced Strobe Mode

This product supports Enhanced Strobe in HS400 mode and refer to the details as described in eMMC5.1 JEDEC standard.

4.4 RPMB Throughput improve

[Table 11] Related parameter register in EXT_CSD : WR_REL_PARAM [166]

Name	Field	Bit	Type
Enhanced RPMB Reliable Write	EN_RPMB_REL_WR	4	R

Bit[4]: EN_RPMB_REL_WR(R)
0x0: RPMB transfer size is either 256B (single 512B frame) or 512B (Two 512B frame).
0x1: RPMB transfer size is either 256B (single 512B frame), 512B (Two 512B frame), or 8KB(Thirthy two 512B frames).

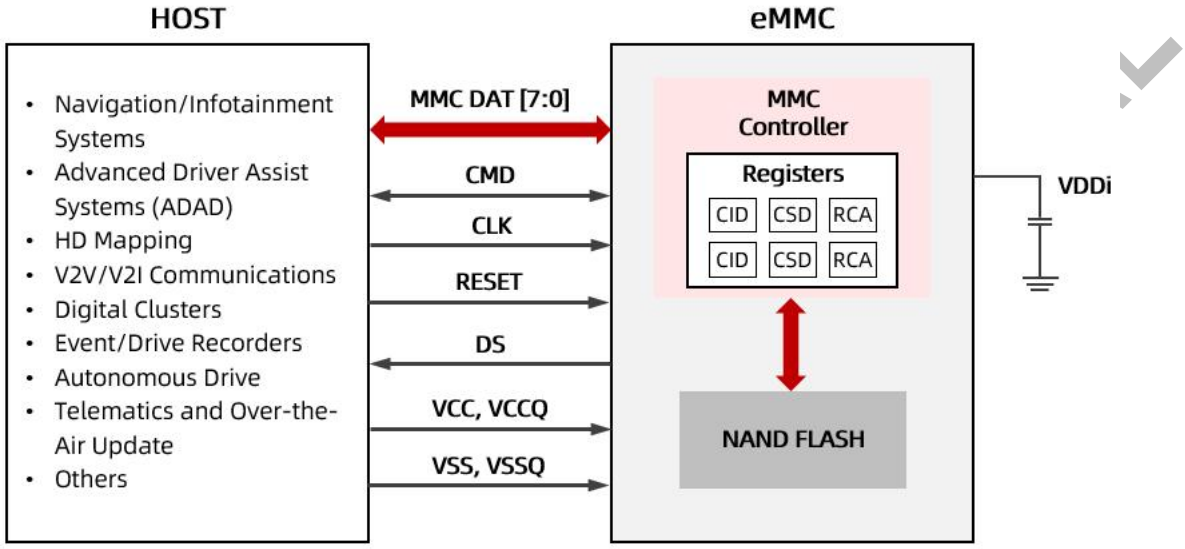
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5 Usage Overview

5.1 General Description

The e•MMC can be operated in 1, 4, or 8-bit mode. NAND flash memory is managed by a controller inside, which manages ECC, wear leveling and bad block management. e•MMC provides easy integration with the host process that all flash management hassles are invisible to the host.



5.2 Partition Management

The memory configuration initially consists (before any partitioning operation) of the User Data Area and RPMB Area Partitions and two Boot Area Partitions.

The embedded device also offers the host the possibility to configure additional local memory partitions with independent address spaces, starting from logical address 0x00000000, for different usage models.

Therefore, the memory block areas can be classified as follows:

- Two Boot Area Partitions, whose size is multiple of 128 KB and where booting from e•MMC can be performed.
- One RPMB Partition accessed through a trusted mechanism, whose size is defined as multiple of 128 KB.
- Four General Purpose Area Partitions to store sensitive data or for other host usage models, whose sizes are a multiple of a Write Protect Group.

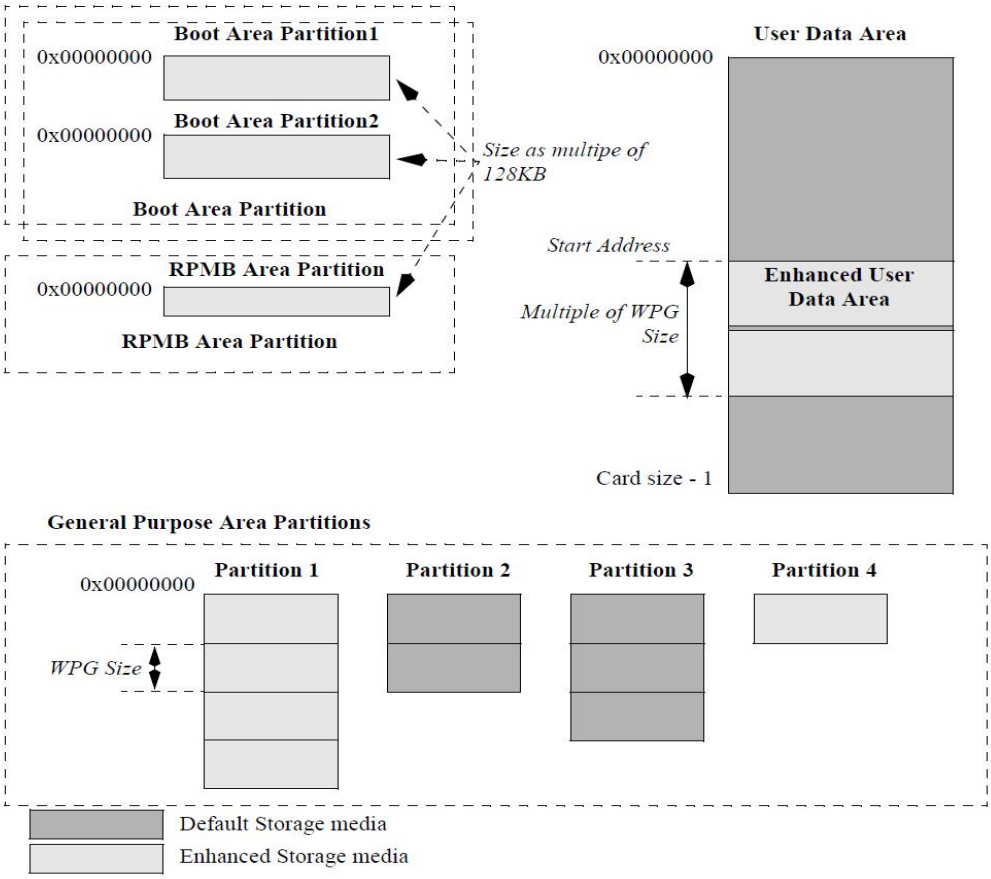
Boot and RPMB Area Partitions' sizes and attributes are defined by the memory manufacturer (read-only), while General Purpose Area Partitions' sizes and attributes can be programmed by the host only once in the device life-cycle (one-time programmable).

Moreover, the host is free to configure one segment in the User Data Area to be implemented as enhanced storage media, and to specify its starting location and size in terms of Write Protect Groups. The attributes of this Enhanced User Data Area can be programmed only once during the device life-cycle (one-time programmable).

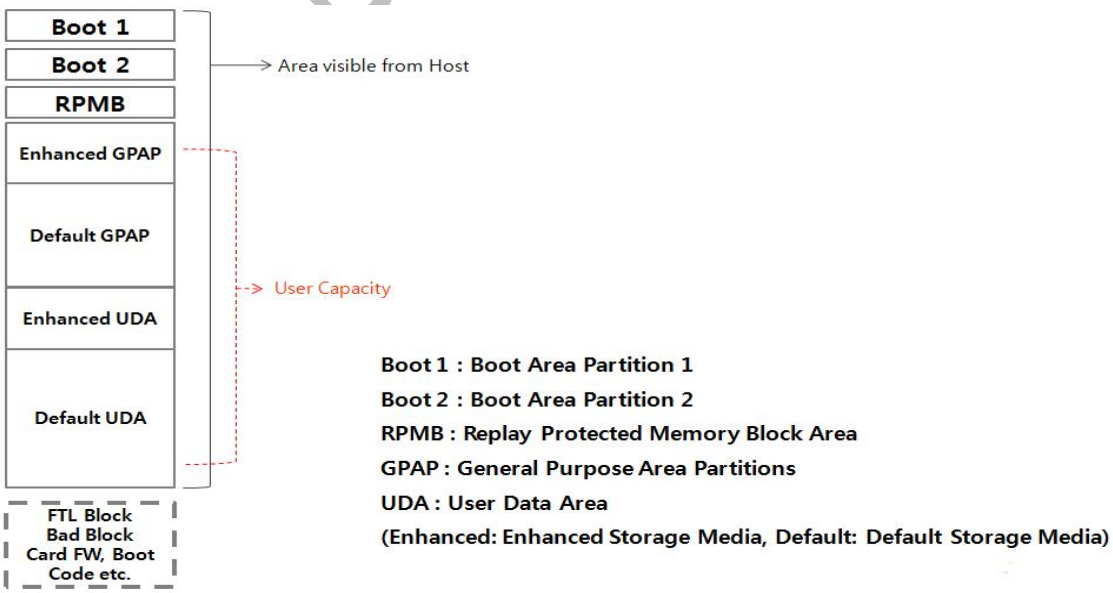
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A possible final configuration can be the following:



5.3 User Density



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■ **Boot and RPMB Size**

	Boot1 Size	Boot2 Size	RPMB Size
Default	4096 KB	4096 KB	4096 KB
Max.	4096 KB	4096 KB	4096 KB

■ **User Density Size**

Capacity	User Area Capacity	SEC_COUNT in Extended CSD
16 GB	15,634,268,160 Bytes (14910 MB)	0x1D1F000
32 GB	31,268,536,320 Bytes (29820 MB)	0x3A3E000
64 GB	62,537,072,640 Bytes (59,640 MB)	0x747C000

5.4 Performance

Capacity	Part Number	Mode	Sequential Read (MB/s)	Sustained Sequential Write (MB/s)
16 GB	SGM8000I-S21BAG	HS400	280	50
32 GB	SGM8000I-S21BBG	HS400	280	55
64 GB	SGM8000I-S21DCG	HS400	280	60

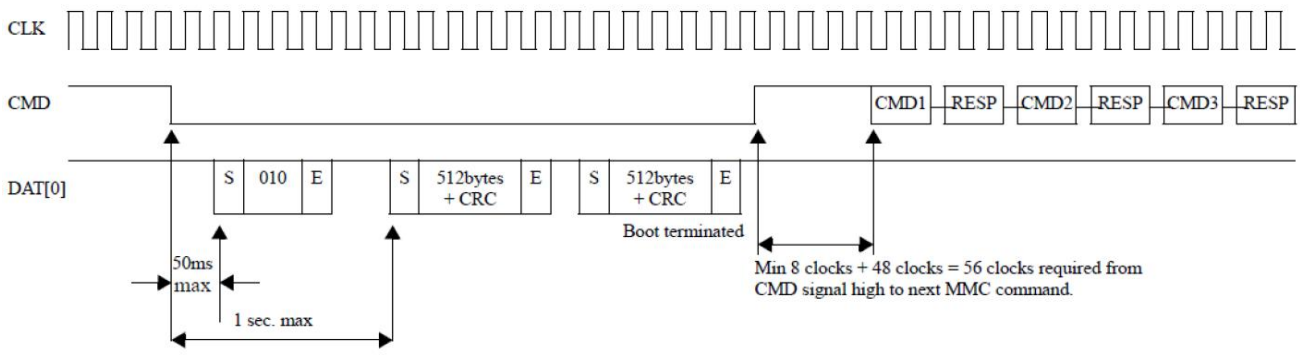
Test Condition: Bus width x8, 200MHz DDR, 512KB data transfer, w/o file system overhead, measured on internal board.

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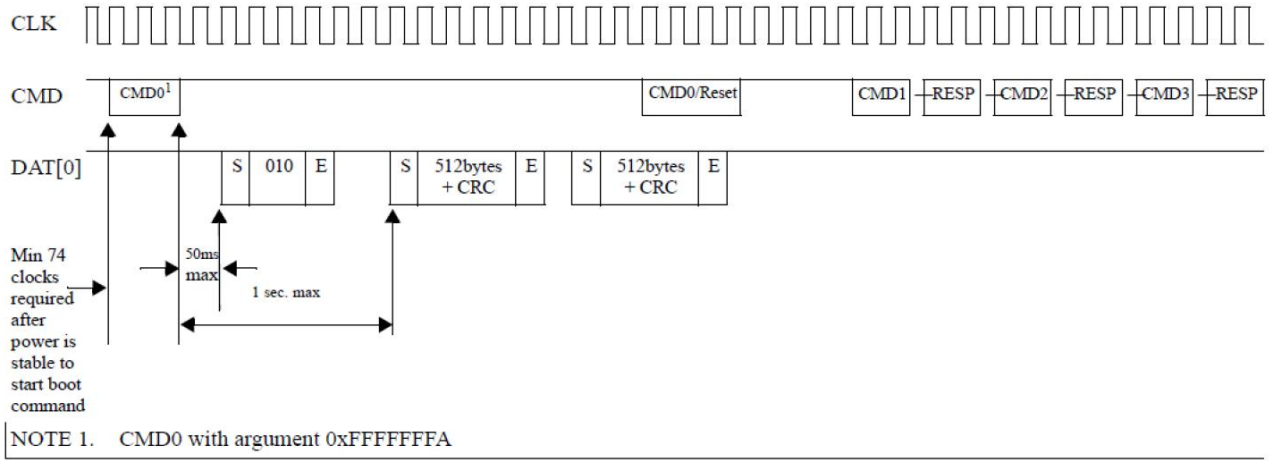
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5.5 Boot Operation Mode

In boot operation mode, the master can read boot data from the slave (device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting.



State diagram (boot mode)
Boot operation complete Clock = 400 kHz
(Compatible with the description which ≤400kHz)



State diagram (alternative boot mode)

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6 Device Register

6.1 OCR Register

The 32-bit operation conditions register (OCR) stores the V_{DD} voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

OCR bit	V_{CCQ} voltage window	e•MMC
[6:0]	Reserved	000 0000b
[7]	1.7–1.95	1b
[14:8]	2.0–2.6	000 0000b
[23:15]	2.7–3.6	1 1111 1111b
[28:24]	Reserved	000 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)
[31]	Card power up status bit (busy)*	

Note*： This bit is set to LOW if the e•MMC has not finished the power up routine. The supported voltage range is coded as shown in table.

6.2 CID Register

The Device IDentification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (e•MMC protocol). Every individual flash or I/O Device shall have a unique identification number. Every type of e•MMC Device shall have a unique identification number. Table 75 lists these identifiers. The structure of the CID register is defined in this section.

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0xEA
Reserved	-	6	[119:114]	0x0
Card/BGA	CBX	2	[113:112]	0x1
OEM/Application ID	OID	8	[111:104]	0x0E
Product name	PNM	48	[103:56]	0x53 50 65 4D 4D 43 (SPeMMC)
Product revision	PRV	8	[55:48]	0x10
Product serial number	PSN	32	[47:16]	Serial number
Manufacturing date	MDT	8	[15:8]	Manufacturing date
CRC7 checksum	CRC	7	[7:1]	CRC7
Not used, always ‘1’	-	1	[0:0]	0x1

6.3 CSD Register

The Card-Specific Data register provides information on how to access the e•MMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:

R: Read only

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W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Name	Field	Width	Cell Type	CSD-slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x3
System specification version	SPEC_VERS	4	R	[125:122]	0x4
Reserved	-	2	R	[121:120]	0x0
Data read access-time 1	TAAC	8	R	[119:112]	0x4F
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x1
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Card command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x9
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x0
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x0
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x0
DSR implemented	DSR_IMP	1	R	[76:76]	0x0
Reserved	-	2	R	[75:74]	0x0
Device size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x6
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x6
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x6
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x6
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x7
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0xF
Write protect group enable	WP_GRP_MULT	1	R	[31:31]	0x1
Manufacturer default	ECC DEFAULT_ECC	2	R	[30:29]	0x0
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x5
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x9
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x0
Reserved	-	4	R	[20:17]	0x0
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x0
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x0
Copy flag(OTP)	COPY	1	R/W	[14:14]	0x0
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x0
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x0
File format	FILE_FORMAT	2	R/W	[11:10]	0x0
ECC code	ECC	2	R/W/E	[9:8]	0x0
CRC	CRC	7	R/W/E	[7:1]	0x0
Not used, always '1'	-	1	-	[0:0]	0x1

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6.4 Extended CSD Register

The Extended CSD register defines the e•MMC properties and selected modes. It is 512 bytes long.

The most significant 320 bytes are the Properties segment, which defines the e•MMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the e•MMC is working in. These modes can be changed by the host by means of the SWITCH command.

R: Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Properties Segment					
Reserved	-	6	TBD	[511:506]	All ”0”
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x0
Supported Command Sets	S_CMD_SET	1	R	[504]	0x1
HPI features	HPI_FEATURES	1	R	[503]	0x1
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x1
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x38
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x38
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x1
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x5
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0x1
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x5
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x1
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x3
Supported modes	SUPPORTED_MODES	1	R	[493]	0x1
FFU features	FFU_FEATURES	1	R	[492]	0x1
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0xD
FFU Argument	FFU_ARG	4	R	[490:487]	0x0
Barrier support	BARRIER_SUPPORT	1	R	[486]	0x1
Reserved	-	177	TBD	[485:309]	All ”0”
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	0x1
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	0x1F
Reserved	-	1	TBD	[306]	0x0
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0x0
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	All “0”
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x1
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x1

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Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x1
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x40
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x40
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x7
Device version	DEVICE_VERSION	2	R	[263:262]	0x0
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	FW version
Power class for 200MHz, DDR at V_{CC}= 3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x0
Cache size	CACHE_SIZE	4	R	[252:249]	0x300
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x40
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x64
Background operations status	BKOPS_STATUS	1	R	[246]	0x0
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x0
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0xA
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0x1
Power class for 52MHz, DDR at V_{CC} = 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x0
Power class for 52MHz, DDR at V_{CC} = 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x0
Power class for 200MHz at V_{CCQ} =1.95V, V_{CC} = 3.6V	PWR_CL_200_195	1	R	[237]	0x0
Power class for 200MHz, at V_{CCQ}=1.3V, V_{CC} = 3.6V	PWR_CL_200_130	1	R	[236]	0x0
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x0
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x0
Reserved		1	TBD	[233]	0x0
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x2
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1Bh
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11
Boot information	BOOT_INFO	1	R	[228]	0x7
Reserved		1	TBD	[227]	0x0
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	0x20
Access size	ACC_SIZE	1	R	[225]	0x6
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x1
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x1
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x1
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10
Sleep current [V_{CC}]	S_C_VCC	1	R	[220]	0xD
Sleep current [V_{CCQ}]	S_C_VCCQ	1	R	[219]	0xD
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0x6
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x17
Sleep Notification Timout1	SLEEP_NOTIFICATION_TIME	1	R	[216]	0xA
Sector Count	SEC_COUNT	4	R	[215:212]	16GB: 0x1D1F000 32GB: 0x3A3E000 64GB: 0x747C000

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Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x0
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x0
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x0
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x0
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x0
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x0
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0x0
Reserved		1	TBD	[204]	0x0
Power class for 26MHz at 3.6 V 1 R	PWR_CL_26_360	1	R	[203]	0x0
Power class for 52MHz at 3.6 V 1 R	PWR_CL_52_360	1	R	[202]	0x0
Power class for 26MHz at 1.95 V 1 R	PWR_CL_26_195	1	R	[201]	0x0
Power class for 52MHz at 1.95 V 1 R	PWR_CL_52_195	1	R	[200]	0x0
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x6
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0xA
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0x1
Device type	DEVICE_TYPE	1	R	[196]	0x57
Reserved		1	TBD	[195]	0x0
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	0x2
Reserved		1	TBD	[193]	0x0
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	0x8
Modes Segment					
Command Set	CMD_SET	1	R/W/E_P	[191]	0x0
Reserved		1	TBD	[190]	0x0
Command set revision	CMD_SET_REV		R	[189]	0x0
Reserved		1	TBD	[188]	0x0
Power class	POWER_CLASS		R/W/E_P	[187]	0x0
Reserved		1	TBD	[186]	0x0
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0x0
Strobe Support	STROBE_SUPPORT	1	R	[184]	0x1
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0x0
Reserved		1	TBD	[182]	0x0
Erased memory range	ERASE_MEM_CONT	1	R	[181]	0x0
Reserved		1	TBD	[180]	0x0
Partition Configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x0
Boot Config protection	BOOT_CONFIG_PROT	1	R/W &R/W/C_P	[178]	0x0
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x0
Reserved		1	TBD	[176]	0x0

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Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0x0
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x0
Boot area write protect register	BOOT_WP	1	R/W &R/W/C_P	[173]	0x0
Reserved		1	TBD	[172]	0x0
User area write protect register	USER_WP	1	R/W,R/W/C_P &R/W/E_P	[171]	0x0
Reserved		1	TBD	[170]	0x0
FW configuration	FW_CONFIG	1	R/W	[169]	0x0
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x14
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x0
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x0
Enable background operations handshake	BKOPS_EN	1	R/W & R/W/E	[163]	0x0
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x0
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x0
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	0x7
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	16GB: 0x747 32GB: 0xE8F 64GB: 0x9B4
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x0
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x0
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x0
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x0
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x0
Reserved		1	TBD	[135]	0x0
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x0
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x0
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x0
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x0
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x0
Reserved		2	TBD	[129:128]	0x0
Vendor Specific Fields	NATIVE_SECTOR_SIZE	1	<vendor specific>	[127:64]	0x0
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x0
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x0
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x0
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x0
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x0

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Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0x0
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x0
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x0
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x0
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x0
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x0
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x0
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x0
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x0
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x0
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x0
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x0
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x0
Reserved		2	TBD	[28:27]	0x0
FFU status	FFU_STATUS	1	R	[26]	0x0
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x0
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	16GB: 0x747C00 32GB: 0XE8F800 64GB: 0x1D1F000
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x3
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x1
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x0
Reserved		15	TBD	[14:0]	0x0

Note：Reserved bits should be read as “0”.

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7 AC Parameter

7.1 Timing Parameter

■ **Timing Parameter：**

Timing Parameter		Max. Value	Unit
Initialization Time (t_{INIT})	Normal	1	s
	After partition setting	3	s
Read Timeout		300	ms
Write Timeout		350	ms
Erase Timeout		600	ms
Force Erase Timeout		3	min
Secure Erase Timeout		8	s
Secure Trim step1 Timeout		5	s
Secure Trim step2 Timeout		3	s
Trim Timeout		300	ms
Partition Switching Timeout (after Init)		60	ms
Power Off Notification (Short) Timeout		100	ms
Power Off Notification (Long) Timeout		600	ms

Note：

- Normal Initialization Time without partition setting
- Initialization Time after partition setting, refer to INI_TIMEOUT_AP in EXT_CSD register
- Be advised Timeout Values specified in Table above are for testing purposes under internal test pattern only and actual timeout situations may vary
- EXCEPTION_EVENT may occur and the actual timeout values may vary due to user environment

7.2 Bus Timing Parameters for DDR52 and HS200 are defined by JEDEC standard

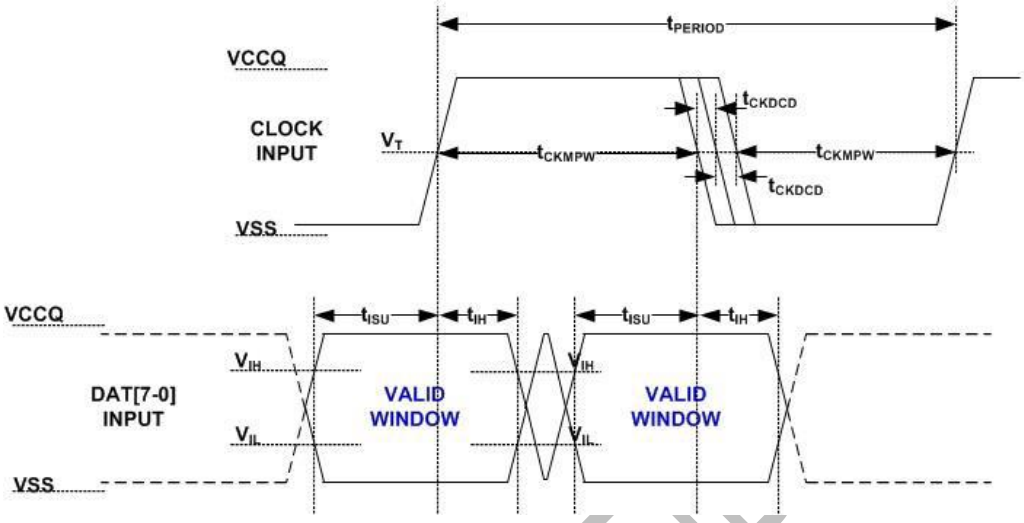
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7.3 Bus Timing Specification in HS400 mode

7.3.1 HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.



NOTE V_T = 50% of V_{CCQ}, indicates clock reference point for timing measurements.

■ **HS400 Device Input Timing**

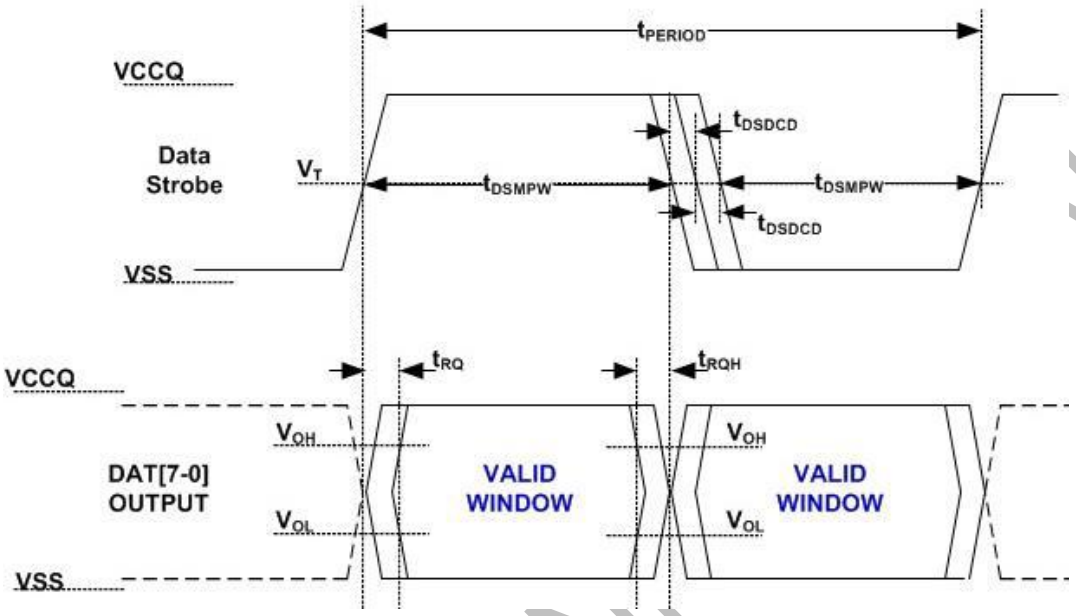
Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5			200 MHz(max), between rising edges With respect to V_T.
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}.
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4		ns	C_{Device} ≤ 6 pF With respect to V_{IH}/V_{IL}.
Input hold time	t_{IHddr}	0.4		ns	C_{Device} ≤ 6 pF With respect to V_{IH}/V_{IL}.
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}.

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7.3.2 HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.



NOTE V_T = 50% of V_{CCQ}, indicates clock reference point for timing measurements.

■ **HS400 Device Output Timing**

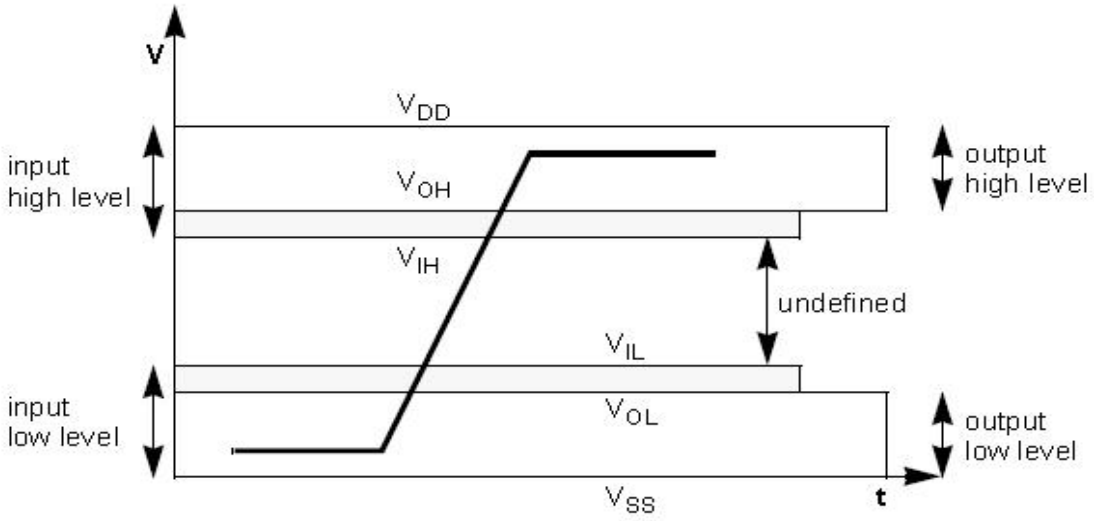
Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5			200 MHz(max), between rising edges With respect to V_T.
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	T_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T.
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid
Output DAT (referenced to Data Strobe)					
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

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7.4 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



7.4.1 Open-Drain Mode Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.2		V	Note
Output LOW voltage	V_{OL}		0.3	V	I_{OL} = 2mA

Note:

Because Voh depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet Voh Min value.

7.4.2 Bus Signal Level (High-Voltage)

The device input and output voltages shall be within the following specified ranges for any V_{CCQ} of the allowed voltage range.

■ **Push-pull signal level—high-voltage e•MMC**

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75 * V_{CCQ}	--	V	I_{OH} = -100uA @ V_{CCQ} min
Output LOW voltage	V_{OL}	--	0.125 * V_{CCQ}	V	I_{OL} = 100uA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625* V_{CCQ}	V_{CCQ} + 0.3	V	--
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25 * V_{CCQ}	V	--

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■ **Push-pull signal level—1.70 V -1.95 V V_{CCQ} voltage Range**

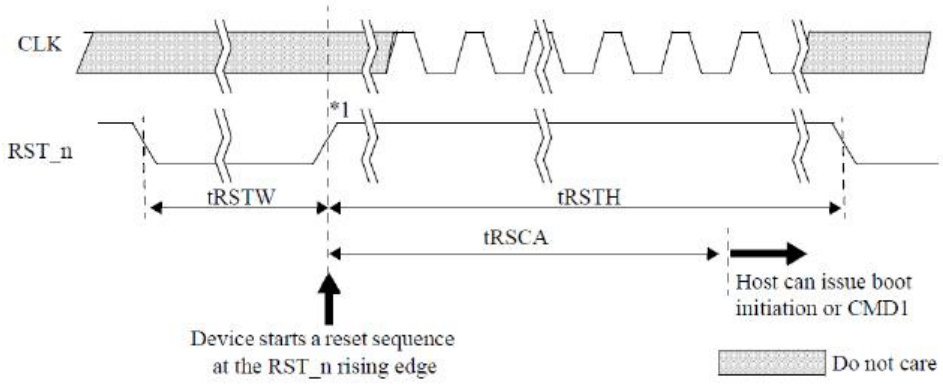
Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.45	--	V	I_{OH} = -2mA
Output LOW voltage	V_{OL}	--	0.45	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 * V_{CCQ} [1]	V_{CCQ} + 0.3	V	--
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35*V_{CCQ} (2)	V	--

Note:

- 0.7 * V_{DD} for MMC4.3 and older revisions.
- 0.3 * V_{DD} for MMC4.3 and older revisions.

7.5 H/W Reset Operation

■ **H/W Reset waveform**



NOTE 1 Device will detect the rising edge of RST_n signal to trigger internal reset sequence.

■ **H/W Reset Timing Parameters**

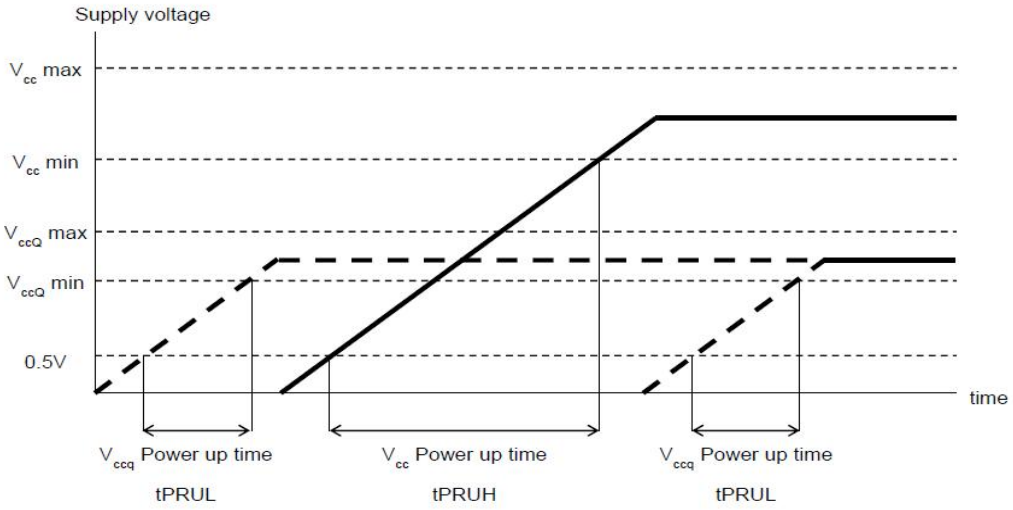
Symbol	Comment	Min	Max	Unit
t_{RSTW}	RST_n pulse width	1		μs
t_{RSCA}	RST_n to Command time	200 [1]		μs
t_{RSTH}	RST_n high period (interval time)	1		μs

Note 1: 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA.

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7.6 Power-up sequence



■ **Power-up parameter**

Parameter	Symbol	Test	Min	Max	Remark
Supply power-up for 3.3V	t_{PRUH}		5 μs	35 ms	--
Supply power-up for 1.8V	t_{PRUL}		5 μs	25 ms	--

8 DC Electrical Characteristics

8.1 Power Supply Voltage

Parameter	Symbol	Test Conditions	Min	Max	Unit
Supply voltage1 （NAND/Core）	V_{CC}	--	2.7	3.6	V
Supply voltage 2 （CTRL/IO）	V_{CCQ}	--	1.7	1.95	V
			2.7	3.6	V

8.2 Operating Current (RMS)

■ **Active Power Consumption during operation**

Capacity	Operation	Icc （Max）	Iccq （Max）	Unit
16 GB	Read	65	75	mA
	Write	75	70	mA
32 GB	Read	65	75	mA
	Write	80	70	mA
64 GB	Read	65	75	mA
	Write	85	70	mA

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Note:

- Power measurement conditions: Bus configuration =x8 @200MHz DDR
- Max RMS current is the average RMS current consumption over a period of 100ms.
- Temperature: 25℃
- V_{CC}=3.3V, V_{CCQ}=1.8V
- Not 100% tested

8.3 Standby Power Consumption

■ **Standby Power Consumption in auto power saving mode and standby state**

Capacity	State	Icc		Iccq		Unit
		25℃	85℃	25℃	85℃	
16 GB	Standby	30	120	160	600	uA
32 GB		40	160	160	600	uA
64 GB		50	200	160	600	uA

Note:

- Power measurement conditions: Bus configuration =x8, No CLK
- V_{CC}=3.3V, V_{CCQ}=1.8V
- Not 100% tested

8.4 Sleep Power Consumption

■ **Sleep Power Consumption in Sleep State**

Capacity	State	Icc		Iccq		Unit
		25℃	85℃	25℃	85℃	
16 GB	Sleep	13	40	160	600	uA
32 GB		13	40	160	600	uA
64 GB		13	40	160	600	uA

Note:

- Power measurement conditions: Bus configuration = x8, No CLK
- Enter sleep state by CMD5, V_{CC} power is switched off, V_{CCQ}=1.8V
- Not 100% tested

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8.5 Bus Signal Line Load

The total capacitance C_L of each line of the e•MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the e•MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

■ **Bus Signal Line Load**

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	--	100	kΩ	to prevent bus floating
Pull-up resistance for DAT0–DAT7	R_{DAT}	10	--	100	kΩ	to prevent bus floating
Internal pull up resistance DAT1–DAT7	R_{int}	10	--	150	kΩ	to prevent unconnected lines floating
Bus signal line capacitance	C_L	--	--	30	pF	Single Device
Single Device capacitance	C_{DEVICE}	--	--	12	pF	Single Device capacitance
Maximum signal line inductance	--	--	--	16	nH	$f_{PP} \leq 52$ MHz

HS400 Capacitance and Resistors

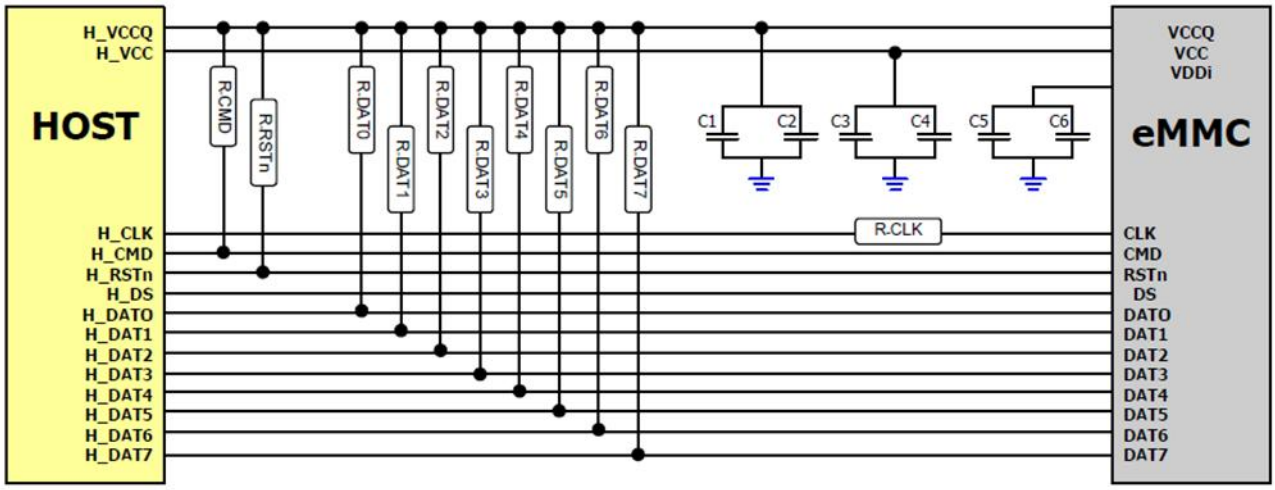
Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-down resistance for Data Strobe	R_{DS}	10	--	100	kΩ	
Single Device capacitance	C_{DEVICE}			6	pF	Single Device
Bus signal line capacitance	C_L			13	pF	Single Device

Note: Recommended maximum value is 50 kΩ for 1.8V interface supply voltages.

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9 Connection Guide



Connection guide specification

Parameter	Symbol	Min	Max	Recommend	Unit	Remark
Pull-up resistance for CMD	R_CMD	4.7	100	-	kohm	Pull-up resistance should be put on CMD line to prevent bus floating.
Pull-up resistance for DAT0~7	R_DAT	10	100	-	kohm	Pull-up resistance should be put on DAT line to prevent bus floating.
Data strobe(DS)	R_DS	NC	NC	NC	-	It is not necessary to put pull-up/pull-down resistance on DS line since DS is internally pulled down. Direct connection to host is required and please float this pin if it is not used
Pull-up resistance for RSTn	R_RSTn	10	100	-	kohm	It is not necessary to put pull-up resistance on RSTn line if host does not use H/W reset. (Extended CSD register [162] = 0b)
Serial resistance on CLK	R_CLK	0	100	-	ohm	To reduce overshooting/undershooting Note: If the host uses HS200, we recommend to remove this resister for better CLK signal
V_{ccq} capacitor value	C1 & C2	2.2±10%	4.7	2.2±10%	uF	Coupling cap should be connected with V_{ccq} closely.
V_{cc} capacitor value	C3 & C4	4.72±10%	10	4.72±10%	uF	Coupling cap should be connected with V_{cc} closely. V_{cc} /V_{ccq} cap. value would be up to Host requirement and the application system characteristics.
VDDi capacitor value	C5 & C6	0	2.2	0.1	uF	Coupling cap should be connected with VDDi and Vssq as closely possible. (Internal Cap : 1uF)

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