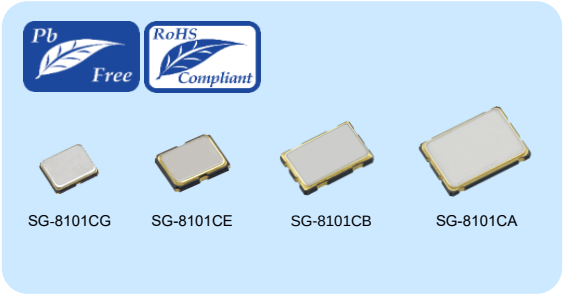
# Programmable Crystal Oscillator: SG-8101CG/SG-8101CE/SG-8101CB/SG-8101CA

## Features

- Crystal oscillator (Programmable)
- Output frequency: 0.67 MHz to 170 MHz (1 × $10^{-6}$ Step)
- Output: CMOS
- Supply voltage: 1.62 V to 3.63 V
- Frequency tolerance, Operating temperature:
  ±15 × $10^{-6}$ / -40 °C to +85 °C
  ±20 × $10^{-6}$, ±50 × $10^{-6}$ / -40 °C to +105 °C

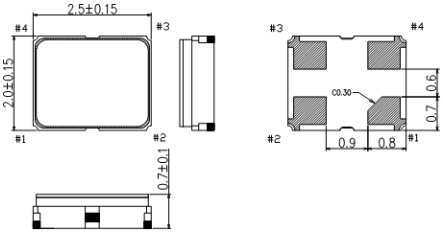



## Description

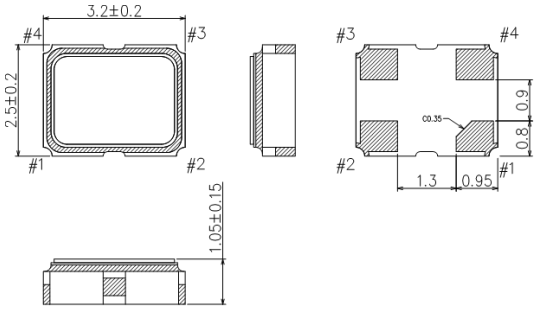
Epson's SG-8101 series are Programmable Crystal Oscillator series with CMOS output.
While this series offer the same easy programmability of frequencies and other parameters as comparable earlier SG-8002/SG-8003 series, they also have a wider operating temperature range, with a top-end limit of 105 °C.
In addition to a 2.5 × 2.0 mm package that will enable electronics manufacturers to save board space, the oscillators will also be available in the following popular package sizes: 3.2 × 2.5 mm, 5.0 × 3.2 mm and 7.0 × 5.0 mm. The oscillator in the SG-8101 series have an approximately 66 % tighter frequency tolerance and 50 % lower current consumption than comparable products, and can be used under a wide range of environmental conditions. This will also significantly contribute to performance, lower power requirements, fast development cycles, and low-volume production.

## Outline Drawing and Terminal Assignment

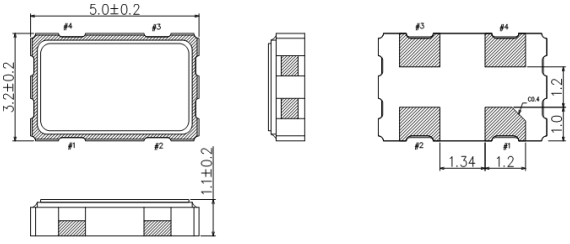
SG-8101CG



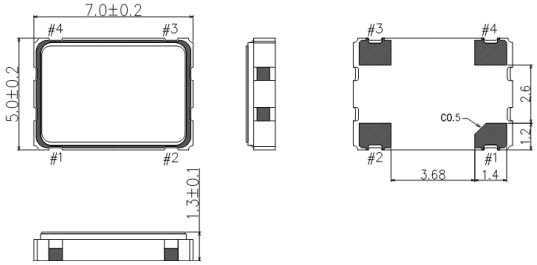

SG-8101CE




SG-8101CB




SG-8101CA




Terminal Assignment

| Pin # | Connection | Function | | |
|---|---|---|---|---|
| #1 | OE | OE terminal | | |
| | | OE function | Osc. Circuit | Output |
| | | "H" * | Oscillation | Specified frequency: Enable |
| | | "L" | Oscillation | Low (weak pull down): Disable |
| | $\overline{ST}$ | $\overline{ST}$ terminal | | |
| | | $\overline{ST}$ function | Osc. Circuit | Output |
| | | "H" * | Oscillation | Specified frequency: Enable |
| | | "L" | Oscillation stop | Low (weak pull down): Disable |
| #2 | GND | GND terminal | | |
| #3 | OUT | Output terminal | | |
| #4 | $V_{CC}$ | $V_{CC}$ terminal | | |

* Please do not use the OE/$\overline{ST}$ terminal in the open state.

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[ 1 ] Product Name / Product Number

(1-1) Product Name (Standard Form)

SG-8101CG: X1G005181xxxx00
SG-8101CE: X1G005211xxxx00
SG-8101CB: X1G005201xxxx00
SG-8101CA: X1G005191xxxx00 (Please contact Epson for details)

(1-2) Product Number / Ordering Code

SG-8101CA 25.000000MHz T C H P A
① ② ③ ④⑤⑥⑦⑧

①Model ②Size ③Frequency ④Supply voltage (T: 1.8 V to 3.3 V Typ.)
⑤Frequency tolerance ⑥Operating temperature ⑦Function ⑧Rise time/Fall time

| ②Size | |
|---|---|
| CG | 2.5 mm × 2.0 mm |
| CE | 3.2 mm × 2.5 mm |
| CB | 5.0 mm × 3.2 mm |
| CA | 7.0 mm × 5.0 mm |

| ⑤Frequency tolerance / ⑥Operating temperature | |
|---|---|
| BG | ±15 × $10^{-6}$ / -40 °C to +85 °C |
| CH | ±20 × $10^{-6}$ / -40 °C to +105 °C |
| JH | ±50 × $10^{-6}$ / -40 °C to +105 °C |

| ⑦Function | |
|---|---|
| P | Output enable (#1pin = OE) |
| S | Standby (#1pin = $\overline{ST}$) |

| ⑧Rise time/Fall time | |
|---|---|
| A | Default |
| B | Fast |
| C* | Slow |

* Available only when fo ≤ 20 MHz

[ 2 ] Absolute Maximum Ratings

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum supply voltage | $V_{CC}$ | -0.3 | - | 4 | V | |
| Input voltage | $V_{IN}$ | GND - 0.3 | - | $V_{CC}$ + 0.3 | V | OE/$\overline{ST}$ terminal |
| Storage temperature range | T_stg | -40 | - | +125 | °C | |

[ 3 ] Operating Range

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply voltage | $V_{CC}$ | 1.62 | - | 3.63 | V | |
| Supply voltage | GND | 0.0 | 0.0 | 0.0 | V | |
| Input voltage | $V_{IN}$ | GND | - | $V_{CC}$ | V | OE/$\overline{ST}$ terminal |
| Operating temperature range | T_use | -40 | +25 | +85 | °C | |
| | | -40 | +25 | +105 | °C | |
| CMOS load condition | L_CMOS | - | - | 15 | pF | |

* Power supply startup time (0 %$V_{CC}$ → 90 %$V_{CC}$) should be between 5 µs and 500 ms
* A 0.1 µF or over bypass capacitor should be connected between $V_{CC}$ and GND pins located close to the device

[ 4 ] Frequency Characteristics (Unless stated otherwise [ 3 ] Operating Range)

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output frequency | fo | 0.67 | | 170 | MHz | |
| Frequency tolerance *1 | f_tol | -15 | - | +15 | ×$10^{-6}$ | T_use = -40 °C to +85 °C |
| | | -20 | - | +20 | ×$10^{-6}$ | T_use = -40 °C to +105 °C |
| | | -50 | - | +50 | ×$10^{-6}$ | |
| Frequency aging | f_age | Included in frequency tolerance | | | ×$10^{-6}$ | +25 °C, First year |

*1 Frequency tolerance includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient, frequency / load coefficient and frequency aging (+25 °C, first year)

[ 5 ] Electrical Characteristics (Unless stated otherwise [ 3 ] Operating Range)

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Start-up time | t_str | - | - | 3 | ms | t = 0 at $V_{CC}$ > 1.62 V |
| Current consumption (No load) $V_{CC}$ = 1.62 V to 1.98 V | $I_{CC}$ | - | 2.7 | 3.2 | mA | 0.67 MHz ≤ fo ≤ 20 MHz |
| | | - | 3.1 | 3.7 | | 20 MHz < fo ≤ 50 MHz |
| | | - | 3.5 | 4.0 | | 50 MHz < fo ≤ 75 MHz |
| | | - | 3.8 | 4.4 | | 75 MHz < fo ≤ 100 MHz |
| | | - | 4.1 | 4.8 | | 100 MHz < fo ≤ 125 MHz |
| | | - | 4.7 | 5.5 | | 125 MHz < fo ≤ 170 MHz |
| Current consumption (No load) $V_{CC}$ = 1.98 V to 2.20 V | | - | 2.7 | 3.3 | mA | 0.67 MHz ≤ fo ≤ 20 MHz |
| | | - | 3.1 | 3.8 | | 20 MHz < fo ≤ 50 MHz |
| | | - | 3.5 | 4.2 | | 50 MHz < fo ≤ 75 MHz |
| | | - | 3.8 | 4.6 | | 75 MHz < fo ≤ 100 MHz |
| | | - | 4.1 | 5.0 | | 100 MHz < fo ≤ 125 MHz |
| | | - | 4.7 | 5.8 | | 125 MHz < fo ≤ 170 MHz |
| Current consumption (No load) $V_{CC}$ = 2.20 V to 2.80 V | | - | 2.9 | 3.4 | mA | 0.67 MHz ≤ fo ≤ 20 MHz |
| | | - | 3.4 | 4.0 | | 20 MHz < fo ≤ 50 MHz |
| | | - | 3.9 | 4.6 | | 50 MHz < fo ≤ 75 MHz |
| | | - | 4.4 | 5.1 | | 75 MHz < fo ≤ 100 MHz |
| | | - | 4.8 | 5.7 | | 100 MHz < fo ≤ 125 MHz |
| | | - | 5.7 | 6.7 | | 125 MHz < fo ≤ 170 MHz |
| Current consumption (No load) $V_{CC}$ = 2.70 V to 3.63 V | | - | 3.0 | 3.5 | mA | 0.67 MHz ≤ fo ≤ 20 MHz |
| | | - | 3.8 | 4.4 | | 20 MHz < fo ≤ 50 MHz |
| | | - | 4.4 | 5.2 | | 50 MHz < fo ≤ 75 MHz |
| | | - | 5.0 | 5.9 | | 75 MHz < fo ≤ 100 MHz |
| | | - | 5.7 | 6.7 | | 100 MHz < fo ≤ 125 MHz |
| | | - | 6.8 | 8.1 | | 125 MHz < fo ≤ 170 MHz |
| Disable current | I_dis | - | 2.8 | 3.2 | mA | $V_{CC}$ = 1.62 V to 1.98 V |
| | | - | 2.8 | 3.3 | | $V_{CC}$ = 1.98 V to 2.20 V |
| | | - | 2.8 | 3.3 | | $V_{CC}$ = 2.20 V to 2.80 V |
| | | - | 2.9 | 3.5 | | $V_{CC}$ = 2.70 V to 3.63 V |
| Stand-by current | I_std | - | 0.3 | 0.9 | µA | $V_{CC}$ = 1.62 V to 1.98 V |
| | | - | 0.4 | 1.0 | | $V_{CC}$ = 1.98 V to 2.20 V |
| | | - | 0.5 | 1.5 | | $V_{CC}$ = 2.20 V to 2.80 V |
| | | - | 1.1 | 2.5 | | $V_{CC}$ = 2.70 V to 3.63 V |
| Output voltage (DC characteristics) | $V_{OH}$ | 90 % $V_{CC}$ | - | - | V | $I_{OH}$ Condition<br>tr/tf \| $V_{CC}$ [V]: 1.62 to 1.98 \| 1.98 to 2.20 \| 2.20 to 2.80 \| 2.70 to 3.63<br>A (fo > 40 MHz), B: -2.5 mA \| -3.5 mA \| -4.0 mA \| -5.0 mA<br>A (fo ≤ 40 MHz): -1.5 mA \| -2.0 mA \| -2.5 mA \| -3.0 mA<br>C: -1.0 mA \| -1.5 mA \| -2.0 mA \| -2.5 mA |
| | $V_{OL}$ | - | - | 10 % $V_{CC}$ | V | $I_{OL}$ Condition<br>tr/tf \| $V_{CC}$ [V]: 1.62 to 1.98 \| 1.98 to 2.20 \| 2.20 to 2.80 \| 2.70 to 3.63<br>A (fo > 40 MHz), B: 2.5 mA \| 3.5 mA \| 4.0 mA \| 5.0 mA<br>A (fo ≤ 40 MHz): 1.5 mA \| 2.0 mA \| 2.5 mA \| 3.0 mA<br>C: 1.0 mA \| 1.5 mA \| 2.0 mA \| 2.5 mA |
| Symmetry | SYM | 45 | 50 | 55 | % | 50 % $V_{CC}$ level, L_CMOS ≤ 15 pF |
| Rise time/Fall time | tr/tf | - | - | 3 | ns | A (fo > 40 MHz); 20 % - 80 % $V_{CC}$ level, L_CMOS = 15 pF |
| | | - | - | 6 | | A (fo ≤ 40 MHz) |
| | | - | - | 3 | | B |
| | | - | - | 10 | | C (fo ≤ 20 MHz) |
| Input voltage | $V_{IH}$ | 70 % $V_{CC}$ | - | - | V | OE/$\overline{ST}$ terminal |
| | $V_{IL}$ | - | - | 30 % $V_{CC}$ | V | |
| Input capacitance | $C_{IN}$ | - | 2.5 | 5 | pF | OE/$\overline{ST}$ terminal |
| Input pull up resistance | $R_{UP1}$ | 20 | - | 150 | kΩ | OE/$\overline{ST}$ = 70 % $V_{CC}$ |
| | $R_{UP2}$ | 5 | - | 60 | MΩ | OE/$\overline{ST}$ = 30 % $V_{CC}$ |
| Output pull down resistance | $R_{DN}$ | 0.5 | - | 5 | MΩ | OE/$\overline{ST}$ = GND, OUT = $V_{CC}$ |
| Output disable time (OE) | tstp_oe | - | - | 1 | µs | OE terminal HIGH → LOW |
| Output disable time (ST) | tstp_st | - | - | 1 | µs | $\overline{ST}$ terminal HIGH → LOW |
| Output enable time (OE) | tsta_oe | - | - | 1 | µs | OE terminal LOW → HIGH |
| Output enable time (ST) | tsta_st | - | - | 3 | ms | $\overline{ST}$ terminal LOW → HIGH |

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(Unless stated otherwise [ 3 ] Operating Range)

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Phase jitter (Offset frequency: 12 kHz to 20 MHz) $V_{CC}$ = 1.62 V to 1.98 V | $t_{PJ}$ | - | - | 68.2 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 67.0 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 76.5 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 74.1 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 57.2 | | 125 MHz < fo ≤ 170 MHz |
| Phase jitter (Offset frequency: 12 kHz to 20 MHz) $V_{CC}$ = 2.25 V to 2.75 V | | - | - | 67.2 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 65.3 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 74.8 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 73.8 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 55.4 | | 125 MHz < fo ≤ 170 MHz |
| Phase jitter (Offset frequency: 12 kHz to 20 MHz) $V_{CC}$ = 2.97 V to 3.63 V | | - | - | 66.9 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 72.9 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 71.3 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 68.7 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 55.4 | | 125 MHz < fo ≤ 170 MHz |
| Peak to Peak jitter (Clock cycle > 50 000) $V_{CC}$ = 1.62 V to 1.98 V | $t_{p-p}$ | - | - | 366.0 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 263.4 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 111.0 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 81.9 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 80.0 | | 125 MHz < fo ≤ 170 MHz |
| Peak to Peak jitter (Clock cycle > 50 000) $V_{CC}$ = 2.25 V to 2.75 V | | - | - | 346.3 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 203.3 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 98.3 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 55.4 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 42.8 | | 125 MHz < fo ≤ 170 MHz |
| Peak to Peak jitter (Clock cycle > 50 000) $V_{CC}$ = 2.97 V to 3.63 V | | - | - | 344.1 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 199.4 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 97.2 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 53.0 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 33.8 | | 125 MHz < fo ≤ 170 MHz |
| RMS jitter (Clock cycle > 50 000) $V_{CC}$ = 1.62 V to 1.98 V | $t_{RMS}$ | - | - | 33.2 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 23.9 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 10.0 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 7.4 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 7.2 | | 125 MHz < fo ≤ 170 MHz |
| RMS jitter (Clock cycle > 50 000) $V_{CC}$ = 2.25 V to 2.75 V | | - | - | 31.4 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 18.4 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 8.9 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 5.0 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 3.8 | | 125 MHz < fo ≤ 170 MHz |
| RMS jitter (Clock cycle > 50 000) $V_{CC}$ = 2.97 V to 3.63 V | | - | - | 31.2 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 18.1 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 8.8 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 4.8 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 3.0 | | 125 MHz < fo ≤ 170 MHz |
| Cycle to Cycle jitter (Clock cycle > 50 000) $V_{CC}$ = 1.62 V to 1.98 V | $t_{c-c}$ | - | - | 265.2 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 208.7 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 75.7 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 63.3 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 66.1 | | 125 MHz < fo ≤ 170 MHz |
| Cycle to Cycle jitter (Clock cycle > 50 000) $V_{CC}$ = 2.25 V to 2.75 V | | - | - | 253.2 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 128.2 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 45.3 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 35.8 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 34.0 | | 125 MHz < fo ≤ 170 MHz |
| Cycle to Cycle jitter (Clock cycle > 50 000) $V_{CC}$ = 2.97 V to 3.63 V | | - | - | 249.9 | ps | 10 MHz ≤ fo ≤ 20 MHz |
| | | - | - | 122.0 | | 20 MHz < fo ≤ 40 MHz |
| | | - | - | 42.8 | | 40 MHz < fo ≤ 85 MHz |
| | | - | - | 28.0 | | 85 MHz < fo ≤ 125 MHz |
| | | - | - | 25.3 | | 125 MHz < fo ≤ 170 MHz |

[ 6 ] Thermal resistance (For reference only)

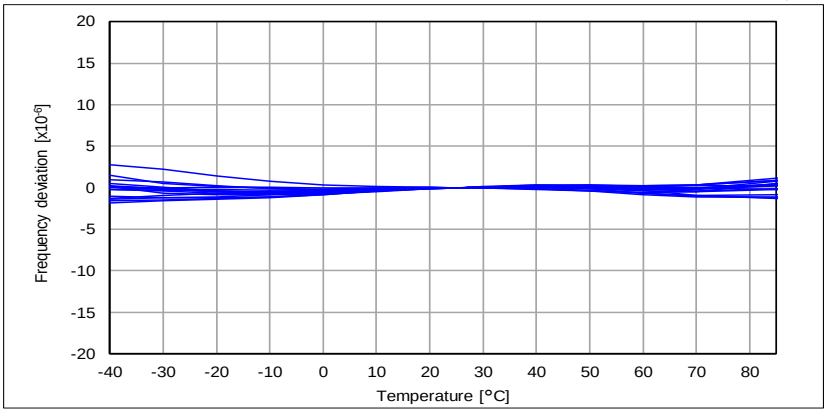
| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Junction temperature | Tj | - | - | +125 | °C | |
| Junction to case | θjc | - | 15.2 | - | °C/W | SG-8101CG |
| | | - | 23.1 | - | | SG-8101CE |
| | | - | 16.1 | - | | SG-8101CB |
| | | - | 28.0 | - | | SG-8101CA |
| Junction to ambient | θja | - | 91.9 | - | °C/W | SG-8101CG |
| | | - | 103.8 | - | | SG-8101CE |
| | | - | 82.5 | - | | SG-8101CB |
| | | - | 78.8 | - | | SG-8101CA |

[ 7 ] Typical Performance Characteristics (For reference only)

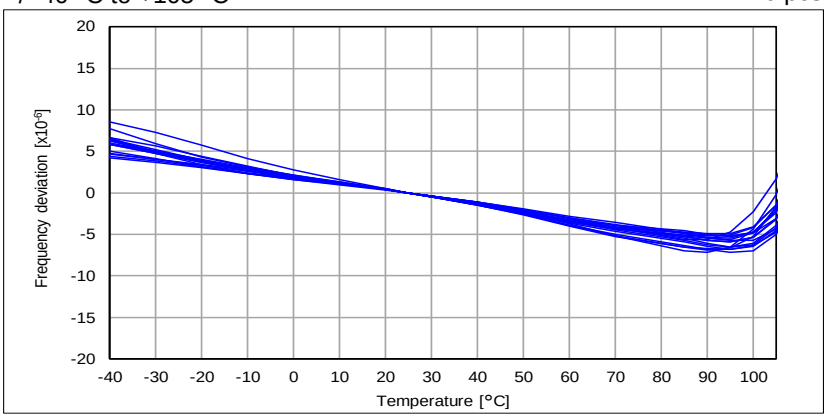
The following data shows typical performance characteristics

(7-1) Frequency / Temperature Characteristics

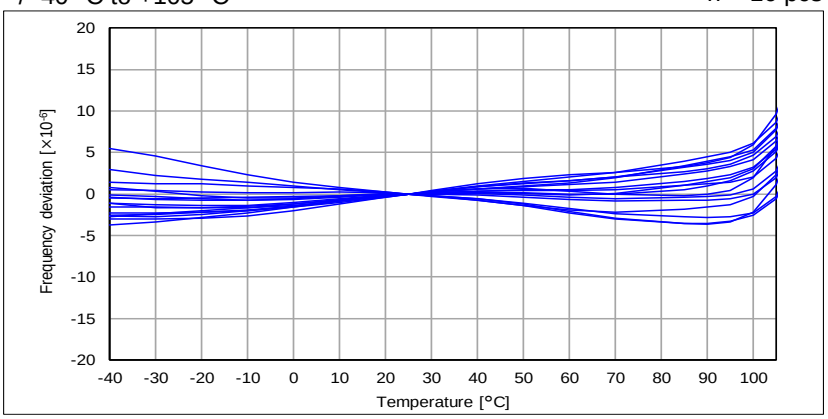
±15 × $10^{-6}$ / -40 °C to +85 °C n = 16 pcs




±20 × $10^{-6}$ / -40 °C to +105 °C n = 16 pcs

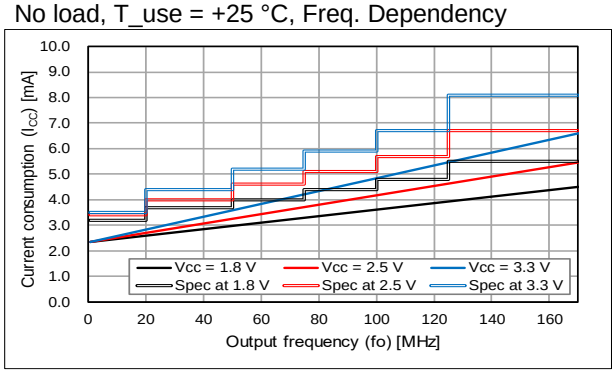



±50 × $10^{-6}$ / -40 °C to +105 °C n = 16 pcs

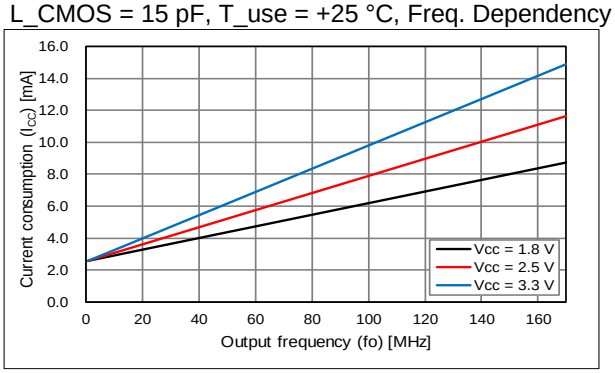


## (7-2) Current Consumption

No load, T_use = +25 °C, Freq. Dependency

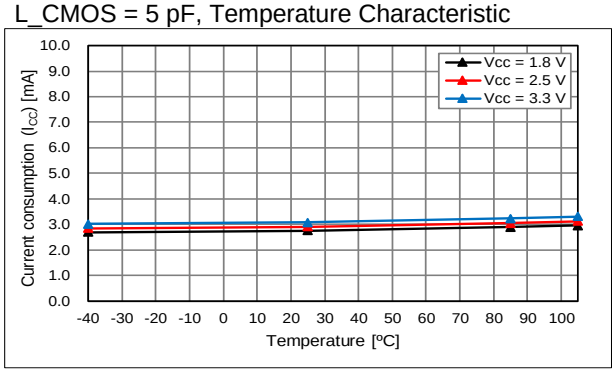



L_CMOS = 15 pF, T_use = +25 °C, Freq. Dependency

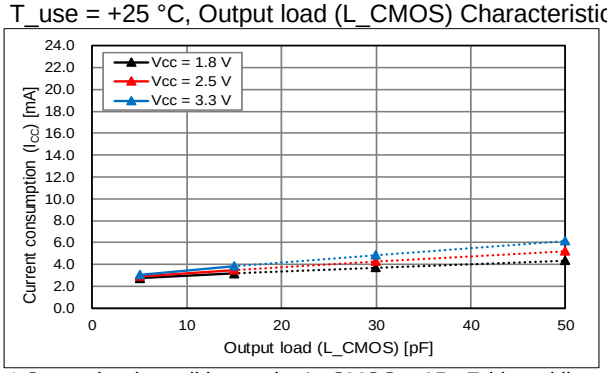



fo = 19.2 MHz

L_CMOS = 5 pF, Temperature Characteristic



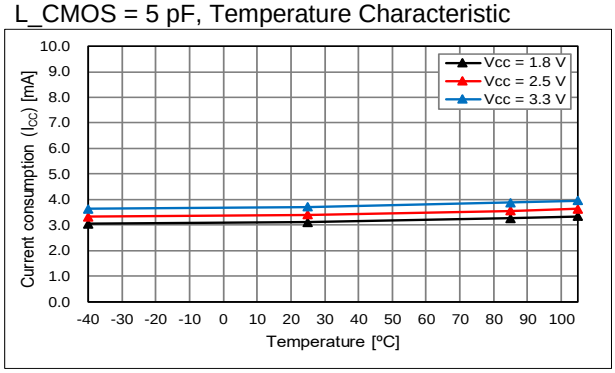

T_use = +25 °C, Output load (L_CMOS) Characteristics



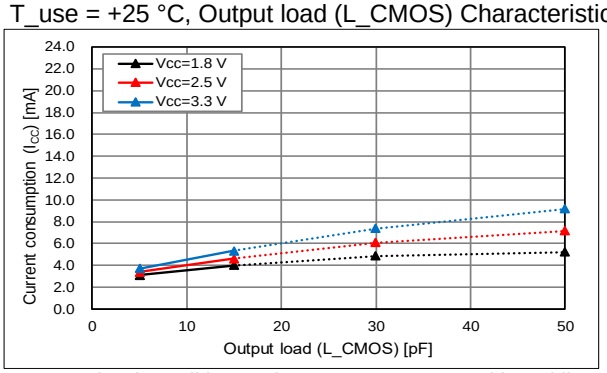

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 40 MHz

L_CMOS = 5 pF, Temperature Characteristic



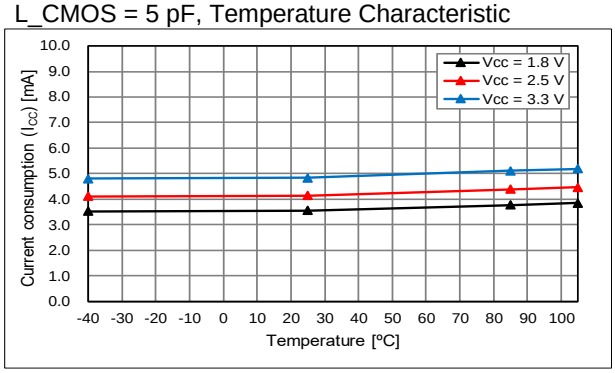

T_use = +25 °C, Output load (L_CMOS) Characteristics



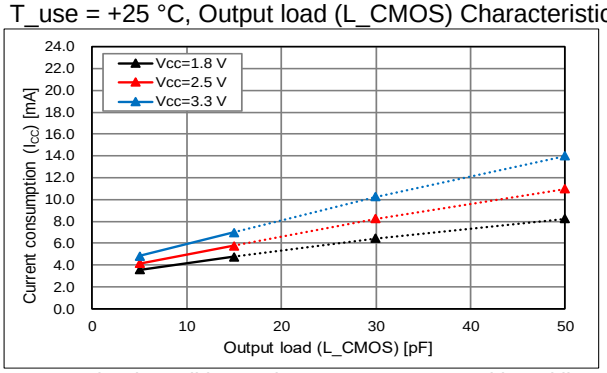

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 60 MHz

L_CMOS = 5 pF, Temperature Characteristic




T_use = +25 °C, Output load (L_CMOS) Characteristics

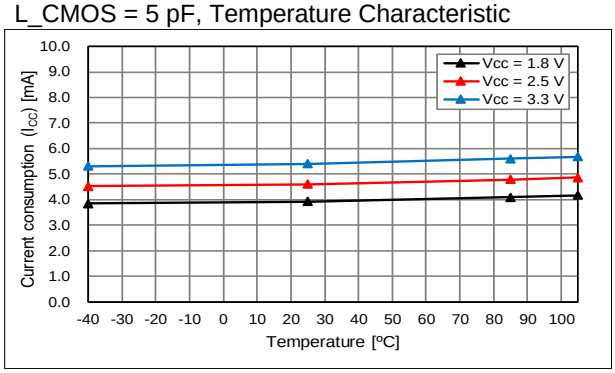



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

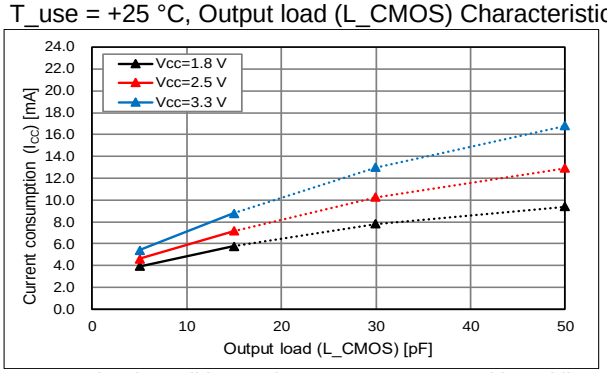
(7-2) Current Consumption [cont'd]

fo = 80 MHz

L_CMOS = 5 pF, Temperature Characteristic



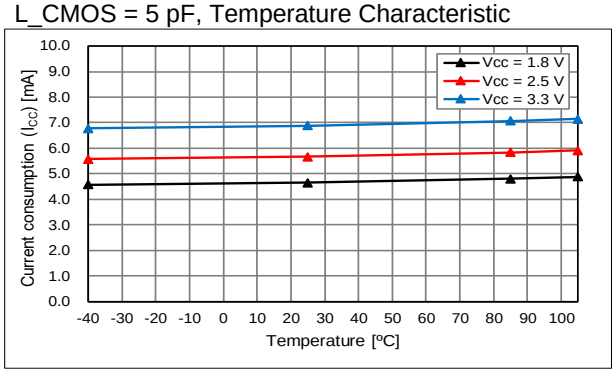

T_use = +25 °C, Output load (L_CMOS) Characteristics



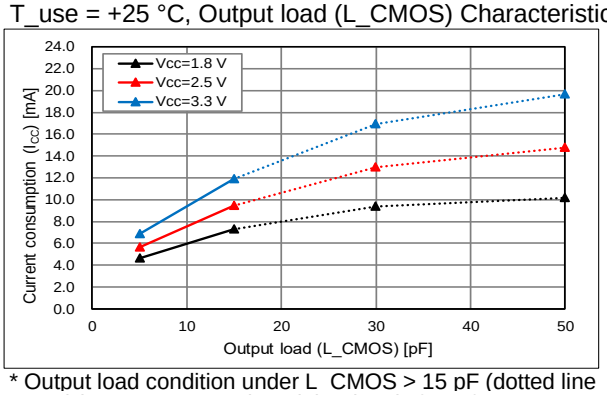

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 122.88 MHz

L_CMOS = 5 pF, Temperature Characteristic



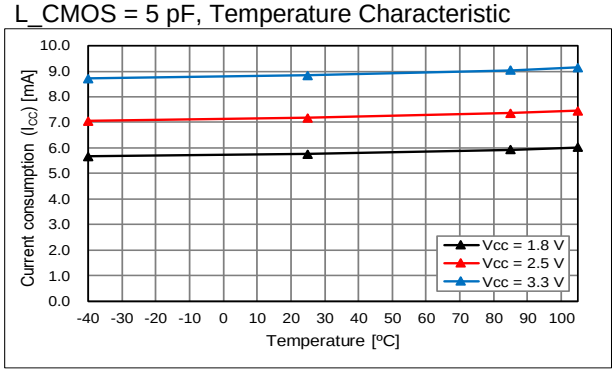

T_use = +25 °C, Output load (L_CMOS) Characteristics



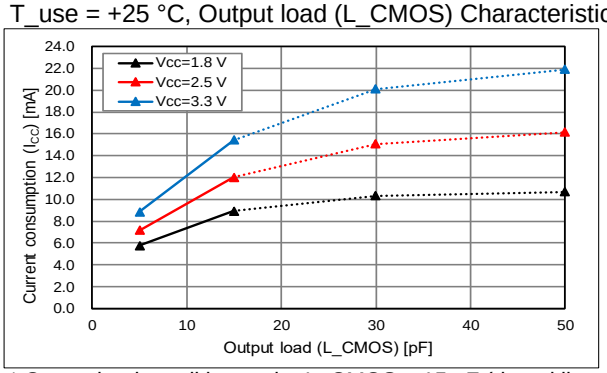

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 170 MHz

L_CMOS = 5 pF, Temperature Characteristic




T_use = +25 °C, Output load (L_CMOS) Characteristics




* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

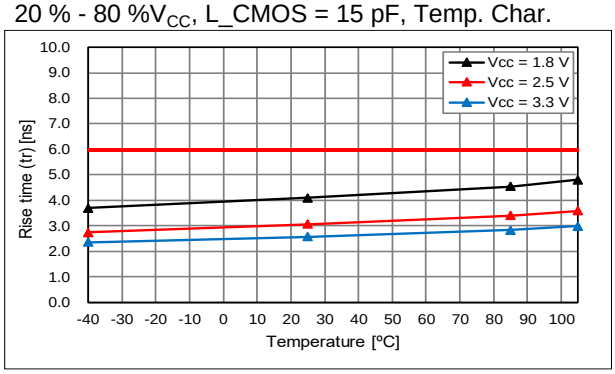
The actual current consumption is the total of the current under the condition of no load and the current to drive the output load (fo × L_CMOS × $V_{CC}$). To reduce the current consumption, it is effective to use lower frequency, lower supply voltage and lower output load.

(7-3) Rise Time/Fall Time

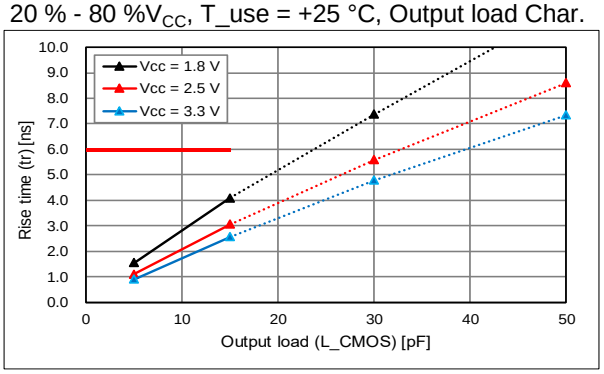
fo = 19.2 MHz, Rise time/Fall time: A (Default)

Rise Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.

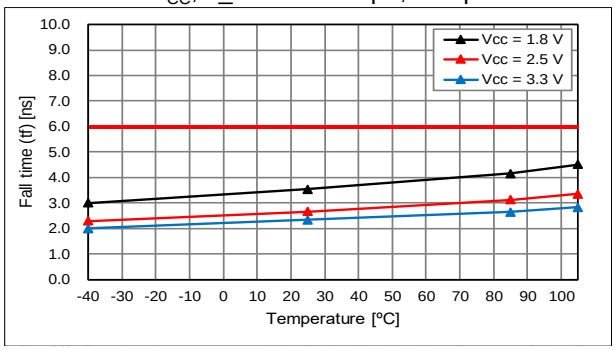



20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

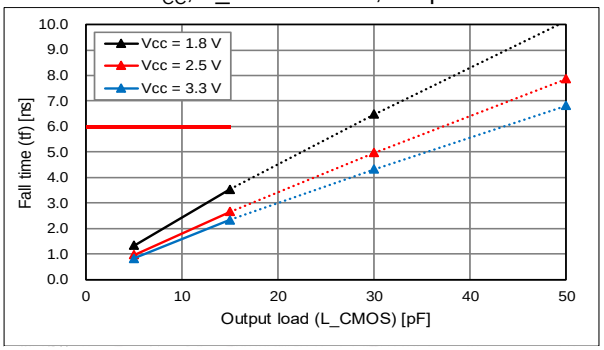



Fall Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

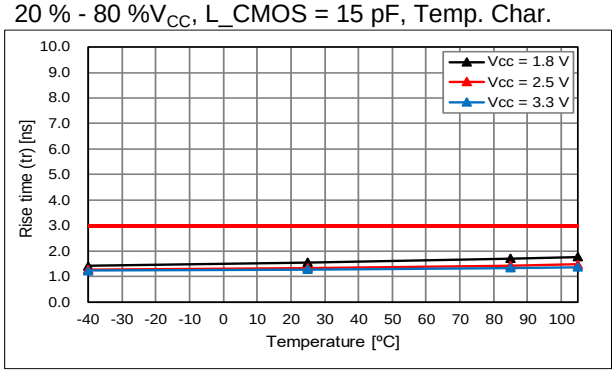



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

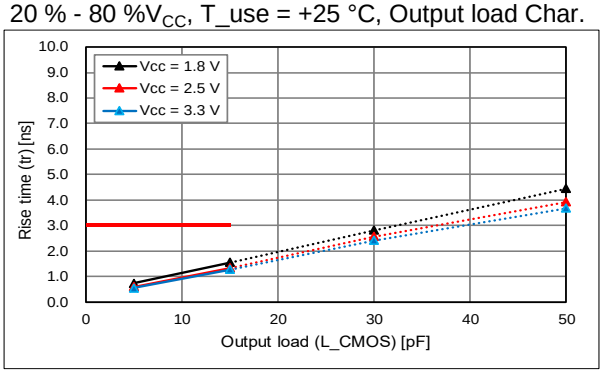
fo = 19.2 MHz, Rise time/Fall time: B (Fast)

Rise Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.

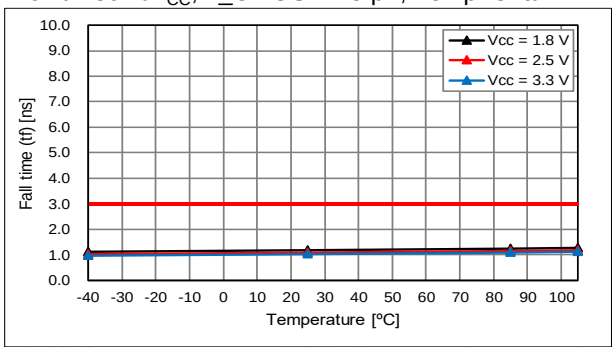



20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

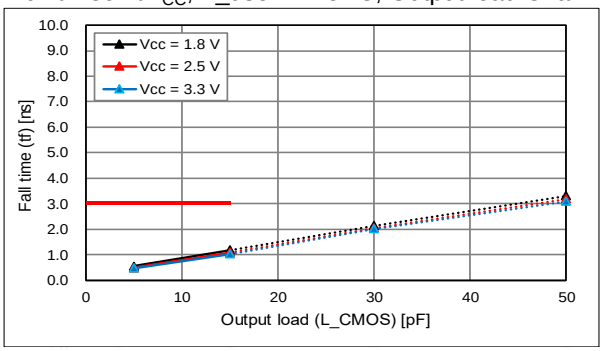



Fall Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.



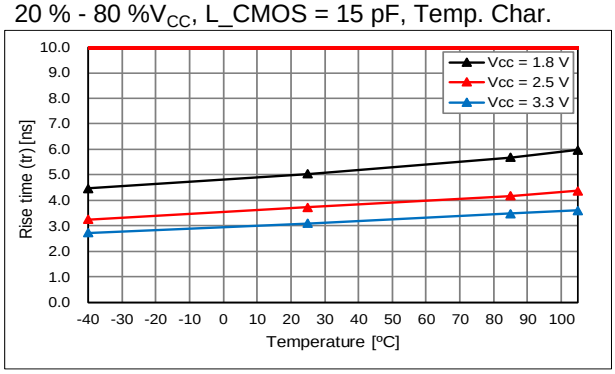

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

(7-3) Rise Time/Fall Time [cont'd]

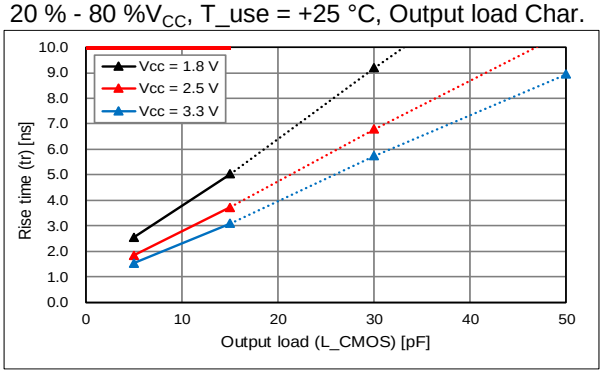
fo = 19.2 MHz, Rise time/Fall time: C (Slow)

Rise Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.

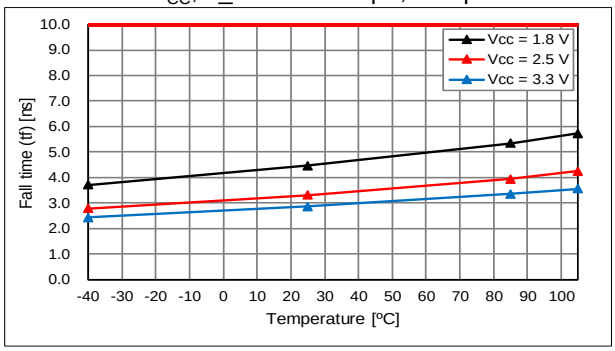



20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

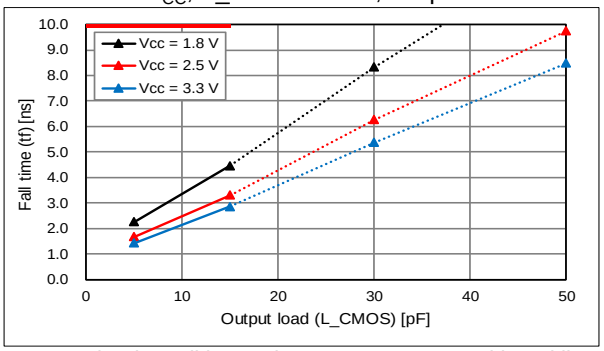



Fall Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.



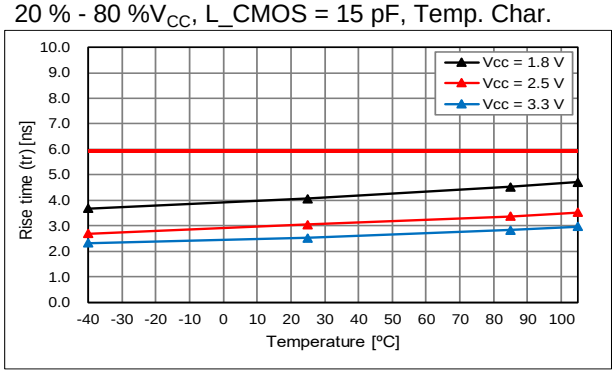

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

(7-3) Rise Time/Fall Time [cont'd]

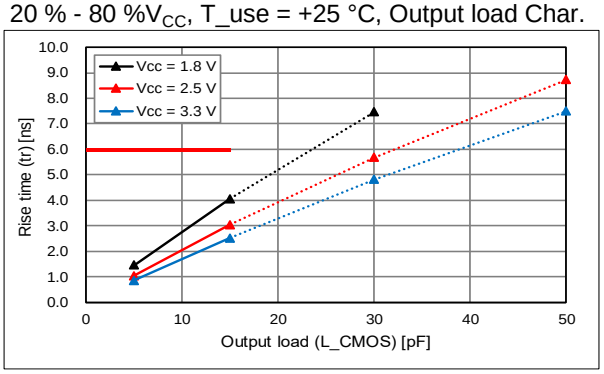
fo = 40 MHz, Rise time/Fall time: A (Default)

Rise Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.

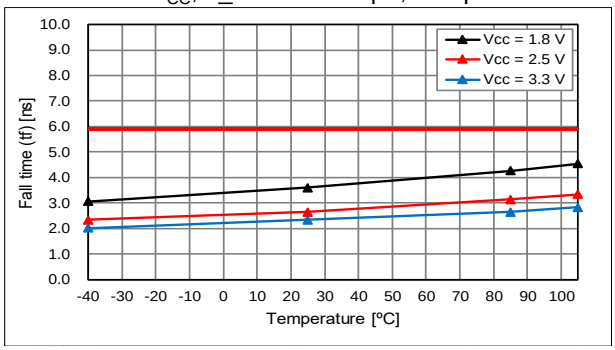



20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

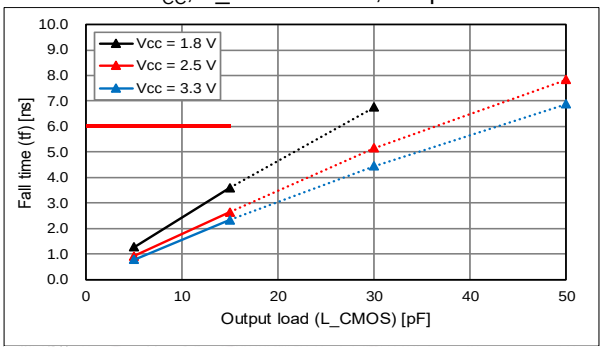



Fall Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

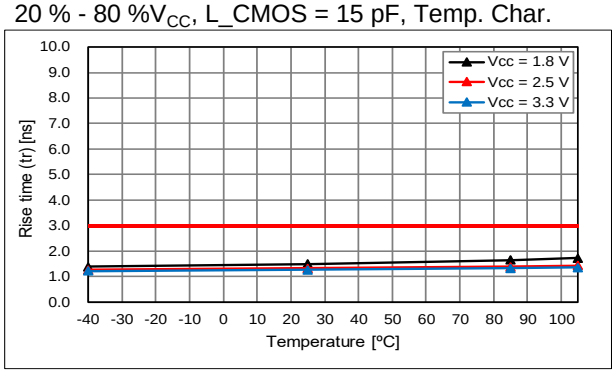



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

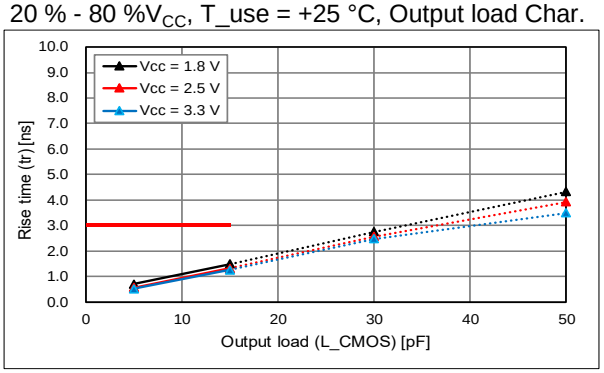
fo = 40 MHz, Rise time/Fall time: B (Fast)

Rise Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.

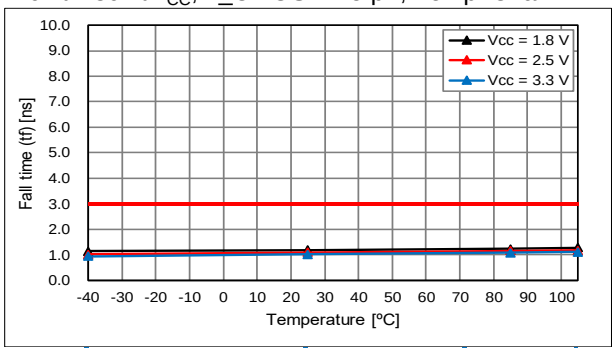



20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

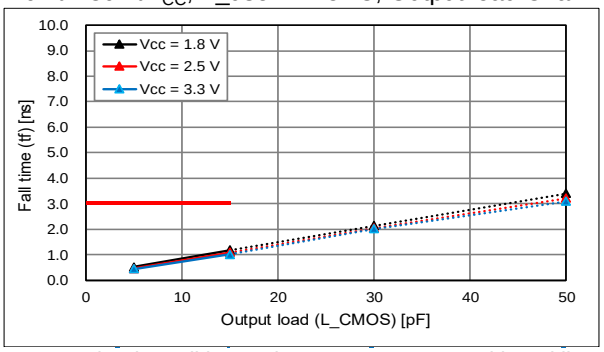



Fall Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.



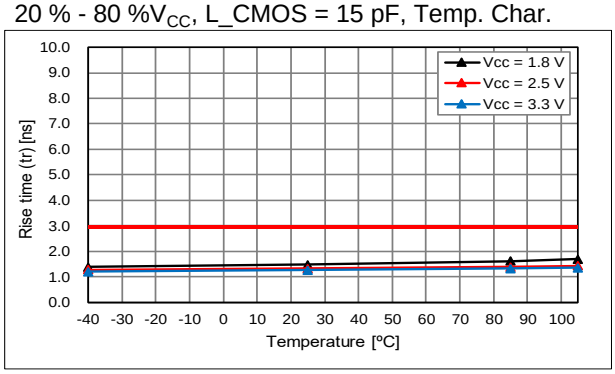

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

(7-3) Rise Time/Fall Time [cont'd]

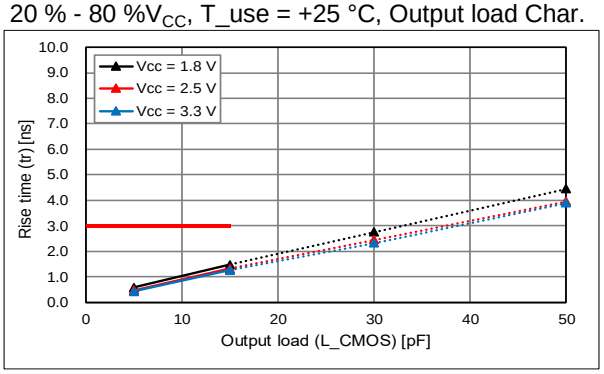
fo = 60 MHz, Rise time/Fall time: A (Default) & B (Fast)

Rise Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.

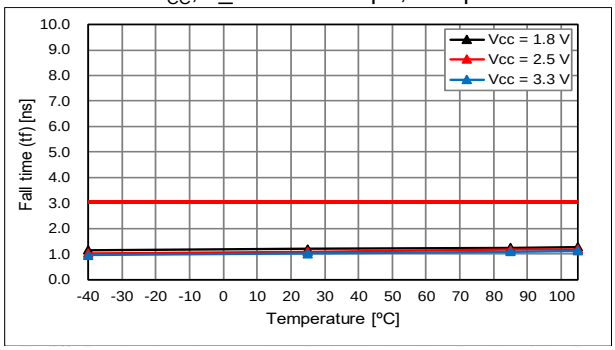



20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

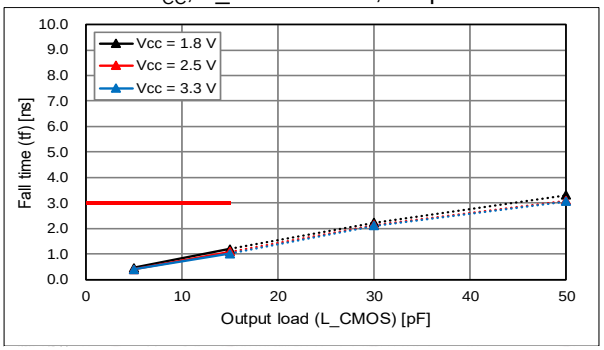



Fall Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

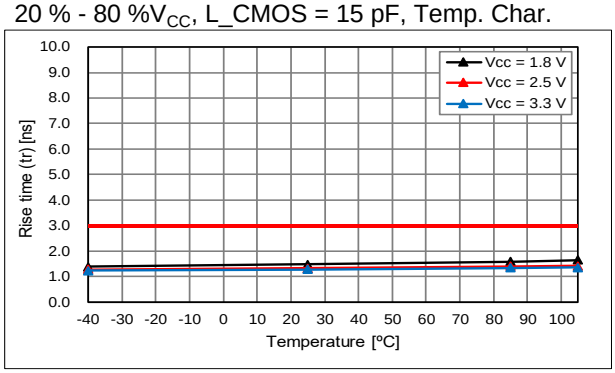



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

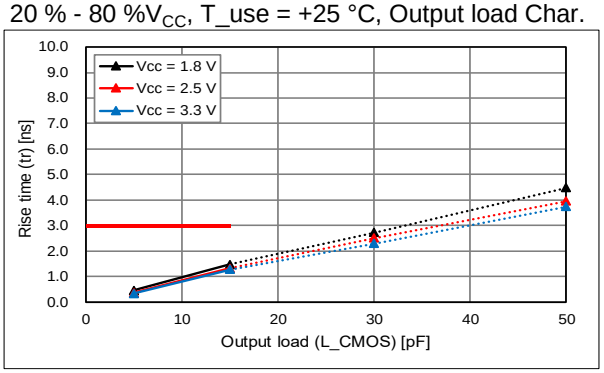
fo = 80 MHz, Rise time/Fall time: A (Default) & B (Fast)

Rise Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.

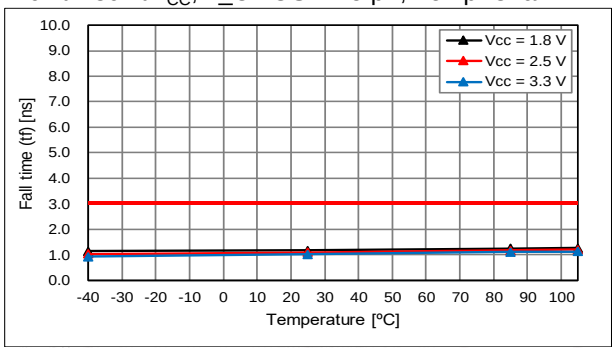



20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

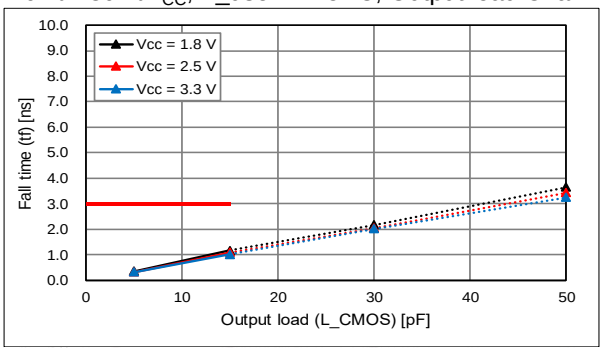



Fall Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.



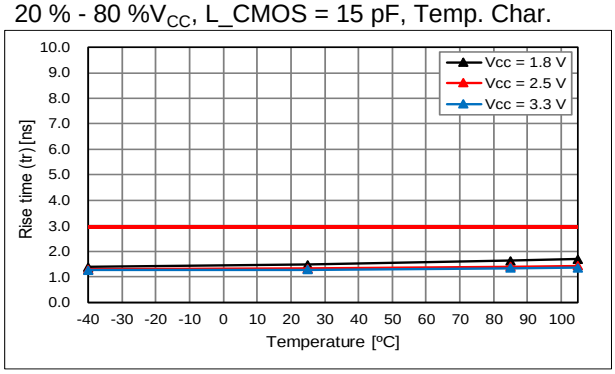

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

(7-3) Rise Time / Fall Time [cont'd]

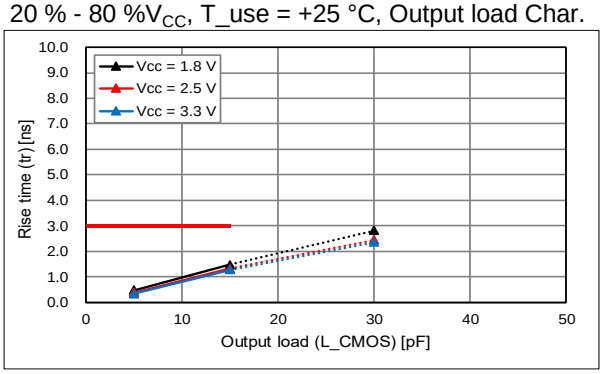
fo = 122.88 MHz, Rise time/Fall time: A (Default) & B (Fast)

Rise Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.

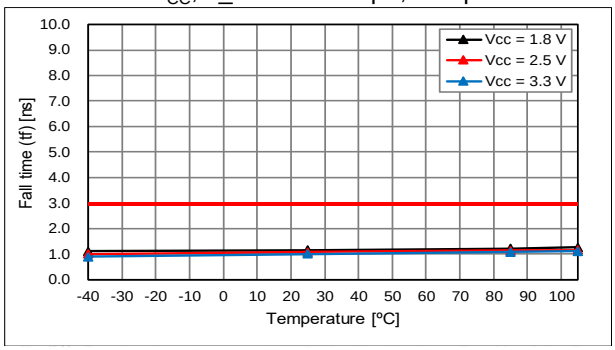



20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

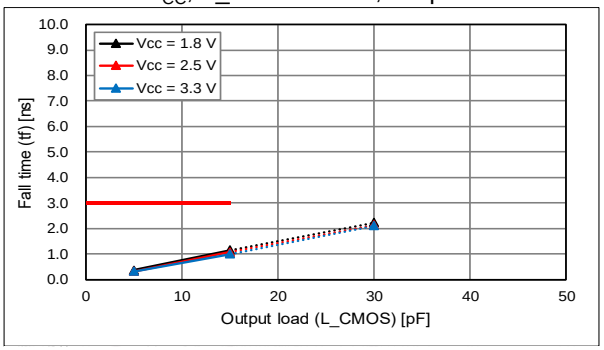



Fall Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

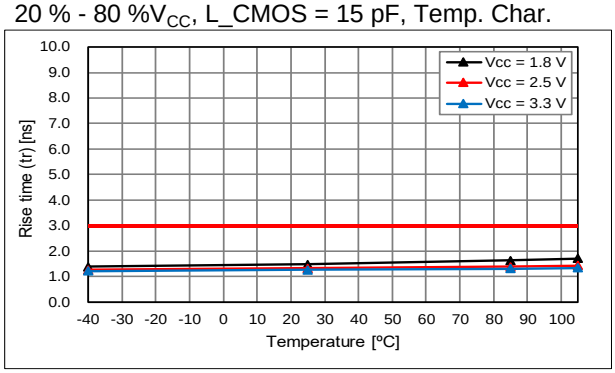



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

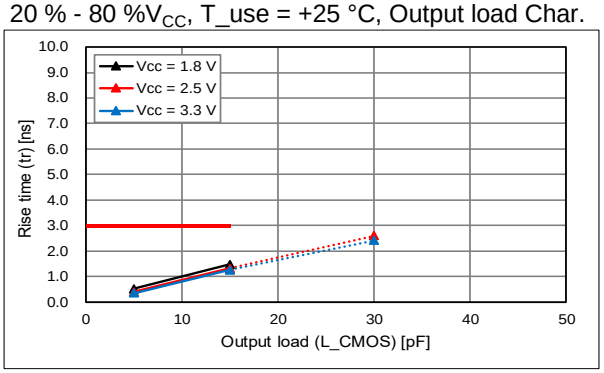
fo = 170 MHz, Rise time/Fall time: A (Default) & B (Fast)

Rise Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.

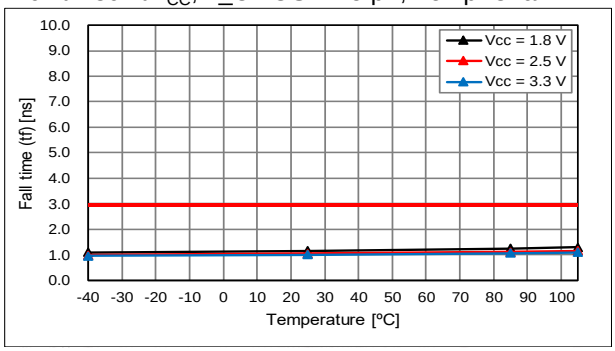



20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

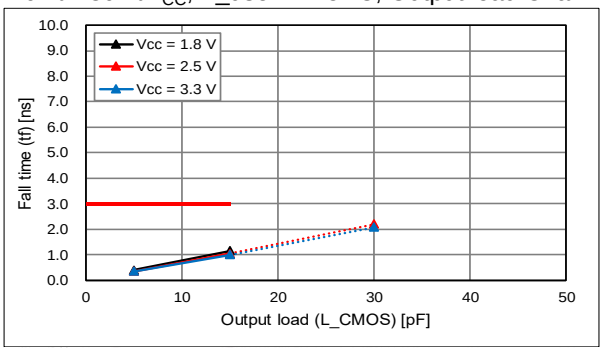



Fall Time

20 % - 80 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




20 % - 80 %$V_{CC}$, T_use = +25 °C, Output load Char.

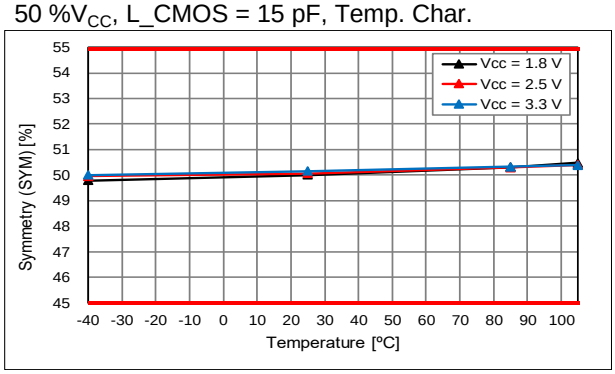



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

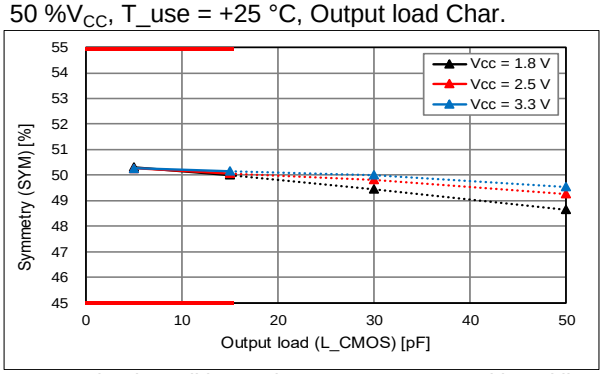
(7-4) Symmetry

fo = 19.2 MHz, Rise time/Fall time: A (Default)

50 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.



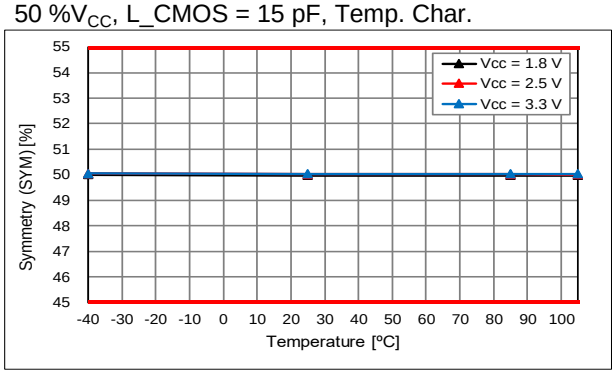

50 %$V_{CC}$, T_use = +25 °C, Output load Char.



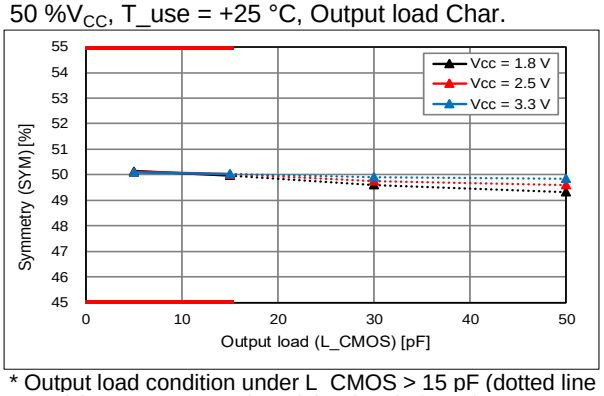

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 19.2 MHz, Rise time/Fall time: B (Fast)

50 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.



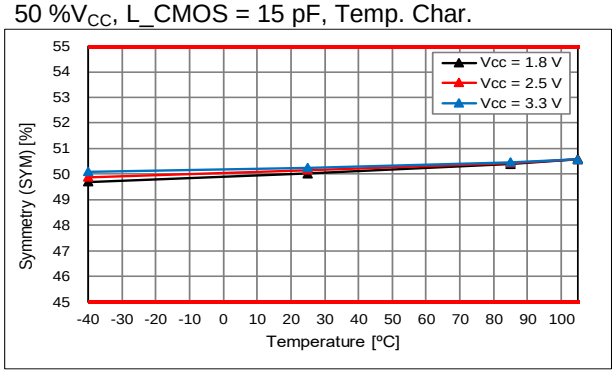

50 %$V_{CC}$, T_use = +25 °C, Output load Char.



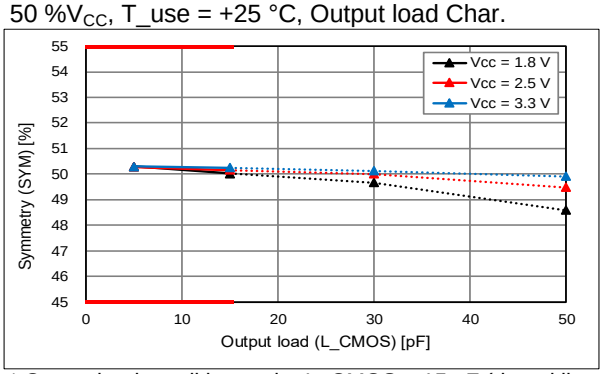

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 19.2 MHz, Rise time/Fall time: C (Slow)

50 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




50 %$V_{CC}$, T_use = +25 °C, Output load Char.

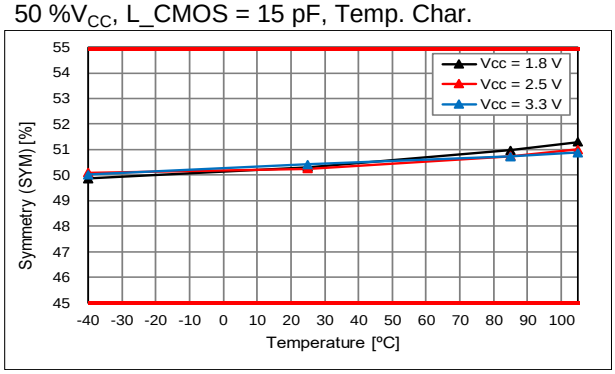



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

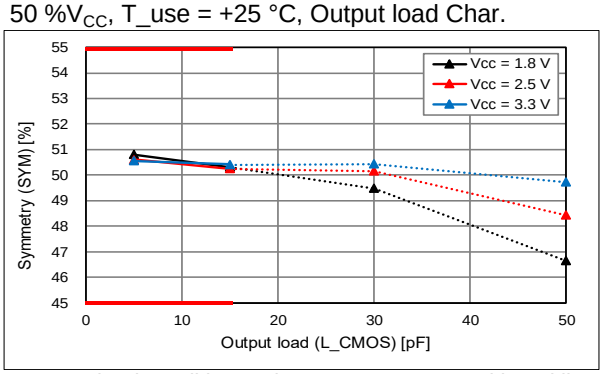
(7-4) Symmetry [cont'd]

fo = 40 MHz, Rise time/Fall time: A (Default)

50 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.



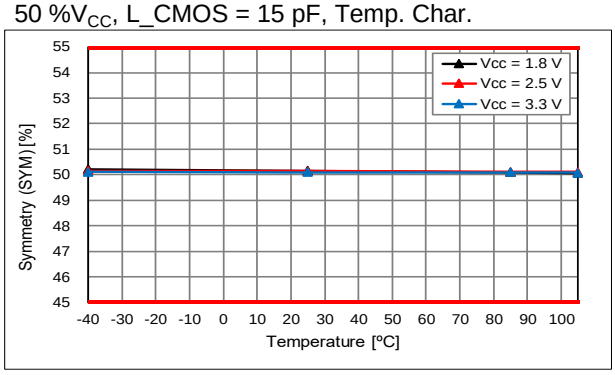

50 %$V_{CC}$, T_use = +25 °C, Output load Char.



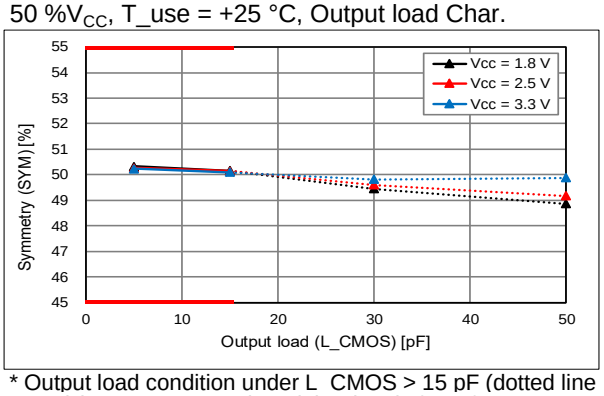

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 40 MHz, Rise time/Fall time: B (Fast)

50 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.



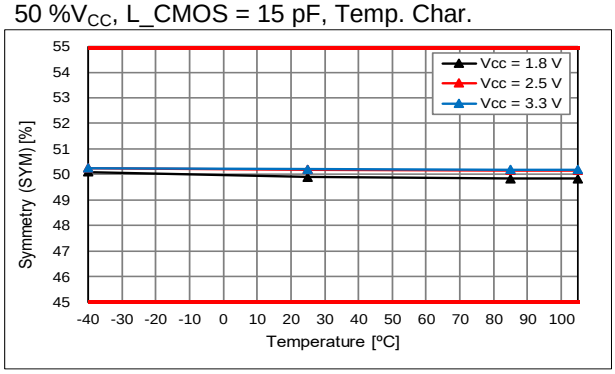

50 %$V_{CC}$, T_use = +25 °C, Output load Char.



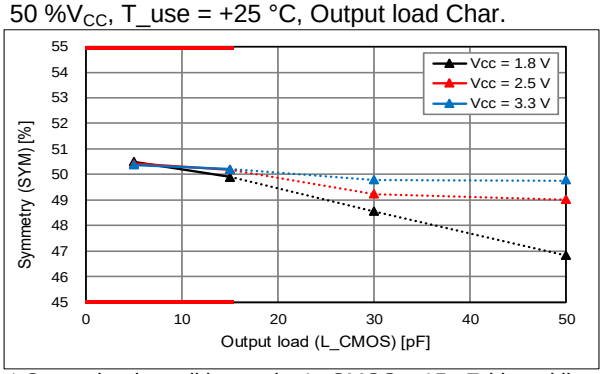

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 60 MHz, Rise time/Fall time: A (Default) & B (Fast)

50 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.



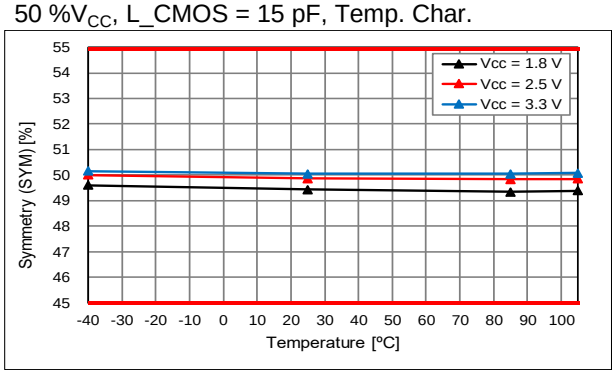

50 %$V_{CC}$, T_use = +25 °C, Output load Char.



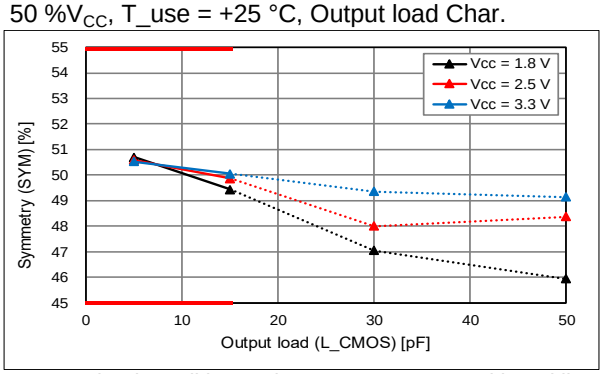

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 80 MHz, Rise time/Fall time: A (Default) & B (Fast)

50 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




50 %$V_{CC}$, T_use = +25 °C, Output load Char.

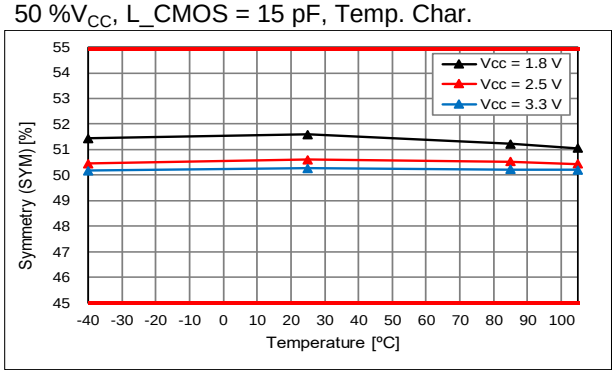



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

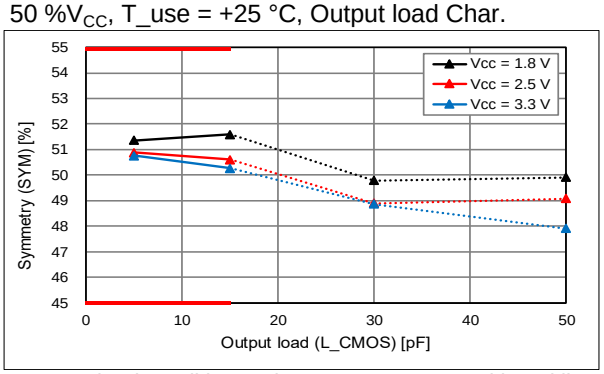
(7-4) Symmetry [cont'd]

fo = 122.88 MHz, Rise time/Fall time: A (Default) & B (Fast)

50 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.



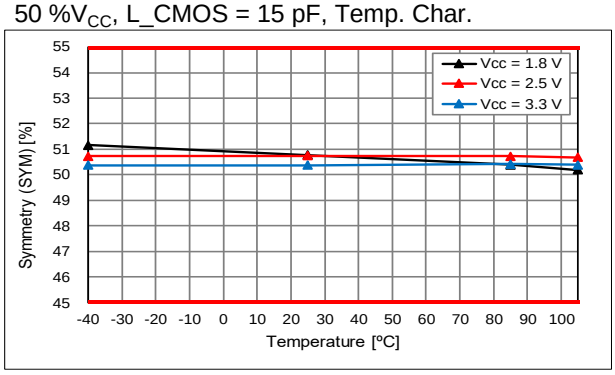

50 %$V_{CC}$, T_use = +25 °C, Output load Char.



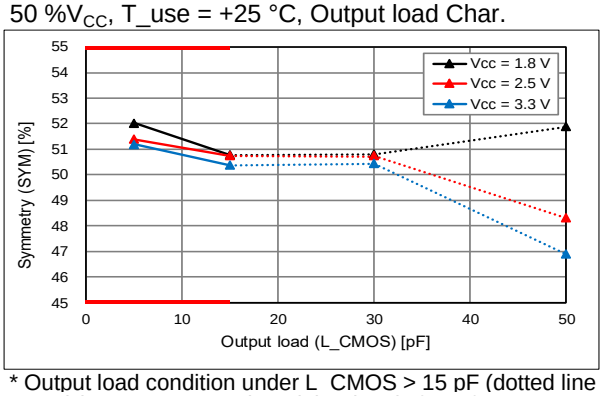

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 170 MHz, Rise time/Fall time: A (Default) & B (Fast)

50 %$V_{CC}$, L_CMOS = 15 pF, Temp. Char.




50 %$V_{CC}$, T_use = +25 °C, Output load Char.

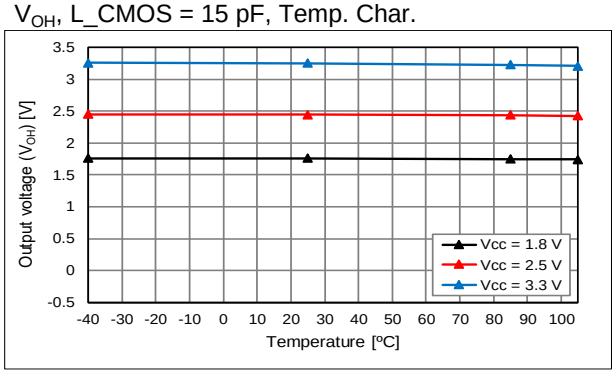



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

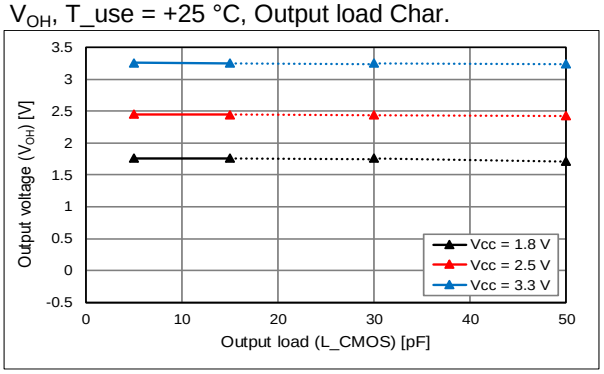
(7-5) Output Voltage

fo = 19.2 MHz, Rise time/Fall time: A (Default)

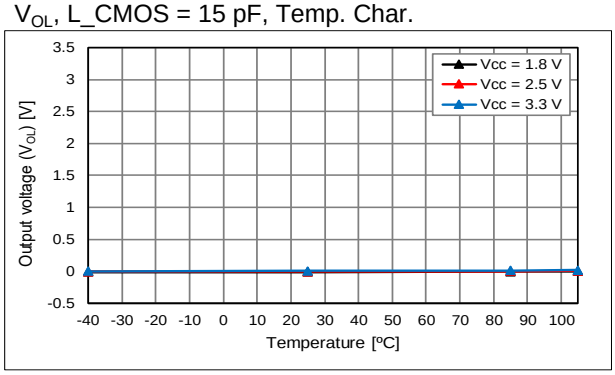
$V_{OH}$, L_CMOS = 15 pF, Temp. Char.



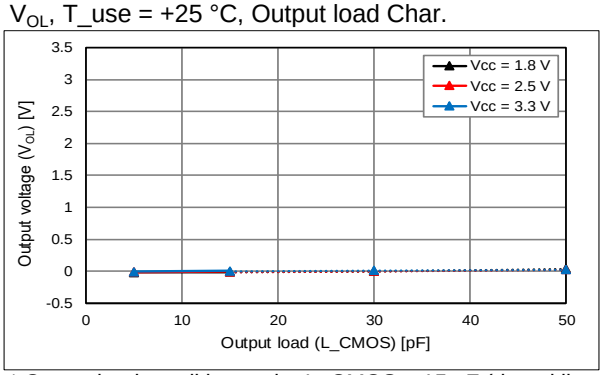

$V_{OH}$, T_use = +25 °C, Output load Char.




$V_{OL}$, L_CMOS = 15 pF, Temp. Char.



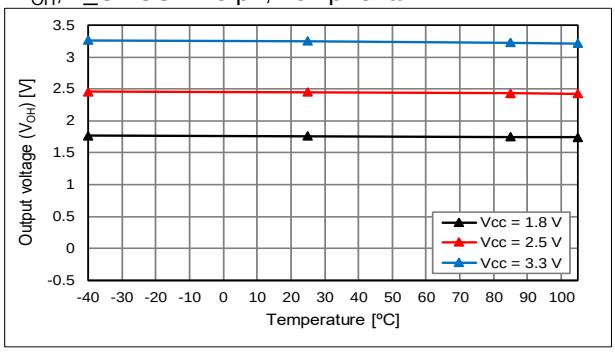

$V_{OL}$, T_use = +25 °C, Output load Char.



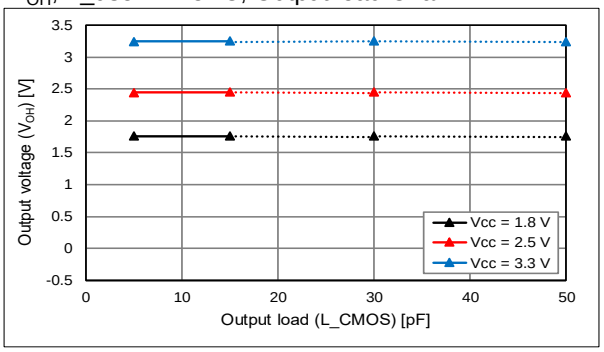

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 19.2 MHz, Rise time/Fall time: B (Fast)

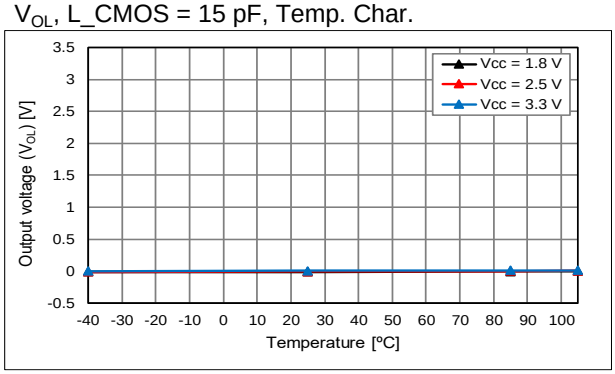
$V_{OH}$, L_CMOS = 15 pF, Temp. Char.



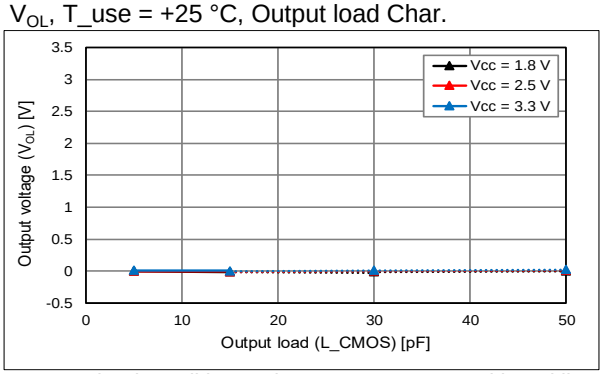

$V_{OH}$, T_use = +25 °C, Output load Char.




$V_{OL}$, L_CMOS = 15 pF, Temp. Char.




$V_{OL}$, T_use = +25 °C, Output load Char.

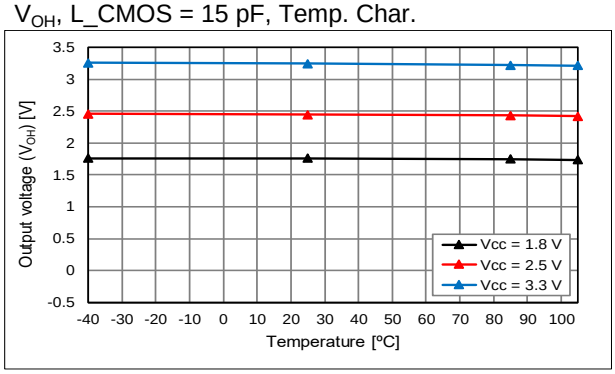



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

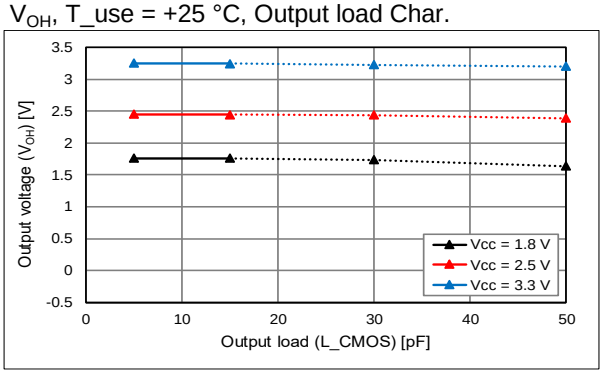
(7-5) Output Voltage [cont'd]

fo = 19.2 MHz, Rise time/Fall time: C (Slow)

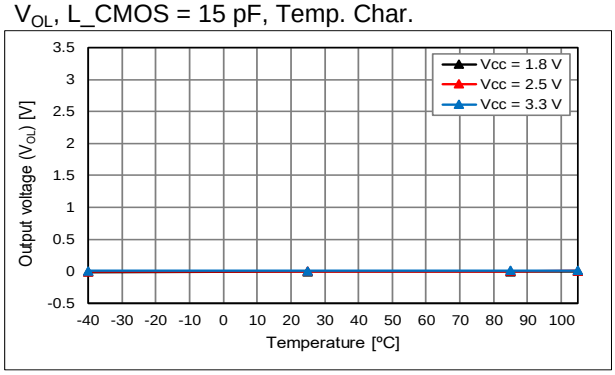
$V_{OH}$, L_CMOS = 15 pF, Temp. Char.



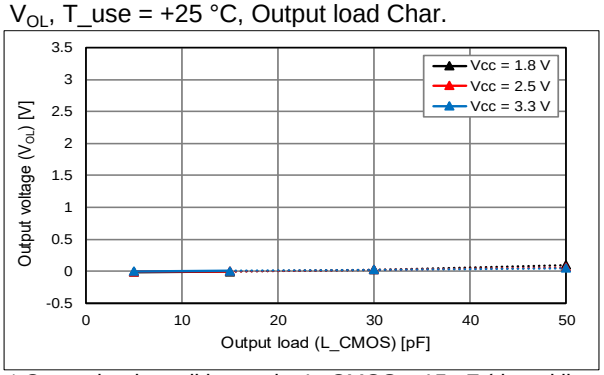

$V_{OH}$, T_use = +25 °C, Output load Char.




$V_{OL}$, L_CMOS = 15 pF, Temp. Char.



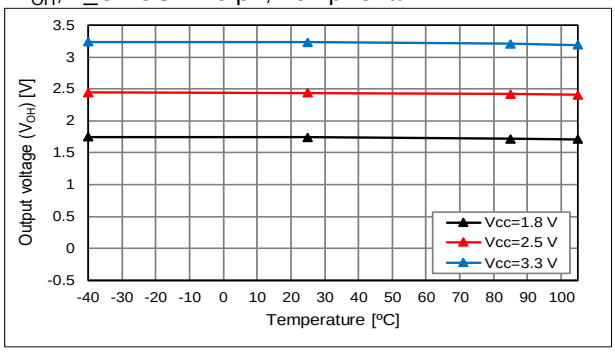

$V_{OL}$, T_use = +25 °C, Output load Char.



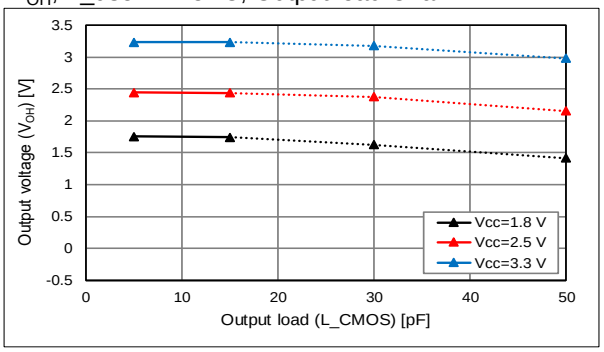

* Output load condition under L CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 40 MHz, Rise time/Fall time: A (Default)

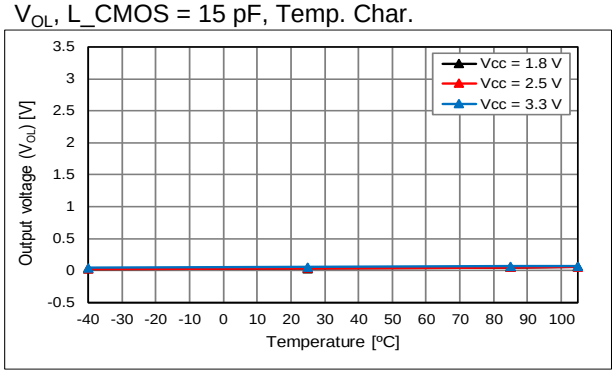
$V_{OH}$, L_CMOS = 15 pF, Temp. Char.



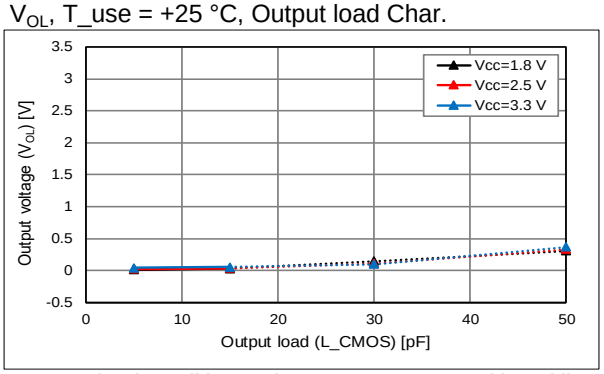

$V_{OH}$, T_use = +25 °C, Output load Char.




$V_{OL}$, L_CMOS = 15 pF, Temp. Char.




$V_{OL}$, T_use = +25 °C, Output load Char.

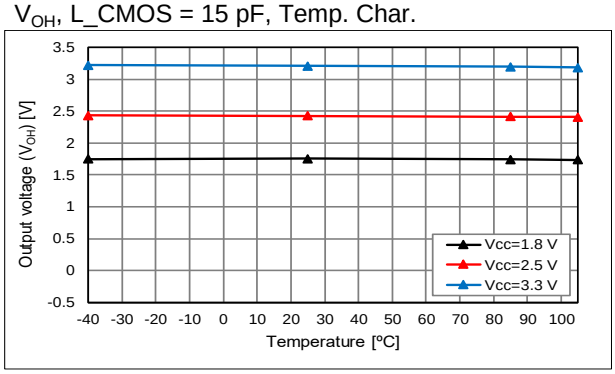



* Output load condition under L CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

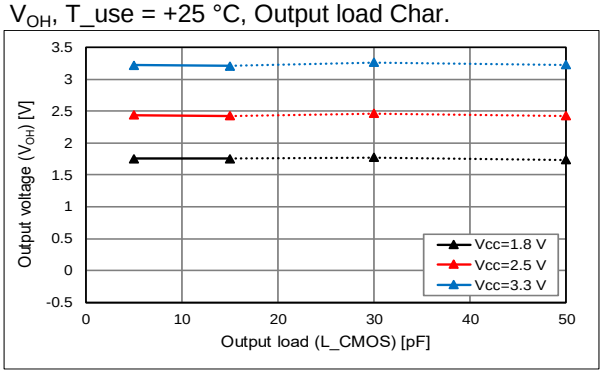
(7-5) Output Voltage [cont'd]

fo = 40 MHz, Rise time/Fall time: B (Fast)

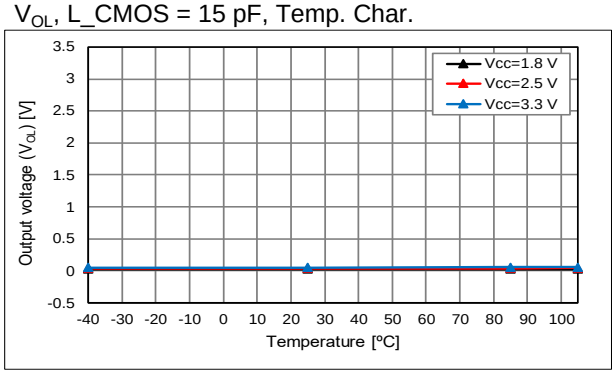
$V_{OH}$, L_CMOS = 15 pF, Temp. Char.



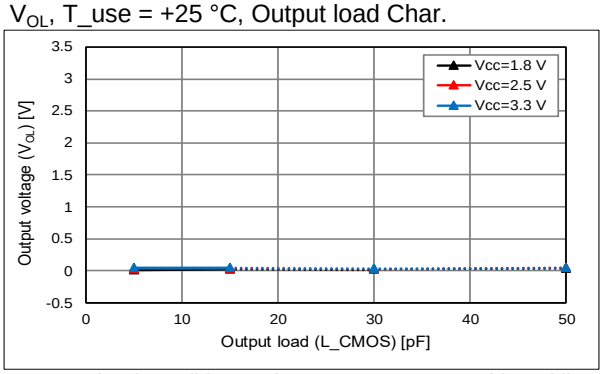

$V_{OH}$, T_use = +25 °C, Output load Char.




$V_{OL}$, L_CMOS = 15 pF, Temp. Char.



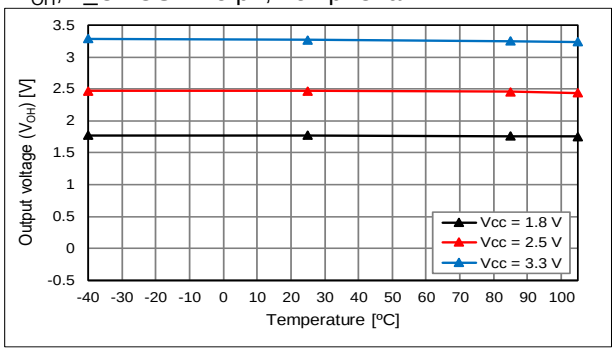

$V_{OL}$, T_use = +25 °C, Output load Char.



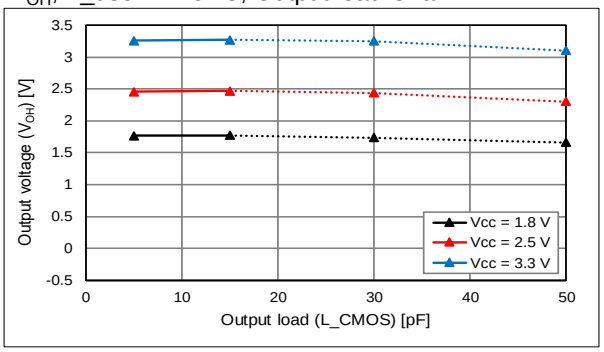

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 60 MHz, Rise time/Fall time: A (Default) & B (Fast)

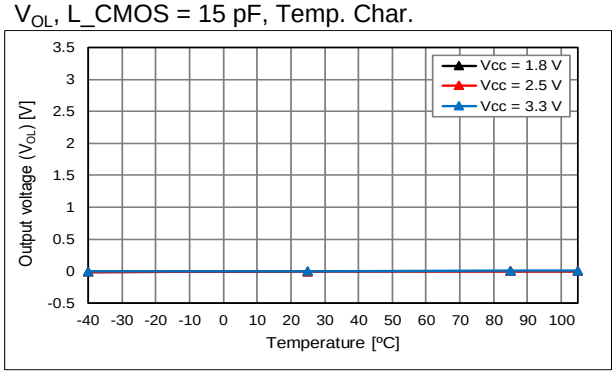
$V_{OH}$, L_CMOS = 15 pF, Temp. Char.



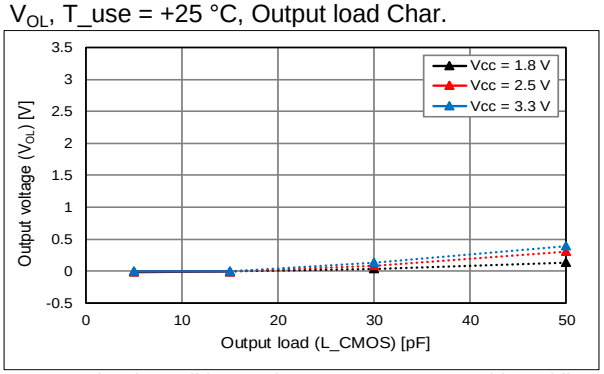

$V_{OH}$, T_use = +25 °C, Output load Char.




$V_{OL}$, L_CMOS = 15 pF, Temp. Char.




$V_{OL}$, T_use = +25 °C, Output load Char.

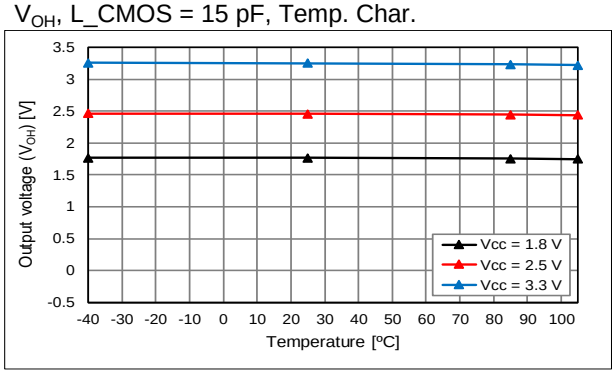



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

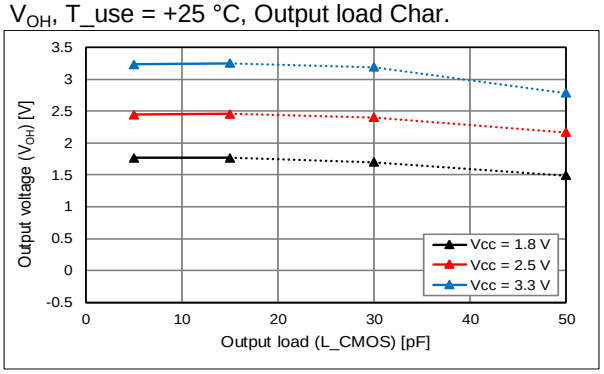
(7-5) Output Voltage [cont'd]

fo = 80 MHz, Rise time/Fall time: A (Default) & B (Fast)

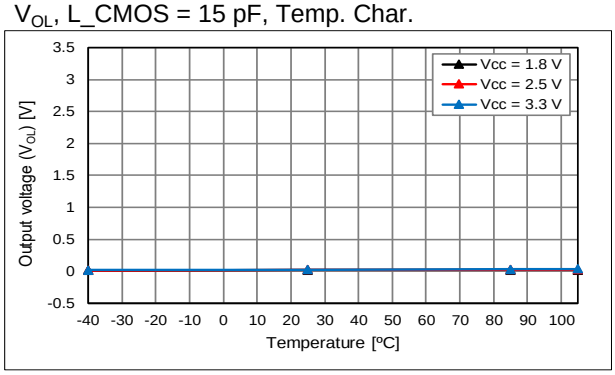
$V_{OH}$, L_CMOS = 15 pF, Temp. Char.



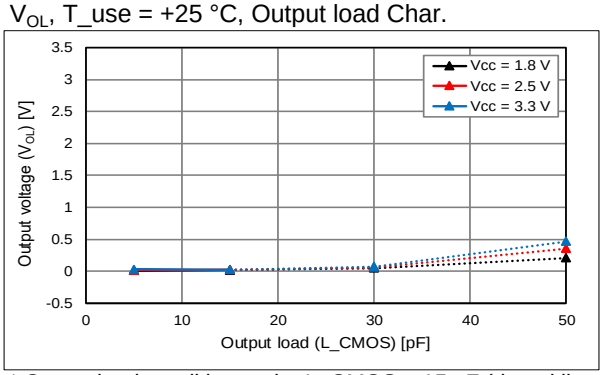

$V_{OH}$, T_use = +25 °C, Output load Char.




$V_{OL}$, L_CMOS = 15 pF, Temp. Char.



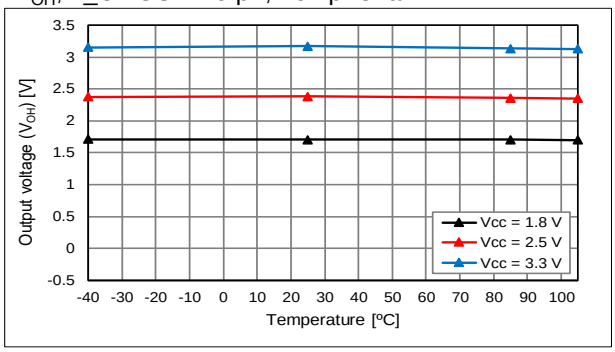

$V_{OL}$, T_use = +25 °C, Output load Char.



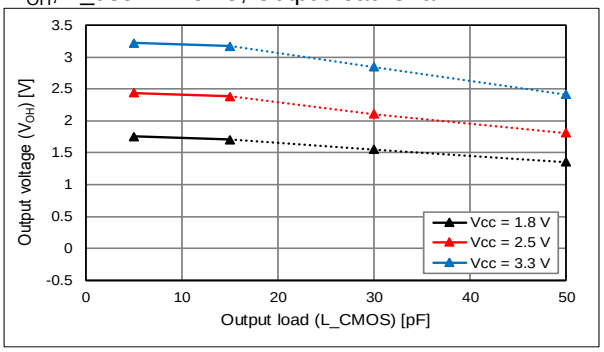

* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

fo = 122.88 MHz, Rise time/Fall time: A (Default) & B (Fast)

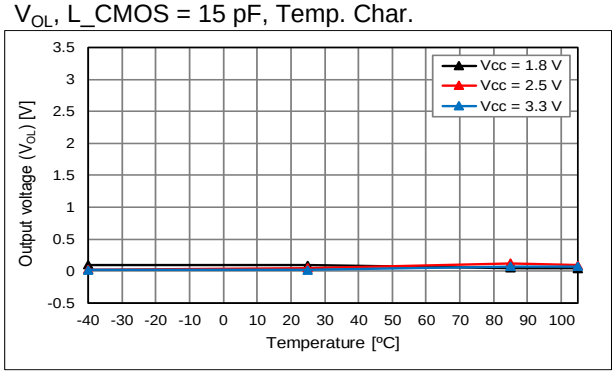
$V_{OH}$, L_CMOS = 15 pF, Temp. Char.



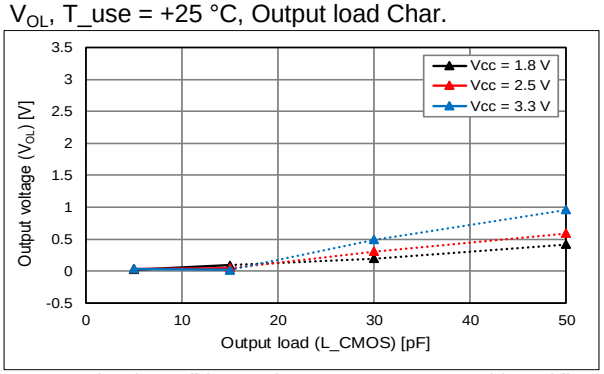

$V_{OH}$, T_use = +25 °C, Output load Char.




$V_{OL}$, L_CMOS = 15 pF, Temp. Char.




$V_{OL}$, T_use = +25 °C, Output load Char.

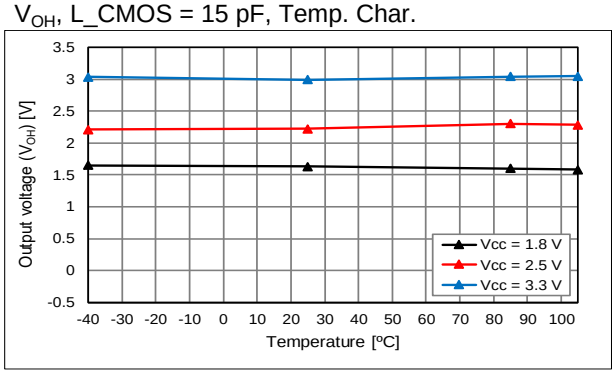



* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

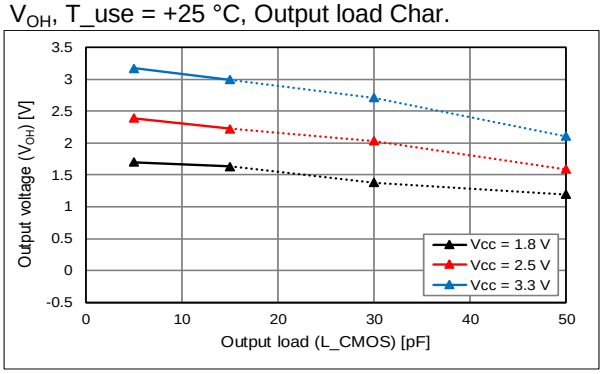
(7-5) Output Voltage [cont'd]

fo = 170 MHz, Rise time/Fall time: A (Default) & B (Fast)

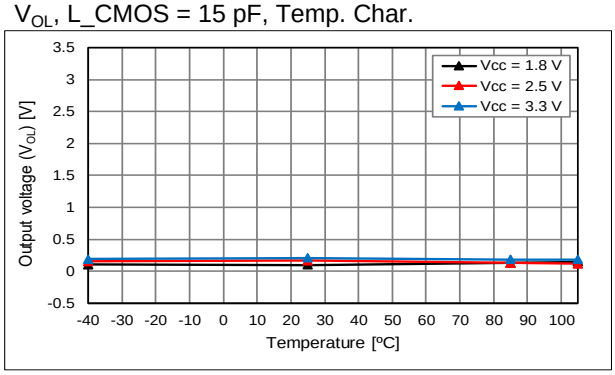
$V_{OH}$, L_CMOS = 15 pF, Temp. Char.



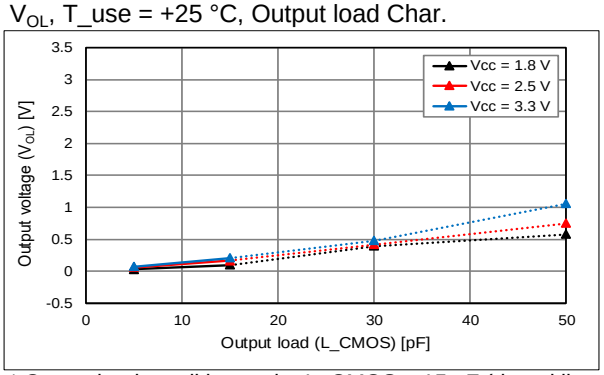

$V_{OH}$, T_use = +25 °C, Output load Char.




$V_{OL}$, L_CMOS = 15 pF, Temp. Char.



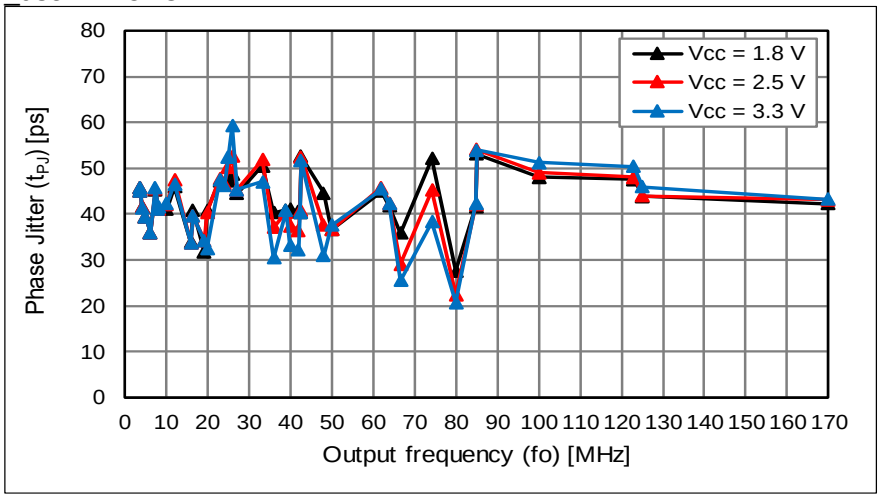

$V_{OL}$, T_use = +25 °C, Output load Char.




* Output load condition under L_CMOS > 15 pF (dotted line area) is not guaranteed, and the data is for reference.

(7-6) Phase Jitter

T_use = +25 °C

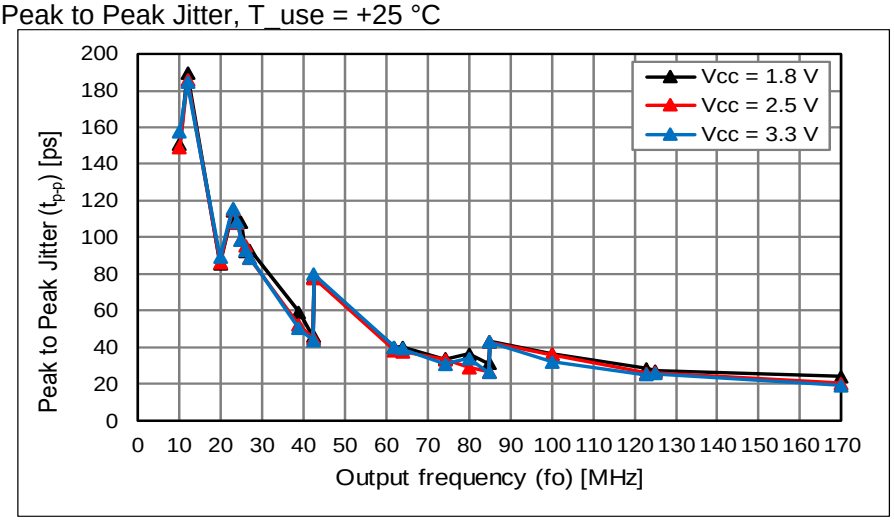



* Offset frequency

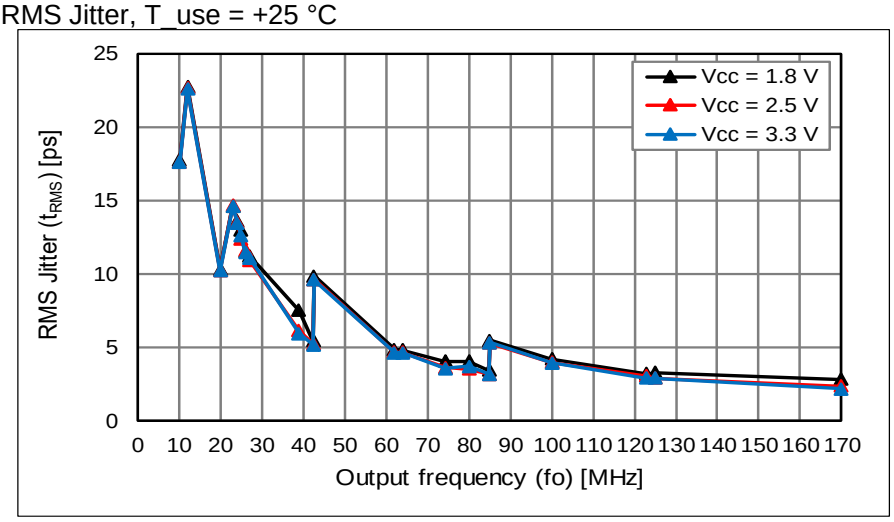
| | |
|---|---|
| fo < 10 MHz: | 12 kHz to 1 MHz |
| 10 MHz ≤ fo < 39 MHz: | 12 kHz to 5 MHz |
| fo ≥ 39 MHz: | 12 kHz to 20 MHz |

(7-7) Jitter

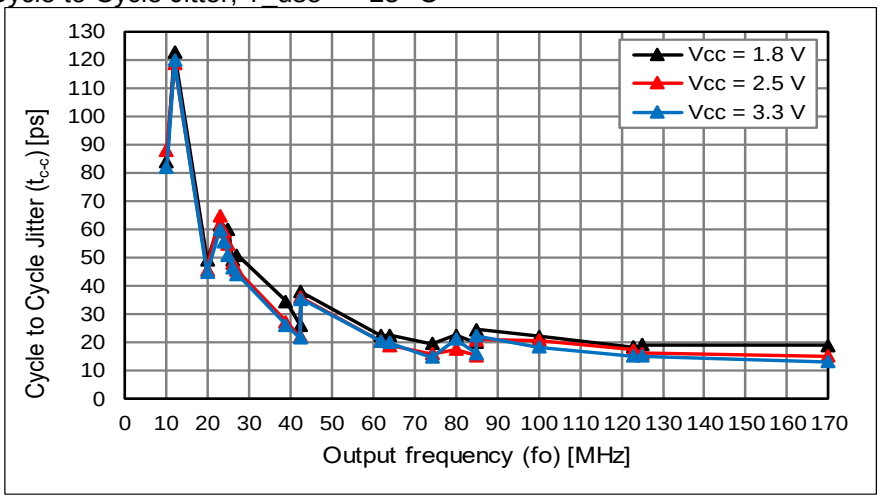
Peak to Peak Jitter, T_use = +25 °C




RMS Jitter, T_use = +25 °C



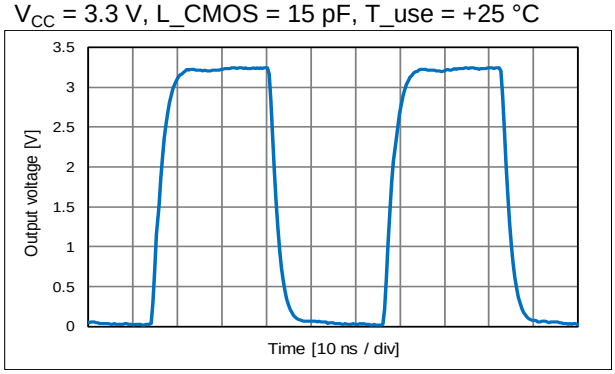

Cycle to Cycle Jitter, T_use = +25 °C



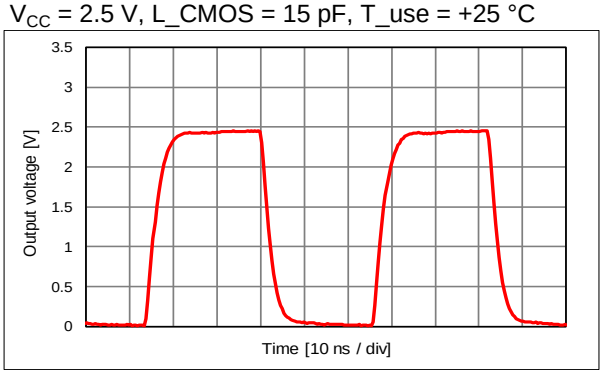
(7-8) Output waveform

fo = 19.2 MHz, Rise time/Fall time: A (Default)

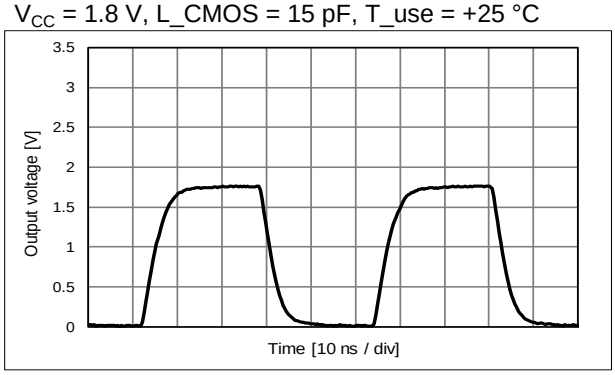
$V_{CC}$ = 3.3 V, L_CMOS = 15 pF, T_use = +25 °C




$V_{CC}$ = 2.5 V, L_CMOS = 15 pF, T_use = +25 °C

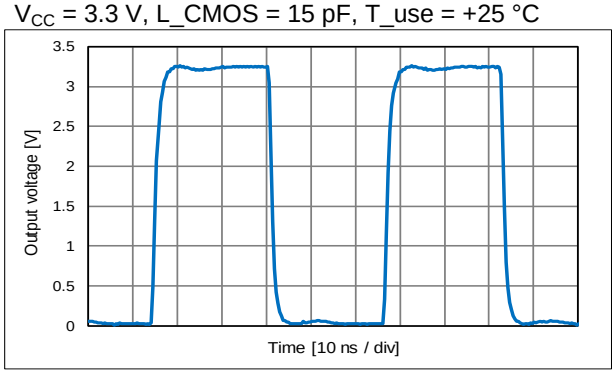



$V_{CC}$ = 1.8 V, L_CMOS = 15 pF, T_use = +25 °C

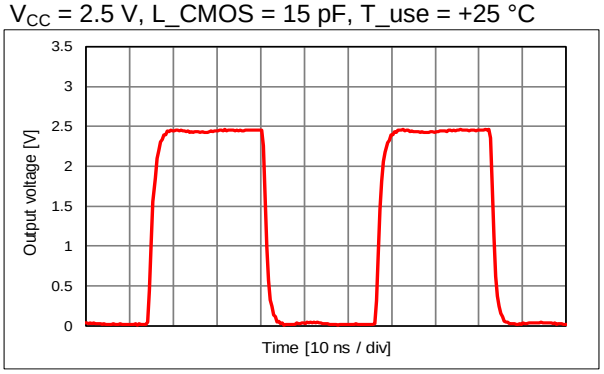



fo = 19.2 MHz, Rise time/Fall time: B (Fast)

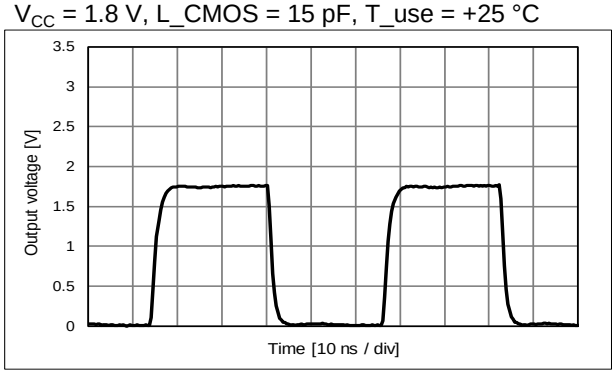
$V_{CC}$ = 3.3 V, L_CMOS = 15 pF, T_use = +25 °C




$V_{CC}$ = 2.5 V, L_CMOS = 15 pF, T_use = +25 °C



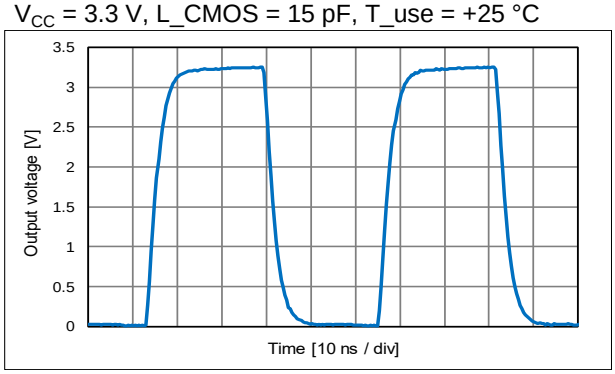

$V_{CC}$ = 1.8 V, L_CMOS = 15 pF, T_use = +25 °C



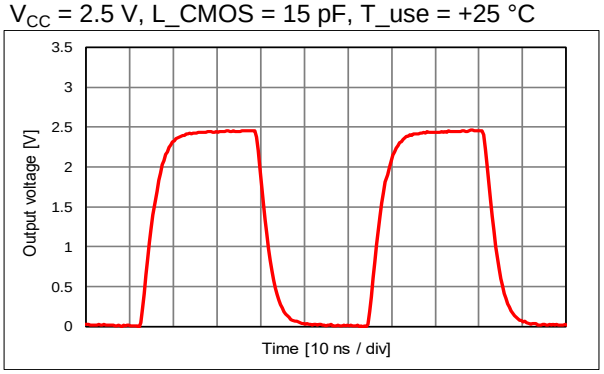
(7-8) Output Waveform [cont'd]

fo = 19.2 MHz, Rise time/Fall time: C (Slow)

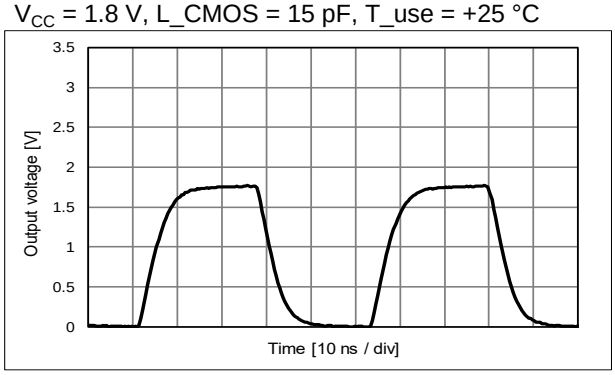
$V_{CC}$ = 3.3 V, L_CMOS = 15 pF, T_use = +25 °C




$V_{CC}$ = 2.5 V, L_CMOS = 15 pF, T_use = +25 °C

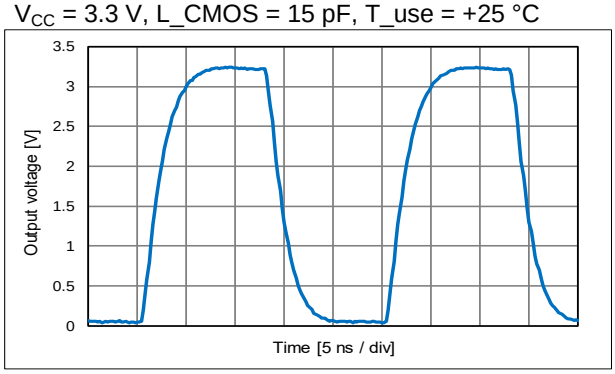



$V_{CC}$ = 1.8 V, L_CMOS = 15 pF, T_use = +25 °C

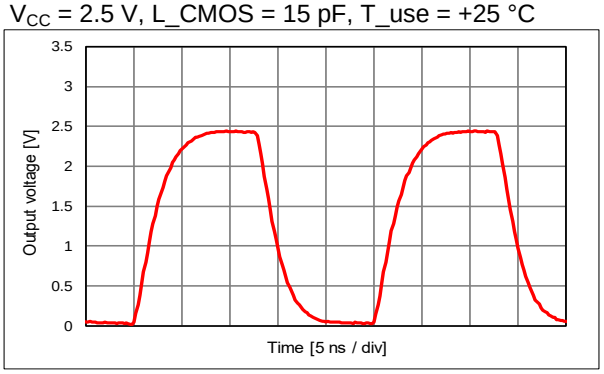



fo = 40 MHz, Rise time/Fall time: A (Default)

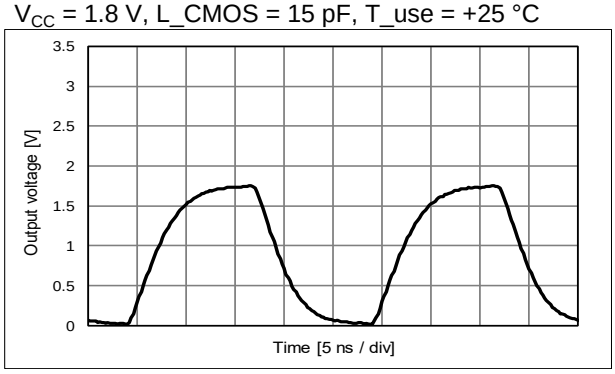
$V_{CC}$ = 3.3 V, L_CMOS = 15 pF, T_use = +25 °C




$V_{CC}$ = 2.5 V, L_CMOS = 15 pF, T_use = +25 °C



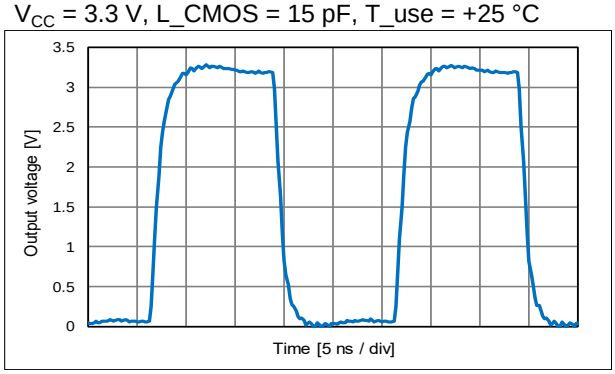

$V_{CC}$ = 1.8 V, L_CMOS = 15 pF, T_use = +25 °C



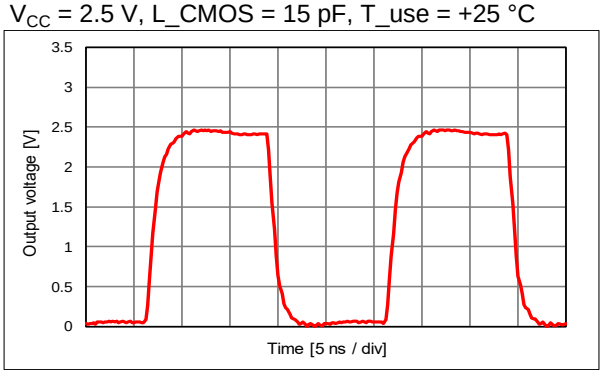
(7-8) Output Waveform [cont'd]

fo = 40 MHz, Rise time/Fall time: B (Fast)

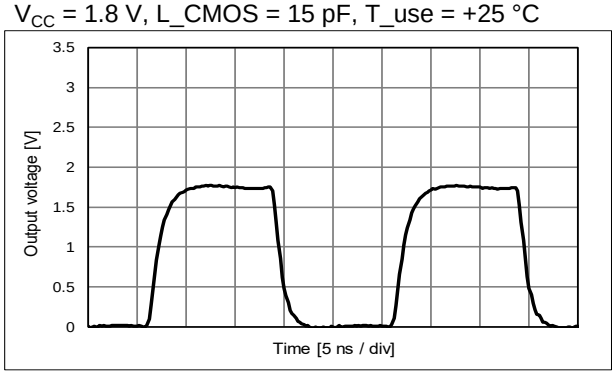
$V_{CC}$ = 3.3 V, L_CMOS = 15 pF, T_use = +25 °C




$V_{CC}$ = 2.5 V, L_CMOS = 15 pF, T_use = +25 °C

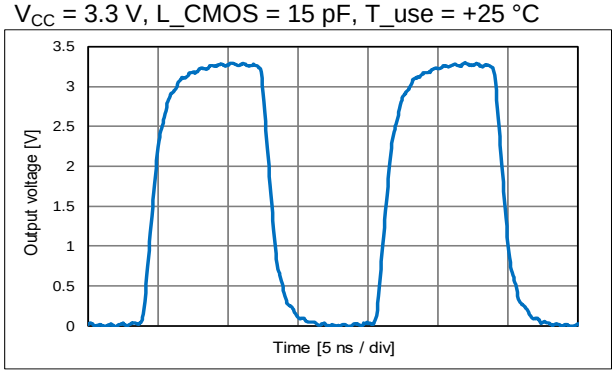



$V_{CC}$ = 1.8 V, L_CMOS = 15 pF, T_use = +25 °C

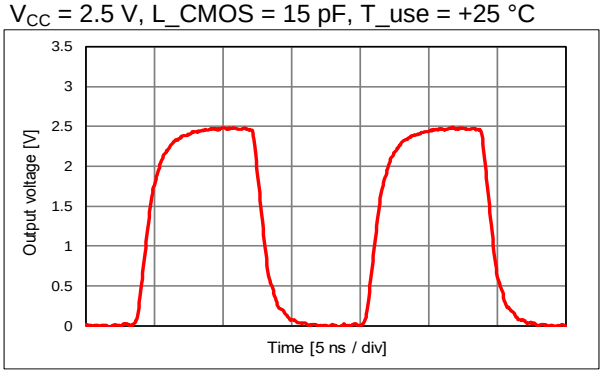



fo = 60 MHz, Rise time/Fall time: A (Default) & B (Fast)

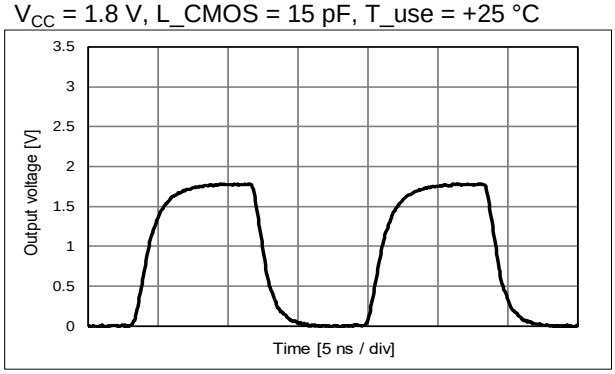
$V_{CC}$ = 3.3 V, L_CMOS = 15 pF, T_use = +25 °C




$V_{CC}$ = 2.5 V, L_CMOS = 15 pF, T_use = +25 °C



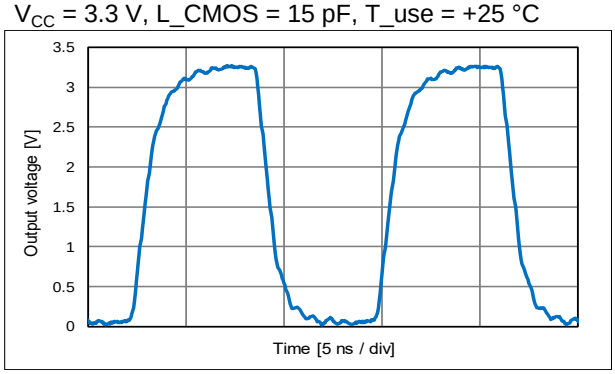

$V_{CC}$ = 1.8 V, L_CMOS = 15 pF, T_use = +25 °C



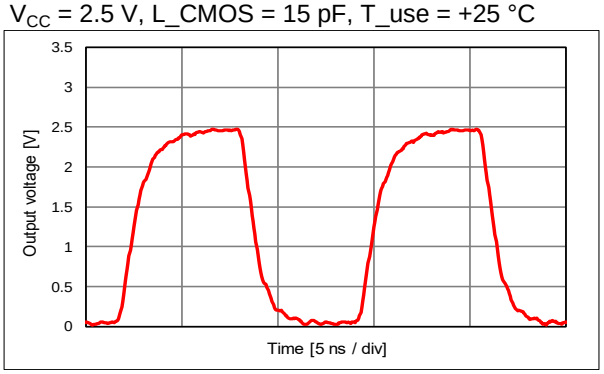
(7-8) Output Waveform [cont'd]

fo = 80 MHz, Rise time/Fall time: A (Default) & B (Fast)

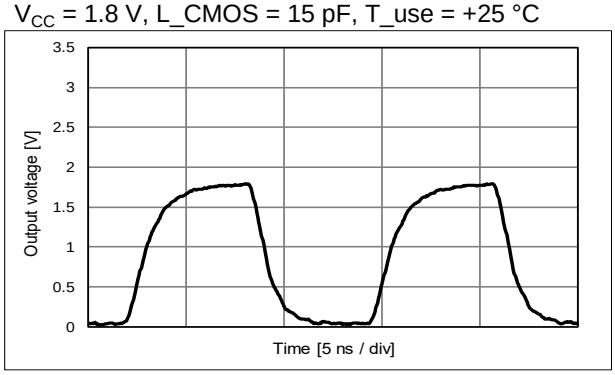
$V_{CC}$ = 3.3 V, L_CMOS = 15 pF, T_use = +25 °C




$V_{CC}$ = 2.5 V, L_CMOS = 15 pF, T_use = +25 °C

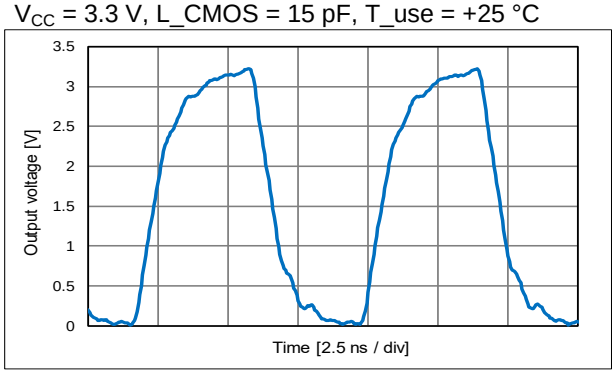



$V_{CC}$ = 1.8 V, L_CMOS = 15 pF, T_use = +25 °C

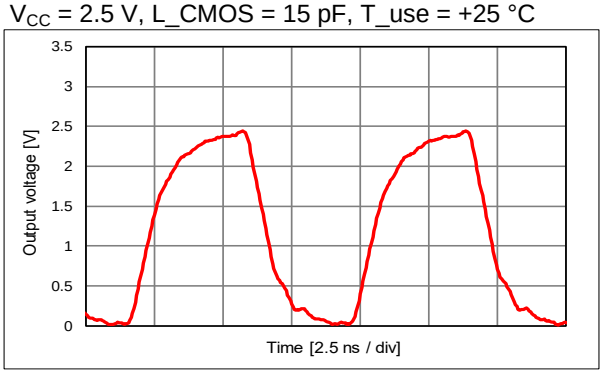



fo = 122.88 MHz, Rise time/Fall time: A (Default) & B (Fast)

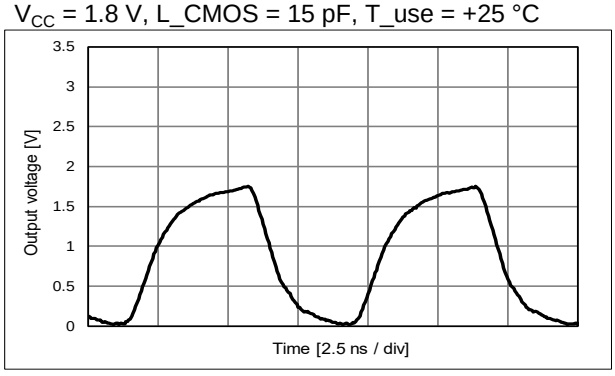
$V_{CC}$ = 3.3 V, L_CMOS = 15 pF, T_use = +25 °C




$V_{CC}$ = 2.5 V, L_CMOS = 15 pF, T_use = +25 °C



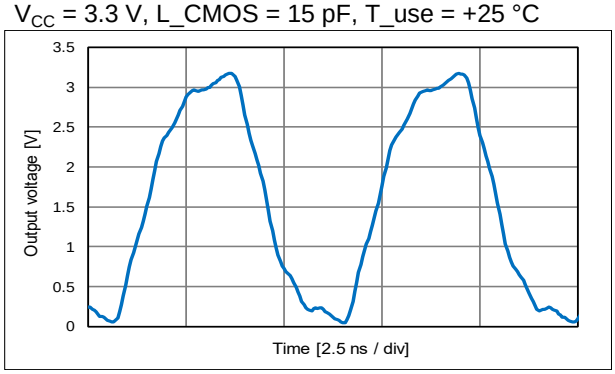

$V_{CC}$ = 1.8 V, L_CMOS = 15 pF, T_use = +25 °C



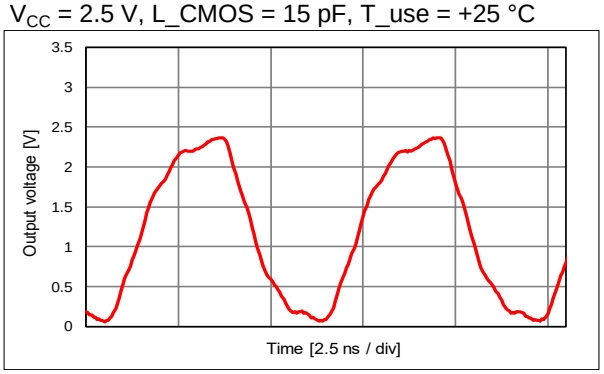
(7-8) Output Waveform [cont'd]

fo = 170 MHz, Rise time/Fall time: A (Default) & B (Fast)

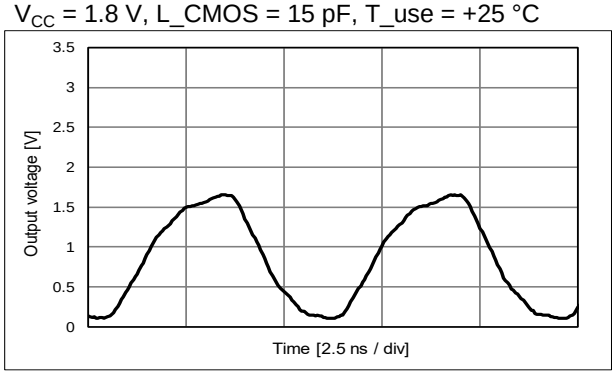
$V_{CC}$ = 3.3 V, L_CMOS = 15 pF, T_use = +25 °C




$V_{CC}$ = 2.5 V, L_CMOS = 15 pF, T_use = +25 °C

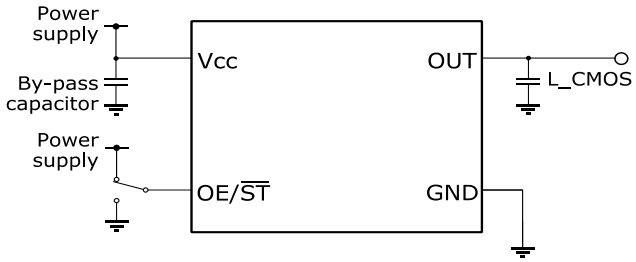



$V_{CC}$ = 1.8 V, L_CMOS = 15 pF, T_use = +25 °C

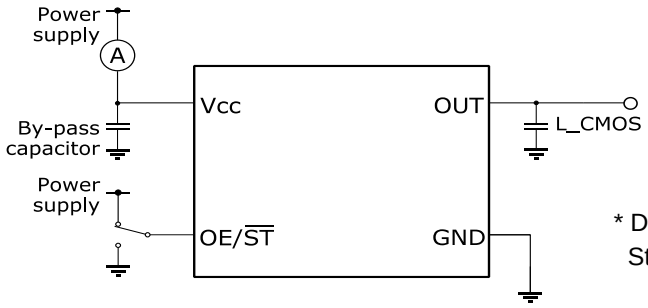


[ 8 ] Test Circuit

(8-1) Waveform Observation

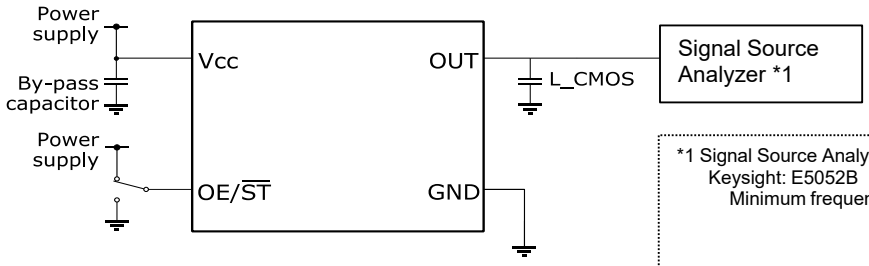



(8-2) Current Consumption Test



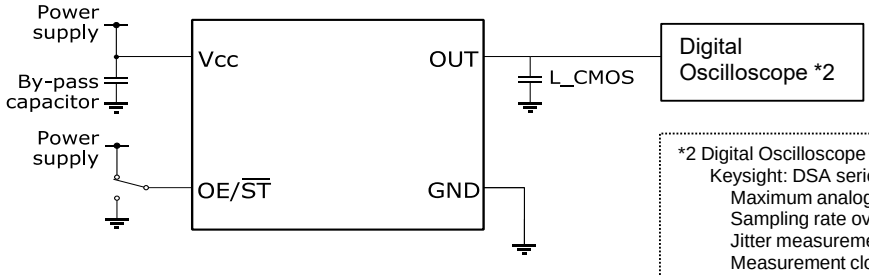

* Disable current test should be OE = GND.
Stand-by current test should be $\overline{ST}$ = GND.

(8-3) Phase Jitter




*1 Signal Source Analyzer
Keysight: E5052B
Minimum frequency: 10 MHz

(8-4) Jitter (Peak to Peak, RMS, Cycle to Cycle)




*2 Digital Oscilloscope
Keysight: DSA series
Maximum analog bandwidth to 1 GHz
Sampling rate over 40 GHz/s
Jitter measurement software tool: EZJIT+
Measurement clock cycle > 50 000

(8-5) Condition

(1) Oscilloscope

The bandwidth should be minimum 5 times wider than measurement frequency
The probe ground should be placed closely to the test point and the lead length should be as short as possible

* It is recommended to use miniature socket. (Don't use earth lead.)

(2) L_CMOS includes probe capacitance.

(3) A 0.1 µF bypass capacitor should be connected between $V_{CC}$ and GND pins located close to the device

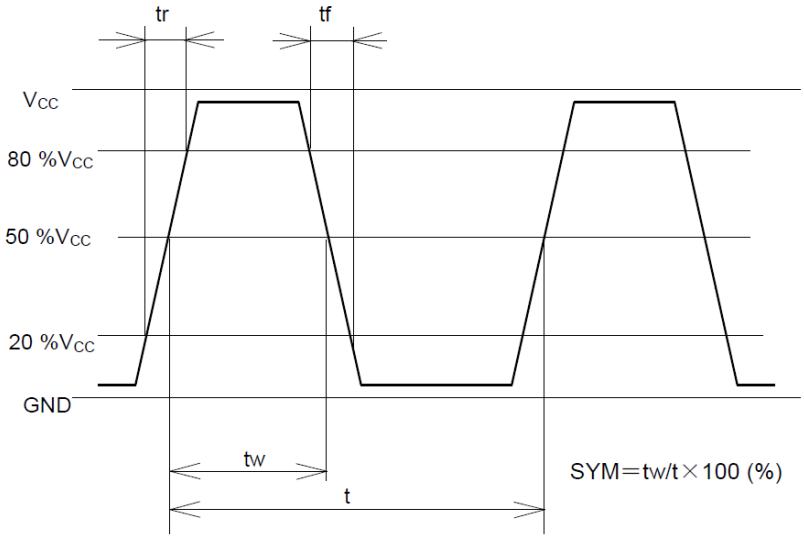
(4) Use a current meter with a low internal impedance

(5) Power Supply

Power supply startup time (0 %$V_{CC}$ → 90 %$V_{CC}$) should be between 5 µs and 500 ms
Power supply impedance should be as low as possible and GND line should be as short as possible

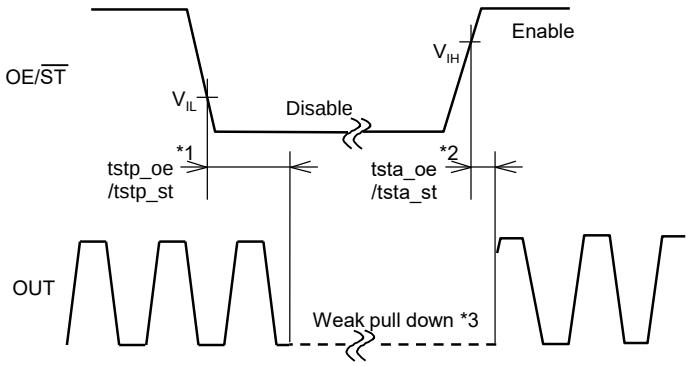
(8-6) Timing Chart

(1) Output Waveform and Level




(2) OE/$\overline{ST}$ Function and Timing

| OE/$\overline{ST}$ terminal | Osc. circuit | Output status |
|---|---|---|
| "H" | Oscillation | Specified frequency: Enable |
| "L" | OE: Oscillation | Low (Weak pull down*3): Disable |
| | $\overline{ST}$: Oscillation stop | |




*1 The period from OE/$\overline{ST}$ = $V_{IL}$ to OUT = Low (weak pull down) (Disable)

*2 The period from OE/$\overline{ST}$ = $V_{IH}$ to OUT = Enable

*3 Pulled down with Output pull down resistance ($R_{DN}$)

* Judging the start of output when output waveform is observed.

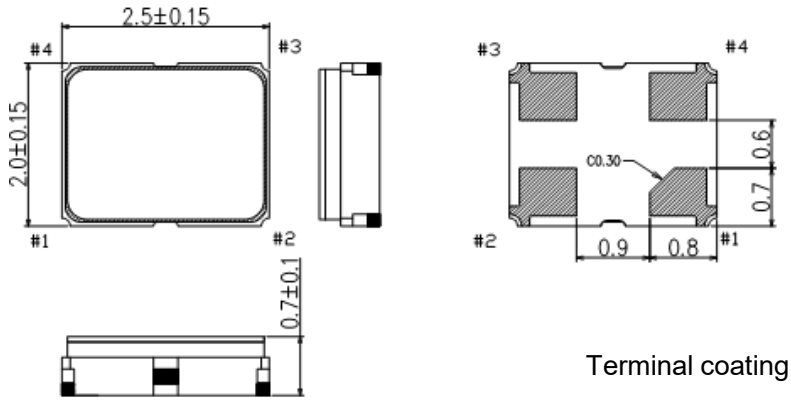
* OE/$\overline{ST}$ terminal voltage level should not exceed supply voltage when using OE/$\overline{ST}$ function.
Please note that OE/$\overline{ST}$ rise time should not exceed supply voltage rise time at the start-up.

* Please do not use the OE/$\overline{ST}$ terminal in the open state.
Typically the output will be enable when OE/ST is open state, but the input pull resistance is large and OE/$\overline{ST}$ terminal may drop to "L" level and be disable due to noise or leakage current.

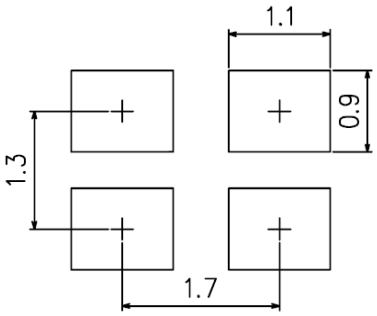
[ 9 ] Outline Drawing and Recommended Footprint

(9-1) SG-8101CG

Units: mm




Terminal coating : Au plating




For stable operation, it is recommended that 0.1 µF bypass capacitor should be connected between $V_{CC}$ and GND and placed as close to the $V_{CC}$ pin as possible.

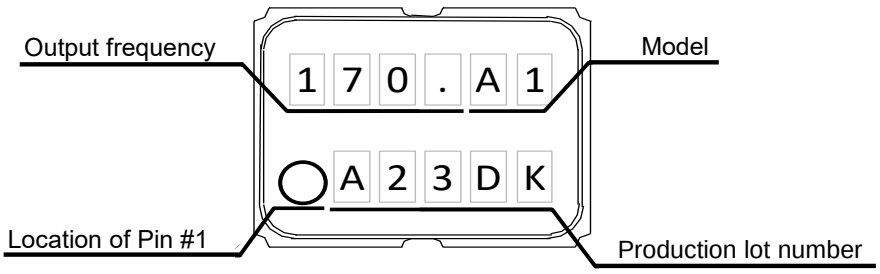
Reference Weight Typ.: 13 mg

Terminal Assignment

| Pin # | Connection | Function | | |
|---|---|---|---|---|
| #1 | OE | OE terminal | | |
| | | OE function | Osc. Circuit | Output |
| | | "H" * | Oscillation | Specified frequency: Enable |
| | | "L" | Oscillation | Low (weak pull down): Disable |
| | $\overline{ST}$ | $\overline{ST}$ terminal | | |
| | | $\overline{ST}$ function | Osc. Circuit | Output |
| | | "H" * | Oscillation | Specified frequency: Enable |
| | | "L" | Oscillation stop | Low (weak pull down): Disable |
| #2 | GND | GND terminal | | |
| #3 | OUT | Output terminal | | |
| #4 | $V_{CC}$ | $V_{CC}$ terminal | | |

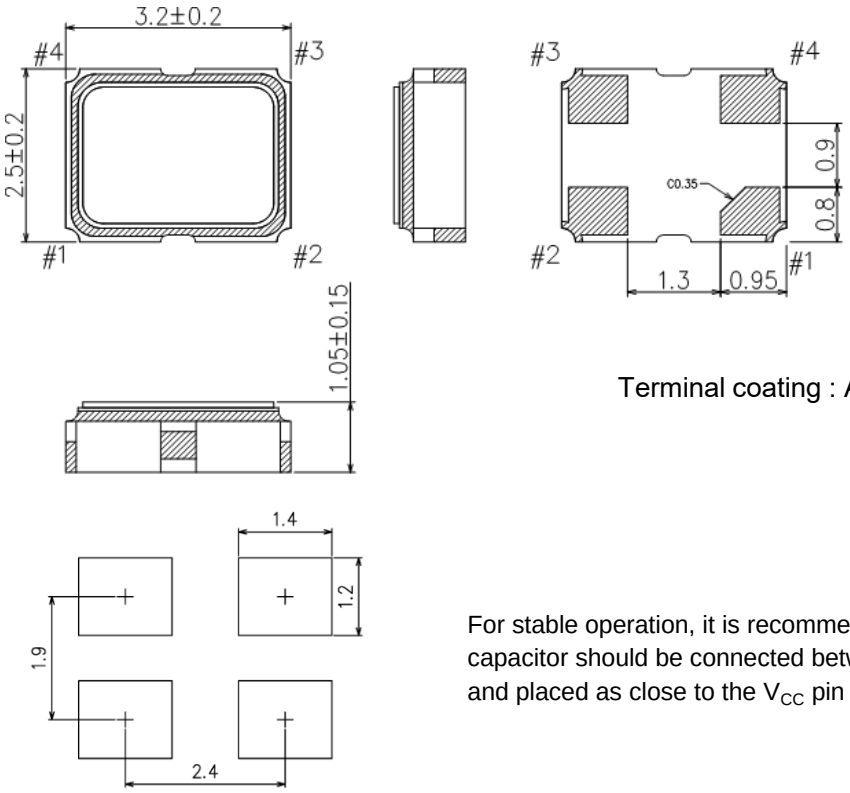
* Please do not use the OE/$\overline{ST}$ terminal in the open state.

Marking



(9-2) SG-8101CE

Units: mm




Terminal coating : Au plating

For stable operation, it is recommended that 0.1 µF bypass capacitor should be connected between $V_{CC}$ and GND and placed as close to the $V_{CC}$ pin as possible.

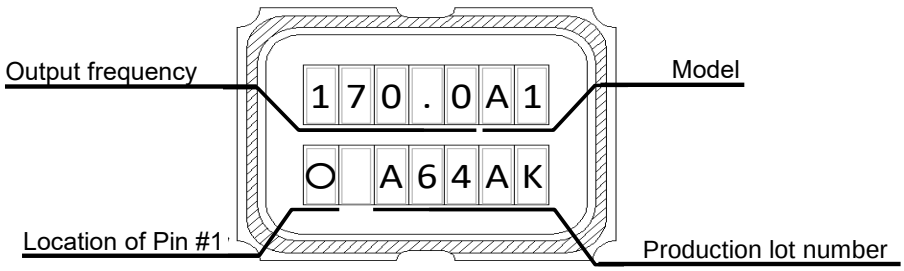
Reference Weight Typ.: 25 mg

Terminal Assignment

| Pin # | Connection | Function | | |
|---|---|---|---|---|
| #1 | OE | OE terminal | | |
| | | OE function | Osc. Circuit | Output |
| | | "H" * | Oscillation | Specified frequency: Enable |
| | | "L" | Oscillation | Low (weak pull down): Disable |
| | $\overline{ST}$ | $\overline{ST}$ terminal | | |
| | | $\overline{ST}$ function | Osc. Circuit | Output |
| | | "H" * | Oscillation | Specified frequency: Enable |
| | | "L" | Oscillation stop | Low (weak pull down): Disable |
| #2 | GND | GND terminal | | |
| #3 | OUT | Output terminal | | |
| #4 | $V_{CC}$ | $V_{CC}$ terminal | | |

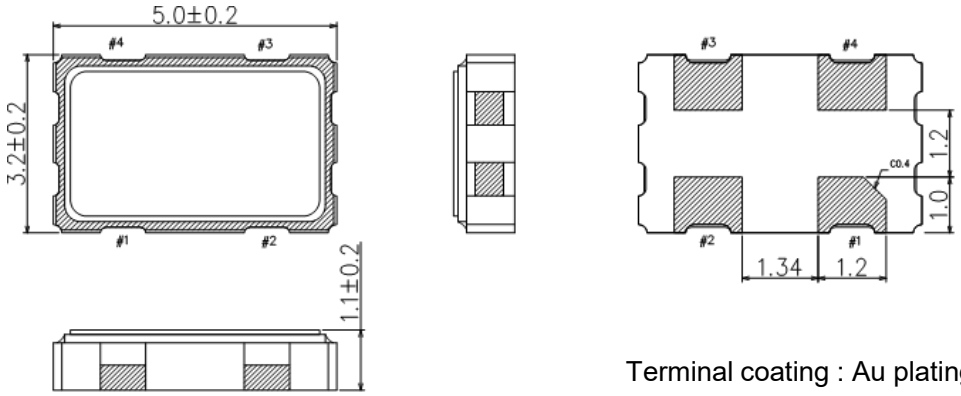
* Please do not use the OE/$\overline{ST}$ terminal in the open state.

Marking

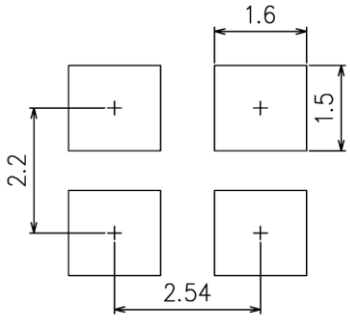


(9-4) SG-8101CB

Units: mm




Terminal coating : Au plating




For stable operation, it is recommended that 0.1 µF bypass capacitor should be connected between $V_{CC}$ and GND and placed as close to the $V_{CC}$ pin as possible.

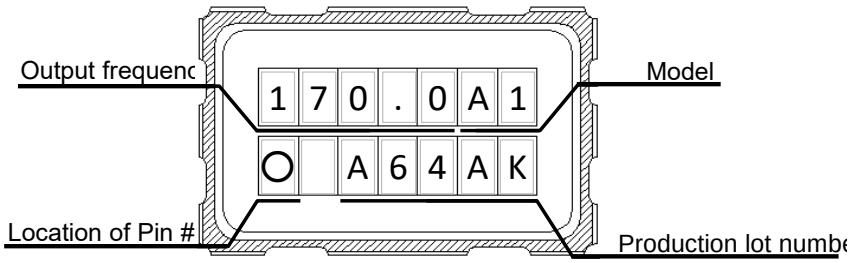
Reference Weight Typ.: 51 mg

Terminal Assignment

| Pin # | Connection | Function | | |
|---|---|---|---|---|
| #1 | OE | OE terminal | | |
| | | OE function | Osc. Circuit | Output |
| | | "H" * | Oscillation | Specified frequency: Enable |
| | | "L" | Oscillation | Low (weak pull down): Disable |
| | $\overline{ST}$ | $\overline{ST}$ terminal | | |
| | | $\overline{ST}$ function | Osc. Circuit | Output |
| | | "H" * | Oscillation | Specified frequency: Enable |
| | | "L" | Oscillation stop | Low (weak pull down): Disable |
| #2 | GND | GND terminal | | |
| #3 | OUT | Output terminal | | |
| #4 | $V_{CC}$ | $V_{CC}$ terminal | | |

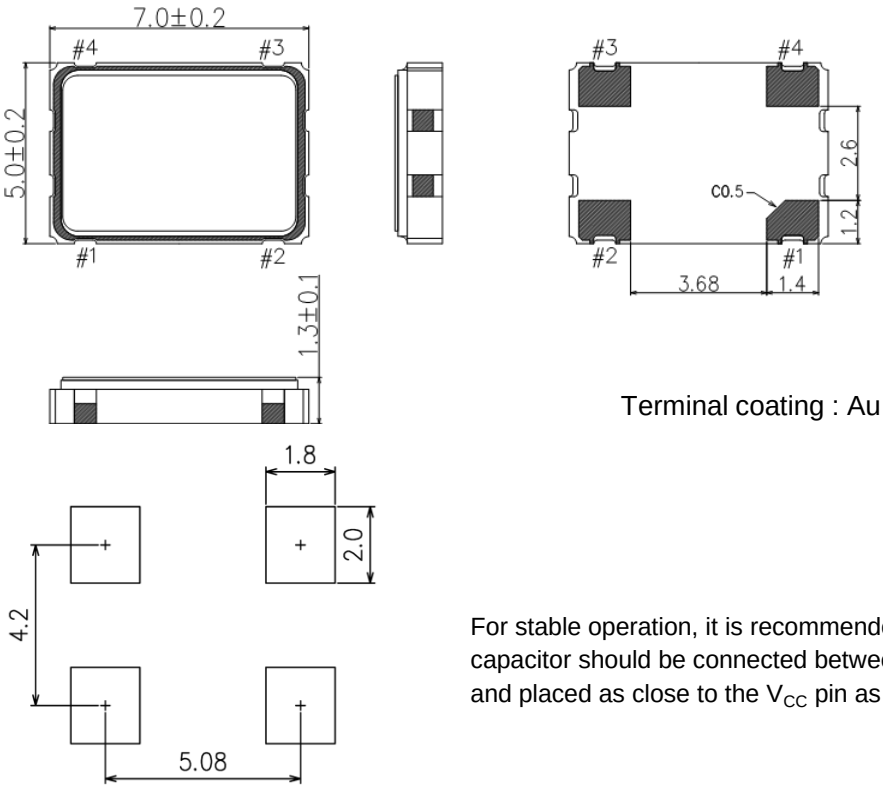
* Please do not use the OE/$\overline{ST}$ terminal in the open state.

Marking



(9-5) SG-8101CA

Units: mm




Terminal coating : Au plating




For stable operation, it is recommended that 0.1 µF bypass capacitor should be connected between $V_{CC}$ and GND and placed as close to the $V_{CC}$ pin as possible.

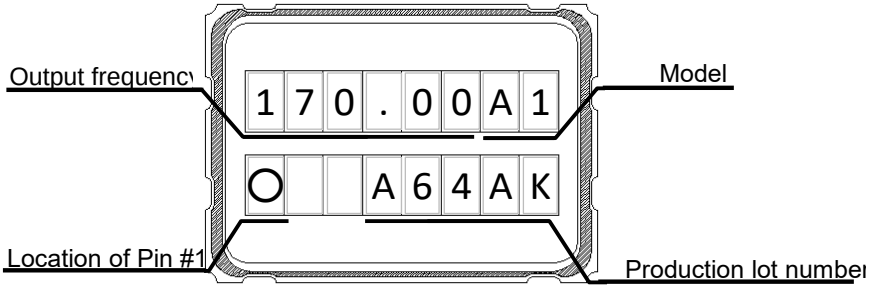
Reference Weight Typ.: 143 mg

Terminal Assignment

| Pin # | Connection | Function | | |
|---|---|---|---|---|
| #1 | OE | OE terminal | | |
| | | OE function | Osc. Circuit | Output |
| | | "H" * | Oscillation | Specified frequency: Enable |
| | | "L" | Oscillation | Low (weak pull down): Disable |
| | $\overline{ST}$ | $\overline{ST}$ terminal | | |
| | | $\overline{ST}$ function | Osc. Circuit | Output |
| | | "H" * | Oscillation | Specified frequency: Enable |
| | | "L" | Oscillation stop | Low (weak pull down): Disable |
| #2 | GND | GND terminal | | |
| #3 | OUT | Output terminal | | |
| #4 | $V_{CC}$ | $V_{CC}$ terminal | | |

* Please do not use the OE/$\overline{ST}$ terminal in the open state.

Marking

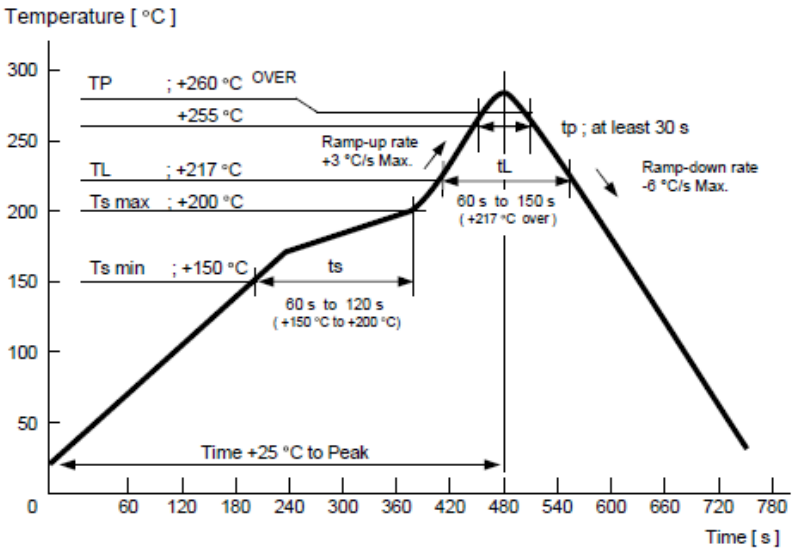


[ 10 ] Moisture Sensitivity Level

| Parameter | Specification | Conditions |
|---|---|---|
| MSL | LEVEL 1 | IPC/JEDEC J-STD-020D.1 |

[ 11 ] Reflow Profiles

IPC/JEDEC J-STD-020D.1



[ 12 ] Packing Information

(12-1) SG-8101CG

(1) Packing Quantity

The last two digits of the Product Number (X1G005181xxxx**xx**) are a code that defines the packing quantity. The standard is "00" for a 3 000 pcs/Reel.

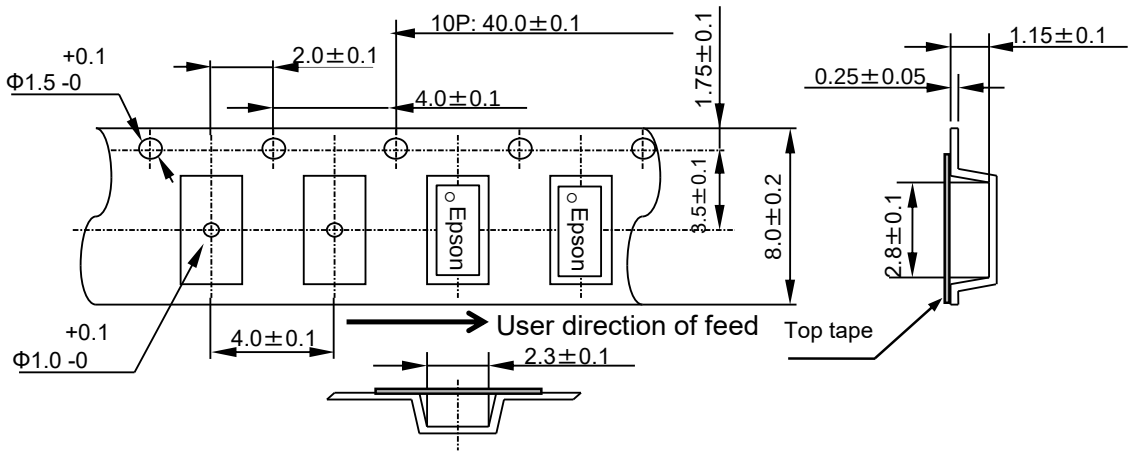
(2) Taping Specification

Subject to EIA-481, IEC-60286 and JIS C0806

1) Tape Dimensions

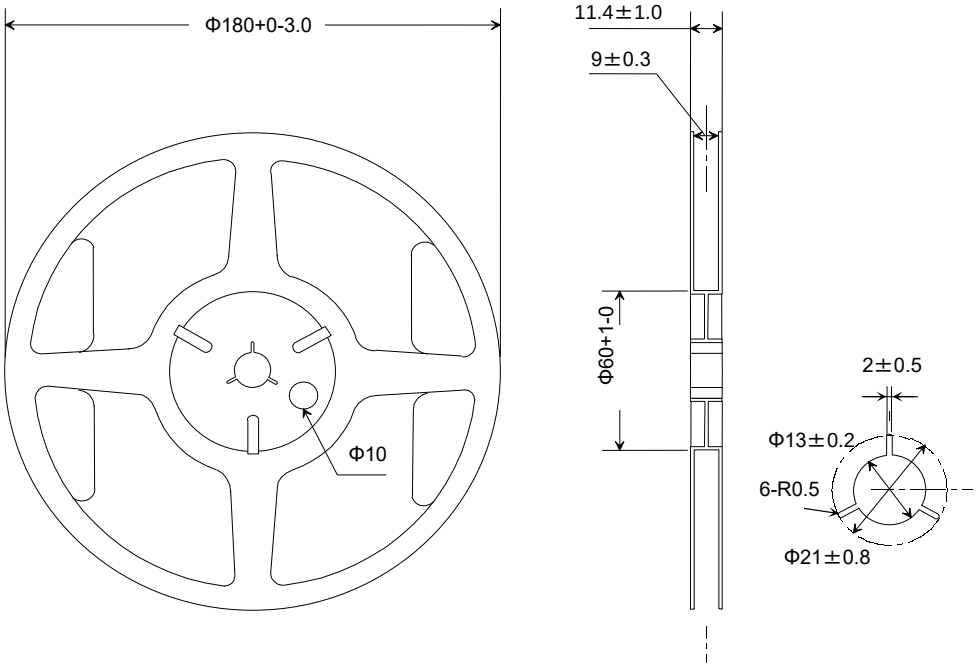
Carrier Tape Material: PS (Polystyrene)

Top Tape Material: PET (Polyethylene Terephthalate) + PE (Polyethylene) Units: mm




2) Reel Dimensions

Reel Material: PS (Polystyrene) Units: mm




3) Storage Environment

We recommend to keep less than +30 °C and 85 %RH of humidity in a packed condition, and to use it less than 6 months after delivery.

(12-2) SG-8101CE

(1) Packing Quantity

The last two digits of the Product Number (X1G005221xxxx**xx**) are a code that defines the packing quantity. The standard is "00" for a 2 000 pcs/Reel.

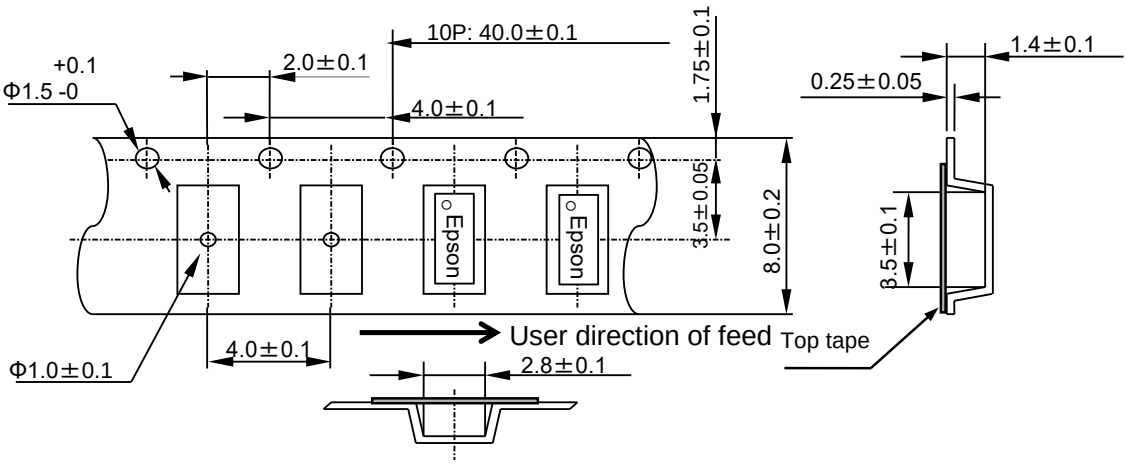
(2) Taping Specification

Subject to EIA-481, IEC-60286 and JIS C0806

1) Tape Dimensions

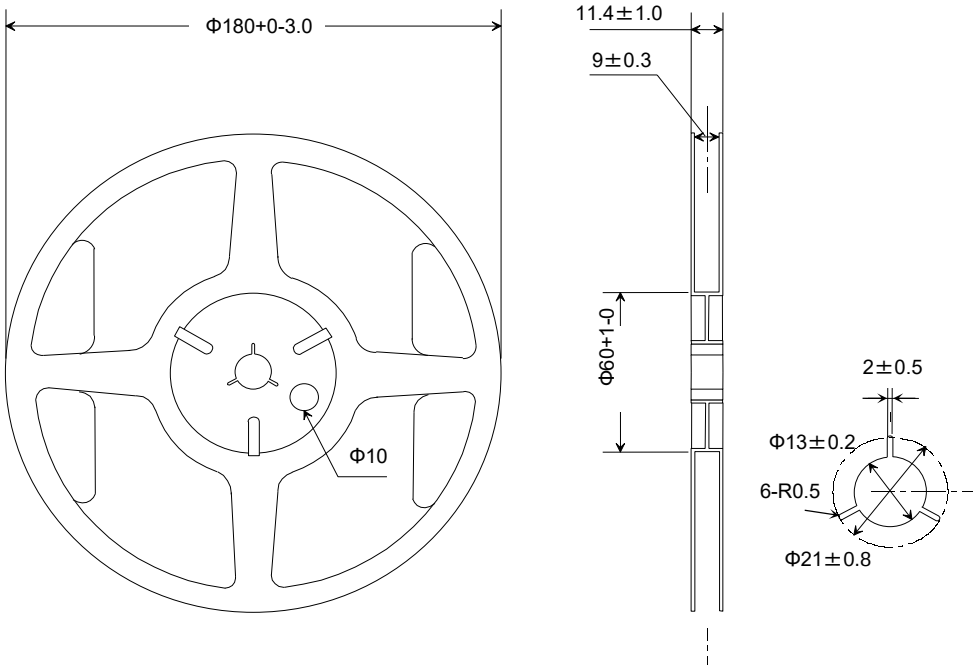
Carrier Tape Material: PS (Polystyrene)

Top Tape Material: PET (Polyethylene Terephthalate) + PE (Polyethylene) Units: mm




2) Reel Dimensions

Reel Material: PS (Polystyrene) Units: mm




3) Storage Environment

We recommend to keep less than +30 °C and 85 %RH of humidity in a packed condition, and to use it less than 6 months after delivery.

(12-3) SG-8101CB

(1) Packing Quantity

The last two digits of the Product Number (X1G005201xxxx**xx**) are a code that defines the packing quantity. The standard is "00" for a 1 000 pcs/Reel.

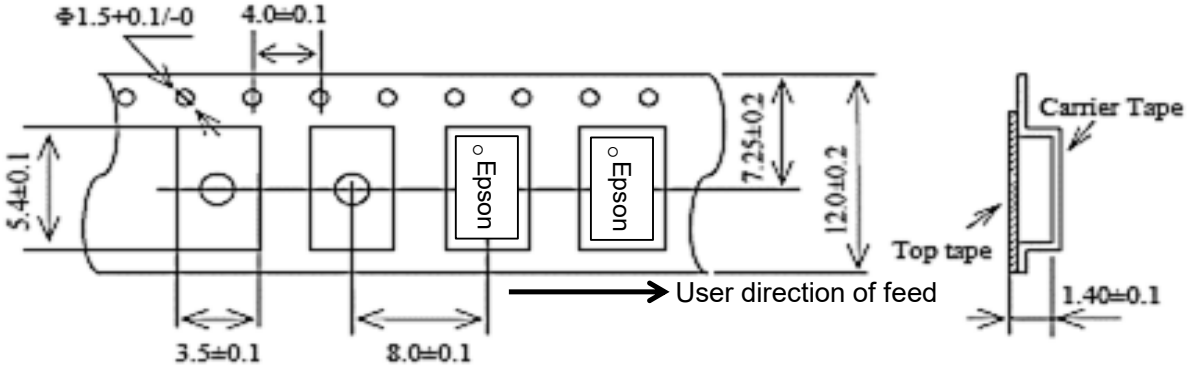
(2) Taping Specification

Subject to EIA-481 & IEC-60286

1) Tape Dimensions

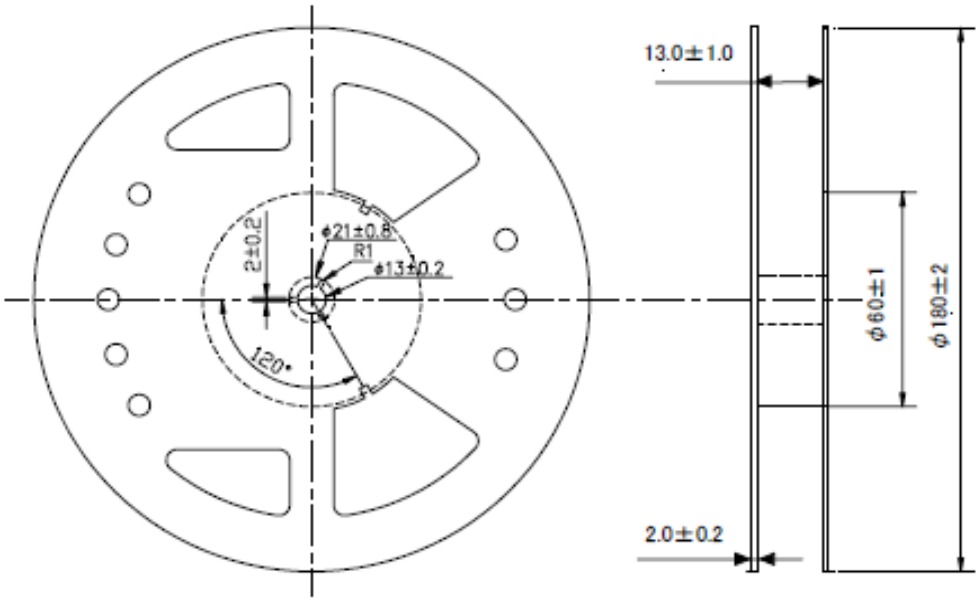
Carrier Tape Material: PS (Polystyrene)

Top Tape Material: PET (Polyethylene Terephthalate) Units: mm




2) Reel Dimensions

Reel Material: PS (Polystyrene) Units: mm




3) Storage Environment

We recommend to keep less than +30 °C and 85 %RH of humidity in a packed condition, and to use it less than 6 months after delivery.

(12-4) SG-8101CA

(1) Packing Quantity

The last two digits of the Product Number (X1G005191xxxx**xx**) are a code that defines the packing quantity. The standard is "00" for a 1 000 pcs/Reel.

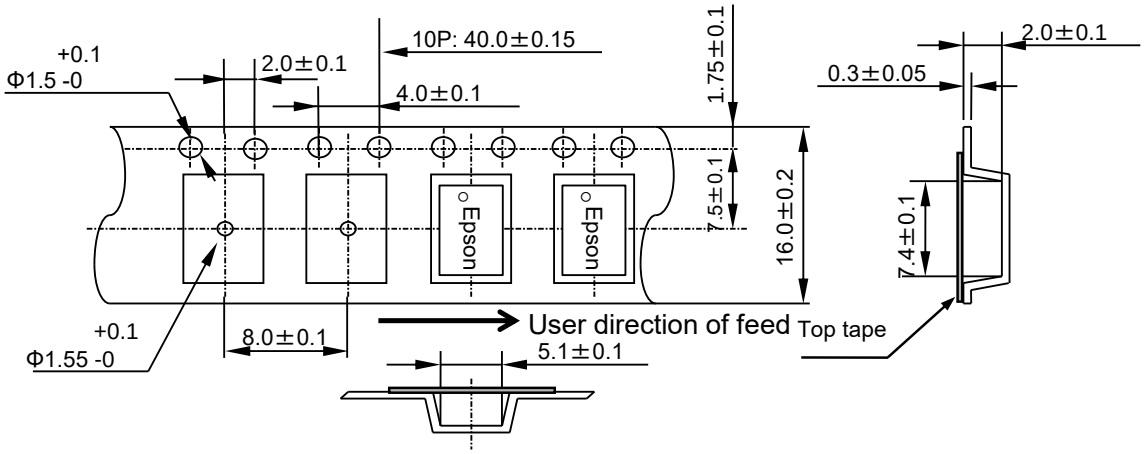
(2) Taping Specification

Subject to EIA-481 & IEC-60286

1) Tape Dimensions

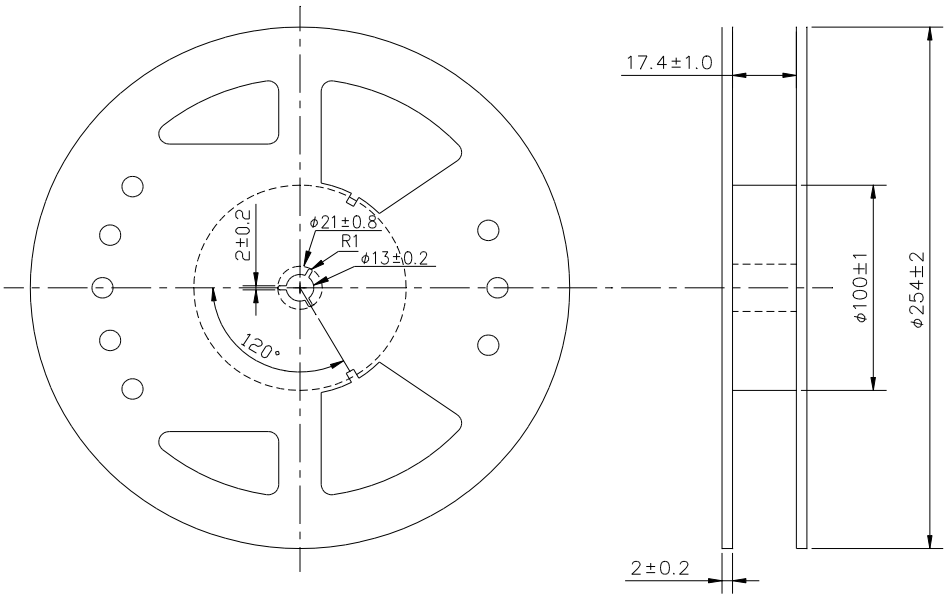
Carrier Tape Material: PS (Polystyrene)

Top Tape Material: PET (Polyethylene Terephthalate) Units: mm




2) Reel Dimensions

Reel Material: PS (Polystyrene) Units: mm




3) Storage Environment

We recommend to keep less than +30 °C and 85 %RH of humidity in a packed condition, and to use it less than 6 months after delivery.

## [ 13 ] Handling Precautions

Prior to using this product, please carefully read the section entitled “Precautions” on our Web site (https://www5.epsondevice.com/en/information/#precaution) for instructions on how to handle and use the product properly to ensure optimal performance of the product in your equipment.
Before using the product under any conditions other than those specified therein, please consult with us to verify and confirm that the performance of the product will not be negatively affected by use under such conditions.
In addition to the foregoing precautions, in order to avoid the deteriorating performance of the product, we strongly recommend that you DO NOT use the product under ANY of the following conditions:

(1) Do not expose this product to excessive mechanical shock or vibration.
(2) This product can be damaged by mechanical shock during the soldering process depending on the equipment used, process conditions, and any impact forces experienced. Always follow appropriate procedures, particularly when changing the assembly process in any way and be sure to follow applicable process qualification standards before starting production.
(3) These devices are sensitive to ESD, use appropriate precautions during handling, assembly, test, shipment, and installation.
(4) The use of ultrasonic technology for cleaning, bonding, etc. can damage the Xtal unit inside this product. Please carefully check for this consideration before using ultrasonic equipment for volume production with this product.
(5) Noise and ripple on the power supply may have undesirable affects on operation and cause degradation of phase noise characteristics. Evaluate the operation of this device with appropriate power supplies carefully before use.
(6) When applying power, ensure that the supply voltage increases monotonically for proper operation. On power down, do not reapply power until the supplies, bypass capacitors, and any bulk capacitors are completely discharged since that may cause the unit to malfunction.
(7) Aging specifications are estimated from environmental reliability tests and expected frequency variation over time. They do not provide a guarantee of aging over the product lifecycle.
(8) The metal cap on top of the device is directly connected to the GND terminal (pin #2). Take necessary precautions to prevent any conductor not at ground potential from contacting the cap as that could cause a short circuit to GND.
(9) To avoid any issues due to interference of other signal lines, please take care not to place signal lines near the product as this may have an adverse affect on the performance of the product.
(10) A bypass capacitor of the recommended value(s) must be connected between the $V_{CC}$ and GND terminals of the product. Whenever possible, mount the capacitor(s) on the same side of the PCB and as close to the product as possible to keep the routing traces short.
(11) Power supply connections to $V_{CC}$ and GND pins should be routed as thick as possible while keeping the high frequency impedance low in order to get the best performance.
(12) The use of a filter or similar element in series with the power supply connections to protect from electromagnetic radiation noise may increase the high frequency impedance of the power supply line and may cause the oscillator to not operate properly. Please verify the design to ensure sufficient operational margin prior to use.
(13) Keep PCB routing from the output terminal(s) to the load as short as possible for best performance.
(14) The Enable (OE or $\overline{ST}$) input terminal is high impedance and so susceptible to noise. Connect it to a low impedance source when used and when not used it is recommended to connect it to Vcc for active high inputs and GND for active low inputs.
(15) Do not short the output to GND as that will damage the product. Always use with an appropriate load resistor connected.
(16) This product should be reflowed no more than 3 times. If rework is needed after reflow, please correct it with a soldering iron with the tip set for a temperature of +350 °C or less and only contact each terminal once and for no more than 5 seconds. If this product is mounted on the bottom of the board during a reflow please check that it soldered down properly afterwards.

[Availability of mounting conditions]

| | |
|---|---|
| Reflow on the board | Available |
| Reflow under the board | The parts may fall. Please judge whether it is possible to implement. |
| Soldering pot/bath (Dip soldering system, Flow soldering system) | **Not Available** |
| Soldering iron | Available |

(17) Product failures during the warranty period only apply when the product is used according to the recommended operating conditions described in the specifications. Products that have been opened for analysis or damaged will not be covered. It is recommended to store and use in normal temperature and humidity environments described in the specifications to ensure frequency accuracy and prevent moisture condensation. If the product is stored for more than one year, please confirm the pin solderability prior to use.
(18) If the oscillation circuit is exposed to condensation, the frequency may change or oscillation may stop. Do not use in any conditions where condensation occurs.
(19) Do not store or use the product in an environment where it can be exposed to chemical substances that are corrosive to metal or plastics such as salt water, organic solvents, chemical gasses, etc. Do not use the product when it is exposed to sunlight, dust, corrosive gasses, or other materials for long periods of time.
(20) When using water-soluble solder flux make sure to completely remove the flux residue after soldering. Pay particular attention when the residues contain active halogens which will negatively affect the product and its performance.
(21) Terminals on the side of the product are internally connected to the IC, be careful not to cause short-circuits or reduce the insulation resistance of them in any way.
(22) Precautions for PLL cascade connection
This product uses a PLL (Phase Locked Loop) circuit to synthesize the required output frequency from the crystal oscillation. Therefore, if the output of this oscillator is further cascaded into a PLL, the jitter of the PLL may become large. Especially for applications such as image processing and communication synchronization, please be sure to check and approve it in advance.
(23) Should any customer use the product in any manner contrary to the precautions and/or advice herein, such use shall be done at the customer’s own risk.

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Email:sales@manduic.com

## PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

At Seiko Epson, all environmental initiatives operate under the Plan-Do-Check-Action (PDCA) cycle designed to achieve continuous improvements. The environmental management system (EMS) operates under the ISO 14001 environmental management standard.

All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

ISO 14000 is an international standard for environmental management that was established by the International Standards Organization in 1996 against the background of growing concern regarding global warming, destruction of the ozone layer, and global deforestation.

## WORKING FOR HIGH QUALITY

In order provide high quality and reliable products and services than meet customer needs, Seiko Epson made early efforts towards obtaining ISO9000 series certification and has acquired ISO9001 for all business establishments in Japan and abroad. We have also acquired IATF 16949 certification that is requested strongly by major manufacturers as standard.

IATF 16949 is the international standard that added the sector-specific supplemental requirements for automotive industry based on ISO9001.

■ Explanation of marks used in this datasheet

| | |
|---|---|
| Pb Free | **●Pb free.** |
| RoHS Compliant | **●Complies with EU RoHS directive.**<br>*About the products without the Pb-free mark.<br>Contains Pb in products exempted by EU RoHS directive<br>(Contains Pb in sealing glass, high melting temperature type solder or other) |

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