EPSON

Application Manual

Real Time Clock Module

RX4901CE/RX8901CE

Product name	Product number
RX4901CE XS A0	**X1B000471000115**
RX4901CE XB A0	**X1B000471000215**
RX4901CE XS B0	**X1B000471000315**
RX4901CE XB B0	**X1B000471000415**
RX4901CE XS C0	**X1B000471000515**
RX4901CE XB C0	**X1B000471000615**
RX4901CE XS D0	**X1B000471000715**
RX4901CE XB D0	**X1B000471000815**
RX8901CE XS A0	**X1B000481000115**
RX8901CE XB A0	**X1B000481000215**
RX8901CE XS B0	**X1B000481000315**
RX8901CE XB B0	**X1B000481000415**

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ETM63E Revision History

Rev. No.	Date	Page	Description
01	2021/12/6	All	First released
02	2022/10/25	8 96	When turning the VDD and VBAT power supplies on after turning off, maintain the VDD = VBAT = GND. condition for at least 10 s after turning off. This 10 s was corrected to more than 100ms. *2.2.1 Power_On/sequence* *5.6 Power-On Characteristics*
		43 98	"*Backup Battery Implementation Precautions*"section is added. By this addition, " Mounting Backup Battery" of *"7 Notes on Mounting"* was deleted.
		91	Explanation of condition in *"current consumption 10(I_{DD}5) and 11(I_{DD}6)"* was optimized.
		99	*1, *2, *3 note in *"8 Sample Connection Diagram"* is updated. Each of Battery name was unified to "Backup Battery".
03	2025/06/30		·Revised notes regarding use of this manual. ·Addition of disclaimer information.
04	2026/04/27	64	Correction of a typographical error in the Register name (function) of Bank1 0x17. Incorrect：(Mirrored Mont Data, = 0x05) ⇒ Correct：(Mirrored Month Data, = 0x05)
		65	Correction of a typographical error in the Register name(function) of Bank3 0x32. Incorrect：(Mirrored our Alarm, = 0x08) ⇒ Correct：(Mirrored Hour Alarm, = 0x08) Correction of the register name for Bit3 to Bit0 of Bank3 0x32. Incorrect：XHAE ⇒ Correct：HALM_L[3:0]

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Preface

This document is the application manual for describing the functions, control method, specifications, and electrical characteristics of Seiko Epson Real-Time Clock (RTC) modules RX4901CE and RX8901CE. This manual is provided for designers who develop products using the RX4901CE/RX8901CE.

The RX4901CE is accessed through SPI from the host; the RX8901CE is accessed through I^2C-Bus. For the operations and control methods of these interfaces, refer to a host device manual or other documents.

Notational conventions and symbols in this manual

Notation of Numbers

This manual describes numbers in decimal, binary, and hexadecimal notations.

Decimal	Examples: 1, 10, 123 (general values, date and time, etc.)
Binary	Examples: 0b0, 0b10, 0b1111 (control bit setting values, read values, etc.)
Hexadecimal	Examples: 0x0, 0xF, 0xFF (addresses, register setting values, etc.)

Notation of Register and Bit Names

This manual describes register and bit names as shown below.

Register name: Register SEC

Bit name: TSTP_INTE.STOP bit
This represents the STOP bit in Register TSTP_INTE.

TCTL.FSEL[1:0] bits
This represents two bits in Register TCTL: FSEL1 and FSEL0 bits.

Notation of Channel Numbers

The time stamp function has provided a pin and control bits for each channel that has the same function as the other channels. The pin and bit names contain a channel number (e.g., 1–3). This manual uses "*n*" for the channel numbers to explain the pins and bits for all channels collectively, if there is no need to be individually described. Some control bits have a different bit width even if the same function has been implemented. This manual uses "*x*" as the bit number. Furthermore, "***" is used as a different part of a bit name for describing plural bit names that have a same part.

Pin name: EVIN1, EVIN2, and EVIN3 → EVIN*n*

Bit name: EVIN_EN.EVIN1EN, EVIN_EN.EVIN2EN, and EVIN_EN.EVIN3EN
→ EVIN_EN.EVIN*n*EN

BUF1_STAT.PTR[5:0], BUF2_STAT.PTR[3:0], and BUF3_STAT.PTR[3:0]
→ BUF*n*_STAT.PTR[*x*:0]

EVIN_EN.EVIN1CPEN, CAP_EN.VBATLCPEN, and others
→ ***CPEN

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1 Overview

The RX4901CE/RX8901CE is a RTC (Real-Time Clock) module with an integrated 32.768 kHz digital temperature compensated crystal oscillator (DTCXO). It includes various functions such as a time stamp function that can record up to 32 dates and times when an external or internal event occurs, as well as the basic RTC functions such as time and calendar, time alarm, wakeup timer, and time update interrupts. With the combination of an auto power switching function, which includes a control circuit to prevent reverse current to the main power supply, a continuous temperature-corrected 32.768 kHz clock generation, and Seiko Epson's original low current consumption technology, the RX4901CE/RX8901CE realizes long battery life on various systems.

RX4901CE XS A0
① ② ③

① Model CE type package 3.2 x 2.5 x 1.0 mm
② Frequency tolerance
③ Pin Option A:-D Option A-D

Table 1.1 Product Lineup

Product name	Interface	Default pin function		Accuracy *3
		Pin 4 *1	Pin 10 *2	
RX4901CE Option A XS	3線SPI	FOUT	EVIN2	XS
RX4901CE Option A XB				XB
RX4901CE Option B XS		EVIN3		XS
RX4901CE Option B XB				XB
RX4901CE Option C XS	4線SPI	FOUT	DI	XS
RX4901CE Option C XB				XB
RX4901CE Option D XS		EVIN3		XS
RX4901CE Option D XB				XB
RX8901CE Option A XS	I²C-Bus *4	FOUT	EVIN2	XS
RX8901CE Option A XB				XB
RX8901CE Option B XS		EVIN3		XS
RX8901CE Option B XB				XB

*1 The default Pin 4 function is different depending on the product. It can be switched to the FOUT (clock output) pin or the EVIN3 (external event input) pin by setting a register after the RX4901CE/RX8901CE starts up.
*2 The default Pin 10 function of the Option A and B models is EVIN2. It can be switched to the FOE (FOUT output control) pin by setting a register after the RX4901CE/RX8901CE starts up.
*3 For the difference between XS and XB (accuracy), refer to the frequency tolerance shown in "*5.3 Frequency Characteristics*."
*4 I²C-Bus is a trademark of NXP Semiconductors.

1.1 Features

Table 1.2 Features

Product lineup		RX4901CE				RX8901CE	
		Option A	Option B	Option C	Option D	Option A	Option B
Host interface		3-wire SPI		4-wire SPI		I²C-Bus	
Crystal oscillator		A 32.768 kHz digital temperature compensated crystal oscillator (DTCXO) is included.					
Clock/calendar		• BCD counters for counting seconds, minutes, hours, days, months, and years, a day-of-week counter, and a binary counter for counting 1/1024 seconds are included. • An automatic leap year correction function is included and a leap second correction method is provided. • Time update interrupts can be generated. (1-second, 1-minute, and/or 1-hour counter update intervals)					
Wakeup timer		• Can generate an interrupt in 976.56 µs to 32-year cycle. • Can be used for time integration of the operation with the main power supply or backup power supply.					
Alarm		Can generate an interrupt at the specified day (or day of the week), hour, minute, and second.					
Time stamp	**Trigger source**	External event (EVIN) input, voltage drop/oscillation stop status detected in the RX4901CE/RX8901CE, command input from the host					
	Record data	1/1024 seconds to 1 second, seconds, minutes, hours, days, months, years, trigger source, internal status					
	Number of recordable events	Max. 32 events					
	External event input pins *1	(EVIN2), (EVIN3)		(EVIN3)		EVIN1, (EVIN2), (EVIN3)	
SRAM memory		256 bytes (also used as the time stamp data recording area)					
Clock output (FOUT) *1		• Selectable from 32.768 kHz, 1024 Hz, and 1 Hz outputs • Output can be controlled by a register or the FOE input (selectable with a register).					
Self-monitoring function		Can generate an interrupt when oscillation stops or V_{DD}/V_{BAT} voltage drop status is detected.					
Auto power switching function		• The V_{DD} and V_{BAT} voltages are monitored to switch between Normal mode (V_{DD} operation) and Backup					

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Product lineup	RX4901CE				RX8901CE	
	Option A	Option B	Option C	Option D	Option A	Option B
	mode (V_{BAT} operation). • Charging control for a backup secondary battery or capacitor					
Operating voltage (V_{DD})	1.60 V to 5.5 V					
Operating temperature	-40 °C to +105 °C					

*1 Either one of EVIN3 input or FOUT output can only be used. Either one of EVIN2 input or FOE input can only be used.

1.2 Block Diagram

RX4901CE

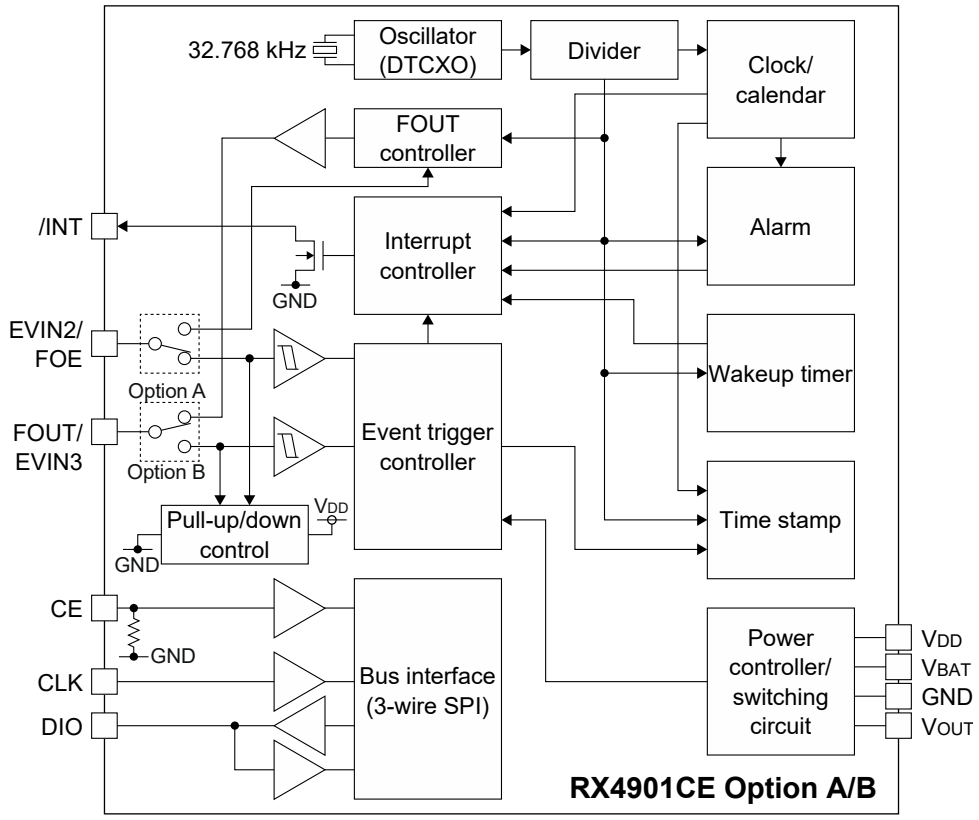


Figure 1.1 RX4901CE Option A/B Block Diagram

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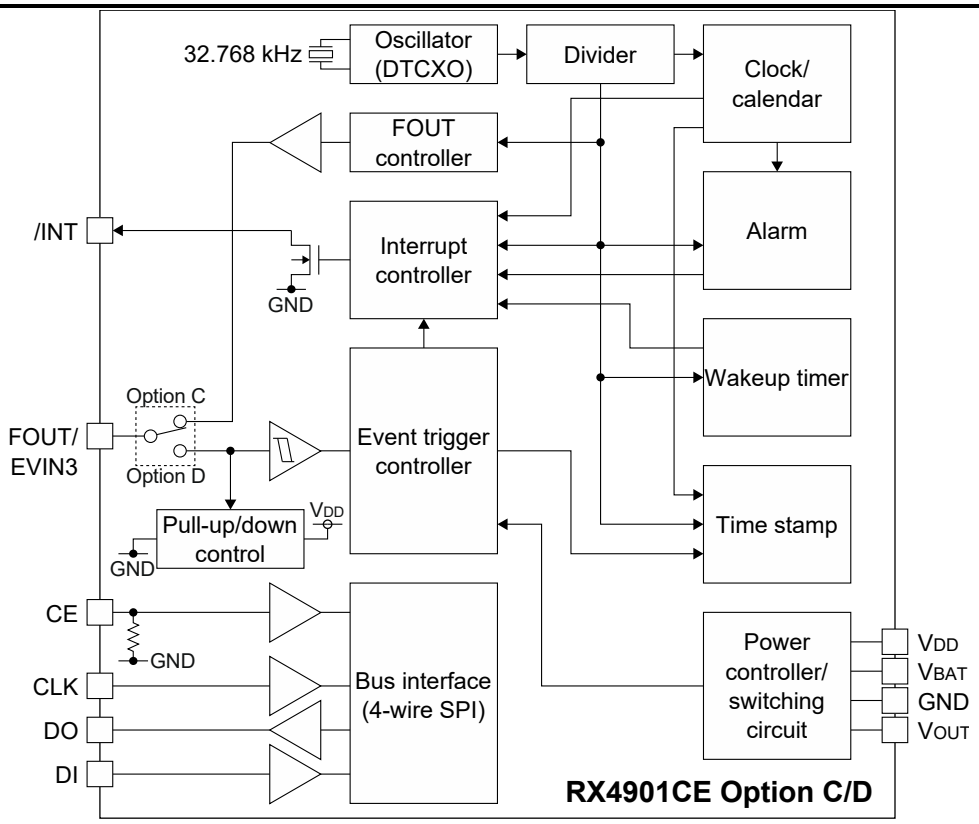


Figure 1.2 RX4901CE Option C/D Block Diagram

RX8901CE

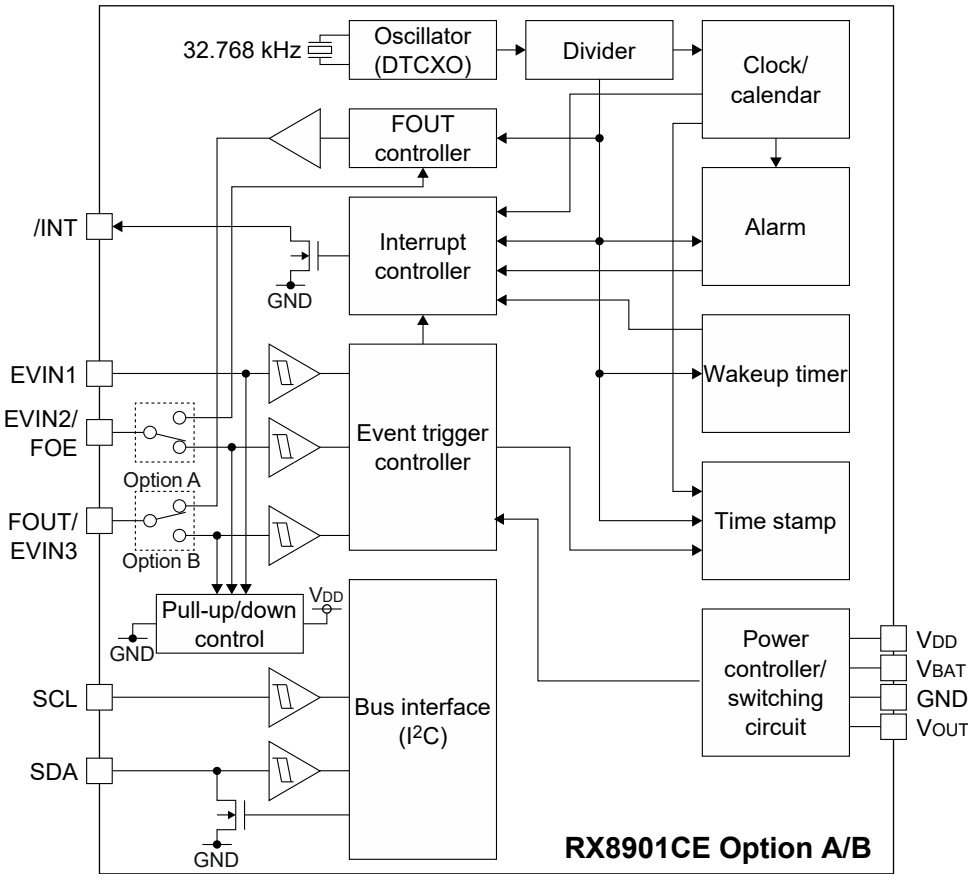


Figure 1.3 RX8901CE Option A/B Block Diagram

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1.3 Pin

1.3.1 Pin Alignment Diagram

RX4901CE

Pin name	No.		No.	Pin name
V_{DD}	1		10	EVIN2 (default)/FOE
V_{OUT}	2		9	GND
V_{BAT}	3		8	/INT
FOUT/EVIN3	4		7	DIO
CLK	5		6	CE

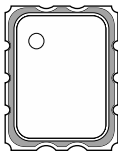


Figure 1.4 RX4901CE Option A/B Pin Alignment Diagram

Pin name	No.		No.	Pin name
V_{DD}	1		10	DI
V_{OUT}	2		9	GND
V_{BAT}	3		8	/INT
FOUT/EVIN3	4		7	DO
CLK	5		6	CE

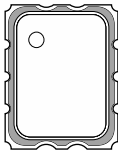


Figure 1.5 RX4901CE Option C/D Pin Alignment Diagram

RX8901CE

Pin name	No.		No.	Pin name
V_{DD}	1		10	EVIN2 (default)/FOE
V_{OUT}	2		9	GND
V_{BAT}	3		8	/INT
FOUT/EVIN3	4		7	SDA
SCL	5		6	EVIN1

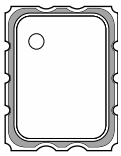


Figure 1.6 RX8901CE Option A/B Pin Alignment Diagram

1.3.2 Pin Descriptions

Symbol Meanings

I/O	I:	Input pin
	O:	Output pin
	I/O:	Input/output pin
Initial state	Hi-Z:	High impedance
	PU:	Pulled up
	PD:	Pulled down
Model-specific column	✓:	Available
	*1:	Only the EVIN3 input or the FOUT output can be used (selectable with a register).
	*2:	Only the EVIN2 input or the FOE input can be used (selectable with a register).
	–:	Unavailable

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Table 1.3 Pin Descriptions

Pin name	I/O	Initial state	Function	RX4901CE				RX8901CE	
				A	B	C	D	A	B
EVIN1	I	PU (1 MΩ)	External event input pins These pins are used to input time stamp trigger signals (detectable even in Backup mode). Pull-up/down and the noise filter on each input are configurable by the registers.	–	–	–	–	✓	✓
EVIN2				✓*2	✓*2	–	–	✓*2	✓*2
EVIN3				(✓)*1	✓*1	(✓)*1	✓*1	(✓)*1	✓*1
CLK	I	Hi-Z	3-wire/4-wire SPI serial clock input pin This pin cannot be left floating in Normal mode, but it can be left floating in Backup mode.	✓	✓	✓	✓	–	–
DIO	I/O	Hi-Z	3-wire SPI serial data input/output pin This pin cannot be left floating in Normal mode, but it can be left floating in Backup mode.	✓	✓	–	–	–	–
DO	O	Hi-Z	4-wire SPI serial data output pin	–	–	✓	✓	–	–
DI	I	Hi-Z	4-wire SPI serial data input pin This pin cannot be left floating in Normal mode, but it can be left floating in Backup mode.	–	–	✓	✓	–	–
CE	I	PD (300 kΩ)	3-wire/4-wire SPI slave select input pin A pull-down resistor is included.	✓	✓	✓	✓	–	–
SCL	I	Hi-Z	I^2C-Bus serial clock input pin This pin cannot be left floating in Normal mode, but it can be left floating in Backup mode. This pin can be externally pulled up to a voltage up to 5.5 V.	–	–	–	–	✓	✓
SDA	I/O	Hi-Z	I^2C-Bus serial data input/output pin (N-ch. open drain) This pin cannot be left floating in Normal mode, but it can be left floating in Backup mode. This pin can be externally pulled up to a voltage up to 5.5 V.	–	–	–	–	✓	✓
FOUT	O	Hi-Z	Clock output pin (CMOS) 32.768 kHz (default), 1024 Hz or 1 Hz clock output is selectable. This pin can be switched to the wakeup timer interrupt output (CMOS).	✓*1	(✓)*1	✓*1	(✓)*1	✓*1	(✓)*1
FOE	I	Hi-Z	FOUT output control pin This pin cannot be left floating in both Normal and Backup modes.	(✓)*2	(✓)*2	–	–	(✓)*2	(✓)*2
/INT	O	Hi-Z	Interrupt output pin (N-ch. open drain) The wakeup timer, time update, alarm, and/or event detection interrupt signals can be selected to output from this pin. When two or more signals are selected, they are NORed before being output. This pin is effective even in Backup mode. This pin can be externally pulled up to a voltage up to 5.5 V.	✓	✓	✓	✓	✓	✓
V_{DD}	–	–	Main power supply pin The supply voltage is supplied from this pin to the internal circuits in Normal mode.	✓	✓	✓	✓	✓	✓
V_{OUT}	–	–	Internal operating voltage output pin Connect a 1.0 µF bypass capacitor to this pin when using the auto power switching function.	✓	✓	✓	✓	✓	✓
V_{BAT}	–	–	Backup power supply pin Connect a backup power supply such as a large-capacity capacitor (EDLC), secondary battery, or primary battery. The operating power voltage is supplied from this pin to the internal circuits in Backup mode.	✓	✓	✓	✓	✓	✓
GND	–	–	Ground pin	✓	✓	✓	✓	✓	✓

Notes:
- Do not leave the unused input and input/output pins open nor apply an intermediate potential to them if the internal pull-up or -down resistor is not enabled.
- Leave the FOUT and /INT pins open when their outputs are not used.
- All the input and input/output pins have a voltage tolerant input structure that allows applying a voltage up to 5.5 V regardless of the operating power voltage.

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2 Power Supply and Initialization

2.1 Power Supply

The table below lists the RX4901CE/RX8901CE power supply pins.

Table 2.1 List of Power Supply Pins

Pin name	Function
V_{DD}	Main power supply pin The operating power voltage is supplied from this pin to the internal circuits in Normal mode.
V_{OUT}	Internal operating voltage output pin Connect a 1 µF bypass capacitor to this pin.
V_{BAT}	Backup power supply pin Connect a backup power supply such as a large-capacity capacitor (EDLC), secondary battery, or primary battery. The operating power voltage is supplied from this pin to the internal circuits in Backup mode.
GND	Ground pin

In normal operation, the RX4901CE/RX8901CE operates with the main power supply voltage applied to the V_{DD} pin (Normal mode). When the V_{DD} voltage drops below the prescribed voltage, although the host interface becomes unusable, the RTC operating power is switched to the backup power supply voltage applied to the V_{BAT} pin to maintain the oscillation circuit operation and clock/calendar function with the internal data retained (Backup mode). This power supply switching is automatically performed by the auto power switching circuit (for more information, refer to "*3.9 Auto Power Switching Function*").
For the operating power supply range, refer to "*5.2 Recommended Operating Conditions*."
Figure 2.1 shows the configuration of the auto power switching circuit.

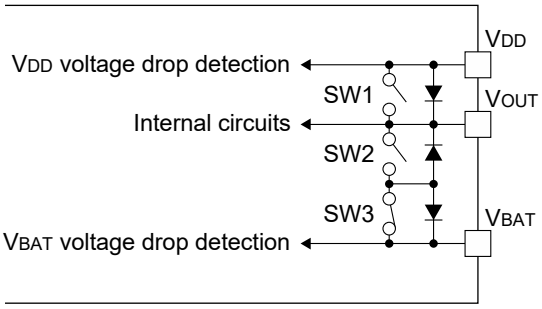
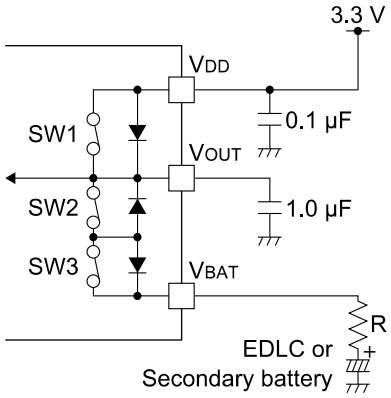


Figure 2.1 Auto Power Switching Circuit

The following shows power supply connection examples.

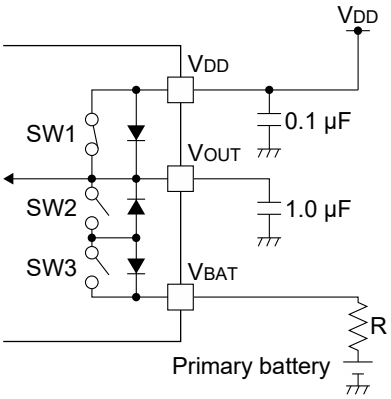
(1) Power supply backup configuration example using a secondary battery



(PWSW_CFG.INIEN = 1, PWSW_CFG.CHGEN = 1)
Figure 2.2 Power Supply Connection Example (1)

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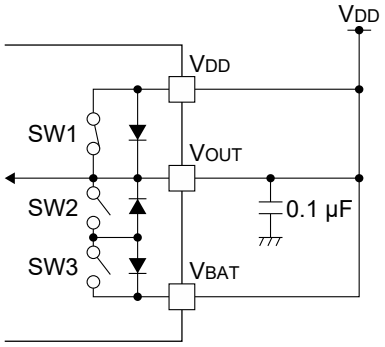
(2) Power supply backup configuration example using a primary battery



(PWSW_CFG.INIEN = 1, PWSW_CFG.CHGEN = 0)

Figure 2.3 Power Supply Connection Example (2)

(3) Single power supply configuration example (no backup power supply is used)

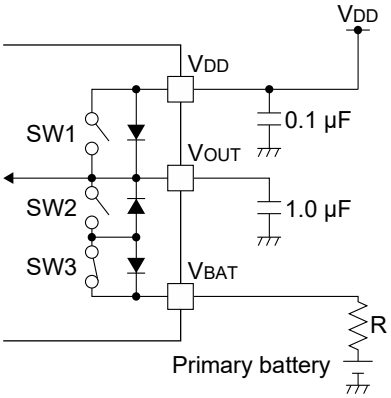


Short-circuit V_{DD}, V_{BAT}, and V_{OUT}.

(PWSW_CFG.INIEN = 0, PWSW_CFG.CHGEN = 0, PWSW_CFG.SWSEL[1:0] = 0b10)

Figure 2.4 Power Supply Connection Example (3)

(4) Power supply backup configuration example using a primary battery (the auto power switching function is not used)



The external main power supply and the primary battery are connected in parallel via the diodes in the RX4901CE/RX8901CE.

(PWSW_CFG.INIEN = 0, PWSW_CFG.CHGEN = 0, PWSW_CFG.SWSEL[1:0] = 0b01)

Figure 2.5 Power Supply Connection Example (4)

Notes:
- The bypass capacitors should be placed as close to each pin as possible.
- When connecting an external power supply device or a large-size battery to the V_{BAT} pin, connect a bypass capacitor of 0.1 µF or more to the V_{BAT} pin as necessary.
- When using the auto power switching function, connect a 1 µF capacitor to the V_{OUT} pin.

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2.2 Initialization

2.2.1 Power-On Sequence

The RX4901CE/RX8901CE executes a power-on reset when the V_{DD} or V_{BAT} voltage is supplied (one supplied in advance is used). To make certain that the RX4901CE/RX8901CE executes a power-on reset, satisfy the specification of the power supply slope (t_{R1}, refer to "*5.6 Power-On Characteristics*"). The t_{CL} in Figure 2.6 shows the time for canceling power-on reset.

When turning the V_{DD} and V_{BAT} power supplies on after turning off, maintain the V_{DD} = V_{BAT} = GND condition for at least 100 ms after turning off. Then turn the power supply back on again with the power supply initial rise time specification satisfied. (VDD OFF time and VBAT OFF time)

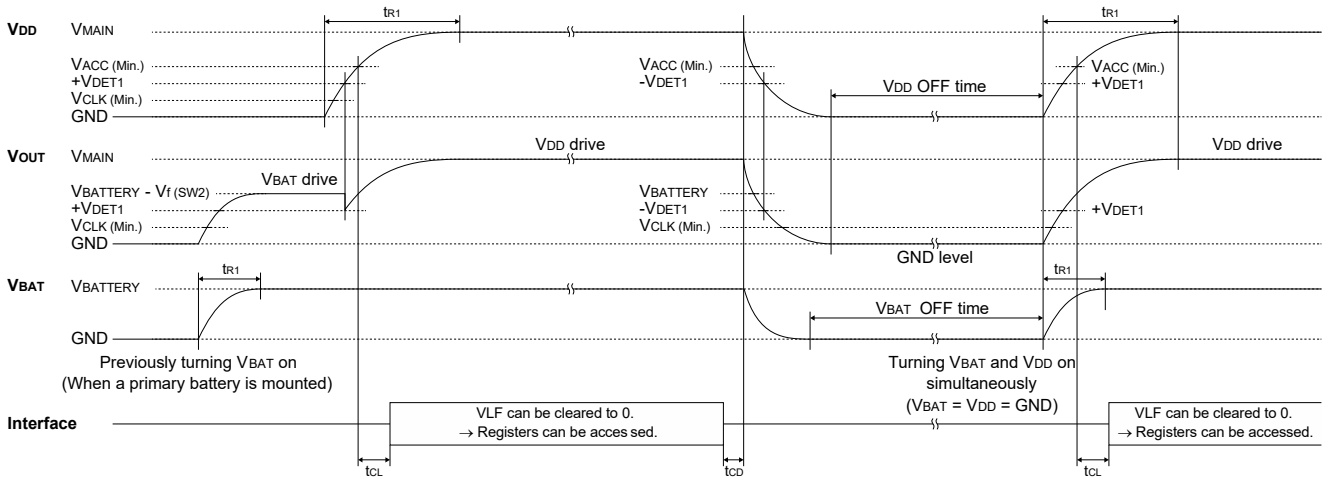


Figure 2.6 Power-On Sequence

2.2.2 Oscillation Start-UP Time

When the V_{DD} or V_{BAT} voltage is applied, the crystal oscillation circuit starts oscillating. The host interface becomes usable after 40 ms from turning V_{DD} on. However, a wait time is required until the internal crystal oscillation waveform has a sufficient amplitude before the clock/calendar counter value can be set and read. This refers to the oscillation start-up time (t_{STA}, refer to "*5.3 Frequency Characteristics*").

There are two methods to secure the wait time: one is the method for repeatedly trying to clear the INTF.OSCSTPF and INTF.VLF bits, another is the method for waiting by the host until t_{STA} has elapsed after applying the V_{DD} or V_{BAT}. The former can shorten the wait time until the clock/calendar counter value will be able to set and read. On the other hand, the latter can set the clock/calendar counter with higher time accuracy, as the crystal oscillation frequency becomes more stable although the wait time becomes longer

The INTF.OSCSTPF and INTF.VLF bits are set to 1 by the oscillation stop detection function immediately after the crystal oscillation circuit starts oscillating. While the oscillation stop status is being detected, these bits cannot be cleared to 0 even if 0 is written to these bits through the host interface. When the oscillation stop status is cancelled by the grown internal oscillation waveform amplitude, the INTF.OSCSTPF and INTF.VLF bits can be cleared. Therefore, try to clear these bits at arbitrary time intervals until they are actually cleared. After that the clock/calendar counter value can be set and read.

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At turning power (V_{DD}) on

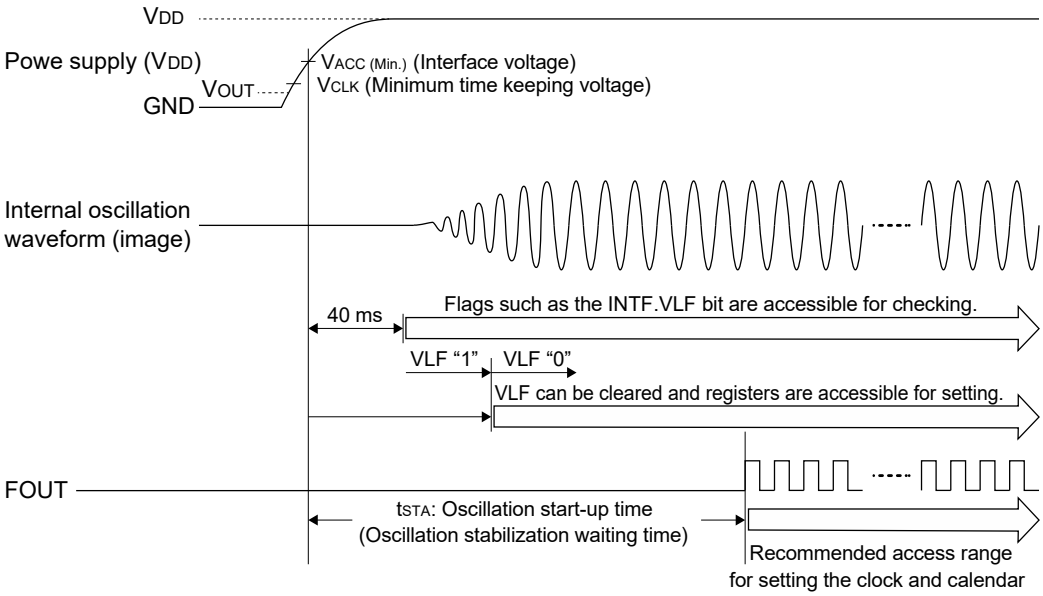


Figure 2.7 Oscillation Start-Up Sequence

At restoring to Normal mode from Backup mode

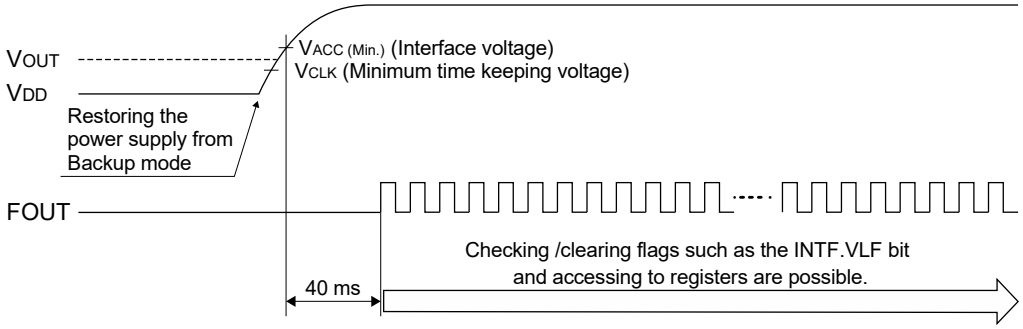


Figure 2.8 Restoring from Backup Mode

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2.2.3 Initial Settings

Initial settings are required after initial power on or a supply voltage drop with the INTF.VLF bit set to 1 from 0. This section shows an example of initial settings.

Initial Setting Procedure

1. Wait for at least 40 ms after the power is turned on or the RX4901CE/RX8901CE returns from Backup mode.
2. Cancelling POR and detecting oscillation start-up (polling of the INTF.VLF bit)
   The INTF.VLF bit is set to 1 when a power-on reset is issued due to a power supply voltage drop or an oscillation stop is detected.
   2.1. Read the INTF.VLF bit and go to Step 3 when the read value = 0.
   If the INTF.VLF bit = 1, perform Steps 2.2 to 2.4.
   2.2. Write 0x00 to Register INTF to try and clear the INTF.VLF bit and to clear the interrupt flags.
   - PORF bit (Power-on reset detection flag)
   - OSCSTPF bit (Oscillation stop detection flag)
   - UF bit (Time update interrupt flag)
   - TF bit (Wakeup timer interrupt flag)
   - AF bit (Alarm interrupt flag)
   - EVF bit (Event detection interrupt flag)
   - VLF bit (RTC initialize interrupt flag)
   - VTMPLF bit (Temperature compensation operation stop interrupt flag)

   2.3. Take a waiting time.
   2.4. Return to Step 2.1.
3. Complete the initial settings in the case of a restoring from Backup mode; otherwise go to Step 4.
4. Configure the auto power switching function. (Register PWSW_CFG)
   - CHGEN and INIEN bits (Enable/disable charging to backup battery)
   - VBATLDETEN and VBATLDETBK bits (Enable/disable V_{BAT} voltage detection)
   - SWSEL[1:0] bits (Configure power-supply switches)
   - VDDSAMP[1:0] bits (Set V_{DD} voltage sampling period)

   For more information, refer to "*3.9 Auto Power Switching Function*."
5. Configure the Pin 4 and Pin 10 assignment functions. (Register WTICFG)
   - FOEMUX bit (Pin 10: Select EVIN2 or FOE)
   - EVIN3MUX bit (Pin 4: Select FOUT or EVIN3)

   * RX4901CE Option C/D does not allow selection of the Pin 10 function.
6. Disable interrupts/counters. (Write 0x00 to Register TSTP_INTE.)
   - CSEL[1:0] bits (Temperature sensor measurement operation interval)
   - UIE bit (Disable time update interrupt)
   - TIE bit (Disable wakeup timer interrupt)
   - AIE bit (Disable alarm interrupt)
   - EIE bit (Disable event detection interrupt)
   - STOP bit (Stop counters)
7. Set the current time.
   For more information, refer to "*3.2 Clock and Calendar Function*."
8. Set alarm.
   For more information, refer to "*3.5 Alarm Function*."
9. Set wakeup timer.
   For more information, refer to "*3.6 Wakeup Timer Function*."

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2.3 Operating Mode

The RX4901CE/RX8901CE has five operating modes.

V_{DD} Power Rise Standby State

The RX4901CE/RX8901CE enters this state when the V_{BAT} power supply voltage becomes higher than the $+V_{LOW}$ voltage level, for instance, when a backup battery is connected before V_{DD}. The 32 kHz oscillation circuit initiates in this state. The host cannot access the RX4901CE/RX8901CE registers.

Initial Mode

The RX4901CE/RX8901CE enters this mode when the V_{DD} voltage that has turned on becomes higher than the $+V_{DET1}$ voltage level and 40 ms has elapsed. Although the host can access the RX4901CE/RX8901CE registers, the clock/calendar counter cannot be set and read, as the RX4901CE/RX8901CE has detected that the 32 kHz oscillation circuit is in stop state. The INTF.OSCSTPF and INTF.VLF bits are not cleared even when attempts are made to clear these bits.

Normal Mode

This mode operates the RX4901CE/RX8901CE with the main power supply V_{DD}. The host can access the RX4901CE/RX8901CE registers including the clock/calendar counter registers. The auto power switching function has been disabled with the internal power switches fixed.

Normal Mode (with transition to Backup mode enabled)

This mode operates the RX4901CE/RX8901CE with the main power supply V_{DD}. The host can access the RX4901CE/RX8901CE registers including the clock/calendar counter registers. The RX4901CE/RX8901CE keeps detecting the voltage level of the main power supply voltage V_{DD} during this mode, and the operating mode transits to Backup mode if V_{DD} drops to the V_{DD} drop detection voltage $-V_{DET1}$ or below.

Backup Mode

This mode operates the RX4901CE/RX8901CE with the backup power supply V_{BAT}. The V_{DD} pin is automatically disconnected from the backup power supply V_{BAT} by the internal power switch SW1 so that current will not flow from V_{BAT} to the main power supply V_{DD}.

The host interface is disabled and the CE, CLK, DI, DIO, SDA, and SCL input pins can be placed into a floating state. The DO and FOUT output pins go into a Hi-Z state.

If the V_{BAT} voltage is equal to or higher than the time keeping voltage V_{CLK}, the clock/calendar function, EVIN*n* input, and /INT output are active similarly to Normal mode.

Figure 2.9 shows the state transition diagram between the operating modes.

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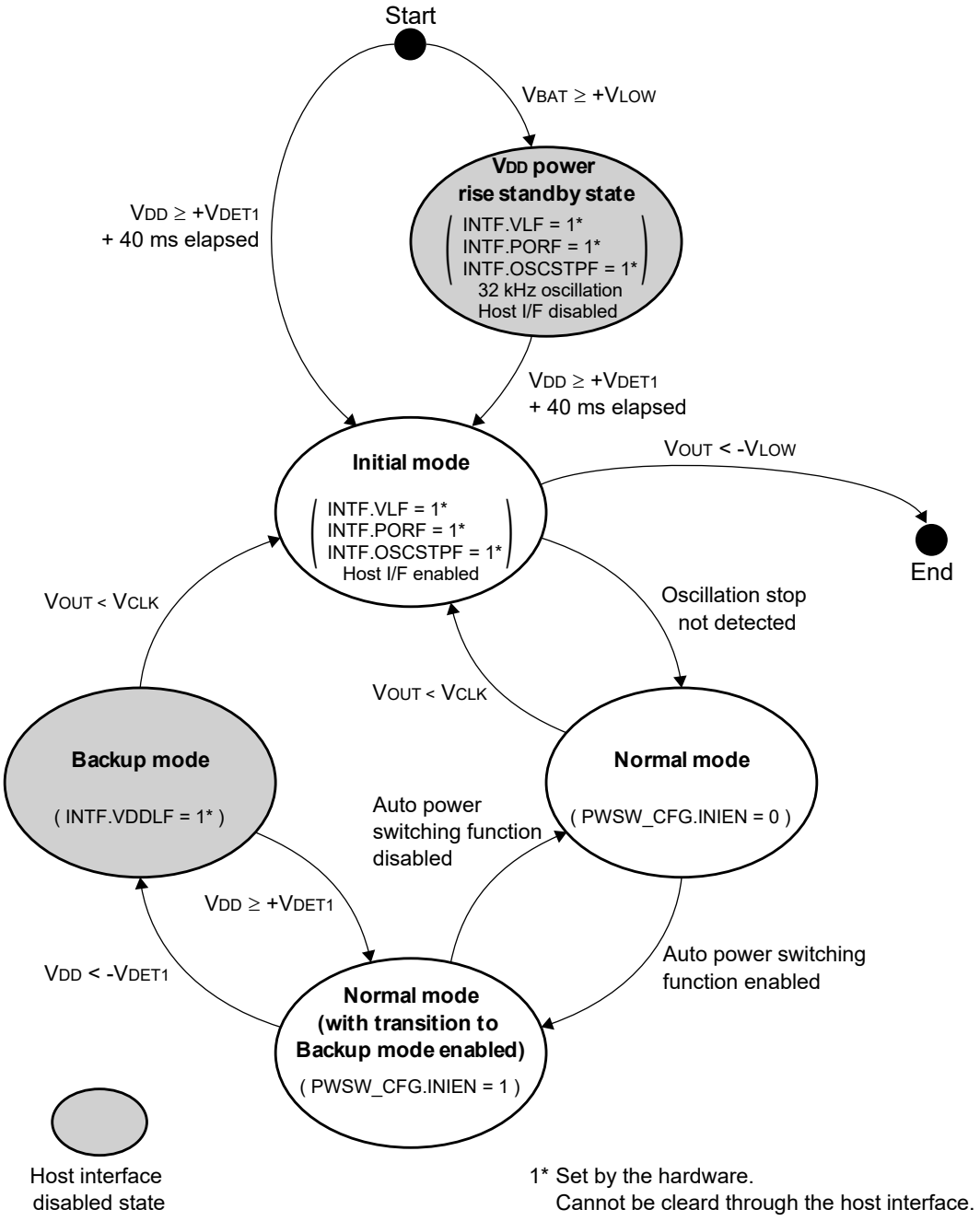


Figure 2.9 State Transition Diagram

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3 Functions

3.1 Host Interface

The RX4901CE includes SPI as the host interface; RX8901CE includes an I^2C-Bus interface. Both models work as a slave device.

3.1.1 Accessing to RX4901CE Registers (SPI)

The RX4901CE registers can be accessed via an SPI bus. The following shows the specifications of the RX4901CE SPI interface:

- Interface type: RX4901CE Option A/B: 3-wire SPI, RX4901CE Option C/D: 4-wire SPI
- Slave device
- Data length: 8 bits
- Data format: MSB first
- Clock polarity: High at idle
- Clock phase: Data sampled at the rising edge and shifted out at the falling edge
- Maximum communication speed: 4 Mbits/s
- Address auto-increment function included
- The CE (Slave Select) input pin has a built-in pull-down resistor.

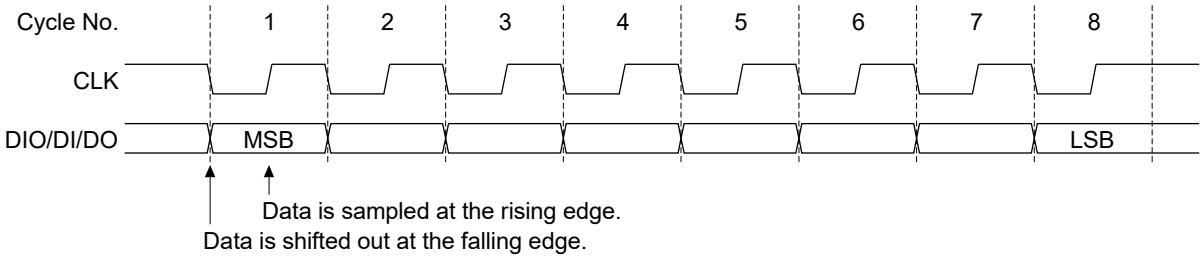


Figure 3.1 SPI Data Format

SPI Interface Pins

The RX4901CE has the SPI interface pins listed in the table below.

Table 3.1 RX4901CE Option A/B SPI Interface Pins

Pin name	I/O	Initial state	Function
CLK	I	Hi-Z	SPI serial clock input pin
DIO	I/O	Hi-Z	SPI serial data input/output pin
CE	I	PD	SPI slave select input pin (A pull-down resistor is included.)

Table 3.2 RX4901CE Option C/D SPI Interface Pins

Pin name	I/O	Initial state	Function
CLK	I	Hi-Z	SPI serial clock input pin
DI	I	Hi-Z	SPI serial data input pin
DO	O	Hi-Z	SPI serial data output pin
CE	I	PD	SPI slave select input pin (A pull-down resistor is included.)

Connection with the host

Figure 3.2 shows examples of connection with the host.

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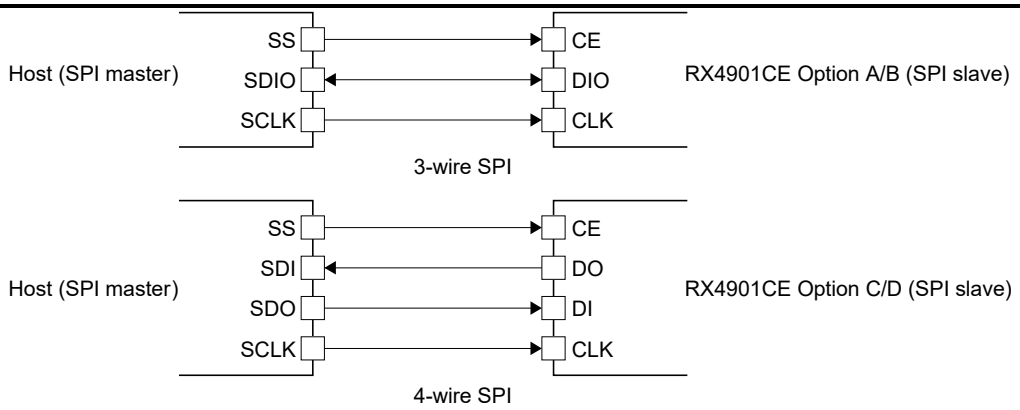


Figure 3.2 Example of Connection Between Host and RX4901CE

Pull-down resistor (CE pin)

The RX4901CE includes a pull-down resistor on the CE pin. It cannot be disconnected via software. The CE pin is always pulled down.

Writing Data to Registers

The host sets the CE signal to high to select the RX4901CE as the slave device to be accessed. Then it starts outputting the synchronous clock (CLK). In sync with this clock, the host first sends an 8-bit address data (register address to which the first data is written) including a bit to specify write mode to the RX4901CE DIO (Option A/B) or DI (Option C/D) pin, and write data follows in eight-bit units. Figure 3.3 shows the bit configuration of the address data to be sent first when writing data.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	7-bit address (0b000 0000–0b110 1111)						

↑ Setting 0 specifies write mode.

Figure 3.3 SPI Data Write Address Data

Figure 3.4 shows RX4901CE register data write operations. Every time an 8-bit data is written, it is stored to the specified register and at the same time only the low-order 4 bits of the register address are automatically incremented. When the low-order 4 bits of the register address exceed 0xF, they wrap to 0x0. The high-order 3 bits of the register address are not automatically incremented, therefore, to change them, negate the CE signal (CE signal = low) to cancel the slave select status once, and then restart communication by sending new address data.

Be sure to avoid negating the CE signal until the last eight-bit data has been sent completely. If the CE signal is negated in the middle of a transfer, the data that has not be sent for 8 bits yet is discarded and not written to the registers.

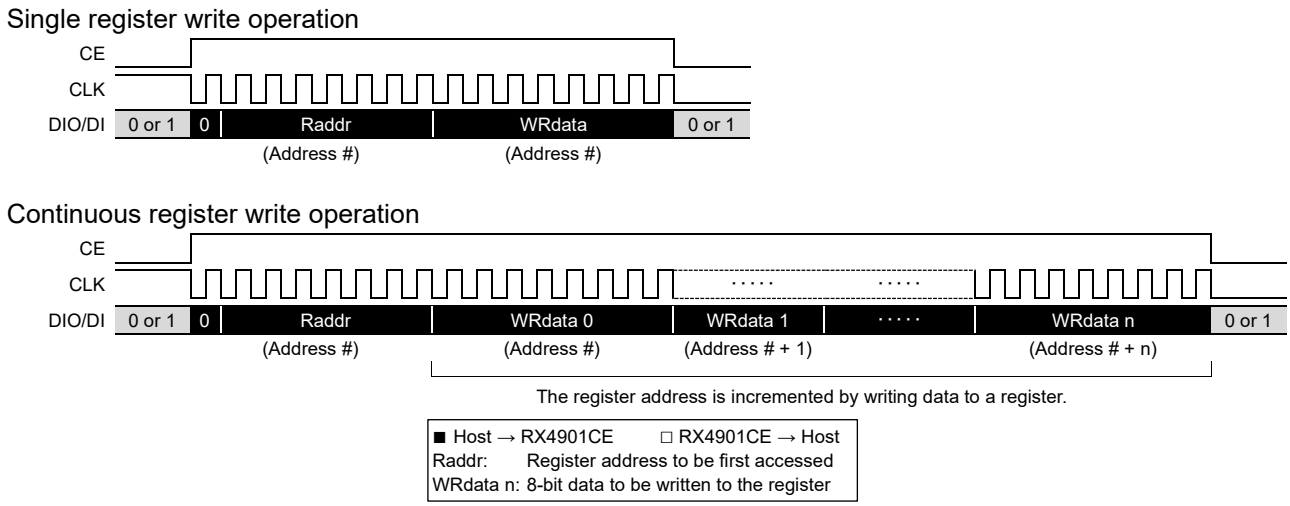


Figure 3.4 SPI Register Write Operation

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Reading Data from Registers

The host sets the CE signal to high to select the RX4901CE as the slave device to be accessed. Then it starts outputting the synchronous clock (CLK). In sync with this clock, the host first sends an 8-bit address data (register address from which the first data is read) including a bit to specify read mode to the RX4901CE DIO (Option A/B) or DI (Option C/D) pin. Once the address data is received, the RX4901CE sends read data from the DIO (Option A/B) or DO (Option C/D) pin to the host in eight-bit units until the host stops outputting the clock. The D1 pin inputs are ineffective in this period. Figure 3.5 shows the bit configuration of the address data to be sent first when reading data.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	7-bit address (0b000 0000–0b110 1111)						

↑ Setting 1 specifies read mode.

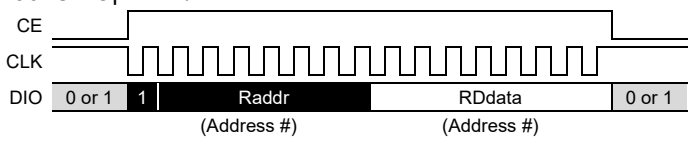
Figure 3.5 SPI Data Read Address Data

Figure 3.6 shows RX4901CE register data read operations. Every time an 8-bit data is read, only the low-order 4 bits of the register address are automatically incremented. When the low-order 4 bits of the register address exceed 0xF, they wrap to 0x0.

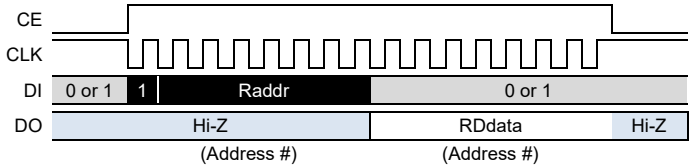
To change the high-order 3 bits of the address to be accessed, negate the CE signal to cancel the slave select status once, and then restart communication by sending new address data.

Single register read operation

RX4901CE Option A/B

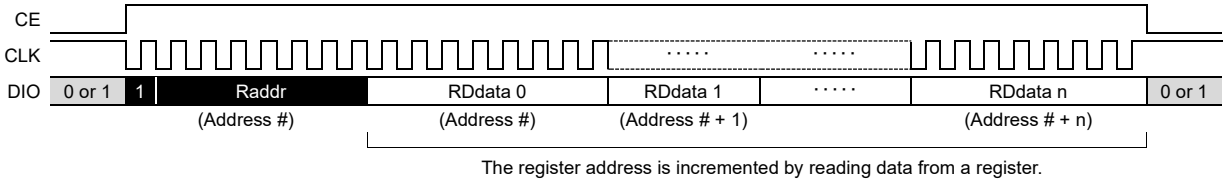


RX4901CE Option C/D



Continuous register read operation

RX4901CE Option A/B



RX4901CE Option C/D

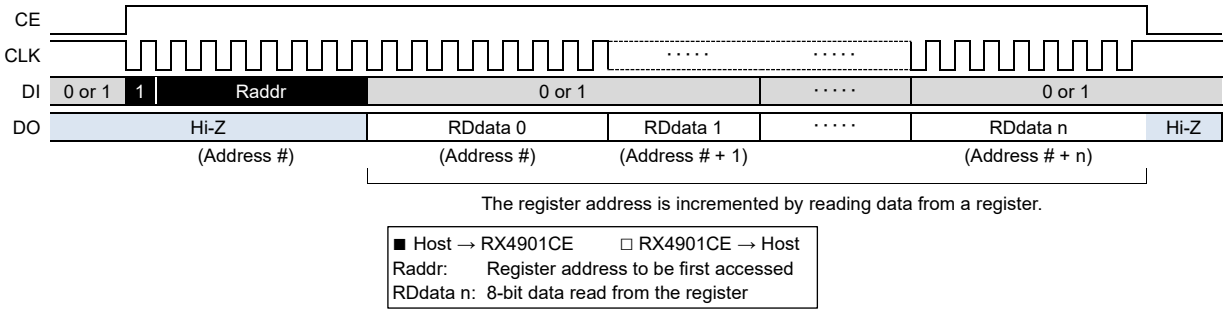


Figure 3.6 SPI Register Read Operation

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3.1.2 Accessing to RX8901CE Registers (I²C-Bus)

The RX8901CE registers can be accessed via an I²C-Bus. The following shows the specifications of the RX8901CE I²C-Bus interface circuit:

- Slave device
- Standard mode (up to 100 kbits/s) and fast mode (up to 400 kbits/s) supported
- 7-bit slave address 0x32

I²C-Bus Interface Pins

The RX8901CE has the I²C-Bus interface pins listed in the table below.

Table 3.3 I²C-Bus Interface Pins

Pin name	I/O	Initial state	Function
SCL	I	Hi-Z	I²C-Bus serial clock input pin
SDA	I/O	Hi-Z	I²C-Bus serial data input/output pin (N-ch. open drain)

Connection with the host

Figure 3.7 shows an example of connection with the host.

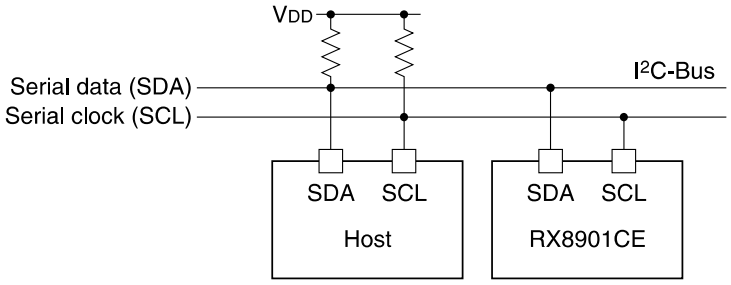


Figure 3.7 Example of Connection Between I²C-Bus Host and RX8901CE

Slave Address

The slave address of the RX8901CE is the 7-bit value shown below.

←			Slave address			→	R/W
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	0	0	1	0	*

* 0: Write mode, 1: Read mode

Figure 3.8 RX8901CE I²C-Bus Slave Address

Writing Data to Registers

A communication starts when the host generates a START condition on the I²C-Bus and outputs a slave address with the R/W bit that specifies write mode. The host then outputs the 8-bit register address to which the first data is written. After that the host outputs write data in eight-bit units for the required number, finally it generates a STOP condition. The RX8901CE returns ACK every time it receives an eight-bit data and gets ready to receive data that follows.
Figure 3.9 shows RX8901CE register data write operations. Every time an 8-bit data is written, only the low-order 4 bits of the register address are automatically incremented. When the low-order 4 bits of the register address exceed 0xF, they wrap to 0x0.

To change the high-order 4 bits of the address to be accessed, generate a Repeated START condition or STOP and START conditions, and then restart by sending new read address.

If a STOP condition is not input and the I²C-Bus has stayed in busy state even when 1 second or more has elapsed from reception of the slave address, to prevent a malfunction, the RX8901CE automatically initializes the I²C-Bus interface circuit to generate a bus timeout. As a result, SDA goes into Hi-Z to wait for a START condition. Therefore, to resume communication, generate a START condition and perform transmission again.

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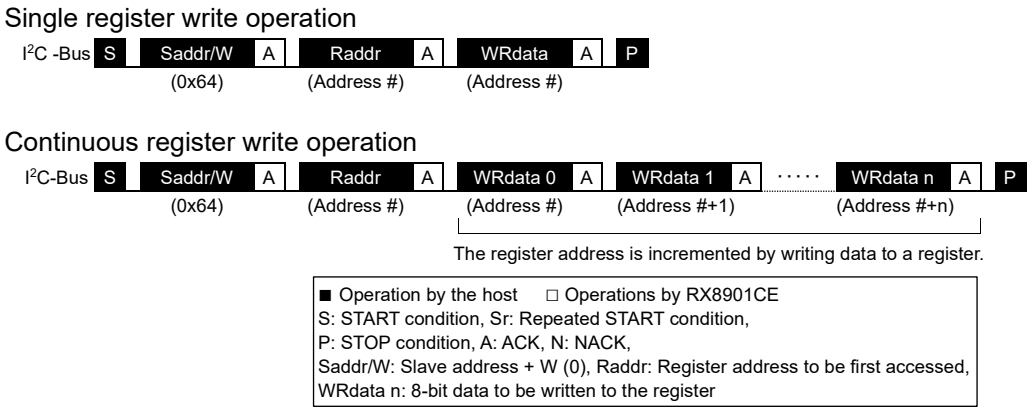


Figure 3.9 Register Write Operation through I²C-Bus

Reading Data from Registers

A communication starts when the host generates a START condition on the I²C-Bus and outputs a slave address with the R/W bit that specifies write mode. The host then outputs the 8-bit register address from which the first data is read. After that the host generates a Repeated START condition and outputs a slave address with the R/W bit that specifies read mode. Once this slave address is received, the RX8901CE sends read data in eight-bit units until the host returns NACK.

The host returns ACK every time it receives an eight-bit data and requests to send data that follows. When the last data is received, the host returns NACK and generates a STOP condition to terminate communication.
Figure 3.10 shows RX8901CE register data read operations. Every time an 8-bit data is read, only the low-order 4 bits of the register address are automatically incremented. When the low-order 4 bits of the register address exceed 0xF, they wrap to 0x0.

To change the high-order 4 bits of the address to be accessed, generate a Repeated START condition or STOP and START conditions, and then restart by sending new read address.

The RX8901CE retains the address from which data has been read at the end of communication. If the host starts the subsequent reading by sending the slave address with the R/W bit that specifies read mode without specifying a read address, the RX8901CE starts reading from the address that follows the last time.

If a STOP condition is not input and the I²C-Bus has stayed in busy state even when 1 second or more has elapsed from reception of the slave address, to prevent a malfunction, the RX8901CE automatically initializes the I²C-Bus interface circuit to generate a bus timeout. As a result, SDA goes into Hi-Z to wait for a START condition. If the data reading is continued in this state, the data is all read as 0xFF.
To resume communication, generate a START condition and perform transmission again.

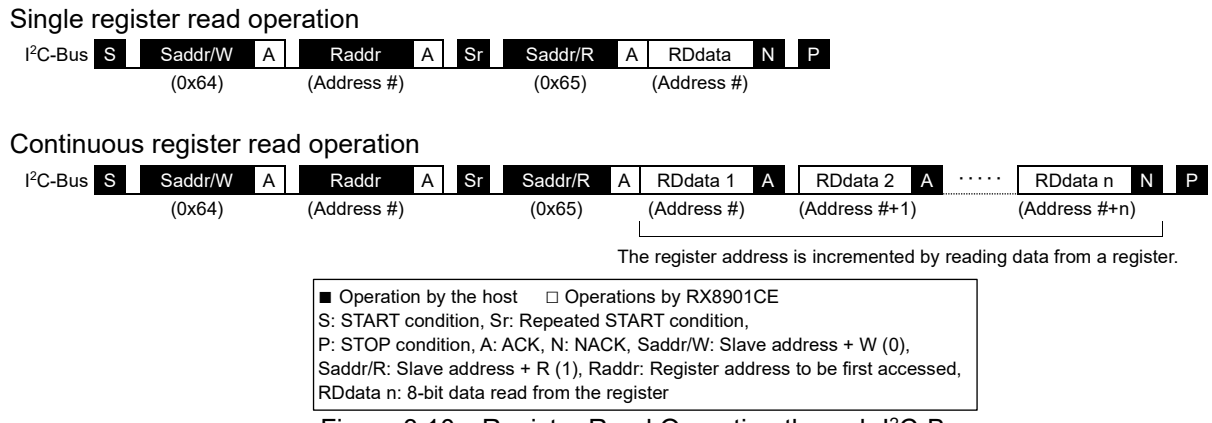


Figure 3.10 Register Read Operation through I²C-Bus

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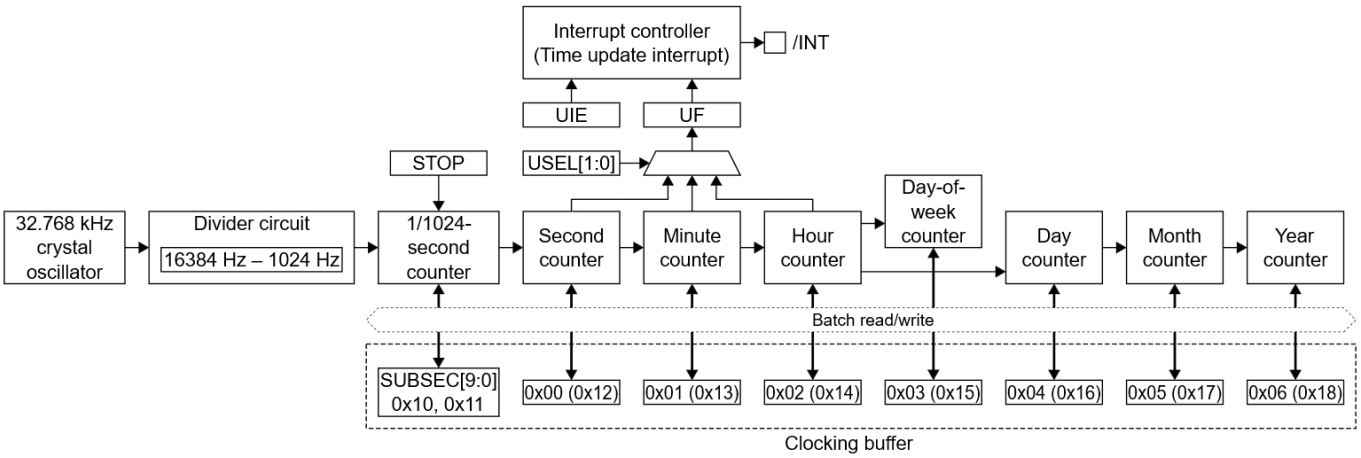
3.2 Clock and Calendar Function

3.2.1 Overview

The following shows the features of the clock and calendar function:

- BCD counters for counting seconds, minutes, hours, days, months, and years, and a day-of-week counter are included.
- An automatic leap year correction function is included (automatically corrected years are within 01 to 99) and a leap second correction method is provided.
- 1/1024-second counter values can be read or written.
- A clocking buffer is included allowing access to the clock/calendar counter data in any timing regardless of the counter operation.

Figure 3.11 shows the configuration of the counters.



The block surrounded by a dotted line is the clocking buffer that performs batch read/write from/to the counters. The values in parentheses represent the mirror register addresses.

Figure 3.11 Clock/Calendar Counter Configuration

Crystal oscillator	This is a digital temperature compensated crystal oscillator (DTCXO) that generates a 32.768 kHz clock.
Divider circuit	This circuit generates 1024 Hz signals by dividing the 32.768 kHz clock.
1/1024-second counter	This is a binary counter to count from 0 to 1023/1024 seconds using the 1024 Hz signal as the source clock. This counter is cleared by writing second counter setting data to Register SEC. This counter stops counting operation by setting the TSTP_INTE.STOP bit to 1.
Second counter	This is a BCD counter to count seconds from 0 to 59 using the 1 Hz signal sent from the divider circuit as the source clock. A time update interrupt can be generated when the second value in this counter is updated.
Minute counter	This is a BCD counter to count minutes from 0 to 59 using the second counter overflow signal as the source clock. A time update interrupt can be generated when the minute value in this counter is updated.
Hour counter	This is a BCD counter to count hours from 0 to 23 using the minute counter overflow signal as the source clock (supports 24-hour system only). A time update interrupt can be generated when the hour value in this counter is updated.
Day counter	This is a BCD counter to count days from 1 to 28, 29, 30, or 31 according to the month and leap year conditions using the hour counter overflow signal as the source clock. The counter starts counting from 1 and 0 is skipped.
Day-of-week counter	This is a 7-bit counter in which the bits are shifted interlocking with the day counter. Each of Bit 0 to Bit 6 corresponds to a day of the week. The bit assignment to the day of the week is optional. However, each bit must be assigned so that the bit shift direction will match with the order of the days of the week.

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Table 3.4 Example of Day-of-Week Assignment

Day of week	(Bit 7)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex. value
Sunday	-	0	0	0	0	0	0	1	0x01
Monday	-	0	0	0	0	0	1	0	0x02
Tuesday	-	0	0	0	0	1	0	0	0x04
Wednesday	-	0	0	0	1	0	0	0	0x08
Thursday	-	0	0	1	0	0	0	0	0x10
Friday	-	0	1	0	0	0	0	0	0x20
Saturday	-	1	0	0	0	0	0	0	0x40

Month counter — This is a BCD counter to count months from 1 to 12 using the day counter overflow signal as the source clock. The counter value is one from 1 to 12 and 0 is skipped.

Year counter — This is a BCD counter to count years from 0 to 99 using the month counter overflow signal as the source clock.

3.2.2 Operations

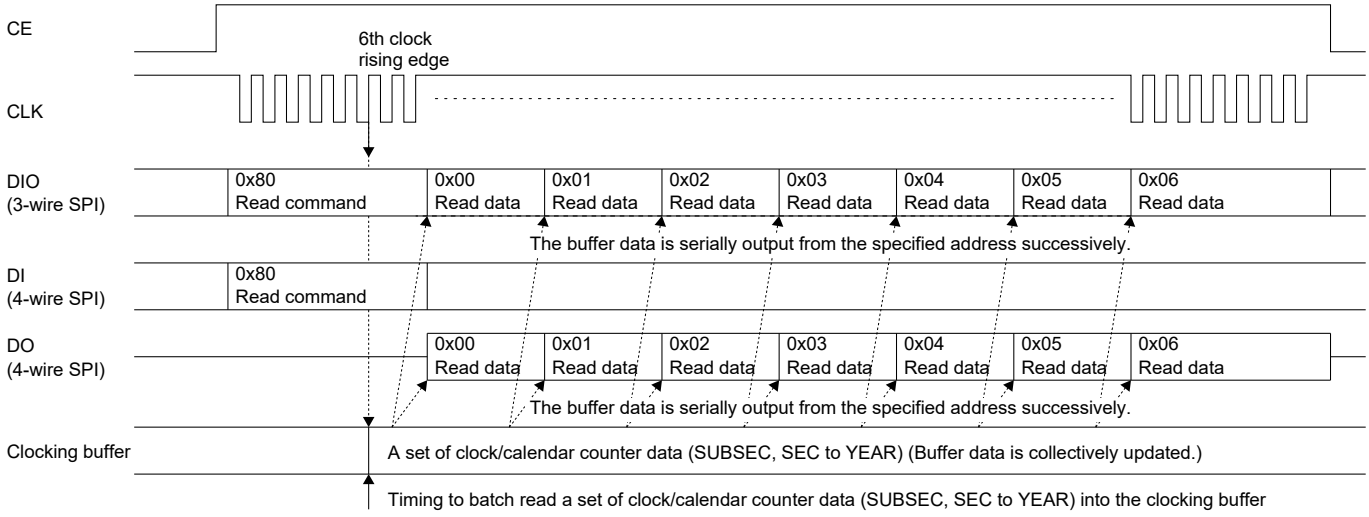
Accessing Clock/Calendar Counter through Clocking Buffer

The clock/calendar counters (1/1024-second, second, minute, hour, day-of-week, day, month, and year counters) are batch read/written into/from the clocking buffer. The host accesses the clocking buffer through Registers SEC to YEAR (Addresses 0x00 to 0x06), which allow reading/writing clock/calendar information in 1-second units, or Registers SUBSEC_L to YEAR_MIR (Addresses 0x10 to 0x18), which allow reading/writing information in 1/1024-second units. The clocking buffer accesses all the clock/calendar counters simultaneously to read/write their information that occupies multiple addresses. This allows reading/writing accurate time information. Furthermore, the conflict between the clocking buffer operation and a time update according to the internal 32.768 kHz clock is automatically arbitrated. Thus, the host can access the clocking buffer at any time.

The timings of the batch write from the clocking buffer to the clock/calendar counters and the batch read in reverse direction depend on the host interface as described below.

In the model with an SPI interface, the information written in the clocking buffer is collectively loaded to the clock/calendar counters at the falling edge of the CE signal. On the other hand, the clock/calendar counter values are simultaneously read into the clocking buffer at the rising edge of the 6th clock within a clock/calendar read command after the CE signal has risen.

Clock/calendar counter read by SPI model (continuous register read from SEC to YEAR)



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Clock/calendar counter write by SPI model (continuous register write from SEC to YEAR)

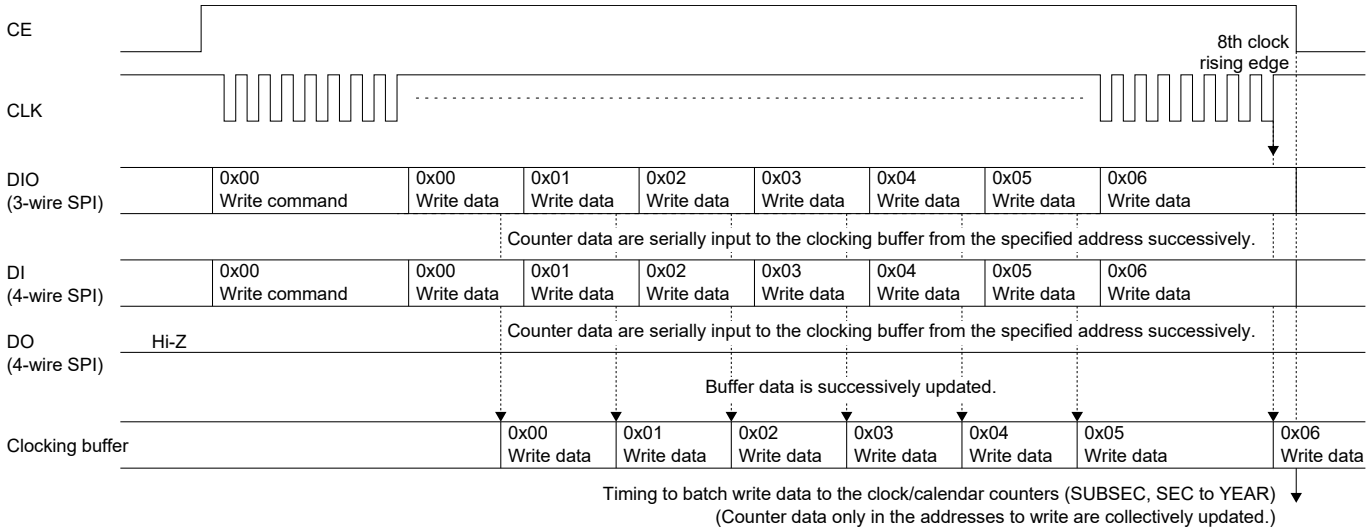
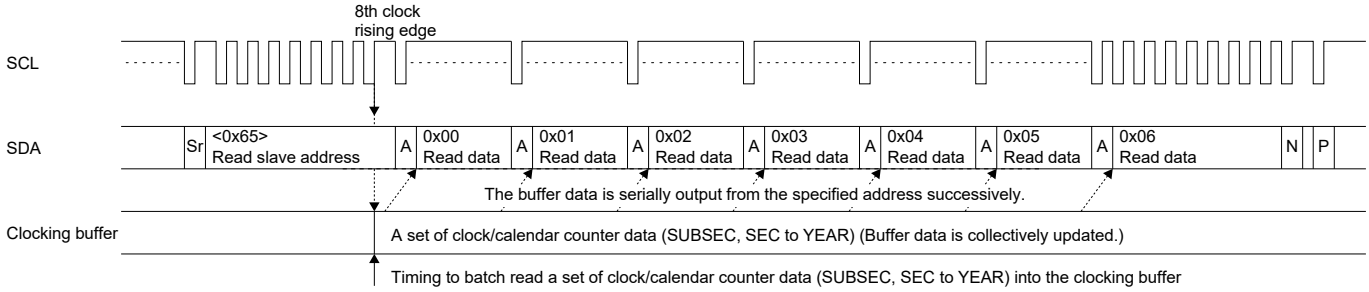


Figure 3.12 SPI Interface Clock/Calendar Counters Access Timing

In the model with an I²C-Bus interface, the information written in the clocking buffer is collectively loaded to the clock/calendar counters when a STOP or Repeated START condition has been received. On the other hand, the clock/calendar counter values are simultaneously read into the clocking buffer at the rising edge of SCL while an ACK is being sent after the 7-bit slave address with the 8th bit set to 1 (read) have been received.

Clock/calendar counter read by I²C-Bus model (continuous register read from SEC to YEAR)



Clock/calendar counter write by I²C-Bus model (continuous register write from SEC to YEAR)

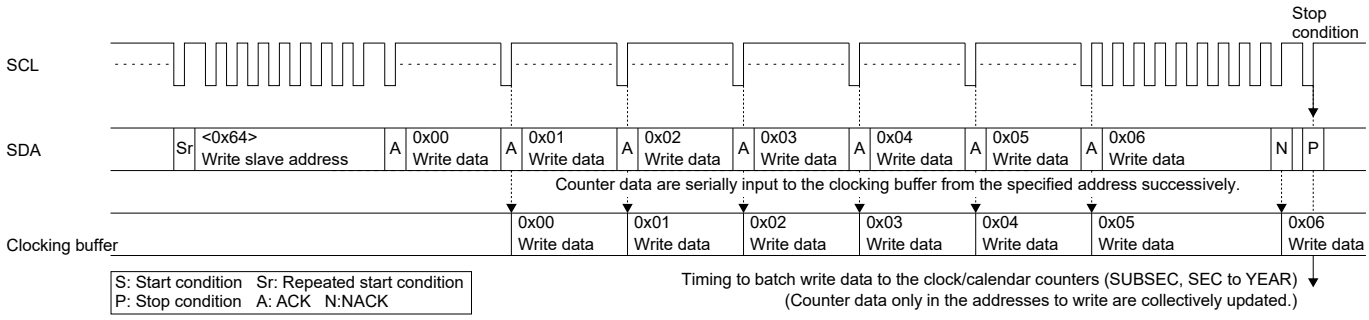


Figure 3.13 I²C-Bus Interface Clock/Calendar Counters Access Timing

Therefore, when writing or reading the clock/calendar data, perform continuous access for the required number of bytes using the automatic address increment function regardless of the interface included. Note that one continuous access for multiple bytes must be completed within 1 second in the model with an I²C-Bus interface, as it has a timeout function.

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Initial Setting and Starting Clock/Calendar

There are two methods for the clock/calendar initial settings: setting the clock/calendar in 1-second units and setting in 1/1024-second units. When setting in 1-second units, write the clock/calendar counter initial values to Register SEC (Address 0x00) through Register YEAR (Address 0x06). When setting in 1/1024-second units, write the initial values to Register SUBSC_L (Address 0x10) through Register YEAR_MIR (Address 0x18).

There are two methods to start clocking: terminating the communication by the host and clearing the TSTP_INTE.STOP bit by the host. Both methods have no difference in the time accuracy.

Example: To set the clock/calendar in 1-second units and to start clocking at the end of communication

1. Write multiple bytes of the clock/calendar information to the following registers continuously:
   - Register SEC (Address 0x0) (Second)
   - Register MIN (Address 0x1) (Minute)
   - Register HOUR (Address 0x2) (Hour)
   - Register WEEKDAY (Address 0x3) (Day of week)
   - Register DAY (Address 0x4) (Day)
   - Register MONTH (Address 0x5) (Month)
   - Register YEAR (Address 0x6) (Year)
2. Clocking starts when the continuous writing in Step 1 has terminated (at the falling edge of the CE signal in the model with an SPI interface or when a STOP condition or a Repeated START condition has received in the model with an I^2C-Bus interface).

Example: To set the clock/calendar in 1-second units and to start clocking by clearing the TSTP_INTE.STOP bit

1. Write 1 to the TSTP_INTE.STOP bit. (Stop clock/calendar counter)
2. Write multiple bytes of the clock/calendar information to the following registers continuously:
   - Register SEC (Address 0x0) (Second)
   - Register MIN (Address 0x1) (Minute)
   - Register HOUR (Address 0x2) (Hour)
   - Register WEEKDAY (Address 0x3) (Day of week)
   - Register DAY (Address 0x4) (Day)
   - Register MONTH (Address 0x5) (Month)
   - Register YEAR (Address 0x6) (Year)
3. Write 0 to the TSTP_INTE.STOP bit. (Start clock/calendar counter)
4. Clocking starts at the rising edge of the clock for writing Bit 0 (STOP bit) of Register TSTP_INTE in the model with an SPI interface or at the rising edge of the SCL while an ACK is being sent after writing to Register TSTP_INTE in the model with an I^2C-Bus interface.

Reading Clock/Calendar

The clock/calendar information in 1-second units should be read from Register SEC (Address 0x0) to Register YEAR (Address 0x06) or the information in 1/1024-second units should be read from Register SUBSEC_L (Address 0x10) to Register YEAR_MIR (Address 0x18).

In the model with an SPI interface, all the clock/calendar counter values are simultaneously read into the clocking buffer at the rising edge of the 6th clock within a clock/calendar read command after the CE signal has risen. The clock/calendar information loaded into the clocking buffer should be read continuously from Register SEC (Address 0x0) to Register YEAR (Address 0x06) or from Register SUBSEC_L (Address 0x10) to Register YEAR_MIR (Address 0x18) by the host.

In the model with an I^2C-Bus interface, the host first writes the read area start address, either Register SEC (Address 0x0) or Register SUBSEC_L (Address 0x10), then writes the 7-bit slave address with the 8th bit set to 1 (read). When this data is received, the RX8901CE sends an ACK back to the host and reads all the clock/calendar values simultaneously into the clocking buffer at the rising edge of the SCL input while an ACK is being sent. After that, the host continuously reads the buffered clock/calendar information.

When reading clock/calendar data, do not stop the clock/calendars by writing 1 to the TSTP_INTE.STOP bit, as it increases time error.

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Leap Year Determination

The RX4901CE/RX8901CE determines the years divisible by 4 as leap years, and others as common years. The count range of the day counter is automatically reconfigured in February. Therefore, software does not need any leap year processing from 2001 to 2099 A.D. Note that software must change the number of days in February as common years in 2100, 2200, and 2300 A.D.

Leap Second Correction Procedure

A leap second can be inserted by writing 0x60 to Register SEC_MIR (Address 0x12). This operation must be performed between 00 seconds and 01 second at the time in which a leap second will be inserted.

The second counter goes to 60 seconds by writing 0x60 and it is updated to 00 seconds from 60 seconds at the second update timing immediately after the writing. The Register SEC or SEC_MIR (Address 0x00 or 0x12) is read as 60 seconds from writing 0x60 to it being updated to 00 seconds. The second counter then performs normal counting operation from 00 seconds to 59 seconds.

Notes:
- Writing 0x60 to Register SEC at Address 0x00 resets the 1/1024-second counter. Therefore, use Register SEC_MIR at Address 0x12 for the leap second correction.
- It is prohibited to write 0x60 to Register SEC_MIR (Address 0x12) except for the time between 00 seconds and 01 second.

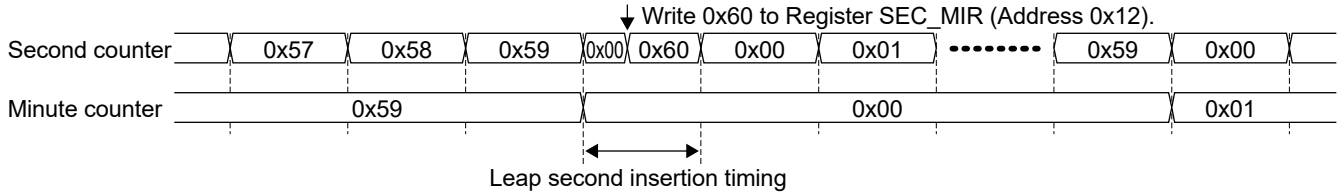


Figure 3.14 Leap Second Insertion Timing

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3.3 Temperature Compensation Function

The RX4901CE/RX8901CE includes a high-precision temperature compensation circuit. Seiko Epson records an oscillation frequency correction value that depends on the embedded temperature sensor characteristics to the internal memory of each RX4901CE/RX8901CE individually at shipping inspection. Based on this value, the temperature compensation circuit compensates the oscillation frequency fluctuation caused by temperature change.

3.3.1 Operations

Setting Temperature Compensation Interval

The temperature compensation circuit always operates if the power supply voltage is within the range of the temperature compensation operable voltage (V_{TMP}). To reduce current consumption, the temperature sensor measurement operation is performed intermittently. The execution interval can be set using the TSTP_INTE.CSEL[1:0] bits as shown in Table 3.5.

Table 3.5 Temperature Compensation Data Update Interval

TSTP_INTE.CSEL[1:0]	Update interval
0b00	0.5 seconds
0b01	2 seconds (default)
0b10	10 seconds
0b11	30 seconds

The temperature compensation circuit measures operating temperature using the embedded temperature sensor and suppresses frequency fluctuation according to the measured temperature.
In an environment with a rapid ambient temperature change, selecting a short temperature compensation data update interval can quickly follow a temperature change.
In an environment with a relatively slow ambient temperature change like a room, selecting a long temperature compensation data update interval can suppress current consumption.

The temperature compensation circuit cannot be disabled by a register operation. However, the temperature compensation update operation is suspended with the last captured temperature compensation data retained when the power supply voltage drops below V_{DET2}. If the power supply voltage is restored to V_{TMP} or more after that, the temperature compensation update operation resumes. An event interrupt can be generated when a V_{DET2} voltage drop is detected (for more information, refer to "*3.10 Time Stamp Function*").

Temperature Compensation Operation Flag: VTMPLF flag (0x0E)

The VTMPLF flag is set to 1 when the power supply voltage drops below the temperature compensation update stop detection voltage (V_{DET2}). In this case, the temperature compensation circuit stops and the oscillation continues under the last frequency correction condition before being stopped. The VTMPLF flag is cleared by writing 0 after the power supply voltage has been restored to above V_{TMP}.

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3.4 Time Update Interrupt Function

3.4.1 Overview

The RX4901CE/RX8901CE has a function to generate an interrupt at clock counter update timings. Its features are shown below.

- The interrupt timing can be selected from three update timings: every second, every minute, and every hour.
- The interrupt signal output from the /INT pin to the host is automatically cleared after a certain time.

Figure 3.15 shows the configuration of the time update interrupt circuit.

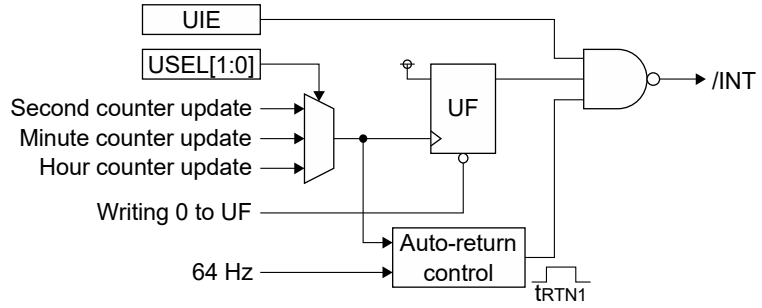


Figure 3.15 Configuration of Time Update Interrupt Circuit

3.4.2 Operations

Selecting Interrupt Period

Time update interrupts can be generated at the timing when a carry update occurs in one of the second, minute, and hour counters selected using the TCTL.USEL0 and UPDISEL.USEL1 bits (can generate an interrupt in 1-second, 1-minute, or 1-hour intervals, or can be disabled to generate interrupts). The interrupt signal output from the /INT pin to the host is automatically cleared after the prescribed time (t_{RTN1}) has elapsed.

Table 3.6 Selecting Time Update Interrupt Event

UPDISEL.USEL1	TCTL.USEL0	Interrupt event	/INT auto-return time (t_{RTN1})
0	0	Second counter update (default)	7.812 ms
0	1	Minute counter update	
1	0	Hour counter update	
1	1	No interrupt event	-

Interrupt Enabling/Disabling Procedure

The time update interrupt should be enabled/disabled as in the procedure below.

Enabling time update interrupts

1. Write 0 to the TSTP_INTE.UIE bit. (Cancel /INT output)
2. Configure the TCTL.USEL0 and UPDISEL.USEL1 bits. (Select time update interrupt event)
3. Write 0 to the INTF.UF bit. (Clear time update interrupt flag)
4. Write 1 to the TSTP_INTE.UIE bit. (Enable time update interrupt)

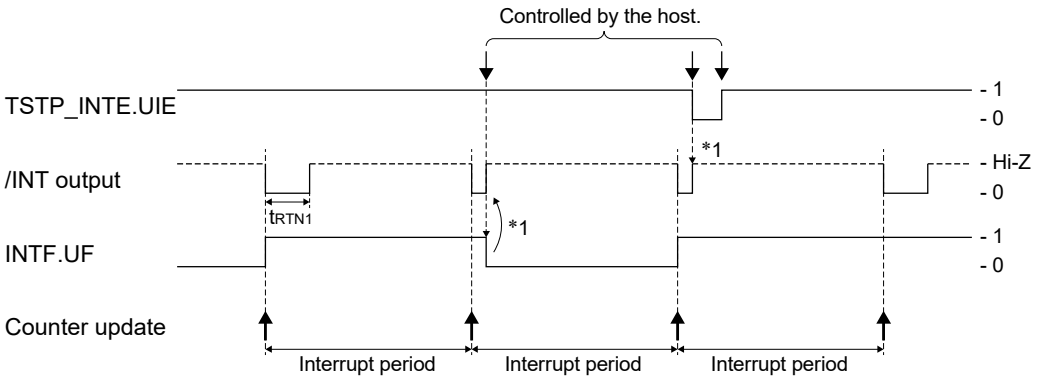
Disabling time update interrupts

1. Write 0 to the TSTP_INTE.UIE bit. (Cancel /INT output, disable output)
2. Write 0 to the INTF.UF bit. (Clear time update interrupt flag)

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Interrupt Operations

When an interrupt generation timing selected via software is reached, INTF.UF bit is set to 1. If the TSTP_INTE.UIE bit = 1 (interrupt enabled) at this time, the /INT pin goes low to output an interrupt request to the host. After that, the /INT pin goes into a Hi-Z state when 0 is written to the TSTP_INTE.UIE bit or automatically goes into a Hi-Z state after t_{RTN1} (7.812 ms) has elapsed from the beginning of a low output from the /INT pin. The INTF.UF bit is not cleared even if the /INT pin goes into a Hi-Z state after t_{RTN1} has elapsed from occurrence of an interrupt request. It is cleared when 0 is written by the host.



*1 Clearing the INTF.UF bit or TSTP_INTE.UIE bit by writing 0 puts the /INT pin into an open (Hi-Z) state without waiting t_{RTN1}.

Figure 3.16 Time Update Interrupt Timing Chart

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3.5 Alarm Function

3.5.1 Overview

The following shows the features of the alarm function:

- Days of the week or a day, an hour, a minute, and a second can be combined to specify alarm times.
- Allows various alarm settings simply by combining date and time conditions arbitrarily, such as 10 A.M. every Friday and Saturday, and 7 P.M. on the 25th of every month.

Figure 3.17 shows the configuration of the alarm circuit.

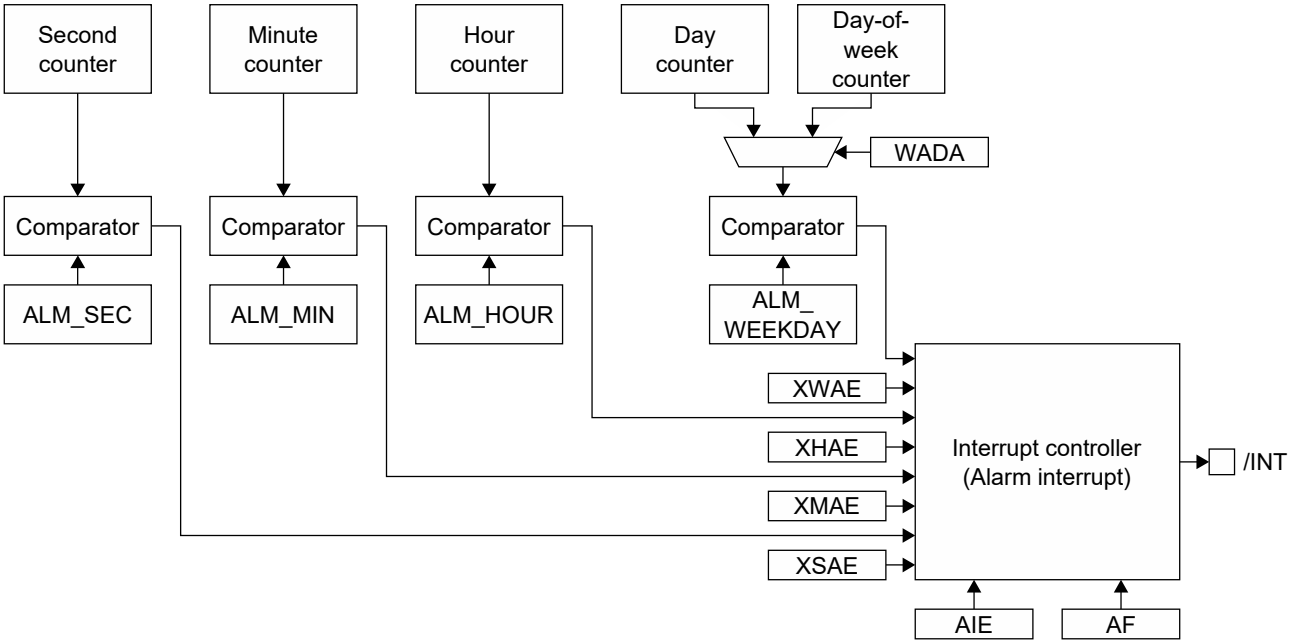


Figure 3.17 Configuration of Alarm Circuit

3.5.2 Operations

Alarm Setting Procedure

The following shows a procedure to set an alarm to generate an interrupt:

1. Write 0 to the TSTP_INTE.AIE bit. (Disable alarm interrupts)
2. Set the alarm second to Register ALM_SEC.
   - XSAE bit (Enable/disable alarm second)
   - SALM_H[2:0] bits (Specify 10-second digit)
   - SALM_L[3:0] bits (Specify 1-second digit)
3. Set the alarm minute to Register ALM_MIN (or ALM_MIN_MIR).
   - XMAE bit (Enable/disable alarm minute)
   - MALM_H[2:0] bits (Specify 10-minute digit)
   - MALM_L[3:0] bits (Specify 1-minute digit)
4. Set the alarm hour to Register ALM_HOUR (or ALM_HOUR_MIR).
   - XHAE bit (Enable/disable alarm hour)
   - HALM_H[1:0] bits (Specify 10-hour digit)
   - HALM_L[3:0] bits (Specify 1-hour digit)

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5. Set the alarm day-of-week or alarm day to Register ALM_WEEKDAY (or ALM_WEEKDAY_MIR).
   - XWAE bit (Enable/disable alarm day-of-week/day)

   When specifying alarm day-of-week (TCTL.WADA bit = 0)
   - WKALM[6:0] bits (Specify days of week)

   These bits allow specification of more than one day a week, such as Monday to Friday.

   When specifying alarm day (TCTL.WADA bit = 1)
   - DALM_H[1:0] bits (Specify 10-day digit)
   - DALM_L[3:0] bits (Specify 1-day digit)
6. Set the TCTL.WADA bit. (Select day-of-week/day alarm)
7. Write 0 to the INTF.AF bit. (Clear alarm interrupt flag)
8. Write 1 to the TSTP_INTE.AIE bit. (Enable alarm interrupts)

* Setting the X*AE bit to 1 excludes its register setting from the alarm condition. For example, when ALM_WEEKDAY.XWAE bit = 1, day-of-week/day setting is disabled so that an alarm will occur at the specified time every day. However, if all the X*AE bits are set to 1, an alarm will occur every second.

Alarm Setting Examples

Alarm setting examples with day of the week specified (TCTL.WADA bit = 0)

Setting example 1

ALM_WEEKDAY (Day-of-week alarm)								ALM_HOUR	ALM_MIN	ALM_SEC
XWAE	SAT	FRI	THU	WED	TUE	MON	SUN	(Hour alarm)	(Minute alarm)	(Second alarm)
0	0	1	1	1	1	1	0	0x07	0x00	XSAE = 1

An alarm will occur repeatedly in one second intervals from 7:00:00 to 7:00:59 A.M., Monday to Friday every week.

Setting example 2

ALM_WEEKDAY (Day-of-week alarm)								ALM_HOUR	ALM_MIN	ALM_SEC
XWAE	SAT	FRI	THU	WED	TUE	MON	SUN	(Hour alarm)	(Minute alarm)	(Second alarm)
0	1	0	0	0	0	0	1	XHAE = 1	0x30	0x00

An alarm will occur at the 30-minute mark of every hour, Saturday and Sunday every week.

Setting example 3

ALM_WEEKDAY (Day-of-week alarm)								ALM_HOUR	ALM_MIN	ALM_SEC
XWAE	SAT	FRI	THU	WED	TUE	MON	SUN	(Hour alarm)	(Minute alarm)	(Second alarm)
0	1	1	1	1	1	1	1	0x18	0x59	0x30
1	X	X	X	X	X	X	X			

An alarm will occur at 6:59:30 P.M. every day.

Alarm setting examples with day specified (TCTL.WADA bit = 1)

Setting example 4

ALM_WEEKDAY (Day alarm)								ALM_HOUR	ALM_MIN	ALM_SEC
XWAE	*	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	(Hour alarm)	(Minute alarm)	(Second alarm)
0	X	0	0	0	0	0	1	0x07	XMAE = 1	XSAE = 1

An alarm will occur repeatedly in one second intervals from 7:00:00 to 7:00:59 A.M., on the first day of every month.

Setting example 5

ALM_WEEKDAY (Day alarm)								ALM_HOUR	ALM_MIN	ALM_SEC
XWAE	*	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	(Hour alarm)	(Minute alarm)	(Second alarm)
0	X	0	1	0	1	0	1	XHAE = 1	0x30	0x00

An alarm will occur at 30:00 every hour, on the 15th of every month.

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Setting example 6

ALM_WEEKDAY (Day alarm)								ALM_HOUR (Hour alarm)	ALM_MIN (Minute alarm)	ALM_SEC (Second alarm)
XWAE	*	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			
1	X	X	X	X	X	X	X	0x18	0x59	0x30

An alarm will occur at 6:59:30 P.M. every day.

X: Don't care.

Alarm Interrupt

Figure 3.18 shows the configuration of the alarm interrupt circuit.

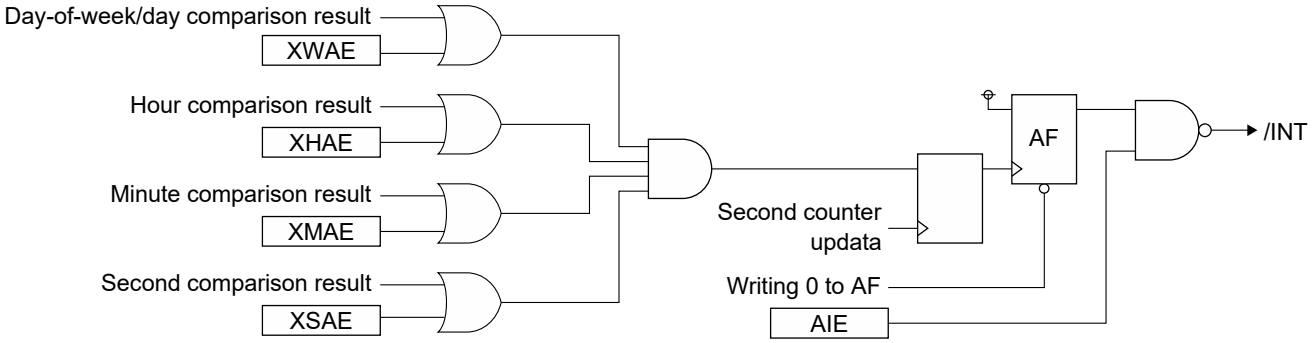
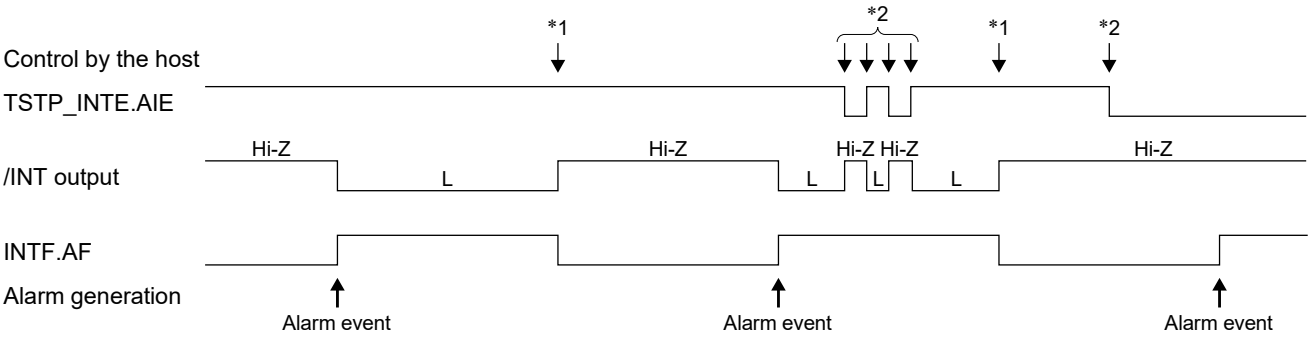


Figure 3.18 Configuration of Alarm Interrupt Circuit

Alarm interrupts can be generated when the time/calendar counters reach the date and time specified using Registers ALM_SEC, ALM_MIN, ALM_HOUR, and ALM_WEEKDAY.
The INTF.AF bit is set to 1 at the specified time and day of week/day. If the TSTP_INTE.AIE bit = 1 (interrupt enabled) at this time, the /INT pin goes low to output an interrupt request to the host. The INTF.AF bit that has been set to 1 is cleared by writing 0. At the same time, the /INT pin goes into a Hi-Z state.



*1 Clearing the INTF.AF bit by writing 0 puts the /INT pin into an open (Hi-Z) state.
*2 Setting the TSTP_INTE.AIE bit to 0 puts the /INT pin into an open (Hi-Z) state regardless of the INTF.AF bit setting.

Figure 3.19 Alarm Interrupt Timing Chart

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3.6 Wakeup Timer Function

3.6.1 Overview

The following shows the features of the wakeup timer function:

- The timer consists of a 24-bit presettable up counter.
- The source clock is selectable from 1024 Hz, 64 Hz, 1 Hz, and 1/60 Hz.
- An interrupt can be generated in an optional cycle from 976 µs to 32 years.
- The interrupt output can also be assigned to the FOUT pin.
- Can be used for time integration of the operation with the main power supply in conjunction with the auto power switching function

Figure 3.20 shows the configuration of the wakeup timer.

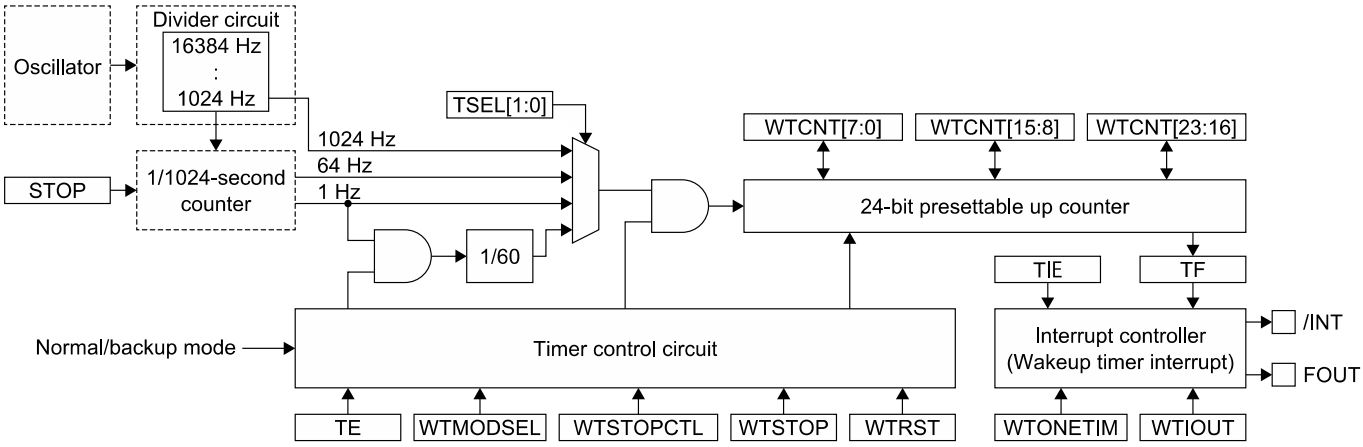


Figure 3.20 Configuration of Wakeup Timer

3.6.2 Operations

Source Clock

The source clock can be selected from the four clocks listed in Table 3.7 using the TCTL.TSEL[1:0] bits.

Table 3.7 Wakeup Timer Source Clock Selection

TCTL.TSEL[1:0]	Source clock		/INT auto-return time (t_{RTN2})
	Frequency	Cycle	
0b00	1024 Hz	976 µs	488 µs
0b01	64 Hz	15.625 ms	7.812 ms
0b10	1 Hz	1 second	7.812 ms
0b11	1/60 Hz	60 seconds	7.812 ms

* t_{RTN2} is the time after the /INT pin goes low until it is automatically placed into open (Hi-Z) state.

Preset Data (wakeup timer interrupt period)

Preset data specifies the count upper limit value to determine the wakeup timer interrupt period. The wakeup timer generates an interrupt when the count value exceeds the preset data. Write preset data to Registers WTCNT_L, WTCNT_M, and WTCNT_H when the TCTL.TE bit = 0.

Notes: • Be sure to avoid writing preset data to Registers WTCNT_L, WTCNT_M, and WTCNT_H while the timer is operating (TCTL.TE bit = 1).

• The preset data cannot be set to 0x000000. If 0x000000 is written to Registers WTCNT_L, WTCNT_M, and WTCNT_H, the wakeup timer cannot perform counting up and an interrupt does not occur.

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Table 3.8 lists examples of wakeup timer interrupt periods according to combinations of the preset data and source clock settings.

Table 3.8 Examples of Wakeup Timer Interrupt Periods

Preset data	Source clock			
	1024 Hz TCTL.TSEL[1:0] = 0b00	64 Hz TCTL.TSEL[1:0] = 0b01	1 Hz TCTL.TSEL[1:0] = 0b10	1/60 Hz TCTL.TSEL[1:0] = 0b11
0	–	–	–	–
1	976 µs	15.625 ms	1 second	60 seconds
:	:	:	:	:
410 (0x00019A)	400.39 ms	6.406 seconds	410 seconds	410 minutes
:	:	:	:	:
3840 (0x000F00)	3.7500 seconds	60 seconds	3840 seconds	3840 minutes
:	:	:	:	:
4096 (0x001000)	4 seconds	64 seconds	4096 seconds	4096 minutes
:	:	:	:	:
16777215 (0xFFFFFF)	4.55 hours	72.81 hours	4660 hours	31.9 years

Counting Condition

Setting the WTCTL.WTSTOPCTL bit to 1 enables the WTCTL.WTMODSEL bit setting to select whether the counting will be performed only in Normal mode or Backup mode.

Table 3.9 Setting of Normal Mode/Backup Mode Condition for Counting

WTCTL.WTSTOPCTL	WTCTL.WTMODSEL	Counting condition
0	X	Enables counting in both Normal and Backup modes.
1	0	Enables counting in Normal mode (in V_{DD} operation) only.
	1	Enables counting in Backup mode (in V_{BAT} operation) only.

For example, when counting is enabled in Normal mode only, the counting stops when the RX4901CE/RX8901CE enters Backup mode. The RX4901CE/RX8901CE retains the counter value at this point and resumes counting from that value after returning to Normal mode again. This makes it possible to use the wakeup timer as an integrating meter that measures the operating time during Normal mode.

Wakeup Timer Setting Procedure

The following shows the procedure to set the wakeup timer to generate an interrupt:

1. Write 0 to the TCTL.TE bit. (Disable wakeup timer)
2. Write 0 to the TSTP_INTE.TIE bit. (Disable wakeup timer interrupts)
3. Configure the TCTL.TSEL[1:0] bits. (Select source clock)
4. Configure Registers WTCNT_L, WTCNT_M, and WTCNT_H. (Set wakeup timer interrupt period)
5. Configure Register WTICFG. (Configure interrupt output)
   - WTONETIM bit (Set /INT auto-return function)
   - WTIOUT bit (Select interrupt output pin)
6. Configure Register WTCTL. (Set timer operating condition)
   - WTMODSEL and WTSTOPCTL bits (Select Normal/Backup mode operating condition)
   - Write 0 to the WTSTOP bit. (Cancel suspending)
7. Write 0 to the INTF.TF bit. (Clear wakeup timer interrupt flag)
8. Write 1 to the TSTP_INTE.TIE bit. (Enable wakeup timer interrupts)
9. Write 1 to the TCTL.TE bit. (Enable wakeup timer)

   This starts counting.

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Starting Count Up

The wakeup timer loads the initial value (1) to the counter and starts counting up when the TCTL.TE bit is set to 1. However, the counting starts in async with the source clock, so a maximum of one source clock cycle of delay occurs until the first counting up.

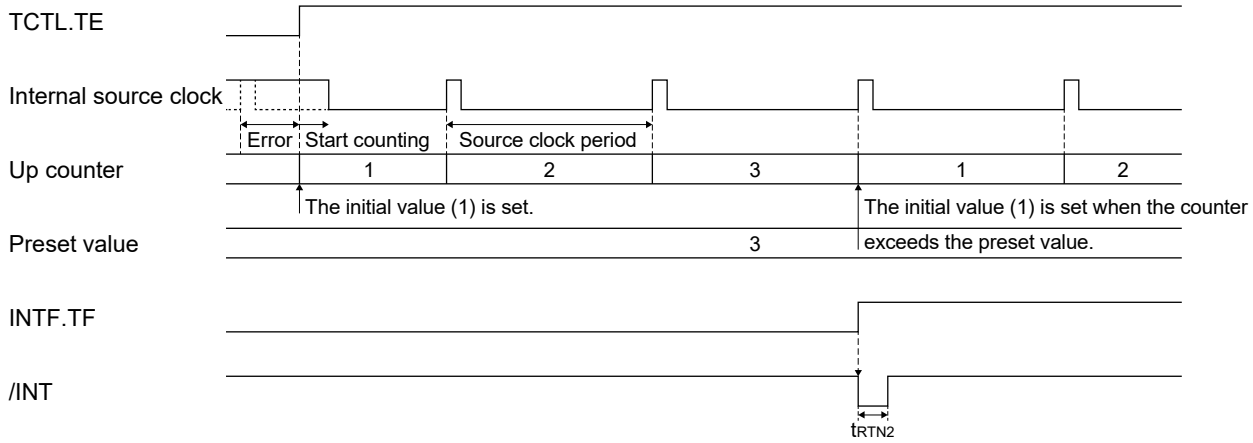


Figure 3.21 Wakeup Timer Count-Up Operation

When the counter exceeds the preset value by counting up, the initial value (1) is loaded to the counter and the counting continues.

Figure 3.22 shows the count start timing after 1 is written to the TCTL.TE bit.

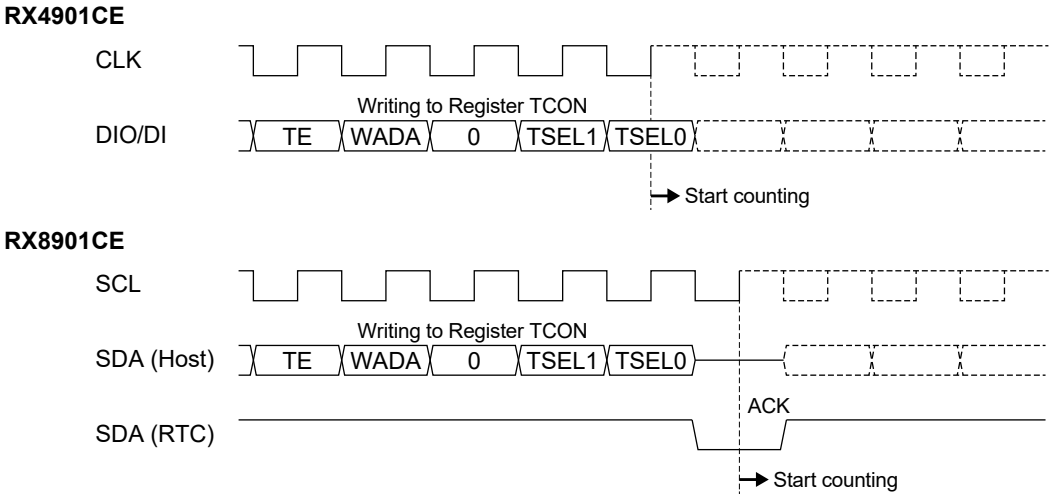


Figure 3.22 Wakeup Timer Count Start Timing

Suspension

To suspend the wakeup timer counting operation, write 1 to the WTCTL.WTSTOP bit. The wakeup timer stops with the counter value at that point retained. When 0 is written to the WTCTL.WTSTOP bit, the wakeup timer resumes counting up from the retained value. This suspending/resuming is performed in async with the source clock, a same error as the time of starting occurs.

Note that the counter will not stop by the WTCTL.WTSTOP bit depending on the setting status of other bits. Table 3.10 shows the wakeup timer operating status according to the related control bit settings.

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Table 3.10 Control of Wakeup Timer Operation

TCTL.TE	TSTP_INTE.STOP	WTCTL.WTSTOPCTL	WTCTL.WTSTOP	Operating status
1	0	0	0	Counting up is in progress.
			1	Counting up is suspended.
		1	X	The WTCTL.WTSTOP bit setting is disabled; setting it to 1 does not suspend counting.
	1	X	X	The counter stops. However, when the source clock = 1024 Hz, the timer performs the same operation as when the TSTP_INTE.STOP bit = 0.
0	X	X	X	The counter is idle.

Reading Counter Data

When the TCTL.TE bit = 1, the counter data can be read from Registers WTCNT_L, WTCNT_M, and WTCNT_H even while it is counting up. However, the valid current value may not be read, as the counter may change while three registers are being read. Therefore, read these registers twice within a wakeup timer source clock cycle and determine that the correct value could be read if both values are the same. If both values are not the same, try to read the registers again.

When the TCTL.TE bit = 1, the wakeup timer preset value is read out from Registers WTCNT_L, WTCNT_M, and WTCNT_H.

Resetting Counter

Writing 1 to the WTCTL.WTRST bit resets the counter being operated. The wakeup timer resumes counting immediately after loading the initial value (1) to the counter. At this time, a wakeup timer interrupt is not generated.

Wakeup Timer Interrupt

Figure 3.23 shows the configuration of the wakeup timer interrupt circuit.

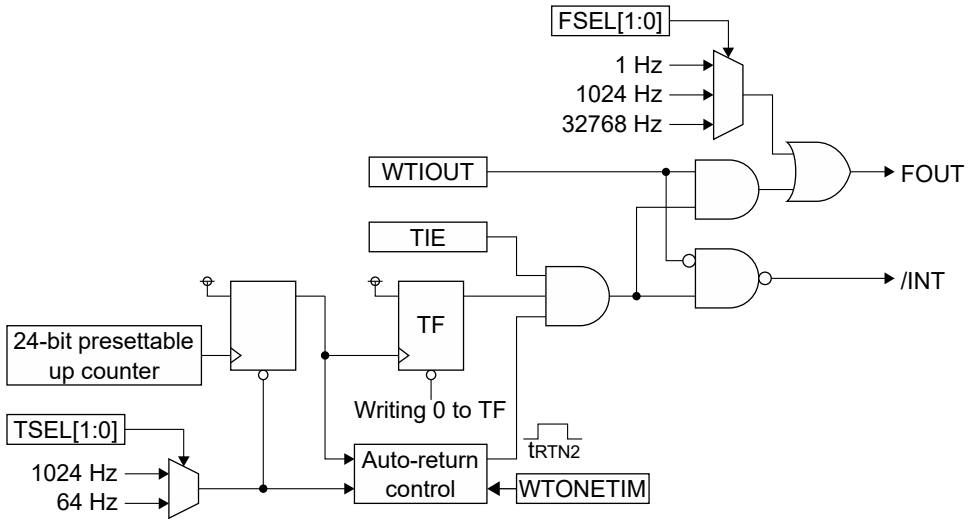
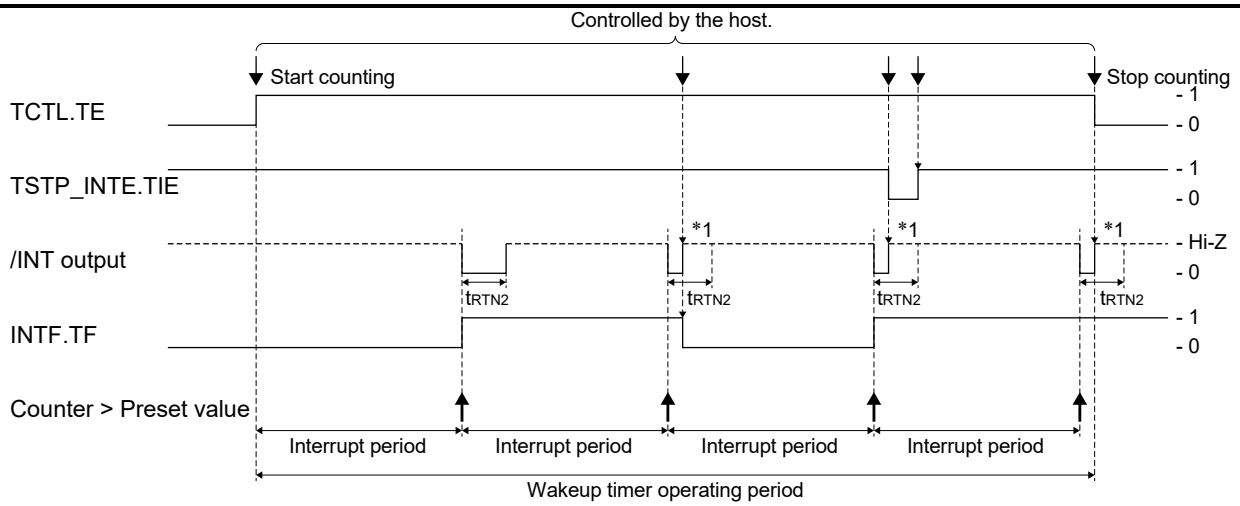


Figure 3.23 Configuration of Wakeup Timer Interrupt Circuit

Wakeup timer interrupts can be generated in the preset count cycle.
The INTF.TF bit is set to 1 at the moment the wakeup timer counter value exceeds the preset value by counting up. If the TSTP_INTE.TIE bit = 1 (interrupt enabled) at this time, the /INT pin goes low to output an interrupt request to the host and returns into a Hi-Z state after the /INT auto-return time (t_{RTN2}, see Table 3.7) has elapsed. The /INT auto-return function can be disabled by setting the WTICFG.WTONETIM bit to 1.
Although the /INT pin automatically returns into a Hi-Z state, the INTF.TF bit that has been set retains 1 until 0 is written by the host. When 0 is written to the INTF.TF bit or TSTP_INTE.TIE bit, the /INT pin returns into a Hi-Z state regardless whether the /INT auto-return time has elapsed or not.

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*1 Clearing the INTF.TF, TSTP_INTE.TIE, or TCTL.TE bits to 0 puts the /INT pin into an open (Hi-Z) state without waiting t_{RTN2}.

Figure 3.24 Wakeup Timer Interrupt Timing Chart

When the WTICFG.WTIOUT bit = 0, the wakeup timer interrupt request signal is NORed with other interrupt request signals and output from the /INT pin.
In the model of which the FOUT pin is enabled, the wakeup timer interrupt request signal can also be output from the FOUT pin by setting the WTICFG.WTIOUT bit to 1.

Note: When the WTICFG.WTIOUT bit = 1, the wakeup timer interrupt request signal is NORed with the FOUT signal and output from the FOUT pin. To output the wakeup timer interrupt request signal only, set the TCTL.FSEL[1:0] bits to 0b11 to disable the FOUT output.

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3.7 FOUT Output Function

3.7.1 Overview

The features of the FOUT output function are shown below.

- A clock generated in the RX4901CE/RX8901CE can be output externally.
- The output clock can be selected from 32.768 kHz, 1024 Hz, and 1 Hz.
- The FOUT output can be controlled using a register or an external input signal (FOE).

Figure 3.25 shows the configuration of the FOUT output circuit.

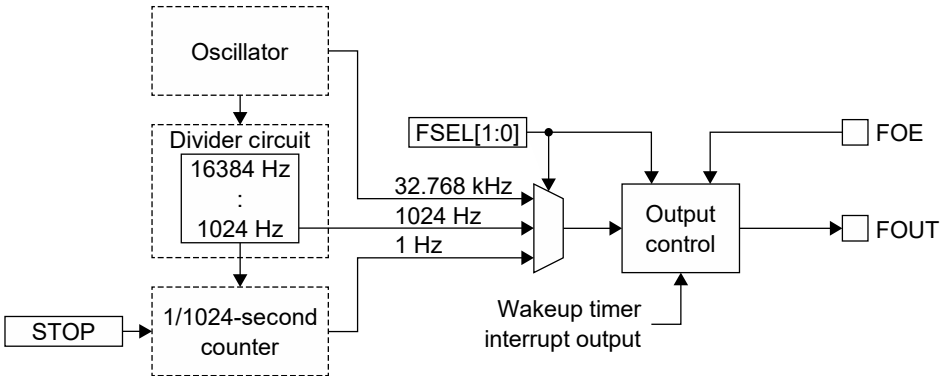


Figure 3.25 Configuration of FOUT Output Circuit

3.7.2 Operations

Initial Settings

FOUT output (Pin 4): In the Option A and C products, Pin 4 has been set to FOUT by default.
To use the FOUT output in the Option A or D product, the Pin 4 function assignment must be changed (set the WTICFG.EVIN3MUX bit to 0).

FOE input (Pin 10): To control the FOUT output with an external input signal (FOE), the Pin 10 function assignment must be changed (set the WTICFG.FOEMUX bit to 1).

Controlling FOUT Output (when not using the FOE pin)

The FOUT output is disabled (Hi-Z) at power-on. The TCTL.FSEL[1:0] bits are used to enable or disable (Hi-Z) the FOUT output. Note that the TSTP_INTE.STOP bit setting affects the 1 Hz output setting.

Table 3.11 FOUT Output Selection

TCTL.FSEL[1:0]	TCTL.FSEL[1:0]	Output clock
0	0b00	32.768 kHz
	0b01	1024 Hz
	0b10	1 Hz
	0b11	Off (Hi-Z)
1	0b00	32.768 kHz
	0b01	1024 Hz
	0b10	Fixed at H or L
	0b11	Off (Hi-Z)

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Controlling FOUT Output (when using the FOE pin)

By setting the WTICFG.FOEMUX bit to 1 at initial setting, the Pin 10 function assignment is changed from EVIN2 input to FOE input allowing the FOE input signal to control the FOUT output. The FOUT output clock frequency should be selected using the TCTL.FSEL[1:0] bits (see Table 3.11).

While the FOE input signal is a high level, the FOUT signal with the frequency selected by setting the TCTL.FSEL[1:0] bits is output from the FOUT pin. While the FOE input signal is a low level, the FOUT pin goes into a Hi-Z state.

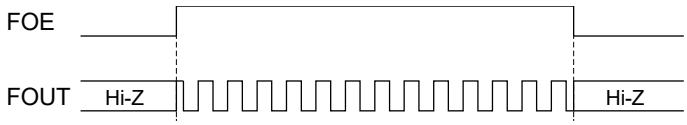


Figure 3.26 FOUT Output by FOE Control

Wakeup Timer Interrupt Signal Output from FOUT pin

If the clock output is not necessary, the FOUT pin can be used as the wakeup timer interrupt request signal output pin by setting the WTICFG.WTIOUT bit to 1. The selected clock and the wakeup timer interrupt request signal are NORed to output together from the FOUT pin if the TCTL.FSEL[1:0] bits are set to other than 0b11.

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3.8 Self-Monitoring Function

3.8.1 Overview

The RX4901CE/RX8901CE includes a function to monitor the power supply voltage and oscillation statuses, and provides the status flags for software to read the monitoring results. These flags can also be used as a time stamp trigger and recording data, and an event detection interrupt source. The following lists the monitoring items:

- Power-on reset execution (PORF flag, VLF flag)
- Oscillation stoppage (OSCSTPF flag, VLF flag)
- Drop of main power supply voltage (V_{DD}) (VDDLF flag)
- Drop of backup power supply voltage (V_{BAT}) (VBATLF flag)
- Drop of power supply voltage (V_{DD}/V_{BAT}) below temperature compensation update stop voltage (VTMPLF flag)

The /INT pin can output the status of these status flags to an external device except for the PORF and VLF flags.

3.8.2 Self-Monitoring Flags

Power-On Reset Detection: PORF flag

The PORF flag (INTF.PORF bit) is set to 1 when a power-on reset execution is detected after power is turned on. This flag does not automatically revert to 0 even if the power-on reset is cancelled after that. When the INTF.PORF bit = 1, perform necessary initial settings and clear the INTF.PORF bit by writing 0.

Crystal Oscillation Stop Detection: OSCSTPF flag

The OSCSTPF flag (INTF.OSCSTPF bit) is set to 1 when the built-in crystal oscillator stops oscillating for 10 ms or more. This flag does not automatically revert to 0 after being set to 1 even if the oscillation is restored. When the INTF.OSCSTPF bit = 1, perform necessary initial settings and clear the INTF.OSCSTPF bit by writing 0.

This flag is also used for a time stamp trigger and an event detection interrupt. For more information, refer to "*3.10.5 Time Stamp (Event Detection) Interrupts*."

Invalid Date and Time Data Warning: VLF Flag

The VLF flag (INTF.VLF bit) is set to 1 when the above PORF flag or OSCSTPF flag is set. If the INTF.VLF bit, this flag, is 1 after turning the V_{DD} power on or restoring from Backup mode, initial settings are required. For an initial setting procedure including INTF.VLF bit manipulations, refer to "*2.2.3 Initial Settings*."

V_{DD} Voltage Drop Detection: VDDLF flag

This flag is effective only when the PWSW_CFG.INIEN bit = 1 (auto power switching function enabled).

The VDDLF flag (BUF_INTF.VDDLF bit) is set to 1 when the main power supply voltage (V_{DD}) drops below the V_{DD} drop detection voltage ($-V_{DET1}$). This flag does not automatically revert to 0 even if V_{DD} rises to V_{DD} rise detection voltage ($+V_{DET1}$) or more. The BUF_INTF.VDDLF bit is cleared by writing 0 after V_{DD} has restored to $+V_{DET1}$ or more.

This flag is also used for a time stamp trigger and an event detection interrupt. For more information, refer to "*3.10.5 Time Stamp (Event Detection) Interrupts*."

V_{BAT} Voltage Drop Detection: VBATLF flag

This flag is effective only when the PWSW_CFG.INIEN bit = 1 (auto power switching function enabled).

The VBATLF flag (BUF_INTF.VBATLF bit) is set to 1 when the backup power supply voltage (V_{BAT}) drop status, which is below the V_{BAT} drop detection voltage ($-V_{LOW}$), is successively detected twice. The BUF_INTF.VBATLF bit is cleared by writing 0 after V_{BAT} has risen to the V_{BAT} rise detection voltage ($+V_{LOW}$) or more.

This flag is also used for a time stamp trigger and an event detection interrupt. For more information, refer to "*3.10.5 Time Stamp (Event Detection) Interrupts*."

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Temperature Compensation Update Stop Detection: VTMPLF flag

The VTMPLF flag (INTF.VTMPLF bit) is set to 1 when the V_{OUT} voltage (V_{DD} or V_{BAT}) drops to the temperature compensation update stop voltage (V_{DET2}) or less. In this case, the temperature compensation circuit stops and the oscillation continues under the last frequency correction condition before being stopped. The INTF.VTMPLF bit is cleared by writing 0 after V_{OUT} has risen above V_{TMP}.

This flag is also used for a time stamp trigger and an event detection interrupt. For more information, refer to "*3.10.5 Time Stamp (Event Detection) Interrupts*."

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3.9 Auto Power Switching Function

3.9.1 Overview

The auto power switching function monitors the main power supply (V_{DD}) and backup power supply (V_{BAT}) voltages and switches between them so that the operating power voltage V_{OUT} can be appropriately maintained. When the main power supply voltage has dropped, the operating power source is switched from the main power supply to the backup power supply. If the main power supply voltage is restored after that, operating power source is switched back to the main power supply again.

- Switches the operating power supply to V_{BAT} when V_{DD} drops.
- Can charge V_{BAT} from V_{DD} when $V_{DD} > V_{BAT}$.
- Switches the operating power supply to V_{DD} when the V_{DD} voltage resumes while the RX4901CE/RX8901CE is operating with V_{BAT}.

Figure 3.27 shows the configuration of the auto power switching circuit.

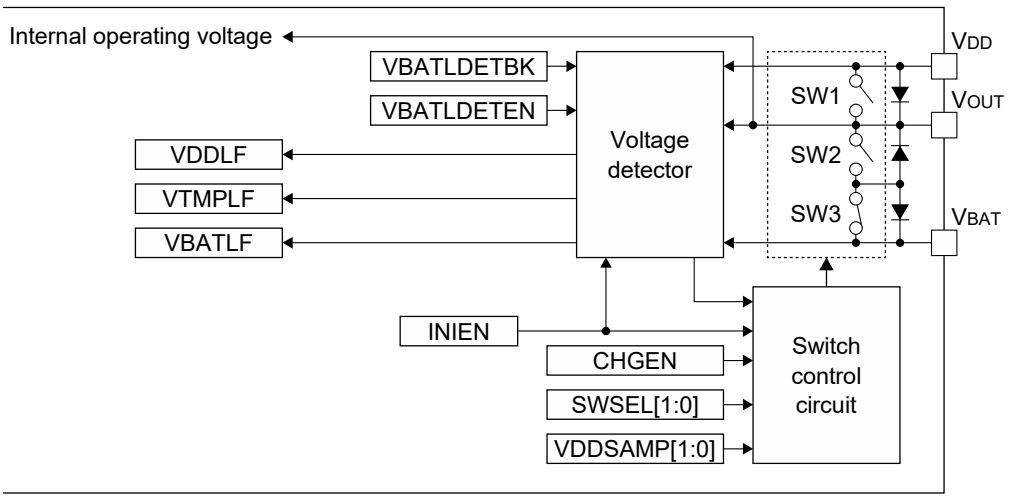


Figure 3.27 Auto Power Switching Circuit

3.9.2 Operations

Operating Mode

By enabling the auto power switching function, two operating modes become usable.

Normal Mode (with transition to Backup mode enabled)

This mode operates the RX4901CE/RX8901CE with the main power supply V_{DD}. The host can access the RX4901CE/RX8901CE registers including the clock/calendar counter registers. The RX4901CE/RX8901CE keeps detecting the voltage level of the main power supply voltage V_{DD} during this mode, and the operating mode transits to Backup mode if V_{DD} drops to the V_{DD} drop detection voltage $-V_{DET1}$ or below.

Backup mode

This mode operates the RX4901CE/RX8901CE with the backup power supply V_{BAT}. The V_{DD} pin is automatically disconnected from the backup power supply V_{BAT} by the internal power switch SW1 so that current will not flow from V_{BAT} to the main power supply V_{DD}.
The host interface is disabled and the CE, CLK, DI, DIO, SDA, and SCL input pins can be placed into a floating state. The DO and FOUT output pins go into a Hi-Z state.
If the V_{BAT} voltage is equal to or higher than the time keeping voltage V_{CLK}, the clock/calendar function, EVIN*n* input, and /INT output activity is similar to Normal mode.

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Setting when Using Auto Power Switching Function

When using the auto power switching function, configure Register PWSW_CFG as below, because this function is disabled by default.

1. Set the PWSW_CFG.CHGEN bit. (Enable/disable charging V_{BAT})

   Set to 1 when a chargeable battery such as a secondary battery or EDLC is connected to V_{BAT}.

2. Set the PWSW_CFG.INIEN bit to 1. (Enable auto power switching function)

   Setting the PWSW_CFG.INIEN bit to 1 disables the PWSW_CFG.SWSEL[1:0] bits that control the SW1 to SW3 states. The switch states will be automatically controlled by the auto power switching function.

3. Set the PWSW_CFG.VBATLDETBK bit. (Enable/disable V_{BAT} voltage detection in backup mode)
4. Set the PWSW_CFG.VBATLDETEN bit to 1. (Enable V_{BAT} voltage detection)
5. Set the PWSW_CFG.VDDSAMP[1:0] bit. (Set V_{DD} voltage sampling period)

Setting when Not Using Auto Power Switching Function

The auto power switching function is disabled by default, therefore, switching between the main power supply (V_{DD}) and the backup power supply (V_{BAT}), and charging to the backup power supply (V_{BAT}) are not performed.

The power switches are set as (SW1 = OFF, SW2 = OFF, SW3 = ON) immediately after power-on, and the main power supply (V_{DD}) and the backup power supply (V_{BAT}) are connected in parallel through the diodes in this module. These diodes prevent current to flow between V_{DD} and V_{BAT}, however, a voltage drop for the forward voltage V_F of the diode occurs. Therefore, the RTC operating voltage V_{OUT} is reduced from the V_{DD} or V_{BAT}, whichever one is higher, by V_F.

To avoid this voltage drop, when the main power supply (V_{DD}) only is used, set the PWSW_CFG.SWSEL[1:0] bits to 0b10 to set the switches as (SW1 = ON, SW2 = OFF, SW3 = OFF) (see Figure 2.4).

When the auto power switching function is not used, the V_{BAT} voltage drop detection function is disabled.

Auto Power Switching Operations

When power is turned on

The power switching control bits and switches are configured as shown below at power on.

PWSW_CFG.INIEN bit = 0 (Disable auto power switching function)
PWSW_CFG.CHGEN bit = 0 (Disable charging V_{BAT})
PWSW_CFG.SWSEL[1:0] bit = 0b01 (SW1 = OFF, SW2 = OFF, SW3 = ON)

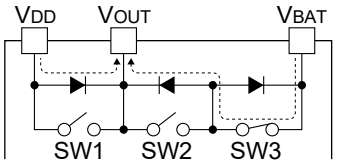


Figure 3.28 From Power ON to Initial Setting

1. After power on, the main power supply (V_{DD}) and the backup power supply (V_{BAT}) are connected in parallel through the diodes inside the IC. The RX4901CE/RX8901CE activates with the previously applied voltage.
2. The host writes data to Register PWSW_CFG to configure whether the auto power switching circuit is used or not, as well as other conditions.

Note: Since the crystal oscillation circuit starts up by just setting a battery for the backup power supply (V_{BAT}) even before turning the main power supply (V_{DD}) on, current for this operation is consumed. For the current consumption value, refer to Current consumption 7 (I_{BAT3}) characteristic (Table 5.4) in the "*5.4 DC Characteristics*" section.

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Switching control 1 (power supply backup configuration using a primary battery)

When the power switching control bits are set as shown below after power on, the RX4901CE/RX8901CE controls the power supply as shown in Figure 3.29. For the power supply connection, refer to Figure 2.3.

PWSW_CFG.INIEN bit = 1	(Enable auto power switching function)
PWSW_CFG.CHGEN bit = 0	(Disable charging V_{BAT})
PWSW_CFG.VBATLDETEN bit = 1	(Enable V_{BAT} voltage detection)
PWSW_CFG.VBATLDETBK bit = 1	(Enable V_{BAT} voltage detection in backup mode)
PWSW_CFG.VDDSAMP[1:0] bits	(Set V_{DD} voltage sampling period)

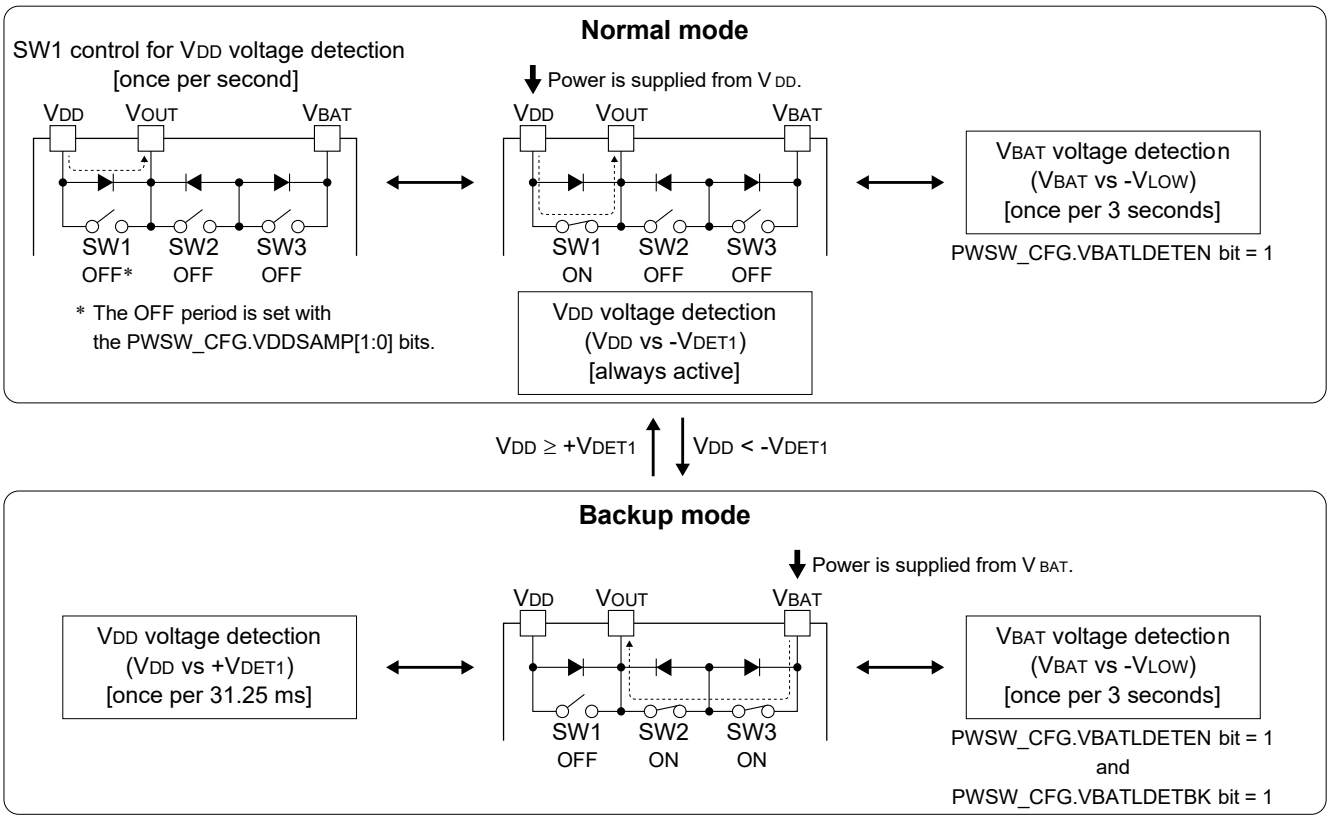


Figure 3.29 Power Switching Control 1 (when using a primary battery as V_{BAT})

1. While the RX4901CE/RX8901CE is operating in Normal mode, the auto power switching circuit always compares the V_{DD} voltage with the V_{DD} drop detection voltage ($-V_{DET1}$). If the V_{DD} voltage drops below $-V_{DET1}$, the auto power switching circuit switches the power source to the backup power supply (V_{BAT}), thus the RX4901CE/RX8901CE enters Backup mode.
2. During Backup mode, the auto power switching circuit compares the V_{DD} voltage with the V_{DD} rise detection voltage ($+V_{DET1}$) once per 31.25 ms. If the V_{DD} voltage rises over $+V_{DET1}$, the auto power switching circuit switches the power source to the main power supply (V_{DD}) to return the RX4901CE/RX8901CE to Normal mode.
3. When the PWSW_CFG.VBATLDETEN bit = 1 (setting of the PWSW_CFG.VBATLDETBK bit = 1 is also necessary for Backup mode), the auto power switching circuit compares the V_{BAT} voltage with the V_{BAT} drop detection voltage ($-V_{LOW}$) once per 3 seconds. If the V_{BAT} voltage drops below $-V_{LOW}$, the auto power switching circuit sets the BUF_INTF.VBATLF bit to 1 to trigger a time stamp or an interrupt. This does not switch the power supply.

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Switching control 2 (power supply backup configuration using a secondary battery)

When the power switching control bits are set as shown below after power on, the RX4901CE/RX8901CE controls the power supply as shown in Figure 3.30. For the power supply connection, refer to Figure 2.2.

PWSW_CFG.INIEN bit = 1	(Enable auto power switching function)
PWSW_CFG.CHGEN bit = 1	(Enable charging V_{BAT})
PWSW_CFG.VBATLDETEN bit = 1	(Enable V_{BAT} voltage detection)
PWSW_CFG.VBATLDETBK bit = 1	(Enable V_{BAT} voltage detection in backup mode)
PWSW_CFG.VDDSAMP[1:0] bits	(Set V_{DD} voltage sampling period)

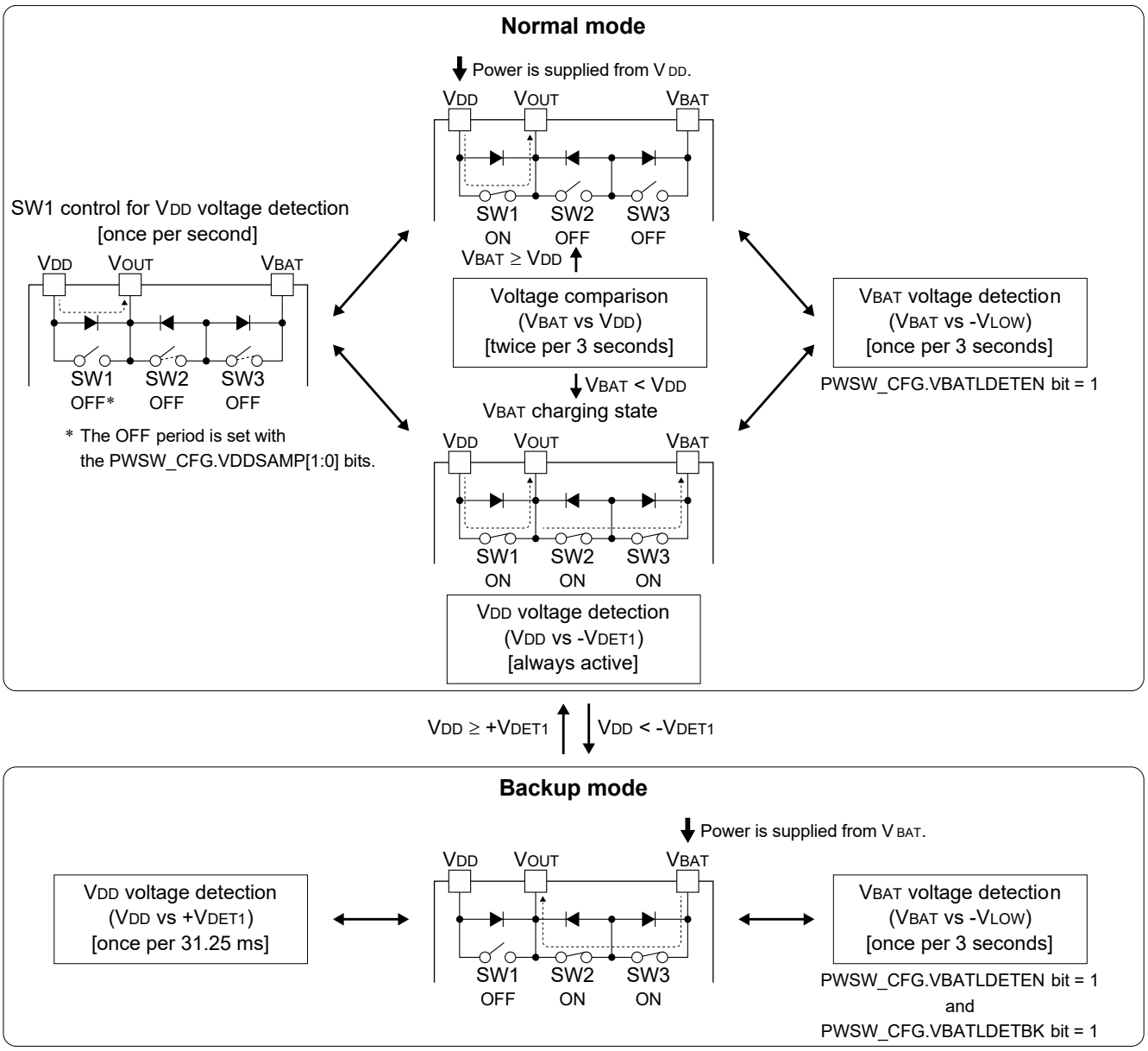


Figure 3.30 Power Switching Control 2 (when using a secondary battery as V_{BAT})

In addition to the switching between Normal mode and Backup mode same as the above (refer to "*Switching control 1*"), a V_{BAT} charge-control is added.

1. During Normal mode, the auto power switching circuit compares the V_{BAT} voltage with the V_{DD} voltage twice per 3 seconds. If the V_{BAT} voltage drops below V_{DD}, the auto power switching circuit turns all the switches on to start charging V_{BAT} from V_{DD}. After that, when the V_{BAT} voltage rises over V_{DD}, SW2 and SW3 are turned off to stop charging. The V_{DD} voltage detection is always performed in both states, and the RX4901CE/RX8901CE enters Backup mode if a voltage drop is detected.
2. During Backup mode, the V_{BAT} charge control is disabled.

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Table 3.12 lists the detection operation status by operating mode.

Table 3.12 Detection Operation by Operating Mode

Operating mode	Normal mode (V_{DD} drive)			Backup mode (V_{BAT} drive)
	PWSW_CFG.CHGEN = 1, PWSW_CFG.INIEN = 1	PWSW_CFG.CHGEN = 0, PWSW_CFG.INIEN = 1	PWSW_CFG.CHGEN = 0, PWSW_CFG.INIEN = 0	
V_{DD} voltage monitor	Always active	Always active	Stop	Once per 31.25 ms
V_{BAT} charge monitor	Twice per 3.0 s	Stop	Stop	Stop
V_{BAT} voltage monitor	Once per 3.0 s	Once per 3.0 s	Once per 3.0 s	Once per 3.0 s

Setting V_{DD} voltage drop detection sampling time

In Normal mode with the auto power switching function enabled, the main power supply voltage (V_{DD}) is always compared to the V_{DD} drop detection voltage ($-V_{DET1}$) and the operating mode transits to Backup mode when a voltage drop is detected. An option is provided to detect a V_{DD} voltage drop with higher accuracy by temporarily setting SW1 to off to disconnect the V_{DD} pin from the V_{BAT} pin during V_{DD} voltage drop detection operation.

The SW1 OFF time should be determined taking the main power supply (V_{DD}) discharge characteristics at power-off and the reduction in charging voltage to V_{BAT} into consideration. The SW1 OFF time should be set longer according to the main power supply discharge characteristics. However, the charging voltage to V_{BAT} during a SW1 OFF period is reduced from V_{DD} by the forward voltage V_F of the diode connected with SW1 in parallel. Therefore, too long an SW1 OFF time reduces effective V_{BAT} charging voltage.

The SW1 OFF time is set using the PWSW_CFG.VDDSAMP[1:0] bits as shown in Table 3.13.

Table 3.13 SW1 OFF Time Settings

PWSW_CFG.VDDSAMP[1:0]	SW1 OFF time
0b00	Not turned off (default)
0b01	2 ms
0b10	128 ms
0b11	256 ms

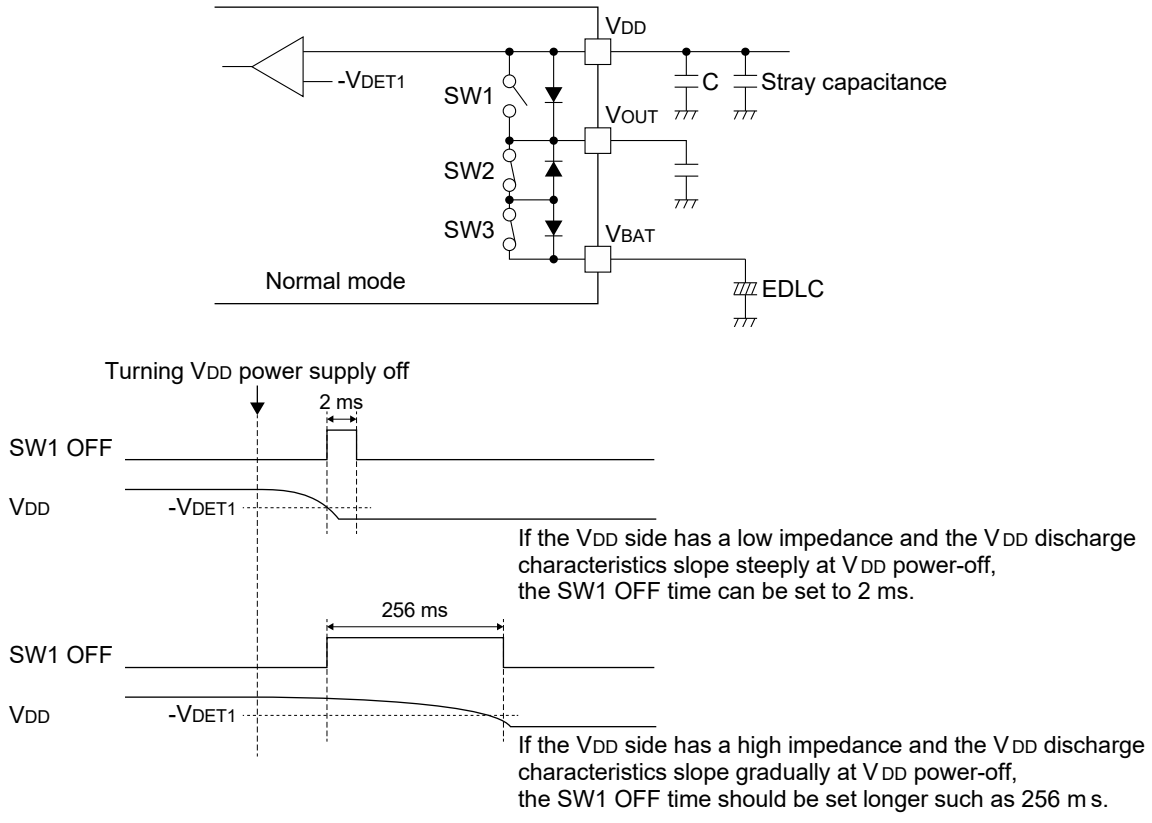


Figure 3.31 SW1 Intermittent Operation for Monitoring V_{DD} Voltage

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Notes on using a small EDLC

Figure 3.32 shows an example of V_{DD} voltage drop detection operation when a small EDLC is used as the backup power supply that should be noted.

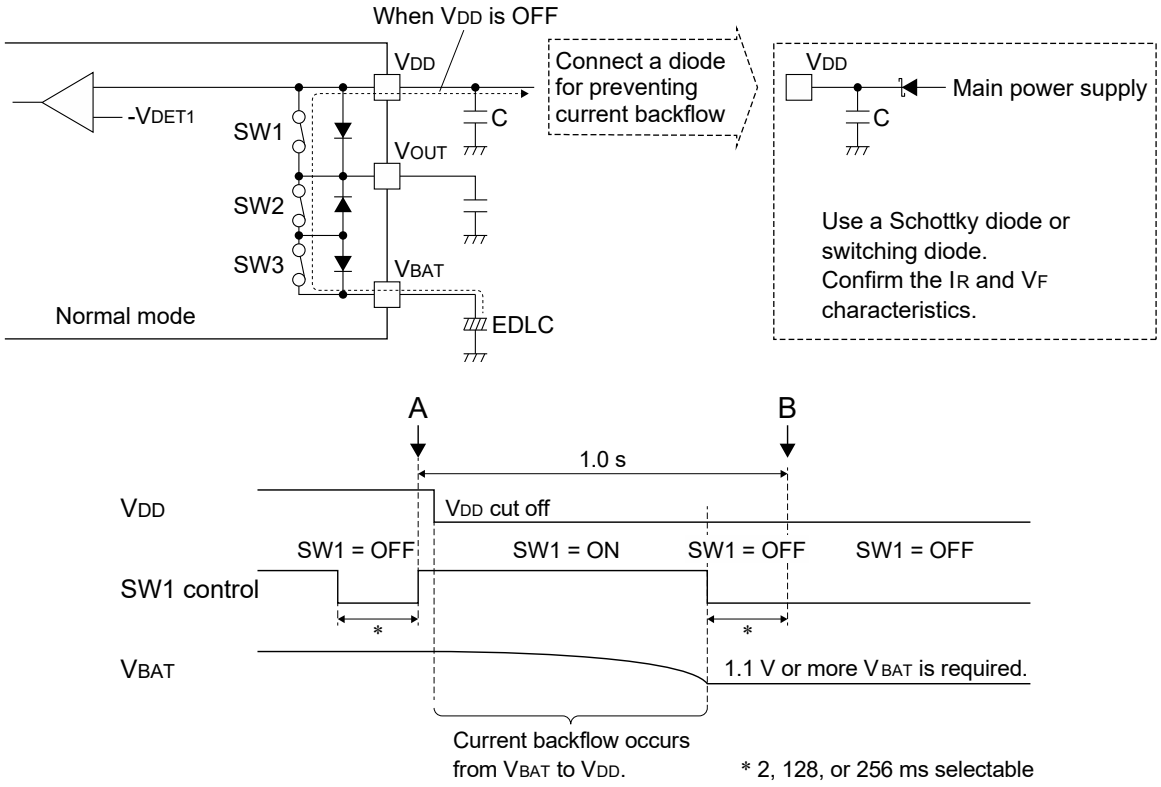


Figure 3.32 Notes on Using Small EDLC

When no V_{DD} voltage drop is detected at Point A during charging in Normal mode, SW1 maintains on state until it is turned off (Point B). If the V_{DD} voltage drops or is turned off immediately after Point A, discharging current flows from the EDLC to the V_{DD} pin until Point B is reached. To prevent this current backflow, take some measures such as inserting a diode to the V_{DD} line.

Backup Battery Implementation Precautions

Please keep the following handling, soldering implements a backup battery or when coin batteries are attached to an implemented battery holder. When VDD of RTC is an OFF and a battery is installed ahead of VDD ON, it have a possibility that POR of RTC doesn't occur by VBAT chattering. Even if VDD was supplied afterwards, RTC is started with no self-initialization. As a results, RTC into unstable condition that current consumption, clock accuracy, I2C/SPI interface. As the measures, following processing STEP1 - STEP4 is guided.

STEP 1: Please fix both +/- terminals where a battery of RTC is connected to in a GND level.
(GND fixation of VDD,VIO is unnecessary.)
STEP 2: Please attach a battery in this state.
STEP 3: Please release a battery terminal and a short of GND more than 100ms from battery wearing after progress.
STEP 4: Please supply VDD in RTC.

Note.
Same as the above, when a battery was installed to a board earlier than VDD-ON by methods such as a re-flow, solder tank or manual labor too, as a results RTC into unstable condition that, current consumption, clock accuracy, I2C/SPI interface.
In this case short-circuit a +terminal of a battery and GND too.
Release it after more than 100ms.
Power-on reset functions and can evade the unstable movement mentioned above
But the processing mentioned above is unnecessary when a VDD power was supplied earlier than a battery installed.

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3.10 Time Stamp Function

3.10.1 Overview

The RX4901CE/RX8901CE has a time stamp function that records the information such as the date/time and event factor when an external event, which is generated due to a change of a EVIN*n* pin input signal, or an internal event, such as a voltage drop or oscillation stop status detected by the self-monitoring function, has occurred. The main features of the time stamp function are outlined below.

- Time stamp trigger sources
  External event inputs:
  - Max. 3 channels (EVIN1, EVIN2, EVIN3)
  - Internal pull-up/pull-down resistors are configurable.
  - Trigger edge is selectable: Rising edge, falling edge, or both edges.
  - Noise filters are included (selectable filtering time: 0 to 5000 ms, 125 ms steps).
  - Event counters are included.
  - Input-pin status can be monitored.

  Internal events:
  - V_{BAT} voltage drop detection
  - $-V_{DET1}$ voltage drop detection
  - V_{DET2} voltage drop detection
  - Oscillation stop detection

  Command trigger:
  - Writing to the specific address can issue a trigger.
- Time stamp buffer
  - A 256-byte SRAMs has been implemented.
  - Three buffer operating modes are supported: FIFO mode that uses the entire SRAM as a FIFO to record data, Direct mode that divides the SRAM into 3 areas for 3 channels of event groups to record data individually, and SRAM mode that allows reading and writing as an SRAM.
  - FIFO mode allows all types of events to record a maximum of 32 complete stamp data.
  - Direct mode allows each channel to record a maximum 10 stamp data (12 data in Channel 2).
  - Two write modes are supported: Overwrite mode that enables overwriting the buffer in full status, and Overwrite Inhibit mode that does not overwrite the buffer.
- Record data: 1/1024 seconds to 1 second, second, minute, hour, day, month, year, EVIN*n* pin status, voltage drop and oscillation statuses, and time stamp trigger factor
- Time stamp data can be captured even in Backup mode.
- Can generate an interrupt when an external or internal event occurs.

Figure 3.33 shows the configuration of the time stamp circuit.

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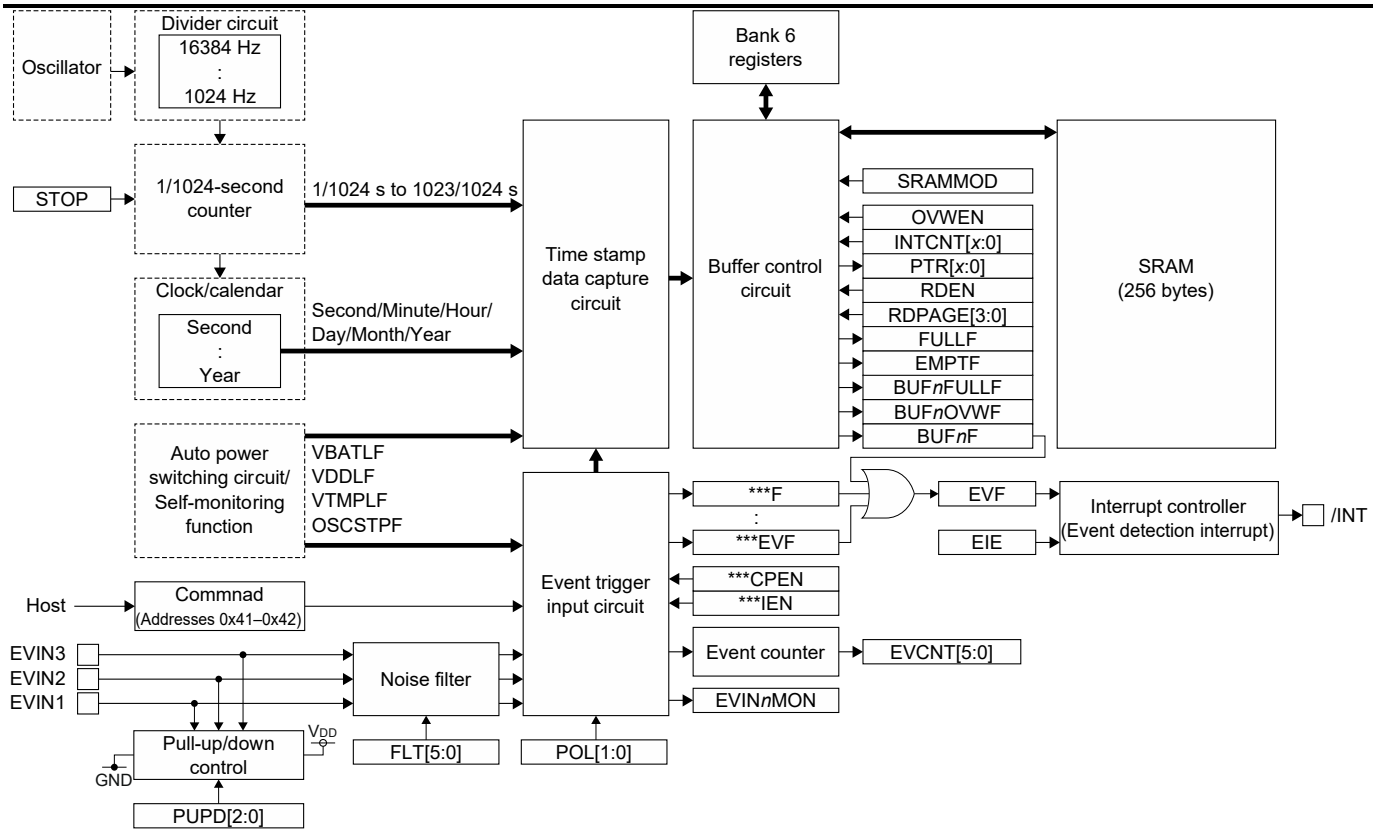


Figure 3.33 Configuration of Time Stamp Circuit

3.10.2 Time Stamp Triggers

When a trigger is generated by an external event, internal event, or writing to the specific address, the RX4901CE/ RX8901CE captures time stamp data at that point and writes it to the buffer. These time stamp triggers are referred to EVIN*n* event input trigger, internal event trigger, and command trigger.

External Event Input (EVIN*n* pin) Trigger

External event input trigger signals are input from the EVIN1 to EVIN3 pins. The following shows the functions, or conditions that should be set, related to the external event trigger input.

Pull-up/pull-down resistors

The EVIN*n* pins have software configurable pull-up and pull-down resistors.

Table 3.14 EVIN*n* Pin Pull-Up/Pull-Down Resistor Selections

EVIN1_CFG.PUPD[2:0] EVIN2_CFG.PUPD[2:0] EVIN3_CFG.PUPD[2:0]	Pull-up/pull-down resistor
0b000	No pull-up/pull-down resistor
0b001	Pull-up resistor 500 kΩ
0b010	Pull-up resistor 1 MΩ(default)
0b011	Pull-up resistor 10 MΩ
0b100	Pull-down resistor 500 kΩ
Other	No pull-up/pull-down resistor

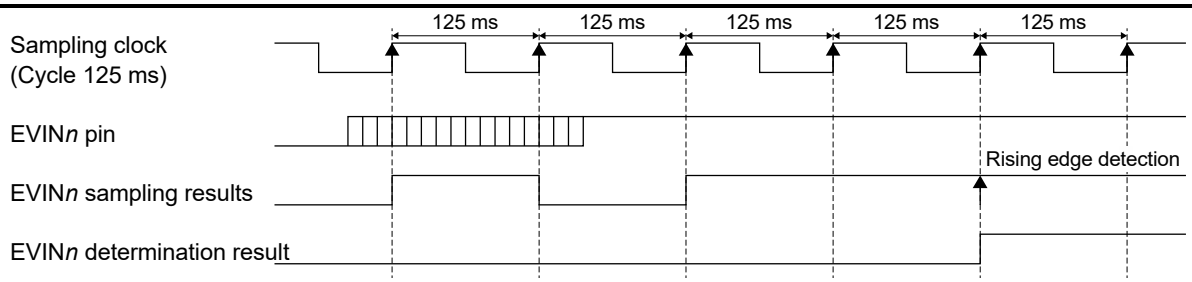
Noise filter

The EVIN*n* pin has a noise filter circuit that eliminates noise on the input signal. The EVIN*n* pin input signal is sampled in 125 ms cycles and when the sampling results are continuously matched the number of times set in the EVIN*n*_FLT.FLT[5:0] bits, it is determined that the sampled logical value has been input.

EVIN1 noise filter: EVIN1_FLT.FLT[5:0] bits
EVIN2 noise filter: EVIN2_FLT.FLT[5:0] bits (Filtering time [ms] = FLT[5:0] × 125)
EVIN3 noise filter: EVIN3_FLT.FLT[5:0] bits

The figure below is an example when the EVIN*n*_FLT.FLT[5:0] bit = 0x03.

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(When rising edge is detected, EVIN*n*_FLT.FLT[5:0] bit = 0x03)

Figure 3.34 EVIN Noise Filter Function

Notes:
- To determine that the EVIN*n* pin input signal is valid, it must have a 1 ms or more pulse width even if the EVIN*n*_FLT.FLT[5:0] bits are set to 0x00.
- The input signal is fetched after 5 ms from the input detection, therefore, a 5 ms delay occurs until the time stamp data is captured.

Table 3.15 Valid EVIN*n* Input Pulse Width

EVIN*n*_FLT. FLT[5:0]	Uncertain EVIN*n* pulse width (Whether the edge input is detected or not depends on the relationship between the edge input timing and the sampling timing in 125 ms cycles.)	Valid EVIN*n* pulse width (The edge input is always detected.)
0x00	–	1 ms or more
0x01 (Setting prohibited)	–	–
0x02	125 ms or more and less than 250 ms	250 ms or more
0x03	250 ms or more and less than 375 ms	375 ms or more
:	:	:
0x27	4750 ms or more and less than 4875 ms	4875 ms or more
0x28	4875 ms or more and less than 5000 ms	5000 ms or more
0x29 or more (Setting prohibited)	–	–

Input detection

The EVIN*n* pin input signal edge to be detected is configurable.

Table 3.16 EVIN*n* Input Detection Edge

EVIN1_CFG.POL[1:0] EVIN2_CFG.POL[1:0] EVIN3_CFG.POL[1:0]	Detection edge
0b00	Falling edge (default)
0b01	Rising edge
0b10	Falling and rising edges
0b11	

Event counter

Each EVIN*n* input has a 6-bit counter to count the number of event trigger inputs within the range from 0 to 63. The counter value can be read from the bits shown below.

EVIN1 event counter: EVIN1_EVCNT.EVCNT[5:0] bits
EVIN2 event counter: EVIN2_EVCNT.EVCNT[5:0] bits
EVIN3 event counter: EVIN3_EVCNT.EVCNT[5:0] bits

Monitor

The RX4901CE/RX8901CE provides the bits for monitoring the current EVIN*n* pin status (input logic level).

EVIN1 monitor: EVINMON.EVIN1MON bit
EVIN2 monitor: EVINMON.EVIN2MON bit (1: High level input, 0: Low level input)
EVIN3 monitor: EVINMON.EVIN3MON bit

Internal Event Trigger

When a power supply voltage drop status or an oscillation stop status is detected, the detector circuit can issue an internal event trigger.

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V_{BAT} voltage drop detection
$-V_{DET1}$ voltage drop detection
V_{DET2} voltage drop detection
Oscillation stop detection (Time stamp data is captured when the oscillator resumes oscillation.)

Note: The PWSW_CFG.INIEN bit must be set to 1 to detect voltage drop statuses. For more information, refer to "*3.9 Auto Power Switching Function*."

Command Trigger

A command trigger can be issued by writing an arbitrary value to Register WRCMD_TRG after setting the WRCMD_CFG.CMDTRGEN bit to 1.

3.10.3 Time Stamp Buffer

The RX4901CE/RX8901CE includes a 256-byte SRAM that are used as a time stamp buffer for storing captured time stamp data.

Time Stamp Data

The buffer data is shown below. It can be read by accessing continuously from Addresses 0x60 to 0x69.

Address	Captured data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	1/1024-second divider counter data	SUBSEC1	SUBSEC0	–	–	–	–	–	–
		2	1						
0x61		SUBSEC9	SUBSEC8	SUBSEC7	SUBSEC6	SUBSEC5	SUBSEC4	SUBSEC3	SUBSEC2
		512	256	128	64	32	16	8	4
0x62	Second data (0–59)	–	SEC_H[2:0]			SEC_L[3:0]			
			10-second digit (BCD)			1-second digit (BCD)			
0x63	Minute data (0–59)	–	MIN_H[2:0]			MIN_L[3:0]			
			10-minute digit (BCD)			1-minute digit (BCD)			
0x64	Hour data (0–23)	–	–	HOUR_H[1:0]		HOUR_L[3:0]			
				10-hour digit (BCD)		1-hour digit (BCD)			
0x65	Day data (1–31)	–	–	DAY_H[1:0]		DAY_L[3:0]			
				10-day digit (BCD)		1-day digit (BCD)			
0x66	Month data (1–12)	–	–	–	MONTH_H	MONTH1[3:0]			
					10-Month digit (BCD)	1-Month digit (BCD)			
0x67	Year data (0–99)	YEAR_H[3:0]				YEAR_L[3:0]			
		10-year digit (BCD)				1-year digit (BCD)			
0x68	Internal status	EVIN3POL	EVIN2POL	EVIN1POL	–	VBATLSTAT	VTMPLSTAT	VDDLSTAT	OSCSTP STAT
		EVIN3 input status	EVIN2 input status	EVIN1 input status		V_{BAT} drop detection status	V_{DET2} drop detection status	$-V_{DET1}$ drop detection status	Oscillation stop detection status
0x69	Data capturing trigger factor	EVIN3TRG *	EVIN2TRG *	EVIN1TRG *	WRCMDTRG	VBATLTRG	VTMPLTRG	VDDLTRG	OSCSTPTRG
		EVIN3 input trigger	EVIN2 input trigger	EVIN1 input trigger	Command trigger	V_{BAT} drop detection trigger	V_{DET2} drop detection trigger	$-V_{DET1}$ drop detection trigger	Oscillation stop detection trigger

* This information is set to 0 in Direct mode.

Figure 3.35 Time Stamp Data and Read Addresses

To read the desired data from these registers, a pointer/page in the buffer must be specified before reading.

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Time Stamp Buffer Operating Mode

The time stamp buffer has three operating modes for different usages, FIFO mode, Direct mode, and SRAM mode.

FIFO mode (EVIN_EN.DIRMOD bit = 0, BUF1_CFG2.SRAMMOD bit = 0)

The entire buffer is used as a FIFO that controls data read/write using pointers. In this mode, the buffered data can be read even in trigger waiting state. The entire area is shared with all the trigger factors. The recorded time stamp data includes the trigger factor, thus it is possible to determine what trigger has captured the time stamp.
A maximum of 32 time stamp data can be captured before being read.

The figure below shows an example when data has been captured six times.

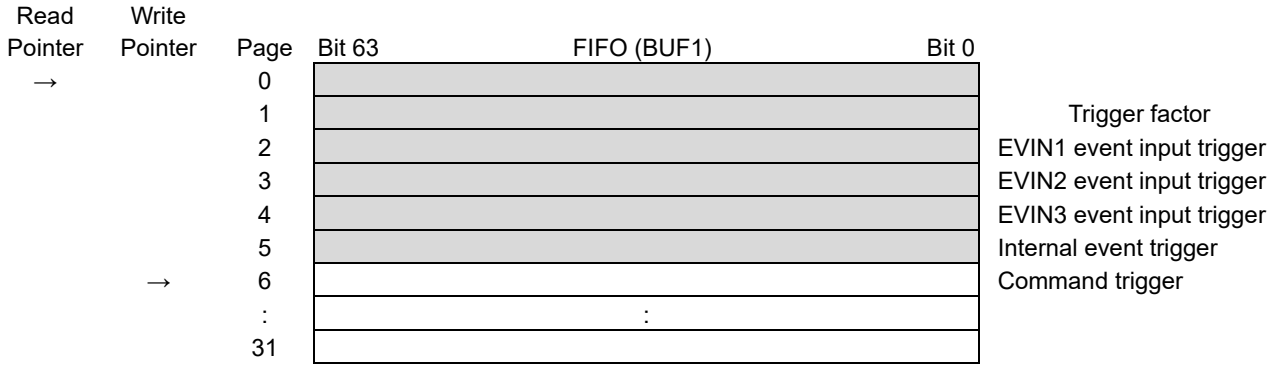


Figure 3.36 Time Stamp Buffer in FIFO Mode (example when six data have been stored)

Direct Mode (EVIN_EN.DIRMOD bit = 1, BUF1_CFG2.SRAMMOD bit = 0)

This mode captures the time stamps triggered by the EVIN1 to EVIN3 events into the corresponding buffer area within the three buffer areas (BUF1, BUF2, BUF3) individually provided for each event input. Time stamps captured by other triggers are stored to a buffer area as shown in Table 3.17.

However, each buffer area does not form a FIFO nor use a pointer to manage reading/writing data. Therefore, it is necessary to stop capturing stamp data to the BUF when reading the buffered data in Direct mode with Overwrite mode specified.

Table 3.17 BUF1 to BUF3 in Direct Mode

Item	BUF1	BUF2	BUF3
Stamp data capturing count	10 data	12 data	10 data
Trigger factor	EVIN1 event input trigger Command trigger	EVIN2 event input trigger	EVIN3 event input trigger Internal event trigger

The figure below shows an example when data has been captured to each buffer twice.

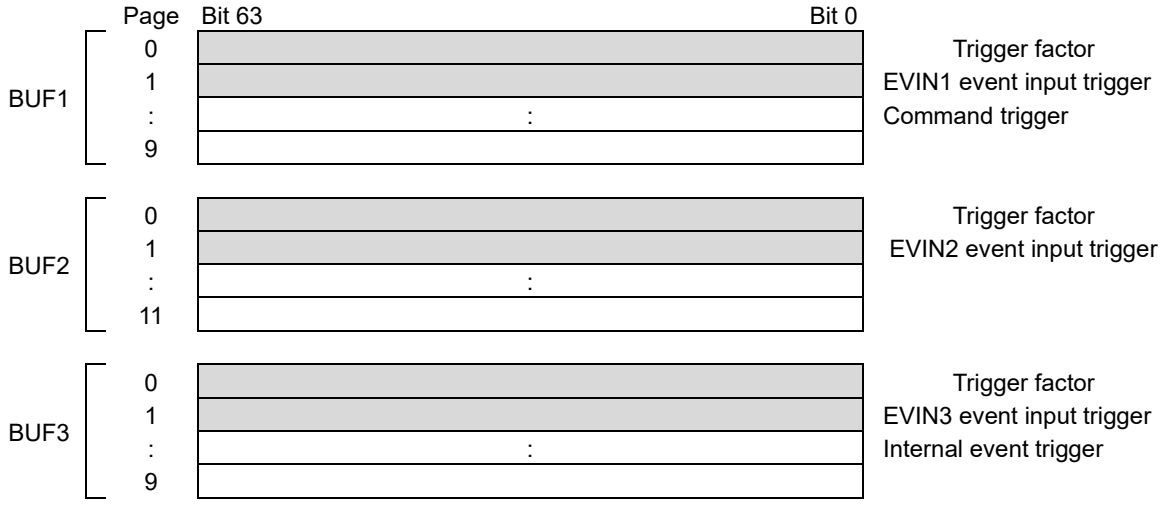


Figure 3.37 Time Stamp Buffer in Direct Mode (example when two data have been stored in each buffer)

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In this mode, the time stamp buffer can be read/written as an SRAM through Bank 6. The SRAM is constituted of 16 bytes × 16 pages. By specifying the page number to be accessed, data can freely be read/written from/to 16 addresses in that page through Bank 6 (Addresses 0x60 to 0x6F).

SRAM access method

1. Set the BUF1_CFG2.SRAMMOD bit to 1. (Set SRAM mode)
2. Set the BUF1_CFG2.RDPAGE[3:0 bits. (Specify SRAM page (0x0–0xF))
   Bank 6 is used as a window to access the specified page.
3. Read/write data from/to the necessary addresses within Addresses 0x60 to 0x6F (corresponding to SRAM address 0x0 to 0xF).

Time Stamp Buffer Write Mode

The RX4901CE/RX8901CE provides two write modes that have a different behavior after the buffer enters full state due to capturing data.

Overwrite mode

Data before being read are overwritten from oldest.
The buffers enter Overwrite mode by setting the following bits to 1.

FIFO mode/BUF1 write mode setting: BUF1_CFG1.OVWEN bit
BUF2 write mode setting: BUF2_CFG1.OVWEN bit
BUF3 write mode setting: BUF3_CFG1.OVWEN bit

When an overwrite occurs, the BUF_OVWF.BUF*n*OVWF bit is set to 1.

Overwrite Inhibit mode

When a time stamp trigger is issued after the buffer becomes full, although the overwrite flag is set, the captured data is discarded. Data before being read are preserved.
The buffer enters Overwrite Inhibit mode by setting the write mode setting bit shown above to 0.

3.10.4 Operations

Initial Settings

1. Disabling event detection interrupt outputs from the /INT pin
   Disable interrupts so that unnecessary event detection interrupts will not occur during initial setting.
   1-1. Set the TSTP_INTE.EIE bit to 0. (Disable time stamp event detection interrupt)
2. Selecting FIFO mode or Direct mode
   2-1. Set the EVIN_EN.DIRMOD bit. (Select FIFO/Direct mode)
3. Setting EVIN input conditions
   3-1. When using the EVIN1 input, configure the following bits in Registers EVIN1_CFG and EVIN1_FLT:
   - EVIN1_CFG.PUPD[2:0] bits (Select pull-up/pull-down resistor)
   - EVIN1_CFG.POL[1:0] bits (Select detection edge)
   - EVIN1_FLT.FLT[5:0] bits (Set input filtering time)

   3-2. When using the EVIN2 input, configure the following bits in Registers EVIN2_CFG and EVIN2_FLT:
   - EVIN2_CFG.PUPD[2:0] bits (Select pull-up/pull-down resistor)
   - EVIN2_CFG.POL[1:0] bits (Select detection edge)
   - EVIN2_FLT.FLT[5:0] bits (Set input filtering time)

   3-3. When using the EVIN3 input, configure the following bits in Registers EVIN3_CFG and EVIN3_FLT:
   - EVIN3_CFG.PUPD[2:0] bits (Select pull-up/pull-down resistor)
   - EVIN3_CFG.POL[1:0] bits (Select detection edge)
   - EVIN3_FLT.FLT[5:0] bits (Set input filtering time)

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4. Setting interrupts

4-1. When enabling external event input interrupts, set the following bits in Register EVNT_INTE to 1 (or set to 0 to disable):
- EVNT_INTE.EVIN1IEN bit *1 (Enable/disable EVIN1 event input interrupt)
- EVNT_INTE.EVIN2IEN bit *1 (Enable/disable EVIN2 event input interrupt)
- EVNT_INTE.EVIN3IEN bit *1 (Enable/disable EVIN3 event input interrupt)

4-2. When enabling internal event interrupts, set the following bits in Register EVNT_INTE to 1 (or set to 0 to disable):
- EVNT_INTE.VBATLIEN bit *1 (Enable/disable V_{BAT} voltage drop detection event interrupt)
- EVNT_INTE.VTMPLIEN bit *1 (Enable/disable V_{DET2} voltage drop detection event interrupt)
- EVNT_INTE.VDDLIEN bit *1 (Enable/disable $-V_{DET1}$ voltage drop detection event interrupt)
- EVNT_INTE.OSCSTPIEN bit *1 (Enable/disable oscillation stop detection event interrupt)

*1 These bits enable/disable interrupts by occurrence of the events regardless of whether time stamp data is captured or not.

5. Setting buffers

5a. FIFO mode (BUF1)

5a-1. Configure the following bits in Register BUF1_CFG1:
- BUF1_CFG1.OVWEN bit (Select Overwrite/Overwrite Inhibit mode)
- BUF1_CFG1.INTCNT[5:0] bits *2 (Specify buffer data count to generate interrupt)

*2 When these bits are set to 0x0, no BUF1 interrupt will occur even when the BUF_INTF.BUF1F bit is set.

5b. Direct mode (BUF1 to BUF3)

5b-1. When using BUF1, configure the following bits in Register BUF1_CFG1.
- BUF1_CFG1.OVWEN bit (Select Overwrite/Overwrite Inhibit mode)
- BUF1_CFG1.INTCNT[5:0] bits *3 (Specify buffer data count to generate interrupt)

5b-2. When using BUF2, configure the following bits in Register BUF2_CFG1.
- BUF2_CFG1.OVWEN bit (Select Overwrite/Overwrite Inhibit mode)
- BUF2_CFG1.INTCNT[3:0] bits *3 (Specify buffer data count to generate interrupt)

5b-3. When using BUF3, configure the following bits in Register BUF3_CFG1.
- BUF3_CFG1.OVWEN bit (Select Overwrite/Overwrite Inhibit mode)
- BUF3_CFG1.INTCNT[3:0] bits *3 (Specify buffer data count to generate interrupt)

*3 When these bits are set to 0x0, no BUF*n* interrupt will occur even when the BUF_INTF.BUF*n*F bit is set.

6. Clearing event counters and buffer flags by issuing a command trigger

6-1. Write 0xF0 to Register WRCMD_CFG. (Clear command)

6.2. Write any value to Register WRCMD_TRG. (Issue command trigger)

7. Enabling event detection interrupt outputs from the /INT pin

7-1. Set the TSTP_INTE.EIE bit to 1. (Enable time stamp event detection interrupt)

8. Setting external events to capture time stamps

8-1. When capturing time stamps using the EVIN inputs, set the following bits in Register EVIN_EN to 1:
- EVIN_EN.EVIN1CPEN bit (Enable/disable time stamp capture by EVIN1 input)
- EVIN_EN.EVIN2CPEN bit (Enable/disable time stamp capture by EVIN2 input)
- EVIN_EN.EVIN3CPEN bit (Enable/disable time stamp capture by EVIN3 input)

9. Setting internal events to capture time stamps

9-1. When capturing time stamps when an internal event occurs, set the following bits in Register CAP_EN to 1:
- CAP_EN.VBATLCPEN bit (Enable/disable time stamp capture by V_{BAT} voltage drop detection event trigger)
- CAP_EN.VTMPLCPEN bit (Enable/disable time stamp capture by V_{DET2} voltage drop detection event trigger)

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- CAP_EN.VDDLCPEN bit (Enable/disable time stamp capture by $-V_{DET1}$ voltage drop detection event trigger)
- CAP_EN.OSCSTPCPEN bit (Enable/disable time stamp capture by oscillation stop detection event trigger)

10. Enabling external event inputs

10-1. When enabling external event inputs from the EVIN pin, set the following bits in Register EVIN_EN to 1:
- EVIN_EN.EVIN1EN bit *4 (Enable/disable external event input from EVIN1)
- EVIN_EN.EVIN2EN bit *4 (Enable/disable external event input from EVIN2)
- EVIN_EN.EVIN3EN bit *4 (Enable/disable external event input from EVIN3)

*4 When setting the EVIN_EN.EVIN*n*EN bit to 0 (EVIN*n* input disabled), the EVIN_EN.EVIN*n*CPEN bit should also be set to 0.

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Time Stamp Capturing Operation

FIFO mode

When an event trigger that is enabled to capture time stamp data or a command trigger is generated, the RX4901CE/ RX8901CE captures time stamp data from the counters and flags, and writes it to the buffer page pointed to by <BUF1_STAT. PTR[5:0] bits + 1>. The BUF1_STAT.PTR[5:0] bits are incremented by this writing. In other words, the BUF1_STAT.PTR[5:0] bits retain the number of buffered data before being read. When this data count reaches the value set in the BUF1_CFG1.INTCNT[5:0] bits, a BUF1 event input interrupt factor occurs and the RX4901CE/ RX8901CE asserts the /INT signal to send an interrupt request to the host if the interrupt is enabled. During data reading, time stamp data is read from the buffer page pointed to by <BUF1_STAT.PTR[5:0] bits = 1>. The BUF1_STAT. PTR[5:0] bits are decremented by this reading and the page number pointed to by the BUF1_STAT. PTR[5:0] bits are updated as well.
Figure 3.38 and Figure 3.39 show the statuses of the FIFO buffer, pointers, and buffer status bits according to capturing data.

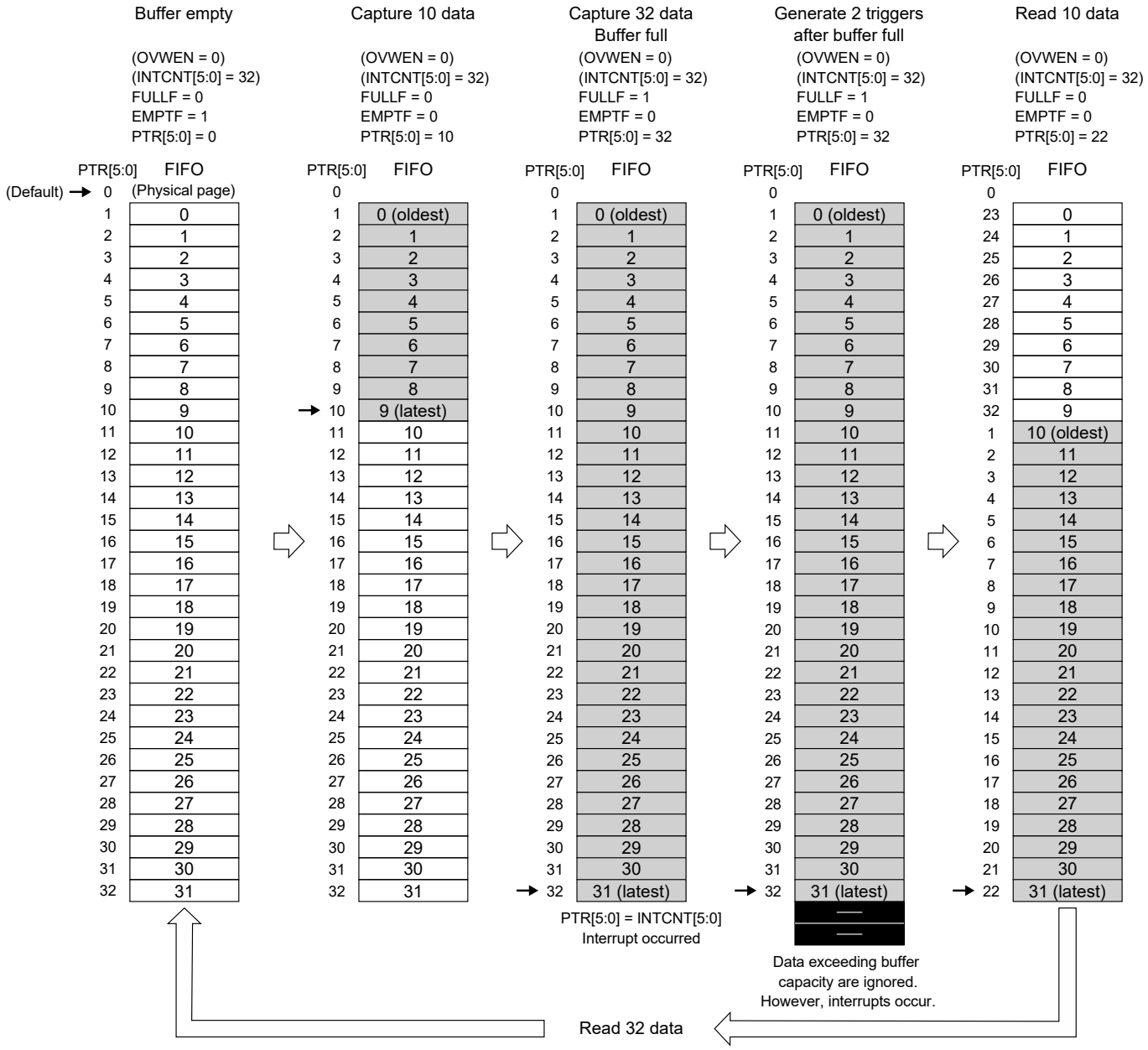


Figure 3.38 Time Stamp Capture Operations (FIFO mode + Overwrite Inhibit mode)

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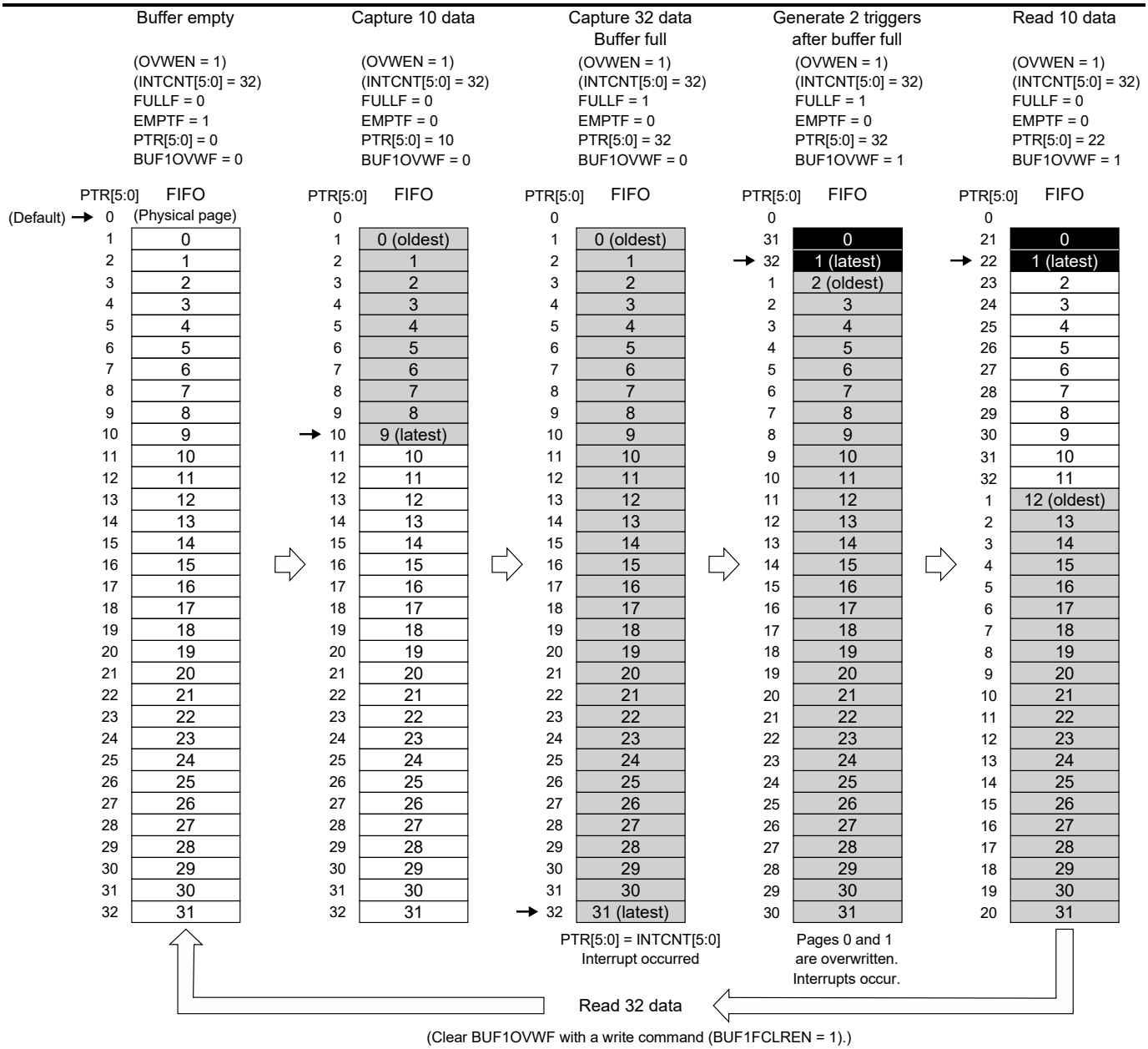


Figure 3.39 Time Stamp Capture Operations (FIFO mode + Overwrite mode)

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Direct mode

When an event trigger that is enabled to capture time stamp data or a command trigger is generated, the RX4901CE/RX8901CE captures time stamp data from the counters and flags, and writes it to BUF*n* according to the event type. The buffers in Direct mode have no pointers as a FIFO. The BUF*n*_STAT.PTR[*x*:0] bits count triggers that have occurred, and the trigger count points to the buffer page where the data is written. The trigger count is incremented every time data is written. When this trigger count reaches the value set in the BUF*n*_CFG1. INTCNT[*x*:0] bits, a BUF*n* event input interrupt factor occurs and the RX4901CE/RX8901CE asserts the /INT signal to send an interrupt request to the host if the interrupt is enabled.
Figure 3.40 and Figure 3.41 show the statuses of the buffer (e.g. BUF1) and buffer status bits according to capturing data .

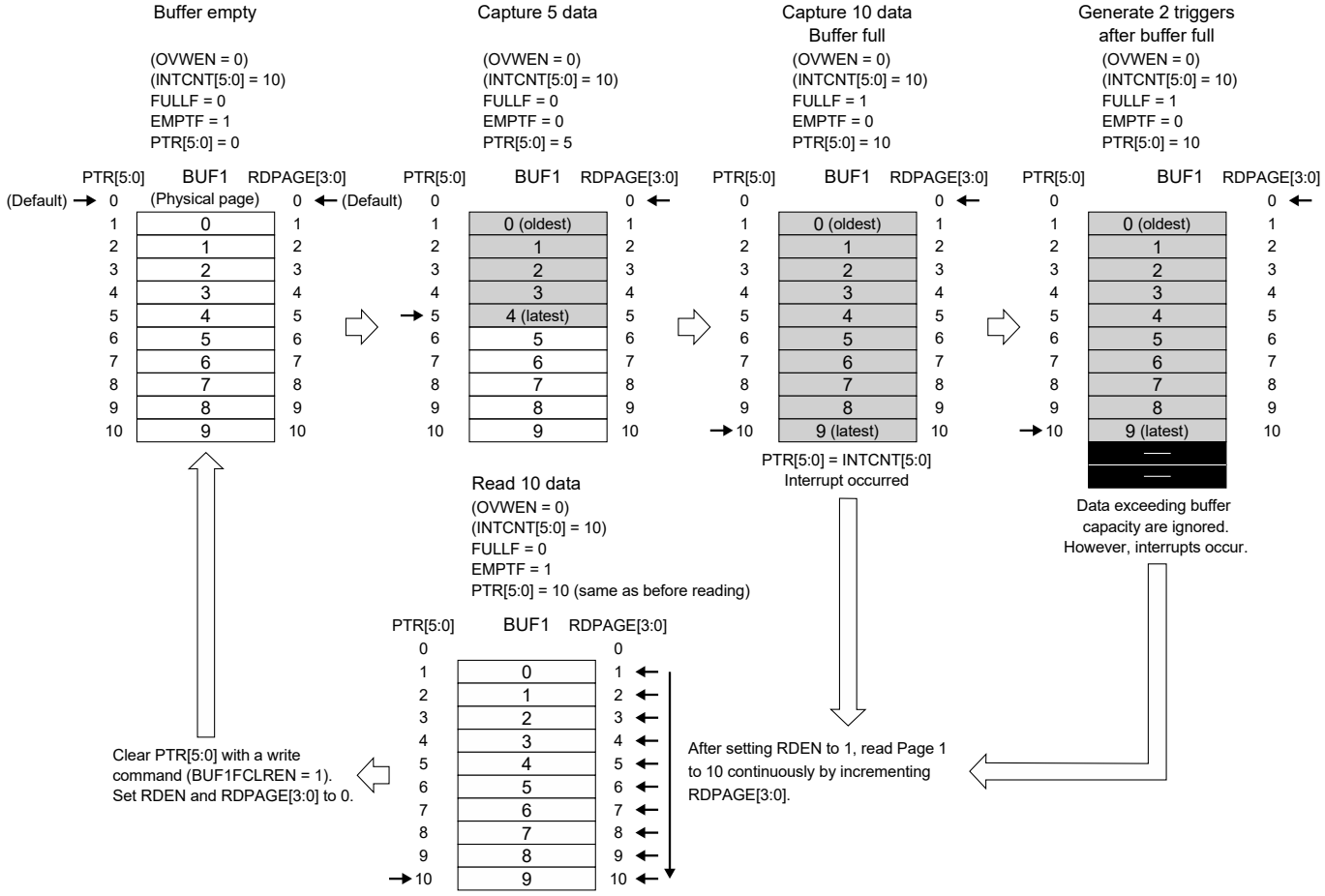


Figure 3.40 Time Stamp Capture Operations (Direct mode + Overwrite Inhibit mode)

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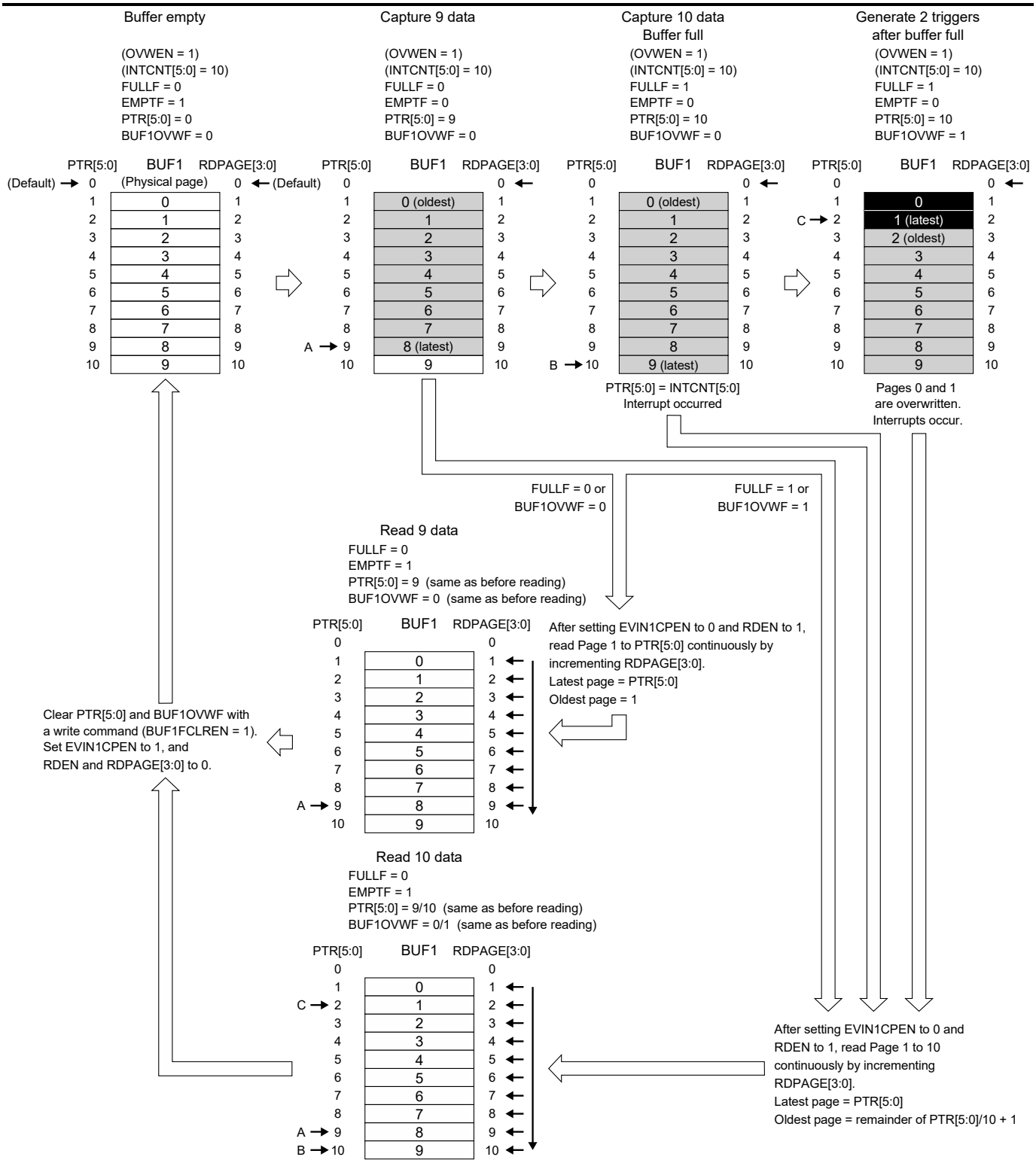


Figure 3.41 Time Stamp Capture Operations (Direct mode + Overwrite mode)

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Buffer full/empty

If the buffer becomes full without reading data, the buffer full flags (BUF*n*_STAT.FULLF bit and BUF_FULLF. BUF*n*FULLF bit *1) are set to 1.

In Overwrite Inhibit mode, time stamp data that will be captured by events subsequently occurring will be discarded until a free space is made in the buffer (until the BUF*n*_STAT.FULLF bit is set to 0). In Direct mode, the BUF*n*_STAT.PTR[*x*:0] bits retain the value when the buffer became full.

In Overwrite mode, the buffered data will be overwritten with data subsequently captured in order from the oldest. In Direct mode, the BUF*n*_STAT.PTR[*x*:0] bits return to 0 and continue counting triggers. When an overflow occurs, the overwrite flag (BUF_OVWF.BUF*n*OVWF bit *2) is set to 1.

When the buffer becomes empty by reading all the buffered data, the buffer empty flag (BUF*n*_STAT.EMPTF bit *3) is set to 1.

*1 Buffer full flag: The BUF*n*_STAT.FULLF bit is automatically cleared when a free space is made in the buffer by reading buffered data. It is also cleared by issuing a command trigger with the WRCMD_CFG.BUF*n*FCLREN bit set to 1.

The BUF_FULLF.BUF*n*FULLF bit is the flag representing the buffer full history and is not cleared even if the buffer full state has disappeared unless 0 is written to.

*2 The BUF_OVWF.BUF*n*OVWF bit is cleared by issuing a command trigger with the WRCMD_CFG. BUF*n*FCLREN bit set to 1.

*3 Buffer empty flag: The BUF*n*_STAT.EMPTF bit is automatically cleared when data is written to the buffer. It is also cleared by issuing a command trigger with the WRCMD_CFG.BUF*n*FCLREN bit set to 1.

Issuing Command Trigger

The RX4901CE/RX8901CE allows the host to issue a time stamp trigger by writing data to specific registers. The following shows its procedure:

1. Set the WRCMD_CFG.CMDTRGEN bit to 1. (Specify command trigger)
2. Write any data to the WRCMD_TRG.WRTRG[7:0] bits. (Issue command trigger)
3. Confirm if the BUF_INTF.BUF1F bit has been set to 1.
   Or confirm if the BUF1_CFG2.RDPAGE[3:0] bits have been incremented.
4. Confirm if the WRCMD_TRG.WRTRG[7:0] bits revert to 0x00.

Step 3 is a method to confirm that the time stamp trigger is accepted normally.
Step 4 is necessary when reading time stamp data or issuing the next command trigger immediately after a command trigger has been issued.

Notes: • The time stamp by issuing a command trigger is stored to BUF1.

• When issuing time stamp triggers in succession, a 5 ms interval is required between the triggers.

Figure 3.42 shows the time stamp trigger timing when a command trigger is issued.
In the RX4901CE, a command trigger is issued at the rising edge of the clock for the LSB of the Register WRCMD_TRG data.
In the RX8901CE, a command trigger is issued at the rising edge of the clock while the RX8901CE is responding with ACK to the Register WRCMD_TRG data sent.

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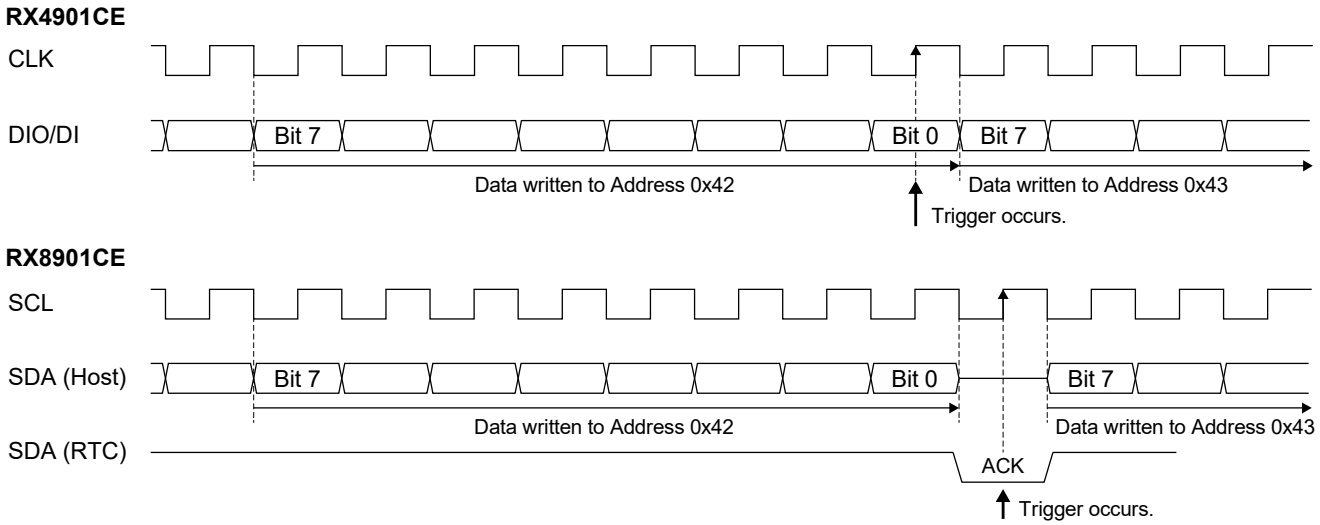


Figure 3.42 Command trigger Timing

The command trigger has the following functions in addition to the time stamp trigger:

WRCMD_CFG.EVCNTCLREN bit: Issuing a command trigger with this bit set to 1 clears the event counters (Registers EVIN*n*_EVCNT).

WRCMD_CFG.BUF1FCLREN bit: Issuing a command trigger with this bit set to 1 clears the following bits.
BUF1_STAT.FULLF bit (BUF1 full flag)
BUF1_STAT.EMPTF bit (BUF1 empty flag)
BUF1_STAT.PTR[5:0] bits (BUF1 event pointer)
BUF_OVWF.BUF1OVWF bit (BUF1 overwrite flag)

WRCMD_CFG.BUF2FCLREN bit: Issuing a command trigger with this bit set to 1 clears the following bits.
BUF2_STAT.FULLF bit (BUF2 full flag)
BUF2_STAT.EMPTF bit (BUF2 empty flag)
BUF2_STAT.PTR[3:0] bits (BUF2 event pointer)
BUF_OVWF.BUF2OVWF bit (BUF2 overwrite flag)

WRCMD_CFG.BUF3FCLREN bit: Issuing a command trigger with this bit set to 1 clears the following bits.
BUF3_STAT.FULLF bit (BUF3 full flag)
BUF3_STAT.EMPTF bit (BUF3 empty flag)
BUF3_STAT.PTR[3:0] bits (BUF3 event pointer)
BUF_OVWF.BUF3OVWF bit (BUF3 overwrite flag)

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Reading Time Stamp Data

FIFO mode

The following shows an example of time stamp data read procedure in FIFO mode:

1. After an interrupt has occurred (/INT = L), read Register INTF.
   When the INTF.EVF bit = 1, a time stamp event detection interrupt has occurred. In this case, perform the procedure from Step 2.

   If another interrupt has occurred, execute the corresponding interrupt handler.

2. Read Registers EVNT_INTF and BUF_INTF to determine the interrupt factor that has occurred.

   <When a flag in Register EVNT_INTF has been set>
   It indicates that an EVIN1 or internal event has occurred. Table 3.18 shows the set condition of each flag. Execute an interrupt handler according to the event that has occurred. The flag that has been set to 1 should be cleared by writing 0 in the interrupt handler.

   <When the BUF_INTF.BUF1F bit has been set>
   This interrupt occurs when the buffered data count retained in the BUF1_STAT.PTR[5:0] bits reaches the value set to the BUF1_CFG1.INTCNT[5:0] bits by occurrences of the events that have been enabled to capture time stamp data.
   Read the captured time stamp data by the following operations.

3. To temporarily disable interrupts, set the TSTP_INTE.EIE bit to 0. (Disable time stamp event detection interrupt))

4. Write 0 to the BUF_INTF.BUF1F bit. (Clear interrupt flag)

5. Read the BUF1_STAT.PTR[5:0] bits to obtain the number of time stamp data that can be read from the buffer.

6. Obtain one time stamp data by burst reading 10 bytes from Addresses 0x60 to 0x69 [Note].
   After that, take a 1 ms of wait time and then repeat this operation for the data count that has been obtained in Step 5.

   It is not necessary to specify the page to be read using the BUF1_CFG2.RDPAGE[3:0] bits for this reading. The oldest data is obtained in the first reading and later data are read sequentially. The BUF1_STAT.PTR[5:0] bits are decremented by reading data for one time and they reach 0 after data are read for the necessary times. See Figure 3.35 for the contents of these addresses.

Notes:
- Be sure to read Addresses 0x60 to 0x69 continuously to obtain time stamp data. Reading only a part of the data is prohibited.
- Do not read the buffer for more than the data count that has been obtained in Step 5.

7. Check if the BUF1_STAT.PTR[5:0] bits are set to 0 or the BUF1_STAT.EMPTF bit is set to 1.

   If the BUF1_STAT.PTR[5:0] bits are not set to 0 or the BUF1_STAT.EMPTF bit is set to 0, a new trigger has occurred during reading in Step 6 and a new time stamp data has been added. In this case, repeat Steps 5 to 7.

8. Set the TSTP_INTE.EIE bit to 1 (if it was set to 0 in Step 3). (Enable time stamp event detection interrupt)

The above procedure does not take buffer full and overwrite conditions into consideration. Read these flags and handle as necessary.

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Direct mode

In Direct mode, the recommended time stamp data read procedure is different between Overwrite Inhibit mode and Overwrite mode. The following shows a recommended read procedure in each mode:

<Overwrite Inhibit mode>

1. After an interrupt has occurred (/INT = L), read Register INTF.
   When the INTF.EVF bit = 1, a time stamp event detection interrupt has occurred. In this case, perform the procedure from Step 2.

   If another interrupt has occurred, execute the corresponding interrupt handler.

2. Read Registers EVNT_INTF and BUF_INTF to determine the interrupt factor that has occurred.

   <When a flag in Register EVNT_INTF has been set>
   It indicates that an EVIN*n* or internal event has occurred. Table 3.18 shows the set condition of each flag. Execute an interrupt handler according to the event occurred. The flag that has been set to 1 should be cleared by writing 0 in the interrupt handler.

   <When the BUF_INTF.BUF*n*F bit has been set>
   This interrupt occurs when the buffered data count retained in the BUF*n*_STAT.PTR[*x*:0] bits reaches the value set to the BUF*n*_CFG1.INTCNT[*x*:0] bits by occurrences of the events that have been enabled to capture time stamp data.
   Read the captured time stamp data by the following operations.

The explanation below assumes that a BUF1 interrupt has occurred.

3. Read the BUF1_STAT.PTR[5:0] bits to obtain the page number of the latest recorded time stamp data.
4. Set the BUF1_CFG2.RDEN bit to 1. (Enable reading of BUF1)
5. Set the BUF1_CFG2.RDPAGE[3:0] bits to 0x1 (oldest data page). (Specify read page)
6. Obtain one time stamp data by burst reading 10 bytes from Addresses 0x60 to 0x69.

   See Figure 3.35 for the contents of these addresses.

   * Be sure to read Addresses 0x60 to 0x69 continuously to obtain time stamp data. Reading a part of data is prohibited.

7. If the BUF1_CFG2.RDPAGE[3:0] bits have not reached the page number obtained in Step 3, increment the BUF1_CFG2.RDPAGE[3:0] bits (to specify from the oldest to the later pages) and repeat Steps 6 and 7.
8. Set the BUF1_CFG2.RDEN bit to 0. (Disable reading of BUF1)
9. Set the WRCMD_CFG.BUF1FCLREN bit to 1 and write any value to Register WRCMD_TRG.
   (Clear BUF1 flags and page pointer)

Note on Overwrite Inhibit mode

When a buffer full state has occurred in Overwrite Inhibit mode (BUF*n*_STAT.PTR[*x*:0] bits = 10 (BUF1/BUF3) or 12 (BUF2), and BUF*n*_STAT.FULLF bit = 1), it is impossible to determine whether a time stamp trigger has occurred or not after the buffer became full. Therefore, it is recommended to perform data read processing by setting an interrupt to occur before the buffer becomes full (e.g. set the BUF1_CFG1.INTCNT[5:0] bits to 8 (= 10 - 2)).

<Overwrite mode>

1. After an interrupt has occurred (/INT = L), read Register INTF.
   When the INTF.EVF bit = 1, a time stamp event detection interrupt has occurred. In this case, perform the procedure from Step 2.

   If another interrupt has occurred, execute the corresponding interrupt handler.

   * Overwrite mode allows reading of time stamp data any time without waiting for an interrupt (INTF.EVF bit = 1). In this case, Steps 1 (waiting for an interrupt) and 2 (confirming the interrupt factor) are not necessary.

2. Read Registers EVNT_INTF and BUF_INTF to determine the interrupt factor that has occurred.

   <When a flag in Register EVNT_INTF has been set>
   It indicates that an EVIN*n* or internal event has occurred. Table 3.18 shows the set condition of each flag. Execute an interrupt handler according to the event occurred. The flag that has been set to 1 should be cleared by writing 0 in the interrupt handler.

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<When the BUF_INTF.BUF*n*F bit has been set>
In Overwrite mode, this interrupt occurs when the buffered data count retained in the BUF*n*_STAT.PTR[*x*:0] bits reaches or exceeds the value set to the BUF*n*_CFG1.INTCNT[*x*:0] bits by occurrences of the events that have been enabled to capture time stamp data. However, when the internal pointer circulates to 0, the BUF_INTF.BUF*n*F bit is cleared to 0 as well and it will not be set until the pointer reaches the BUF*n*_CFG1.INTCNT[*x*:0] bit setting value. Therefore, be sure to avoid differing the interrupt handling when the BUF_INTF.BUF*n*F bit is set to 1.
Read the captured time stamp data by the following operations.

The explanation below assumes that a BUF1 interrupt has occurred.

3. Set the EVIN_EN.EVIN1CPEN bit to 0 to disable time stamp capturing to BUF1. (See the Note below.)

   * When a BUF3 interrupt has occurred, not only the EVIN_EN.EVIN3CPEN bit but also the CAP_EN.V***L.CPEN and CAP_EN.OSCSTPCPEN bits should be set to 0 to disable the time stamp capturing to BUF3.

4. Read Register BUF1_STAT to obtain the page number of the latest recorded time stamp data (BUF1_STAT.PTR[5:0] bits) and to confirm whether the buffer is full or not (BUF1_STAT.FULLF bit). In addition to this, check if an overwrite has occurred (BUF_OVWF.BUF1OVWF bit).

5. Set the BUF1_CFG2.RDEN bit to 1. (Enable reading of BUF1)

6. Set the BUF1_CFG2.RDPAGE[3:0] bits to 0x1. (Specify read page)

7. Obtain one time stamp data by burst reading 10 bytes from Addresses 0x60 to 0x69.

   See Figure 3.35 for the contents of these addresses.

   * Be sure to read Addresses 0x60 to 0x69 continuously to obtain time stamp data. Reading a part of data is prohibited.

8. Repeat Step 7 within the necessary range of the buffer according to the buffer full status obtained in Step 4.

   <BUF1_STAT.FULLF bit = 0 (buffer has a free space)>
   If the BUF1_CFG2.RDPAGE[3:0] bits has not reached the page number obtained in Step 4, increment the BUF1_CFG2.RDPAGE[3:0] bits and repeat Step 7. The oldest data is obtained in the first reading from Page 0x1.

   <BUF1_STAT.FULLF bit = 1 (buffer full status)>
   Execute Step 7 repeatedly by incrementing the BUF1_CFG2.RDPAGE[3:0] bits from 1 to 10 successively to obtain all time stamp data once.

   If the BUF_OVWF.BUF1OVWF bit is read as 0 (overwrite has not occurred) in Step 4, the latest data is read when the BUF1_CFG2.RDPAGE[3:0] bits = 10. By tracking back from the latest data in reverse order of reading, older data can be obtained in time series.

   If the BUF_OVWF.BUF1OVWF bit is read as 1 (overwrite has occurred), the latest data is read when the BUF1_CFG2.RDPAGE[3:0] bits are set to the page number that has been obtained in Step 4. By tracking back from the latest data in reverse order of reading, older data can be obtained in time series. The buffer forms a ring buffer in which pages are arranged circularly in the order of the 1st captured data page → 10th → 9th … 2nd →1st. The data read from the page <page number obtained in Step 4 + 1> is the oldest.
   However, data in this page is invalid when a time stamp data is captured during reading. To determine if it is valid, check whether the BUF1_CFG2.PTR[3:0] bits are incremented or not after being read.

9. Set the BUF1_CFG2.RDEN bit to 0. (Disable reading of BUF1)

10. Set the WRCMD_CFG.BUF1FCLREN bit to 1 and write any value to Register WRCMD_TRG.
    (Clear BUF1 flags and page pointer)

11. Set the EVIN_EN.EVIN1CPEN bit to 1 to enable time stamp capturing to BUF1. (See the Note below.)

Note on Overwrite mode

In Direct mode with Overwrite mode set, reading and writing from/to the same page in the same buffer may occur simultaneously. For example, there is a possibility of occurrence of this case when an attempt is made to read the page (e.g. Page 1) next to the page indicated by the BUF*n*_STAT.PTR[*x*:0] bits. Steps (3) and (11) are operations to avoid this conflict. They temporarily disable writing of captured data to the buffer to be read. However, the disabled event cannot be recorded in this period.

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Clearing Time Stamp Data

Setting buffer to empty state

As described in "*Issuing Command trigger*," a command trigger is used to initialize the buffer flags and pointers. This can be used to set the buffer into empty state (BUFs can be controlled individually in Direct mode).

1. Set the WRCMD_CFG.BUF*n*FCLREN bit to 1. (Specify BUF*n* initialization)
2. Write any value to the WRCMD_TRG.WRTRG[7:0] bits. (Issue command trigger)
3. Confirm if the WRCMD_TRG.WRTRG[7:0] bits revert to 0x00. (Command execution completed)

Although the SRAM contents are not cleared, buffer empty state can be set.

Clearing SRAM to 0

To clear the SRAM contents to 0, set the buffer into SRAM mode and write 0 directly.

1. Set the following bits in Register BUF1_CFG2:
   - Set the BUF1_CFG2.SRAMMOD bit to 1. (Specify SRAM mode)
   - Set the BUF1_CFG2.RDPAGE[3:0] bit to 0x0. (Specify Page 0)
2. Write 0x00 to Addresses 0x60 to 0x6F. (Clear one page)
3. Terminate the processing if BUF1_CFG2.RDPAGE[3:0] bits = 0xF.
   Increment the BUF1_CFG2.RDPAGE[3:0] bits if not 0xF. (Specify next page)
4. Repeat Steps 2 and 3 until all pages are cleared.
5. Set the BUF1_CFG2.SRAMMOD bit to 0. (Cancel SRAM mode)

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3.10.5 Time Stamp (Event Detection) Interrupts

Figure 3.43 shows the configuration of the time stamp interrupt circuit.

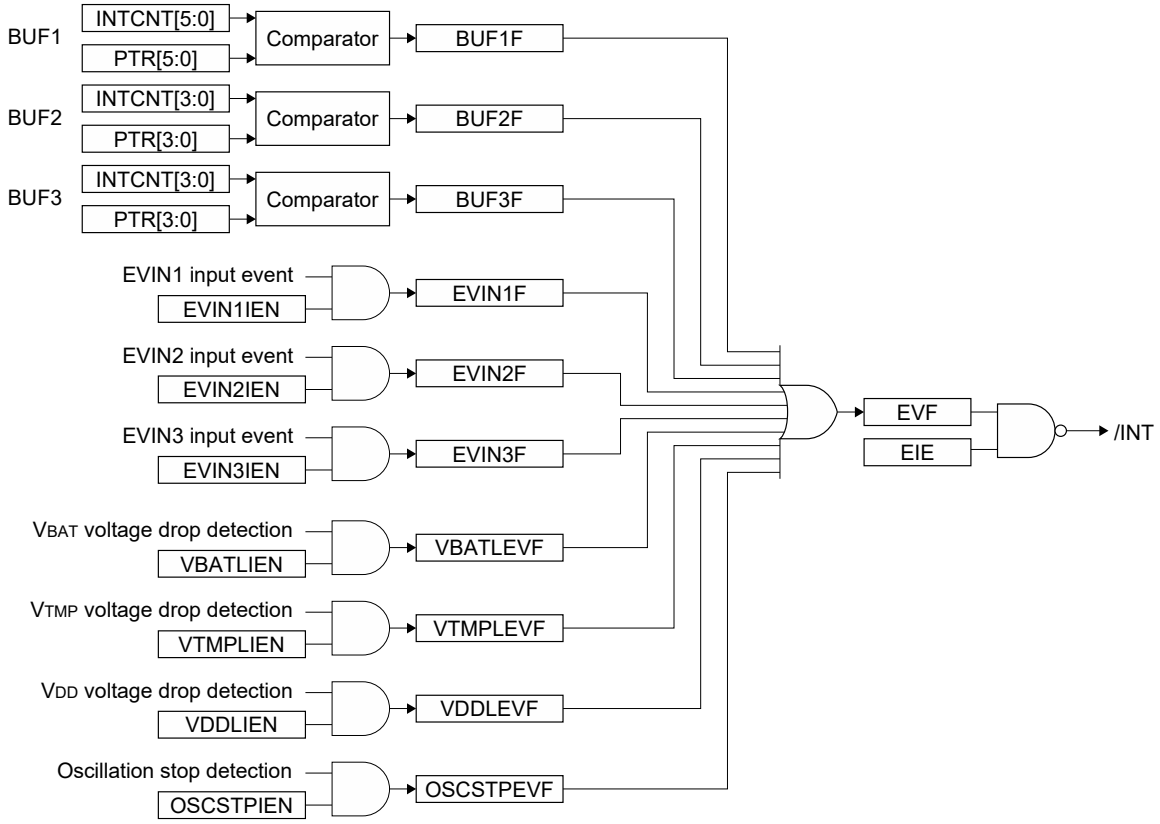


Figure 3.43 Configuration of Time Stamp Interrupt Circuit

The time stamp function has the event detection interrupt factors shown below.

Table 3.18 Event Detection Interrupt Factors and Control Bits

Interrupt factor flag	Interrupt enable bit	Interrupt flag set condition	Clear condition
BUF_INTF.BUF1F	BUF1_CFG1.INTCNT[5:0]	Set when the number of stamp data in BUF*n* reaches the value set in the INTCNT[*x*:0] bits. Not set if the INTCNT[*x*:0] bits = 0x0.	Cleared by writing 0.
BUF_INTF.BUF2F	BUF2_CFG1.INTCNT[3:0]		
BUF_INTF.BUF3F	BUF3_CFG1.INTCNT[3:0]		
EVNT_INTF.EVIN1F	EVNT_INTE.EVIN1IEN	Set when an event trigger is input from the EVIN*n* pin regardless of whether a data is written to the buffer or not. Not set if the EVIN*n*IEN bit = 0.	Cleared by writing 0.
EVNT_INTF.EVIN2F	EVNT_INTE.EVIN2IEN		
EVNT_INTF.EVIN3F	EVNT_INTE.EVIN3IEN		
EVNT_INTF.VBATLEVF	EVNT_INTE.VBATLIEN	Set when a V_{BAT} voltage drop is detected. Not set if the VBATLIEN bit = 0.	Cleared by writing 0.
EVNT_INTF.VTMPLEVF	EVNT_INTE.VTMPLIEN	Set when a V_{DET2} voltage drop is detected. Not set if the VTMPLIEN bit = 0.	Cleared by writing 0.
EVNT_INTF.VDDLEVF	EVNT_INTE.VDDLIEN	Set when a $-V_{DET1}$ voltage drop is detected. Not set if the VDDLIEN bit = 0.	Cleared by writing 0.
EVNT_INTF.OSCSTPEVF	EVNT_INTE.OSCSTPIEN	Set when an oscillation stoppage is detected. Not set if the OSCSTPIEN bit = 0.	Cleared by writing 0.

These factors can be individually enabled/disabled to generate an interrupt. When a factor occurs, the interrupt factor flag is set and INTF.EVF bit is also set. If the TSTP_INTE.EIE bit = 1 (interrupt enabled) at this time, the /INT pin goes low to output an interrupt request to the host. The INTF.EVF bit that has been set to 1 is not cleared by writing 0. To clear the INTF.EVF bit, the flags in Registers BUF_INTF and EVNT_INTF must be all cleared. When the INTF.EVF bit is cleared, the /INT pin goes into a Hi-Z state.

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4 Registers

4.1 List of Registers

Symbol meanings

Bit name = –: This bit is not writable, and the read value is always 0.
Bit name = ×: This bit is not writable, and the read value is undefined.
Bit name = (GP): This is a general-purpose bit that allows writing 0 and 1 as well as reading the contents.

Notes:
- The address values indicate {bank number, address in bank}. (Example: 0x0F = Bank 0, Address 0xF)
- The registers must be accessed in eight-bit units.
- Be sure to avoid writing/reading data to/from an address not listed in the register tables.
- After power is turned on or if the INTF.VLF bit = 1 after the RX4901CE/RX8901CE returns from Backup mode, be sure to initialize all the registers.

Bank 0

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	SEC (Second Data)	–	SEC_H[2:0]			SEC_L[3:0]			
0x01	MIN (Minute Data)	–	MIN_H[2:0]			MIN_L[3:0]			
0x02	HOUR (Hour Data)	–	–	HOUR_H[1:0]		HOUR_L[3:0]			
0x03	WEEKDAY (Day-of-Week Data)	–	WEEK[6:0]						
0x04	DAY (Day Data)	–	–	DAY_H[1:0]		DAY_L[3:0]			
0x05	MONTH (Month Data)	–	–	–	MONTH_H	MONTH_L[3:0]			
0x06	YEAR (Year Data)	YEAR_H[3:0]				YEAR_L[3:0]			
0x07	ALM_MIN (Minute Alarm)	XMAE	MALM_H[2:0]			MALM_L[3:0]			
0x08	ALM_HOUR (Hour Alarm)	XHAE	(GP)	HALM_H[1:0]		HALM_L[3:0]			
0x09	ALM_WEEKDAY (Day-of-Week Alarm / Day Alarm)	XWAE	WKALM[6:0]						
			(GP)	DALM_H[1:0]		DALM_L[3:0]			
0x0A	WTCNT_L (Wakeup Timer Counter Low)	WTCNT[7:0]							
0x0B	WTCNT_M (Wakeup Timer Counter Middle)	WTCNT[15:8]							
0x0C	WTCNT_H (Wakeup Timer Counter High)	WTCNT[23:16]							
0x0D	TCTL (Timer Control)	FSEL[1:0]		USEL0	TE	WADA	–	TSEL[1:0]	
0x0E	INTF (Status Flag)	PORF	OSCSTPF	UF	TF	AF	EVF	VLF	VTMPLF
0x0F	TSTP_INTE (Timer Stop and Interrupt Enable)	CSEL[1:0]		UIE	TIE	AIE	EIE	–	STOP

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Bank 1

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	SUBSEC_L (Sub-Second Data Low)	SUBSEC[1:0]		–	–	–	–	–	–
0x11	SUBSEC_H (Sub-Second Data High)	SUBSEC[9:2]							
0x12	SEC_MIR (Mirrored Second Data, = 0x00)	–	SEC_H[2:0]			SEC_L[3:0]			
0x13	MIN_MIR (Mirrored Minute Data, = 0x01)	–	MIN_H[2:0]			MIN_L[3:0]			
0x14	HOUR_MIR (Mirrored Hour Data, = 0x02)	–	–	HOUR_H[1:0]		HOUR_L[3:0]			
0x15	WEEKDAY_MIR (Mirrored Day-of-Week Data, = 0x03)	–	WEEK[6:0]						
0x16	DAY_MIR (Mirrored Day Data, = 0x04)	–	–	DAY_H[1:0]		DAY_L[3:0]			
0x17	MONTH_MIR (Mirrored Month Data, = 0x05)	–	–	–	MONTH_H	MONTH_L[3:0]			
0x18	YEAR_MIR (Mirrored Year Data, = 0x06)	YEAR_H[3:0]				YEAR_L[3:0]			

Bank 2

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x20	EVIN_EN (Event Input Enable)	–	DIRMOD	EVIN3CPEN	EVIN2CPEN	EVIN1CPEN	EVIN3EN	EVIN2EN	EVIN1EN
0x21	EVIN1_CFG (EVIN1 Configuration)	–	–	–	PUPD[2:0]			POL[1:0]	
0x22	EVIN1_FLT (EVIN1 Noise Filter)	–	–	FLT[5:0]					
0x23	EVIN2_CFG (EVIN2 Configuration)	–	–	–	PUPD[2:0]			POL[1:0]	
0x24	EVIN2_FLT (EVIN2 Noise Filter)	–	–	FLT[5:0]					
0x25	EVIN3_CFG (EVIN3 Configuration)	–	–	–	PUPD[2:0]			POL[1:0]	
0x26	EVIN3_FLT (EVIN3 Noise Filter)	–	–	FLT[5:0]					
0x27	BUF1_CFG1 (BUF1 Configuration 1)	–	OVWEN	INTCNT[5:0]					
0x28	BUF1_STAT (BUF1 Status)	FULLF	EMPTF	PTR[5:0]					
0x29	BUF1_CFG2 (BUF1 Configuration 2)	RDEN	SRAMMOD	–	–	RDPAGE[3:0]			
0x2A	BUF2_CFG1 (BUF2 Configuration 1)	–	OVWEN	–	–	INTCNT[3:0]			
0x2B	BUF2_STAT (BUF2 Status)	FULLF	EMPTF	–	–	PTR[3:0]			
0x2C	BUF2_CFG2 (BUF2 Configuration 2)	RDEN	–	–	–	RDPAGE[3:0]			
0x2D	BUF3_CFG1 (BUF3 Configuration 1)	–	OVWEN	–	–	INTCNT[3:0]			
0x2E	BUF3_STAT (BUF3 Status)	FULLF	EMPTF	–	–	PTR[3:0]			
0x2F	BUF3_CFG2 (BUF3 Configuration 2)	RDEN	–	–	–	RDPAGE[3:0]			

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Bank 3

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x30	ALM_SEC (Second Alarm)	XSAE	SALM_H[2:0]			SALM_L[3:0]			
0x31	ALM_MIN_MIR (Mirrored Minute Alarm, = 0x07)	XMAE	MALM_H[2:0]			MALM_L[3:0]			
0x32	ALM_HOUR_MIR (Mirrored Hour Alarm, = 0x08)	XHAE	(GP)	HALM_H[1:0]		HALM_L[3:0]			
0x33	ALM_WEEKDAY_MIR (Mirrored Day-of-Week Alarm / Day Alarm, = 0x09)	XWAE	WKALM[6:0]						
			(GP)	DALM_H[1:0]		DALM_L[3:0]			
0x34	UPDISEL (Time Update Interrupt Select)	–	–	–	–	–	–	USEL1	–
0x37	PWSW_CFG (Power Switch Configuration)	CHGEN	INIEN	VBATLDETBK	VBATLDETEN	SWSEL[1:0]		VDDSAMP[1:0]	
0x38	WTICFG (Wakeup Timer Interrupt Configuration)	FOEMUX	EVIN3MUX	–	WTONETIM	–	–	WTIOUT	–
0x39	WTCTL (Wakeup Timer Control)	WTRST	–	–	–	WTMODSEL	WTSTOPCTL	–	WTSTOP
0x3A	WTCNT_L_MIR (Mirrored Wakeup Timer Counter Low, = 0x0A)	WTCNT[7:0]							
0x3B	WTCNT_M_MIR (Mirrored Wakeup Timer Counter Middle, = 0x0B)	WTCNT[15:8]							
0x3C	WTCNT_H_MIR (Mirrored Wakeup Timer Counter High, = 0x0C)	WTCNT[23:16]							

Bank 4

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x41	WRCMD_CFG (Command trigger Configuration)	EVCNTCLREN	BUF3FCLREN	BUF2FCLREN	BUF1FCLREN	–	–	–	CMDTRGEN
0x42	WRCMD_TRG (Command trigger)	WRTRG[7:0]							
0x43	EVNT_INTE (Event Interrupt Enable)	EVIN3IEN	EVIN2IEN	EVIN1IEN	–	VBATLIEN	VTMPLIEN	VDDLIEN	OSCSTPIEN
0x44	CAP_EN (Capture Enable)	–	–	–	–	VBATLCPEN	VTMPLCPEN	VDDLCPEN	OSCSTPCPEN
0x46	BUF_INTF (Buffer Interrupt Factor)	BUF3F	BUF2F	BUF1F	–	VBATLF	–	VDDLF	–
0x47	EVNT_INTF (Event Interrupt Factor)	EVIN3F	EVIN2F	EVIN1F	–	VBATLEVF	VTMPLEVF	VDDLEVF	OSCSTPEVF
0x4E	BUF_FULLF (Buffer Full Flag)	–	BUF3FULLF	BUF2FULLF	BUF1FULLF	–	–	–	–
0x4F	BUF_OVWF (Buffer Overwrite Flag)	–	BUF3OVWF	BUF2OVWF	BUF1OVWF	–	–	–	–

Bank 5

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x51	EVIN1_EVCNT (EVIN1 Event Counter)	–	–	EVCNT[5:0]					
0x52	EVIN2_EVCNT (EVIN2 Event Counter)	–	–	EVCNT[5:0]					
0x53	EVIN3_EVCNT (EVIN3 Event Counter)	–	–	EVCNT[5:0]					
0x54	EVINMON (EVIN Monitor)	EVIN3MON	EVIN2MON	EVIN1MON	–	–	–	–	–

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Bank 6 (when reading time stamp data in FIFO mode)

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	TIMESTAMP_SUBSEC_L (SUBSEC Time Stamp Data Low)	SUBSEC[1:0]		×	×	×	×	×	×
0x61	TIMESTAMP_SUBSEC_H (SUBSEC Time Stamp Data High)	SUBSEC[9:2]							
0x62	TIMESTAMP_SEC (SEC Time Stamp Data)	×	SEC_H[2:0]			SEC_L[3:0]			
0x63	TIMESTAMP_MIN (MIN Time Stamp Data)	×	MIN_H[2:0]			MIN_L[3:0]			
0x64	TIMESTAMP_HOUR (HOUR Time Stamp Data)	×	×	HOUR_H[1:0]		HOUR_L[3:0]			
0x65	TIMESTAMP_DAY (DAY Time Stamp Data)	×	×	DAY_H[1:0]		DAY_L[3:0]			
0x66	TIMESTAMP_MONTH (MONTH Time Stamp Data)	×	×	×	MONTH_H	MONTH_L[3:0]			
0x67	TIMESTAMP_YEAR (YEAR Time Stamp Data)	YEAR_H[3:0]				YEAR_L[3:0]			
0x68	TIMESTAMP_EVSTAT (Event Status Time Stamp Data)	EVIN3POL	EVIN2POL	EVIN1POL	×	VBATLSTAT	VTMPLSTAT	VDDLSTAT	OSCSTP STAT
0x69	TIMESTAMP_TRG (Time Stamp Trigger Factor)	EVIN3TRG	EVIN2TRG	EVIN1TRG	WRCMDTRG	VBATLTRG	VTMPLTRG	VDDLTRG	OSCSTPTRG

Bank 6 (when reading time stamp data in Direct mode)

Address	Register name (function)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	TIMESTAMP_SUBSEC_L (SUBSEC Time Stamp Data Low)	SUBSEC[1:0]		×	×	×	×	×	×
0x61	TIMESTAMP_SUBSEC_H (SUBSEC Time Stamp Data High)	SUBSEC[9:2]							
0x62	TIMESTAMP_SEC (SEC Time Stamp Data)	×	SEC_H[2:0]			SEC_L[3:0]			
0x63	TIMESTAMP_MIN (MIN Time Stamp Data)	×	MIN_H[2:0]			MIN_L[3:0]			
0x64	TIMESTAMP_HOUR (HOUR Time Stamp Data)	×	×	HOUR_H[1:0]		HOUR_L[3:0]			
0x65	TIMESTAMP_DAY (DAY Time Stamp Data)	×	×	DAY_H[1:0]		DAY_L[3:0]			
0x66	TIMESTAMP_MONTH (MONTH Time Stamp Data)	×	×	×	MONTH_H	MONTH_L[3:0]			
0x67	TIMESTAMP_YEAR (YEAR Time Stamp Data)	YEAR_H[3:0]				YEAR_L[3:0]			
0x68	TIMESTAMP_EVSTAT (Event Status Time Stamp Data)	EVIN3POL	EVIN2POL	EVIN1POL	×	VBATLSTAT	VTMPLSTAT	VDDLSTAT	OSCSTP STAT
0x69	TIMESTAMP_TRG (Time Stamp Trigger Factor)	×	×	×	WRCMDTRG	VBATLTRG	VTMPLTRG	VDDLTRG	OSCSTPTRG

Bank 6 (SRAM mode)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	SRAM Page N Address 0x0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x61	SRAM Page N Address 0x1								
0x62	SRAM Page N Address 0x2								
0x63	SRAM Page N Address 0x3								
0x64	SRAM Page N Address 0x4								
0x65	SRAM Page N Address 0x5								
0x66	SRAM Page N Address 0x6								
0x67	SRAM Page N Address 0x7								
0x68	SRAM Page N Address 0x8								
0x69	SRAM Page N Address 0x9								
0x6A	SRAM Page N Address 0xA								
0x6B	SRAM Page N Address 0xB								
0x6C	SRAM Page N Address 0xC								
0x6D	SRAM Page N Address 0xD								
0x6E	SRAM Page N Address 0xE								
0x6F	SRAM Page N Address 0xF								

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4.2 Description of Registers

* “x” in the initial value row indicates that the initial value is undefined.

0x00: SEC (Second Data)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	SEC_H[2:0]			SEC_L[3:0]			
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W			R/W			

Bits 6–4: SEC_H[2:0]
Bits 3–0: SEC_L[3:0]

The second counter value can be set or read through these bits.
The SEC_H[2:0] bits are the BCD code (0–5) of the 10-second digit and the SEC_L[3:0] bits are the BCD code (0–9) of the 1-second digit. Writing second data to this address resets the 1/1024-second counter and clears Registers SUBSEC_L and SUBSEC_H to 0.

*1 For more information on the clock and calendar function, refer to “*3.2 Clock and Calendar Function*.”

0x01: MIN (Minute Data)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	MIN_H[2:0]			MIN_L[3:0]			
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W			R/W			

Bits 6–4: MIN_H[2:0]
Bits 3–0: MIN_L[3:0]

The minute counter value can be set or read through these bits.
The MIN_H[2:0] bits are the BCD code (0–5) of the 10-minute digit and the MIN_L[3:0] bits are the BCD code (0–9) of the 1-minute digit.

*1 For more information on the clock and calendar function, refer to “*3.2 Clock and Calendar Function*.”

0x02: HOUR (Hour Data)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	HOUR_H[1:0]		HOUR_L[3:0]			
Initial value	0	0	x	x	x	x	x	x
R/W	R	R	R/W		R/W			

Bits 5–4: HOUR_H[1:0]
Bits 3–0: HOUR_L[3:0]

The hour counter value can be set or read through these bits.
The HOUR_H[1:0] bits are the BCD code (0–2) of the 10-hour digit and the HOUR_L[3:0] bits are the BCD code (0–9) of the 1-hour digit.

*1 For more information on the clock and calendar function, refer to “*3.2 Clock and Calendar Function*.”

0x03: WEEKDAY (Day-of-Week Data)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	WEEK[6:0]						
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W						

Bits 6–0: WEEK[6:0]

The day-of-week counter value can be set or read through these bits.
Each WEEK[6:0] bit one-to-one corresponds to a day of the week as the setting example shown below. Therefore, only one bit corresponding to today must be set. The WEEK[6:0] bits are shifted one bit to the left at the same time the day counter is updated (bit 6 is shifted to bit 0).

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Example of day of week setting

WEEK6	WEEK5	WEEK4	WEEK3	WEEK2	WEEK1	WEEK0
Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday
(0x40)	(0x20)	(0x10)	(0x08)	(0x04)	(0x02)	(0x01)

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

0x04: DAY (Day Data)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	DAY_H[1:0]		DAY_L[3:0]			
Initial value	0	0	x	x	x	x	x	x
R/W	R	R	R/W		R/W			

Bits 5–4: DAY_H[1:0]
Bits 3–0: DAY_L[3:0]

The day counter value can be set or read through these bits.
The DAY_H[1:0] bits are the BCD code (0–3) of the 10-day digit and the DAY_L[3:0] bits are the BCD code (0–9) of the 1-day digit.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

*2 For the behavior of the register at leap years, refer to "*Leap Year Determination*" in Section 3.2.

0x05: MONTH (Month Data)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	MONTH_H	MONTH_L[3:0]			
Initial value	0	0	0	x	x	x	x	x
R/W	R	R	R	R/W	R/W			

Bit 4: MONTH_H
Bits 3–0: MONTH_L[3:0]

The month counter value can be set or read through these bits.
The MONTH_H bits are the BCD code (0–1) of the 10-month digit and the MONTH_L[3:0] bits are the BCD code (0–9) of the 1-month digit.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

0x06: YEAR (Year Data)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	YEAR_H[3:0]				YEAR_L[3:0]			
Initial value	x	x	x	x	x	x	x	x
R/W	R/W				R/W			

Bits 7–4: YEAR_H[3:0]
Bits 3–0: YEAR_L[3:0]

The year counter value can be set or read through these bits.
The YEAR_H[3:0] bits are the BCD code (0–9) of the 10-year digit and the YEAR_L[3:0] bits are the BCD code (0–9) of the 1-year digit.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

0x07: ALM_MIN (Minute Alarm)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	XMAE	MALM_H[2:0]			MALM_L[3:0]			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W			R/W			

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Bit 7: XMAE

This bit enables/disables the minute alarm setting.

1 (R/W): Minute alarm is disabled.
0 (R/W): Minute alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation.
When this bit is set to 0, the setting in this register is enabled and coincidence between the minute counter value and the setting value of the MALM_H[2:0] and MALM_L[3:0] bits is included in the alarm generation condition.

Bits 6–4: MALM_H[2:0]
Bits 3–0: MALM_L[3:0]

These bits set the minute alarm condition in a BCD code.
The MALM_H[2:0] bits specify the 10-minute digit (0–5) and the MALM_L[3:0] bits specify 1-minute digit (0–9).

*1 For more information on the alarm function, refer to "*3.5 Alarm Function*."

*2 When the alarm function is not used, this register can be used as a readable/writable general-purpose register. However, set the TSTP_INTE.AIE bit to 0 (alarm interrupt disabled) to prevent unnecessary interrupts from occurring.

0x08: ALM_HOUR (Hour Alarm)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XHAE**	**(GP)**	**HALM_H[1:0]**		**HALM_L[3:0]**			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W	R/W		R/W			

Bit 7: XHAE

This bit enables/disables the hour alarm setting.

1 (R/W): Hour alarm is disabled.
0 (R/W): Hour alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation.
When this bit is set to 0, the setting in this register is enabled and coincidence between the hour counter value and the setting value of the HALM_H[1:0] and HALM_L[3:0] bits is included in the alarm generation condition.

Bits 5–4: HALM_H[1:0]
Bits 3–0: HALM_L[3:0]

These bits set the hour alarm condition in a BCD code.
The HALM_H[1:0] bits specify the 10-hour digit (0–2) and the HALM_L[3:0] bits specify 1-hour digit (0–9).

*1 For more information on the alarm function, refer to "*3.5 Alarm Function*."

*2 When the alarm function is not used, this register can be used as a readable/writable general-purpose register. However, set the TSTP_INTE.AIE bit to 0 (alarm interrupt disabled) to prevent unnecessary interrupts from being occurred.

0x09: ALM_WEEKDAY (Day-of-Week Alarm / Day Alarm)

Day-of-Week Alarm

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XWAE**	**WKALM[6:0]**						
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W						

Day Alarm

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XWAE**	**(GP)**	**DALM_H[1:0]**		**DALM_L[3:0]**			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W	R/W		R/W			

Note: This register switches its function according to the TCTL.WADA bit setting.
TCTL.WADA bit = 0: Day-of-Week Alarm
TCTL.WADA bit = 1: Day Alarm

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Bit 7: XWAE

This bit enables/disables the day-of-week or day alarm setting.

1 (R/W): Day-of-week/day alarm is disabled.
0 (R/W): Day-of-week/day alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation.
When this bit is set to 0, the setting in this register is enabled and an alarm will be generated if the following condition is met.

TCTL.WADA bit = 0: The same bit in the day-of-week counter as one that has been set within WKALM[6:0] is set.

TCTL.WADA bit = 1: The day counter value matches with the DALM_H[1:0]/DALM_L[3:0] bit setting value.

Bits 6–0: WKALM[6:0] (Day-of-Week Alarm)

These bits set the day-of-week alarm condition.
More than one bit can be set to specify two or more days of the week.

Bits 5–4: DALM_H[1:0] (Day Alarm)
Bits 3–0: DALM_L[3:0] (Day Alarm)

These bits set the day alarm condition in a BCD code.
The DALM_H[1:0] bits specify the 10-day digit (0–3) and the DALM_L[3:0] bits specify 1-day digit (0–9).

*1 For more information on the alarm function, refer to "*3.5 Alarm Function*."

*2 When the alarm function is not used, this register can be used as a readable/writable general-purpose register. However, set the TSTP_INTE.AIE bit to 0 (alarm interrupt disabled) to prevent unnecessary interrupts from being occurred.

0x0A: WTCNT_L (Wakeup Timer Counter Low)
0x0B: WTCNT_M (Wakeup Timer Counter Middle)
0x0C: WTCNT_H (Wakeup Timer Counter High)

Wakeup Timer Counter Low

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	WTCNT[7:0]							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Wakeup Timer Counter Middle

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	WTCNT[15:8]							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Wakeup Timer Counter High

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	WTCNT[23:16]							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Bits 7–0: WTCNT[7:0] (Wakeup Timer Counter Low)
WTCNT[15:8] (Wakeup Timer Counter Middle)
WTCNT[23:16] (Wakeup Timer Counter High)

When writing
These registers set the preset value for the wakeup timer counter. The wakeup timer allows setting of a preset value within the range from 1 to 16777215 and uses it as the count period. If 0x000000 is written to these registers, the preset data is treated as 0x000001. When the counter exceeds the preset value, the initial value (1) is loaded to the counter.

Note: Make sure the TCTL.TE bit = 0 (wakeup timer disabled) before setting a preset value.

When reading
When the TCTL.TE bit = 1 (wakeup timer enabled), the current counter value is read out from these registers.
When the TCTL.TE bit = 0 (wakeup timer disabled), the currently set preset value is read out.

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Note: The counter value can be read even while the wakeup timer is operating. However, the valid current value may not be read, as the counter may change while three registers are being read. To obtain the correct value, read the registers twice or more and determine that the read value is correct if the same value is read twice in succession.

*1 For more information on the wakeup timer function, refer to "*3.6 Wakeup Timer Function*."

*2 When the wakeup timer is not used (both the TCTL.TE and TSTP_INTE.TIE bits are set to 0), these registers can be used as readable/writable general-purpose registers.

0x0D: TCTL (Timer Control)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**FSEL[1:0]**		**USEL0**	**TE**	**WADA**	**–**	**TSEL[1:0]**	
Initial value	0	0	0	0	0	0	1	0
R/W	R/W		R/W	R/W	R/W	R	R/W	

Bits 7–6: FSEL[1:0]

These bits select an FOUT frequency.

Table 4.1 FOUT Output Clock Selections

TCTL.FSEL[1:0]	Output clock
0b00	32.768 kHz (default)
0b01	1024 Hz
0b10	1 Hz
0b11	Off

Bit 5: USEL0

This bit selects a time update interrupt event by using it together with the UPDISEL.USEL1 bit.

Table 4.2 Time Update Interrupt Event Selections

UPDISEL.USEL1	TCTL.USEL0	Interrupt event
0	0	Second counter update (default)
0	1	Minute counter update
1	0	Hour counter update
1	1	No interrupt event

Bit 4: TE

This bit enables/disables wakeup timer interrupts.

1 (R/W): Wakeup timer interrupts are enabled.
0 (R/W): Wakeup timer interrupts are disabled.

Bit 3: WADA

This bit selects either day-of-week alarm or day alarm to be used as an alarm generation condition.

1 (R/W): Day alarm
0 (R/W): Day-of-week alarm

Bits 1–0: TSEL[1:0]

These bits select the source clock of the wakeup timer.

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Table 4.3 Wakeup Timer Source Clock Selections

TCTL.TSEL[1:0]	Source clock
0b00	1024 Hz
0b01	64 Hz
0b10	1 Hz (default)
0b11	1/60 Hz

*1 For more information on the FOUT function, refer to "*3.7 FOUT Output Function*."

*2 For more information on the time update interrupt, refer to "*3.4 Time Update Interrupt Function*."

*3 For more information on the wakeup timer function, refer to "*3.6 Wakeup Timer Function*."

*4 For more information on the alarm function, refer to "*3.5 Alarm Function*."

0x0E: INTF (Status Flag)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**PORF**	**OSCSTPF**	**UF**	**TF**	**AF**	**EVF**	**VLF**	**VTMPLF**
Initial value	1	1	x	0	x	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

Bit 7: PORF

This is a self-monitoring flag that indicates whether a power-on-reset is executed after power is turned on or not.

1 (R): Power-on-reset has been detected.
0 (R): Power-on-reset has not been detected.
1 (W): Ineffective
0 (W): Flag clear (effective only when power-on reset has been cancelled)

Bit 6: OSCSTPF

This is a self-monitoring flag that indicates whether the oscillation of the crystal oscillator has stopped or not.

1 (R): Oscillation stop state has been detected. (Set to 1 by detecting an oscillation stop for 10 ms or more.)
0 (R): Oscillator stop state has not been detected.
1 (W): Ineffective
0 (W): Flag clear (effective only when an oscillation stop state has not been detected)

Bit 5: UF
Bit 4: TF
Bit 3: AF
Bit 2: EVF

They are interrupt flags that indicate occurrence of an RTC interrupt event.

1 (R): Interrupt event has occurred.
0 (R): No interrupt event has occurred.
1 (W): Ineffective
0 (W): Flag clear (except for EVF)

The following shows the correspondence between the bit and interrupt:

UF: Time update interrupt
TF: Wakeup timer interrupt
AF: Alarm interrupt
EVF: Time stamp event detection interrupt

In the wakeup timer (TF), time update (UF), and alarm (AF) interrupts, clearing the flag by writing 0 negates the /INT signal (low to Hi-Z).
The low output from /INT by a wakeup timer or time update interrupt event is automatically cancelled after a prescribed time has elapsed from occurrence of an interrupt event. However, the interrupt flag (TF or UF) is not automatically cleared.

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Various events that generate an interrupt exist in the event detection and time stamp function, and the interrupt flags that are set when the corresponding event occurs are assigned in Registers BUF_INTF and EVNT_INTF. The EVF bit is set to 1 at the same time one or more interrupt flags are set and it is cleared to 0 when all the flags in Registers BUF_INTF and EVNT_INTF are cleared (it is not cleared by writing 0). This clear operation also negates the /INT signal.

Bit 1: VLF

This is a self-monitoring flag that indicates an abnormality of the RX4901CE/RX8901CE.

1 (R): There is an abnormality. (PORF bit = 1 or OSCSTPF bit = 1)
0 (R): No abnormality
1 (W): Ineffective
0 (W): Flag clear (effective only when power-on reset has been cancelled and an oscillation stop state has not been detected)

Bit 0: VTMPLF

This is a self-monitoring flag that indicates the history of a V_{OUT} voltage drop to the temperature compensation update stop voltage or less ($V_{OUT} = V_{DD}$ or $V_{BAT} \leq V_{DET2}$).

1 (R): Voltage drop has been detected. (V_{DD} or $V_{BAT} \leq V_{DET2}$, temperature compensation update stopped)
0 (R): Voltage drop has not been detected.
1 (W): Ineffective
0 (W): Flag clear (effective only when the V_{OUT} voltage is normal)

*1 For more information on the self-monitoring function, refer to "*3.8 Self-Monitoring Function*."

*2 For more information on the interrupts, refer to "*3.4 Time Update Interrupt Function*," "*3.6 Wakeup Timer Function*," "*3.5 Alarm Function*," or "*3.10 Time Stamp Function*."

0x0F: TSTP_INTE (Timer Stop and Interrupt Enable)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**CSEL[1:0]**		**UIE**	**TIE**	**AIE**	**EIE**	**–**	**STOP**
Initial value	0	1	0	0	0	0	0	0
R/W	R/W		R/W	R/W	R/W	R/W	R	R/W

Bits 7–6: CSEL[1:0]

These bits set the execution interval of the temperature sensor measurement operation.

Table 4.4 Execution Interval of Temperature Sensor Measurement Operation

TSTP_INTE.CSEL[1:0]	Execution interval
0b00	0.5 seconds
0b01	2 seconds (default)
0b10	10 seconds
0b11	30 seconds

Bit 5: UIE
Bit 4: TIE
Bit 3: AIE
Bit 2: EIE

These bits enable the RX4901CE/RX8901CE interrupts.

1 (W): Enables interrupts.
0 (W): Disables interrupts. (Clears the interrupt signal. Note)

Note: The interrupt signals from all the interrupt sources are NORed before being output from the /INT pin. Therefore, clearing the interrupt signal from an interrupt source may not negate the /INT signal.

Each bit corresponds to an interrupt as shown below.

UIE: Time update interrupt
TIE: Wakeup timer interrupt
AIE: Alarm interrupt
EIE: Time stamp event detection interrupt

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Bit 0: STOP

This bit controls the counter operations.

1 (W): Stops operating of the counters.
0 (W): Starts operating of the counters.
1 (R): The timer is idle.
0 (R): The timer is operating.

The STOP bit stops the following operations:

1) 1/1024-second, second, minute, day, day of week, month, and year counter update operations
Consequently, a time update interrupt and an alarm interrupt do not occur.
The time stamp function uses the time at the point the counters stop as the clock data.

2) Wakeup timer interrupt
The wakeup timer stops and does not generate an interrupt.

3) FOUT output
The FOUT output is fixed at H or L when 1 Hz output is selected.
When 32.768 kHz or 1024 Hz is selected, the output continues even if the STOP bit = 1.

Note: If the timer is stopped by the STOP bit when reading clock/calendar data, time error is increased. Therefore, do not stop the counter using the STOP bit when reading the clock/calendar registers.

*1 For more information on the temperature compensation operation, refer to "*3.3 Temperature Compensation Function*."

*2 For more information on the interrupts, refer to "*3.4 Time Update Interrupt Function*," "*3.6 Wakeup Timer Function*," "*3.5 Alarm Function*," or "*3.10 Time Stamp Function*."

0x10: SUBSEC_L (Sub-Second Data Low)
0x11: SUBSEC_H (Sub-Second Data High)

Sub-Second Data Low

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**SUBSEC[1:0]**		–	–	–	–	–	–
Initial value	x	x	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R	R	R	R

Sub-Second Data High

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**SUBSEC[9:2]**							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Bits 7–6: SUBSEC[1:0] (Sub-Second Data Low)
Bits 7–0: SUBSEC[9:2] (Sub-Second Data High)

These bits are used to set and read the 1/1024-second counter, which is a 10-bit binary counter.
The SUBSEC_L.SUBSEC[1:0] bits are the low-order 2 bits of the 1/1024-second counter and the SUBSEC_H. SUBSEC[9:2] bits are the high-order 8 bits.

Table 4.5 SUBSEC[9:0] bits

Bit	SUBSEC9	SUBSEC8	SUBSEC7	SUBSEC6	SUBSEC5	SUBSEC4	SUBSEC3	SUBSEC2	SUBSEC1	SUBSEC0
Count value (1024 Hz cycle)	512	256	128	64	32	16	8	4	2	1

To obtain or change the 1/1024-second counter value, read or write these two addresses continuously. By accessing Addresses 0x12 to 0x18 following it, the clock/calendar data can be read/written successively.
Writing data to Register SEC (Address 0x00) resets the 1/1024-second counter, as a result, Registers SUBSEC_L and SUBSEC_H are cleared to 0. On the other hand, writing data to Register SEC_MIR (Address 0x12), which is the mirror address of Register SEC, does not reset the 1/1024-second counter.

*1 For more information on the clock and calendar function, refer to "*3.2 Clock and Calendar Function*."

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0x12: SEC_MIR (Mirrored Second Data, = 0x00)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	SEC_H[2:0]			SEC_L[3:0]			
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W			R/W			

This is a mirror register of Register SEC. For more information, refer to "*0x00: SEC (Second Data)*." However, writing to this address does not reset the 1/1024-second counter.

0x13: MIN_MIR (Mirrored Minute Data, = 0x01h)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	MIN_H[2:0]			MIN_L[3:0]			
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W			R/W			

This is a mirror register of Register MIN. For more information, refer to "*0x01: MIN (Minute Data)*."

0x14: HOUR_MIR (Mirrored Hour Data, = 0x02)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	HOUR_H[1:0]		HOUR_L[3:0]			
Initial value	0	0	x	x	x	x	x	x
R/W	R	R	R/W		R/W			

This is a mirror register of Register HOUR. For more information, refer to "*0x02: HOUR (Hour Data)*."

0x15: WEEKDAY_MIR (Mirrored Day-of-Week Data, = 0x03)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	WEEK[6:0]						
Initial value	0	x	x	x	x	x	x	x
R/W	R	R/W						

This is a mirror register of Register WEEKDAY. For more information, refer to "*0x03: WEEKDAY (Day-of-Week Data)*."

0x16: DAY_MIR (Mirrored Day Data, = 0x04)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	DAY_H[1:0]		DAY_L[3:0]			
Initial value	0	0	x	x	x	x	x	x
R/W	R	R	R/W		R/W			

This is a mirror register of Register DAY. For more information, refer to "*0x04: DAY (Day Data)*."

0x17: MONTH_MIR (Mirrored Month Data, = 0x05)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	MONTH_H	MONTH_L[3:0]			
Initial value	0	0	0	x	x	x	x	x
R/W	R	R	R	R/W	R/W			

This is a mirror register of Register MONTH. For more information, refer to "*0x05: MONTH (Month Data)*."

0x18: YEAR_MIR (Mirrored Year Data, = 0x06)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	YEAR_H[3:0]				YEAR_L[3:0]			
Initial value	x	x	x	x	x	x	x	x
R/W	R/W				R/W			

This is a mirror register of Register YEAR. For more information, refer to "*0x06: YEAR (Year Data)*."

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0x20: EVIN_EN (Event Input Enable)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	DIRMOD	EVIN3CPEN	EVIN2CPEN	EVIN1CPEN	EVIN3EN	EVIN2EN	EVIN1EN
Initial value	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 6: DIRMOD

This bit selects the time stamp buffer operating mode.

1 (R/W): Direct mode
0 (R/W): FIFO mode

Bit 5 EVIN3CPEN
Bit 4 EVIN2CPEN
Bit 3 EVIN1CPEN

These bits enable/disable external event trigger inputs from the EVIN*n* pin to capture time stamp data to the buffer.

1 (R/W): EVIN*n* is enabled to capture time stamp data.
0 (R/W): EVIN*n* is disabled to capture time stamp data.

The EVIN*n*CPEN bit setting is effective when the EVIN*n*EN bit (described below) = 1.

Bit 2 EVIN3EN
Bit 1 EVIN2EN
Bit 0 EVIN1EN

These bits enable/disable the EVIN*n* pin to input external event triggers.

1 (R/W): EVIN*n* is enabled to input event triggers.
0 (R/W): EVIN*n* is disabled to input event triggers.

*1 For more information on the time stamp function, refer to "*3.10 Time Stamp Function*."

0x21: EVIN1_CFG (EVIN1 Configuration)
0x23: EVIN2_CFG (EVIN2 Configuration)
0x25: EVIN3_CFG (EVIN3 Configuration)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	PUPD[2:0]			POL[1:0]	
Initial value	0	0	0	0	1	0	0	0
R/W	R	R	R	R/W			R/W	

Bits 4–2: PUPD[2:0]

These bits select an internal pull-up or pull-down resistor to be connected to the EVIN*n* pin.

Table 4.6 EVIN*n* Pin Pull-Up/Pull-Down Resistor Selections

EVIN*n*_CFG.PUPD[2:0]	Pull-up/down resistor
0b000	No pull-up/down resistor
0b001	Pull-up resistor 500 kΩ
0b010	Pull-up resistor 1 MΩ (default)
0b011	Pull-up resistor 10 MΩ
0b100	Pull-down resistor 500 kΩ
Other	No pull-up/down resistor

Bits 1–0: POL[1:0]

These bits select the EVIN*n* input signal detection edge polarity that captures time stamp data.

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Table 4.7 Selecting EVIN*n* Input Signal Detection Edge Polarity

EVIN*n*_CFG.POL[1:0]	Detection edge polarity
0b00	Falling edge (default)
0b01	Rising edge
0b10	Rising and falling edges
0b11	

*1 For more information on the time stamp function, refer to "*3.10 Time Stamp Function*."

0x22: EVIN1_FLT (EVIN1 Noise Filter)
0x24: EVIN2_FLT (EVIN2 Noise Filter)
0x26: EVIN3_FLT (EVIN3 Noise Filter)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	FLT[5:0]					
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R/W					

Bits 5–0: FLT[5:0]

These bits set the noise filtering time for the EVIN*n* input signals (FLT[5:0] × 125 ms).

Table 4.8 Valid EVIN*n* Input Pulse Width

EVIN*n*_FLT. FLT[5:0]	Uncertain EVIN*n* pulse width (Whether the edge input is detected or not depends on the relationship between the edge input timing and the sampling timing in 125 ms cycles.)	Valid EVIN*n* pulse width (The edge input is always detected.)
0x00	–	1 ms or more
0x01 (Setting prohibited)	–	–
0x02	125 ms or more and less than 250 ms	250 ms or more
0x03	250 ms or more and less than 375 ms	375 ms or more
:	:	:
0x27	4750 ms or more and less than 4875 ms	4875 ms or more
0x28	4875 ms or more and less than 5000 ms	5000 ms or more
0x29 or more (Setting prohibited)	–	–

*1 For more information on the time stamp function, refer to "*3.10 Time Stamp Function*."

0x27: BUF1_CFG1 (BUF1 Configuration 1)
0x2A: BUF2_CFG1 (BUF2 Configuration 1)
0x2D: BUF3_CFG1 (BUF3 Configuration 1)

BUF1 Configuration 1

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	OVWEN	INTCNT[5:0]					
Initial value	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W					

BUF2/BUF3 Configuration 1

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	OVWEN	0	0	INTCNT[3:0]			
Initial value	0	0	0	0	0	0	0	0
R/W	R	R/W	R	R	R/W			

Bit 6: OVWEN

This bit sets the write mode after the buffer (FIFO or BUF*n*) becomes full.

1 (R/W): Overwrite mode (buffer data is overwritten from oldest.)
0 (R/W): Overwrite Inhibit mode (recording stops in buffer full state, captured data are discarded.)

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Bit 5–0: INTCNT[5:0] (BUF1 Configuration 1)
Bit 3–0: INTCNT[3:0] (BUF2/BUF3 Configuration 1)

These bits set the number of data captured to the buffer (BUF*n*) to generate an interrupt.

INTCNT[5:0] bits (BUF1/FIFO buffer event input)
An event input interrupt factor occurs when the BUF1_STAT.PTR[5:0] bit value (FIFO mode: number of remaining buffer data, Direct mode: number of data captured in the buffer) reaches the INTCNT[5:0] bit setting value. After that, an event input interrupt factor occurs every time a time stamp capture to the FIFO/BUF1 occurs until the BUF1_STAT.PTR[5:0] bit value decreases below the INTCNT[5:0] bit setting value.

Examples:

1) When the INTCNT[5:0] bits = 0x00
   No event interrupt factor occurs regardless of the number of events issued.
2) When the INTCNT[5:0] bits = 0x01
   An event interrupt factor occurs every time an event is issued.
3) When the INTCNT[5:0] bits = 0x20 (in FIFO mode)
   An event interrupt factor occurs when the number of data captured in the buffer (FIFO) by event trigger input reaches 32.

The INTCNT[3:0] bits (BUF2/BUF3 event input) have the same function except the in setting range as shown in the table below.

Table 4.9 Number of BUF*n* Event Inputs to Generate Interrupt

Control bits for specifying event input count	Specifiable range		Pointer indicating valid buffered data count
	FIFO mode	Direct mode	
BUF1_CFG1.INTCNT[5:0] bits	0x00 to 0x1F	0x00 to 0x09 (BUF1)	BUF1_STAT.PTR[5:0] bits
BUF2_CFG1.INTCNT[3:0] bits	Ineffective	0x0 to 0xB (BUF2)	BUF2_STAT.PTR[3:0] bits
BUF3_CFG1.INTCNT[3:0] bits	Ineffective	0x0 to 0x9 (BUF3)	BUF3_STAT.PTR[3:0] bits

*1 For more information on the time stamp function, refer to "*3.10 Time Stamp Function*."

0x28: BUF1_STAT (BUF1 Status)
0x2B: BUF2_STAT (BUF2 Status)
0x2E: BUF3_STAT (BUF3 Status)

BUF1 Status

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**FULLF**	**EMPTF**	**PTR[5:0]**					
Initial value	0	1	0	0	0	0	0	0
R/W	R	R	R					

BUF2/BUF3 Status

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**FULLF**	**EMPTF**	**–**	**–**	**PTR[3:0]**			
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R			

Bit 7: FULLF

This flag indicates whether the buffer (FIFO or BUF*n*) is in full state or not.

1 (R): Buffer full state
0 (R): Free space available in the buffer

In FIFO mode, the BUF1_STAT.FULLF bit indicates the buffer status.
The flag set to 1 reverts to 0 when a free space is made in the buffer.

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Bit 6: EMPTF

This flag indicates whether the buffer (FIFO or BUF*n*) is in empty state or not.

1 (R): Buffer empty state
0 (R): Buffer data available

In FIFO mode, the BUF1_STAT.EMPTF bit indicates the buffer status.
The flag set to 1 reverts to 0 when data is captured in the buffer.

Bits 5–0: PTR[5:0] (BUF1 Status)
Bits 3–0: PTR[3:0] (BUF2/BUF3 Status)

These bits indicate the number of data stored in the buffer (FIFO or BUF*n*).

FIFO mode: Indicates the number of remaining data in the FIFO that can be read (BUF1: 0 to 32).

Direct mode: Indicates the number of data captured in BUF*n* (capture count, BUF1/BUF3: 0 to 10, BUF2: 0 to 12)

Note: Updating the flags and pointers in this register needs a time interval of up to 1 ms after a stamp data is read from the buffer in FIFO mode.

*1 For more information on the time stamp function, refer to "*3.10 Time Stamp Function*."

0x29: BUF1_CFG2 (BUF1 Configuration 2)
0x2C: BUF2_CFG2 (BUF2 Configuration 2)
0x2F: BUF3_CFG2 (BUF3 Configuration 2)

BUF1 Configuration 2

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**RDEN**	**SRAMMOD**	**–**	**–**	**RDPAGE[3:0]**			
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R/W			

BUF2/BUF3 Configuration 2

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**RDEN**	**–**	**–**	**–**	**RDPAGE[3:0]**			
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R/W			

Bit 7: RDEN

This bit specifies the buffer (BUF*n*) from which stamp data is read in Direct mode.

1 (R/W): BUF*n* is enabled to be read.
0 (R/W): BUF*n* is disables to be read.

Bit 6: SRAMMOD (BUF1 Configuration 2)

This bit enables/disables SRAM mode for reading/writing from/to the buffer.

1 (R/W): SRAM mode is enabled.
0 (R/W): SRAM mode is disabled.

Bits 3–0: RDPAGE[3:0]

These bits specify the page number of the buffer to be read in Direct or SRAM mode. It is effective only when the RDEN bit = 1.

Direct mode: Pages 1 to 10 (BUF1/3), Pages 1 to 12 (BUF2)
In Direct mode, it is necessary to specify a page number indicated by the BUF3_STAT. PTR[3:0] bits or less, or disable the event trigger to be issued before reading data.

SRAM mode: Pages 0x0 to 0xF

*1 For more information on the time stamp function and how to read/write the SRAM/buffer, refer to "*3.10 Time Stamp Function*."

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0x30: ALM_SEC (Second Alarm)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XSAE**	**SALM_H[2:0]**			**SALM_L[3:0]**			
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W			R/W			

Bit 7: XSAE

This bit enables/disables the second alarm setting.

1 (R/W): Second alarm is disabled.
0 (R/W): Second alarm is enabled.

When this bit is set to 1, the setting in this register is disabled and it does not affect alarm generation.
When this bit is set to 0, the setting in this register is enabled and coincidence between the second counter value and the setting value of the SALM_H[2:0] and SALM_L[3:0] bits is included in the alarm generation condition.

Bits 6–4: SALM_H[2:0]
Bits 3–0: SALM_L[3:0]

These bits set the second alarm condition in a BCD code.
The SALM_H[2:0] bits specify the 10-second digit (0–5) and the SALM_L[3:0] bits specify 1-second digit (0–9).

*1 For controlling the alarm function, refer to "*3.5 Alarm Function*."

*2 When the alarm function is not used, this register can be used as a readable/writable general-purpose register. However, set the TSTP_INTE.AIE bit to 0 (alarm interrupt disabled) to prevent unnecessary interrupts from being occurred.

0x31: ALM_MIN_MIR (Mirrored Minute Alarm, = 0x07)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XMAE**	**MALM_H[2:0]**			**MALM_L[3:0]**			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W			R/W			

This is a mirror register of Register ALM_MIN. For more information, refer to "*0x07: ALM_MIN (Minute Alarm)*."

0x32: ALM_HOUR_MIR (Mirrored Hour Alarm, = 0x08)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XHAE**	**(GP)**	**HALM_H[1:0]**		**HALM_L[3:0]**			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W	R/W		R/W			

This is a mirror register of Register ALM_HOUR. For more information, refer to "*0x08: ALM_HOUR (Hour Alarm)*."

0x33: ALM_WEEKDAY_MIR (Mirrored Day-of-Week Alarm / Day Alarm, = 0x09)

Mirrored Day-of-Week Alarm

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XWAE**	**WKALM[6:0]**						
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W						

Mirrored Day Alarm

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**XWAE**	**(GP)**	**DALM_H[1:0]**		**DALM_L[3:0]**			
Initial value	1	x	x	x	x	x	x	x
R/W	R/W	R/W	R/W		R/W			

This is a mirror register of Register ALM_WEEKDAY. For more information, refer to "*0x09: ALM_WEEKDAY (Day-of-Week Alarm / Day Alarm)*."

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0x34: UPDISEL (Time Update Interrupt Select)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	–	–	–	**USEL1**	–
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W	R

Bit 1: USEL1

This bit selects a time update interrupt event by using it together with the TCTL.USEL0 bit (see Table 4.2.).

0x37: PWSW_CFG (Power Switch Configuration)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**CHGEN**	**INIEN**	**VBATLDETBK**	**VBATLDETEN**	**SWSEL[1:0]**		**VDDSAMP[1:0]**	
Initial value	0	0	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W		R/W	

Bit 7: CHGEN

This bit controls the V_{BAT} charge function.

1 (R/W): Charge is enabled.
0 (R/W): Charge is disabled.

When a secondary battery is connected to the V_{BAT} pin, set both the INIEN bit and this bit to 1 to enable the auto power switching function and V_{BAT} charge functions.

Bit 6: INIEN

This bit controls the auto power switching function.

1 (R/W): Auto power switching function is enabled.
0 (R/W): Auto power switching function is disabled.

Bit 5: VBATLDETBK

This bit selects whether the V_{BAT} voltage detection is performed in Backup mode or not. This setting is effective when the VBATLDETEN bit = 1 (V_{BAT} voltage detection enabled).

1 (R/W): V_{BAT} voltage detection is enabled in Backup mode.
0 (R/W): V_{BAT} voltage detection is disabled in Backup mode.

Bit 4: VBATLDETEN

This bit selects whether the V_{BAT} voltage detection is performed or not.

1 (R/W): V_{BAT} voltage detection is enabled.
0 (R/W): V_{BAT} voltage detection is disabled.

Bits 3–2: SWSEL[1:0]

These bits select a power supply change over switch (SW) status when the auto power switching function is not used.

Table 4.10 Fixing Power Switch Setting

PWSW_CFG.SWSEL[1:0]	Power switch status	Power supply configuration example
0b00	SW1 = ON, SW2 = OFF, SW3 = ON	The main power supply (V_{DD}) only is used.
0b01 (default)	SW1 = OFF, SW2 = OFF, SW3 = ON	Power supply backup configuration using a primary battery
0b10	SW1 = ON, SW2 = OFF, SW3 = OFF	The main power supply (V_{DD}) only is used.
0b11 (Setting prohibited)	–	Setting prohibited

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Bits 1–0: VDDSAMP[1:0]

These bits select a SW1 OFF period to be controlled for V_{DD} voltage detection.

Table 4.11 SW1 OFF Period Settings

PWSW_CFG.VDDSAMP[1:0]	SW1 OFF period
0b00	Not OFF (default)
0b01	2 ms
0b10	128 ms
0b11	256 ms

For more information, refer to "*Setting V_{DD} voltage drop detection sampling time*" in Section 3.9.

*1 For more information on the auto power switching function, refer to "*3.9 Auto Power Switching Function*."

0x38: WTICFG (Wakeup Timer Interrupt Configuration)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**FOEMUX**	**EVIN3MUX**	**–**	**WTONETIM**	**–**	**–**	**WTIOUT**	**–**
Initial value	0	0	0	0	0	0	0	0

Bit 7: FOEMUX

This bit selects the Pin 10 function.

1 (R/W): FOE (FOUT Enable) input
0 (R/W): EVIN2 input

For controlling the FOUT output with the FOE input, refer to "*Controlling FOUT Output (when using the FOE pin)*" in Section 3.7.

Bit 6: EVIN3MUX

This bit selects the Pin 4 function.

1 (R/W): EVIN3 input
0 (R/W): FOUT output

Bit 4: WTONETIM

This bit selects whether to automatically negate the /INT output or not after a wakeup timer interrupt occurs.

1 (R/W): Not negated automatically (low output)
0 (R/W): Negated automatically (7.812 ms width low pulse output)

Bit 1: WTIOUT

This bit selects the wakeup timer interrupt signal output pin.

1 (R/W): Output from the FOUT pin (CMOS buffer output)
0 (R/W): Output from the /INT pin (N-ch. open drain output)

When the FOUT pin is selected as the wakeup timer interrupt output pin, the wakeup timer interrupt signal is NORed with the FOUT signal before being output from the FOUT pin. Therefore, when using the FOUT pin only for the wakeup timer interrupt signal output, set the TCTL.FSEL[1:0] bits to 0b11 to disable the FOUT output.

This bit is effective when the EVIN3MUX bit = 0.

*1 For more information on the wakeup timer function, refer to "*3.6 Wakeup Timer Function*."

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0x39: WTCTL (Wakeup Timer Control)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**WTRST**	**–**	**–**	**–**	**WTMODSEL**	**WTSTOPCTL**	**–**	**WTSTOP**
Initial value	0	0	0	0	0	0	0	0
R/W	W	R	R	R	R/W	R/W	R	R/W

Bit 7: WTRST

This bit reloads the preset value to the wakeup timer.

1 (W): Timer is preset.
0 (W): Ineffective

Writing 1 to this bit outputs a reset pulse to the wakeup timer. During resetting, the TCTL.TE bit is set to 0. After the reset state is cancelled, the WTRST bit is cleared and the wakeup timer restarts with the preset value loaded. This makes it possible to use the wakeup timer as a watchdog timer.
This bit is always read as 0 even after writing 1.

Bit 3: WTMODSEL

This bit restricts the wakeup timer to operate either in Normal mode or Backup mode.

1 (R/W): The counter stops in Normal mode.
0 (R/W): The counter stops in Backup mode.

Bit 2: WTSTOPCTL

This bit enables/disables the WTMODSEL and WTSTOP bit functions.

1 (R/W): WTMODSEL is enabled and WTSTOP is disabled.
0 (R/W): WTMODSEL is disabled and WTSTOP is enabled.

Bit 0: WTSTOP

This bit temporarily stops the wakeup timer.

1 (R/W): The wakeup timer is temporarily stopped.
0 (R/W): The wakeup timer temporary stop state is cancelled (the wakeup timer is operating normally).

*1 For more information on the wakeup timer function, refer to "*3.6 Wakeup Timer Function*."

0x3A: WTCNT_L_MIR (Mirrored Wakeup Timer Counter Low, = 0x0A)
0x3B: WTCNT_M_MIR (Mirrored Wakeup Timer Counter Middle, = 0x0B)
0x3C: WTCNT_H_MIR (Mirrored Wakeup Timer Counter High, = 0x0C)

Mirrored Wakeup Timer Counter Low

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**WTCNT[7:0]**							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Mirrored Wakeup Timer Counter Middle

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**WTCNT[15:8]**							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

Mirrored Wakeup Timer Counter High

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**WTCNT[23:16]**							
Initial value	x	x	x	x	x	x	x	x
R/W	R/W							

These are mirror registers of Registers WTCNT_L, WTCNT_M, and WTCNT_H. For more information, refer to "*0x0A–0x0C: WTCNT_L/WTCNT_M/WTCNT_H (Wakeup Timer Counter Low/Middle/High)*."

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0x41: WRCMD_CFG (Command trigger Configuration)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**EVCNTCLREN**	**BUF3FCLREN**	**BUF2FCLREN**	**BUF1FCLREN**	**–**	**–**	**–**	**CMDTRGEN**
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R	R/W

Note: This register specifies the functions that will be executed when any data is written to Register WRCMD_TRG (Address 0x42).

Bit 7: EVCNTCLREN

This bit specifies whether to initialize the event counters or not when a command trigger is executed by writing to Register WRCMD_TRG.

1 (R/W): Event counter initialization is enabled.
0 (R/W): Event counter initialization is disabled.

Executing a command trigger with this bit set to 1 initializes all the event counters listed below that count the number of events input to EVIN1 to 3 (cleared to 0).

EVIN1_EVCNT.EVCNT[5:0] bits (EVIN1 event counter)
EVIN2_EVCNT.EVCNT[5:0] bits (EVIN2 event counter)
EVIN3_EVCNT.EVCNT[5:0] bits (EVIN3 event counter)

Bit 6: BUF3FCLREN
Bit 5: BUF2FCLREN
Bit 4: BUF1FCLREN

These bits specify whether to initialize the BUF*n* time stamp flags and event pointers when a command trigger is executed.

1 (R/W): Time stamp flag/event pointer initialization is enabled.
0 (R/W): Time stamp flag/event pointer initialization is disabled.

Executing a command trigger with these bits set to 1 initializes the BUF*n* flags/pointers shown below.

<BUF1FCLREN>
BUF1_STAT.FULLF bit (BUF1 full flag)
BUF1_STAT.EMPTF bit (BUF1 empty flag)
BUF1_STAT.PTR[5:0] bits (BUF1 event pointer)
BUF_OVWF.BUF1OVWF bit (BUF1 overwrite flag)

<BUF2FCLREN>
BUF2_STAT.FULLF bit (BUF2 full flag)
BUF2_STAT.EMPTF bit (BUF2 empty flag)
BUF2_STAT.PTR[3:0] bits (BUF2 event pointer)
BUF_OVWF.BUF2OVWF bit (BUF2 overwrite flag)

<BUF3FCLREN>
BUF3_STAT.FULLF bit (BUF3 full flag)
BUF3_STAT.EMPTF bit (BUF3 empty flag)
BUF3_STAT.PTR[3:0] bits (BUF3 event pointer)
BUF_OVWF.BUF3OVWF bit (BUF3 overwrite flag)

Bit 0: CMDTRGEN

This bit specifies whether to issue a time stamp trigger to BUF1 when a command trigger is executed.

1 (R/W): Issue of BUF1 time stamp trigger is enabled.
0 (R/W): Issue of BUF1 time stamp trigger is disabled.

Executing a command trigger with this bit set to 1 issues a time stamp trigger to BUF1. To issue this time stamp trigger successively, a 5 ms or more longer interval must be inserted between the triggers. Use the bits below to confirm whether the time stamp trigger is accepted normally or not:

BUF_INTF.BUF1F bit Check if this bit is set to 1.
or
BUF1_CFG2.RDPAGE[3:0] bit Check if the contents are incremented.

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0x42: WRCMD_TRG (Command trigger)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	WRTRG[7:0]							
Initial value	0	0	0	0	0	0	0	0
R/W	R/W							

Bits 7–0: WRTRG[7:0]

Writing any value to this address issues a command trigger configured in Register WRCMD_CFG at Address 0x41 (the command trigger is issued at the beginning of data written to the register).

After a command trigger has been issued, this register retains a value other than 0x00 until the command execution is completed, or data writing and flag settings are completed when a time stamp trigger is issued. Make sure the register has reverted to 0x00 by reading this register if the stamp data is read or a subsequent command trigger is issued immediately after a time stamp trigger is issued.

0x43: EVNT_INTE (Event Interrupt Enable)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**EVIN3IEN**	**EVIN2IEN**	**EVIN1IEN**	**–**	**VBATLIEN**	**VTMPLIEN**	**VDDLIEN**	**OSCSTPIEN**
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit 7: EVIN3IEN
Bit 6: EVIN2IEN
Bit 5: EVIN1IEN

These bits enable/disable the EVIN*n* event input to generate interrupts.

1 (R/W): EVIN*n* event input interrupts are enabled.
0 (R/W): EVIN*n* event input interrupts are disabled.

Bit 3: VBATLIEN

This bit enables/disables the V_{BAT} voltage drop detection function to issue event triggers.

1 (R/W): V_{BAT} voltage drop detection event trigger is enabled.
0 (R/W): V_{BAT} voltage drop detection event trigger is disabled.

If this bit has been set to 1, an event flag (EVNT_INTF.VBATLEVF bit) is set to 1 when a V_{BAT} voltage drop is detected.

Bit 2: VTMPLIEN

This bit enables/disables the V_{DET2} voltage drop detection function (to detect if the power supply voltage drops below the lower limit of temperature compensation operating voltage for the oscillator circuit) to issue event triggers.

1 (R/W): V_{DET2} voltage drop detection event trigger is enabled
0 (R/W): V_{DET2} voltage drop detection event trigger is disabled.

If this bit has been set to 1, an event flag (EVNT_INTF.VTMPLEVF bit) is set to 1 when a V_{DET2} voltage drop is detected.

Bit 1: VDDLIEN

This bit enables/disables the $-V_{DET1}$ voltage drop detection function (to detect if the V_{DD} voltage drops below $-V_{DET1}$) to issue event triggers.

1 (R/W): $-V_{DET1}$ voltage drop detection event trigger is enabled.
0 (R/W): $-V_{DET1}$ voltage drop detection event trigger is disabled.

If this bit has been set to 1, an event flag (EVNT_INTF.VDDLEVF bit) is set to 1 when a V_{DD} voltage drop is detected.

Bit 0: OSCSTPIEN

This bit enables/disables the oscillation stop detection function to issue event triggers.

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1 (R/W): Oscillation stop detection event trigger is enabled.
0 (R/W): Oscillation stop detection event trigger is disabled.

If this bit has been set to 1, an event flag (EVNT_INTF.OSCSTPEVF bit) is set to 1 when an oscillation stoppage is detected.

0x44: CAP_EN (Capture Enable)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	–	–	–	**VBATLCPEN**	**VTMPLCPEN**	**VDDLCPEN**	**OSCSTPCPEN**
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit 3: VBATLCPEN

This bit enables/disables the V_{BAT} voltage drop detection event trigger to capture time stamp data.

1 (R/W): V_{BAT} voltage drop detection time stamp capturing is enabled.
0 (R/W): V_{BAT} voltage drop detection time stamp capturing is disabled.

Bit 2: VTMPLCPEN

This bit enables/disables the V_{DET2} voltage drop detection (to detect if the power supply voltage drops below the lower limit of temperature compensation operating voltage for the oscillator circuit) event trigger to capture time stamp data.

1 (R/W): V_{DET2} voltage drop detection time stamp capturing is enabled.
0 (R/W): V_{DET2} voltage drop detection time stamp capturing is disabled.

Bit 1: VDDLCPEN

This bit enables/disables the $-V_{DET1}$ voltage drop detection (to detect if the V_{DD} voltage drops below $-V_{DET1}$) event trigger to capture time stamp data.

1 (R/W): $-V_{DET1}$ voltage drop detection time stamp capturing is enabled.
0 (R/W): $-V_{DET1}$ voltage drop detection time stamp capturing is disabled.

Bit 0: OSCSTPCPEN

This bit enables/disables the oscillation stop detection event trigger to capture time stamp data.

1 (R/W): Oscillation stop detection time stamp capturing is enabled.
0 (R/W): Oscillation stop detection time stamp capturing is disabled.

To actually execute time stamp capturing by each event trigger, it is necessary to set the ***IEN bit in Register EVNT_INTE corresponding to the event enabling the event flag (***EVF bit) in Register EVNT_INTF to be set.

0x46: BUF_INTF (Buffer Interrupt Factor)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**BUF3F**	**BUF2F**	**BUF1F**	–	**VBATLF**	–	**VDDLF**	–
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R/W	R	R/W	R

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Bit 7: BUF3F
Bit 6: BUF2F
Bit 5: BUF1F

These flags indicate that an event trigger input interrupt factor has occurred in the time stamp buffer BUF*n*.

1 (R): An event trigger input has occurred.
0 (R): No event trigger input has occurred.
1 (W): Ineffective
0 (W): Flag clear

Each flag is set to 1 when data of the number set using the BUF1_CFG1.INTCNT[5:0] bits (BUF1), BUF2_CFG1.INTCNT[3:0] bits (BUF2), or BUF3_CFG1.INTCNT[3:0] bits (BUF3) are written to the buffer.

Bit 3: VBATLF

This flag is set when a V_{BAT} voltage drop status is detected twice successively.

1 (R): A V_{BAT} voltage drop has been detected.
0 (R): No V_{BAT} voltage drop has been detected.
1 (W): Ineffective
0 (W): Flag clear (Takes effect after the V_{BAT} voltage is restored.)

If a V_{BAT} voltage drop status is being continued, this flag cannot be cleared by writing 0.

Bit 1: VDDLF

This flag is set once a $-V_{DET1}$ voltage drop status (the V_{DD} voltage drops below $-V_{DET1}$) is detected.

1 (R): A $-V_{DET1}$ voltage drop has been detected.
0 (R): No $-V_{DET1}$ voltage drop has been detected.
1 (W): Ineffective
0 (W): Flag clear (Takes effect after the V_{DD} voltage is restored.)

If a $-V_{DET1}$ voltage drop status is being continued, this flag cannot be cleared by writing 0.

0x47: EVNT_INTF (Event Interrupt Factor)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**EVIN3F**	**EVIN2F**	**EVIN1F**	**–**	**VBATLEVF**	**VTMPLEVF**	**VDDLEVF**	**OSCSTPEVF**
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit 7: EVIN3F
Bit 6: EVIN2F
Bit 5: EVIN1F

These flags indicate that an event input has occurred to EVIN*n*.

1 (R): An EVIN*n* event input has occurred.
0 (R): No EVIN*n* event input has occurred.
1 (W): Ineffective
0 (W): Flag clear

Bit 3: VBATLEVF

This flag indicates that a V_{BAT} voltage drop detection event has occurred.

1 (R): A V_{BAT} voltage drop detection event has occurred
0 (R): No V_{BAT} voltage drop detection event has occurred
1 (W): Ineffective
0 (W): Flag clear

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Bit 2: VTMPLEVF

This flag indicates that a V_{DET2} voltage drop detection event (the power supply voltage drops below the lower limit of temperature compensation operating voltage for the oscillator circuit) has occurred.

1 (R): A V_{DET2} voltage drop detection event has occurred
0 (R): No V_{DET2} voltage drop detection event has occurred
1 (W): Ineffective
0 (W): Flag clear

Bit 1: VDDLEVF

This flag indicates that a $-V_{DET1}$ voltage drop detection event (the V_{DD} voltage drops below $-V_{DET1}$) has occurred.

1 (R): A $-V_{DET1}$ voltage drop detection event has occurred
0 (R): No $-V_{DET1}$ voltage drop detection event has occurred
1 (W): Ineffective
0 (W): Flag clear

Bit 0: OSCSTPEVF

This flag indicates that an oscillation stop detection event has occurred.

1 (R): An oscillation stop detection event has occurred
0 (R): No oscillation stop detection event has occurred
1 (W): Ineffective
0 (W): Flag clear

When an oscillation stop detection event has occurred, time stamp data will be captured after the oscillation restarts.

Note: The flags in this register are not set even if an event has occurred when the corresponding ****IEN bit in Register EVNT_INTE has been set to 0.

0x4E: BUF_FULLF (Buffer Full Flag)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	**BUF3FULLF**	**BUF2FULLF**	**BUF1FULLF**	**–**	**–**	**–**	–
Initial value	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R	R	R	R

Bit 6: BUF3FULLF
Bit 5: BUF2FULLF
Bit 4: BUF1FULLF

These flags indicate that a buffer full has occurred in BUF*n*.

1 (R): Buffer full state has occurred.
0 (R): No buffer full state has occurred.
1 (W): Ineffective
0 (W): Flag clear

In FIFO mode, the BUF1FULLF bit is used to indicate the FIFO buffer status.
These flags do not automatically revert to 0 even if a free space is made in the buffer by reading data. Therefore, the flag that has been set to 1 should be cleared by writing 0.

0x4F: BUF_OVWF (Buffer Overwrite Flag)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	–	**BUF3OVWF**	**BUF2OVWF**	**BUF1OVWF**	**–**	**–**	**–**	**–**
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

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Bit 6: BUF3OVWF
Bit 5: BUF2OVWF
Bit 4: BUF1OVWF

These flags indicate that an overwrite has occurred in BUF*n*.

1 (R): An overwrite has occurred.
0 (R): No overwrite has occurred.

Each flag is cleared individually by issuing a command trigger (writing to Register WRCMD_TRG) with the BUF*n*FCLREN bit in Register WRCMD_CFG set to 1.

0x51: EVIN1_EVCNT (EVIN1 Event Counter)
0x52: EVIN2_EVCNT (EVIN2 Event Counter)
0x53: EVIN3_EVCNT (EVIN3 Event Counter)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**–**	**–**	**EVCNT[5:0]**					
Initial value	0	0	0	0	0	0	0	0
R/W	R	R	R					

Bits 5–0: EVCNT[5:0]

These bits indicate the event count (0 to 63 times) input to the EVIN*n* pin.

If the input count exceeds 63 times, the counter reverts to 0 and continues counting. The EVIN*n* event counter does not operate when the EVIN_EN.EVIN*n*EN bit = 0.

0x54: EVINMON (EVIN Monitor)

Bit No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	**EVIN3MON**	**EVIN2MON**	**EVIN1MON**	**–**	**–**	**–**	**–**	**–**
Initial value	x	x	x	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit 7: EVIN3MON
Bit 6: EVIN2MON
Bit 5: EVIN1MON

These bits indicate the current input level on the EVIN*n* pin.

1 (R): High level
0 (R): Low level

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5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rated value	Unit
Main power supply voltage	V_{DD}	–	-0.3 to +6.5	V
Internal operating voltage	V_{OUT}	–	-0.3 to +6.5	V
Backup power supply voltage	V_{BAT}	–	-0.3 to +6.5	V
Input voltage 1	V_{IN1}	SCL, SDA, FOE, CE, CLK, DIO, DI, EVIN1, EVIN2, EVIN3	-0.3 to +6.5	V
Output voltage 1	V_{OUT1}	/INT, SDA, DIO, DO, FOUT	-0.3 to +6.5	V
Storage temperature	T_{STG}	When stored separately, without packaging	-55 to +125	°C

(Notes)
- All the voltages are based on GND = 0 V.
- Operating or placing the device under the condition exceeding the above absolute maximum ratings may cause permanent damage to the device. In normal operation, the device is desired to be used within the recommended operating condition ranges, otherwise, it may cause a malfunction or may adversely affect reliability.
- Voltages must always satisfy the condition of $V_{DD} \geq V_{SS}$.
- Device operations are guaranteed within the ranges of the electrical characteristics.

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

Unless otherwise specified: GND = 0 V, Ta = -40 °C to +105 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating power voltage *1	V_{DD}	When operating with the main power supply	1.60	3.0	5.5	V
Interface power voltage	V_{ACC}	V_{DD} pin voltage (I^2C-Bus IF, SPI IF 3-wire/4-wire)	1.60	3.0	5.5	V
Backup power voltage	V_{BAT}	Backup power supply voltage	1.10	3.0	5.5	V
Temperature compensation voltage	VT_{MP}	V_{OUT} power voltage that can keep temperature compensation operation	1.60 *2	3.0	5.5	V
Time keeping voltage	V_{CLK}	V_{OUT} power voltage that can keep clocking operation	V_{VLF} *3	3.0	5.5	V
Operating temperature	Ta	No condensation	-40	+25	+105	°C

*1 A bypass capacitor for noise suppression must be connected as close to the power supply pin as possible.

*2 When the V_{OUT} power voltage is less than the Min. value of the temperature compensation voltage, the temperature-dependent frequency correction value update function is stopped.

*3 V_{VLF} is the minimum time keeping voltage value after a power-on-reset in $V_{DD} \geq V_{ACC(Min.)}$.

5.3 Frequency Characteristics

Table 5.3 Frequency Characteristics

Unless otherwise specified: V_{DD} = 3.0 V, GND = 0 V, Ta = -40 °C to +105 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output frequency	fo	Ta = +25 °C			32.768		kHz
Frequency tolerance	Δf/f	XS	Ta = 0 °C to +50 °C	–	–	±1.9 *1	×10^{-6}
			Ta = -40 °C to +85 °C	–	–	±3.0 *2	
			Ta = +85 °C to +105 °C	–	–	±5.0 *3	
		XB	Ta = 0 °C to +50 °C	–	–	±3.8 *4	
			Ta = -40 °C to +85 °C	–	–	±5.0 *3	
			Ta = +85 °C to +105 °C	–	–	±8.0 *5	
Frequency-voltage characteristics	f/V	Ta = +25 °C, V_{DD} = 1.6 V to 5.5 V		–	–	±1	×10^{-6}/V
FOUT duty	Duty	Vth = 50% V_{DD}, Ta = -40 °C to +105 °C, V_{DD} = 1.6 V to 5.5 V		40	–	60	%
Crystal oscillation start-up time	t_{STA}	Ta = +25 °C, V_{DD} = 1.6 V to 5.5 V		–	0.5	1.0	s
		Ta = -40 °C to +105 °C, V_{DD} = 1.6 V to 5.5 V		–	–	3.0	
Aging	fa	Ta = +25 °C, power supply voltage = 3.0 V, first year		–	–	±3	×10^{-6}/year
Reflow	Δfref	Reflow process: 260°C Max., twice		–		±3 *6	10^{-6}

∗1 Monthly rate: ±5 seconds ∗2 Monthly rate: ±8 seconds ∗3 Monthly rate: ±13.2 seconds ∗ 4 Monthly rate: ±10 seconds

∗5 Monthly rate: ±21 seconds

∗6 Frequency change rate before and after being mounted by reflow soldering that was measured under a room temperature environment after being left for 24 hours

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5.4 DC Characteristics

DC Characteristics

Table 5.4 DC Characteristics

Unless otherwise specified: V_{BAT} = 1.1 V to 5.5 V, V_{DD} = 1.6 V to 5.5 V, Ta = -40 °C to +105 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	/INT = Hi-Z FOUT: Output OFF (Hi-Z) Temperature compensation interval: 2 s FSEL1, FSEL0 = 1 INIEN = 1, CHGEN = 0 SCL, SDA = H, CE = L	V_{DD} = 5 V	–	0.42	1.8	µA
Current consumption 2	I_{DD2}		V_{DD} = 3 V	–	0.40	1.70	
Current consumption 3	I_{32K1}	/INT = Hi-Z FOUT: 32 kHz output, C_L = 0 pF Temperature compensation interval: 2 s FSEL1, FSEL0 = 0 INIEN = 1, CHGEN = 0 SCL, SDA = H, CE = L	V_{DD} = 5 V	–	1.10	3.10	µA
Current consumption 4	I_{32K2}		V_{DD} = 3 V	–	1.00	3.00	
Current consumption 5	I_{BAT1}	/INT= Hi-Z FOUT: Output OFF (Hi-Z) Temperature compensation interval: 2 s FSEL1, FSEL0 = 1 INIEN = 1, CHGEN = 0 SCL, SDA = L, CE = L	V_{BAT} = 5 V	–	0.30	1.60	µA
Current consumption 6	I_{BAT2}		V_{BAT} = 3 V	–	0.24	1.50	
Current consumption 7	I_{BAT3}	Current value when V_{BAT} only is applied at initial power on /INT = Hi-Z FOUT: Output OFF (Hi-Z) Temperature compensation interval: Inactive	V_{BAT} = 3 V	–	0.23	1.50	µA
Current consumption 8	I_{DD3}	/INT = Hi-Z FOUT: Output OFF (Hi-Z) Temperature compensation interval: Inactive FSEL1, FSEL0 = 1, INIEN = 1, CHGEN = 0 SCL, SDA = H, CE = L	V_{DD} = 5 V	–	0.40	1.70	µA
Current consumption 9	I_{DD4}		V_{DD} = 3 V	–	0.38	1.60	
Current consumption 10	I_{DD5}	/INT = Hi-Z FOUT: Output OFF (Hi-Z) Temperature compensation peak current. See *Figure 5.1* FSEL1, FSEL0 = 1, INIEN = 1, CHGEN = 0 SCL, SDA = H, CE = L	V_{DD} = 5 V	–	55	100	µA
Current consumption 11	I_{DD6}		V_{DD} = 3 V	–	50	95	
V_{DD} rise detection voltage	$+V_{DET1}$	Voltage to switch from V_{BAT} to V_{DD}		1.40	1.50	1.60	V
V_{DD} drop detection voltage	$-V_{DET1}$	Voltage to switch from V_{DD} to V_{BAT}		1.35	1.45	1.55	V
Temperature compensation update stop detection voltage	V_{DET2}	Detection power system: V_{OUT}		1.45	1.50	1.55	V
V_{BAT} rise detection voltage	$+V_{LOW}$	V_{BAT} pin voltage		1.15	1.25	1.35	V
V_{BAT} drop detection voltage	$-V_{LOW}$	V_{BAT} pin voltage		1.10	1.20	1.30	V
VLF detection voltage	V_{VLF}	V_{OUT} power drop detection voltage		–	–	1.1	V
“H” input voltage	V_{IH}	SCL, SDA, CE, CLK, DIO, DI, FOE		0.8 x V_{DD}	–	5.5	V
		EVIN*n*		0.8 x V_{OUT}	–	5.5	
“L” input voltage	V_{IL}	SCL, SDA, CE, CLK, DIO, DI, FOE		GND - 0.3	–	0.2 x V_{DD}	V
		EVIN*n*		GND - 0.3	–	0.2 x V_{OUT}	
“H” output voltage	V_{OH1}	DIO, DO, FOUT	V_{DD} = 5.0 V, I_{OH} = -1 mA	4.5	–	5.0	V
	V_{OH2}		V_{DD} = 3.0 V, I_{OH} = -1 mA	2.2	–	3.0	
	V_{OH3}		V_{DD} = 3.0 V, I_{OH} = -100 µA	2.9	–	3.0	
“L” output voltage	V_{OL1}	FOUT	V_{DD} = 5.0 V, I_{OL} = 1 mA	GND	–	GND + 0.5	V
	V_{OL2}		V_{DD} = 3.0 V, I_{OL} = 1 mA	GND	–	GND + 0.8	
	V_{OL3}		V_{DD} = 3.0 V, I_{OL} = 100 µA	GND	–	GND + 0.1	
	V_{OL4}	DIO, DO, /INT	V_{DD} = 5.0 V, I_{OL} = 1 mA	GND	–	GND + 0.25	V
	V_{OL5}		V_{DD} = 3.0 V, I_{OL} = 1 mA	GND	–	GND + 0.4	
	V_{OL6}	SDA	$V_{DD} \geq$ 2.0 V, I_{OL} = 3 mA	GND	–	GND + 0.4	V
Input leakage current	I_{LK}	Input pin, input voltage = V_{DD} or GND		-0.5	–	0.5	µA
	IL_{KPD}	EVIN pin, input voltage = GND		-0.5	–	0.5	
Output leakage current	I_{OZ}	Output pin, output voltage = V_{DD} or GND		-0.5	–	0.5	µA

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Item	Symbol	Condition	Min.	Typ.	Max.	Unit
EVIN*n* input pull-up resistance	R_{UP1}	EVIN1/EVIN2/EVIN3 pin, V_{DD} = 3 V, 500 kΩ setting	100	500	2000	kΩ
	R_{UP2}	EVIN1/EVIN2/EVIN3 pin, V_{DD} = 3 V, 1 MΩ setting	0.2	1.0	4.0	MΩ
	R_{UP3}	EVIN1/EVIN2/EVIN3 pin, V_{DD} = 3 V, 10 MΩ setting	2.0	10.0	40.0	MΩ
EVIN*n* input pull-down resistance	R_{DWN3}	EVIN1/EVIN2/EVIN3 pin, V_{DD} = 3 V, 500 kΩ setting	100	500	2000	kΩ
CE input pull-down resistance	R_{DWN1}	CE pin, V_{DD} = 5 V	75	150	300	kΩ
	R_{DWN2}	CE pin, V_{DD} = 3 V	150	300	600	kΩ
Off-leak current from V_{DD} to V_{OUT}	I_{SW1}	V_{OUT} = 5.0 V, V_{DD} = 0.0 V	–	–	50	nA
Off-leak current from V_{BAT} to V_{OUT}	I_{SW2}	V_{BAT} = 0.0 V, V_{OUT} = 5.0 V	–	–	50	nA
Off-leak current from V_{BAT} to V_{DD}	I_{SW23}	V_{BAT} = 5.5 V, V_{OUT} = 3.3 V	–	–	150	nA
SW ON current between V_{DD} and V_{OUT}	I_{SWON1}	Internal SW between V_{DD} and V_{OUT} = ON ΔV = +0.1 V, V_{OUT} = 5.5 V, V_{DD} = 5.4 V ΔV = +0.1 V, V_{OUT} = 3.0 V, V_{DD} = 2.9 V R_{SWON1} = 20 Ω to 100 Ω	1	–	5	mA
SW ON current between V_{BAT} and V_{OUT}	I_{SWON2}	Internal SW between V_{BAT} and V_{OUT} = ON ΔV = +0.1 V, V_{OUT} = 5.5 V, V_{BAT} = 5.4 V ΔV = +0.1 V, V_{OUT} = 3.0 V, V_{BAT} = 2.9 V R_{SWON1} = 33 Ω to 200 Ω	500	–	3000	μA

Temperature Compensation Operation and Current Consumption

This IC activates the temperature sensor in the temperature compensation intervals to update the temperature compensation value, therefore, current consumption increases during this operation period. I_{DD1} or I_{DD2} is average current consumption when the temperature sensor measurement operation execution interval is set to 2 seconds.

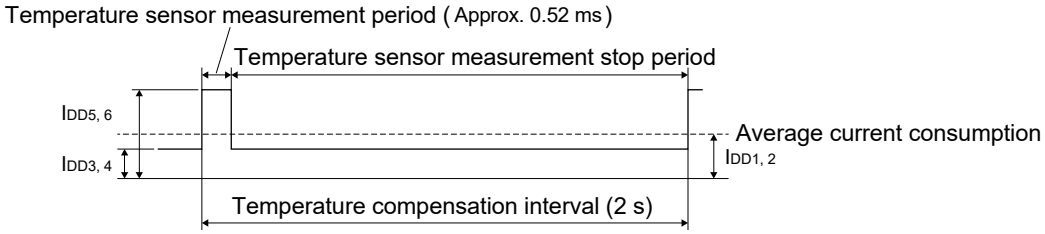


Figure 5.1 Temperature Compensation Operation and Current Consumption

Power Switching Element Characteristics (for reference)

Table 5.5 Power Switching Element Characteristics (for reference)

Item	Characteristics for reference	Condition
Pch-Switch rated current	40 mA Max.	SW1 = SW2 = SW3 = ON, +25°C
Diode forward voltage V_F	0.60 V / 1 mA Typ. 0.85 V / 10 mA Typ.	V_{DD} = 3.0 V, +25 °C
Diode reverse current I_R	5 nA Max.	V_R = 5.5 V, -40 °C to +105 °C

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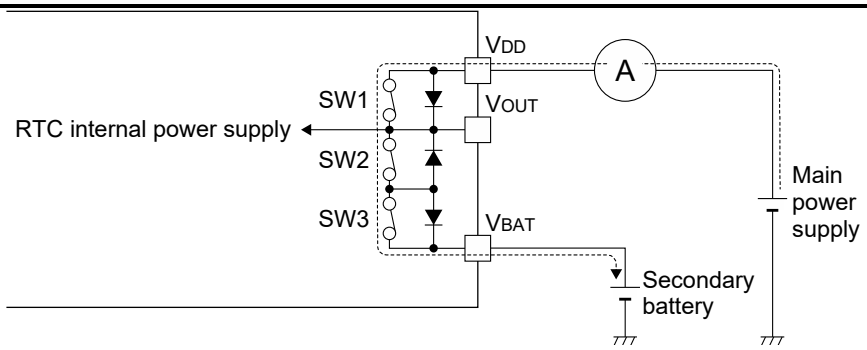


Figure 5.2 Charge Path for Secondary Battery

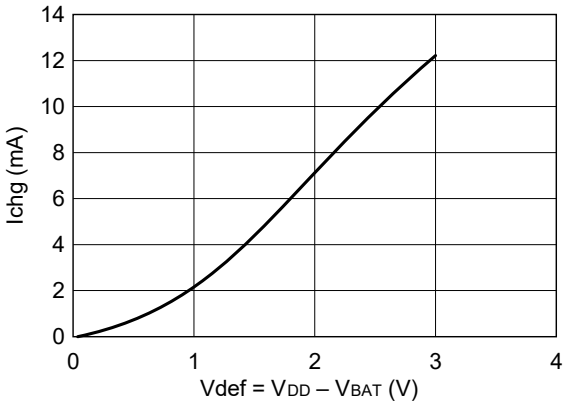


Figure 5.3 V_{BAT} Charging Characteristic (V_{DD} = 3.0 V)

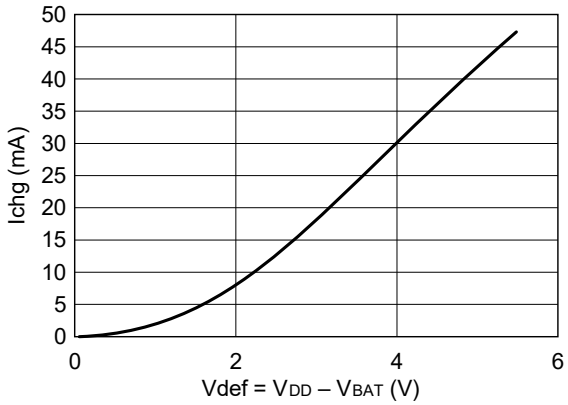


Figure 5.4 V_{BAT} Charging Characteristic (V_{DD} = 5.5 V)

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5.5 AC Characteristics

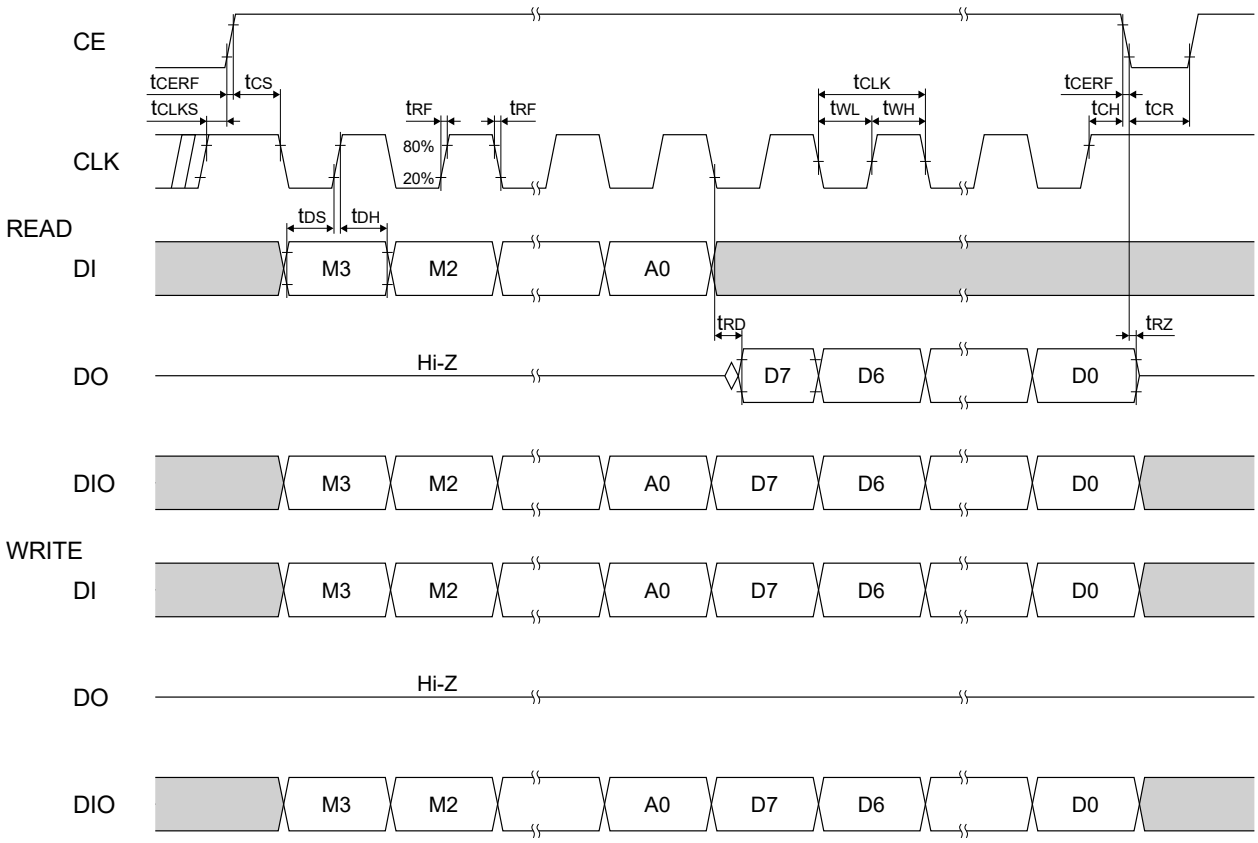
RX4901CE AC Characteristics

Table 5.6 RX4901CE AC Characteristics

Unless otherwise specified: GND = 0 V , V_{DD} = 1.6 V to 5.5 V, Ta = -40 °C to +105 °C

Item	Symbol	Condition	V_{DD} = 1.8 V ± 0.2 V		V_{DD} = 3.0 V ± 10 %		V_{DD} = 5.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
CLK clock cycle	t_{CLK}		500	–	332	–	250	–	ns
CLK “H” pulse width	t_{WH}		250	–	166	–	125	–	ns
CLK “L” pulse width	t_{WL}		250	–	166	–	125	–	ns
CLK rise/ fall time	t_{RF}		–	100	–	50	–	40	ns
CLK setup time	t_{CLKS}		50	–	30	–	30	–	ns
CE setup time	t_{CS}		200	–	150	–	130	–	ns
CE hold time	t_{CH}		200	–	150	–	130	–	ns
CE recovery time	t_{CR}		300	–	200	–	150	–	ns
CE rise/ fall time	t_{CERF}		–	100	–	50	–	40	ns
Write data setup time	t_{DS}		100	–	50	–	40	–	ns
Write data hold time	t_{DH}		100	–	50	–	40	–	ns
Read data delay time	t_{RD}	C_L = 50 pF	–	200	–	150	–	150	ns
DO (DIO) output disable time	t_{RZ}	C_L = 50 pF, R_L = 10 kΩ	–	200	–	120	–	110	ns

∗1 When V_{DD} = 2.0 V to 2.7 V, the V_{DD} = 1.8 V ± 0.2 V specifications should be applied. When V_{DD} = 3.3 V to 4.5 V, the V_{DD} = 3.0 V ± 10% specifications should be applied.



∗ Do not place the CLK and DI or DIO pins into a floating state during Normal mode.

Figure 5.5 RX4901CE AC Characteristics (SPI Timing Chart)

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RX8901CE AC Characteristics

Table 5.7 RX8901CE AC Characteristics

Unless otherwise specified: GND = 0 V , V_{DD} = 1.6 V to 5.5 V, Ta = -40 °C to +105 °C

Item	Symbol	100 kHz access (Standard mode)		400 kHz access (Fast mode)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	–	100	–	400	kHz
START condition setup time	$t_{SU;STA}$	4.7	–	0.6	–	µs
START condition hold time	$t_{HD;STA}$	4.0	–	0.6	–	µs
Data setup time	$t_{SU;DAT}$	250	–	100	–	ns
Data hold time	$t_{HD;DAT}$	0	–	0	–	ns
STOP condition setup time	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between STOP and START conditions	t_{BUF}	4.7	–	1.3	–	µs
SCL “L” width	t_{LOW}	4.7	–	1.3	–	µs
SCL “H” width	t_{HIGH}	4.0	–	0.6	–	µs
SCL, SDA rise time	tr	–	1.0	–	0.3	µs
SCL, SDA fall time	tf	–	0.3	–	0.3	µs
Allowable spike time on bus	t_{SP}	–	50	–	50	ns

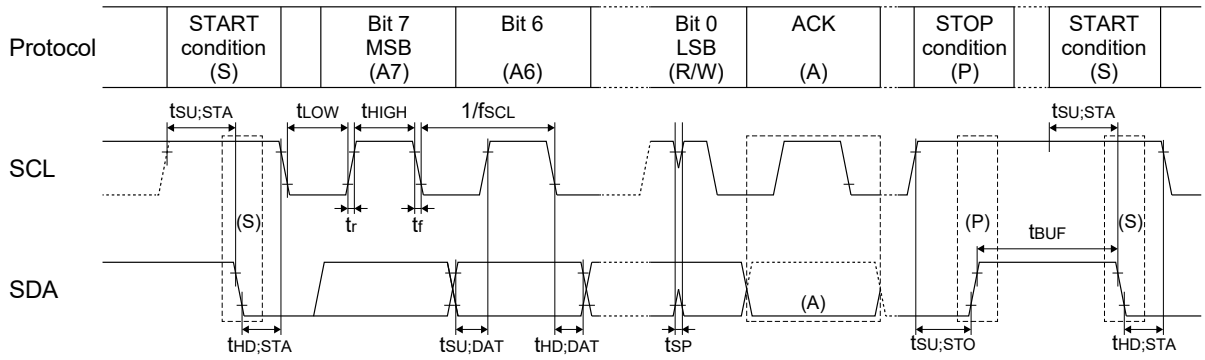


Figure 5.6 RX8901CE AC Characteristics (I^2C-Bus Timing Chart)

∗1 The I^2C-Bus interface of the RX4901CE/RX8901CE is reset and SDA is set into Hi-Z in two counts of the internal 1 Hz clock after the slave address is received. Therefore, an I^2C-Bus communication from sending the slave address to generating STOP condition must be completed in one second.

∗2 The RX4901CE/RX8901CE loads the 8-bit write data sent from the host at the SCL rising edge while responding with an ACK after all the 8 bits have been received. If the communication is disconnected before loading 8-bit data, the data, which has unreceived bits, is not written to the RX4901CE/RX8901CE register.

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5.6 Power-On Characteristics

Table 5.8 Power-On Characteristics

Unless otherwise specified: GND = 0 V , V_{DD} = 1.3 V to 5.5 V, Ta = -40 °C to +105 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power supply initial rise time*1	t_{R1}	Voltage slope (voltage variation rate) while the V_{OUT} voltage rising from GND after power is supplied to V_{DD} or V_{BAT}	3 V	0.1	–	10	ms/V
			5 V	0.5	–	10	ms/V
Access waiting time after power on	t_{CL}	Time after V_{DD} reaches $V_{ACC\ (Min.)}$ until accessing can be started		40	–	–	ms
Access end hold time before power off	t_{CD}	The waiting time until the V_{DD} voltage starts dropping in the t_F voltage slope after the end of access		0	–	–	ms
Power supply fall time	t_F	Voltage slope (voltage variation rate) while the V_{DD} voltage is dropping		1	–	–	ms/V
Power supply restoration rise time	t_{R2}	Voltage slope (voltage variation rate) while the V_{DD} voltage is rising after re-turning power on or rerising		0.1	–	–	ms/V
Access waiting time after power restored	t_{CU}	Time after V_{DD} reaches $V_{ACC\ (Min.)}$ until accessing can be started when power is restored		40	–	–	ms

*1 Power-on reset starts with either V_{DD} or V_{BAT} supplied in advance. To execute power-on reset with certainly at the initial power on, the power supply rise time condition must be satisfied and the power voltage must be supplied from the GND level.
To ensure that power-on reset takes effect, maintain the V_{DD} = GND condition for at least 100 ms after power-off.

*2 At the initial power on, the V_{DD} voltage must be risen to at least the $+V_{DET1}$ level.

*3 The backup period in the figure below is assumed to be a long enough time (60 seconds or more) and it is not caused by noise on the power supply voltage.

*4 A maximum of 31.25 ms delay occurs until the power supply is switched after V_{DD} reaches $+V_{DET1}$, as the V_{DD} voltage detection is performed intermittently in 31.25 ms intervals during Backup mode.

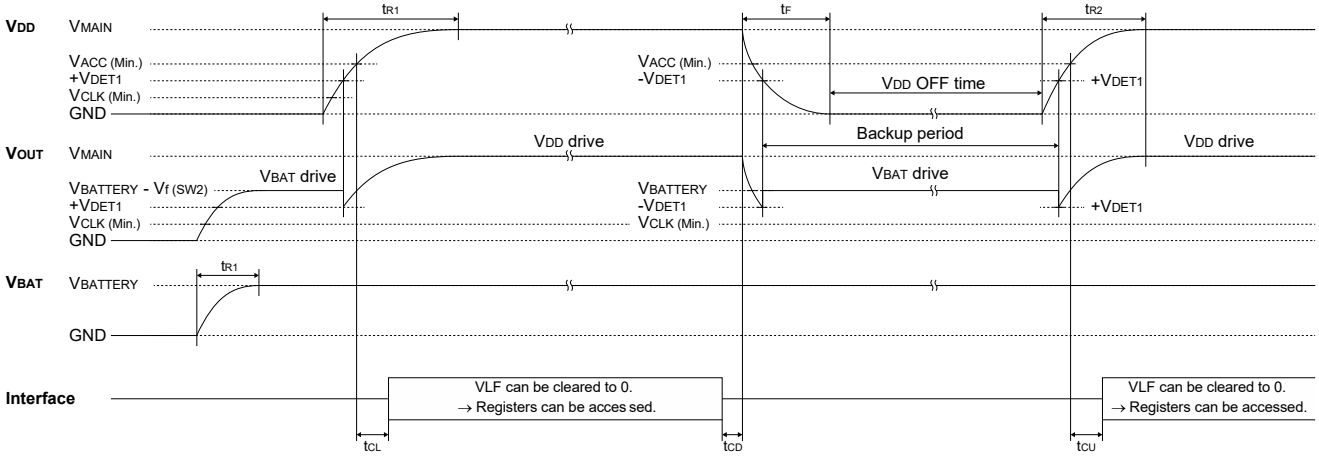


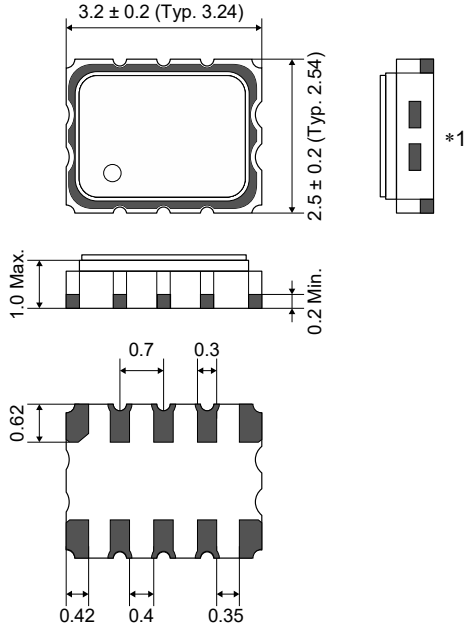
Figure 5.7 Power-On Sequence

Jump to Top / Bottom
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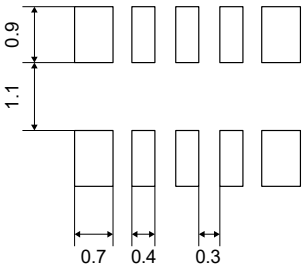
6 Package

6.1 Package Dimensions

• External dimensions



• Recommended soldering pattern

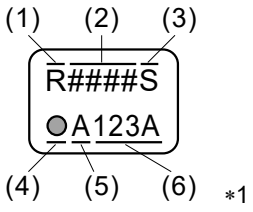


Unit: mm

*1 The metal pads on the short side of the 1st and 10th pins of the package are inspection pads for the crystal unit. For stable oscillation, make sure that leakage current due to condensation or dust does not occur between these pads.
The metal pads on the short side of the 5-pin and 6-pin sides are not connected inside the RTC.

Figure 6.1 Package Dimensions

6.2 Marking Layout



(1) Logo	R	→ RX
(2) Type	4901	→ RX4901CE
	8901	→ RX8901CE
(3) Frequency tolerance	S	→ XS
	B	→ XB
(4) Pin 1 mark		
(5) Product option	ex.) A	→ Option A
(6) Production lot number		

*1 Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

Figure 6.2 Marking Layout

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7 Notes on Mounting

This module includes a crystal oscillator. Do not apply excessive shock and vibration. Further, the module is fabricated with a C-MOS process employed to realize low power consumption. It is necessary to take a measure against static electricity when performing mounting work.

Static Electricity

Although this module includes an electrostatic breakdown protection circuit, the internal circuits may be damaged due to a large discharge of static electricity. Electrically conductive containers should be used for packing and transport.
In addition, use a soldering iron and measurement equipment without high voltage leakage, and take a measure against static electricity in mounting and other works.

Noise

If a signal with excessive external noise is applied to the power supply or input pins, the internal circuits may be damaged due to latch up or other malfunctions. In order to ensure stable operation, connect a 0.1 µF or larger ceramic capacitor as close to the power supply pins of this module as possible. Also, avoid placing any device that generates a large noise near this module.

Input Voltage

When a voltage out of the allowable range is constantly applied to an input pin, shoot-through current flows. This causes current consumption to increase or latch up to occur, and the internal circuits may be damaged. Apply a voltage of V_{IL} Max. or lower and V_{IH} Min. or higher to the input pin according to the input voltage specifications.

Handling of Unused Pins

Leaving input pins open causes current consumption to increase and quality deterioration. Fix the input level of unused pins with the internal pull-up and pull-down resistor disabled at either V_{DD} or GND.

Soldering Temperature

If the temperature in the package exceeds +260 °C at soldering, the characteristics of the crystal resonator will be degraded or the internal circuits may be damaged. Check the mounting temperature and time before mounting this device following the solder heat resistance evaluation profile provided by Seiko Epson.

Mounting Equipment

When using general-purpose mounting equipment, check the equipment and its operating conditions, as there is a possibility that the internal crystal resonator will be damaged by a shock at mounting depending on the conditions. If the mounting conditions are later changed, the same check should be performed again. In addition, take a measure against static electricity when performing mounting work.

Ultrasonic Cleaning

Depending on the usage conditions, there is a possibility that the crystal resonator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

Mounting Orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

Leakage between Pins

Current leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

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8 Sample Connection Diagram

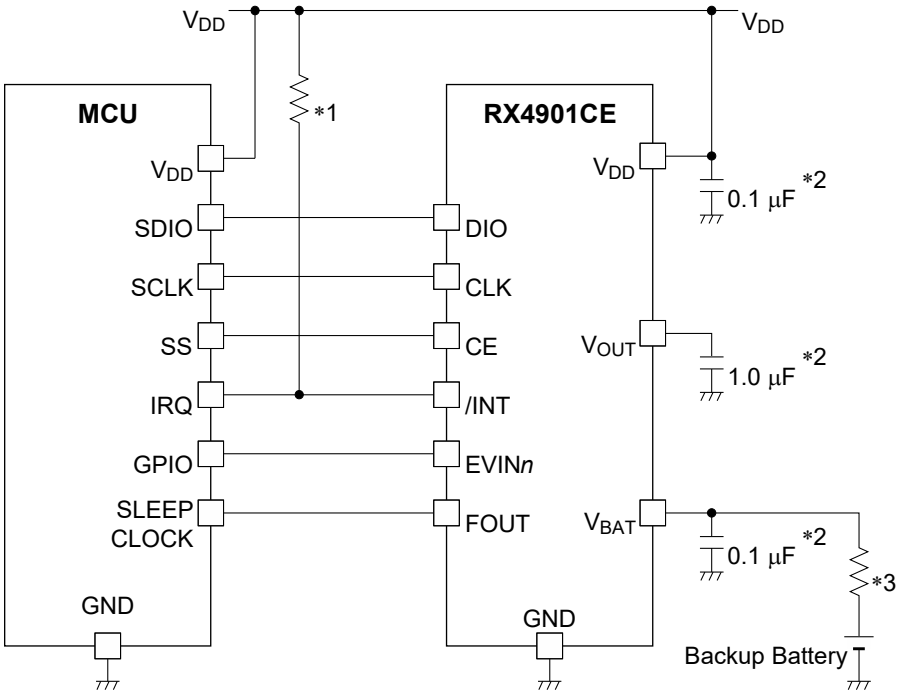


Figure 8.1 Sample Connection Diagram with a Typical MCU (RX4901CE Option A/B)

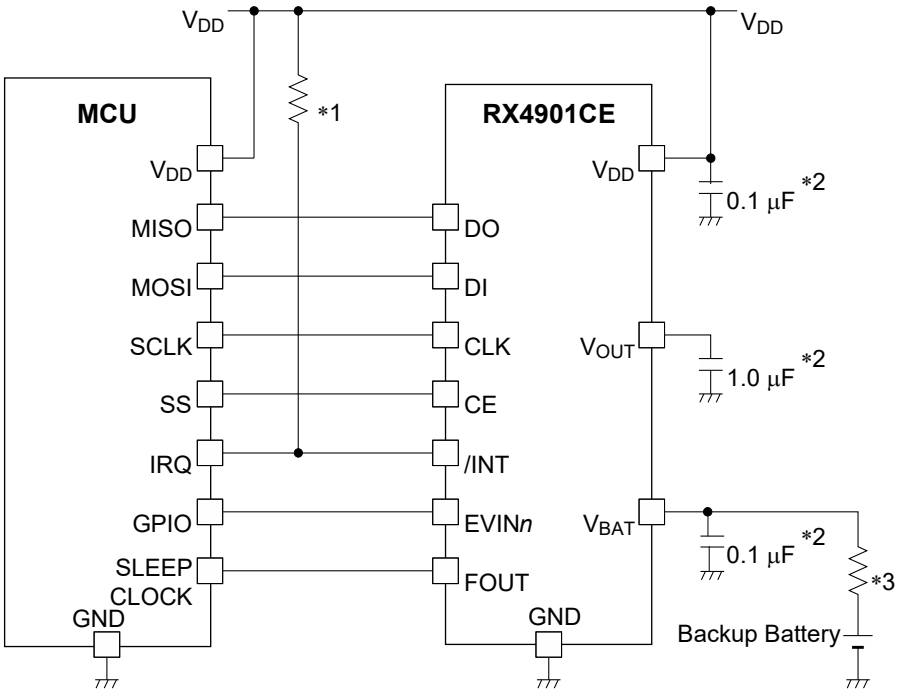


Figure 8.2 Sample Connection Diagram with a Typical MCU (RX4901CE Option C/D)

*1 A pull-up resistor of 1 kΩ to 10 kΩ is recommended for the /INT pin.
*2 Place each bypass capacitor close to the RX4901 pin nearest.
*3 When inserting this resistor to protect the battery, set a resistance value that can supply a current of at least 100µA.
See page 93 DC characteristics current consumption 10 (IDD5) and current consumption 11 (IDD6).
When conforming to the recommended current value of the battery manufacturer and the specifications of the UL standard, etc., please set a resistor that prioritizes them.
Even if it has a current supply capacity of 100µA or more, the RTC will not consume more current than specified.

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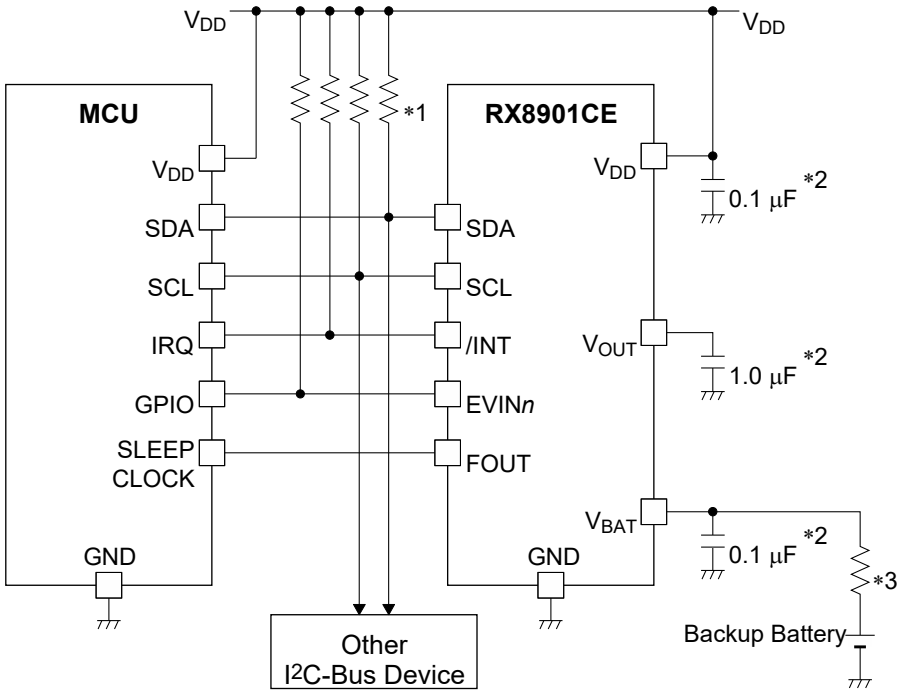


Figure 8.3 Sample Connection Diagram with a Typical MCU (RX8901CE)

*1 Each of pull-up resistors of 1 kΩ to 10 kΩ is recommended.:
Please check with an oscilloscope that the SDA and SCL signals conform to the AC timing characteristics.
*2 Place each bypass capacitor close to the RX8901 pin nearest.
*3 When inserting this resistor to protect the battery, set a resistance value that can supply a current of at least 100µA.
See page 93 DC characteristics current consumption 10 (IDD5) and current consumption 11 (IDD6).
When conforming to the recommended current value of the battery manufacturer and the specifications of the UL standard, etc., please set a resistor that prioritizes them.
Even if it has a current supply capacity of 100µA or more, the RTC will not consume more current than specified.

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