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Application Manual

Real Time Clock Module

RX-8731LC

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ETM23E Revision History

Rev No.	Date	Page	Description
-01	26.Jan.2015		Release
-02	7.Mar.2013		Input voltage correction
-03	15.Jul.2014	6,34	Bus out function description modification
-04	24.Feb.2015	7,33	Add 8.4 and 8.5 11-1)(4) modification

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I²C-BUS / Low Power / Ultra Small RTC with E²PROM and Unique ID-ROM

RX – 8731 LC

- Built in frequency adjusted 32.768 kHz crystal unit.
- Built in 80 bit E²PROM and 48 bit ID-ROM.
- 4 Programmable I/O ports.
- Compliant with I²C high-speed bus specifications (400 kHz).
- Equipped with alarm, timer, and frequency output (32.768kHz, 1024 Hz, 1 Hz) features.
- Low backup current : 0.35 µA / 3 $V_{Typ.}$
- Wide operating voltage range : 1.7 V to 5.5 V
- Wide timekeeper voltage range : 1.3 V to 5.5 V
- Ultra Small package. (VSOJ - 12 pin)

The I²C-BUS is a trademark of NXP Semiconductors.

1. Overview

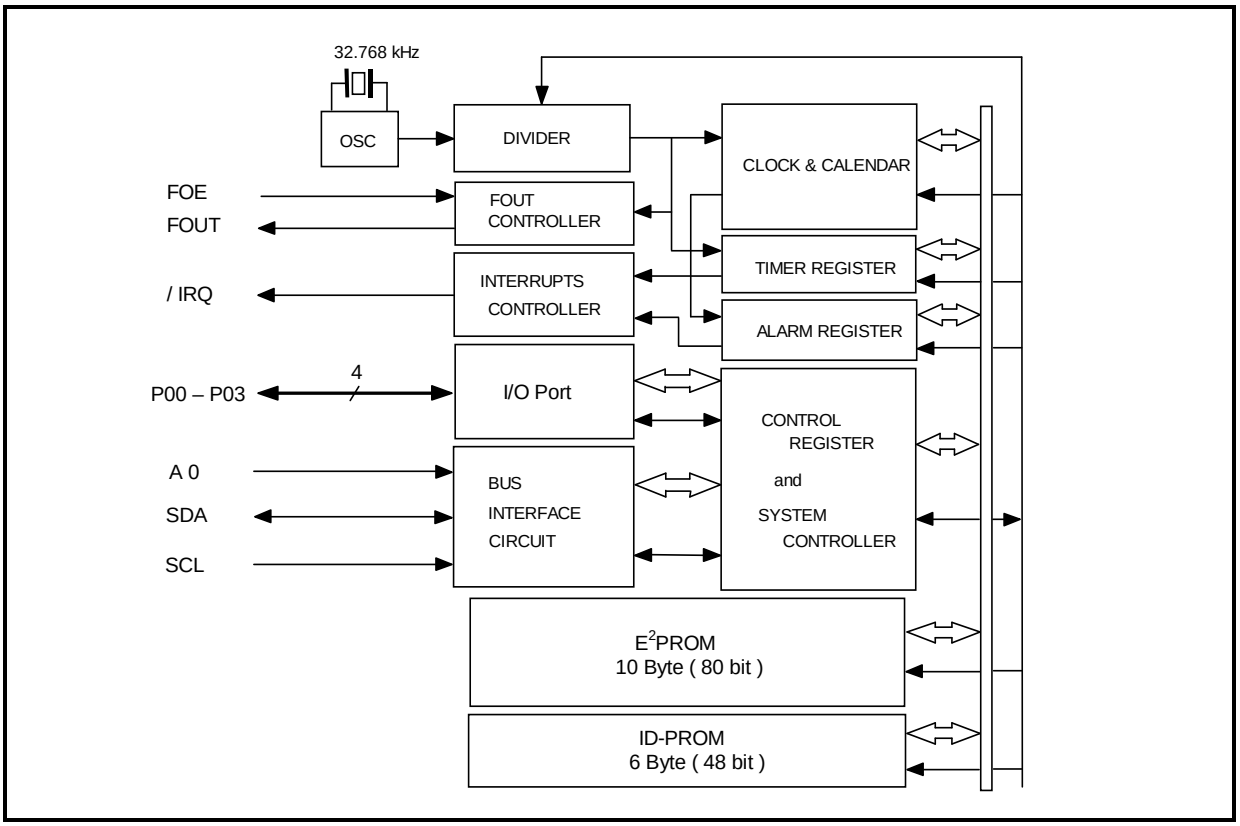
This is a real-time clock module of the I²C-BUS interface system that incorporates a 32.768 kHz crystal oscillator.

The real-time clock function incorporates not only a calendar and clock counter for the year, month, day, day of the week, hour, minute, and second, but also a time alarm, interval timer, and time update interruption, among other features.

The device operates with low current consumption due to the C-MOS process, and is thus able to operate on backup battery power for an extended period.

With such multiple functions housed in a downsized package, the module is perfect for use in a diverse range of cellular phones, handy terminals, and other compact electronic devices.

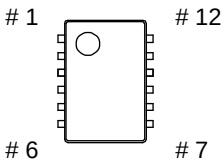
2. Block Diagram



3. Terminal description

3.1. Terminal connections

RX – 8731 LC



3.2. Pin Functions

Signal name	I/O	Function
SDA	Bi-directional	Addresses, data, acknowledge bits, etc. are input and output in synchronization with the I^2C-BUS communication serial clock. An appropriate pull-up resistance in accordance with the capacity of the signal cable must be connected to this terminal, which is an open drain at the time of output.
SCL	Input	The serial clock for I^2C-BUS communication is input here.
A0	Input	Device Address
P00, P01	Bi-directional	I/O Port (N-ch Open drain Output)
P02, P03	Bi-directional	I/O Port (C-MOS Output)
FOUT	Output	The FOUT terminal is a 32.768-kHz clock output terminal provided with output control. The FOE terminal is an input terminal for controlling the FOUT output.
FOE	Input	
/ IRQ	Output	This terminal outputs interrupt signals ("L" level) for alarm interval timers, time update interruptions, and the like. This is an N-ch open-drain output terminal.
VDD	–	This is a power-supply terminal for the of the main power supply.
GND	–	This terminal is connected to the negative side (Ground) of the power supply.

FOE pin input	FSEL1 bit	FSEL0 bit	FOUT pin output
X (Don't care)	0	0	32768 Hz Output (C-MOS output)
	0	1	1024 Hz Output (C-MOS output)
	1	0	1 Hz Output (C-MOS output)
" H "	1	1	32768 Hz Output (C-MOS output) *
" L "	1	1	OFF (high impedance)

Note: FOUT outputs 32.768 kHz when the initial power-on occurs. (FOE needs high level.)

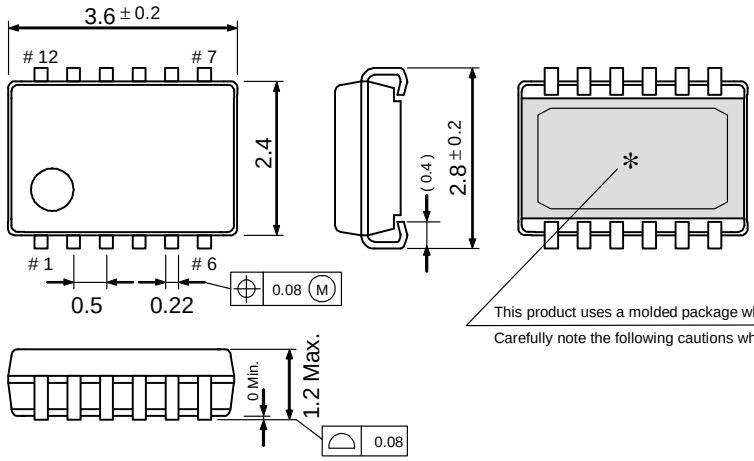
Note : Be sure to connect a bypass capacitor rated at least 0.1 µF between VDD and GND.

4. External Dimensions / Marking Layout

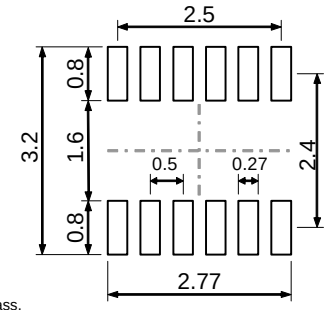
4.1. External Dimensions

RX – 8731 LC (VSOJ – 12pin)

• External dimensions



• Recommended soldering pattern



Unit : mm

* Notes on packaging

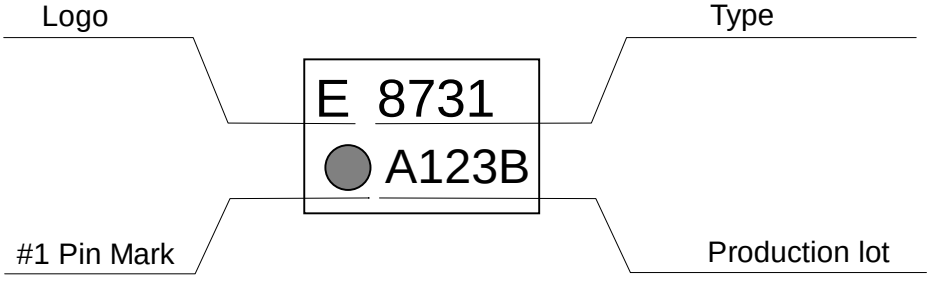
This product uses a molded package whose back contains glass.
Carefully note the following cautions when handling.

(1) Packaging equipment
This product uses a molded package whose back contains glass.
Therefore, it is possible for shocks during packaging to cause product breakage, depending on the packaging machinery and conditions.
Please be sure to check that the load placed on products during packaging is as low as possible (low speeds during loading onto the substrate, low chuck forces, etc.) before using packaging equipment.
Carry out the same checks when changing packaging conditions.
The presence of foreign objects between this product and the packaging substrate may result in product breakage.
Guard against introduction of foreign objects during packaging.
Also, carry out measures to eliminate static electricity during packaging of and operations with this product.

(2) Stop using the glue
Any glue must never use it after soldering RTC to a circuit board.
This product has glass on the back side of a package.
When glue invasions between circuit board side and glass side, then glass cracks by thermal expansion of glue.
In this case a crystal oscillation stops.
Consider glue abolition or glue do not touch to RTC.

4.2. Marking Layout

RX – 8731 LC (VSOJ – 12pin)



* Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

5. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Between V_{DD} and GND	–0.3 to +6.5	V
Input voltage	V_{IN}	FOE, A0, P0x, SCL, SDA pins	GND–0.3 to +6.5	V
Output voltage	V_{OUT}	FOUT, P0x, SDA, /IRQ pins	GND –0.3 to +6.5	V
Storage temperature	T_{STG}	When stored separately, without packaging	–55 to +125	°C

6. Recommended Operating Conditions

GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	–	1.7	3.0	5.5	V
Clock supply voltage	V_{CLK}	Ta = –40 °C to +85 °C	1.3	3.0	5.5	V
Pull-up voltage	V_{PUP}	SDA, /IRQ,P00,P01 pins			5.5	V
Operating temperature range	T_{OPR}	No condensation	–40	+25	+85	°C

7. Frequency Characteristics

* Unless otherwise specified, GND = 0 V, Ta = +25 °C, V_{DD} = 3.0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output frequency	fo			32.768 (Typ.)		kHz
Frequency precision	$\Delta f / f$	Ta = +25 °C V_{DD} = 3.0 V		5 ± 23 (*1) (*2)		$\times 10^{-6}$
Frequency/voltage characteristics	f / V	Ta = +25 °C V_{DD} = 2.0 V to 5.0 V	–2		+2	$\times 10^{-6}$ / V
Frequency/temperature characteristics Oscillation start time	Top	Ta = –20 °C to +70 °C V_{DD} = 3.0 V ; +25 °C reference	–120		+10	$\times 10^{-6}$
Oscillation start time	tSTA	Ta = +25 °C V_{DD} = 1.7 V		0.5	1.0	s
		Ta = –40 °C to +85 °C V_{DD} = 1.7 V			3.0	s
Aging	fa	Ta = +25 °C V_{DD} = 3.0 V ; first year	–5		+5	$\times 10^{-6}$ / year

*1) This difference is 1 minute by 1 month. (excluding offset)
*2) Including the frequency variation arising from three reflow processings.
Reflow processing as conducted under Epson Toyocom's conditions (Refer to the individual l specification).

8. Electrical Characteristics

8.1. DC characteristics

* Unless otherwise specified,
f_{SCL} = 0 Hz, GND = 0 V, V_{DD} = 1.7 V to 5.5 V, Ta = –40 °C to +85 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	f_{SCL} = 0 Hz, /IRQ = OFF FOUT : OFF (Hi - z) Ta = –40 °C to +70 °C	V_{BK} = 5 V		450	900	nA
Current consumption (2)	I_{DD2}		V_{BK} = 3 V		350	800	
Current consumption (3)	I_{DD3}	f_{SCL} = 0 Hz, /IRQ = OFF FOUT : OFF (Hi - z)	V_{DD} = 5 V		450	1500	nA
Current consumption (4)	I_{DD4}		V_{DD} = 3 V		350	1400	
Current consumption (5)	I_{DD5}	f_{SCL} = 0 Hz, /IRQ = OFF , FOE = V_{DD} FOUT : 32.768 kHz ON, C_L = 0 pF	V_{DD} = 5 V		3.0	6.0	µA
Current consumption (6)	I_{DD6}		V_{DD} = 3 V		2.0	4.0	
Current consumption (7)	I_{DD7}	f_{SCL} = 0 Hz, /IRQ = OFF , FOE = V_{DD} FOUT : 32.768 kHz ON, C_L = 30 pF	V_{DD} = 5 V		8.0	16.0	µA
Current consumption (8)	I_{DD8}		V_{DD} = 3 V		5.0	10.0	
"H" input voltage	V_{IH}	Input pins		0.8 × V_{DD}		6.5	V
"L" input voltage	V_{IL}	Input pins		GND – 0.3		0.2 × V_{DD}	V
"H" output voltage	V_{OH1}	FOUT, P0x pins	V_{DD} = 5 V, I_{OH} = –1 mA	4.5		5.0	V
	V_{OH2}		V_{DD} = 3 V, I_{OH} = –1 mA	2.2		3.0	
	V_{OH3}		V_{DD} = 3 V, I_{OH} = –100 µA	2.9		3.0	
"L" output voltage	V_{OL1}	FOUT, P0x pins	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND+0.5	V
	V_{OL2}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND+0.8	
	V_{OL3}		V_{DD} = 3 V, I_{OL} = 100 µA	GND		GND+0.1	
	V_{OL4}	/IRQ pin	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND+0.25	V
	V_{OL5}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND+0.4	
	V_{OL6}	SDA pin	V_{DD} ≥2 V, I_{OL}=3 mA	GND		GND+0.4	V
Input leakage current	I_{LK}	Input pins V_{IN} = V_{DD} or GND		–0.5		0.5	µA
Output leakage current	I_{OZ}	Output pins V_{OUT} = V_{DD} or GND		–0.5		0.5	µA

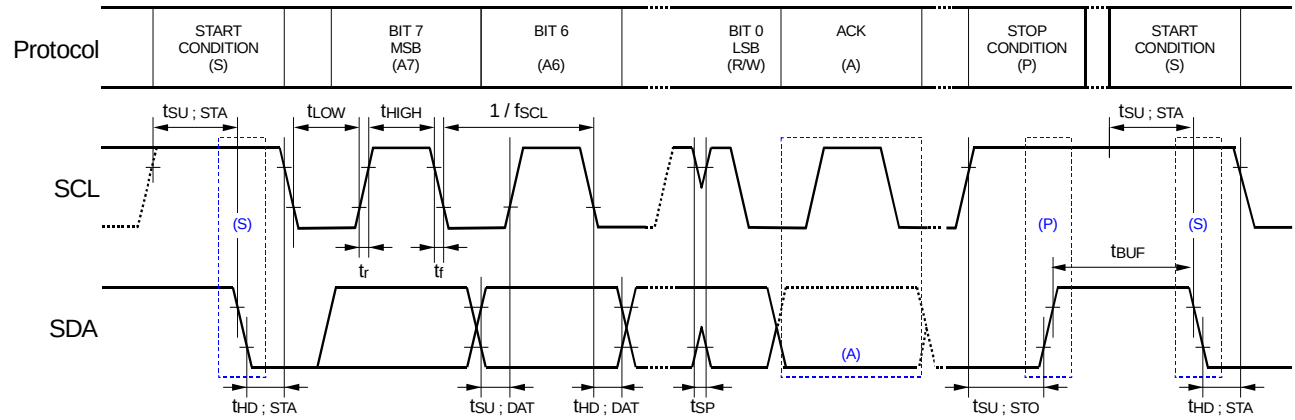
8.2. AC characteristics

8.2.1. AC characteristics(1)

* Unless otherwise specified,
f_{SCL} = 0 Hz, GND = 0 V, V_{DD} = 1.7 V to 5.5 V, Ta = –40 °C to +85 °C

Item	Symbol	Standard-Mode (f_{SCL}=100kHz)		Fast-Mode (f_{SCL}=400kHz)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}		100		400	kHz
Start condition setup time	$t_{SU;STA}$	4.7		0.6		µs
Start condition hold time	$t_{HD;STA}$	4.0		0.6		µs
Data setup time	$t_{SU;DAT}$	250		100		ns
Data hold time	$t_{HD;DAT}$	0		0		ns
Stop condition setup time	$t_{SU;STO}$	4.0		0.6		µs
Bus idle time of "Stop" from "Start".	t_{BUF}	4.7		1.3		µs
Time when SCL = "L"	t_{LOW}	4.7		1.3		µs
Time when SCL = "H"	t_{HIGH}	4.0		0.6		µs
Rise time for SCL and SDA	t_r		1.0		0.3	µs
Fall time for SCL and SDA	t_f		0.3		0.3	µs

Timing chart

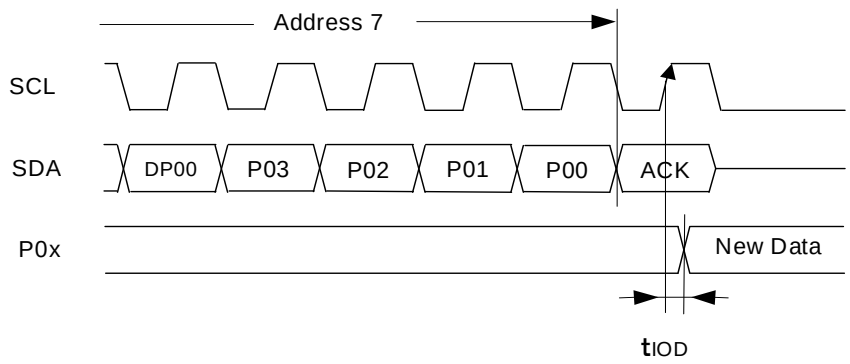


Caution: When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access **should be completed within 0.95 seconds**.
If such communication requires **0.95 seconds** or longer, the I^2C bus interface is reset by the internal bus timeout function, and the time is late for maximum one second.
However, there is a condition under which reset function is activated.Please refer to [9.11 bus timeout function] for details.

8.2.2. AC characteristics(2)

* Unless otherwise specified,
f_{SCL} = 0 Hz, GND = 0 V, V_{DD} = 1.7 V to 5.5 V, Ta = –40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
I/O port Delay Time	t_{IOD}	P0x pin, C_L = 30 pF			300	ns
FOUT duty	Duty	50% of V_{DD} level	40	50	60	%

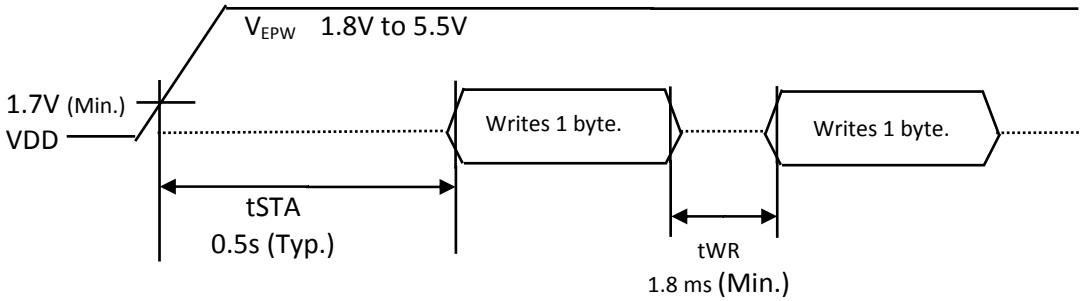


8.3. EEPROM characteristics

* Unless otherwise specified GND = 0 V, V_{DD} = 1.7 V to 5.5 V, Ta = –40 °C to +85 °C

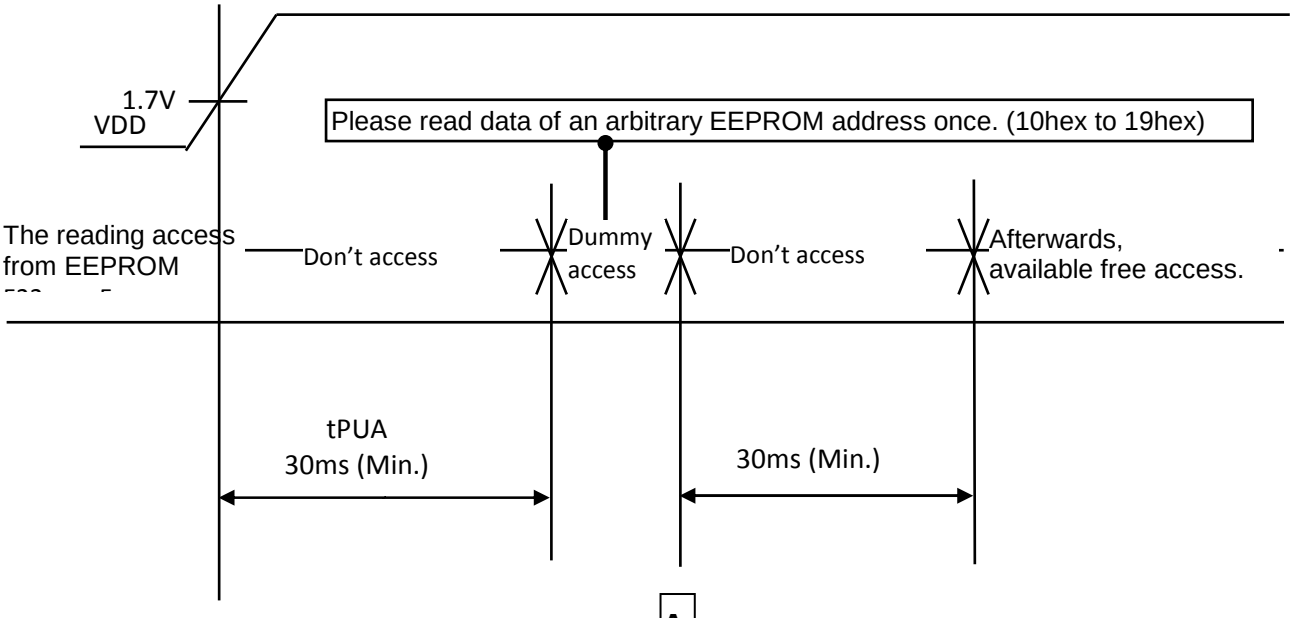
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Operation voltage range*1	V_{EPW}	V_{DD} pin	1.8		5.5	V
Current consumption	I_{DD9}	Writing to E^2PROM			2	mA
Power-on to E^2PROM access*2	t_{PUA}	–			30	ms
Write cycle time*3	t_{wr}	–			1.8	ms
Program/Erase Cycle	N_W	–	10^5			cycles
Data Retention	T_{DR}	–	10			Years

8.4 The procedure of writing to EEPROM.



A built-in crystal oscillation clock is necessary for data writing to E2PROM.
Therefore, when writing to E2PROM, please wait for tSTA (0.5 sec Typ.).
Please write E2PROM by a byte unit. Wait time of tWR (1.8ms) is necessary by every 1 byte.

8.5 The procedure of data reading from EEPROM.



A

Please supply the voltage more than 1.7V to a VDD terminal.
Please wait more than 30ms from power-on.
Please do dummy read access to E2PROM area.
(one of 10hex - 19hex)
Please wait 30ms.
Afterwards, available free access.

The more fast reading method.

1:Please read bit2 of register F from an "A" timing.
2:if bit2 is "1" then read again.
3:Please repeat this reading.
4:If 0 is read from bit2, waiting is finished.

9. Description of Functions

9.1. Memory Map

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	note
00	SEC	○	40	20	10	8	4	2	1	∗3
01	MIN	○	40	20	10	8	4	2	1	∗3
02	HOUR	○	○	20	10	8	4	2	1	∗3
03	WEEK	○	6	5	4	3	2	1	0	∗3
04	DAY	○	○	20	10	8	4	2	1	∗3
05	MONTH	○	○	○	10	8	4	2	1	∗3
06	YEAR	80	40	20	10	8	4	2	1	
07	I/O Port DDR / Data	DP03	DP02	DP01	DP00	P03	P02	P01	P00	∗5
08	MIN Alarm	AE	40	20	10	8	4	2	1	
09	HOUR Alarm	AE	•	20	10	8	4	2	1	∗4
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	∗4
	DAY Alarm		•	20	10	8	4	2	1	
0B	Timer Counter 0	128	64	32	16	8	4	2	1	
0C	Timer Counter 1	•	•	•	•	2048	1024	512	256	∗4
0D	Extension Register	***TEST***	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	∗1
0E	Flag Register	***TEST***	○	UF	TF	AF	○	VLF	○	∗1 , ∗3
0F	Control Register	***TEST***	EWP	UIE	TIE	AIE	○	STOP	○	∗3 , ∗6

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	note
10 | 19	E^2PROM	80 bit (10 byte x 8 bit)								∗6
1A | 1F	ID-ROM	48 bit (6 byte x 8 bit)								∗7

∗1. During the initial power-on (from 0 V), the power-on reset function sets "1" to the VLF bit.
∗ Since the value of other registers is undefined at this time, be sure to reset all registers before using them.

∗2. The *TEST* bits are Epson Tyocom test bits.
∗ Be sure to write "0" by initializing before using the clock module. Afterward, be sure to set "0" when writing.
∗ The three *TEST* bits are undefined when read. Those bits should be masked after being read.

∗3. The '□ ○ ' mark indicates a write-prohibited bit, which returns a "0" when read.

∗4. The ' • ' mark indicates a read/write-accessible RAM bit for any data.

∗5. When supplying initial power from 0 V, a value of register 07 is initialized to"1100 1011"(cb h), and P00,01 is set to input port and P02,03 is set to output port. Further, P02 is set to Low and P03 is set to High output.

∗6. EWP bit is a bit for write-protection of E^2PROM. When setting EWP bit to " 1 " , writing operation to E^2PROM is permitted. When supplying initial power, EWP bit is initialized to " 0 ".It is unable to execute continuous writing to E^2PROM with auto-increment. Further, after Byte writing, waiting time for 1.8ms is needed until next writing.

∗7. When shipping from factory, unique ID information is written to ID-ROM individually. End user can only read it.

9.2. Description of registers

9.2.1. Clock counter (Reg – 00[h] to 02[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	SEC	○	40	20	10	8	4	2	1
01	MIN	○	40	20	10	8	4	2	1
02	HOUR	○	○	20	10	8	4	2	1

- The clock counter counts seconds, minutes, and hours.
- The data format is BCD format. For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.

∗ Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

1) [Seconds] register (Reg – 00 [h])
This counter counts seconds.
Count values are updated as: 00 seconds, 01 second, 02 to 59 seconds, 00 seconds, 01 second, etc. in that order.

2) [Minutes] register (Reg – 01 [h])
This counter counts minutes.
Count values are updated as: 00 minutes, 01 minute, 02 to 59 minutes, 00 minutes, 01 minute, etc. in that order.

3) [Hours] register (Reg – 02 [h])
The [Hours] counter uses a 24-hour clock.
Count values are updated as: 00 hours, 01 hour, 02 to 23 hours, 00 hours, 01 hour, etc. in that order.

9.2.2. Day counter (Reg – 03[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
03	WEEK	○	6	5	4	3	2	1	0

- The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
  The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
- The correspondence between days and count values is shown below.

[WEEK]	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day	Data[h]
Write / Read	0	0	0	0	0	0	0	**1**	Sunday	01 h
	0	0	0	0	0	0	**1**	0	Monday	02 h
	0	0	0	0	0	**1**	0	0	Tuesday	04 h
	0	0	0	0	**1**	0	0	0	Wednesday	08 h
	0	0	0	**1**	0	0	0	0	Thursday	10 h
	0	0	**1**	0	0	0	0	0	Friday	20 h
	0	**1**	0	0	0	0	0	0	Saturday	40 h
Write prohibit	∗ Do not set "1" to more than one day at the same time. Also, note with caution that any setting other than the seven shown above should not be made as it may interfere with normal operation.								–	–

9.2.3. Calendar counter (Reg – 04[h] to 06[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
04	DAY	○	○	20	10	8	4	2	1
05	MONTH	○	○	○	10	8	4	2	1
06	YEAR	80	40	20	10	8	4	2	1

- The clock counter counts seconds, minutes, and hours.
- The data format is BCD format. For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.

∗ Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

1) [Day] register (Reg – 04 [h])

- This is the date counter.
  Updating of this counter varies depending on the month.

∗ A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01," "02," "03," to "28," "29," "01," etc.

DAY	Month	Date update pattern
Write / Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 ~ 30, 31, 01 ~
	4, 6, 9, or 11	01, 02, 03 ~ 30, 01, 02 ~
	February in normal year	01, 02, 03 ~ 28, 01, 02 ~
	February in leap year	01, 02, 03 ~ 28, 29, 01 ~

2) [Months] register (Reg – 05 [h])

- This is the month counter.
  It is updated in annual cycles of regularly ordered months (January, February, March, etc.).

3) [YEAR] register (Reg – 06 [h])

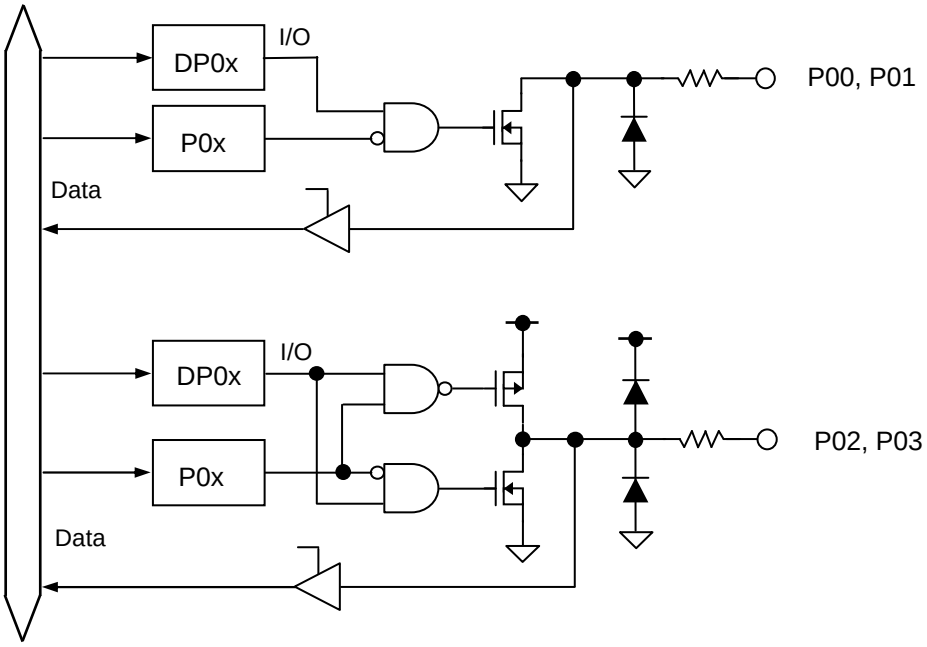
- This is the year counter.
  It is updated in 100-year cycles of regularly ordered years (00, 01, 02 to 99, etc.).

∗ Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as a leap year.

9.2.4. I/O Port DDR / Data register (Reg – 07 [h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
07	I/O Port DDR / Data	DP03	DP02	DP01	DP00	P03	P02	P01	P00
		Data direction (0: In, 1: Out)				Port Data			

- Register for programable I/O port.
  Execute input and output setting for each port with DP00 to DP03 bits, and consequently P00 to P03 s set to data bits.



- When supplying initial power, a value of register 07 is initialized to ”1100 1011”(cb h), then 00,01 is set to input port and P02,03 is set to output port.
  Further, P02 is set to Low, and P03 is set to High.

Pin	I/O	Data	condition
P00	In	1	Hi-Z (N-ch Open drain)
P01	In	1	Hi-Z (N-ch Open drain)
P02	Out	0	Low level (C-MOS)
P03	Out	1	High level (C-MOS)

- If read data of P00 to P03, it is able to retrieve a condition of corresponding pins.
  (Register content from DP00 to DP03 can be retrieved)
- In case of writing to a port, data is latched to data register P00 to P03.
  Insuch case, if corresponding setting bits DP00 to DP03 is"1", data of P00 to P03 is output to the pin, and data is not output if "0" (for setting of input port).
- In case of change over from input mode to output mode, (DPx : "0"→"1")
  data latched to data register Pox is output to the pin.

9.2.5. Alarm registers (Reg – 08[h] to 0A[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	•	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1

- The alarm interrupt function is used, along with the AEI, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.
- When the settings in the above alarm registers and the WADA bit match the current time, the /IRQ pin goes to low level and "1" is set to the AF bit to report that and alarm interrupt event has occurred.

9.2.6. Down counter for fixed-cycle timer (Reg – 0B[h] to 0C[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Timer Counter 0	128	64	32	16	8	4	2	1
C	Timer Counter 1	•	•	•	•	2048	1024	512	256

- This register is used to set the default (preset) value for the counter. Any count value from 1 (001 h) to 4095 (FFFh) can be set
- To use the fixed-cycle timer interrupt function, the TE, TF, TIE, TSEL0, and TSELD1 bits are set and used.
- When this down counter's count value changes from 001h to 000h, when TF bit = "1", or when the /IRQ pin is at low level ("L"), it indicates that a fixed-cycle timer interrupt event has occurred.

9.2.7. Extension Register (Reg – 0D [h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Extension Register	*TEST*	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0

- This register is used to specify the target for the alarm function or time update interrupt function and to select or set operations such as fixed-cycle timer operations.

1) *TEST* bit

Those bits are the manufacturer's test bit.
Always leave this bit value as "0" except when testing.
Be careful to avoid writing to this bit when writing "1" to other bits in this register.

∗ The three *TEST* bits are undefined when read. Those bits should be masked after being read.

2) WADA bit (Week Alarm / Day Alarm Select)

This bit is used to specify either WEEK or DAY as the target of the alarm interrupt function.
Writing a "1" to this bit specifies DAY as the comparison object for the alarm interrupt function.
Writing a "0" to this bit specifies WEEK as the comparison object for the alarm interrupt function.

3) USEL bit (Update Interrupt Select)

This bit is used to specify either "1 second period" or "minute update" as the update generation timing of the time update interrupt function.
Writing a "1" to this bit specifies the internal clock's "minute update" (once per minute) operation as the timing by which time update interrupts are generated.
Writing a "0" to this bit specifies the internal clock's "one-second period" (once per second) operation as the timing by which time update interrupts are generated.

4) TE bit (Timer Enable)

This bit is used to control operation of the fixed-cycle timer interrupt function.
When "1" is written to this bit, the fixed-cycle timer interrupt function starts operating.
When "0" is written to this bit, the fixed-cycle timer interrupt function stops operating.

5) FSEL1,FSEL0 bits (Frequency Select 1, 0)

A combination of the FSEL1 and FSEL0 bits is used to select the frequency to be output.
The choice is possible by a combination of FSEL-bits and FOE-pin, select the frequency of clock output or inhibit the clock output.

6) TSEL1,TSEL0 bits (Timer Select 1, 0)

These bits specify the fixed-cycle timer interrupt function's countdown period (source clock).
Four different periods can be selected via combinations of these two bit values.

9.2.8. Flag Register (Reg – 0E [h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0E	Flag Register	*TEST*	○	UF	TF	AF	○	VLF	○

- This is a flag register that indicates circumstantial results, such as the state of power supply, the generated state of various interrupt events, the reliability of internal data, and the like.

1) UF bit (Update Flag)
This flag bit holds the result of the detection of a time-update interrupt event.
If a time-update interrupt event is generated, this bit shifts from "0" to "1."

2) TF bit (Timer Flag)
This flag bit holds the result of the detection of a fixed-cycle timer interrupt event.
If a fixed-cycle timer interrupt event is generated, this bit shifts from "0" to "1."

3) AF bit (Alarm Flag)
This is a flag bit that retains the result when an alarm interrupt event has been detected.
When an alarm interrupt event occurs, this bit's value changes from "0" to "1".

4) VLF bit (Voltage Low Flag)
This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
During the initial power-on (from 0 V) and if the value of the VLF bit is "1" when the VLF bit is read, be sure to initialize all registers before using them.

VLF	Data	Description
Write	0	The VLF is cleared to 0, and waiting for next low voltage detection.
	1	It is impossible to write in 1 to VLF.
Read	0	RTC register data are valid.
	1	RTC register data are invalid. Should be initialized of all register data. VLF is maintained till it is cleared by zero.

9.2.9. Control Register (Reg – 0F [h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0F	Control Register	*TEST*	EWP	UIE	TIE	AIE	○	STOP	○

- This is a flag register that indicates circumstantial results, such as the state of power supply, the generated state of various interrupt events, the reliability of internal data, and the like.

1) EWP bit (E^2PROM Write Protect)
When "1" is written to this bit, can use E^2PROM Write operation.
During the initial power-on (from 0 V), the power-on reset function resets "0" to the EWP bit.

2) UIE bit (Update Interrupt Enable)
This bit sets the operation of the /INT interrupt signal when a time update event has occurred (the UF bit value changes from "0" to "1").
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /INT pin.
Writing "0" to this bit prohibits low-level output from the /INT pin.

3) TIE bit (Timer Interrupt Enable)
This bit sets the operation of the /INT interrupt signal when a fixed-cycle interrupt event has occurred (the TF bit value changes from "0" to "1").
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /INT pin.
Writing "0" to this bit prohibits low-level output from the /INT pin.

4) AIE bit (Alarm Interrupt Enable)
This bit sets the operation of the /INT interrupt signal when an alarm interrupt event has occurred (the AF bit value changes from "0" to "1").
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /INT pin.
Writing "0" to this bit prohibits low-level output from the /INT pin.

5) STOP bit
This bit is used to stop functions related to the RTC's internal counter operations.
Writing a "1" to this bit stops the counter operations.
Writing a "0" to this bit cancels stop status (restarts operations).
∗ For optimum performance, do not use this bit for functions other than the clock and calendar functions.

- The relation between STOP bit and other operation.

If STOP bit is " 1 ", it comes under the influence of the followings.

* Stop 1) updates of year, month, date, day of the week, hours, minutes and seconds are stopped.
  · All updates of clock and calendar operation are stopped.
  Further, an alarm interrupt event is not functioned with them.

* Stop 2) Periodical time interrupt function is partially stopped.
  · If source lock setting of periodical timer is set to 64 Hz, 1 Hz, 1/60 Hz,
  periodical timer interrupt function is not worked.
  (It is only operated if source lock setting is 4096 Hz)

9.3. E^2PROM and ID-ROM

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0F	Control Register	TEST	**EWP**	UIE	TIE	AIE	○	STOP	○

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10 | 19	**E^2PROM**	80 bit (10 byte x 8 bit)							
1A | 1F	**ID-ROM**	48 bit (6 byte x 8 bit)							

1) EWP bit (E^2PROM Write Protect)

EWP is a bit for write- protect of E^2PROM.
When setting EWP bit to " 1 ", writing to E^2PROM is permitted.
When supplying initial power, EWP bit is initialized to " 0 ".

2) E^2PROM

Continuous wrting to E^2PROM with auto-increment cannot be executed.
And after Byte writing, waiting time with 1.8ms is needed until next writing.
In case of execution writing to E^2PROM without waiting, it is ignored.
Access to area except E^2PROM is available.
The quartz oscillation clock is used for data writing to E^2PROM, therefore it is unable to write to E^2PROM until the quartz oscillator is worked after supplying power.

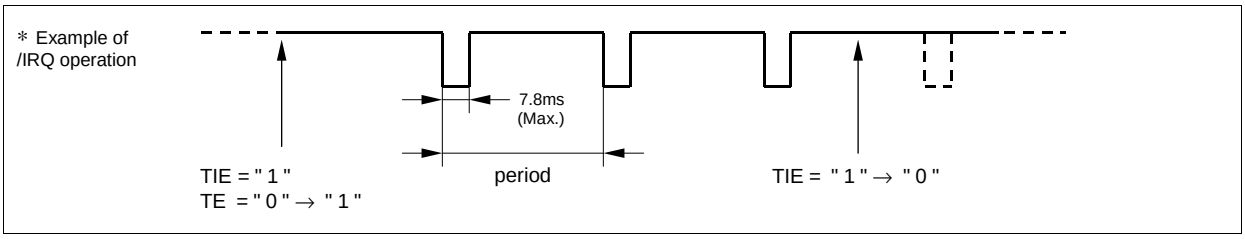
3) ID-ROM

Individual unique ID is written to ID-ROM when shipping from factory.
ID-ROM cannot be written by customer. Only reading is available.

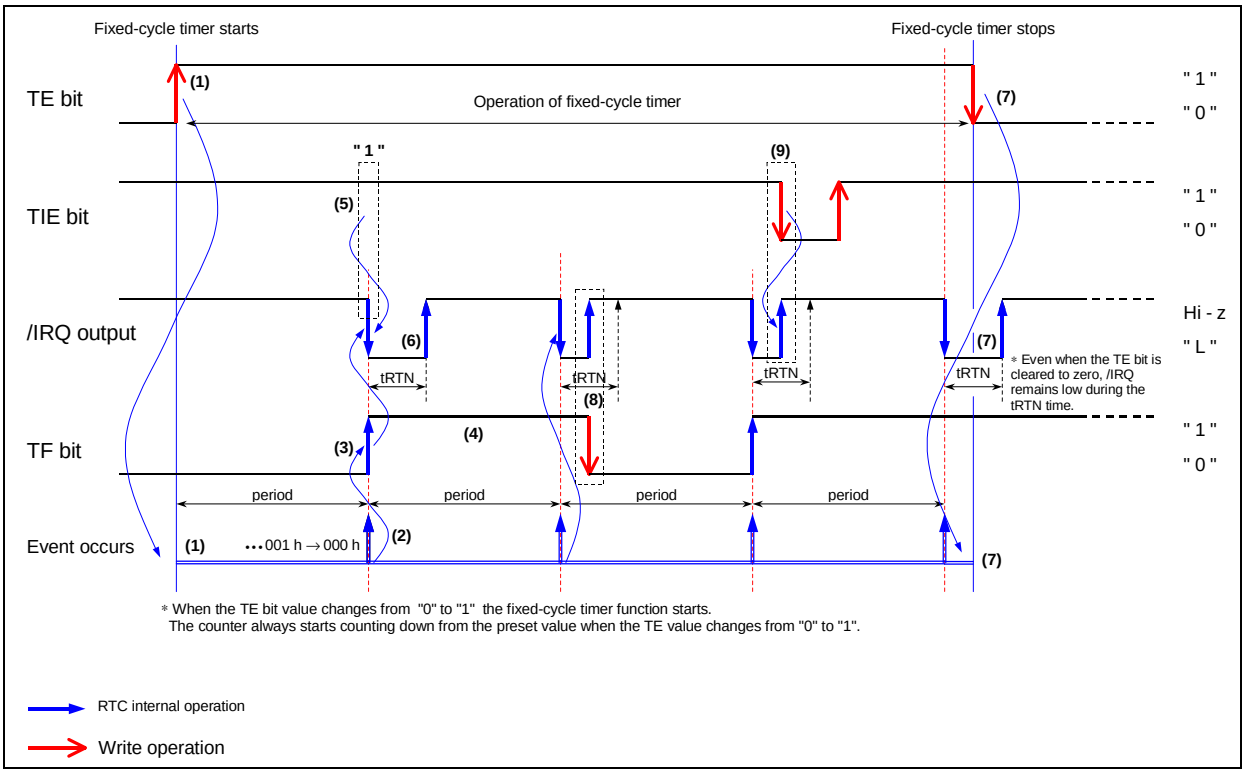
+86-0755-2990-5940

9.4. Fixed-cycle Timer Interrupt Function

The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 4095 minutes.
When an interrupt event is generated, the /IRQ pin goes to low level and "1" is set to the TF bit to report that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated low-level output from the /IRQ pin occurs only when the value of the control register's TIE bit is "1". Up to 7.8 ms after the interrupt occurs, the /IRQ status is automatically cleared (/IRQ status changes from low-level to Hi-Z).



9.4.1. Diagram of fixed-cycle timer interrupt function



(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 001h to 000h, an interrupt event occurs.
∗ After the interrupt event that occurs when the count value changes from 001h to 000h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

(3) When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.

(4) When the TF bit = "1" its value is retained until it is cleared to zero.

(5) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /IRQ pin output goes low.
∗ If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /IRQ pin output remains Hi-Z.

(6) Output from the /IRQ pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
∗ /IRQ is again set low when the next interrupt event occurs.

(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped and the /IRQ pin is set to Hi-Z status.
∗ When /IRQ = low, the fixed-cycle timer function is stopped. The tRTN period is the maximum amount of time before the /IRQ pin status changes from low to Hi-Z.

(8) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the TF bit value changes from "1" to "0".

(9) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the TIE bit value changes from "1" to "0".

9.4.2. Related registers for function of fixed-cycle timer interrupt function

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
0C	Timer Counter 1	•	•	•	•	**2048**	**1024**	**512**	**256**
0D	Extension Register	***TEST***	WADA	USEL	**TE**	FSEL1	FSEL0	**TSEL1**	**TSEL0**
0E	Flag Register	***TEST***	○	UF	**TF**	AF	○	VLF	○
0F	Control Register	***TEST***	EWP	UIE	**TIE**	AIE	○	STOP	○

∗ Before entering operation settings, we recommend first clearing the TE bit to "0" and then clearing the TF and TIE bits to "0" in that order, so that all control-related bits are zero-cleared (= set to operation stop mode) to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (Reg – 0B to 0C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) TSEL1, TESL0 bits (Timer Select 1, 0)

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

TSEL1, 0	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock	Auto reset time tRTN	Effects of STOP and RESET bits
W / R	0	0	4096 Hz /Once per 244.14 µs	122 µs	–
	0	1	64 Hz /Once per 15.625 ms	7.813 ms	∗ Does not operate when the STOP bit or RESET bit value is "1".
	1	0	1 Hz /Once per second	7.813 ms	
	1	1	1/60 Hz /Once per minute	7.813 ms	

∗1) The /IRQ pin's auto reset time (tRTN) varies as shown above according to the source clock setting.

∗2) An interrupt that occurs when the source clock is in 1 Hz mode is not linked to the internal clock. (Instead, a dedicated 1 Hz timer circuit is used for independent operation.)

∗3) An interrupt that occurs when the source clock is in 1/60 Hz mode is linked to the internal clock's "minute" update operation.

2) Down counter for fixed-cycle timer (Timer Counter 1, 0)

This register is used to set the default (preset) value for the counter. Any count value from 1 (001 h) to 4095 (FFFh) can be set. The counter counts down based on the source clock's period, and when the count value changes from 001h to 000h, the TF bit value becomes "1".
The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.
Be sure to write "0" to the TE bit before writing the preset value. If a value is written while TE = "1" the first subsequent event will not be generated correctly.

Address 0C Timer Counter 1								Address 0B Timer Counter 0							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
•	•	•	•	2048	1024	512	256	128	64	32	16	8	4	2	1

∗ By the status of TE-bit, contents changes when reads these register.

TE bit	Description
" 0 " ∗ Stops fixed-cycle timer interrupt function.	The default (preset) value can be checked by reading this register.
" 1 " ∗ Starts fixed-cycle timer interrupt function.	The status during a countdown can be checked by reading this register. ∗ However, since the read data is not held (the data may be changing), to obtain accurate data the countdown status should be read twice and then compared.

∗ When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (Reg – 0B to 0C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

3) TE bit (Timer Enable)

When TE bit is "0", the default (preset) can be checked by reading this register.

TE	Data	Description
Write / Read	0	Stops fixed-cycle timer interrupt function. * Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-Z).
	1	Starts fixed-cycle timer interrupt function. * The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4) TF bit (Timer Flag)

This is a flag bit that retains the result when a fixed-cycle timer interrupt event is detected.

If it was already cleared to zero, this value changes from "0" to "1" when an event occurs, and the new value is retained.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-Z).
	1	This bit is invalid after a "1" has been written to it.
Read	0	Fixed-cycle timer interrupt events are not detected.
	1	Fixed-cycle timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

5) TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when a fixed-cycle timer interrupt event has occurred.

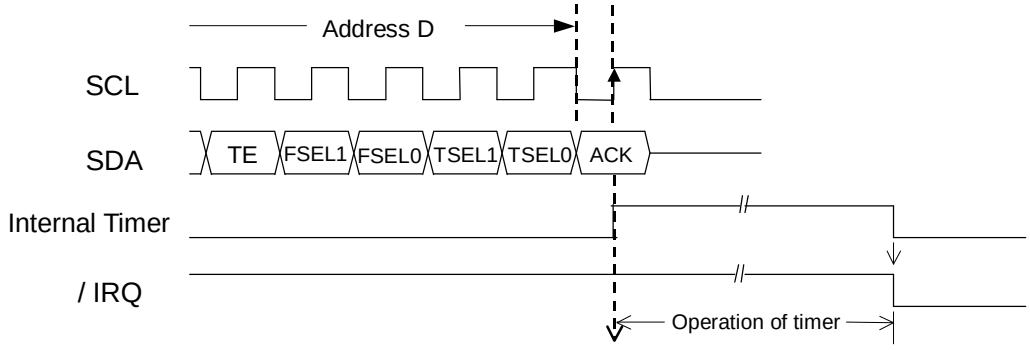
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /IRQ pin.

When a "0" is written to this bit, output from the /IRQ pin is prohibited (disabled).

TIE	Data	Description
Write / Read	0	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-Z). 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-Z). * Even when the TIE bit value is "0" another interrupt event may change the /IRQ status to low (or may hold /IRQ = "L").
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low).

9.4.3. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the SCL signal that occurs when the TE value is changed from "0" to "1" (after bit 0 is transferred).



9.4.4. Fixed-cycle timer interrupt interval (example)

The combination of the source clock settings (settings in TSEL1 and TSEL0) and fixed-cycle timer countdown setting (Reg–0B to Reg-0C setting) sets the fixed-cycle timer interrupt interval, as shown in the following examples.

Timer Counter setting	Source clock			
	4096 Hz TSEL1,0 0 , 0	64 Hz TSEL1,0 0 , 1	1 Hz TSEL1,0 1 , 0	1/60 Hz TSEL1,0 1 , 1
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.25 ms	2 s	2 min
⋮	⋮	⋮	⋮	⋮
41	10.010 ms	640.63 ms	41 s	41 min
82	20.020 ms	1.281 s	82 s	82 min
128	31.250 ms	2.000 s	128 s	128 min
192	46.875 ms	3.000 s	192 s	192 min
205	50.049 ms	3.203 s	205 s	205 min
320	78.125 ms	5.000 s	320 s	320 min
410	100.10 ms	6.406 s	410 s	410 min
640	156.25 ms	10.000 s	640 s	640 min
820	200.20 ms	12.813 s	820 s	820 min
1229	300.05 ms	19.203 s	1229 s	1229 min
1280	312.50 ms	20.000 s	1280 s	1280 min
1920	468.75 ms	30.000 s	1920 s	1920 min
2048	500.00 ms	32.000 s	2048 s	2048 min
2560	625.00 ms	40.000 s	2560 s	2560 min
3200	0.7813 s	50.000 s	3200 s	3200 min
3840	0.9375 s	60.000 s	3840 s	3840 min
⋮	⋮	⋮	⋮	⋮
4095	0.9998 s	63.984 s	4095 s	4095 min

- Fixed-cycle timer interrupt time error and fixed-cycle timer interrupt interval time

A fixed-cycle timer interrupt time error is an error in the selected source clock's $^{+0}/_{-1}$ interval time. Accordingly, the fixed-cycle timer interrupt's interval (one cycle) falls within the following range in relation to the set time.

Fixed-cycle timer interrupt's interval

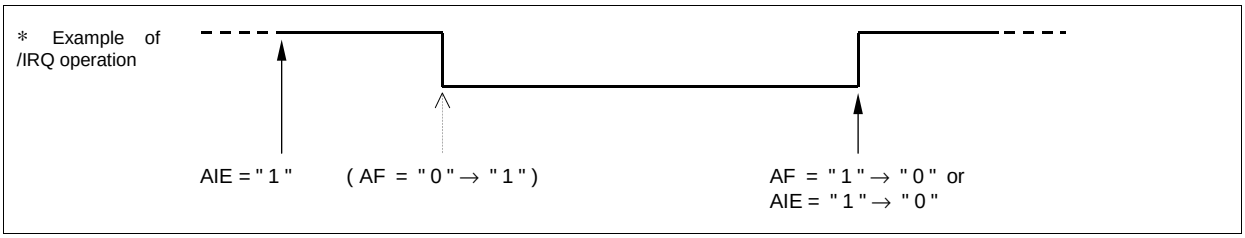
(Fixed-cycle timer interrupt's set time(∗) – source clock interval) to (fixed-cycle timer interrupt set time)

∗) Fixed-cycle timer interrupt's set time = Source clock setting × Countdown timer setting for fixed-cycle timer

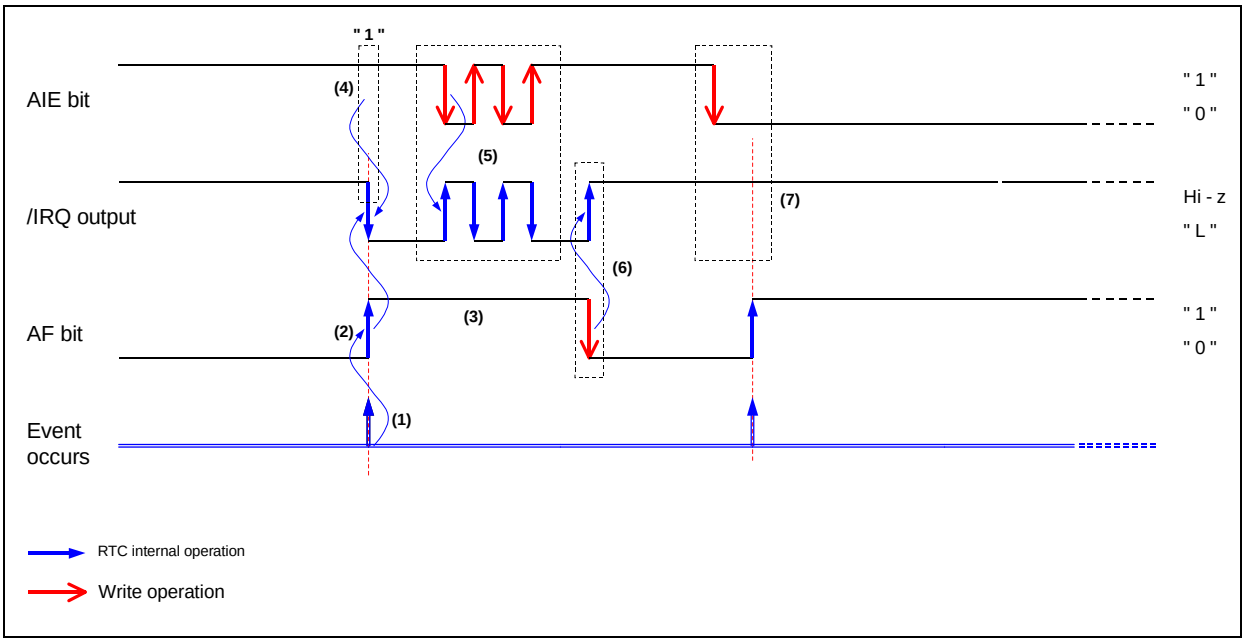
∗ The time actually set to the timer is adjusted by adding the time described above to the communication time for the serial data transfer clock used for the setting.

9.5. Alarm Interrupt Function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.
When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred.



9.5.1. Diagram of alarm interrupt function



(1) The hour, minute, date or day when an alarm interrupt event is to occur is set in advance along with the WADA bit, and when the setting matches the current time an interrupt event occurs.
(Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

(2) When a time update interrupt event occurs, the AF bit values becomes "1".

(3) When the AF bit = "1", its value is retained until it is cleared to zero.

(4) If AIE = "1" when an alarm interrupt occurs, the /IRQ pin output goes low.
* When an alarm interrupt event occurs, /IRQ pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from "1" to "0" while /IRQ is low, the /IRQ status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /IRQ status can be controlled via the AIE bit.

(6) If the AF bit value is changed from "1" to "0" while /IRQ is low, the /IRQ status immediately changes from low to Hi-Z.

(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /IRQ pin status remains Hi-Z.

9.5.2. Related registers for Alarm interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01	MIN	○	40	20	10	8	4	2	1
02	HOUR	○	○	20	10	8	4	2	1
03	WEEK	○	6	5	4	3	2	1	0
04	DAY	○	○	20	10	8	4	2	1
08	MIN Alarm	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	**AE**	•	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0D	Extension Register	***TEST***	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E	Flag Register	***TEST***	○	UF	TF	**AF**	○	VLF	○
0F	Control Register	***TEST***	EWP	UIE	TIE	**AIE**	○	STOP	○

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the STOP bit value is "1" alarm interrupt events do not occur.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg - 08h to 0Ah) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

∗ When the AIE bit value is "1" and the Alarm registers (Reg - 08h to 0Ah) is being used as a RAM register, /IRQ may be changed to low level unintentionally.

1) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write / Read	0	Sets WEEK as target of alarm function (DAY setting is ignored)
	1	Sets DAY as target of alarm function (WEEK setting is ignored)

2) Alarm registers (Reg – 08[h] to 0A[h])

The hour, minute, date or day when an alarm interrupt event will occur is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (Reg - A), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

When the settings made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /IRQ pin goes low.

∗1) The register that "1" was set to "AE" bit, doesn't compare alarm.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - A):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only an hour and minute accords with alarm data.

∗2) If all three AE bit values are "1" the week/date settings are ignored and an alarm interrupt event will occur once per minute.

3) AF bit (Alarm Flag)

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-Z) when an alarm interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE bit (Alarm Interrupt Enable)

When an alarm interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/IRQ status changes from Hi-Z to low) or is not generated (/IRQ status remains Hi-Z).

AIE	Data	Description
Write / Read	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-Z). ∗ Even when the AIE bit value is "0" another interrupt event may change the /IRQ status to low (or may hold /IRQ = "L").
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low). ∗ When an alarm interrupt event occurs, low-level output from the /IRQ pin occurs only when the AIE bit value is "1". This value is retained (not automatically cleared) until the AF bit is cleared to zero.

9.5.3. Examples of alarm settings

1) Example of alarm settings when "Day" has been specified (and WADA bit = "0")

Day is specified WADA bit = "0"	Reg – A								Reg - 9	Reg - 8
	bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S	HOUR Alarm	MIN Alarm
Monday through Friday, at 7:00 AM ∗ Minute value is ignored	0	0	1	1	1	1	1	0	07 h	80 h ~ FF h
Every Saturday and Sunday, for 30 minutes each hour ∗ Hour value is ignored	0	1	0	0	0	0	0	1	80 h ~ FF h	30 h
Every day, at 6:59 AM	0	1	1	1	1	1	1	1	18 h	59 h
	1	X	X	X	X	X	X	X		

X: Don't care

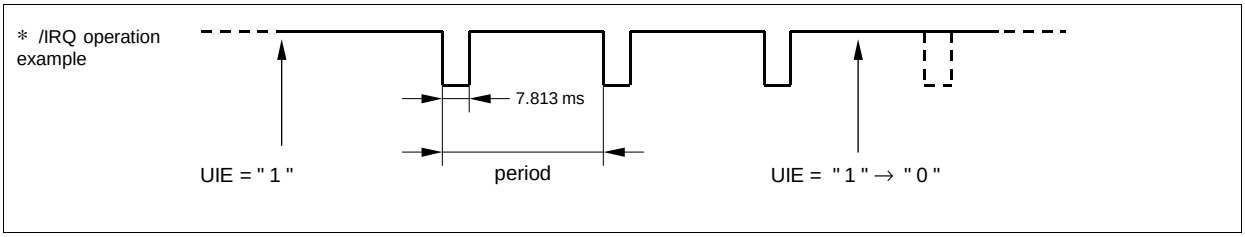
2) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

Day is specified WADA bit = "1"	Reg - A								Reg - 9	Reg - 8
	bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01	HOUR Alarm	MIN Alarm
First of each month, at 7:00 AM ∗ Minute value is ignored	0	0	0	0	0	0	0	1	07 h	80 h ~ FF h
15th of each month, for 30 minutes each hour ∗ Hour value is ignored	0	0	0	1	0	1	0	1	80 h ~ FF h	30 h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18 h	59 h

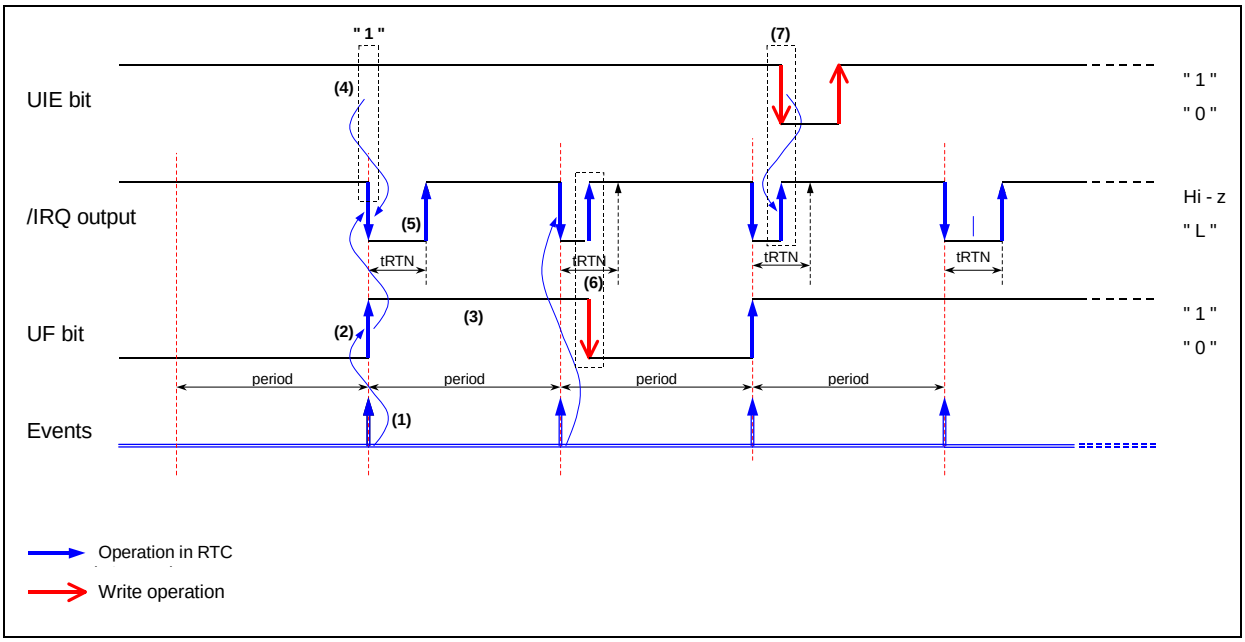
X: Don't care

9.6. Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.
When an interrupt event occurs, the UF bit value becomes "1" and the /INT pin goes to low level to indicate that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared (/INT status changes from low level to Hi-Z) 7.8 ms (fixed value) after the interrupt occurs.



9.6.1. Time update interrupt function diagram



(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.
* But, actually, it is an interrupt that occurs when the source clock is in second update mode is not linked to the internal clock. (Instead, a dedicated 1 Hz timer circuit is used for independent operation.)

(2) When a time update interrupt event occurs, the UF bit value becomes "1".

(3) When the UF bit value is "1" its value is retained until it is cleared to zero.

(4) When a time update interrupt occurs, /IRQ pin output is low if UIE = "1".
* If UIE = "0" when a timer update interrupt occurs, the /IRQ pin status remains Hi-Z.

(5) Each time an event occurs, /IRQ pin output is low only up to the tRTN time (which is fixed as 7.1825 ms for time update interrupts) after which it is automatically cleared to Hi-Z.
* /IRQ pin output goes low again when the next interrupt event occurs.

(6) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the UF bit value changes from "1" to "0".

(7) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the UIE bit value changes from "1" to "0".

9.6.2. Related registers for time update interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Extension Register	***TEST***	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E	Flag Register	***TEST***	○	**UF**	TF	AF	○	VLF	○
0F	Control Register	***TEST***	EWP	**UIE**	TIE	AIE	○	STOP	○

∗ Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the STOP bit value is "1" time update interrupt events do not occur.

∗ Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /IRQ pin status to low.

1) USEL bit (Update Interrupt Select)

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Data	Description
Write / Read	0	Selects "second update" (once per second) as the timing for generation of interrupt events ∗ But, actually, it is an interrupt that occurs when the source clock is in second update mode is not linked to the internal clock. (Instead, a dedicated 1 Hz timer circuit is used for independent operation.)
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF bit (Update Flag)

Once it has been set to "0", this flag bit value changes from "0" to "1" when a time update interrupt event occurs. When this flag bit = "1" its value is retained until a "0" is written to it.

UF	Data	Description
Write	0	The UF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-Z) when an time update interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Time update interrupt events are not detected.
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

3) UIE bit (Update Interrupt Enable)

When a time update interrupt event occurs (UF bit value changes from "0" to "1"), this bit selects whether to generate an interrupt signal (/IRQ status changes from Hi-Z to low) or to not generate it (/IRQ status remains Hi-Z).

UIE	Data	Description
Write / Read	0	1) Does not generate an interrupt signal when a time update interrupt event occurs (/IRQ remains Hi-Z) 2) Cancels interrupt signal triggered by time update interrupt event (/IRQ changes from low to Hi-Z). ∗ Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-Z) when an time update interrupt event has occurred.
	1	When a time update interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low). ∗ When a time update interrupt event occurs, low-level output from the /IRQ pin occurs only when the UIE bit value is "1". Up to 7.8 ms after the interrupt occurs, the /IRQ status is automatically cleared (/IRQ status changes from low to Hi-Z).

9.7. /IRQ "L" Interrupt Output When Interrupt Function Operates

1) Setting interrupt events to occur in response to /IRQ "L" interrupt output

The /IRQ interrupt output pin is shared as the output pin for three kinds of interrupt events: events related to the fixed-cycle timer interrupt function and events related to the time update interrupt function and events related to the alarm interrupt function.

When an interrupt occurs (when /IRQ is at low level ("L")), read the TF and UF and AF flags to determine which type of interrupt event occurred (which flag value changed to "1").

2) How to prevent /IRQ pin from going to low level ("L")

To prevent the /IRQ pin from going to low level ("L"), clear all TIE and UIE and AIE bits to zero.
To detect when an interrupt event has occurred without having to set the /IRQ pin to low level, monitor the TF and AF flag bit values to see if the target interrupt event has occurred (i.e., to see if either flag bit value changes from "0" to "1").

9.8. FOUT function [clock output function]

The clock signal (with precision equal to that of the on-chip crystal osillator) can be output (as C-MOS output) via the FOUT pin.

9.8.1. FOUT control register.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D	Extension Register	***TEST1***	WADA	○	TE	**FSEL1**	**FSEL0**	TSEL1	TSEL0

By a combination of FSEL and FOE, an FOUT terminal outputs 32768Hz and 1024Hz and 1Hz and can stop the output.

9.8.2. FOUT function table.

FOE pin input	FSEL1 bit	FSEL0 bit	FOUT pin output	
X (Don't care)	0	0	32768 Hz Output (C-MOS output)	
	0	1	1024 Hz Output (C-MOS output)	
	1	0	1 Hz Output (C-MOS output)	
" H "	1	1	32768 Hz Output (C-MOS output)	∗1
" L "	1	1	OFF (high impedance)	∗2

*1 At initial power-on , in case of FOE input is high, 32768Hz is selected automatically by power-on-reset-function.

*2 The combination to disable the FOUT output is FOE=Low and FSEL=FSEL1 = "1" only.
Other combinations output any frequency from FOUT terminal.

*3 When control about ON and OFF of the output from FOUT by only FSEL, should FOE=L.

FOE pin input	FSEL1 bit	FSEL0 bit	FOUT pin output
" L "	0	0	32768 Hz Output (C-MOS output)
	0	1	1024 Hz Output (C-MOS output)
	1	0	1 Hz Output (C-MOS output)
	1	1	OFF (high impedance)

*4 When control about ON and OFF of the output from FOUT by only by FOE terminal, should FSEL0=FSEL1="1".
Note: The control frequency is 32768Hz only.

FSEL1 bit	FSEL0 bit	FOE pin input	FOUT pin output
1	1	" H "	32768 Hz Output (C-MOS output)
		" L "	OFF (high impedance)

At initial power-on, FSEL0 and FSEL1 are set to "1" by power-on-reset function.

9.8.3. Attention of FOUT function.

Note 1
A disappearance of the FOUT output when the voltage sharply went up and down.

Note 2
The effect of STOP bit to FOUT functions.
When STOP = "1", 32768Hz and 1024Hz output is possible.
But 1Hz output is disabled.

9.9. Reading/Writing Data via the I²C Bus Interface

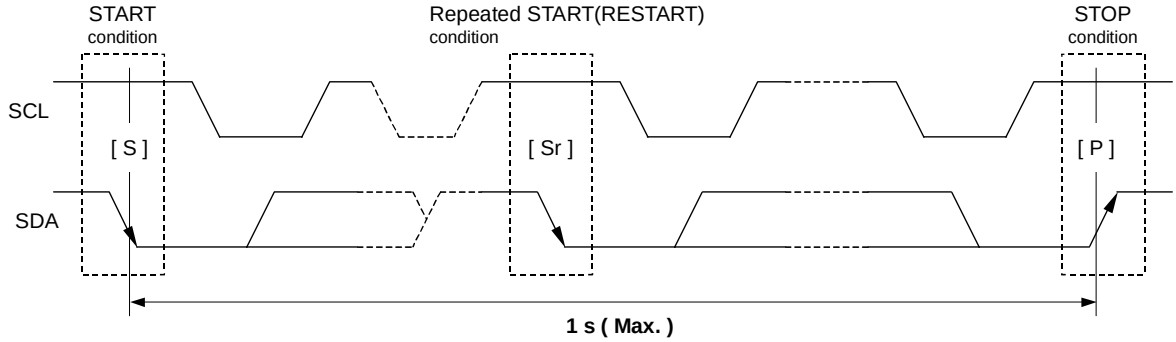
9.9.1. Overview of I²C-BUS

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.
The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is output while the SCL line is at high level.
The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse.

9.9.2. Starting and stopping I²C bus communications



1) START condition, repeated START condition, and STOP condition

(1) START condition
- The SDA level changes from high to low while SCL is at high level.

(2) STOP condition
- This condition regulates how communications on the I²C -BUS are terminated. The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)
- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Caution points

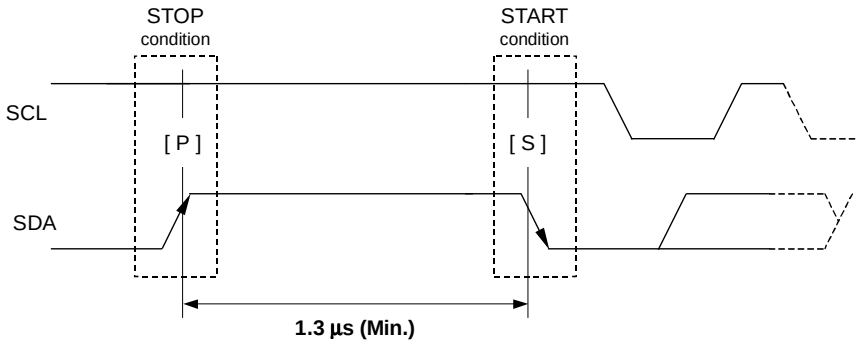
∗1) The master device always controls the START, RESTART, and STOP conditions for communications.

∗2) The master device does not impose any restrictions on the timing by which STOP conditions affect transmissions, so communications can be forcibly stopped at any time while in progress. (However, this is only when this RTC module is in receiver mode (data reception mode = SDA released).

∗3) When communicating with this RTC module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur **within 1 seconds**. (A RESTART condition may be sent between a START condition and STOP condition, but even in such cases the series of operations from transmitting the START condition to transmitting the STOP condition should still occur **within 1 seconds**.)

If this series of operations requires **1 seconds or longer,** the I²C bus interface will be automatically cleared and set to standby mode by this RTC module's bus timeout function. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. (When the read operation is invalid, all data that is read has a value of "1"). Restarting of communications begins with transfer of the START condition again

∗4) When communicating with this RTC module, wait **at least 1.3 µs (see the tBUF rule)** between transferring a STOP condition (to stop communications) and transferring the next START condition (to start the next round of communications).



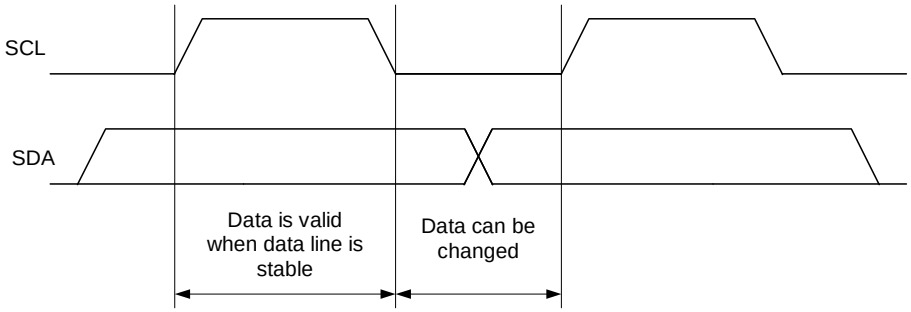
9.9.3. Data transfers and acknowledge responses during I^2C -BUS communications

1) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition. (**However, the transfer time must be no longer than 1 seconds**.)

The address auto increment function operates during both write and read operations.
After address Fh, incrementation goes to address 0h.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) receives data while the SCL line is at high level.

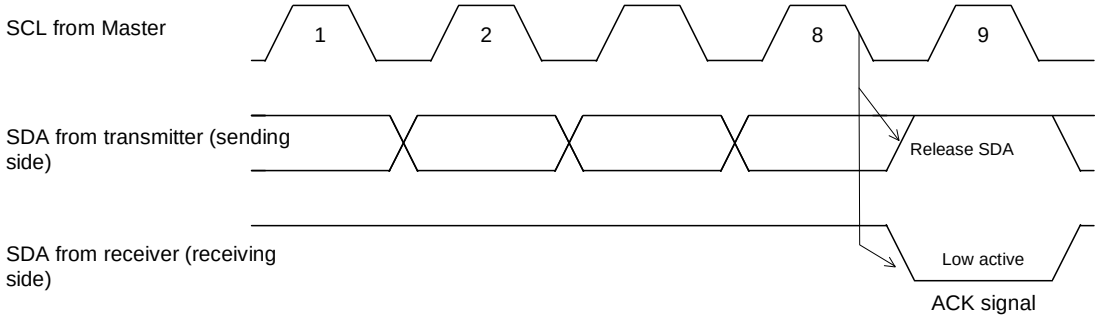


∗ Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

2) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

9.9.4. Slave address

The I^2C-BUS devices do not have any chip select or chip enable pins. All I^2C-BUS devices are memorized with a fixed unique number in it. The chip selection on the I^2C-BUS is executed, when the interface starts, the master device send the required slave address to all devices on the I^2C-BUS. The receiving device only reacts for interfacing, when the required slave address is agreed with its own slave address.

The slave address is 7 bits data that is made of 4 bits fixed data (group 1), and 3 bits data (group 2). As in the RX-8731, the data in group 1 is (1010), group 2 is (00X). The data X in group 2 is given by A0 pin input logic level. The upper 2 bits of group 2 is fixed as (00).

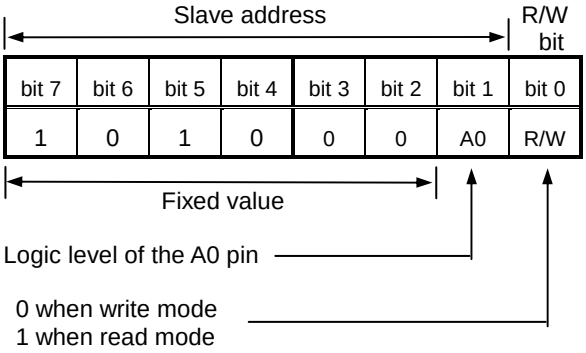
In case, two RX-8731s are installed on a system, it is possible to select each device using A0 terminal logic level. Note that if more RX-8731s are installed, it is possible to access each device by using dynamic control to the A0 pins.

RX-8731 slave address

1	0	1	0	0	0	A0

Group 1 Group 2

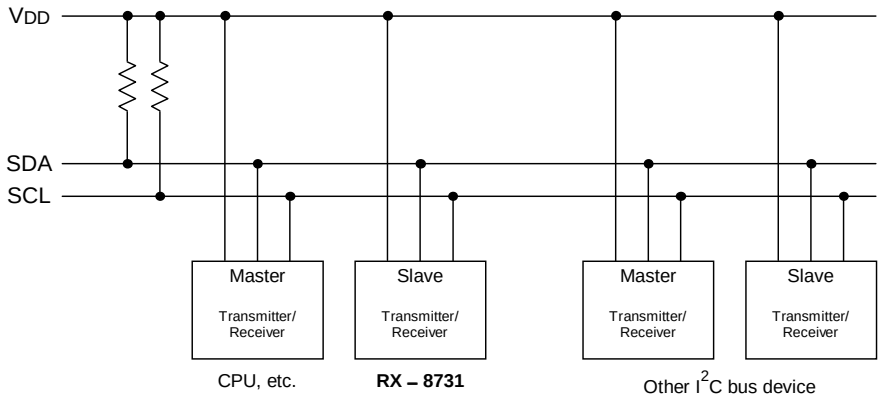
During in actual data transmission, the transmitted data contains the slave address and the data with R/W (read/write) bit.



9.9.5. System configuration

All ports connected to the I^2C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the V_{DD} line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).



Any device that controls the data transmission and data reception is defined as a "Master".
and any device that is controlled by a master device is defined as a “Slave”.
The device transmitting data is defined as a “Transmitter” and the device receiving data is defined as a receiver”

In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

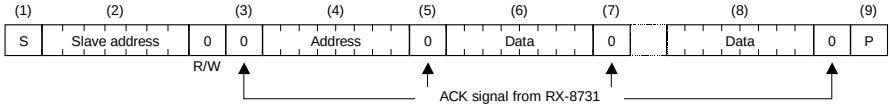
9.9.6. I²C bus protocol

In the following sequence descriptions, it is assumed that the CPU is the master and the RX-8581 is the slave.

1) Address specification write sequence

Since the RX-8731 includes an address auto increment function, once the initial address has been specified, the RX-8731 increments (by one byte) the receive address each time data is transferred.

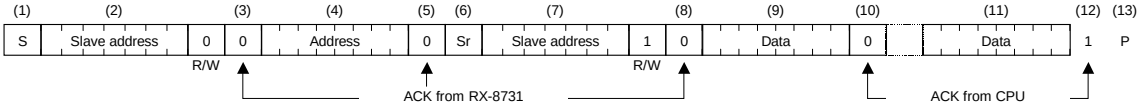
(1) CPU transfers start condition [S].
(2) CPU transmits the RX-8731's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX-8731.
(4) CPU transmits write address to RX-8731.
(5) Check for ACK signal from RX-8731.
(6) CPU transfers write data to the address specified at (4) above.
(7) Check for ACK signal from RX-8731.
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
(9) CPU transfers stop condition [P].



2) Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

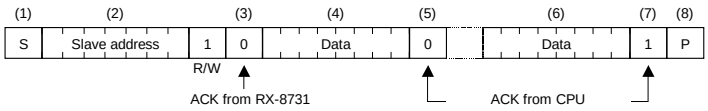
(1) CPU transfers start condition [S].
(2) CPU transmits the RX-8731's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX-8731.
(4) CPU transfers address for reading from 8731.
(5) Check for ACK signal from RX-8731.
(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
(7) CPU transfers RX-8731's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from RX-8731 (from this point on, the CPU is the receiver and the RX-8731 is the transmitter).
(9) Data from address specified at (4) above is output by the RX-8731.
(10) CPU transfers ACK signal to RX-8731.
(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
(12) CPU transfers ACK signal for "1".
(13) CPU transfers stop condition [P].



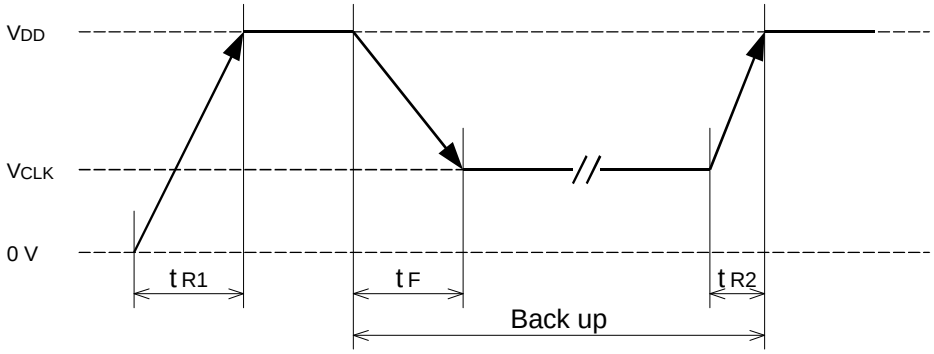
3) Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].
(2) CPU transmits the RX-8731's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from RX-8731 (from this point on, the CPU is the receiver and the RX-8731 is the transmitter).
(4) Data is output from the RX-8731 to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to RX-8731.
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RX-8731.
(7) CPU transfers ACK signal for "1".
(8) CPU transfers stop condition [P].



9.10. Backup and Recovery



Item	Symbol	Min.	Typ.	Max.
Power supply drop time	t_F	2 µs /V		
Initial power-up time	t_{R1}	1 µs /V		100 ms /V
Initial power-up supply Voltage	V_{DD}	1.6 V		5.5 V
Clock maintenance power-up time	t_{R2}	1 µs /V		

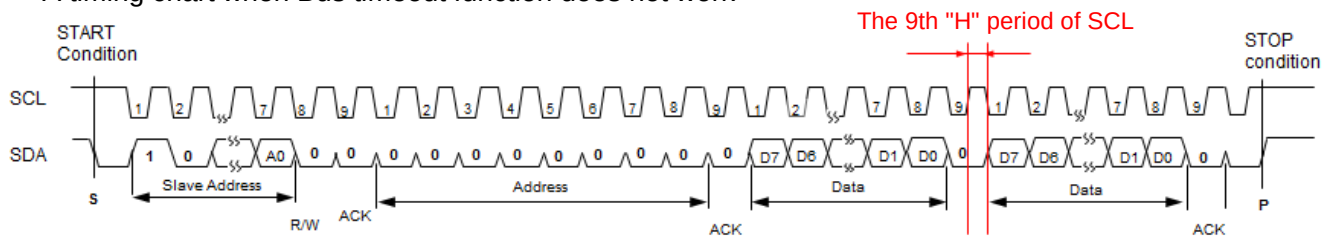
* It is necessary to give initial resetting to have proper opetation of this product. To give initial resetting, surely input initial voltage from (0V) and adjust to get voltage level more than 1.6V after startup.

9.11. Bus timeout function

When communication to RX-8731 continued more than one second, RX-8731 finishes communication automatically, and SDA becomes Hi-z. Communication is a period of STOP condition from START condition. However, if the communication is stopped in ACK processing of the immediately after writing to Address 00h, Bus timeout function does not work even if it passes more than one second, and RX-8731 continues outputting "L".

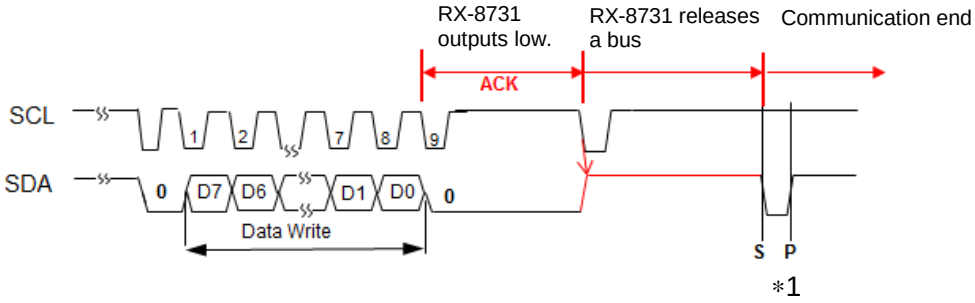
∗ In the case of STOP bit ="1", Bus timeout function does not work.

A timing chart when Bus timeout function does not work



A return method when halted communication during ACK processing

When halt communication during ACK processing, and BUS timeout function does not work, must finish ACK processing. In that case, lower the 9th clock of ACK processing.

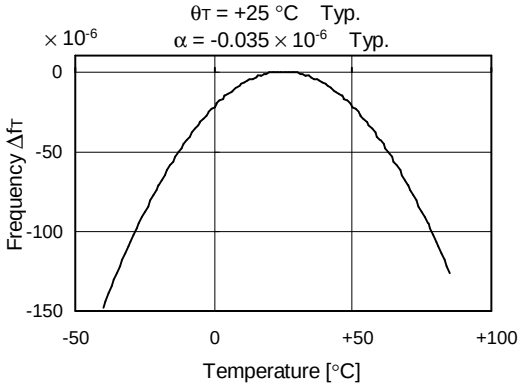


∗1 Only STOP condition transmits and can stop communication.

10. Reference information

10.1. Reference Data

Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta fT = \alpha\ (\theta T - \theta X)^2$

ΔfT		: Frequency deviation in any temperature
α	$(1 / °C^2)$	: Coefficient of secondary temperature $(-0.035 \pm 0.005) \times 10^{-6} / °C^2$
θT	(°C)	: Ultimate temperature (+25±5 °C)
θX	(°C)	: Any temperature

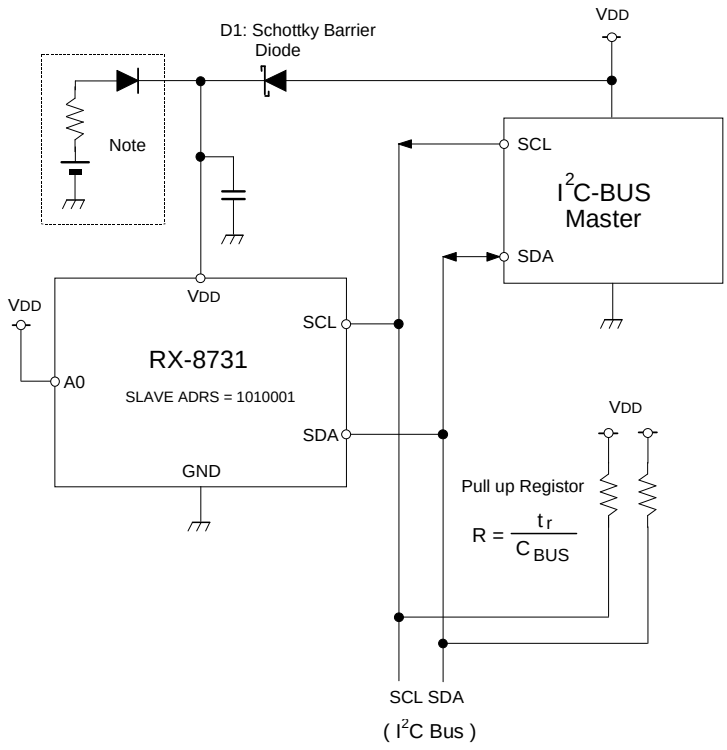
2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta fT + \Delta fV$

$\Delta f/f$	: Clock accuracy (stable frequency) in any temperature and voltage
$\Delta f/fo$	: Frequency precision
ΔfT	: Frequency deviation in any temperature
ΔfV	: Frequency deviation in any voltage

3. How to find the date difference
   Date difference = $\Delta f/f \times 86400$ (seconds)
   * For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

10.2. Connection with Typical Microcontroller



Note : It uses the secondary battery or a lithium battery. When using the seconding battery, the diode is not required. When using the lithium battery, the diode is required.
For detailed value on the resistance, please consult a battery maker.

11. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 µF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.
* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Input voltage

When the voltage of out of the input voltage specifications range input into an input terminal constantly, a penetration electric current occurs. Thus, current consumption increases very much.
This causes Latch-up, and there is the case that, as a result, a built-in IC is destroyed.
Please use an input terminal according to input voltage specifications.
Furthermore, please input the VDD or GND most recent voltage as much as possible.

(4) Disposal of unused input terminals.

When an input terminal is open state, it causes increase of a consumption electric current and the behavior that are instability.
Please fix an unused input terminal to the voltage that is near to VDD or GND.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.
* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Packaging equipment

This product uses a molded package whose back contains glass.
Therefore, it is possible for shocks during packaging to cause product breakage, depending on the packaging machinery and conditions.
Please be sure to check that the load placed on products during packaging is as low as possible (low speeds during loading onto the substrate, low chuck forces, etc.) before using packaging equipment.
Carry out the same checks when changing packaging conditions.
The presence of foreign objects between this product and the packaging substrate may result in product breakage.
Guard against introduction of foreign objects during packaging.
Also, carry out measures to eliminate static electricity during packaging of and operations with this product.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

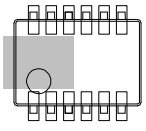
(6) Stop using the glue

Any glue must never use it after soldering RTC to a circuit board.

Fig. 1 : Example GND Pattern

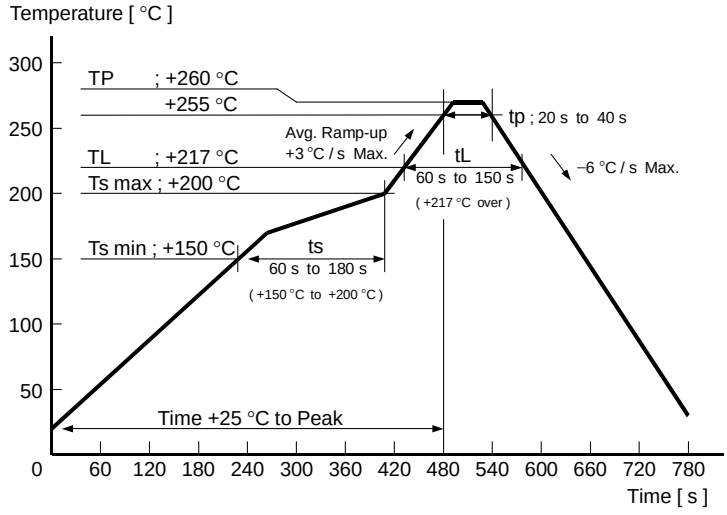
RX – 8731 LC

(VSOJ – 12 pin)



* The shaded part ( ) indicates where a GND pattern should be set without getting too close to a signal line

Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



Application Manual

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