PY32MD530 Datasheet

32-bit ARM® Cortex®-M0+ Microcontroller

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Puya Semiconductor (Shanghai) Co., Ltd.

Features

- Core
  - — 32-bit ARM® Cortex®-M0+
  - — Frequency up to 72 MHz
- Memories
  - — 64 KB Flash memory
  - — 8 KB SRAM
- Clock management
  - — 8 MHz high-speed internal RC oscillator (HSI)
  - — 32.768 kHz low-speed internal RC oscillator (LSI)
  - — 4 to 32 MHz high-speed external crystal oscillator (HSE)
  - — 32.768 kHz Low-speed external crystal oscillator (LSE)
  - — External clock input
  - — PLL (supports 2 to 18 multiplication of HSI or HSE)
- Power management and reset
  - — Operating voltage: 2.0 to 5.5 V
  - — Low-power modes: Sleep/Stop
  - — Power-on/power-down reset (POR/PDR)
  - — Brown-out reset (BOR)
  - — Programmable voltage detector (PVD)
- General-purpose input and output (I/O)
  - — Up to 23 I/Os, all available as external interrupts
  - — All IOs support 50 mA sink current (5 V)
  - — 4 GPIOs supporting high sink current (configurable as 80mA/60mA/40mA/20mA) for driving common-cathode LED digital tubes
- 1 x 12-bit ADC
  - — Up to 7 external channels and 5 internal channels
  - — Support injection mode
  - — Input voltage conversion range: 0 to V_{CC}
  - — Internal voltage: 1.024 V/1.5 V/2.048 V
- Timers
  - — 1 x 16-bit advanced-control timer (TIM1) supporting 144 MHz counting
  - — 4 x 16-bit general-purposed timers (TIM3/TIM14/TIM16/TIM17), where TIM17 supports 144 MHz counting
  - — 1 x low power timer (LPTIM) with 16-bit/32-bit counting and wake-up from low power mode
  - — 1 x independent watchdog timer (IWDG)
  - — 1 x window watchdog timer (WWDG)
  - — 1 x SysTick timer
- RTC
- 3-channel DMA controller
- Communication interfaces
  - — 2 x serial peripheral interface (SPI), 1 with I^2S interface multiplexed
  - — 1 x I^2C interface, supporting Standard mode (100 kHz), Fast mode (400 kHz) and Fast mode plus (1 MHz)
  - — 1 x universal synchronous/asynchronous receiver transmitter (USART) with automatic baud rate detection and LIN capability
  - — 1 x universal asynchronous receiver/transmitter (UART)

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  - — 1 x low-power universal asynchronous receiver/transmitter (LPUART)
- Hardware CRC-32 module
- Built-in multi-function three-phase NN half-bridge gate driver
  - — High-side floating supply absolute voltage: 150 V
  - — Operating voltage: 5.5 to 26 V
  - — Output current: +1 A/-1 A
  - — LDO: 5 V/50 mA
- 2 x comparators
- 2 x operational amplifier/programmable gain amplifier
- Unique UID
- Serial wire debug (SWD)
- Operating temperature: -40 to 105 °C
- Packages: QFN40

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Content

Features **2**
1. Introduction **7**
2. Functional overview **10**
2.1. Arm® Cortex®-M0+ core 10
2.2. Memories 10
2.3. Boot modes 10
2.4. Clock management 11
2.5. Power management 13
2.5.1. Power block diagram 13
2.5.2. Power monitoring 13
2.5.3. Voltage regulator 14
2.5.4. Low-power mode 14
2.6. Reset 15
2.6.1. Power reset 15
2.6.2. System reset 15
2.7. General-purpose inputs and outputs (GPIOs) 15
2.8. DMA 15
2.9. Interrupts and events 16
2.9.1. Nested vectored interrupt controller (NVIC) 16
2.9.2. Extended interrupt/event controller (EXTI) 17
2.10. Analog-to-digital converter (ADC) 17
2.11. Comparators (COMP) 18
2.12. OPA/PGA 18
2.13. Timers 18
2.13.1. Advanced-control timer 19
2.13.2. General-purpose timers 19
2.13.3. Low power timer (LPTIM) 19
2.13.4. Independent watchdog (IWDG) 19
2.13.5. Window watchdog (WWDG) 20
2.13.6. SysTick timer 20
2.14. Real-time clock (RTC) 20
2.15. Cyclic redundancy check calculation unit (CRC) 20
2.16. System configuration controller (SYSCFG) 20
2.17. Debug support (DBG) 21
2.18. Inter-integrated circuit interface (I^2C) 21
2.19. Serial peripheral interface (SPI) 22
2.20. Universal Asynchronous Receiver/Transmitter (UART) 23
2.21. Low-power universal asynchronous receiver/transmitter (LPUART) 23
2.22. Universal synchronous/asynchronous receiver/transmitter (USART) 24

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2.23. SWD 25
3. Pinouts and pin descriptions 26
3.1. Alternate functions selected through GPIOA_AFR registers for port A 34
3.2. Alternate functions selected through GPIOB_AFR registers for port B 35
3.3. Alternate functions selected through GPIOF_AFR registers for port F 35
4. Memory mapping 36
5. Electrical characteristics 40
5.1. Parameter conditions 40
5.1.1. Minimum and maximum values 40
5.1.2. Typical values 40
5.2. Absolute maximum ratings 40
5.3. Operating conditions 41
5.3.1. General operating conditions 41
5.3.2. Operating conditions at power-on/power-down 41
5.3.3. Embedded reset and PVD module characteristics 41
5.3.4. Supply current characteristics 43
5.3.5. Wakeup time from low-power mode 46
5.3.6. External clock source characteristics 47
5.3.7. High-speed internal (HSI) RC oscillator 49
5.3.8. Low-speed internal (LSI) RC oscillator 50
5.3.9. Phase locked loop (PLL) characteristics 50
5.3.10. Memory characteristics 50
5.3.11. ESD & LU characteristics 50
5.3.12. I/O port characteristics 51
5.3.13. ADC characteristics 52
5.3.14. Comparator characteristics 53
5.3.15. Operational amplifier characteristics 54
5.3.16. Temperature sensor characteristics 55
5.3.17. Embedded voltage reference characteristics 55
5.3.18. COMP voltage reference buffer characteristics (6-bit DAC) 56
5.3.19. Timer characteristics 56
5.3.20. Communication interfaces 57
5.4. Multifunction gate driver electrical characteristics 61
5.4.1. Drive logic control 61
5.4.2. Switching time 61
5.4.3. Shoot-through protection 61
5.4.4. Dead time function 62
5.4.5. Absolute maximum ratings 62
5.4.6. Recommended operating conditions 63
5.4.7. Electrical characteristics 63

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6. Application circuit 65
7. Package information 66
7.1. QFN40 package size 66
8. Ordering information 67
9. References 68
10. Version history 69

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1. Introduction

The PY32MD530 microcontrollers feature the high-performance ARM® 32-bit Cortex®-M0+ core operating at up to 72 MHz frequency, embed up to 64 KB Flash and 8 KB SRAM, and are available in multiple package options. The PY32MD530 integrates multi-channel I^2C, SPI, USART, LPUART and other communication peripherals, one 12-bit ADC, five 16-bit timers, two comparators and two operational amplifiers or programmable gain amplifiers.

In addition, the PY32MD530 integrates a 3-phase NN pre-driver with 150 V maximum voltage capability for driving external MOSFETs or IGBTs. The PY32MD530 has a built-in 5 V LDO, which can meet the 5 V power supply requirements of the MCU.

The PY32MD530 microcontrollers operates across a temperature range of -40 to 105 °C and a voltage range of 2.0 to 5.5 V. It provides Sleep and Stop modes to meet the needs of different low-power applications.

The PY32MD530 microcontrollers are suitable for drive control of 5.5 to 26 V input 3-phase/single-phase BLDC/PMSM and servo motors. Common application scenarios are listed as follows: cooling fans, power tools, low-voltage vacuum cleaners, high-speed fans, joint motors, low-voltage water pump motors, etc.

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Table 1-1 PY32MD530 series product features and peripheral counts

Peripherals		PY32MD530H28U7
Flash (KB)		64
SRAM (KB)		8
Timers	Advanced-control	1
	General-purpose	4
	Low power	1
	SysTick	1
	Watchdog	2
Comm. interfaces	SPI (I^2S)	2(1)
	UART	1
	USART	1
	LPUART	1
	I^2C	1
DMA		3ch
RTC		Yes
GPIOs		23
ADC (external + internal)		7+5
LED COM		4
LCD COM		23
Comparators		2
OPA/PGA		2
Max. CPU frequency		72 MHz
Operating voltage		2.0 to 5.5 V
Operating temperature		-40 to 105 °C
Packages		QFN40

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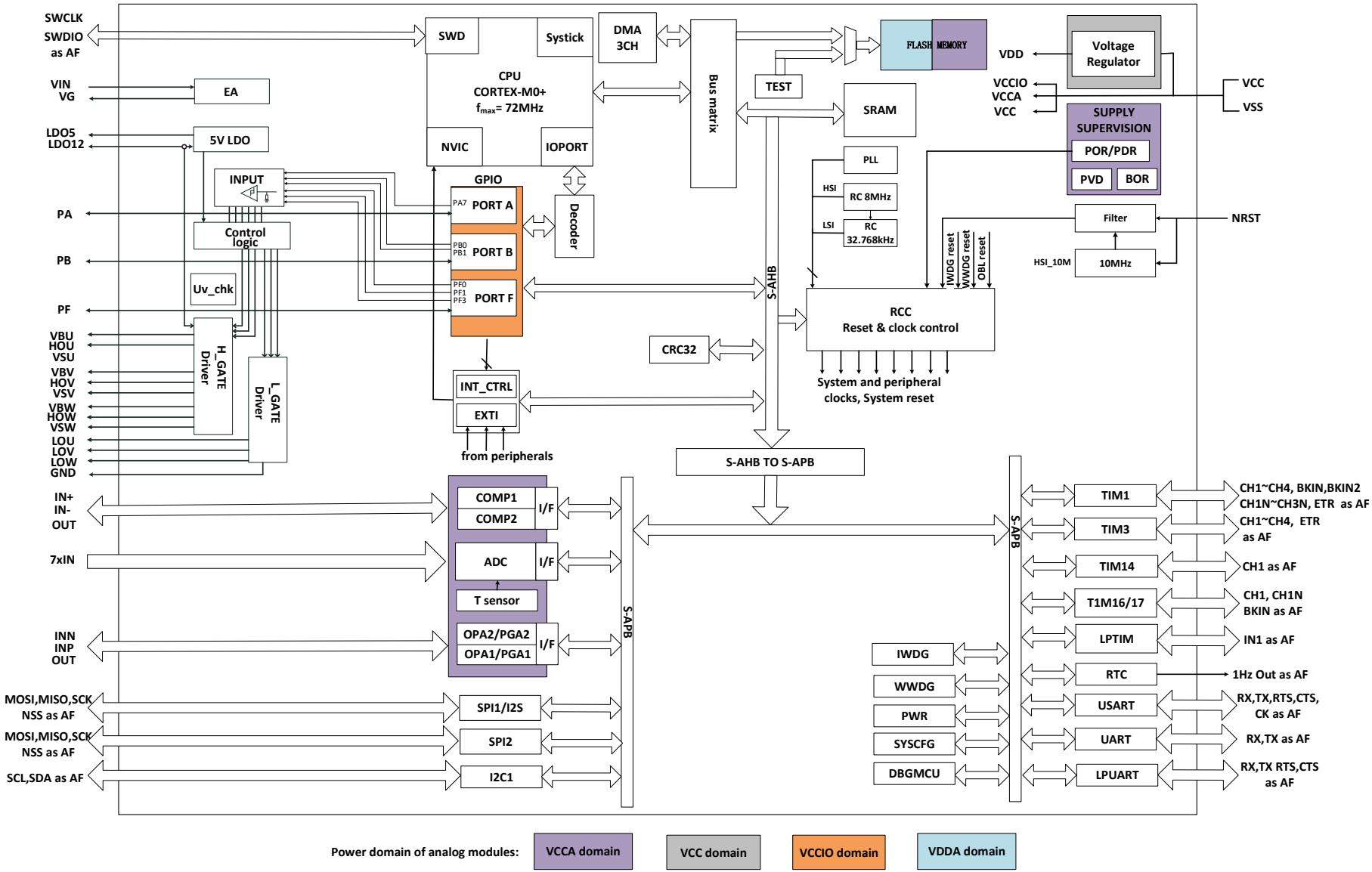


Figure 1-1 System block diagram

2. Functional overview

2.1. Arm® Cortex®-M0+ core

The Arm® Cortex®- M0+ is an entry-level Arm 32-bit Cortex processor designed for embedded applications. It provides developers with significant benefits, including:

- Simple architecture for easy learning and programming
- Ultra-low power consumption for energy-efficient operation
- Reduced code density

The Arm® Cortex®-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. It delivers high performance through a streamlined instruction set and hardware enhancements like a single-cycle multiplier, while achieving higher code density than other 8/16-bit MCUs.

The Arm® Cortex®-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC).

2.2. Memories

Embedded SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits).
The Flash memory is composed of two distinct physical areas:

- The Main flash area consists of application and user data
- 384 bytes of Information area:
  - — Option bytes
  - — UID bytes
  - — User data bytes
  - — System memory

The protection of Main flash area includes the following mechanisms:

- Read protection (RDP) blocks external access.
- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 4 KB.
- Option byte write protection is a special design for unlock.
- proprietary code read out protection (PCROP)
- Security protection (SECPROT), for securing protected areas.

2.3. Boot modes

At startup, the BOOT0 pin, the boot configuration bit nBOOT1 and BOOT_LOCK (both stored in option bytes) are used to select one of the three boot options in the following table:

Table 2-1 Boot configuration

BOOT_LOCK	Boot mode configuration		Mode
	nBOOT1 bit	BOOT0 pin	
1	X	X	Forced boot from Main flash
0	X	0	Boot from Main flash
0	1	1	Boot from System memory
0	0	1	Boot from SRAM

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2.4. Clock management

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. After the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- An 8 MHz internal high-precision HSI clock.
- A 32.768 kHz configurable internal LSI clock.
- A 4 to 32 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI. A CPU NMI interrupt is generated at the same time.
- A 32.768 kHz LSE clock, and used to enable the CSS function to detect the LSE. If CSS fails, the hardware will automatically convert the system clock to LSI, and software configures the LSI frequency. Simultaneously, CPU NMI interrupt is generated.
- PLL clock has HSI and HSE sources. If the HSE source is selected, when CSS is enabled and CSS fails, the PLL and HSE will be turned off, and the hardware selects the system clock source as HSI.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The maximum frequency of the AHB and the APB domains is 72 MHz.

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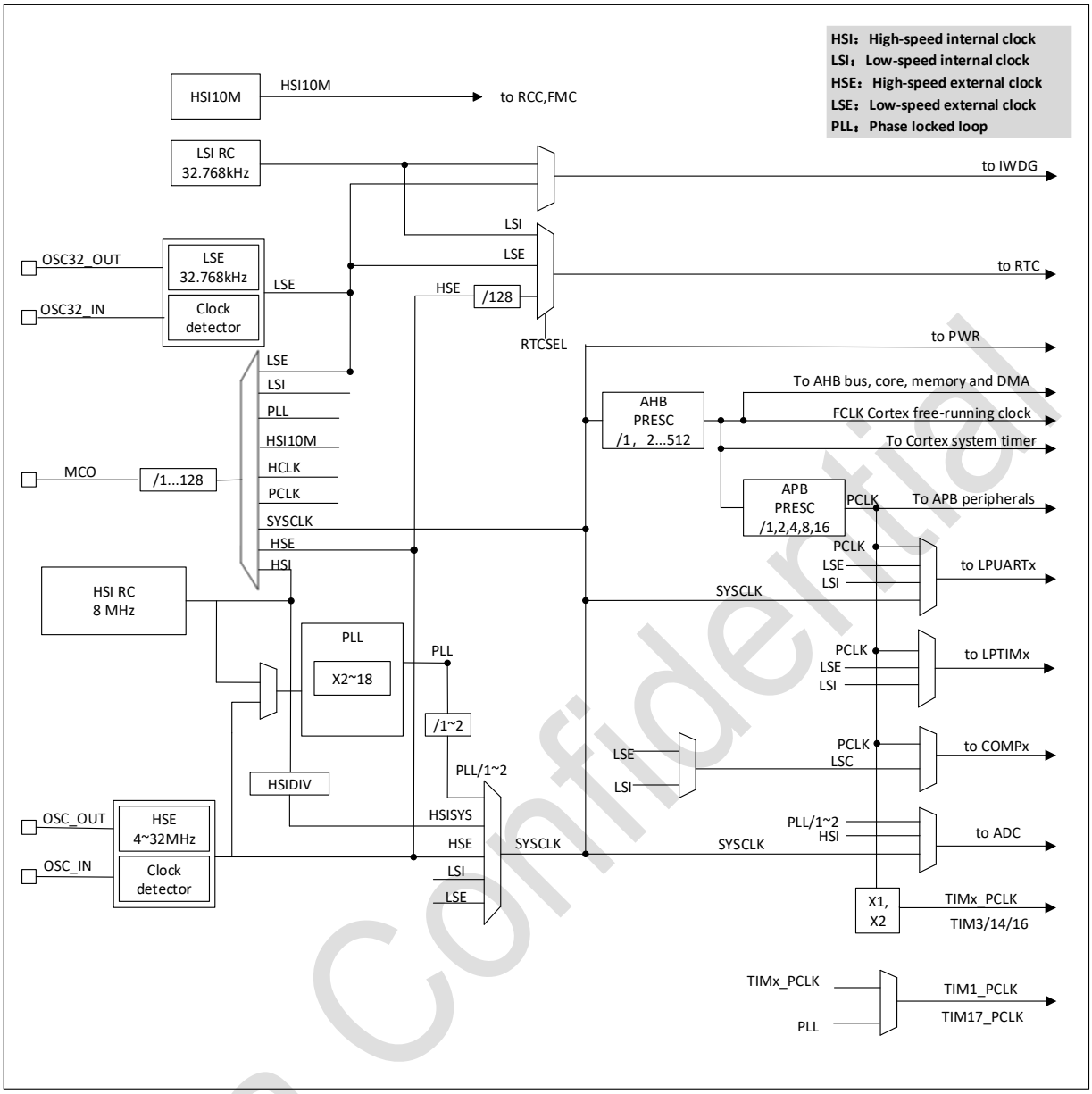


Figure 2-1 System clock structure diagram

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2.5. Power management

2.5.1. Power block diagram

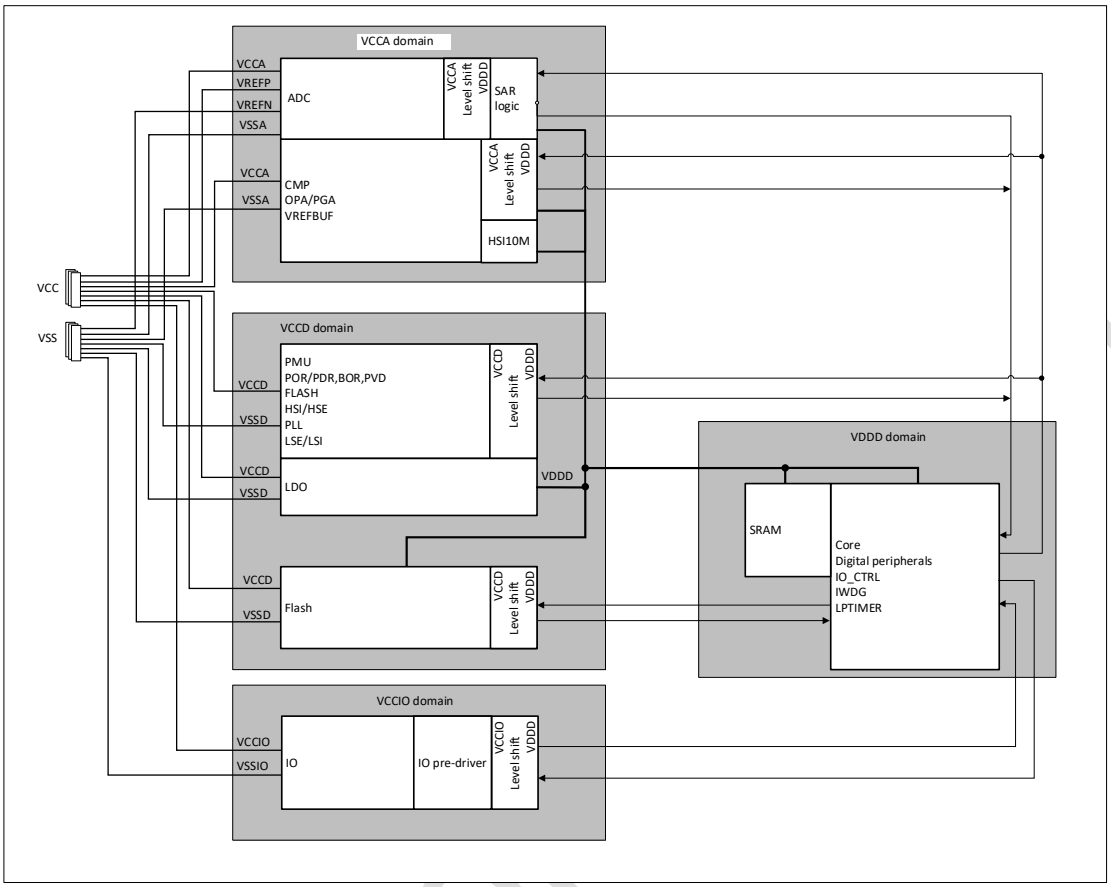


Figure 2-2 Power block diagram

Table 2-2 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	2.0 to 5.5 V	The power is supplied to the chip through the power pins, with the power supply module comprising: Partial analog circuits
2	V_{CCA}	2.0 to 5.5 V	Powers for most analog modules, sourced from the V_{CC} PAD (a dedicated power PAD can also be designed separately).
3	V_{CCIO}	2.0 to 5.5 V	Power to IO from V_{CC} PAD
4	V_{DDD}	1.2 V	VR supplies power to the main logic circuits (CPU, bus, RCC, PWR and peripheral IPs) and SRAM inside the device. When the MR is powered, it outputs 1.2 V. When entering Stop mode, the software configures DLPR mode.

2.5.2. Power monitoring

2.5.2.1. Power on reset/Power down reset (POR/PDR)

The POR/PDR module, which provides power-on and power-down reset, remains active in all modes.

2.5.2.2. Brown-out reset (BOR)

In addition to POR/PDR, BOR (Brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte.

When the BOR is turned on, the BOR threshold can be selected by the option byte.

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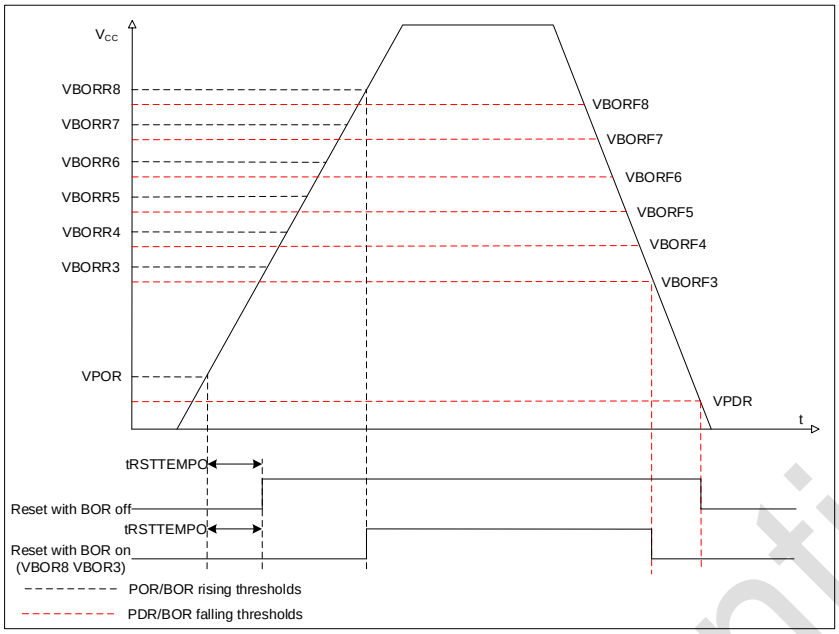


Figure 2-3 POR/PDR/BOR threshold

2.5.2.3. Programmable voltage detector (PVD)

Programmable voltage detector (PVD) module can be used to detect the V_{CC} power supply and the detection point is configured through the register. When V_{CC} is higher or lower than the detection point of PVD, the corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when V_{CC} rises above the detection point of PVD, or V_{CC} falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

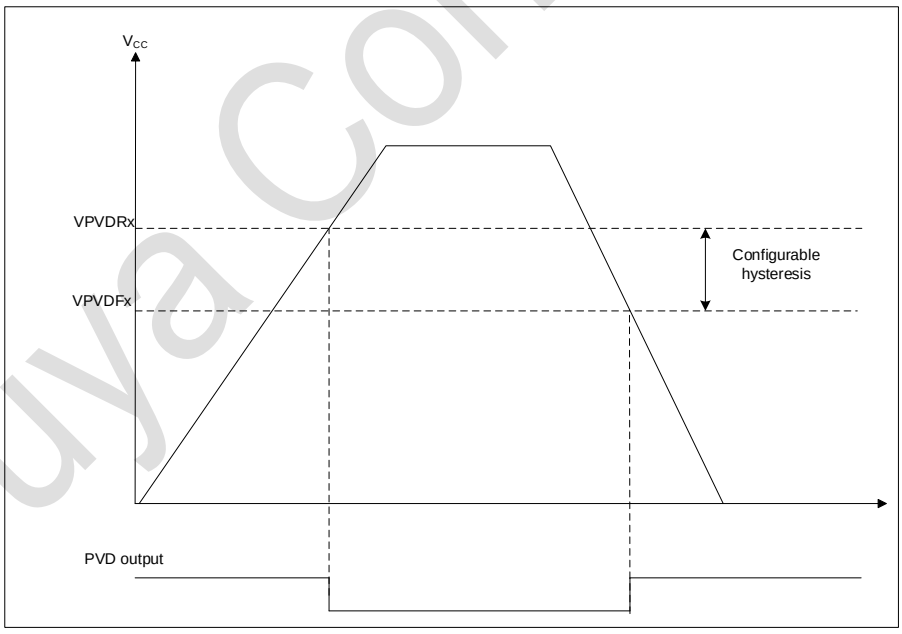


Figure 2-3 PVD threshold

2.5.3. Voltage regulator

The regulator has two operating modes:

- Main regulator (MR) is used in Run mode.
- Deep low power regulator (DLPR) ensures the lowest power consumption in Stop mode.

2.5.4. Low-power mode

In addition to the Run mode, the device has two low-power modes:

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- Sleep mode: peripherals can be configured to keep working when the CPU HCLK clock is off (NVIC, SysTick, etc. are operating). (It is recommended to enable only essential modules and disable them after task completion). The V_{DDD} regulator is in MR mode.
- Stop mode: The high-speed clocks (PLL, HIS, HSE) are disabled, while LSI and LSE can be enabled or disabled based on the wake-up source. The working mode of V_{DDD} regulator needs to be configured to DLPR mode.

2.6. Reset

Two resets are designed in the chip: power reset and system reset.

2.6.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out reset (BOR)

2.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load (OBL) reset

2.7. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating, pull-up or pull-down and analog) or as peripheral alternate function. The I/O configuration can be locked and can be configured LCD 1/2 Bias output.

- Support read/write operations via IO Port or AHB bus
- Output states: push-pull or open drain + pull-up/down
- Output data from output data register (GPIOx_ODR) or peripheral (alternate function output)
- Speed selection for each I/O
- Input states: floating, pull-up/down, analog
- Input data to input data register (GPIOx_IDR) or peripheral (alternate function input)
- Bit set and reset register (GPIOx_BSRR) for bitwise write access to GPIOx_ODR
- Locking mechanism (GPIOx_LCKR) provided to freeze the I/O port configurations
- Analog function
- Alternate function selection registers (Max. 16 alternate functions for each IO)
- Fast toggle capable of changing every clock cycles
- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several peripheral functions
- Configurable LCD 1/2 Bias output

2.8. DMA

Direct memory access (DMA) is used to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations. The DMA controller have 3 channels

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in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 3 configurable channels
- Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
- Priority between multiple requests on the same DMA module is software-programmable. For equal priorities, hardware resolves conflicts (lower channel number = higher priority).
- The transfer sizes of the source and destination are independent (byte, half word and word), simulating packing and unpacking. Source and destination addresses must be aligned to the transfer width.
- Programmable address modes: Increment, decrement, or fixed.
- Each channel has 4 event flags: transfer complete (circular mode), block transfer, half-block transfer and transfer error. They are logically ORed to generate a single interrupt request.
- Support transfers between memory to memory, peripheral to memory, memory to peripheral and peripheral to peripheral.
- SRAM, APB and AHB peripherals can act as source or destination. Flash can only act as a source.
- Support single-trigger mode and four circular modes:
  - Peripheral address retained, memory address retained
  - Peripheral address reloaded, memory address retained
  - Peripheral address retained, memory address reloaded
  - Both addresses reloaded
- Single-trigger mode: Programmable transfer count (0 to 65,535)
- Circular mode: Infinite looping or finite looping (1 to 255)
- Support single transfer and bulk transfer
  - Single transfer: Generates 1 ACK per data transfer.
  - Bulk transfer: Generates 1 ACK after all configured data is transferred (bus released post-completion).
- Two transfer modes
  - Fast mode: Holds the bus until all data is transferred.
  - Round-robin mode: Releases the bus after each transfer for re-arbitration.
- Support pausing transfers upon entering the block transfer Complete interrupt in circular mode.

2.9. Interrupts and events

The PY32MD530 handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.9.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

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If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Support 1 NMI
- Supports 27 maskable external interrupts (excluding 16 CPU interrupts).
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.9.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from Sleep/Stop mode.

The EXTI controller has multiple channels, including up to 23 GPIOs that can be connected to the 16 EXTI lines, 2 COMP outputs, and RTC/I^2C/LPUART wake-up signals. GPIO and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI 0 to 15 channel through the select signal.

- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.10. Analog-to-digital converter (ADC)

The device has a 12-bit SAR-ADC. The module has a total of up to 12 channels to be measured, including 7 external and 5 internal channels. The internal voltage reference: V_{REFBUF} (1.024V, 1.5 V, 2.048 V, 2.5 V) or the power supply voltage.

Internal channels include T_S, V_{REFINT}, V_{CC}/3, OPA1 and OPA2.

- A/D conversion of the various channels can be performed in single, continuous, or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.
- The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.
- Interrupt generation at ADC ready, the end of sampling, the end of conversion, end of sequence conversion, analog watchdog or overrun events
- The ADC is configurable with 12/10/8/6-bit resolutions.
- Maximum ADC sampling rate: 3 Msps
- Support self-calibration (initiated by software)
- Support programmable sampling time
- The data register allows configurable data alignment
- Support DMA requests for regular channel data conversion
- Support configurable conversion of 16 regular channels
- Support configurable conversion of 4 injected sequences

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2.11. Comparators (COMP)

The device integrates two general-purpose comparators (COMP), namely COMP1 and COMP2. The COMP1/2 module can be used as a separate module or in combination with timer.

The COMP features:

- Triggered by analog signal to wake-up function from low-power mode
- Analog signal conditioning
- Cycle by cycle current control loop when comparators are connected with PWM output from timer
- Voltage comparison function is supported. Each comparator has configurable positive or negative input for flexible voltage selection:
  - Multiple I/O pins
  - 64 steps voltage of V_{CC}/V_{REFBUF}
  - Temperature sensor output
  - OPA1/OPA2 output
  - V_{REFINT}
- Programmable speed and power consumption
- Programmable hysteresis function
- Write protection for configuration registers (LOCK function)
- The output can be triggered by a connection to the I/O or timer input
- Each COMP has interrupt generation capability and is used to wake up the chip from low power mode (Sleep/Stop) (via EXTI)
- Provides software to configure the digital filtering time to enhance the anti-interference capability of the chip
- It supports output blanking to reduce switching noise.
- Support the Window Comp function

2.12. OPA/PGA

The OPA1/2 modules can be flexibly configured for simple filter and buffer applications.

- Two independently configured operational amplifier
- The inputs can be individually configured to select from one channel, and the outputs can be configured to select from one IO channel. The outputs can be internally directed to the comparator and ADC.
- The input range of the OPA is from 0 to V_{CC}, and the output range is from 0.2 V to V_{CC}-0.2 V.
- Can be configured for the following modes
  - General operational mode (general purpose OPA)
  - Programmable gain amplifier

2.13. Timers

The different timers feature as blow:

Table 2-3 Timer characteristics

Type	Timer	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Complementary outputs
Advanced-control	TIM1	16-bit	up, down, up/down	1 to 65536	Yes	4	3
General-purpose	TIM3	16-bit	up, down, up/down	1 to 65536	Yes	4	-
	TIM14	16-bit	up	1 to 65536	-	1	-

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Type	Timer	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Complemen-tary outputs
	TIM16,TIM17	16-bit	up	1 to 65536	Yes	1	1

2.13.1. Advanced-control timer

The advanced-control timer (TIM1) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output
- PWM phase shift function

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, TIM1/TIM8 have full modulation capability (0 to 100%).

TIM1 supports 144 MHz counting.

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the Timer Link feature for synchronization or event chaining.

TIM1 supports the DMA function.

2.13.2. General-purpose timers

The general-purpose timers TIM3/TIM14/TIM16/TIM17 are consist of 16-bit auto-reload counters driven by a prescaler.

TIM14/TIM16/TIM17 features one single channel for input capture/output compare, PWM or one-pulse mode output.

TIM3 features four single channel for input capture/output compare, PWM or one-pulse mode output

The TIM17 supports 144 MHz counting.

The counter can be frozen in debug mode.

2.13.3. Low power timer (LPTIM)

LPTIM is a 16-bit timer. The ability of LPTIM to wake the system from low-power modes makes it suitable for practical low-power applications. LPTIM introduces a flexible clock scheme that can provide the required functionality and performance while minimizing power consumption.

- LPTIM is a 16-bit increment counter
- It has a 3-bit prescaler with 8 possible division factors (1, 2, 4, 8, 16, 32, 64, 128)
- Optional clocks include LSE, LSI, APB clock, or an external clock source
- Support single-shot and continuous modes
- Support software/hardware input triggering
- The counter can be frozen in debug mode.

2.13.4. Independent watchdog (IWDG)

Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

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The IWDG is clocked by LSI or LSE, so even if the main clock fails, it can keep working.

The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, but have lower timing accuracy constraints.

The IWDG hardware mode can be enabled by option byte.

IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.

The counter can be frozen in debug mode.

2.13.5. Window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

2.13.6. SysTick timer

SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.14. Real-time clock (RTC)

The RTC is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

- RTC is a 32-bit programmable counter with a prescaler factor of up to 2^{20} bits.
- The RTC counter clock source can be LSE, LSI, HSE/128.
- LSI or LSE can be selected as the working clock in Stop mode.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).
- RTC supports clock calibration.
- RTC can be frozen in debug mode.

2.15. Cyclic redundancy check calculation unit (CRC)

CRC computing unit is based on a fixed generation polynomial to obtain 32-bit CRC computing results. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage. The CRC calculation unit contains a 32-bit data register:

- Using CRC-32 (Ethernet) polynomial: 0x4C11DB7
- Supports 32-bit data input
- Single input/output 32-bit data and result output share a single register
- General-purpose 8-bit registers (can be used as temporary storage).
- Calculation time: 4 AHB clocks for 32 bits data

2.16. System configuration controller (SYSCFG)

The SYSCFG module provides the following functions:

- Enable and disable I^2C type IO filter
- Mapping the initial program area according to different boot modes
- DMA peripheral channel selection control
- Analog input channel enable

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- Analog input channel switch enabled (PA9/PA10)
- Enable and disable Noise filter for all GPIOs
- Enable and disable PVD Lock
- Enable and disable Cortex-M0+ LOCKUP

2.17. Debug support (DBG)

The MCU DBG module assists the debugger with the following functions:

- Support Sleep and Stop mode
- When the CPU enters the HALT mode, the control timer or watchdog stops counting or continues counting
- Prevent I^2C bus timeout during HALT mode

The MCUDBG register also provides chip ID encoding. This ID encoding can be accessed by a SW debug interface, or by a user program.

2.18. Inter-integrated circuit interface (I^2C)

The I^2C (Inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode plus (Fm+).

I^2C features:

- Support Slave and Master mode
  - Support different communication speeds
  - Standard mode (Sm): up to 100 kHz
  - Fast Mode (Fm): up to 400 kHz
  - Fast mode plus (Fm+): up to 1 MHz
- As master
  - Generate clock
  - Generation of start and stop
- As slave
  - Programmable I^2C address detection
  - Discovery of the Stop bit
- 7-bit/10-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I^2C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disabled)
- Optional clock stretching
- Software reset

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- Analog noise filter function
- Low-power address matching wake-up

2.19. Serial peripheral interface (SPI)

The serial peripheral interface (SPI) protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also operate in a multi-master configuration, and only SPI1 supports I^2S

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- Master mode frequency up to 36 MHz
- Slave mode frequency up to 24 MHz
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Support Motorola and TI mode
- Interrupt-causing Master mode faults, overrun errors and CRC errors
- Two embedded Rx and Tx FIFOs with DMA capability, depth of four, and width of 16 bits (8 bits when data frame is set to 8 bits)

I^2S features:

- Half-duplex communication (only transmitter or receiver)
- Master or slave operations
- 8-bit programmable linear prescaler to reach accurate audio sample frequencies (from 8 kHz to 192 kHz)
- Data format may be 16-bit, 24-bit or 32-bit
- Packet frame is fixed to 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit, 32-bit data frame) by audio channel
- Programmable clock polarity (steady state)
- Underflow flag in slave transmit mode and Overflow flag in master/slave receive mode
- 16-bit register for transmission and reception with one data register for both channel sides
- Support I^2S protocols:
  - I^2S Phillps standard
  - MSB-justified standard (left-justified)
  - LSB-justified standard (right-justified)
  - PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)

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- Data direction is always MSB first
- DMA capability for transmission and reception
- Master clock may be output to drive an external audio component. Ratio is fixed at 256 × fs (where fs is the audio sampling frequency)

2.20. Universal Asynchronous Receiver/Transmitter (UART)

Universal Asynchronous Receivers/Transmitter (UART)

- Support 5/6/7/8/9-bit serial data
- Support 1/2 STOP bits (1/1.5 STOP bits for 5-bit data)
- Support sending address/data
- Support fixed parity check
- Support break frames
- Detect start bit errors
- Support programmable fractional baud rates
- Support Tx/Rx pin swapping
- Support MSB FIRST endianness switching
- Full-duplex asynchronous communication
- NRZ standard format
- Support DMA transmission
- Support 4-bit fractional baud

2.21. Low-power universal asynchronous receiver/transmitter (LPUART)

Low-power universal asynchronous receivers/transmitters (LPUART) supports:

- Full-duplex asynchronous communication
- NRZ standard mode
- Programmable baud rate
- 32.768 kHz clock with baud rate range 300 to 9600; higher rates need higher clock freq
- Dual clock domains: PCLK and dedicated kernel clock
- Configurable word length (7/8/9 bits)
- Configurable MSB or LSB first shifting
- Configurable stop bits (1/2 bit)
- Single-wire half-duplex communication
- Support continuous DMA transfer
- Independent enable for transmission and reception
- Independent polarity control for Tx/Rx signals
- Interchangeable Tx/Rx pins
- Support hardware RS-485/modem flow control
- Parity control: generates parity bit on transmission, checks on reception
- Transfer detection flag
  - Busy flag
  - End of transmission flags
- Four error detection flags:

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  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- Interrupt sourcrs with flags:
  - CTS change
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Error detection
  - Match address byte
- Support 7/8/9-bit serial data
- Support wake-up from Stop/Sleep modes

2.22. Universal synchronous/asynchronous receiver/transmitter (USART)

The USART provides a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

To distinguish it from the UART described in Section 2.20, the term SCI is used in this section to refer to the asynchronous mode of the USART.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baud rate detection
- Programmable data length of 8 or 9 bits
- Configurable Stop bits (1 or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control

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- Receive/transmit bytes by DMA buffer
- Transfer detection flag
  - Receive buffer full
  - Send empty buffer
  - End of transmission flags
- Parity control
  - Transmit parity bit
  - Check the received data byte
- Configurable Tx and Rx pin SWAP
- MSB First data transmission and reception format
- Support LIN master transmit sync break and slave detect break
  - Generates 13-bit break and detects 10/11-bit breaks when configured for LIN
- Flagged interrupt sources
  - CTS change
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Error detection
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

2.23. SWD

An ARM SWD interface allows serial debugging tools to be connected to the PY32MD530.

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3. Pinouts and pin descriptions

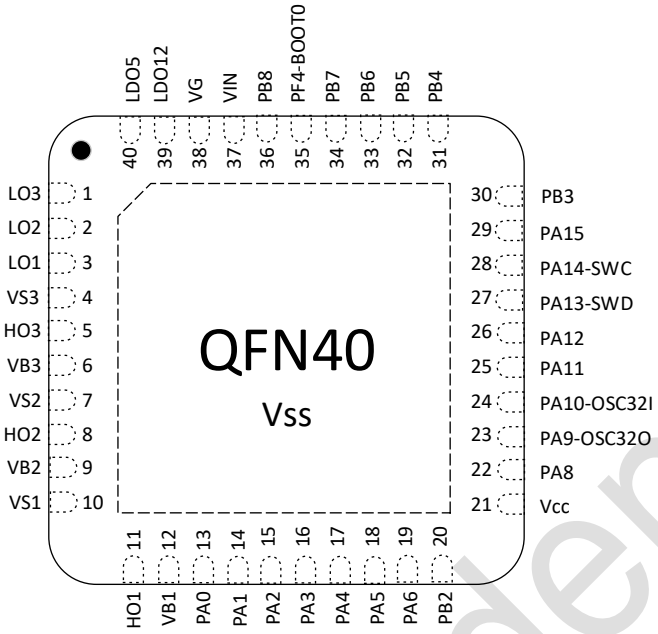


Figure 3-1 QFN40 Pinout2 PY32MD530H2xU7（Top view）

Table 3-1 Legend/abbreviations used in the pinout table

Type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I/O	Input/output pin
		NC	No internal connection
I/O structure		COM	Standard 5 V I/O supports analog input/output functions
		NRST	Bidirectional reset pin with embedded weak pull-up resistor
		COM_T	Tolerant port, allows input voltage range greater than V_{CC}, supports analog input/output functions
		COM_L	LED COM port supports analog input/output functions
Notes		-	Unless otherwise specified, all ports are used as floating inputs be- tween and after reset
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers

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Table 3-2 Legend/abbreviations used for the Gate Driver pin definitions

Packages	Pin name	Pin function
QFN40 H2		
1	LO3	Channel 3 low-side gate driver output
2	LO2	Channel 2 low-side gate driver output
3	LO1	Channel 1 low-side gate driver output
4	VS3	Channel 3 high-side floating reference ground
5	HO3	Channel 3 high-side gate driver output
6	VB3	Channel 3 high-side floating power supply
7	VS2	Channel 2 high-side floating reference ground
8	HO2	Channel 2 high-side gate driver output
9	VB2	Channel 2 high-side floating power supply
10	VS1	Channel 1 high-side floating reference ground
11	HO1	Channel 1 high-side gate driver output
12	VB1	Channel 1 high-side floating power supply
37	V_{IN}	Input operating power supply, externally connected to a 1 μF capacitor to ground
38	VG	12 V LDO gate
39	LDO12	LDO12 input/output pin
40	LDO5	LDO5 output pin

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Table 3-3 Pin definitions

Packages	Reset	Driver	Pin type	I/O structure	Notes	Pin functions	
QFN40 H2						Alternate functions	Additional functions
1	PB1	LO3	-	-	-	TIM1_CH3N	-
2	PB0	LO2	-	-	-	TIM1_CH2N	-
3	PA7	LO1	-	-	-	TIM1_CH1N	-
4	-	VS3	-	-	-	-	-
5	PF0	HO3	-	-	-	TIM1_CH3	-
6	-	VB3	-	-	-	-	-
7	-	VS2	-	-	-	-	-
8	PF1	HO2	-	-	-	TIM1_CH2	-
9	-	VB2	-	-	-	-	-
10	-	VS1	-	-	-	-	-
11	PF3	HO1	-	-	-	TIM1_CH1	-
12	-	VB1	-	-	-	-	-
13	PA0	-	I/O	COM	-	SPI2_SCK USART1_CTS LPUART_CTS COMP1_OUT UART1_TX SPI1_MISO/I2S1_MCK TIM1_CH3 TIM1_CH1N IR_OUT	ADC_IN0 COMP1_INM COMP1_OUT
14	PA1	-	I/O	COM	-	SPI1_SCK/I2S1_CK USART1_RTS LPUART_RX LPUART_RTS EVENTOUT UART1_RX SPI1_MOSI/I2S1_SD TIM3_ETR TIM1_CH4 TIM1_CH2N MCO	COMP1_INP ADC_IN1
15	PA2	-	I/O	COM	-	SPI1_MOSI/I2S1_SD USART1_TX UART1_TX LPUART_RX	COMP2_INM ADC_IN2 COMP2_OUT

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Packages	Reset	Driver	Pin type	I/O structure	Notes	Pin functions	
QFN40 H2						Alternate functions	Additional functions
						COMP2_OUT	
						SPI1_SCK/I2S1_CK	
						I2C_SDA	
						TIM3_CH1	
16	PA3	-	I/O	COM	-	SPI2_MISO	COMP2_INP ADC_IN3
						USART1_RX	
						UART1_RX	
						EVENTOUT	
						SPI1_MOSI/I2S1_SD	
						I2C_SCL	
						TIM1_CH1	
17	PA4	-	I/O	COM	-	SPI1_NSS/I2S1_WS	ADC_IN4
						USART1_CK	
						SPI2_MOSI	
						TIM14_CH1	
						LPUART_TX	
						EVENTOUT	
						UART1_TX	
						TIM3_CH3	
						RTC_OUT	
18	PA5	-	I/O	COM	-	SPI1_SCK/I2S1_CK	ADC_IN5
						EVENTOUT	
						UART1_RX	
						TIM3_CH2	
						MCO	
19	PA6	-	I/O	COM	-	SPI1_MISO/I2S1_MCK	ADC_IN6
						TIM3_CH1	
						TIM1_BKIN	
						TIM16_CH1	
						COMP1_OUT	
						USART1_CK	
						RTC_OUT	
20	PB2	-	I/O	COM	-	USART1_RX	COMP1_INP
						SPI2_SCK	
						UART1_RX	
						LPUART_RX	
						TIM1_CH1N	

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Packages	Reset	Driver	Pin type	I/O structure	Notes	Pin functions	
QFN40 H2						Alternate functions	Additional functions
						TIM1_CH2N	
21	V_{CC}	-	S	-	-	Digital power supply	
22	PA8	-	I/O	COM	-	SPI2_NSS	PGA1_OUT
						USART1_CK	
						TIM1_CH1	
						MCO	
						EVENTOUT	
						USART1_RX	
						UART1_RX	
						SPI1_MOSI/I2S1_SD	
						TIM1_CH1	
						I2C_SCL	
						TIM1_CH3N	
23	PA9	-	I/O	COM_T	-	SPI2_MISO	OSC32OUT PGA1_INP
						USART1_TX	
						TIM1_CH2	
						UART1_TX	
						MCO	
						I2C_SCL	
						EVENTOUT	
						USART1_RX	
						SPI1_SCK/I2S1_CK	
						I2C_SDA	
						TIM1_BKIN	
24	PA10	-	I/O	COM_T	-	SPI2_MOSI	OS32IN PGA1_INN
						USART1_RX	
						TIM1_CH3	
						UART1_RX	
						TIM17_BKIN	
						I2C_SDA	
						EVENTOUT	
						USART1_TX	
						SPI1_NSS/I2S1_WS	
						I2C_SCL	
25	PA11	-	I/O	COM	-	SPI1_MISO/I2S1_MCK	COMP1_OUT
						USART1_CTS	
						TIM1_CH4	

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Packages	Reset	Driver	Pin type	I/O structure	Notes	Pin functions	
QFN40 H2						Alternate functions	Additional functions
						EVENTOUT	
						I2C_SCL	
						COMP1_OUT	
						TIM1_CH3N	
						I2C_SDA	
26	PA12	-	I/O	COM	-	SPI1_MOSI/I2S1_SD	COMP2_OUT
						USART1_RTS	
						TIM1_ETR	
						EVENTOUT	
						I2C_SDA	
						COMP2_OUT	
						I2C_SCL	
27	PA13-SWD	-	I/O	COM_T	(1)	SWDIO	-
						IR_OUT	
						EVENTOUT	
						USART1_RX	
						SPI1_MISO/I2S1_MCK	
						TIM1_CH2	
						MCO	
28	PA14-SWC	-	I/O	COM_T	(1)	SWCLK	-
						USART1_TX	
						UART1_TX	
						LPUART_TX	
						EVENTOUT	
						MCO	
29	PA15	-	I/O	COM_L	-	SPI1_NSS/I2S1_WS	PGA2_INN
						USART1_RX	
						UART1_RX	
						LPUART_RX	
						EVENTOUT	
30	PB3	-	I/O	COM_L	-	SPI1_SCK/I2S1_CK	COMP2_INM PGA2_INP
						TIM1_CH2	
						USART1_RTS	
						LPUART_RTS	
						EVENTOUT	
31	PB4	-	I/O	COM_L	-	SPI1_MISO/I2S1_MCK	COMP2_INP PGA2_OUT
						TIM3_CH1	

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Packages	Reset	Driver	Pin type	I/O structure	Notes	Pin functions	
QFN40 H2						Alternate functions	Additional functions
						USART1_CTS	
						TIM17_BKIN	
						LPUART_CTS	
						EVENTOUT	
32	PB5	-	I/O	COM_L	-	SPI1_MOSI/I2S1_SD	COMP1_OUT
						TIM3_CH2	
						TIM16_BKIN	
						USART1_CK	
						COMP1_OUT	
33	PB6	-	I/O	COM	-	USART1_TX	COMP2_INP
						TIM1_CH3	
						TIM16_CH1N	
						SPI2_MISO	
						UART1_TX	
						I2C_SCL	
						EVENTOUT	
						TIM1_BKIN	
34	PB7	-	I/O	COM	-	USART1_RX	COMP2_INM
						SPI2_MOSI	
						TIM17_CH1N	
						UART1_RX	
						I2C_SDA	
						EVENTOUT	
						I2C_SCL	
35	PF4-BOOT0	-	I/O	COM	(2)	-	BOOT0
36	PB8	-	I/O	COM	-	SPI2_SCK	COMP1_INP
						TIM16_CH1	
						UART1_TX	
						I2C_SCL	
						EVENTOUT	
						USART1_TX	
						SPI2_NSS	
						I2C_SDA	
						TIM17_CH1	
						IR_OUT	
37	-	V_{IN}	-	-	-	-	-
38	-	VG	-	-	-	-	-

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Packages	Reset	Driver	Pin type	I/O structure	Notes	Pin functions	
QFN40 H2						Alternate functions	Additional functions
39	-	LDO12	-	-	-	-	-
40	-	LDO5	-	-	-	-	-

1. After reset, PA13 and PA14 are configured as SWDIO AF and SWCLK functions, the former has an internal pull-up resistor and the latter has an internal pull-down resistor activated. PF0 and PF1 can be configured as SWCLK and SWDIO by option bytes.
2. PF4-BOOT0 defaults to digital input mode and pull-down is enabled.

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3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-4 Port A alternate functions mapping

PortA	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	SPI2_SCK	USART1_CTS	-	-	-	-	LPUART_CTS	COMP1_OUT	-	UART1_TX	SPI1_MISO/I2S1_MCK	-	-	TIM1_CH3	TIM1_CH1N	IR_OUT
PA1	SPI1_SCK/I2S1_CK	USART1_RTS	-	-	-	LPUART_RX	LPUART_RTS	EVENTOUT	-	UART1_RX	SPI1_MOSI/I2S1_SD	-	TIM3_ETR	TIM1_CH4	TIM1_CH2N	MCO
PA2	SPI1_MOSI/I2S1_SD	USART1_TX	-	-	UART1_TX	-	LPUART_RX	COMP2_OUT	-	-	SPI1_SCK/I2S1_CK	-	I2C_SDA	TIM3_CH1	-	-
PA3	SPI2_MISO	USART1_RX	-	-	UART1_RX	-	-	EVENTOUT	-	-	SPI1_MOSI/I2S1_SD	-	I2C_SCL	TIM1_CH1	-	-
PA4	SPI1_NSS/I2S1_WS	USART1_CK	SPI2_MOSI	-	TIM14_CH1	-	LPUART_TX	EVENTOUT	-	UART1_TX	-	-	-	TIM3_CH3	-	RTC_OUT
PA5	SPI1_SCK/I2S1_CK	-	-	-	-	-	-	EVENTOUT	-	UART1_RX	-	-	-	TIM3_CH2	-	MCO
PA6	SPI1_MISO/I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	-	COMP1_OUT	USART1_CK		-	-	-	-	-	RTC_OUT
PA7	-	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	-	-	-
PA8	SPI2_NSS	USART1_CK	TIM1_CH1	-		MCO	-	EVENTOUT	USART1_RX	UART1_RX	SPI1_MOSI/I2S1_SD	TIM1_CH1	I2C_SCL	TIM1_CH3N	-	-
PA9	SPI2_MISO	USART1_TX	TIM1_CH2	-	UART1_TX	MCO	I2C_SCL	EVENTOUT	USART1_RX	-	SPI1_SCK/I2S1_CK	-	I2C_SDA	TIM1_BKIN	-	-
PA10	SPI2_MOSI	USART1_RX	TIM1_CH3	-	UART1_RX	TIM17_BKIN	I2C_SDA	EVENTOUT	USART1_TX	-	SPI1_NSS/I2S1_WS	-	I2C_SCL	-	-	-
PA11	SPI1_MISO/I2S1_MCK	USART1_CTS	TIM1_CH4	-	-	EVENTOUT	I2C_SCL	COMP1_OUT	-	-	-	TIM1_CH3N	-	I2C_SDA	-	-
PA12	SPI1_MOSI/I2S1_SD	USART1_RTS	TIM1_ETR	-	-	EVENTOUT	I2C_SDA	COMP2_OUT	-	-	-	-	-	I2C_SCL	-	-
PA13	SWDIO	IR_OUT	-	-	-	-	-	EVENTOUT	USART1_RX	-	SPI1_MISO/I2S1_MCK	-	-	TIM1_CH2	-	MCO
PA14	SWCLK	USART1_TX	-	-	UART1_TX	-	LPUART_TX	EVENTOUT	-	-	-	-	-	-	-	MCO
PA15	SPI1_NSS/I2S1_WS	USART1_RX	-	-	UART1_RX	-	LPUART_RX	EVENTOUT	-	-	-	-	-	-	-	-

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3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-5 Port B alternate function mapping

PortB	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	-	-	TIM1_CH2N	-	-	-	-	-	-	-	-	-	-	-	-	-
PB1	-	-	TIM1_CH3N	-	-	-	-	-	-	-	-	-	-	-	-	-
PB2	USART1_RX	SPI2_SCK	-	UART1_RX	-	-	LPUART_RX	-	-	-	-	TIM1_CH1N	TIM1_CH2N	-	-	-
PB3	SPI1_SCK/I2S1_CK	TIM1_CH2	-	USART1_RTS	-	-	LPUART_RTS	EVENTOUT	-	-	-	-	-	-	-	-
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	USART1_CTS	-	TIM17_BKIN	LPUART_CTS	EVENTOUT	-	-	-	-	-	-	-	-
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN	USART1_CK	-	-	-	COMP1_OUT	-	-	-	-	-	-	-	-
PB6	USART1_TX	TIM1_CH3	TIM16_CH1N	SPI2_MISO	UART1_TX	-	I2C_SCL	EVENTOUT	-	-	-	TIM1_BKIN	-	-	-	-
PB7	USART1_RX	SPI2_MOSI	TIM17_CH1N	-	UART1_RX	-	I2C_SDA	EVENTOUT	-	-	-	-	I2C_SCL	-	-	-
PB8	-	SPI2_SCK	TIM16_CH1	-	UART1_TX	-	I2C_SCL	EVENTOUT	USART1_TX	-	-	SPI2_NSS	I2C_SDA	TIM17_CH1	-	IR_OUT

3.3. Alternate functions selected through GPIOF_AFR registers for port F

Table 3-6 Port F alternate function mapping

PortF	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	-	-	-	-	-	-	-	-	-	-	-	TIM1_CH3	-	-	-	-
PF1	-	-	-	-	-	-	-	-	-	-	-	TIM1_CH2	-	-	-	-
PF3	-	-	-	-	-	-	-	-	-	-	-	TIM1_CH1	-	-	-	-
PF4	-	-	USART1_RX	SPI2_NSS	UART1_RX	-	-	-	-	-	-	-	-	-	-	-

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4. Memory mapping

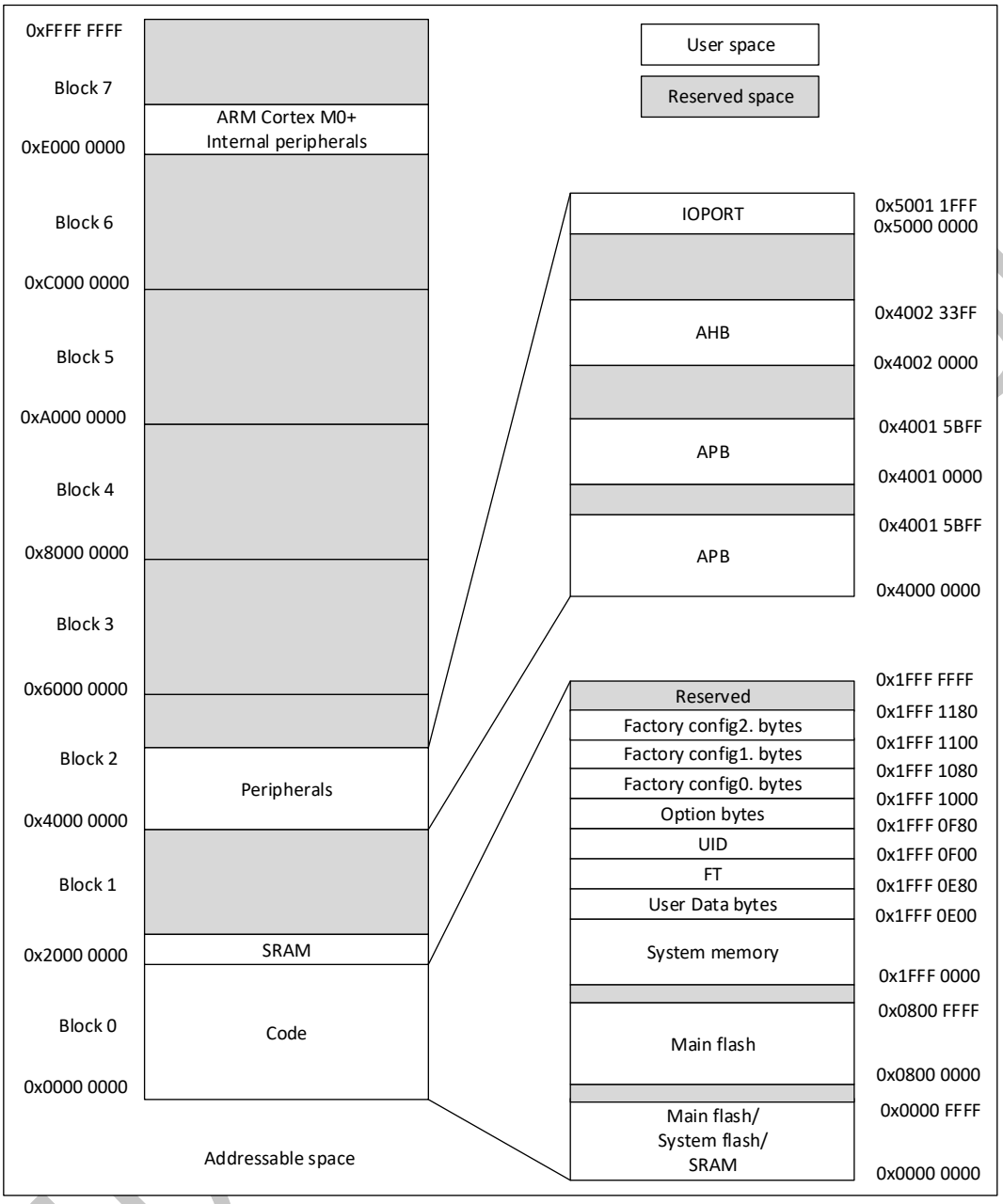


Figure 4-1 Memory mapping

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Table 4-1 Memory boundary address

Type	Boundary address	Size	Memory area	Description
SRAM	0x2000 2000-0x3FFF FFFF	-	Reserved	-
	0x2000 0000-0x2000 1FFF	8 KB	SRAM	SRAM address space: 0x2000 0000–0x2000 1FFF when configured to 4KB on power-on.
Code	0x1FFF 1180-0x1FFF FFFF	59.6 KB	Reserved	-
	0x1FFF 1100-0x1FFF 117F	128 bytes	Factory config2. bytes	Stores trimming data (including HSI trimming data), Flash/SRAM size configuration information, power-on verification code reading and IP enable information
	0x1FFF 1080-0x1FFF 10FF	128 bytes	Factory config1. bytes	HSI trimming data, Flash erase/write time configuration parameters, TS data storage.
	0x1FFF 1000-0x1FFF 107F	128 bytes	Factory config0. bytes	-
	0x1FFF 0F80-0x1FFF 0FFF	128 bytes	Option bytes	Option bytes information
	0x1FFF 0F00-0x1FFF 0F7F	128 bytes	UID	Unique ID
	0x1FFF 0E80-0x1FFF 0EFF	128 bytes	FT	FT info
	0x1FFF 0E00-0x1FFF 0E7F	128 bytes	User Data bytes	User OTP
	0x1FFF 0000-0x1FFF 0DFF	3.5 KB	System memory	Store boot loader
	0x0801 0000-0x1FFE FFFF	-	Reserved	-
	0x0800 0000-0x0800 FFFF	64 KB	Main flash memory	-
	0x0001 0000-0x07FF FFFF	-	Reserved	-
	0x0000 0000-0x0000 FFFF	64 KB	Depending on the Boot configuration selection: 1. Main flash 2. System flash 3. SRAM	-

Table 4-2 Peripheral register address

Bus	Boundary address	Size	Peripheral
	0xE000 000-0xE00F FFFF	1 MB	M0+
IOPORT	0x5000 1800-0x5FFF FFFF	~256 MB	Reserved
	0x5000 1400-0x5000 17FF	1 KB	GPIOF
	0x5000 1000-0x5000 13FF	1 KB	Reserved
	0x5000 0C00-0x5000 0FFF	1 KB	Reserved
	0x5000 0800-0x5000 0BFF	1 KB	Reserved

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Bus	Boundary address	Size	Peripheral
	0x5000 0400-0x5000 07FF	1 KB	GPIOB
	0x5000 0000-0x5000 03FF	1 KB	GPIOA
AHB	0x4002 4000-0x4FFF FFFF	~	Reserved
	0x4002 3C00-0x4002 3FFF	1 KB	Reserved
	0x4002 3800-0x4002 3BFF	1 KB	Reserved
	0x4002 3400-0x4002 37FF	1 KB	Reserved
	0x4002 3000-0x4002 33FF	1 KB	CRC
	0x4002 2400-0x4002 2FFF	~	Reserved
	0x4002 2000-0x4002 23FF	1 KB	Flash
	0x4002 1C00-0x4002 1FFF	2 KB	Reserved
	0x4002 1800-0x4002 1BFF	1 KB	EXTI
	0x4002 1400-0x4002 17FF	1 KB	Reserved
	0x4002 1000-0x4002 13FF	1 KB	RCC
	0x4002 0400-0x4002 0FFF	1 KB	Reserved
	0x4002 0000-0x4002 03FF	1 KB	DMA
APB	0x4001 5C00-0x4001 FFFF	32 KB	Reserved
	0x4001 5800-0x4001 5BFF	1 KB	MCUDBG
	0x4001 5000-0x4001 57FF	2 KB	Reserved
	0x4001 4C00-0x4001 4FFF	1 KB	Reserved
	0x4001 4800-0x4001 4BFF	1 KB	TIM17
	0x4001 4400-0x4001 47FF	1 KB	TIM16
	0x4001 4000-0x4001 43FF	1 KB	Reserved
	0x4001 3C00-0x4001 3FFF	1 KB	Reserved
	0x4001 3800-0x4001 3BFF	1 KB	USART1
	0x4001 3400-0x4001 37FF	1 KB	Reserved
	0x4001 3000-0x4001 33FF	1 KB	SPI1/I2S
	0x4001 2C00-0x4001 2FFF	1 KB	TIM1
	0x4001 2800-0x4001 2BFF	1 KB	Reserved
	0x4001 2400-0x4001 27FF	1 KB	ADC
	0x4001 0C00-0x4001 23FF	6 KB	Reserved
	0x4001 0800-0x4001 0BFF	1 KB	V_{REFBUF}
	0x4001 0400-0x4001 07FF	1 KB	Reserved
	0x4001 0300-0x4001 03FF	1 KB	PGAx/OPAx
	0x4001 0200-0x4001 02FF		COMP1 COMP2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 B400-0x4000 FFFF	19 KB	Reserved

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Bus	Boundary address	Size	Peripheral
	0x4000 B000-0x4000 B3FF	1 KB	Reserved
	0x4000 9C00-0x4000 AFFF	5 KB	Reserved
	0x4000 9800-0x4000 9BFF	1 KB	Reserved
	0x4000 9400-0x4000 97FF	1 KB	Reserved
	0x4000 8400-0x4000 93FF	4 KB	Reserved
	0x4000 8000-0x4000 83FF	1 KB	LPUART1
	0x4000 7C00-0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800-0x4000 7BFF	1 KB	Reserved
	0x4000 7400-0x4000 77FF	1 KB	Reserved
	0x4000 7000-0x4000 73FF	1 KB	PWR
	0x4000 6C00-0x4000 6FFF	1 KB	Reserved
	0x4000 6800-0x4000 6BFF	1 KB	Reserved
	0x4000 6400-0x4000 67FF	1 KB	Reserved
	0x4000 5C00-0x4000 63FF	2 KB	Reserved
	0x4000 5800-0x4000 5BFF	1 KB	Reserved
	0x4000 5400-0x4000 57FF	1 KB	I^2C
	0x4000 5000-0x4000 53FF	1 KB	Reserved
	0x4000 4C00-0x4000 4FFF	1 KB	Reserved
	0x4000 4800-0x4000 4BFF	1 KB	UART1
	0x4000 4400-0x4000 47FF	1 KB	Reserved
	0x4000 3C00-0x4000 43FF	2 KB	Reserved
	0x4000 3800-0x4000 3BFF	1 KB	SPI2
	0x4000 3400-0x4000 37FF	1 KB	Reserved
	0x4000 3000-0x4000 33FF	1 KB	IWDG
	0x4000 2C00-0x4000 2FFF	1 KB	WWDG
	0x4000 2800-0x4000 2BFF	1 KB	RTC
	0x4000 2400-0x4000 27FF	1 KB	Reserved
	0x4000 2000-0x4000 23FF	1 KB	TIM14
	0x4000 1800-0x4000 1FFF	2 KB	Reserved
	0x4000 1400-0x4000 17FF	1 KB	Reserved
	0x4000 1000-0x4000 13FF	1 KB	Reserved
	0x4000 0800-0x4000 0FFF	2 KB	Reserved
	0x4000 0400-0x4000 07FF	1 KB	TIM3
	0x4000 0000-0x4000 03FF	1 KB	Reserved

1. In the above table, the reserved address marked by AHB cannot be written, read back is 0, and a hardfault is generated; The reserved address marked by APB cannot be written, read back is 0, and no hardfault is generated.

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5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency, based on production tests performed on 100% of devices at T_A = 25 °C and $T_A = T_{A(max)}$ (as per the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A =25°C and V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95 % of the devices have an error less than or equal to the value indicated.

5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Descriptions	Min	Max	Unit
V_{CC}	External mains power supply	-0.30	6.25	V
V_{IN}	Input voltage of Tolerant I/O	-0.30	6.25	V
	Input voltage of other pins	-0.30	V_{CC}+0.30	

1. Power supply V_{CC} and ground V_{SS} pins must always be connected to an external power supply system that is within the permitted range.

Table 5-2 Current characteristics

Symbol	Descriptions	Max	Unit
I_{VCC}	Total current into V_{CC} pin (supply current)(1)	120	mA
I_{VSS}	Total current out of V_{SS} pin (sink current)(1)	120	
$\Sigma I_{IO(PIN)}$(2)	Total output current sunk by sum of all I/Os and control pins	100	
	Total output current sourced by sum of all I/Os and control pins	100	
$I_{IO(PIN)}$	Output current sunk by any I/O (except COM_L I/O)	20	
	Output current sunk by any COM_L I/O and control pin	80	

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Symbol	Descriptions	Max	Unit
	Output current sourced by any I/O	20	

1. Power supply V_{CC} and ground V_{SS} pins must always be connected to an external power supply system that is within the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.

Table 5-3 Thermal characteristics

Symbol	Descriptions	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK}	Internal APB clock frequency	-	0	72	MHz
V_{CC}	Standard operating voltage	-	2.0	5.5	V
V_{IN}	Input voltage of Tolerant I/O	-	-0.3	5.5	V
	Input voltage of other pins	-	-0.3	V_{CC}+0.3	
T_A	Ambient temperature	-	-40	105	℃
T_J	Junction temperature	-	-40	125	℃

5.3.2. Operating conditions at power-on/power-down

Table 5-5 Operating conditions at power-on/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise rate	-	10	∞	μs/V
	V_{CC} fall rate	V_{CC} drop	20	∞	

5.3.3. Embedded reset and PVD module characteristics

Table 5-6 POR/PDR/BOR module characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$	POR reset temporization	-	-	4.00	7.50	ms
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.50	1.63	1.70	V
		Falling edge	1.45	1.60	1.68	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	30	-	mV
V_{BOR}	BOR threshold	BOR_LEV[2:0]=000 (Rising edge)	Reserved			V
		BOR_LEV[2:0]=000 (Falling edge)				
		BOR_LEV[2:0]=001 (Rising edge)				

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		BOR_LEV[2:0]=001 (Falling edge)				
		BOR_LEV[2:0]=010 (Rising edge)	2.10(2)	2.20	2.30	
		BOR_LEV[2:0]=010 (Falling edge)	2.00	2.10	2.20(2)	
		BOR_LEV[2:0]=011 (Rising edge)	2.29(2)	2.41	2.52	
		BOR_LEV[2:0]=011 (Falling edge)	2.19	2.30	2.41(2)	
		BOR_LEV[2:0]=100 (Rising edge)	2.47(2)	2.59	2.71	
		BOR_LEV[2:0]=100 (Falling edge)	2.39	2.51	2.63(2)	
		BOR_LEV[2:0]=101 (Rising edge)	2.67(2)	2.80	2.93	
		BOR_LEV[2:0]=101 (Falling edge)	2.55	2.68	2.81(2)	
		BOR_LEV[2:0]=110 (Rising edge)	2.84(2)	2.98	3.12	
		BOR_LEV[2:0]=110 (Falling edge)	2.77	2.90	3.03(2)	
		BOR_LEV[2:0]=111 (Rising edge)	3.06(2)	3.21	3.36	
		BOR_LEV[2:0]=111 (Falling edge)	2.96	3.10	3.25(2)	
$V_{_BOR_hyst}$	BOR hysteresis	-	-	100	-	mV

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

Table 5-7 PVD module characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	PVD threshold	PVDT[2: 0] = 000 (Rising edge)	Reserved			V
		PVDT[2: 0] = 000 (Falling edge)				
		PVDT[2: 0] = 001 (Rising edge)				
		PVDT[2: 0] = 001 (Falling edge)				
		PVDT[2: 0] = 010 (Rising edge)	2.10(2)	2.20	2.30	
		PVDT[2: 0] = 010 (Falling edge)	2.00	2.10	2.20(2)	
		PVDT[2: 0] = 011 (Rising edge)	2.29(2)	2.41	2.52	
		PVDT[2: 0] = 011 (Falling edge)	2.19	2.30	2.41(2)	
		PVDT[2: 0] = 100 (Rising edge)	2.47(2)	2.59	2.71	
		PVDT[2: 0] = 100 (Falling edge)	2.39	2.51	2.63(2)	
		PVDT[2: 0] = 101 (Rising edge)	2.67(2)	2.80	2.93	
		PVDT[2: 0] = 101 (Falling edge)	2.55	2.68	2.81(2)	
		PVDT[2: 0] = 110 (Rising edge)	2.84(2)	2.98	3.12	
		PVDT[2: 0] = 110 (Falling edge)	2.77	2.90	3.03(2)	
		PVDT[2: 0] = 111 (Rising edge)	3.06(2)	3.21	3.36	
		PVDT[2: 0] = 111 (Falling edge)	2.96	3.10	3.25(2)	
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

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5.3.4. Supply current characteristics

Table 5-8 Current consumption in Run mode

Symbol	Conditions						Typ(1)	Max		Unit
	Run	Code	System clock source	Frequency (MHz)	Peripheral clock	Power supply	T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{CC}(Run)	Flash	While(1)	PLL	72	Disabled	MR_VSEL = 2'b00	3.38	-	-	mA
			HSI	8		MR_VSEL = 2'b01	0.92	-	-	
			LSI (SLEEP_EN = 0)	32.768 kHz		MR_VSEL = 2'b01	0.48	-	-	
			LSI (SLEEP_EN = 1)	32.768 kHz		MR_VSEL = 2'b01	0.42	-	-	
			PLL	72	Enabled	MR_VSEL = 2'b00	5.41	-	-	
			HSI	8		MR_VSEL = 2'b01	1.13	-	-	
			LSI (SLEEP_EN = 0)	32.768 kHz		MR_VSEL = 2'b01	0.48	-	-	
			LSI (SLEEP_EN = 1)	32.768 kHz		MR_VSEL = 2'b01	0.42	-	-	

1. Guaranteed by design, not tested in production.

Table 5-9 Current consumption in Sleep mode

Symbol	Conditions						Typ(1)	Max		Unit
	Run	Code	System clock source	Frequency (MHz)	Peripheral clock	Power supply	T_A = 25 ℃	T_A = 85 °C	T_A = 105 °C	
I_{CC}(Sleep)	Flash	While(1)	PLL	72	Disabled	MR_VSEL = 2'b00	1.98	-	-	mA
			HSI	8		MR_VSEL = 2'b01	0.58	-	-	
			LSI (SLEEP_EN = 0)	32.768 kHz		MR_VSEL = 2'b01	0.48	-	-	
			LSI (SLEEP_EN = 1)	32.768 kHz		MR_VSEL = 2'b01	0.42	-	-	
			PLL	72	Enabled	MR_VSEL = 2'b00	4.26	-	-	
			HSI	8		MR_VSEL = 2'b01	0.82	-	-	
			LSI (SLEEP_EN = 0)	32.768 kHz		MR_VSEL = 2'b01	0.48	-	-	
			LSI (SLEEP_EN = 1)	32.768 kHz		MR_VSEL = 2'b01	0.42	-	-	

1. Data based on characterization results, not tested in production.

Table 5-10 Current consumption in Stop mode

Symbol	Conditions		Typ(1)		Max		Unit
	-	Power supply	T_A = 25 ℃		T_A = 85 °C	T_A = 105 °C	
			MCU	Driver			
I_{CC}(Stop)	RTC + IWDG + LPTIM with LSI	DLPR_VSEL = 2'b10	3.3	175	-	-	μA
	IWDG with LSI	DLPR_VSEL = 2'b10	3.3	175	-	-	
	LPTIM with LSI	DLPR_VSEL = 2'b10	3.3	175	-	-	
	RTC with LSI	DLPR_VSEL = 2'b10	3.3	175	-	-	
	Peripheral shutdown	DLPR_VSEL = 2'b10	3.0	175	-	-	

1. Data based on characterization results, not tested in production.

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5.3.5. Wakeup time from low-power mode

Table 5-11 Wake-up time from low-power mode

Symbol	Parameter[1]	Power Supply[2]	Conditions	Typ[3]	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode	-	Run program in Flash, HSI (8 MHz) as system clock	11	-	CPU cycles
t_{WUSTOP}	Wake up time from Stop mode to Run mode	DLPR Power, DLPR_VSEL=00	Run program in Flash, HSI (8 MHz) as system clock	15	-	μs
		DLPR powered, DLPR_VSEL=01	Run program in Flash, HSI (8 MHz) as system clock	15	-	
		DLPR powered, DLPR_VSEL=10	Run program in Flash, HSI (8 MHz) as system clock	15	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Power supply mode before wake-up.
3. Data based on characterization results, not tested in production.

5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the device stops working, the corresponding I/O is used as a standard GPIO.

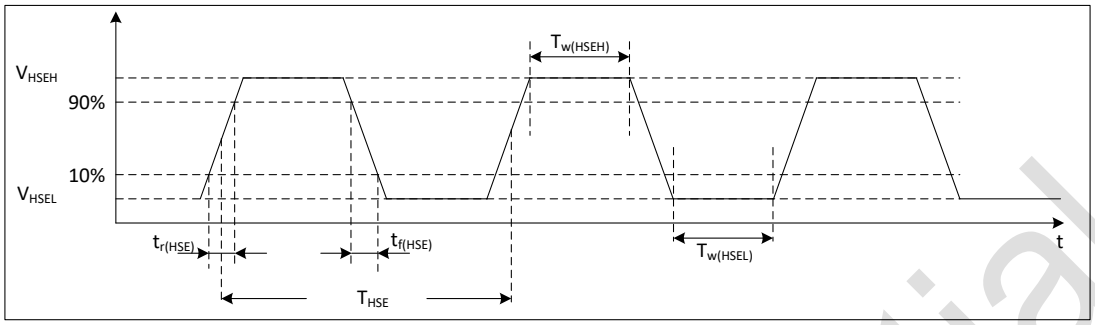


Figure 5-1 High-speed external clock timing diagram

Table 5-12 High-speed external clock characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	1	8	32	MHz
V_{HSEH}	Input pin high level voltage	0.7*V_{CC}	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	V_{SS}	-	0.3*V_{CC}	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	High or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Rise or fall time	-	-	20	ns
$DuCy_{(HSE)}$	Duty cycle	45	-	55	%

1. Guaranteed by design, not tested in production.

5.3.6.2. Low-speed external clock generated from an external source

In the bypass mode of LSE (the LSEBYP of RCC_BDCR is set), the low-speed start-up circuit in the chip stops working, and the corresponding I/O is used as a standard GPIO.

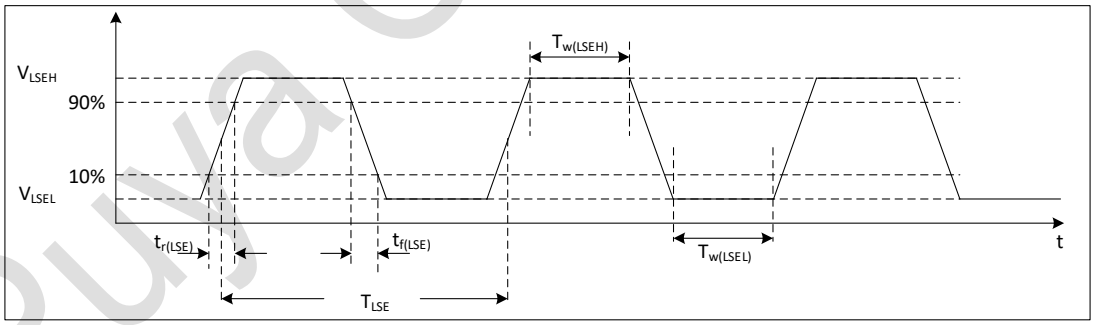


Figure 5-2 Low-speed external clock timing diagram

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Table 5-13 Low-speed external clock characteristics(1)

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	32.768	1000	kHz
V_{LSEH}	Input pin high level voltage	0.7*V_{CC}	-	-	V
V_{LSEL}	Input pin low level voltage	-	-	0.3*V_{CC}	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	High or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Rise or fall time	-	-	50	ns
$DuCy_{(LSE)}$	Duty cycle	45	-	55	%

1. Guaranteed by design, not tested in production.

5.3.6.3. High-speed external clock generated from a crystal resonator

The high-speed external (HSE) clock can be supplied with 4 to 32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-14 HSE oscillator characteristics

Symbol	Parameter	Conditions(1)		Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-		4	-	32	MHz
I_{CC}(4)	HSE current consumption	R_m=100 Ω, C_L=12 pF@4 MHz, HSE_DRV[1: 0] = 00		-	0.60	-	mA
		R_m=150 Ω, C_L=12 pF@8 MHz, HSE_DRV[1:0] = 00		-	0.63	-	
		R_m=70 Ω, C_L=12 pF@16 MHz, HSE_DRV[1:0] = 01		-	1.10	-	
		R_m=40 Ω, C_L=20 pF@24 MHz, HSE_DRV[1:0] = 10		-	1.45	-	
		R_m=40 Ω, C_L=10 pF@32 MHz, HSE_DRV[1:0] = 10		-	1.50	-	
g_m(2)	Maximum critical crystal gm	Startup	HSE_DRV[1:0]=00	3.5	-	-	mA/V
			HSE_DRV[1:0]=01	5.0	-	-	
			HSE_DRV[1:0]=10	7.5	-	-	
			HSE_DRV[1:0]=11	10.0	-	-	
$t_{SU(HSE)}$(3)(4)	Startup time	R_m=100 Ω, C_L=12 pF@4 MHz, HSE_DRV[1: 0] = 00		-	1.80	-	ms
		R_m=150 Ω, C_L=12 pF@8 MHz, HSE_DRV[1:0] = 00		-	1.90	-	
		R_m=70 Ω, C_L=12 pF@16 MHz, HSE_DRV[1:0] = 01		-	0.40	-	
		R_m=40 Ω, C_L=20 pF@24 MHz, HSE_DRV[1:0] = 10		-	0.55	-	
		R_m=40 Ω, C_L=10 pF@32 MHz, HSE_DRV[1:0] = 10		-	0.45	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state, measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another.
4. Data based on characterization results, not tested in production.

5.3.6.4. Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

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Table 5-15 LSE oscillator characteristics

Symbol	Parameter	Conditions[1]	Min[2]	Typ	Max[2]	Unit
I_{CC}[4]	LSE current consumption	C_L=6 pF, R_m=70 kΩ LSE_STARTUP[1:0] = 00 LSE_DRIVER[1:0] = 00	-	600	-	nA
		C_L=6 pF, R_m=70 kΩ LSE_STARTUP[1:0] = 00 LSE_DRIVER[1:0] = 01	-	700	-	
		C_L=12 pF, R_m=45 kΩ LSE_STARTUP[1:0] = 00 LSE_DRIVER[1:0] = 10	-	1100	-	
		C_L=12 pF, R_m=45 kΩ LSE_STARTUP[1:0] = 00 LSE_DRIVER[1:0] = 11	-	1400	-	
g_m[2]	Maximum critical crystal gm	LSE_DRV[1:0]=00	2.5	-	-	μA/V
		LSE_DRV[1:0]=01	3.5	-	-	
		LSE_DRV[1:0]=10	7.0	-	-	
		LSE_DRV[1:0]=11	10.0	-	-	
$t_{SU(LSE)}$[3][4]	Startup time	C_L=6 pF, R_m=70 kΩ LSE_STARTUP[1:0] = 00 LSE_DRIVER[1:0] = 00	-	0.6	-	s
		C_L=6 pF, R_m=70 kΩ LSE_STARTUP[1:0] = 00 LSE_DRIVER[1:0] = 01	-	0.5	-	
		C_L=12 pF, R_m=45 kΩ LSE_STARTUP[1:0] = 00 LSE_DRIVER[1:0] = 10	-	0.7	-	
		C_L=12 pF, R_m=45 kΩ LSE_STARTUP[1:0] = 00 LSE_DRIVER[1:0] = 11	-	0.5	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable, measured for a standard crystal/resonator , which may vary greatly from crystal to resonator.
4. Data based on characterization results, not tested in production.

5.3.7. High-speed internal (HSI) RC oscillator

Table 5-16 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	-	-	8.0	-	MHz
$\Delta_{Temp(HSI8)}$	HSI 8M frequency drift over temperature	V_{CC} = 3.3 V, T_A = 25 ℃	-1[2]	-	1[2]	%
		V_{CC} = 2.0 to 5.5 V, T_A = -20 to 85 ℃	-1.5[2]	-	1.5[2]	
		V_{CC} = 2.0 to 5.5 V T_A = -40 to 105 ℃	-2[2]	-	2[2]	
f_{TRIM}[1]	HSI trimming accuracy	-	-	0.1	-	%
D_{HSI}[1]	Duty cycle	-	45[1]	-	55[1]	%
$t_{Stab(HSI)}$	HSI stabilization time	-	-	5	-	μs
$I_{CC(HSI)}$[2]	HSI power consumption	8 MHz	-	95	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

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5.3.8. Low-speed internal (LSI) RC oscillator

Table 5-17 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	-	-	32.768	-	kHz
$\Delta_{Temp(LSI)}$	LSI frequency drift over temperature	T_A = 25 °C， V_{CC} = 3.3 V	-3(2)	-	3(2)	%
		V_{CC} = 2.0 to 5.5 V, T_A =0 to 85 °C	-5(2)	-	5(2)	
		V_{CC} = 2.0 to 5.5 V, T_A =-40 to 105 °C	-8(2)	-	8(2)	
f_{TRIM}(1)	LSI trimming accuracy	-	-	0.5	-	%
$t_{Stab(LSI)}$(1)	LSI stabilization time	-	-	100	-	μs
$I_{CC(LSI)}$(1)	LSI power consumption	-	-	300	-	nA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.9. Phase locked loop (PLL) characteristics

Table 5-18 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	T_A = 25 °C, V_{CC} = 3.3 V	8(1)	-	24(1)	MHz
f_{PLL_OUT}	PLL output clock	T_A = 25 °C, V_{CC} = 3.3 V	48(1)	-	144(1)	MHz
t_{LOCK}	PLL lock time	f_{PLL_IN} = 24 MHz	-	50(1)	-	μs

1. Guaranteed by design, not tested in production.

5.3.10. Memory characteristics

Table 5-19 Memory characteristics(2)

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}	Page programming time	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase time	-	3.5	4.5	ms
I_{CC}	Page programming supply current	-	2.0	3.0	mA
	Page/sector/mass erase supply current	-	2.0	3.0	

1. Guaranteed by design, not tested in production.
2. When the program runs in SRAM and executes the Flash erase/write program, the CPU will stop working.

Table 5-20 Memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 to 85 ℃	100	kcycles
		T_A = 85 to 105 ℃	10	
t_{RET}	Data retention time	10 kcycles T_A = 55 °C	20	Years

1. Data based on characterization results, not tested in production.

5.3.11. ESD & LU characteristics

Table 5-21 ESD&LU characteristics

Symbol	Parameter	Standard	Conditions	Typ	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	-	2	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	ESDA/JEDEC JS-002-2018	-	1	kV
LU	Static latch-up	JESD78E	-	200	mA

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5.3.12. I/O port characteristics

Table 5-22 IO port characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage Tolerant I/O input low level		2.0 V≤V_{CC}≤5.5 V	-	-	0.3*V_{CC}	V
V_{IH}	High level input voltage Tolerant I/O input high level		2.0 V≤V_{CC}≤5.5 V	0.7*V_{CC}	-	-	V
V_{hys}(1)	Schmitt trigger hysteresis Tolerant I/O Schmitt trigger hysteresis		-	-	200	-	mV
I_{lkg}(2)	Input leakage current	Standard I/O	V_{SS}≤V_{IN}≤V_{CC}	-	-	±1	μA
		Tolerant I/O	V_{SS}≤V_{IN}≤V_{CC}	-	-	±1	
			V_{CC}≤V_{IN}≤V_{CC}+1 V(4)	-	-	3	
			V_{CC}+1 V≤V_{IN}≤5.5 V	-	-	1	
R_{PU}(3)	Internal pull-up resistor		V_{IN}=V_{SS}	30	50	70	kΩ
R_{PD}(3)	Internal pull-down resistor		V_{IN}=V_{CC}	30	50	70	kΩ
C_{IO}	Pin capacitance		-	-	5	-	pF
$t_{ns(EXTI)}$(1)	Input filter width		ENI=1, ENS=1	3	5	10	ns
$t_{ns(I2C)}$(1)	I^2C Input filter width		IIC_FILT_EN=1	100	145	300	ns

1. Guaranteed by design, not tested in production.
2. If there is reverse current pouring in adjacent pins, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are designed to be a real resistor in series with a switchable PMOS/NMOS.
4. The maximum value of V_{CC}+1 should not exceed 5.5 V.

Table 5-23 Output voltage characteristics(3)

Symbol	Parameter(2)	Driver	Conditions	Min	Max	Unit
V_{OL}(1)	COM IO output low level	GPIOx_OSPEEDR=11	I_{OL} = 50 mA, V_{CC} ≥ 5.0 V	-	0.50	V
		GPIOx_OSPEEDR=11	I_{OL} = 50 mA, V_{CC} ≥ 3.3 V	-	0.55	
		GPIOx_OSPEEDR=11	I_{OL} = 8 mA, V_{CC} ≥ 2.7 V	-	0.40	
		GPIOx_OSPEEDR=11	I_{OL} = 4 mA, V_{CC} = 1.8 V	-	0.40	
V_{OL}(1)	COM_L output low level	GPIOx_OSPEEDR=11, EHS=1	I_{OL} = 80 mA, V_{CC} ≥ 5 V	-	0.55	V
		GPIOx_OSPEEDR=10, EHS=1	I_{OL} = 60 mA, V_{CC} ≥ 5 V	-	0.45	
		GPIOx_OSPEEDR=01, EHS=1	I_{OL} = 40 mA, V_{CC} ≥ 5 V	-	0.40	
		GPIOx_OSPEEDR=00, EHS=1	I_{OL} = 20 mA, V_{CC} ≥ 5 V	-	0.30	
V_{OH}(1)	COM and COM_L IO output high level	GPIOx_OSPEEDR=11	I_{OL} = 16 mA, V_{CC} ≥ 3.3 V	V_{CC}-0.70	-	V
		GPIOx_OSPEEDR=11	I_{OL} = 8 mA, V_{CC} ≥ 2.7 V	V_{CC}-0.45	-	
		GPIOx_OSPEEDR=11	I_{OL} = 4 mA, V_{CC} = 1.8 V	V_{CC}-0.35	-	

1. These I/O types refer to the terms and symbols defined by pins.
2. Data based on characterization results, not tested in production.
3. The combined maximum current across all output pins (including contributions from both V_{OL} and V_{OH} states) must not exceed the $\Sigma I_{IO(PIN)}$ maximum rating specified in Table 5-2 Current Characteristics.

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5.3.13. ADC characteristics

Table 5-24 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Analog power supply	-	1.7	-	5.5	V
I_{CC}	V_{CC} pin current	f_{ADC} = 16 MHz	-	1(1)	-	mA
		f_{ADC} = 32 MHz	-	1(1)	-	
		f_{ADC} = 48 MHz	-	1(1)	-	
f_{ADC}	ADC clock frequency	1.7 V≤V_{REF+} = V_{CC}<5.5 V	4	-	8	MHz
		2.5 V≤V_{REF+} = V_{CC}<5.5 V	4	-	16	
		2.7 V≤V_{REF+} = V_{CC}<5.5 V	4	-	48	
		V_{REF}+ = V_{REFBUF}	-	-	2	
f_S(2)	Sampling rate	V_{REF+} = V_{CC}≥1.7 V	-	-	0.5	Msps
		V_{REF+} = V_{CC}≥2.5V	-	-	1	
		V_{REF+} = V_{CC}≥2.7 V	-	-	3	
		V_{REF+} = V_{REFBUF}, f_{ADC} = 2 MHz	-	-	0.125	
V_{AIN}	Conversion voltage range	Single-ended mode	0	-	V_{CC}	V
R_{AIN}(2)	External Input Impedance(3)	-	-	-	33	kΩ
R_{ADC}(1)(2)	Sampling switch resistance	-	-	-	1.2	kΩ
C_{ADC}(1)(2)	Internal sampling and holding capacitor	-	-	2.5	3	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 16 MHz	12			μs
		-	192			1/f_{ADC}
t_S(2)	Sampling time	f_{ADC} = 16 MHz	0.156	-	40.03	μs
		-	2.5	-	640.5	1/f_{ADC}
t_{samp_setup}	Sampling time for internal channels	-	20	-	-	μs
t_{STAB}(2)	Power-on stabilization time	-	0	0	3	μs
t_{CONV}(2)	Total conversion time	f_{ADC} = 16 MHz	1	-	40.875	μs
		-	16 to 654			1/f_{ADC}

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. When using external triggering, an additional delay of 1/f_{PCLK2} is required.
   a) $R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$
   b) The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution).

Table 5-25 R_{AIN} Max for f_{ADC} = 32 MHz(1)

Sampling period (T_S)	Sampling time (t_s)(ns)	Maximum value of R_{AIN} (Ω)	
		Fast channel	Slow channel
2.5	78.13	100	-
6.5	203.13	330	100
12.5	390.63	680	470
24.5	765.63	1500	1200
47.5	1484.38	2200	1800

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Sampling period (T_S)	Sampling time (t_s)(ns)	Maximum value of R_{AIN} (Ω)	
		Fast channel	Slow channel
92.5	2890.63	4700	3900
247.5	7734.38	12000	10000
640.5	20015.63	39000	33000

1. Guaranteed by design, not tested in production.

Table 5-26 ADC static characteristics(1)(2)(3)

Symbol	Parameter	Mode	Min	Typ	Max	Unit
ET	Total unadjusted error	Single-ended mode	-	±4.0	±8.0	LSB
EO	Offset error	Single-ended mode	-	±2.0	±5.0	
EG	Gain error	Single-ended mode	-	±3.0	±6.0	
DNL	Differential nonlinearity error	Single-ended mode	-	±0.8	±1.0	
INL	Integral nonlinearity error	Single-ended mode	-	±2.5	±5.0	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. Relationship between ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

Table 5-27 ADC dynamic characteristics(1)(2)(3)

Symbol	Parameter	Mode	Min	Typ	Max	Unit
ENOB	Effective number of bits	Single-ended mode	-	10.0	-	bit
SINAD	Signal to noise and distortion ratio	Single-ended mode	-	62.0	-	dB
SNR	Signal to noise ratio	Single-ended mode	-	62.9	-	
SFDR	spurious free dynamic range	Single-ended mode	-	72.3	-	
THD	Total harmonic distortion	Single-ended mode	-	-69.5	-	

1. Guaranteed by design, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur.

5.3.14. Comparator characteristics

Table 5-28 Comparator characteris(1)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IN}	Input voltage range	-			0	-	V_{CC}	V
t_{START}	Startup time	High-speed mode			-	-	5	μs
		Medium-speed mode			-	-	15	
t_D	Propagation delay	200 mV step 100 mV over-drive	High-speed mode	-	-	50	200	ns
			Medium-speed mode	-	-	1500	4000	
		>200 mV step 100 mV over-drive	High-speed mode	-	-	-	300	
			Medium-speed mode	-	-	-	4000	

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Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{offset}	Offset voltage	-		-	-	±5	±10	mV
V_{hys}	Hysteresis voltage	No hysteresis		-	-	0	-	mV
		With hysteresis		-	-	20	-	
I_{CC}	Consumption	Static	High-speed mode	-	-	250	-	μA
			Medium-speed mode	-	-	10	-	
		With 50 kHz and ±100 mv overdrive square signal 50 kHz square wave	High-speed mode	-	-	250	-	
			Medium-speed mode	-	-	10	-	

1. Guaranteed by design, not tested in production.

5.3.15. Operational amplifier characteristics

Table 5-29 Operational amplifier characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	2.5	3.3	5.5	V
V_{IN}	Input voltage range	-	0	-	V_{CC}	V
V_{OUT}	Output voltage	C_{LOAD} ≤ 25 pF, R_{LOAD} ≥ 5 kΩ	0.2	-	V_{CC}-0.2	V
I_{LOAD}	Drive current	-	-	-	1	mA
I_{LOAD_PGA}(1)	Drive current in PGA mode	-	-	-	0.5	mA
C_{LOAD}	Load capacitance	-	-	-	25	pF
R_{LOAD}	Load resistor	-	5	-	-	kΩ
V_{IO}	Input offset voltage	T_A = 25 °C, V_{CC}/2	-	-	±10	mV
CMRR(1)	Common mode rejection ratio	Frequency 1 kHz	-	60	-	dB
PSRR(1)	Power supply rejection ratio (to V_{CC}) (static DC measurement)	Frequency 1 kHz, C_{LOAD} ≤ 25 pF, R_{LOAD} ≥ 5 kΩ, Vcom = V_{CC}/2	-	80	-	dB
		Frequency 1 MHz, C_{LOAD} ≤ 25 pF, R_{LOAD} ≥ 5 kΩ, Vcom = V_{CC}/2	40	-	-	
		Frequency 10 MHz, C_{LOAD} ≤ 25 pF, R_{LOAD} ≥ 5 kΩ, Vcom = V_{CC}/2	20	-	-	
UGBW(1)	Unit gain bandwidth	200mV ≤ Vout ≤ V_{CC}-200 mV	5	10	-	MHz
SR	Slew rate (from 10% * V_{CC} to 90% * V_{CC})	Normal mode	-	8	-	V/μs
AO(1)	Open loop gain	100 mV ≤ Vout ≤ V_{CC}-100 mV	65	95	-	dB
		200 mV ≤ Vout ≤ V_{CC}-300 mV	75	95	-	
V_{OHSAT}	Maximum output saturation voltage	I_{LOAD} = max or R_{LOAD} = min, Input at V_{CC}. follower mode	V_{CC}-200	-	-	mV
V_{OLSAT}	Minimum output saturation voltage	I_{LOAD} = max or R_{LOAD} = min, Input at 0. follower mode	-	-	200	mV
φ_m	Phase margin	Follower mode, Vcom = V_{CC}/2	55	65	-	°
GM	Gain margin	Follower mode, Vcom = V_{CC}/2	8	-	-	dB
t_{SU}	Start up time (off to output 98% * V_{CC})	Normal mode, C_{LOAD} ≤ 25 pF, R_{LOAD} ≥ 5 kΩ, follower mode	-	3	6	μs
PGA gain error	Non inverting gain value	PGA gain = 2, 200mV ≤ Vout ≤V_{CC}-200mV	-1	-	1	%
		PGA gain = 4, 200mV ≤ Vout ≤ V_{CC}-200mV	-2	-	2	
		PGA gain = 8, 200mV ≤ Vout ≤ V_{CC}-200mV	-3	-	3	
		PGA gain = 16, 200mV ≤ Vout ≤ V_{CC}-200mV	-5	-	5	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Inverting gain error	PGA gain = -1, 200mV ≤ Vout ≤ V_{CC}-200mV	-1	-	1	%
		PGA gain = -3, 200mV ≤ Vout ≤ V_{CC}-200mV	-2	-	2	
		PGA gain = -7, 200mV ≤ Vout ≤ V_{CC}-200mV	-3	-	3	
		PGA gain = -15, 200mV ≤ Vout ≤ V_{CC}-200mV	-5	-	5	
Resistance network	R2/R1 (internal resistance values in non-inverting PGA mode)	PGA gain = 2	-	640/640	-	kΩ/ kΩ
		PGA gain = 4	-	960/320	-	
		PGA gain = 8	-	1120/160	-	
		PGA gain = 16	-	1200/80	-	
	R2/R1 (internal resistance values in inverting PGA mode)	PGA gain = -1	-	640/640	-	kΩ/ kΩ
		PGA gain = -3	-	960/320	-	
		PGA gain = -7	-	1120/160	-	
		PGA gain = -15	-	1200/80	-	
eN(1)	Voltage noise density	1 kHz, output resistive load 5 kΩ	-	250	-	nV/ √Hz
		10 kHz, output resistive load 4 kΩ	-	90	-	
I_{CC}	OPAMP supply current	Normal mode, no load, follower mode	-	1.3	2.2	mA

1. Guaranteed by design, not tested in production.

5.3.16. Temperature sensor characteristics

Table 5-30 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	± 2	± 5	℃
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/℃
V_{30}	Voltage at 30 °C (±5 °C)	0.74	0.76	0.78	V
t_{START}(1)	Start up time	-	70	120	μs
t_{S_temp}(1)	ADC sampling time when reading the temperature	20	-	-	μs

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.17. Embedded voltage reference characteristics

Table 5-31 Embedded internal voltage reference (V_{REFINT}) characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$t_{start_vrefint}$	Start time of V_{REFINT}	-	10	15	μs
T_{coeff}	Temperature coefficient	-	100(1)	-	ppm/℃
I_{vcc}	V_{REFINT} consumption from V_{CC}	-	12	20	μA

1. Guaranteed by design, not tested in production.

Table 5-32 Internal voltage reference buffer (V_{REFBUF}) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REF20}	2.048 V internal reference buffer	T_A = 25 °C, V_{CC} = 3.3 V	2.028	2.048	2.068	V
V_{REF15}	1.5 V internal reference buffer	T_A = 25 °C, V_{CC} = 3.3 V	1.485	1.5	1.515	V
$V_{REF1024}$	1.024 V Internal reference voltage	T_A = 25 °C, V_{CC} = 3.3 V	1.014	1.024	1.034	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{coeff_VREFBUF}$(1)	Temperature coefficient of V_{REFBUF}	T_A = -40 to 105 °C	-	150	-	ppm/°C
$t_{start_VREFBUF}$(1)	Start time of V_{REFBUF}	-	-	350	450	μs

1. Guaranteed by design, not tested in production.

5.3.18. COMP voltage reference buffer characteristics (6-bit DAC)

Table 5-33 Embedded internal voltage reference (V_{REFCMP}) characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
$\triangle V_{abs}$	Absolute deviation	-	-	±0.5	-	LSB

1. Guaranteed by design, not tested in production.

5.3.19. Timer characteristics

Table 5-34 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.889	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 72 MHz	-	36	
Res_{TIM}	Timer resolution time	-	-	16	bit
$t_{COUNTER}$	16-bit counter internal clock period	-	1	2^{16}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	910	μs

Table 5-35 LPTIM characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PRESC[2:0]	Min	Max	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.946	
/8	3	0.2441	15997.338	
/16	4	0.4883	32001.229	
/32	5	0.9766	64002.458	
/64	6	1.9531	127998.362	
/128	7	3.9063	256003.277	

Table 5-36 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

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Table 5-37 WWDG characteristics (timeout period at 48 MHz PCLK)

Prescaler	WDGTB[1:0]	Min	Max	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

5.3.20. Communication interfaces

5.3.20.1. I²C interface characteristics

The I²C interface meets the requirements of the I²C bus specification and user manual:

- Standard-mode (Sm): 100 kHz
- Fast-mode (Fm): 400 kHz
- Fast-mode plus (Fm+): 1 MHz

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-38 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

5.3.20.2. SPI characteristics

Table 5-39 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	36(1)	MHz
		Slave mode	-	24(2)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	2*T_{pclk}	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2*T_{pclk}	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high level/low level time	Master mode, presc = 2	T_{pclk} -2	T_{pclk} +1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	1	-	ns
		Slave mode	3	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	ns
$t_{h(SI)}$		Slave mode	2	-	
$t_{a(SO)}$	Data output access time	Slave mode	0	3*T_{pclk}	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	2.5*T_{pclk}	-	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	0	20	ns
$t_{v(MO)}$		Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$	Data output hold time	Slave mode	2	-	ns
$t_{h(MO)}$		Master mode	1	-	
$DuCy_{(SCK)}$	SPI slave input clock duty cycle	Slave mode	45	55	%

1. The prerequisite: f_{PCLK} = 72 MHz.
2. The prerequisite: f_{PCLK} ≥ 48 MHz.

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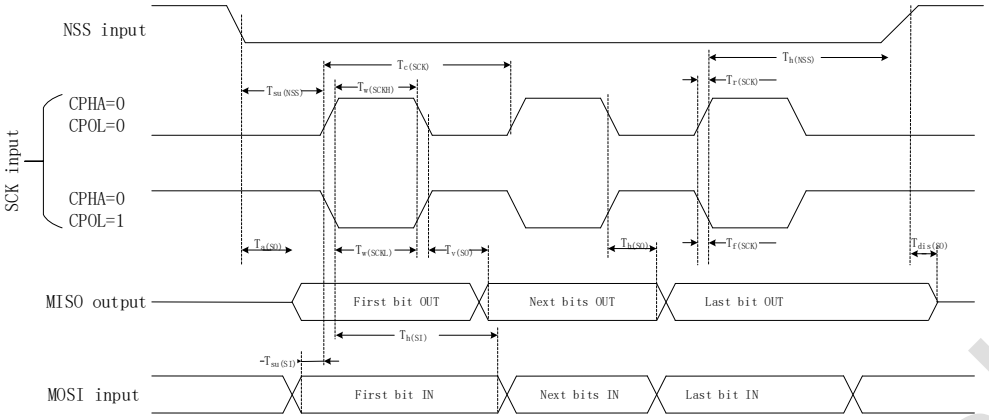


Figure 5-3 SPI timing diagram – Slave mode and CPHA=0

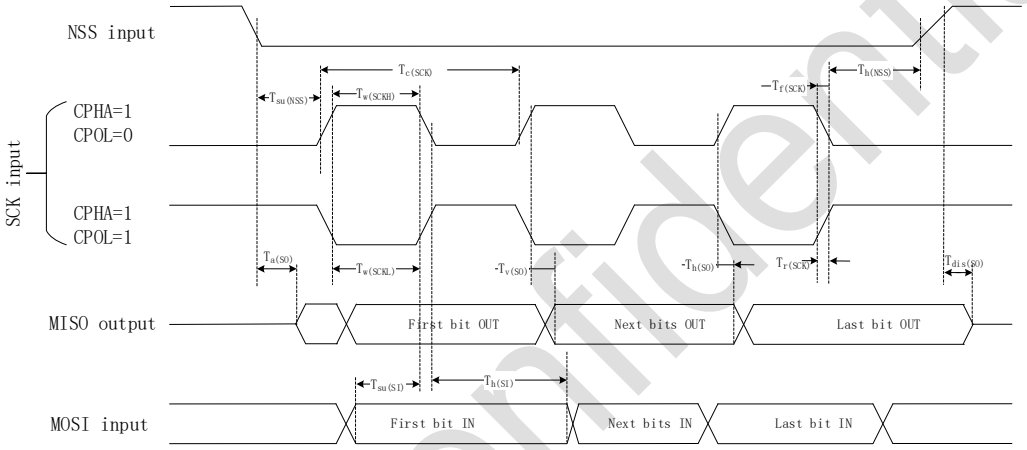


Figure 5-4 SPI timing diagram – Slave mode and CPHA=1

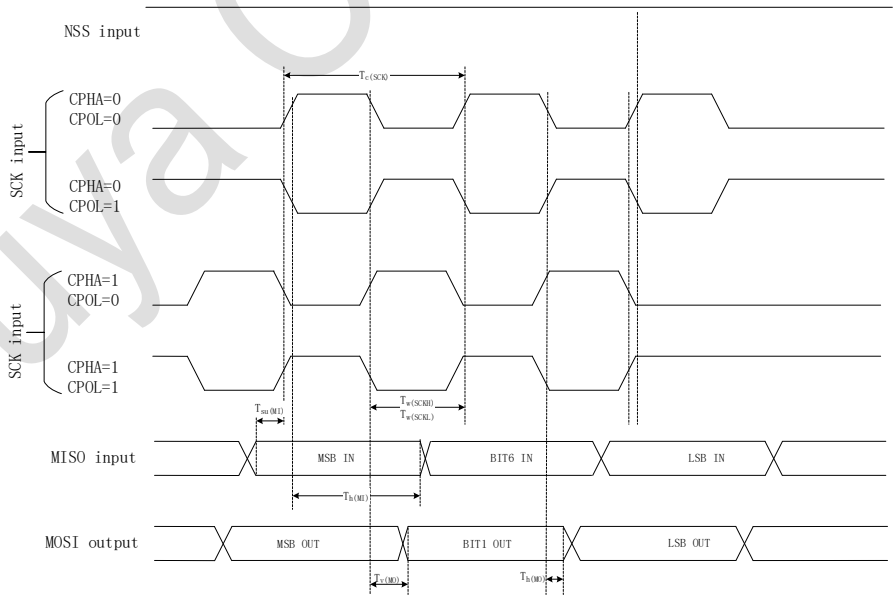


Figure 5-5 SPI timing diagram – Master mode

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5.3.20.3. I²S characteristics

Table 5-40 I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_S	I²S sampling frequency	-	8	192	kHz
f_{MCLK}	I²S main clock output	-	256 x f_s	256 x f_s	kHz
f_{CK} $1/t_{c(CK)}$	I²S clock frequency	Master data	-	64 x f_s	kHz
		Slave master	-	64 x f_s	
D_{CK}	I²S clock frequency duty cycle	Slave receiver	30	70	%
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load C_L = 50 pF	-	8	ns
$t_{v(WS)}$	W_S valid time	Master mode	-	2	
$t_{h(WS)}$	W_S hold time	Master mode	3	-	
		Slave mode	2	-	
$t_{su(WS)}$	W_S setup time	Slave mode	4	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	3	-	
$t_{su(SD_SR)}$		Slave receiver	4	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD_SR)}$		Slave receiver	2	-	
$t_{v(SD_ST)}$	Data output valid time	Slave receiver (after enable edge)	-	20	
$t_{v(SD_MT)}$		Master receiver (after enable edge)	-	5	
$t_{h(SD_ST)}$	Data output hold time	Slave receiver (after enable edge)	2	-	
$t_{h(SD_MT)}$		Master receiver (after enable edge)	1	-	

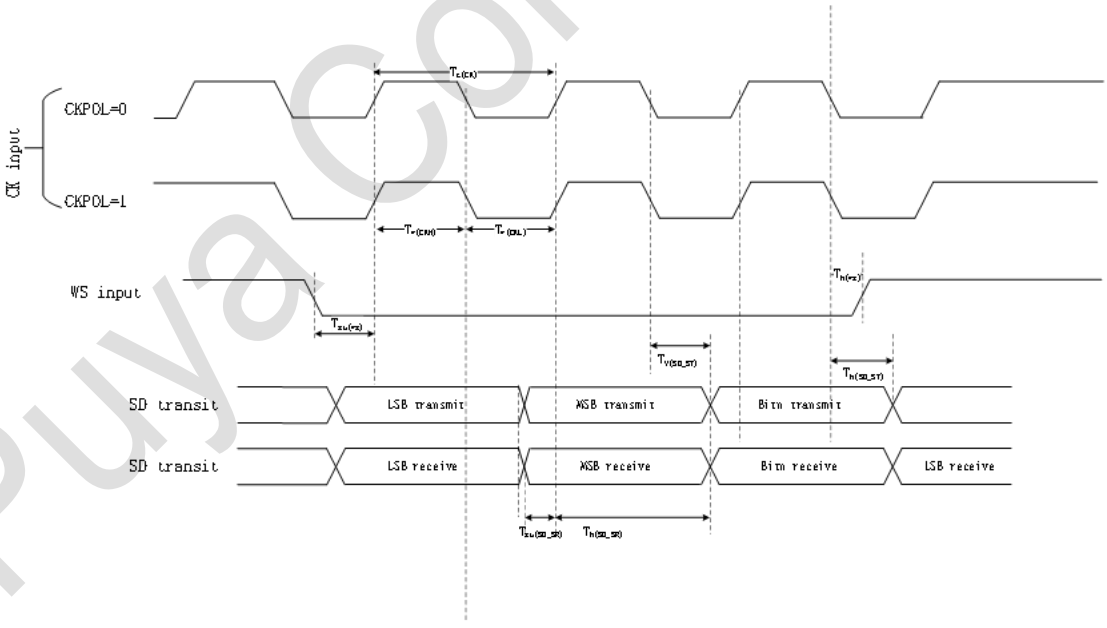


Figure 5-6 I²S slave timing diagram (Philips protocol)

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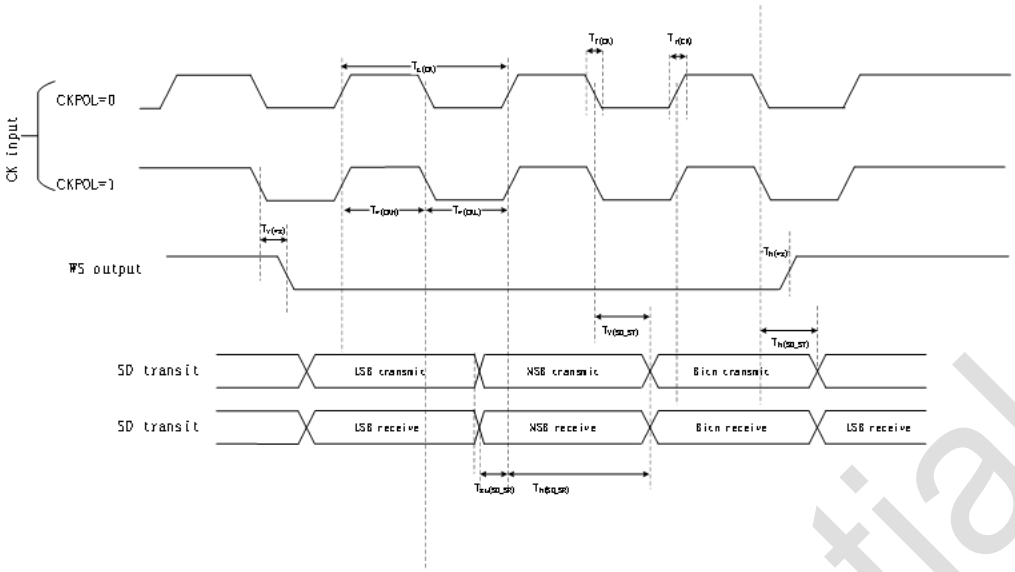


Figure 5-7 I²S master timing diagram (Philips protocol)

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5.4. Multifunction gate driver electrical characteristics

The gate driver is a three-phase brushless gate driver that can drive N+N MOS and operate at a power supply voltage of 5.5 to 26 V. The gate driver has a built-in 50 mA LDO that can provide power to the MCU or other devices.

The gate driver features built-in shoot-through prevention and a 100 ns dead time to prevent shoot-through of the driven high- and low-side MOSFETs, effectively protecting the power devices.

The gate driver also features a built-in input voltage V_{IN}/V_B under-voltage lockout (UVLO) function, which can effectively prevent the power devices from operating at excessively low voltages.

5.4.1. Drive logic control

The gate driver features input/output high- and low-side channel matching. The HINx input channel is active high and controls the high-side HOx output; the LINx input channel is active high and controls the low-side LOx output.

Table 5-41 Logic control truth table

HINx	LINx	HOx	LOx
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

5.4.2. Switching time

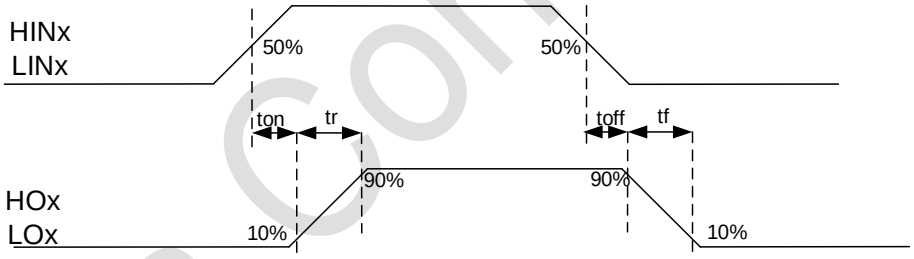
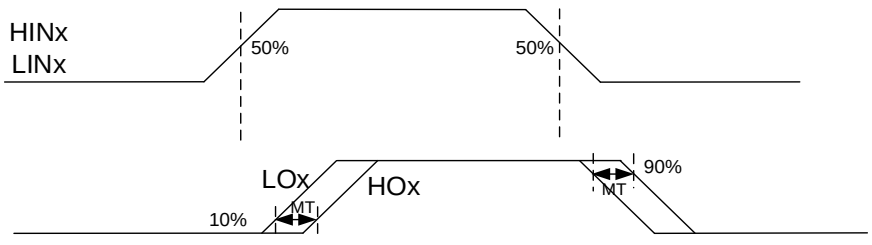


Figure 5-8 Switching time

5.4.3. Shoot-through protection

The gate driver is internally designed with a dedicated protection circuit to prevent shoot-through of the power devices, effectively preventing shoot-through damage caused by interference to the high-side and low-side input signals.



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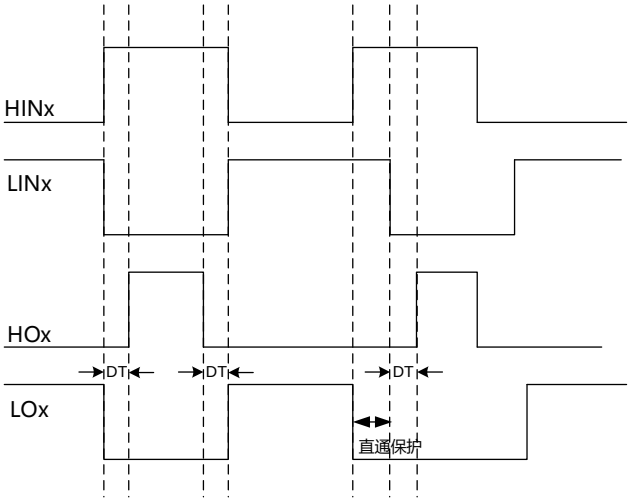


Figure 5-9 Shoot-through protection

5.4.4. Dead time function

A fixed dead time protection circuit is set inside the gate driver. During the dead time, both the high-side and low-side outputs are set to a low level. The set dead time must ensure that one power device is turned off before the other is turned on, effectively preventing shoot-through between the upper and lower power devices. If the logic input has an external dead time set and this time is greater than the chip's internal dead time (100 ns), the external logic input's dead time is used as the chip's dead time; if the logic input has an external dead time set and this time is less than the chip's internal dead time (100 ns), the chip's internal dead time (100 ns) shall prevail.

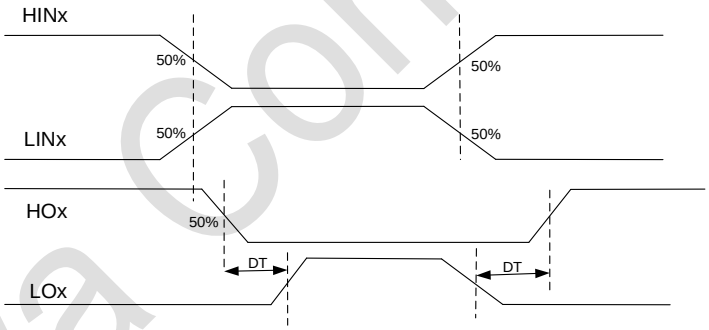


Figure 5-10 Dead time function

5.4.5. Absolute maximum ratings

Table 5-42 Absolute maximum ratings

Symbol	Descriptions	Min	Max	Unit
V_{IN}	Low-side supply voltage	-0.3 to 29		V
V_{Bx}	High-side floating supply	-0.3 to 150		V
V_{Sx}	High-side floating reference ground	-8 to 150		V
V_{LDO5}	5V LDO output voltage range	-0.3 to 5.5		V
V_{LDO12}	12V LDO input/output voltage range	-0.3 to 17		V
$V_{HIN1,2,3}$	High-side control input voltage	-0.3 to V_{LDO5} +0.3		V
$V_{LIN1,2,3}$	Low-side control input voltage	-0.3 to V_{LDO5} +0.3		V
$V_{HO1,2,3}$	High-side gate driver output voltage	V_{Sx}-0.3 to V_{Bx}+0.3		V
$V_{LO1,2,3}$	Low-side gate driver output voltage	-0.3 to V_{IN}+0.3		V

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5.4.6. Recommended operating conditions

Table 5-43 Recommended operating conditions

Symbol	Descriptions	Min	Typ	Max	Unit
V_{IN}	Low-side supply voltage	5.5	21	26	V
V_{Bx}	High-side floating absolute voltage	V_{Sx}+5.5	-	150	V
V_{Sx}	High-side floating offset voltage	-0.3	-	150	V
V_{LDO5}	5V LDO output voltage range	-	5.0	-	V
V_{LDO12}	12V LDO input/output voltage range	-	12.0	15	V
$V_{HIN1,2,3}$	High-side control input voltage	0	-	V_{LDO5}	V
$V_{LIN1,2,3}$	Low-side control input voltage	0	-	V_{LDO5}	V

5.4.7. Electrical characteristics

Note: Unless otherwise specified, T_A=25 ℃, V_{IN}=15 V, V_{LDO12}=12 V, V_{Sx}=V_{GND}, C_L=1nF.

Table 5-44 Electrical characteristics table

Symbol	Descriptions	Min	Typ	Max	Unit
Electrical Characteristics					
I_{VIN}	V_{IN} operating current, H_{INX}=L_{INX}=20 kHz	-	300	-	μA
I_{VINQ}	V_{IN} quiescent current, H_{INX}=L_{INX}=0 V	-	200	-	μA
I_{VBS}	V_{BS} operating current, H_{INX}=L_{INX}=20 kHz	-	300	-	μA
I_{VBSQ}	V_{BS} quiescent current, H_{INX}=L_{INX}=0 V	-	200	-	μA
V_{SN}	V_S static negative voltage	-	-8	-	V
LDO5					
V_{LDO5}	5V LDO output voltage, I_{OUT}=1 mA, V_{LDO12}=12 V	-	5	-	V
I_{OUT}	5V LDO output current capability, V_{LDO12}=12 V, V_{OUT}>95 % * V_{REG}	-	-	50	mA
Load regulation	1 mA≤I_{OUT}<50 mA	-	100	-	mV
Line regulation	8 V≤V_{VIN}<18 V	-	-	10	mV
LDO12					
V_{LDO12}	12V LDO output voltage, I_{OUT}=1 mA	-	12	-	V
I_{OUT2}	Maximum output current	-	300	-	mA
Three-phase gate driver					
V_{IL}	Logic input low voltage	-	-	1.2	V
V_{IH}	Logic input high voltage	2.5	-	-	V
VCCSUV+	V_{IN} undervoltage protection trigger voltage	-	4.6	-	V
VCCSUV-	V_{IN} undervoltage protection recovery voltage	-	4.9	-	V
VBSUV+	V_B undervoltage protection trigger voltage	-	3.9	-	V
VBSUV-	V_B undervoltage protection recovery voltage	-	4.1	-	V
V_{UVLO_HYS}	V_{IN}/V_B undervoltage lockout hysteresis	-	0.3	-	V
I_{LK}	Floating supply leakage current V_{Bx}=V_{Sx}=150 V	-	0.1	5	μA
I_{LIN+}	LIN high-level input bias current V_{LIN}=5 V	-	50	-	μA
I_{LIN-}	LIN low-level input bias current V_{LIN}=0 V	-	-	1	μA
I_{HIN+}	HIN high-level input bias current V_{HIN}=5 V	-	50	-	μA
I_{HIN-}	HIN low-level input bias current V_{HIN}=0 V	-	-	1	μA

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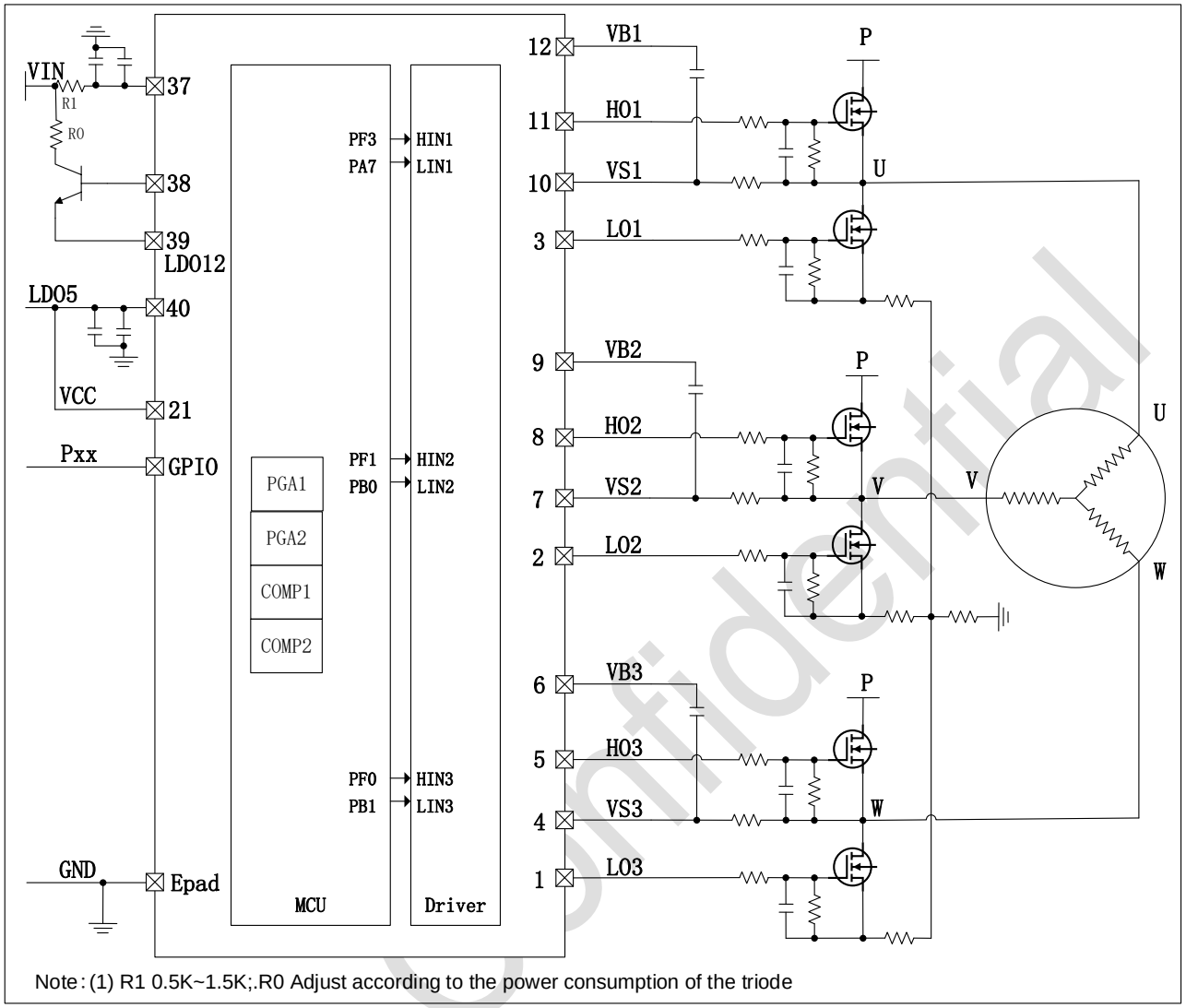
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Symbol	Descriptions	Min	Typ	Max	Unit
R_{PD}	Weak pull-down equivalent resistor	-	100	-	kΩ
I_{DRIVEP}	IO output current	-	1.0	-	A
I_{DRIVEN}	IO output current	-	-1.0	-	A
t_{DT}	Dead time	-	100	-	ns
t_r	Output rise time, C_L=1000 pF	-	35	-	ns
t_f	Output fall time, C_L=1000 pF	-	15	-	ns
t_{on}	Output rising edge propagation time	-	200	-	ns
t_{off}	Output falling edge propagation time	-	100	-	ns
MT	High and low side delay matching	-	10	-	ns

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6. Application circuit



Note: (1) R1 0.5K~1.5K;.R0 Adjust according to the power consumption of the triode

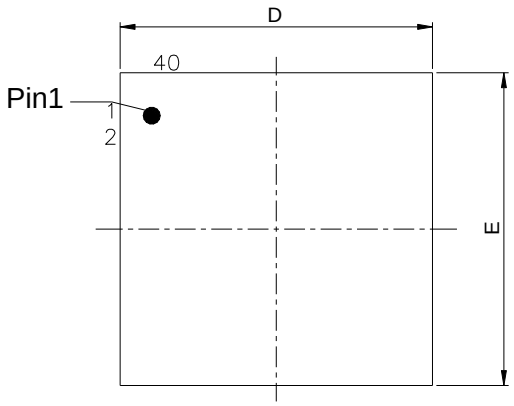
Figure 6-1 PY32MD530H2 recommended application circuit diagram

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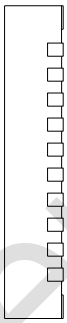
7. Package information

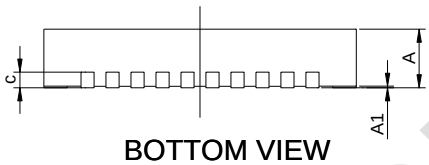
7.1. QFN40 package size

TOP VIEW

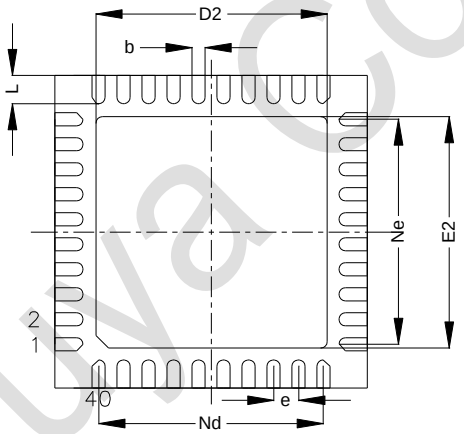


SIDE VIEW





BOTTOM VIEW



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	-	0.020	0.050
b	0.150	0.200	0.250
c	0.200REF		
D	4.900	5.000	5.100
D2	3.600	3.700	3.800
E	4.900	5.000	5.100
E2	3.600	3.700	3.800
e	0.400BSC		
Nd	3.600BSC		
Ne	3.600BSC		
L	0.350	0.400	0.450

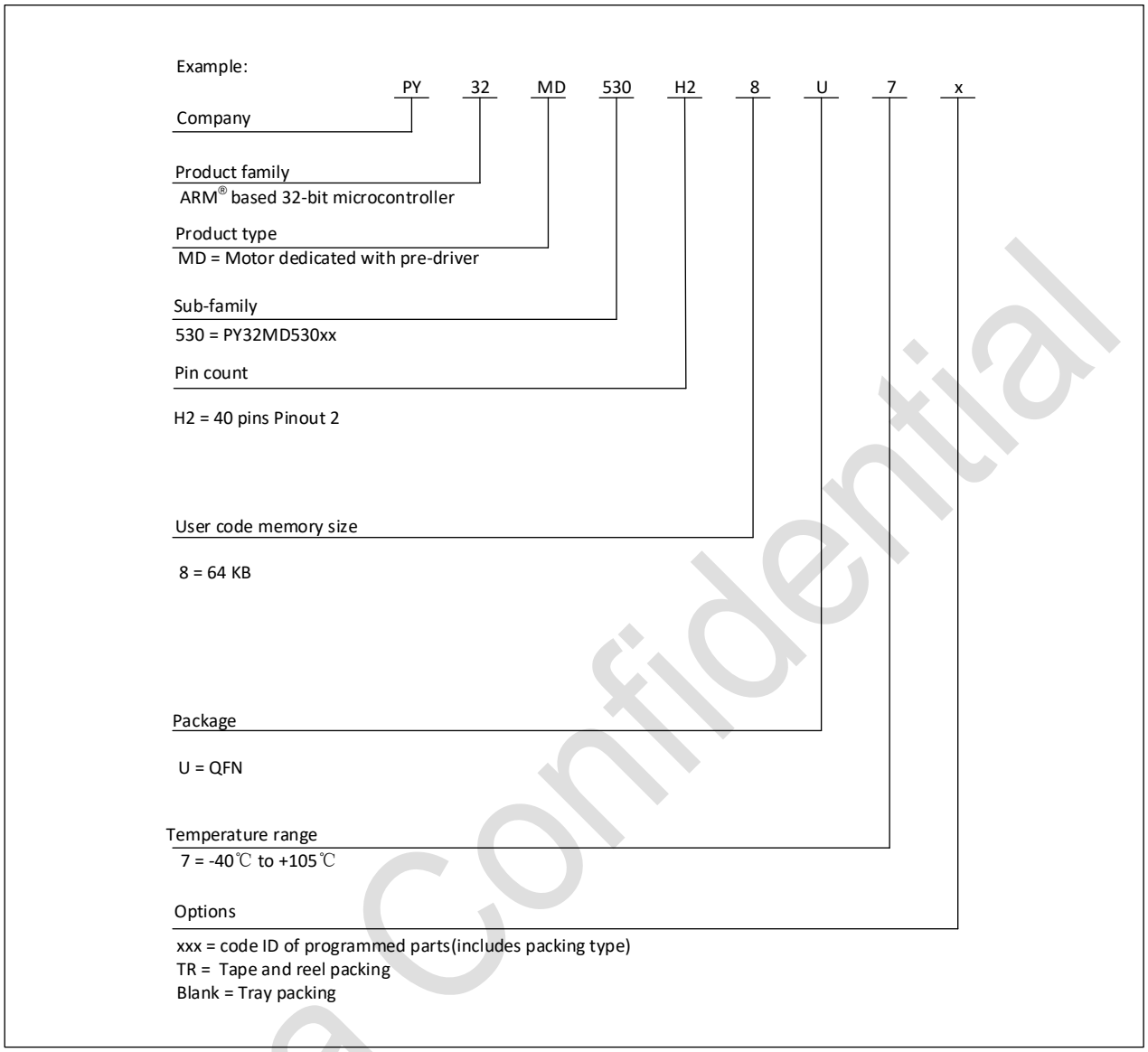
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN40L 5X5X0.75-0.4PITCH POD	QRPD-0075	1.1

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8. Ordering information



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9. References

For the latest version of the MCU datasheet, please refer to the "PY32F032 Datasheet"

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10. Version history

Version	Date	Descriptions
V0.2	2025.12.31	Initial version
V0.3	2026.04.27	Updated application circuit diagram
V0.4	2026.05.25	Updated operational amplifier parameters

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