PY32MD310 Datasheet

32-bit ARM® Cortex®-M0+ Microcontroller

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Puya Semiconductor (Shanghai) Co., Ltd.

Features

- Core
  - — 32-bit ARM® Cortex®-M0+
  - — Frequency up to 48 MHz
- Memories
  - — 64 KB Flash memory
  - — 8 KB SRAM
- Clock management
  - — 4/8/16/22.12/24 MHz High-speed internal RC oscillator (HSI)
  - — 32.768 kHz low-speed internal RC oscillator (LSI)
  - — 4 to 32 MHz High-speed external crystal oscillator (HSE)
  - — PLL (supports 2 multiplication of HSI or HSE)
- Power management and reset
  - — Operating voltage: 2.0 to 5.5 V
  - — Low-power modes: Sleep/Stop
  - — Power-on/power-down reset (POR/PDR)
  - — Brown-out reset (BOR)
  - — Programmable voltage detector (PVD)
- General-purpose input and output (I/O)
  - — Up to 16 I/Os, all available as external interrupts
- 3-channel DMA controller
- 1 x 12-bit ADC
  - — Up to 7 external channels
  - — Input voltage conversion range: 0 to V_{CC}
- Timers
  - — 1 x 16-bit advanced-control timer (TIM1)
  - — 4 x 16-bit general-purpose timers (TIM3/TIM14/TIM16/TIM17)
  - — 1 x low-power timer (LPTIM), supporting wake-up from Stop mode
  - — 1 x independent watchdog timer (IWDG)
  - — 1 x window watchdog timer (WWDG)
  - — 1 x SysTick timer
  - — 1 x IRTIM
- RTC
- Communication interfaces
  - — 2 x serial peripheral interfaces (SPI)
  - — 2 x universal synchronous/asynchronous resceiver/transmitters (USART) with automatic baud rate detection
  - — 1 x I^2C interface, supporting Standard mode (100 kHz) and Fast mode (400 kHz), with 7-bit addressing mode
- Hardware CRC-32 module
- 2 x comparators
- Built-in multi-function three-phase PN half-bridge pre-driver
  - — Recommended operating voltage: 6 to 36 V
  - — LDO: 5 V/50 mA
- Unique UID
- Serial wire debug (SWD)
- Operating temperature: -40 to 105 °C
- Packages: QFN32, SSOP24

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1. Introduction

The PY32MD310 microcontrollers feature the high-performance 32-bit ARM® Cortex®-M0+ core operating at up to 48 MHz frequency, embed up to 64 KB Flash and 8 KB SRAM, and are available in multiple package options. The PY32MD310 integrates multi-channel I^2C, SPI, USART and other communication peripherals, one 12-bit ADC, five 16-bit timers, and two comparators.

The PY32MD310 microcontrollers operates across a temperature range of -40 to 105 °C and a voltage range of 2.0 to 5.5 V. It provides Sleep and Stop modes to meet the needs of different low-power applications.

The PY32MD310 microcontrollers are suitable for three-phase/single-phase BLDC/PMSM drive control. Common application scenarios are listed as follows: blowers, ceiling fans, pedestal fans, water pumps, power tools, model aircraft, etc.

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Table 1-1 PY32MD310 series product features and peripheral counts

Peripherals		PY32MD310K18U7	PY32MD310E18M7
Flash (KB)		64	64
SRAM(KB)		8	8
Timers	Advanced-control	1 (16-bit)	
	General-purpose	4 (16-bit)	
	Low power	1	
	SysTick	1	
	Watchdog	2	
Comm. interfaces	SPI	2	1
	I^2C	1	
	USART	2	
DMA		3 ch	
RTC		Yes	
GPIOs		16	8
ADC (external + internal)		6+2	7+2
Comparators		2	
Max. CPU frequency		48 MHz	
Operating voltage		2.0 to 5.5 V	
Operating temperature		-40 to 105 °C	
Packages		QFN32	SSOP24

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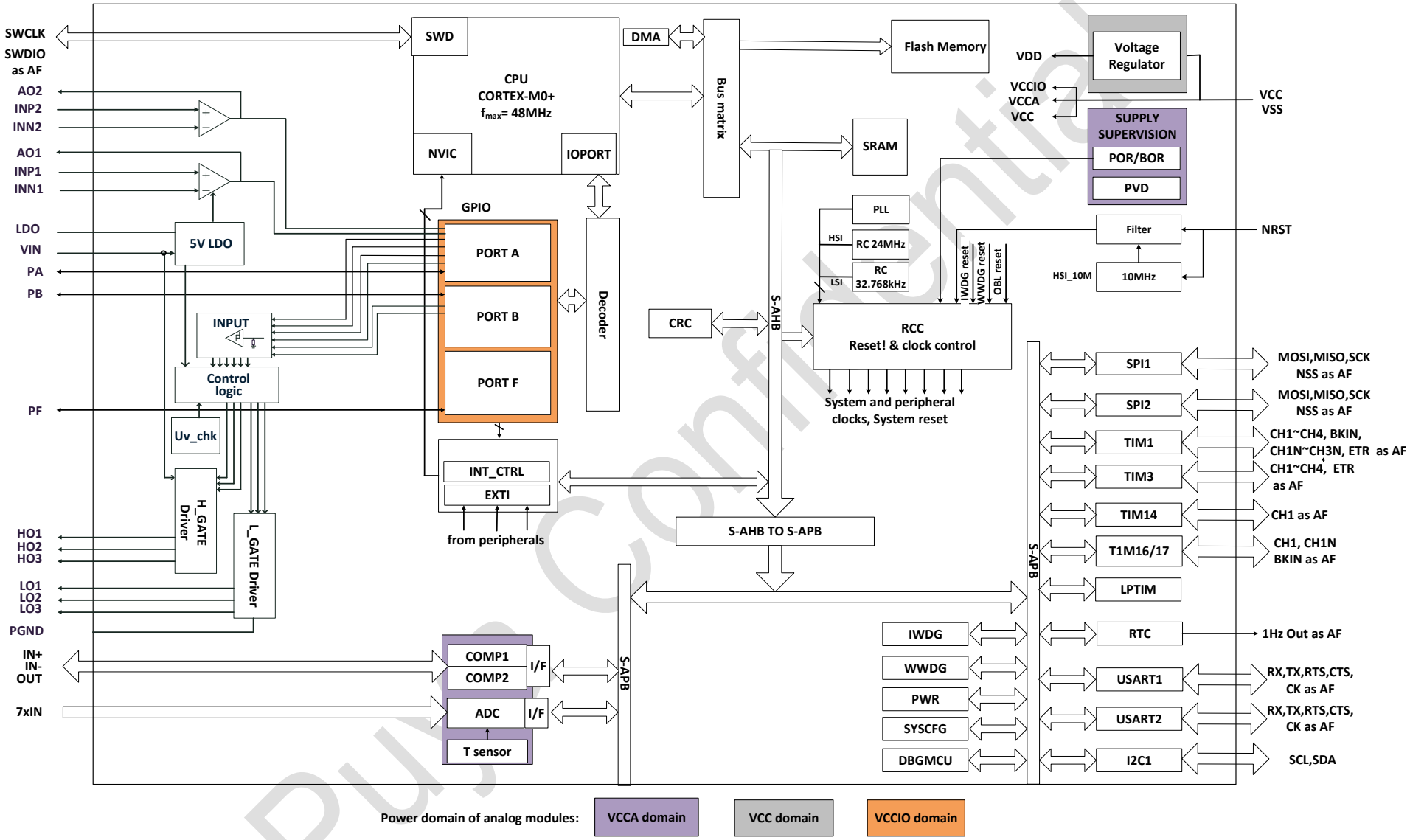


Figure 1-1 System block diagram

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2. Functional overview

2.1. Arm® Cortex®-M0+ core

The Arm® Cortex®- M0+ is an Arm 32-bit Cortex processor designed for embedded applications. It provides developers with significant benefits, including:

- Simple architecture for easy learning and programming
- Ultra-low power consumption for energy-efficient operation
- Reduced code density

The Arm® Cortex®-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. It delivers high performance through a streamlined instruction set and hardware enhancements like a single-cycle multiplier, while achieving higher code density than other 8/16-bit MCUs.

The Arm® Cortex®-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC).

2.2. Memories

Embedded SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits).

The Flash memory is composed of two distinct physical areas:

- The Main flash area consists of application and user data
- 4 KB of Information area:
  - Option bytes
  - UID bytes
  - System memory

The protection of Main flash memory includes the following mechanisms:

- Read protection (RDP) blocks external access.
- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 4 KB.
- Option byte write protection is a special design for unlock.

2.3. Clock management

After CPU startup, the default system clock frequency is HSI 8 MHz. The system clock frequency and system clock source can be reconfigured once the program is running. The frequency clocks that can be selected are:

- A 4/8/16/22.12/24 MHz internal high-precision HSI clock
- A 32.768 kHz configurable internal LSI clock
- A 4 to 32 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. A CPU NMI interrupt is generated at the same time.

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- PLL clock has HSE and HSI sources. If the HSE source is selected, when CSS is enabled and CSS fails, the PLL and HSE will be turned off, and the hardware selects the system clock source as HSI.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The maximum frequency of the AHB and the APB domains is 48 MHz.

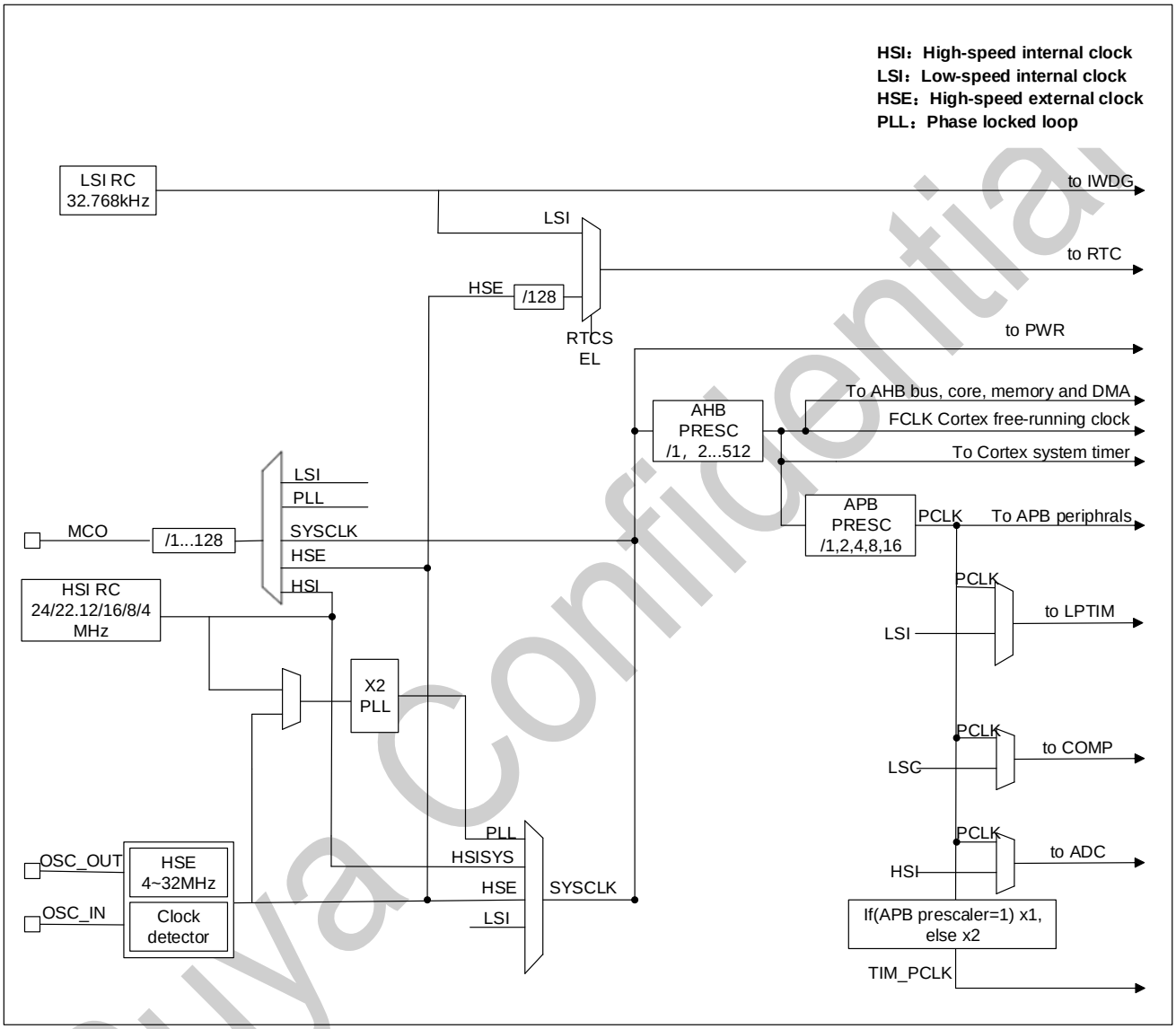


Figure 2-1 System clock structure diagram

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2.4. Power management

2.4.1. Power block diagram

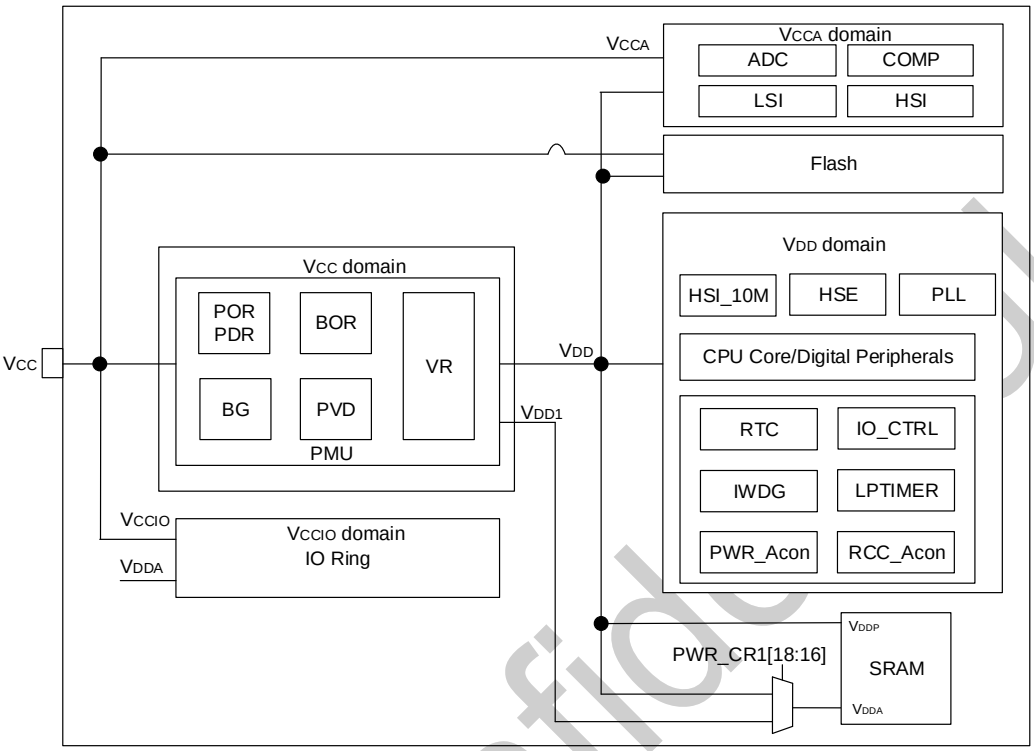


Figure 2-2 Power block diagram

Table 2-1 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	2.0 V to 5.5 V	The power is supplied to the chip through the power pins, with the power supply module comprising: Partial analog circuits
2	V_{CCA}	2.0 V to 5.5 V	Powers for most analog modules, sourced from the V_{CC} PAD (a dedicated power PAD can also be designed separately).
3	V_{CCIO}	2.0 V to 5.5 V	Power to IO from V_{CC} PAD
4	V_{DDD}	1.2 V	VR supplies power to the main logic circuits and SRAM inside the chip. When the MR is powered, it outputs 1.2 V. According to the software configuration, when entering the Stop mode, it powered by MR or LPR, and the LPR output is determined by software.

2.4.2. Power monitoring

2.4.2.1. Power-on/power-down reset (POR/PDR)

The POR/PDR module, which provides power-on and power-down reset, remains active in all modes.

2.4.2.2. Brown-out reset (BOR)

In addition to POR/PDR, BOR (Brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte.

When the BOR is turned on, the BOR threshold can be selected by the option byte.

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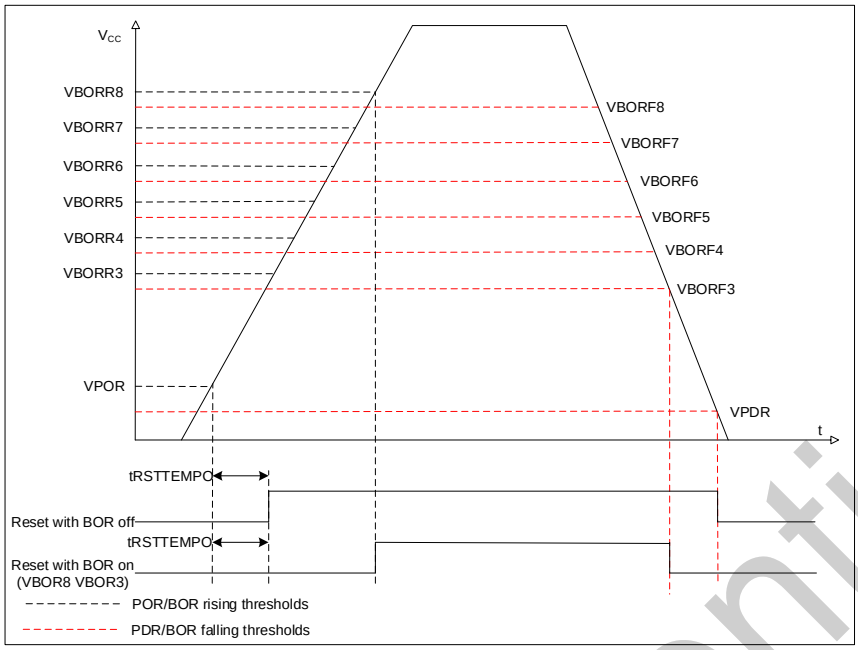


Figure 2-3 POR/PDR/BOR threshold

2.4.2.3. Programmable voltage detector (PVD)

Programmable voltage detector (PVD) module can be used to detect the V_{CC} power supply (or detect the voltage on the PB7 pin), with the detection point configurable via registers. The device remains in reset mode when the monitored supply voltage V_{CC} is below a specified threshold.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when V_{CC} rises above the detection point of PVD, or V_{CC} falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

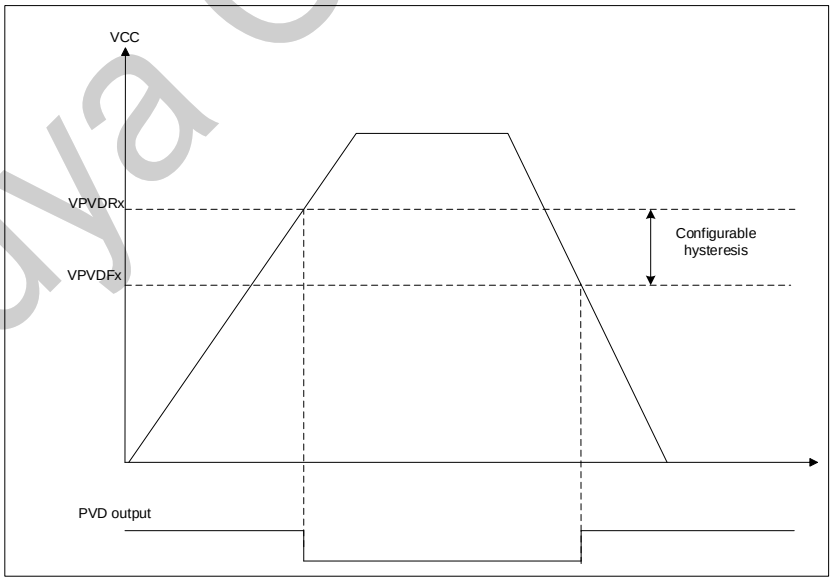


Figure 2-4 PVD threshold

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2.4.3. Voltage regulator

The regulator has two operating modes:

- Main regulator (MR) is used in Run mode.
- Low power regulator (LPR) provides an option for even lower power consumption in Stop mode.

2.4.4. Low-power mode

In addition to the Run mode, the device has two low-power modes:

- **Sleep mode**: Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc. are operating). It is recommended to enable only essential modules and disable them after task completion.
- **Stop mode:** In this mode, SRAM and register contents are retained. PLL, HSI and HSE are turned off and most module clocks in the V_{DD} domain are disabled. GPIO, PVD, COMP output, RTC, and LPTIM can wake up the Stop mode.

2.5. Reset

Two resets are designed in the chip: power reset and system reset.

2.5.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out reset (BOR)

2.5.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load (OBL) reset

2.6. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating, pull-up or pull-down and analog) or as peripheral alternate function. The I/O configuration can be locked.

2.7. DMA

Direct memory access (DMA) is used to provide a high-speed data transfer between peripherals and memory as well as from memory to memory.

The DMA controller have 3 channels in total, each one dedicated to manage memory access requests from one or more peripherals. The DMA controller includes an arbiter to handle DMA requests, which manages the priority of each DMA request.

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DMA supports circular buffer management, eliminating the need for user code intervention when the controller reaches the end of the buffer.

Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.

DMA can be used for major peripherals: SPI, I^2C, USART, ADC and all TIMx timers (except TIM14 and LPTIM).

2.8. Interrupts and events

The PY32MD310 handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.8.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Support 1 NMI
- Support 23 maskable external interrupts
- Support 6 Cortex-M0+ exceptions
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.8.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from Stop mode.

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The EXTI controller has multiple channels, including up to 16 GPIOs, 1 PVD output, 2 COMP outputs, as well as RTC and LPTIM Wake-up signals. GPIO, PVD and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 15 channel through the select signal.

- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.9. Analog-to-digital converter (ADC)

The device has a 12-bit SAR-ADC. The module has a total of up to 9 channels to be measured, including 7 external and 2 internal channels.

A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.

An efficient low-power mode is implemented to allow very low consumption at low frequency.

Interrupt requests are triggered by the following events: end of sampling, conversion, continuous conversion and Analog watchdog threshold violation (converted voltage exceeds preset limits)

2.10. Comparators (COMP)

General purpose comparators are integrated, which can be used in combination with Timer. Comparators can be used as:

- Triggered by analog signal to wake-up function from low-power mode
- Analog signal conditioning
- Cycle by cycle current control loop when comparators are connected with PWM output from timer

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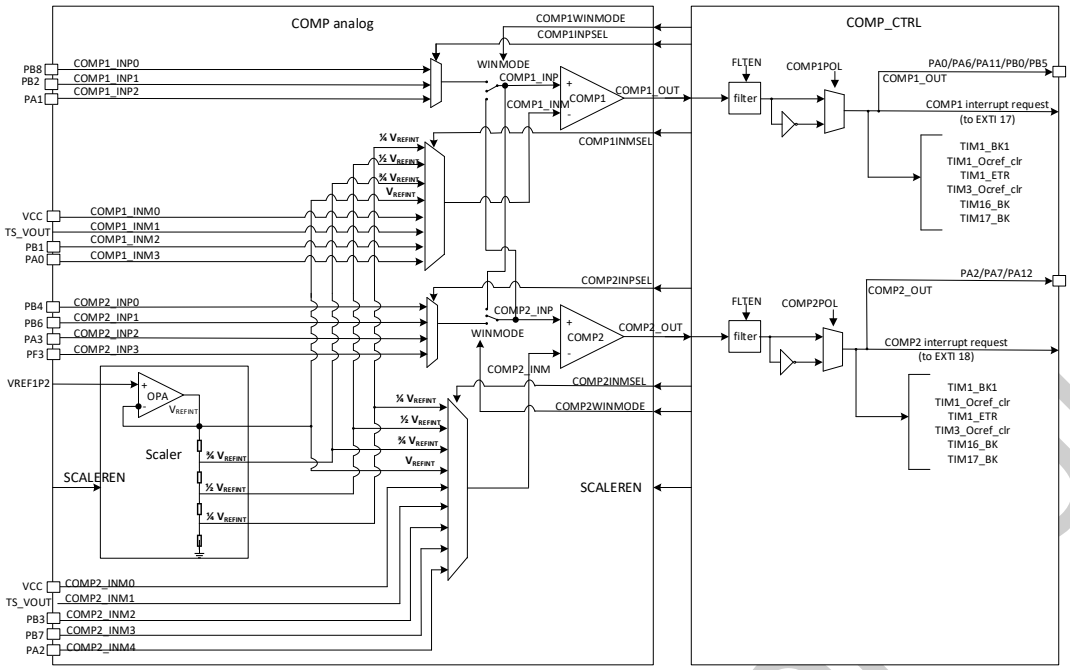


Figure 2-5 COMP block diagram

2.10.1. COMP main features

- Each comparator has configurable positive or negative input for flexible voltage selection:
  - Multiple I/O pins
  - Power supply V_{CC}
  - Output of the temperature sensor
  - Power supply V_{CC} and 3 fractional values provided by voltage division (1/4, 1/2 and 3/4).
- Configurable hysteresis function
- Programmable speed and consumption
- The output can be triggered by a connection to the I/O or timer input
  - OCREF_CLR event (cycle-by-cycle current control)
  - Brakes for fast PWM shutdown

Each COMP has interrupt generation capability and is used to wake up the device from low power mode (Sleep/Stop) (via EXTI)

2.11. Timers

The different timers feature as blow:

Table 2-2 Timer characteristics

Type	Timer	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Complementary outputs
Advanced-control	TIM1	16-bit	up, down, up/down	1 to 65536	Yes	4	3
General-purpose	TIM3	16-bit	up, down, up/down	1 to 65536	Yes	4	-
	TIM14	16-bit	up	1 to 65536	-	1	-
	TIM16,TIM17	16-bit	up	1 to 65536	Yes	1	1

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2.11.1. Advanced-control timer

The advanced-control timer (TIM1) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, TIM1/TIM8 have full modulation capability (0 to 100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the Timer Link feature for synchronization or event chaining.

TIM1 supports the DMA function.

2.11.2. General-purpose timers

2.11.2.1. TIM3

- The TIM3 general-purpose timer consists of a 16-bit auto-reload counter driven by a 16-bit programmable prescaler. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.
- TIM3 can work with the TIM1 by the Timer Link.
- TIM3 supports the DMA function.
- This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.
- The counter can be frozen in debug mode.

2.11.2.2. TIM14

- The general-purpose timer TIM14 is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM14 features two single channel for input capture/output compare, PWM or one-pulse mode output.
- The counter can be frozen in debug mode.

2.11.2.3. TIM16/TIM17

- TIM16 and TIM17 consist of a 16-bit auto-reload counter driven by a programmable prescaler.

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- TIM16/TIM17 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- TIM16/TIM17 have complementary outputs with dead time.
- TIM16/TIM17 supports DMA function.
- The counter can be frozen in debug mode.

2.11.3. Low power timer

- LPTIM is a 16 -bit upcounter with a 3-bit prescaler and support a single count.
- LPTIM can be configured as a Stop mode wake-up source.
- The counter can be frozen in debug mode.

2.11.4. IWDG

- Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.
- The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.
- The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, but have lower timing accuracy constraints.
- The IWDG hardware mode can be enabled by option byte.
- IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.
- The counter can be frozen in debug mode.

2.11.5. WWDG

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

2.11.6. SysTick timer

SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.12. Real-time clock (RTC)

The RTC is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

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- RTC is a 32-bit programmable counter with a prescaler factor of up to 2^{20} bits.
- RTC counter clock source can be LSI and the stop wake-up source.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).
- RTC supports clock calibration.
- RTC can be frozen in debug mode.

2.13. Inter-integrated circuit interface (I^2C)

The Inter-integrated circuit (I^2C) bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard mode (Sm) and Fast mode (Fm).

I^2C features:

- Support Slave and Master mode
  - Support different communication speeds
  - Standard mode (Sm): up to 100 kHz
  - Fast Mode (Fm): up to 400 kHz
- As master
  - Generate clock
  - Generation of start and stop
- As Slave
  - Programmable I^2C address detection
  - Discovery of the STOP bit
- 7-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I^2C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching
- Single-byte buffer with DMA capability
- Software reset
- Analog noise filter function

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2.14. Universal synchronous/asynchronous receiver transmitter (USART)

The PY32MD310 contains two USARTs, and the two function exactly the same.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate shared by transmit
- Automatic baud rate detection
- Programmable data length of 8 or 9 bits
- Configurable STOP bit (1 or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Receive/transmit bytes by DMA buffer
- Transfer detection flag
  - Receive buffer full
  - Send empty buffer
  - End of transmission flags
- Parity control
  - Transmit parity bit
  - Check the received data byte
- Flagged interrupt sources
  - CTS change
  - Transmit data register empty
  - Transmission complete

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  - Receive full data register
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Detection error
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

2.15. Serial peripheral interface (SPI)

PY32MD310 contains 2 SPIs.

The serial peripheral interface (SPI) protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- Master mode frequency up to $f_{PCLK}/4$
- Slave mode frequency up to $f_{PCLK}/4$
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Interrupt-causing Master mode faults or overloads
- Two 32-bit Rx and Tx FIFOs with DMA capability

2.16. SWD

An ARM SWD interface allows serial debugging tools to be connected to the PY32MD310.

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3. Pinouts and pin descriptions

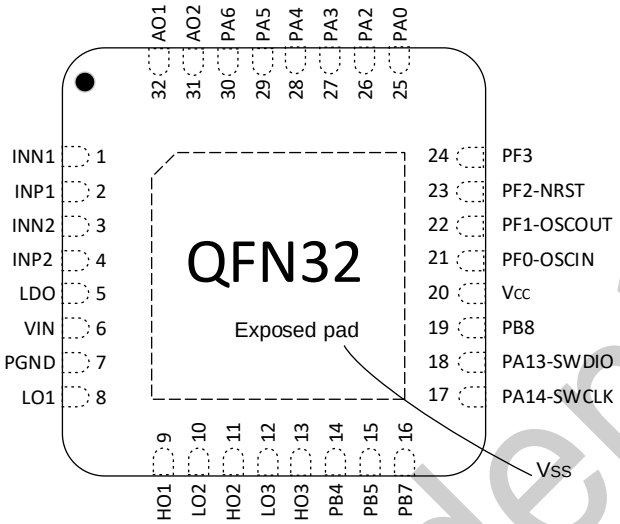


Figure 3-1 QFN32 Pinout1 PY32MD310K1xU7 (Top view)

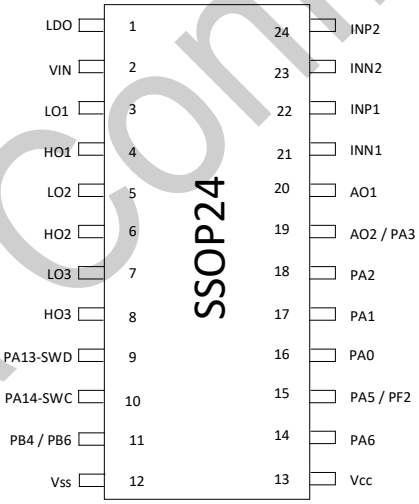


Figure 3-2 SSOP24 Pinout1 PY32MD310E1xM7 (Top view)

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Table 3-1 Legend/abbreviations used in the pinout table

Type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I/O	Input/output pin
		NC	No internal connection
I/O structure		COM	Standard 5 V I/O, supporting analog input/output functions
		NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		-	Unless otherwise specified, all ports are used as analog inputs between and after reset
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers

Table 3-2 Legend/abbreviations used for the Gate Driver pin definitions

Packages		Pin name	Pin function
QFN32 K1	SSOP24 E1		
1	21	INN1	Channel 1 low-offset op-amp negative input
2	22	INP1	Channel 1 low-offset op-amp positive input
3	23	INN2	Channel 2 low-offset op-amp negative input
4	24	INP2	Channel 2 low-offset op-amp positive input
5	1	LDO	5 V LDO output, external 1 μF capacitor to ground
6	2	VIN	Input operating power supply, externally connected to a 1 μF capacitor to ground
7	-	PGND	Power ground, connected to gate driver
8	3	LO1	Channel 1 low-side gate driver output
9	4	HO1	Channel 1 high-side gate driver output
10	5	LO2	Channel 2 low-side gate driver output
11	6	HO2	Channel 2 high-side gate driver output
12	7	LO3	Channel 3 low-side gate driver output
13	8	HO3	Channel 3 high-side gate driver output
31	19	AO2	Channel 2 low-offset op-amp output
32	20	AO1	Channel 1 low-offset op-amp output

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Table 3-3 QFN32 pin definitions

Packages	IO	Driver	Pin type	I/O structure	Pin functions		
QFN32 K1					Notes	Alternate functions	Additional functions
1	-	INN1	-	-	-	-	-
2	-	INP1	-	-	-	-	-
3	-	INN2	-	-	-	-	-
4	-	INP2	-	-	-	-	-
5	-	LDO	-	-	-	-	-
6	-	VIN	-	-	-	-	-
7	-	PGND	-	-	-	-	-
8	PA10	LO1	-	-	-	TIM1_CH3	-
9	PB1	HO1	-	-	-	TIM1_CH3N	-
10	PA8	LO2	-	-	-	TIM1_CH1	-
11	PA7	HO2	-	-	-	TIM1_CH1N	-
12	PB3	LO3	-	-	-	TIM1_CH2	-
13	PA1	HO3	-	-	-	TIM1_CH2N	-
21	PF0-OSC _ IN-(PF0)	-	I/O	COM	-	SPI2_SCK USART2_RX TIM14_CH1 USART1_RX USART2_TX I^2C_SDA	OSC_IN
22	PF1-OSC_OUT-（PF1）	-	I/O	COM	-	SPI2_MISO USART2_TX USART1_TX USART2_RX I^2C_SCL SP1_NSS TIM14_CH1	OSC_OUT
23	PF2-NRST	-	I/O	NRST	(1)	MCO SPI2_MOSI USART2_RX	NRST
24	PF3	-	I/O	COM	-	USART1_TX USART2_TX SPI2_MISO SPI1_NSS TIM3_CH3 RTC_OUT	COMP2_INP
25	PA0	-	I/O	COM	-	SPI2_SCK USART1_CTS USART2_CTS COMP1_OUT	ADC_IN0COMP1_INM

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Packages	IO	Driver	Pin type	I/O structure	Pin functions		
QFN32 K1					Notes	Alternate functions	Additional functions
						TIM1_CH3	
						TIM1_CH1N	
						SPI1_MISO	
						USART2_TX	
						IR_OUT	
26	PA2	-	I/O	COM	-	SPI1_MOSI	COMP2_INM ADC_IN2
						USART1_TX	
						USART2_TX	
						COMP2_OUT	
						SPI1_SCK	
						TIM3_CH1	
						I^2C_SDA	
27	PA3	-	I/O	COM	-	SPI2_MISO	COMP2_INP ADC_IN3
						USART1_RX	
						USART2_RX	
						EVENTOUT	
						SPI1_MOSI	
						TIM1_CH1	
						I^2C_SCL	
28	PA4	-	I/O	COM	-	SPI1_NSS	ADC_IN4
						USART1_CK	
						SPI2_MOSI	
						TIM14_CH1	
						USART2_CK	
						ENENTOUT	
						RTC_OUT	
						TIM3_CH3	
						USART2_TX	
29	PA5	-	I/O	COM	-	SPI1_SCK	ADC_IN5
						LPTIM_ETR	
						EVENTOUT	
						TIM3_CH2	
						USART2_RX	
						MCO	
30	PA6	-	I/O	COM	-	SPI1_MISO	ADC_IN6
						TIM3_CH1	
						TIM1_BKIN	
						TIM16_CH1	
						COMP1_OUT	
						USART1_CK	

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Packages	IO	Driver	Pin type	I/O structure	Pin functions		
QFN32 K1					Notes	Alternate functions	Additional functions
						RTC_OUT	
20	V_{CC}	-	S	-	-	Digital power supply	
18	PA13 (SWDIO)	-	I/O	COM	(2)	SWDIO	-
						IR_OUT	
						EVENTOUT	
						SPI1_MISO	
						TIM1_CH2	
						USART1_RX	
						MCO	
17	PA14 (SWCLK)	-	I/O	COM	(2)	SWCLK	-
						USART1_TX	
						USART2_TX	
						EVENTOUT	
						MCO	
14	PB4	-	I/O	COM	-	SPI1_MISO	COMP2_INP
						TIM3_CH1	
						USART2_CTS	
						USART1_CTS	
						TIM17_BKIN	
						EVENTOUT	
15	PB5	-	I/O	COM	-	SPI1_MOSI	-
						TIM3_CH2	
						TIM16_BKIN	
						USART2_CK	
						USART1_CK	
						LPTIM_IN1	
						COMP1_OUT	
16	PB7	-	I/O	COM	-	USART1_RX	COMP2_INMPVD_IN
						SPI2_MOSI	
						TIM17_CH1N	
						USART2_RX	
						I^2C_SDA	
						EVENTOUT	
19	PB8	-	I/O	COM	-	SPI2_SCK	COMP1_INP
						TIM16_CH1	
						I2C1_SCL	
						USART2_TX	
						EVENTOUT	
						USART1_TX	
						SPI2_NSS	

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Packages	IO	Driver	Pin type	I/O structure	Pin functions		
QFN32 K1					Notes	Alternate functions	Additional functions
						I^2C_SDA	
						TIM17_CH1	
						IR_OUT	
31	-	AO2	-	-	-	-	-
32	-	AO1	-	-	-	-	-

1. Configured by option bytes to choose PF2 or NRST.
2. After reset, PA13 and PA14 are configured as SWDIO AF and SWCLK functions, the former has an internal pull-up resistor and the latter has an internal pull-down resistor activated.

Table 3-4 SSOP24 pin definitions

Packages	IO	Driver	Pin type	I/O structure	Pin functions		
SSOP24 E1					Notes	Alternate functions	Additional functions
1	-	LDO	-	-	-	-	-
2	-	VIN	-	-	-	-	-
3	PA10	LO1	-	-	-	TIM1_CH3	-
4	PB1	HO1	-	-	-	TIM1_CH3N	-
5	PA9	LO2	-	-	-	TIM1_CH2	-
6	PB0	HO2	-	-	-	TIM1_CH2N	-
7	PA8	LO3	-	-	-	TIM1_CH1	-
8	PA7	HO3	-	-	-	TIM1_CH1N	-
9	PA13 (SWDIO)	-	I/O	COM	(2)	SWDIO	-
						IR_OUT	
						EVENTOUT	
						SPI1_MISO	
						TIM1_CH2	
						USART1_RX	
						MCO	
10	PA14 (SWCLK)	-	I/O	COM	(2)	SWCLK	
						USART1_TX	
						USART2_TX	
						EVENTOUT	
						MCO	
11	PB4	-	I/O	COM	(3)	SPI1_MISO	COMP2_INP
						TIM3_CH1	
						USART2_CTS	
						USART1_CTS	
						TIM17_BKIN	
						EVENTOUT	

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Packages	IO	Driver	Pin type	I/O structure	Pin functions		
SSOP24 E1					Notes	Alternate functions	Additional functions
11	PB6	-	I/O	COM	(3)	USART1_TX TIM1_CH3 TIM16_CH1N USART2_TX SPI2_MISO I²C_SCL LPTIM_ETR EVENTOUT	COMP2_INP
12	VSS	-	G	-	-	Ground	
13	V_{CC}	-	S	-	-	Digital power supply	
14	PA6	-	I/O	COM	-	SPI1_MISO TIM3_CH1 TIM1_BKIN TIM16_CH1 COMP1_OUT USART1_CK RTC_OUT	ADC_IN6
15	PF2-NRST	-	I/O	NRST	(1)(3)	MCO SPI2_MOSI USART2_RX	NRST
15	PA5	-	I/O	COM	(3)	SPI1_SCK LPTIM_ETR EVENTOUT TIM3_CH2 USART2_RX MCO	ADC_IN5
16	PA0	-	I/O	COM	-	SPI2_SCK USART1_CTS USART2_CTS COMP1_OUT TIM1_CH3 TIM1_CH1N SPI1_MISO USART2_TX IR_OUT	ADC_IN0COMP1_INM
17	PA1	-	I/O	COM	-	SPI1_SCK USART1_RTS USART2_RTS LED_DATA_C	COMP1_INP ADC_IN1

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Packages	IO	Driver	Pin type	I/O structure	Pin functions		
SSOP24 E1					Notes	Alternate functions	Additional functions
						EVENTOUT	
						SPI1_MOSI	
						USART2_RX	
						TIM1_CH4	
						TIM1_CH2N	
						MCO	
18	PA2	-	I/O	COM	-	SPI1_MOSI	COMP2_INM ADC_IN2
						USART1_TX	
						USART2_TX	
						COMP2_OUT	
						SPI1_SCK	
						TIM3_CH1	
						I^2C_SDA	
19	PA3	-	I/O	COM	-	-	COMP2_INP ADC_IN3
19	-	AO2	-	-	-	-	-
20	PA4	AO1	-	-	-	-	ADC_IN4
21	-	INN1	-	-	-	-	-
22	-	INP1	-	-	-	-	-
23	-	INN2	-	-	-	-	-
24	-	INP2	-	-	-	-	-

1. Configured by option bytes to choose PF2 or NRST.
2. After reset, PA13 and PA14 are configured as SWDIO AF and SWCLK functions, the former has an internal pull-up resistor and the latter has an internal pull-down resistor activated.
3. Two IO ports are brought out on the same pin. Only one of the IO ports can be used at the same time, and the other IO must be configured in analog mode (MODEy[1:0] = 0b11).

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3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-5 Port A alternate functions mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI2_SCK	USART1_CTS	-	-	USART2_CTS	-	-	COMP1_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_TX	SPI1_MISO	-	-	TIM1_CH3	TIM1_CH1N	IR_OUT
PA1	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	USART1_RTS	-	-	USART2_RTS	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_RX	SPI1_MOSI	-	-	TIM1_CH4	TIM1_CH2N	MCO
PA2	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	USART1_TX	-	-	USART2_TX	-	-	COMP2_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_SCK	-	I^2C_SDA	TIM3_CH1	-	-
PA3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_MISO	USART1_RX	-	-	USART2_RX	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_MOSI	-	I^2C_SCL	TIM1_CH1	-	-
PA4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_NSS	USART1_CK	SPI2_MOSI	-	TIM14_CH1	USART2_CK	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_TX	-	-	-	TIM3_CH3	-	RTC_OUT
PA5	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	-	-	-	-	LPTIM1_ETR	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	USART2_RX	-	-	-	TIM3_CH2	-	MCO
PA6	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	-	COMP1_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_CK	-	-	-	-	-	-	RTC_OUT
PA7	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	USART2_TX	SPI1_MISO	-	I^2C_SDA	-	-	-
PA8	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_NSS	USART1_CK	TIM1_CH1	-	USART2_CK	MCO	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	USART2_RX	SPI1_MOSI	-	I^2C_SCL	-	-	-

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PA9	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_MISO	USART1_TX	TIM1_CH2	-	USART2_TX	MCO	I²C_SCL	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	-	SPI1_SCK	-	I²C_SDA	TIM1_BKIN	-	-
PA10	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI2_MOSI	USART1_RX	TIM1_CH3	-	USART2_RX	TIM17_BKIN	I²C_SDA	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	-	SPI1_NSS	-	I²C_SCL	-	-	-
PA11	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MISO	USART1_CTS	TIM1_CH4	-	USART2_CTS	EVENTOUT	I²C_SCL	COMP1_OUT
PA12	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	USART1_RTS	TIM1_ETR	-	USART2_RTS	EVENTOUT	I²C_SDA	COMP2_OUT
PA13	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SWDIO	IR_OUT	-	-	-	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	-	SPI1_MISO	-	-	TIM1_CH2	-	MCO
PA14	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SWCLK	USART1_TX	-	-	USART2_TX	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	-	-	-	-	-	MCO
PA15	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_NSS	USART1_RX	-	-	USART2_RX	-	-	EVENTOUT

3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-6 Port B alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI1_NSS	TIM3_CH3	TIM1_CH2N	-	-	EVENTOUT	-	COMP1_OUT
PB1	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	EVENTOUT
PB2	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_RX	SPI2_SCK	-	USART2_RX	-	-	-	-
PB3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_SCK	TIM1_CH2	-	USART1_RTS	USART2_RTS	-	-	EVENTOUT
PB4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MISO	TIM3_CH1	-	USART1_CTS	USART2_CTS	TIM17_BKIN	-	EVENTOUT
PB5	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	USART1_CK	USART2_CK	LPTIM_IN1	-	COMP1_OUT
PB6	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_TX	TIM1_CH3	TIM16_CH1N	SPI2_MISO	USART2_TX	LPTIM_ETR	I²C_SCL	EVENTOUT

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PB7	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_RX	SPI2_MOSI	TIM17_CH1N	-	USART2_RX	-	I^2C_SDA	EVENTOUT
PB8	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	SPI2_SCK	TIM16_CH1	-	USART2_TX	-	I^2C_SCL	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	-	-	SPI2_NSS	I^2C_SDA	TIM17_CH1	-	IR_OUT

3.3. Alternate functions selected through GPIOF_AFR registers for port F

Table 3-7 Port F alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0-OSC_IN	-	-	TIM14_CH1	SPI2_SCK	USART2_RX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	USART2_TX	-	-	I^2C_SDA	-	-	-
PF1_OSC_OUT	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	SPI2_MISO	USART2_TX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	USART2_RX	SPI1_NSS	-	I^2C_SCL	TIM14_CH1	-	-
PF2-NRST	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	SPI2_MOSI	USART2_RX	-	MCO	-
PF3	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	USART1_TX	-	-	SPI2_MISO	USART2_TX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	SPI1_NSS	-	-	TIM3_CH3	-	RTC_OUT
PF4	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
	-	-	-	-	-	-	-	-

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4. Memory mapping

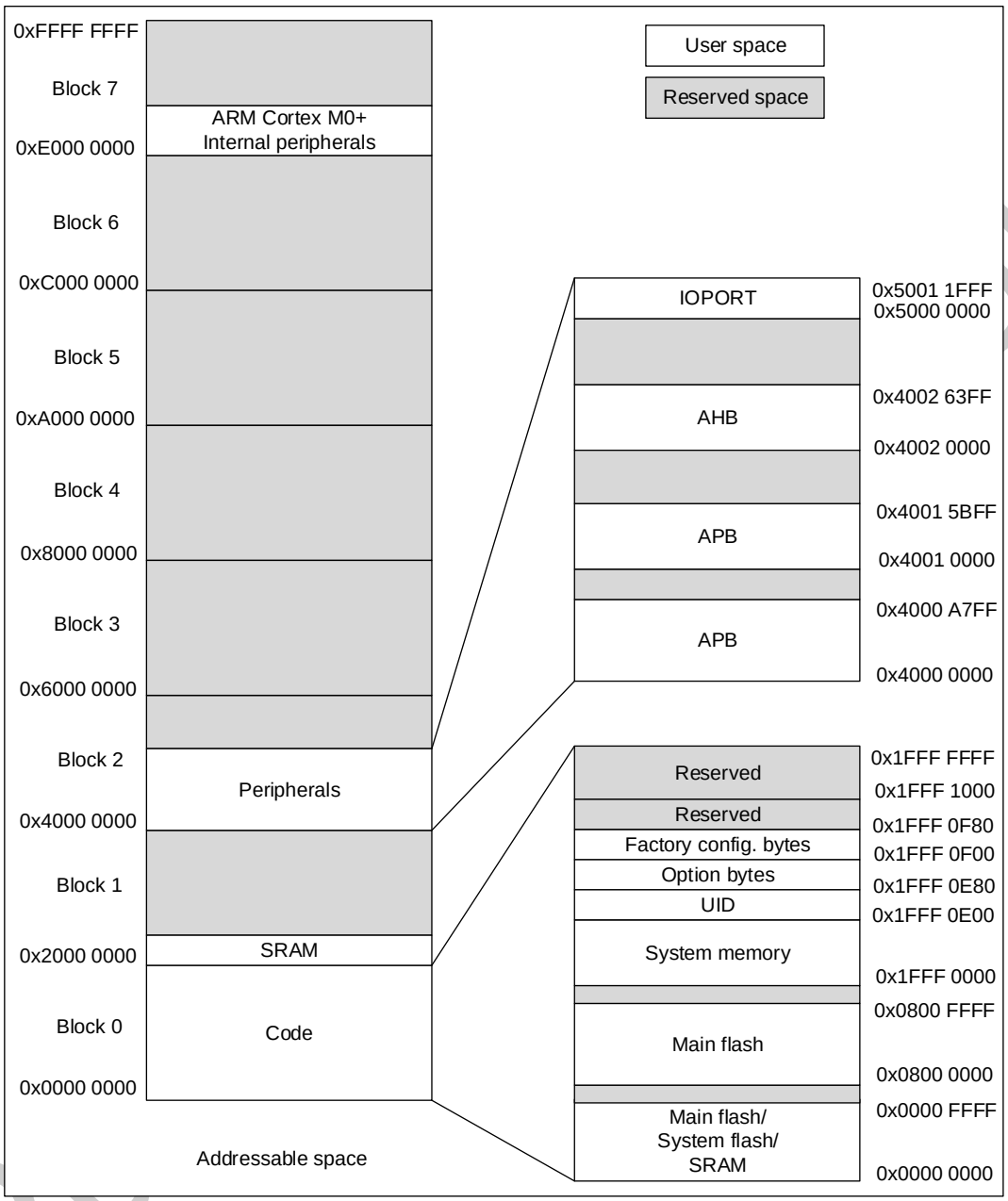


Figure 4-1 Memory mapping

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Table 4-1 Memory boundary address

Type	Boundary Address	Size	Memory area	Description
SRAM	0x2000 2000-0x3FFF FFFF	-	Reserved	-
	0x2000 0000-0x2000 1FFF	8 KB	SRAM	SRAM up to 8 KB depending on hardware
Code	0x1FFF 1000-0x1FFF FFFF	-	Reserved	-
	0x1FFF 0F80-0x1FFF 0FFF	128 bytes	Reserved	-
	0x1FFF 0F00-0x1FFF 0F7F	128 bytes	Factory config. bytes	HSI trimming data, Flash erase/write time configuration parameters
	0x1FFF 0E80-0x1FFF 0EFF	128 bytes	Option bytes	Option byte
	0x1FFF 0E00-0x1FFF 0E7F	128 bytes	UID	Unique ID
	0x1FFF 0000-0x1FFF 0DFF	-	Reserved	-
	0x0801 0000-0x1FFF FFFF	-	Reserved	-
	0x0800 0000-0x0800 FFFF	64 KB	Main flash memory	-
	0x0001 0000-0x07FF FFFF	-	Reserved	-
	0x0000 0000-0x0000 FFFF	64 KB	Main flash memory	-

Table 4-2 Peripheral register address

Bus	Boundary Address	Size	Peripheral
	0xE000 0000-0xE00F FFFF	-	M0+
IOPORT	0x5000 1800-0x5FFF FFFF	-	Reserved
	0x5000 1400-0x5000 17FF	1 KB	GPIOF
	0x5000 0800-0x5000 13FF	-	Reserved
	0x5000 0400-0x5000 07FF	1 KB	GPIOB
	0x5000 0000-0x5000 03FF	1 KB	GPIOA
AHB	0x4002 3400-0x4FFF FFFF	-	Reserved
	0x4002 300C-0x4002 33FF	1 KB	Reserved
	0x4002 3000-0x4002 3008		CRC
	0x4002 2400-0x4002 2FFF	-	Reserved
	0x4002 2124-0x4002 23FF	1 KB	Reserved
	0x4002 2000-0x4002 2120		Flash
	0x4002 1C00-0x4002 1FFF	-	Reserved
	0x4002 1888-0x4002 1BFF	1 KB	Reserved
	0x4002 1800-0x4002 1884		EXTI
	0x4002 1400-0x4002 17FF	-	Reserved
	0x4002 1064-0x4002 13FF	1 KB	Reserved
	0x4002 1000-0x4002 1060		RCC
	0x4002 0C00-0x4002 0FFF	-	Reserved
	0x4002 0040-0x4002 03FF	1 KB	Reserved
	0x4002 0000-0x4002 003C		DMA
APB	0x4001 5C00-0x4001 FFFF	-	Reserved

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Bus	Boundary Address	Size	Peripheral
	0x4001 5880-0x4001 5BFF	1 KB	Reserved
	0x4001 5800-0x4001 587F		DBG
	0x4001 4C00-0x4001 57FF	-	Reserved
	0x4001 4850-0x4001 4BFF	1 KB	Reserved
	0x4001 4800-0x4001 484C		TIM17
	0x4001 4450-0x4001 47FF	1 KB	Reserved
	0x4001 4400-0x4001 404C		TIM16
	0x4001 3C00-0x4001 43FF	2 KB	Reserved
	0x4001 381C-0x4001 3BFF	1 KB	Reserved
	0x4001 3800-0x4001 3018		USART1
	0x4001 3400-0x4001 37FF	-	Reserved
	0x4001 3010-0x4001 33FF	1 KB	Reserved
	0x4001 3000-0x4001 300C		SPI1
	0x4001 2C50-0x4001 2FFF	1 KB	Reserved
	0x4001 2C00-0x4001 2C4C		TIM1
	0x4001 2800-0x4001 2BFF	-	Reserved
	0x4001 270C-0x4001 27FF	1 KB	Reserved
	0x4001 2400-0x4001 2708		ADC
	0x4001 0400-0x4001 23FF	-	Reserved
	0x4001 0220-0x4001 03FF	1 KB	Reserved
	0x4001 0200-0x4001 021F		COMP1 and COMP2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 8000-0x4000 FFFF	-	Reserved
	0x4000 7C28-0x4000 7FFF	1 KB	Reserved
	0x4000 7C00-0x4000 7C24		LPTIM
	0x4000 7400-0x4000 7BFF	-	Reserved
	0x4000 7018-0x4000 73FF	1 KB	Reserved
	0x4000 7000-0x4000 7014		PWR
	0x4000 5800-0x4000 6FFF	-	Reserved
	0x4000 5434-0x4000 57FF	1 KB	Reserved
	0x4000 5400-0x4000 5430		I^2C
	0x4000 4800-0x4000 53FF	-	Reserved
	0x4000 441C-0x4000 47FF	1 KB	Reserved
	0x4000 4400-0x4000 4418		USART2
	0x4000 3C00-0x4000 43FF	-	Reserved
	0x4000 3810-0x4000 3BFF	1 KB	Reserved
	0x4000 3800-0x4000 380C		SPI2
	0x4000 3400-0x4000 37FF	-	Reserved
	0x4000 3014-0x4000 33FF	1 KB	Reserved

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Bus	Boundary Address	Size	Peripheral
	0x4000 3000-0x4000 0010		IWDG
	0x4000 2C0C-0x4000 2FFF	1 KB	Reserved
	0x4000 2C00-0x4000 2C08		WWDG
	0x4000 2830-0x4000 2BFF	1 KB	Reserved
	0x4000 2800-0x4000 282C		RTC
	0x4000 2420-0x4000 27FF	-	Reserved
	0x4000 2400-0x4000 241C		Reserved
	0x4000 2054-0x4000 23FF	1 KB	Reserved
	0x4000 2000-0x4000 0050		TIM14
	0x4000 1400-0x4000 1FFF	-	Reserved
	0x4000 1030-0x4000 13FF	-	Reserved
	0x4000 1000-0x4000 102C		Reserved
	0x4000 0800-0x4000 0FFF	-	Reserved
	0x4000 0450-0x4000 07FF	1 KB	Reserved
	0x4000 0400-0x4000 044C		TIM3
	0x4000 0000-0x4000 03FF	-	Reserved

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5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_{A(max)}$ (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation.

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A = 25°C and V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated.

5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Descriptions	Min	Max	Unit
V_{CC}	External mains power supply	-0.3	6.25	V
V_{IN}	Input voltage of other pins	-0.3	V_{CC}+0.30	V

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply in the permitted range.

Table 5-2 Current characteristics

Symbol	Descriptions	Max	Unit
I_{VCC}	Total current into V_{CC} pin (supply current)(1)	100	mA
I_{VSS}	Total current flowing out of the V_{SS} pin (sink current)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any COM I/O and control pin(2)	20	
	Total output current sourced by sum of all I/Os and control pins	-20	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply in the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.

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Table 5-3 Thermal characteristics

Symbol	Descriptions	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	℃
T_J	Maximum junction temperature	150	℃

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	MHz
V_{CC}	Standard operating voltage	-	2.0	5.5	V
V_{IN}	I/O input voltage	-	-0.3	V_{CC}+0.3	V
T_A	Ambient temperature	-	-40	105	℃
T_J	Junction temperature	-	-40	125	℃

5.3.2. Operating conditions at power-on/power-down

Table 5-5 Operating conditions at power-on/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise rate	-	10	∞	μs/V
	V_{CC} fall rate	-	20	∞	

5.3.3. Embedded reset and PVD module characteristics

Table 5-6 Embedded reset characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization	-	-	4.0	7.5	ms
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.50(2)	1.60	1.70	V
		Falling edge	1.45(1)	1.55	1.65(2)	
V_{BOR1}	BOR1 threshold	Rising edge	Reserved			V
		Falling edge				
V_{BOR2}	BOR2 threshold	Rising edge				V
		Falling edge				
V_{BOR3}	BOR3 threshold	Rising edge	2.10(2)	2.20	2.30	V
		Falling edge	2.00	2.10	2.20(2)	
V_{BOR4}	BOR4 threshold	Rising edge	2.30(2)	2.40	2.50	V
		Falling edge	2.20	2.30	2.40(2)	
V_{BOR5}	BOR5 threshold	Rising edge	2.50(2)	2.60	2.70	V
		Falling edge	2.40	2.50	2.60(2)	
V_{BOR6}	BOR6 threshold	Rising edge	2.70(2)	2.80	2.90	V
		Falling edge	2.60	2.70	2.80(2)	
V_{BOR7}	BOR7 threshold	Rising edge	2.90(2)	3.00	3.10	V
		Falling edge	2.80	2.90	3.00(2)	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR8}	BOR8 threshold	Rising edge	3.10(2)	3.20	3.30	V
		Falling edge	3.00	3.10	3.20(2)	
V_{PVD0}	PVD0 threshold	Rising edge	Reserved			V
		Falling edge				
V_{PVD1}	PVD1 threshold	Rising edge				V
		Falling edge				
V_{PVD2}	PVD2 threshold	Rising edge	2.10(2)	2.20	2.30	V
		Falling edge	2.00	2.10	2.20(2)	
V_{PVD3}	PVD3 threshold	Rising edge	2.30(2)	2.40	2.50	V
		Falling edge	2.20	2.30	2.40(2)	
V_{PVD4}	PVD4 threshold	Rising edge	2.50(2)	2.60	2.70	V
		Falling edge	2.40	2.50	2.60(2)	
V_{PVD5}	PVD5 threshold	Rising edge	2.70(2)	2.80	2.90	V
		Falling edge	2.60	2.70	2.80(2)	
V_{PVD6}	PVD6 threshold	Rising edge	2.90(2)	3.00	3.10	V
		Falling edge	2.80	2.90	3.00(2)	
V_{PVD7}	PVD7 threshold	Rising edge	3.10(2)	3.20	3.30	V
		Falling edge	3.00	3.10	3.20(2)	
$V_{POR_PDR_hyst}$(1)	POR/PDR hysteresis	-	-	50	-	mV
$V_{PVD_BOR_hyst}$(1)	PVD hysteresis	-	-	100	-	mV
$I_{CC(PVD)}$	PVD power consumption	-	-	0.6	-	μA
$I_{CC(BOR)}$	BOR consumption	-	-	0.6	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

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5.3.4. Supply current characteristics

Table 5-7 Current consumption in Run mode

Symbol	Conditions						Typ(1)	Max	Unit
	System clock	Frequency	Code	Run	Peripheral Clock	Flash sleep			
I_{CC}(Run)	HSI	48 MHz	While(1)	Flash	ON	DISABLE	2.6	-	mA
					OFF	DISABLE	1.7	-	
		24 MHz			ON	DISABLE	1.5	-	
					OFF	DISABLE	0.9	-	
		16 MHz			ON	DISABLE	1.1	-	
					OFF	DISABLE	0.7	-	
		8 MHz			ON	DISABLE	0.7	-	
					OFF	DISABLE	0.5	-	
		4 MHz			ON	DISABLE	0.5	-	
					OFF	DISABLE	0.35	-	
	LSI	32.768 kHz			ON	DISABLE	170	-	µA
					OFF	DISABLE	170	-	
		32.768 kHz			ON	ENABLE	95	-	
					OFF	ENABLE	95	-	

1. Data based on characterization results, not tested in production.

Table 5-8 Current consumption in Sleep mode

Symbol	Conditions				Typ(1)	Max	Unit
	System clock	Frequency	Peripheral Clock	Flash sleep			
I_{CC}(Sleep)	HSI	48 MHz	ON	DISABLE	1.8	-	mA
			OFF	DISABLE	1.1	-	
		24 MHz	ON	DISABLE	1	-	
			OFF	DISABLE	0.6	-	
		16 MHz	ON	DISABLE	0.75	-	
			OFF	DISABLE	0.5	-	
		8 MHz	ON	DISABLE	0.5	-	
			OFF	DISABLE	0.35	-	
		4 MHz	ON	DISABLE	0.4	-	
			OFF	DISABLE	0.35	-	
	LSI	32.768 kHz	ON	DISABLE	170	-	µA
			OFF	DISABLE	170	-	
		32.768 kHz	ON	ENABLE	95	-	
			OFF	ENABLE	96	-	

1. Data based on characterization results, not tested in production.

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Table 5-9 Current consumption in Stop mode

Symbol	Conditions					Typ(1)	Max	Unit
	V_{CC}	VDD	MR/LPR	LSI	Peripheral Clock			
I_{CC}(Stop)	2.0 to 5.5 V	1.2 V	MR	-	-	70	-	μA
		1.2 V	LPR	ON	RTC+IWDG+LPTIM	6	-	
					IWDG	6	-	
					LPTIM	6	-	
					RTC	6	-	
				OFF	No	6	-	
		1.0 V		ON	RTC+IWDG+LPTIM	4.5	-	
					IWDG	4.5	-	
					LPTIM	4.5	-	
					RTC	4.5	-	
				OFF	No	4.5	-	

1. Data based on characterization results, not tested in production.

5.3.5. Wakeup time from low-power mode

Table 5-10 Wake-up time from low-power mode

Symbol	Parameter(1)		Conditions		Typ(2)	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode		-		10	-	CPU cycles
t_{WUSTOP}	Wake-up from Stop mode	MR	Run program in Flash, HSI (24 MHz) as system clock		3.5	-	μs
		LPR	Run program in Flash, HSI (24 MHz) as system clock	V_{CC}=1.2 V	6	-	
				V_{CC}=1.0 V	6	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data based on characterization results, not tested in production.

5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the device stops working, the corresponding I/O is used as a standard GPIO.

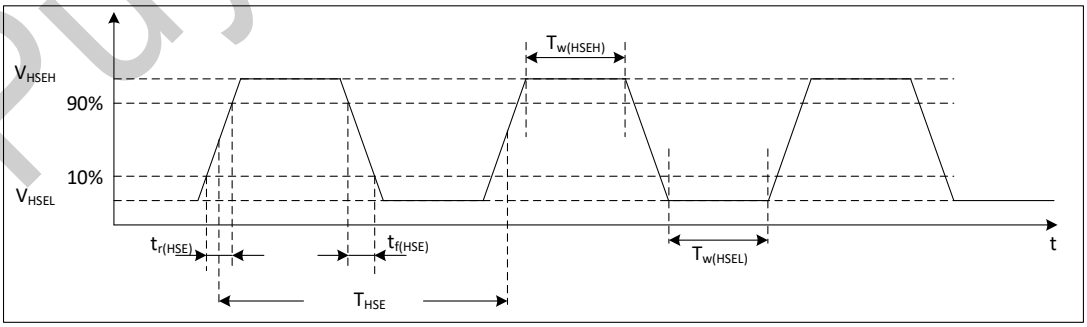


Figure 5-1 High-speed external clock timing diagram

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Table 5-11 High-speed external clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	1	8	32	MHz
V_{HSEH}	Input pin high level voltage	0.7*V_{CC}	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	V_{SS}	-	0.3*V_{CC}	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	High or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Rise or fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

5.3.6.2. High-speed external clock generated from a crystal resonator

The high-speed external (HSE) clock can be supplied with 4 to 32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-12 HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
I_{CC}(4)	HSE current consumption	Startup time	-	-	5.5	mA
		V_{CC}=3 V, R_m=30 Ω, C_L=10 pF@8 MHz	-	0.58	-	
		V_{CC}=3 V, R_m=45 Ω, C_L=10 pF@8 MHz	-	0.59	-	
		V_{CC}=3 V, R_m=30 Ω, C_L=5 pF@32 MHz	-	0.89	-	
		V_{CC}=3 V, R_m=30 Ω, C_L=10 pF@32 MHz	-	1.14	-	
		V_{CC}=3 V, R_m=30 Ω, C_L=20 pF@32 MHz	-	1.94	-	
$t_{SU(HSE)}$(3)(4)	Startup time	f_{OSC_IN}=32 MHz	-	3	-	ms
		f_{OSC_IN}=4 MHz	-	15	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable, measured for a standard crystal/resonator, which may vary greatly from crystal to resonator.
4. Data based on characterization results, not tested in production.

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5.3.7. High-speed internal (HSI) RC oscillator

Table 5-13 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	T_A=25 °C, V_{CC}=3.3 V	23.76(2)	24	24.24(2)	MHz
			21.89(2)	22.12	22.34(2)	
			15.84(2)	16	16.16(2)	
			7.92(2)	8	8.08(2)	
			3.96(2)	4	4.04(2)	
$\Delta_{Temp(HSI)}$	HSI frequency drift over temperature	V_{CC}=2.0 to 5.5 V, T_A=0 to 85 °C	-2(2)	-	2(2)	%
		V_{CC}=2.0 to 5.5 V, T_A=-40 to 105 °C	-4(2)	-	2(2)	
f_{TRIM}(1)	HSI trimming step	-	-	0.1	-	%
D_{HSI}(1)	Duty cycle	-	45(1)	-	55(1)	%
$t_{Stab(HSI)}$	HSI stabilization time	-	-	2	4(1)	μs
$I_{CC(HSI)}$(2)	HSI power consumption	4 MHz	-	100	-	μA
		8 MHz	-	105	-	
		16 MHz	-	150	-	
		22.12 MHz, 24 MHz	-	180	-	

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.8. Low-speed internal (LSI) RC oscillator

Table 5-14 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	T_A=25 °C, V_{CC}=3.3 V	-3	-	+3	%
$\Delta_{Temp(LSI)}$	LSI frequency drift over temperature	V_{CC}=2.0 to 5.5 V, T_A=0 to 85 ℃	-10(2)	-	10(2)	%
		V_{CC}=2.0 to 5.5 V, T_A=-40 to 105 ℃	-20(2)	-	20(2)	
f_{TRIM}(1)	LSI trimming step	-	-	0.2	-	%
$t_{Stab(LSI)}$(1)	LSI stabilization time	-	-	150	-	μs
$I_{CC(LSI)}$(1)	LSI power consumption	-	-	210	-	nA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.9. Phase locked loop (PLL) characteristics

Table 5-15 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	T_A=25 °C, V_{CC}=3.3 V	16(1)	-	24(1)	MHz
f_{PLL_OUT}	PLL output clock	T_A=25 °C, V_{CC}=3.3 V	48	-	48	MHz
Jitter	Period jitter	-	-	-	0.3(1)	ns
t_{LOCK}	PLL lock time	f_{PLL_IN}=24 MHz	-	15	40(1)	μs

1. Guaranteed by design, not tested in production.

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5.3.10. Memory characteristics

Table 5-16 Memory characteristics(2)

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}	Page programming time	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase time	-	3.5	4.5	ms
I_{CC}	Page programming supply current	-	2.1	2.9	mA
	Page/sector/mass erase supply current	-	2.1	2.9	

1. Guaranteed by design, not tested in production.
2. When the program runs in SRAM and executes the Flash erase/write program, the CPU will stop working.

Table 5-17 Memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 to 85 ℃	100	kcycles
		T_A = 85 to 105 ℃	10	
t_{RET}	Data retention time	10 kcycles T_A = 55 °C	20	Years

1. Data based on characterization results, not tested in production.

5.3.11. EFT characteristics

Table 5-18 EFT characteristics

Symbol	Parameter	Conditions	Grade
EFT to Power	-	IEC61000-4-4	4 A

5.3.12. ESD & LU characteristics

Table 5-19 ESD&LU characteristics

Symbol	Parameter	Conditions	Typ	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	6	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	ESDA/JEDEC JS-002-2018	1	kV
$V_{ESD(MM)}$	Static Discharge Voltage (machine model)	JESD22-A115C	200	V
LU	Static Latch-up	JESD78E	200	mA

5.3.13. I/O port characteristics

Table 5-20 IO port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{CC}=2.0 to 5.5 V	0.7*V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC}=2.3 to 5.5 V	-	-	0.3*V_{CC}	V
V_{hys}(1)	I/O Schmitt trigger hysteresis	-	-	200	-	mV
	NRST Schmitt trigger hysteresis	-	-	300	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}	Internal pull-up resistor	-	30	50	70	kΩ
R_{PD}	Internal pull-down resistor	-	30	50	70	kΩ
C_{IO}(1)	Pin capacitance	-	-	5	-	pF

1. Guaranteed by design, not tested in production.

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Table 5-21 Output voltage characteristics

Symbol	Parameter(1)	Conditions	Min	Max	Unit
V_{OL}	COM IO output low level	I_{OL} = 8 mA, V_{CC} ≥ 2.7 V	-	0.4	V
		I_{OL} = 4 mA, V_{CC} = 1.8 V	-	0.5	
V_{OH}	COM IO output high level	I_{OH} = 8 mA, V_{CC} ≥ 2.7 V	V_{CC}-0.4	-	V
		I_{OH} = 4 mA, V_{CC} = 1.8 V	V_{CC}-0.5	-	

1. These I/O types refer to the terms and symbols defined by pins.
2. Data based on characterization results, not tested in production.

5.3.14. ADC characteristics

Table 5-22 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Analog power supply	-	2.0	-	5.5	V
I_{CC}	Consumption	@0.75 Msps	-	1.0	-	mA
C_{IN}(1)	Internal sampling and holding capacitor	-	-	5	-	pF
f_{ADC}	ADC clock frequency	V_{CC}=2.0 to 2.3 V	1	4	6(2)	MHz
		V_{CC}=2.3 to 5.5 V	1	8	12(2)	MHz
t_{samp}(1)	Sampling time	V_{CC}=2.0 to 5.5 V	3.5	-	239.5	$1/f_{ADC}$
t_{samp_setup}(1)	V_{REFINT} sampling setup time	f_{ADC}=12 MHz	20	-	-	μs
t_{conv}(1)	Total conversion time	-	-	12	-	$1/f_{ADC}$
t_{eoc}(1)	Conversion end time	-	-	0.5	-	$1/f_{ADC}$
DNL(2)	Differential nonlinearity error	-	-	±2	-	LSB
INL(2)	Integral nonlinearity error	-	-	±3	-	LSB
Offset(2)	Offset error	-	-	±2	-	LSB

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.15. Comparator characteristics

Table 5-23 Comparator characteris(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Input voltage range	-		0	-	V_{CC}	V
V_{SC}	Offset voltage	-		-	±5	±10	mV
$I_{CC(SCALER)}$	Static consumption	-		-	0.8	1	μA
t_{START_SCALER}	Startup time	-		-	100	200	μs
t_{START}	Startup time	High-speed mode		-	-	5	μs
		Medium-speed mode		-	-	15	
t_D	Propagation delay	High-speed mode	200 mV step 100 mV over-drive	-	40	70	ns
			>200 mV step 100 mV over-drive	-	-	85	
		Medium-speed mode	200 mV step 100 mV over-drive	-	0.9	2.3	μs
			>200 mV step 100 mV over-drive	-	-	3.4	
V_{offset}	Offset voltage	-		-	±5	-	mV

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{hys}	Hysteresis voltage	No hysteresis		-	0	-	mV
		With hysteresis		-	20	-	
I_{CC}	Operating current	Medium-speed mode	Static	-	7	-	μA
			With 50 kHz and ±100 mv overdrive square signal	-	8	-	
		High-speed mode	Static	-	250	-	
			With 50 kHz and ±100 mv overdrive square signal	-	250	-	

1. Guaranteed by design, not tested in production.

5.3.16. Temperature sensor characteristics

Table 5-24 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±2	±5	℃
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/℃
V_{30}	Voltage at 30 °C (±5 °C)	0.742	0.76	0.785	V
t_{START}(1)	Start up time entering in continuous mode	-	70	120	μs
t_{S_temp}(1)	ADC sampling time when reading the temperature	20	-	-	μs

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.17. Embedded voltage reference characteristics

Table 5-25 Embedded voltage reference characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$t_{start_vrefint}$	Start time of V_{REFINT}	-	10	15	μs
T_{coeff}	Temperature coefficient of V_{REFINT}	-	-	100(1)	ppm/℃
I_{vcc}	V_{REFINT} consumption from V_{CC}	-	12	20	μA

1. Guaranteed by design, not tested in production.

5.3.18. Timer characteristics

Table 5-26 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.833	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 48 MHz	-	24	
Res_{TIM}	Timer resolution time	TIM1/3/14/16/17	-	16	bit
$t_{COUNTER}$	16-bit counter internal clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.020833	1365	μs

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Table 5-27 LPTIM characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PRESC[2:0]	Min	Max	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

Table 5-28 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 5-29 WWDG characteristics (clock selection 48 MHz PCLK)

Prescaler	WDGTB[1:0]	Min	Max	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

5.3.19. Communication interfaces

5.3.19.1. I²C interface characteristics

The I²C interface meets the requirements of the I²C bus specification and user manual:

- Standard mode (Sm): 100 kHz
- Fast mode (Fm): 400 kHz

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-30 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

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5.3.19.2. SPI characteristics

Table 5-31 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	12	MHz
		Slave mode	-	12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4*t_{pclk}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2*t_{pclk}$ + 10	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, presc = 4	$t_{pclk}*2$ - 2	$t_{pclk}*2$ + 1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode, presc = 4	t_{pclk} + 5(1)	-	ns
		Slave mode, presc = 4	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	ns
$t_{h(SI)}$		Slave mode	t_{pclk} + 5	-	
$t_{a(SO)}$	Data output access time	Slave mode, presc = 4	0	$3*t_{pclk}$	ns
$t_{dis(SO)}$	Data output access time	Slave mode	$2*t_{pclk}$ + 5	$4*t_{pclk}$ + 5	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge) presc = 4	0	$1.5*t_{pclk}$(2)	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	ns
$t_{h(SO)}$	Data output hold time	Slave mode, presc = 4	0(3)	-	ns
$t_{h(MO)}$		Master mode	2	-	
$DuCy_{(SCK)}$	SPI slave input clock duty cycle	Slave mode	45	55	%

1. The Master generates a 1 PCLK receive control signal before the receive edge.
2. Slave defines 1.5 PCLK based on the maximum 1 PCLK delay on the SCK transmission edge, considering IO delay, etc.
3. The Slave updates the data before the transmit edge if the SCK duty cycle sent by the Master is wide between the receive edge and the transmit edge.

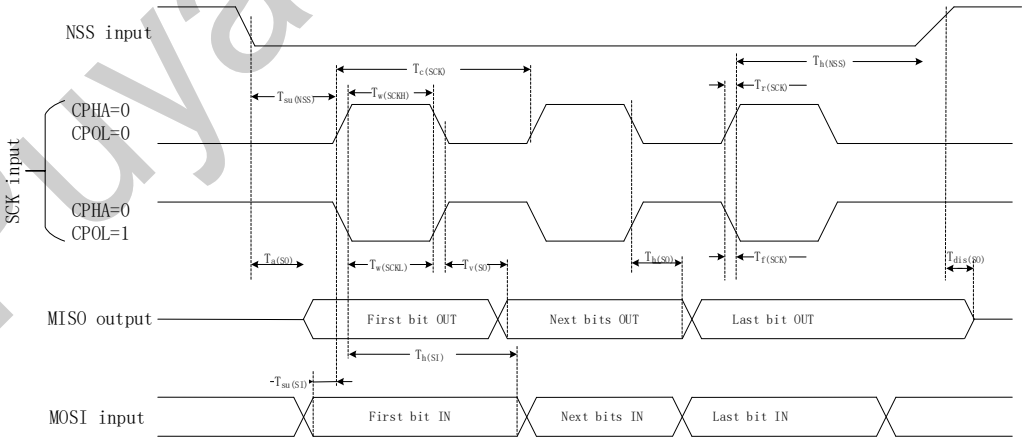


Figure 5-2 SPI timing diagram – Slave mode and CPHA=0

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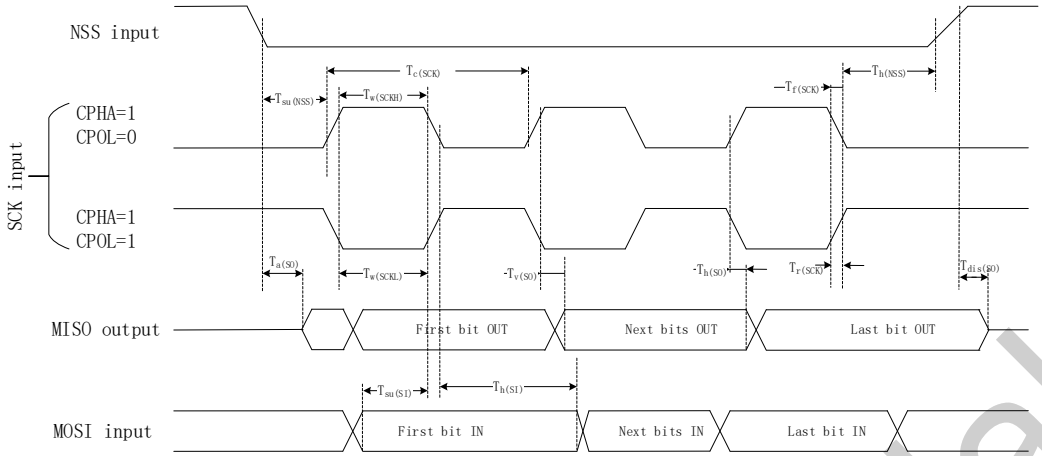


Figure 5-3 SPI timing diagram – Slave mode and CPHA=1

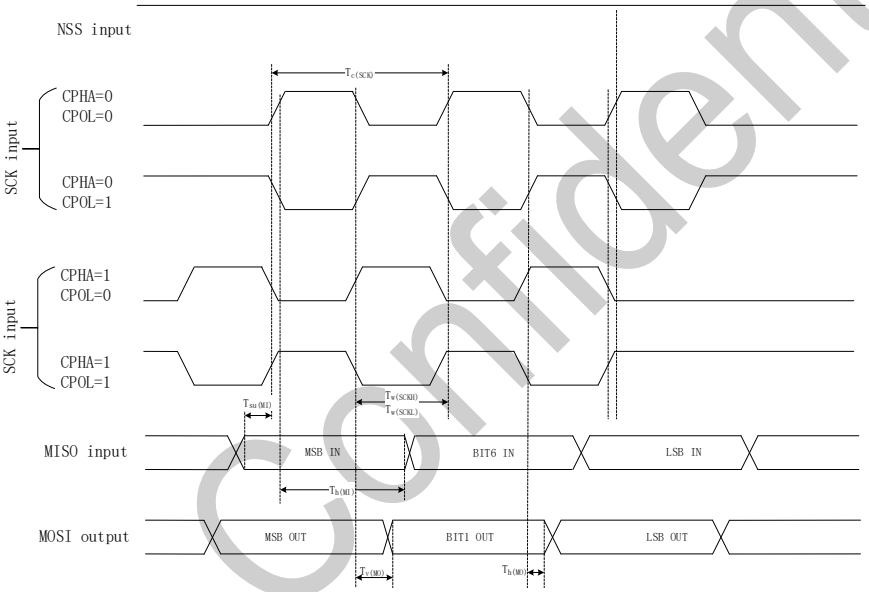


Figure 5-4 SPI timing diagram – Master mode

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5.4. Multifunction gate driver electrical characteristics

5.4.1. Operating conditions

Table 5-32 Gate driver absolute maximum ratings

Symbol	Descriptions	Min	Max	Unit
V_{IN}	Power supply voltage range	-0.3	45	V
$V_{HIN1,2,3}$	High-Side Control Input Voltage	-0.3	V_{LDO}	V
$V_{LIN1,2,3}$	Low-Side Control Input Voltage	-0.3	V_{LDO}	V
$V_{INP1,2}$	Low-offset op-amp positive input voltage range	-0.3	V_{LDO}	V
$V_{INN1,2}$	Low-offset op-amp negative input voltage range	-0.3	V_{LDO}	V
ESD	HBM	±2000		V
	CDM	±1000		

Table 5-33 Gate driver recommended operating range

Symbol	Descriptions	Min	Max	Unit
V_{IN}	Power supply voltage range	6	36	V
V_{LDO}	LDO Output Voltage Range	4.5	5.5	V
$V_{HIN1,2,3}$	High-Side Control Input Voltage	0	V_{LDO}	V
$V_{LIN1,2,3}$	Low-Side Control Input Voltage	0	V_{LDO}	V
$V_{HO1,2,3}$	High-Side Gate Driver Output Voltage	V_{IN}-12	36	V
$V_{LO1,2,3}$	Low-Side Gate Driver Output Voltage	0	12	V
$V_{AO1,2}$	Low offset op-amp output voltage range	0	V_{LDO}	V
$V_{INP1,2}$	Low-offset op-amp positive input voltage range	0	V_{LDO}	V
$V_{INN1,2}$	Low-offset op-amp negative input voltage range	0	V_{LDO}	V

5.4.2. Electrical characteristics

Table 5-34 Legend/abbreviations used for the Gate Driver pin definitions

Symbol	Descriptions	Min	Typ	Max	Unit
Electrical Characteristics					
V_{IN}	Power supply voltage range	6	-	36	V
I_{VIN}	V_{IN} quiescent current	-500		1000	μA
V_{UVLO}	V_{IN} undervoltage lockout voltage, falling edge	-	5.1	-	V
$V_{STARTUP}$	V_{IN} undervoltage lockout voltage, rising edge	-	5.5	-	V
LDO					
V_{LDO}	LDO output voltage, I_{OUT}=1 mA, V_{IN}=12 V	4.75	5	5.25	V
Three-phase gate driver					
V_{IL}	Logic input low voltage	-	-	0.4	V
V_{IH}	Logic input high voltage	1.6	-	-	V
R_{PD}	Weak pull-down equivalent resistor	-	9.3	-	kΩ
I_{OH}	High-level output short-circuit pulse current	-	300	-	mA
I_{OL}	Low-level output short-circuit pulse current	-	300	-	mA
V_{PCLAMP}	V_{GS} clamp voltage, driving external PMOS	-12	-10	-9	V

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Symbol	Descriptions	Min	Typ	Max	Unit
V_{NCLAMP}	V_{GS} clamp voltage, driving external NMOS	9	10	12	V
t_{DT}	Dead time	300	500	800	ns
t_r	Output rising edge propagation time	-	70	150	ns
t_f	Output falling edge propagation time	-	70	150	ns
t_{on}	Output rising edge propagation time	-	50	100	ns
T_{OTP}	Overtemperature protection threshold, shuts down the entire chip	-	160	-	℃
T_{OTPHYS}	Overtemperature protection hysteresis	-	20	-	℃
Op-amp					
V_{OP}	Op-amp operating voltage	-	5	-	V
V_{OFFSET}	Offset voltage	-	3	-	mV
V_{CRANGE}	Input voltage range	0	-	V_{OP}-0.2	V
I_{IN}	Low input bias current	-	-	1	μA
I_{SOURCE}	Output current	1000	-	-	μA
I_{SINK}	Output current	1000	-	-	μA
V_{SW}	Output voltage swing	0	-	V_{OP}	V
Av	Open loop gain	-	10	-	kV/V
BW	Bandwidth	-	6	-	MHz

Table 5-35 PWM input/output status table

LINx	HINx	LOx	HOx	Output status
0	0	GND	V_{IN}	External NMOS and PMOS are turned off simultaneously
0	1	GND	V_{IN}-10V	External NMOS is turned off, PMOS is turned on
1	0	10 V	V_{IN}	External NMOS is turned on, PMOS is turned off
1	1	GND	V_{IN}	External NMOS and PMOS are turned off simultaneously

Table 5-36 MOSFET recommendations

	Symbol	Descriptions	Min	Typ	Max	Unit
PMOS						
Gate threshold voltage	$V_{GS(th)}$	Recommended range of PMOS turn-on threshold	1.2	-	-	V

Note: To ensure optimal BLDC performance, it is recommended to select PMOS devices with $V_{GS(th)}$ > 1.2V

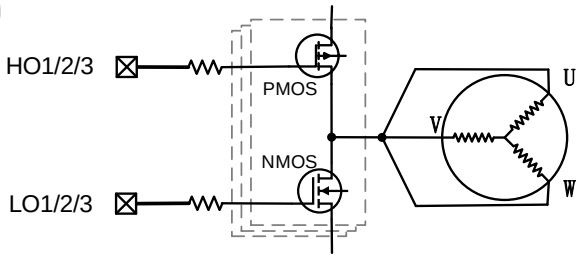


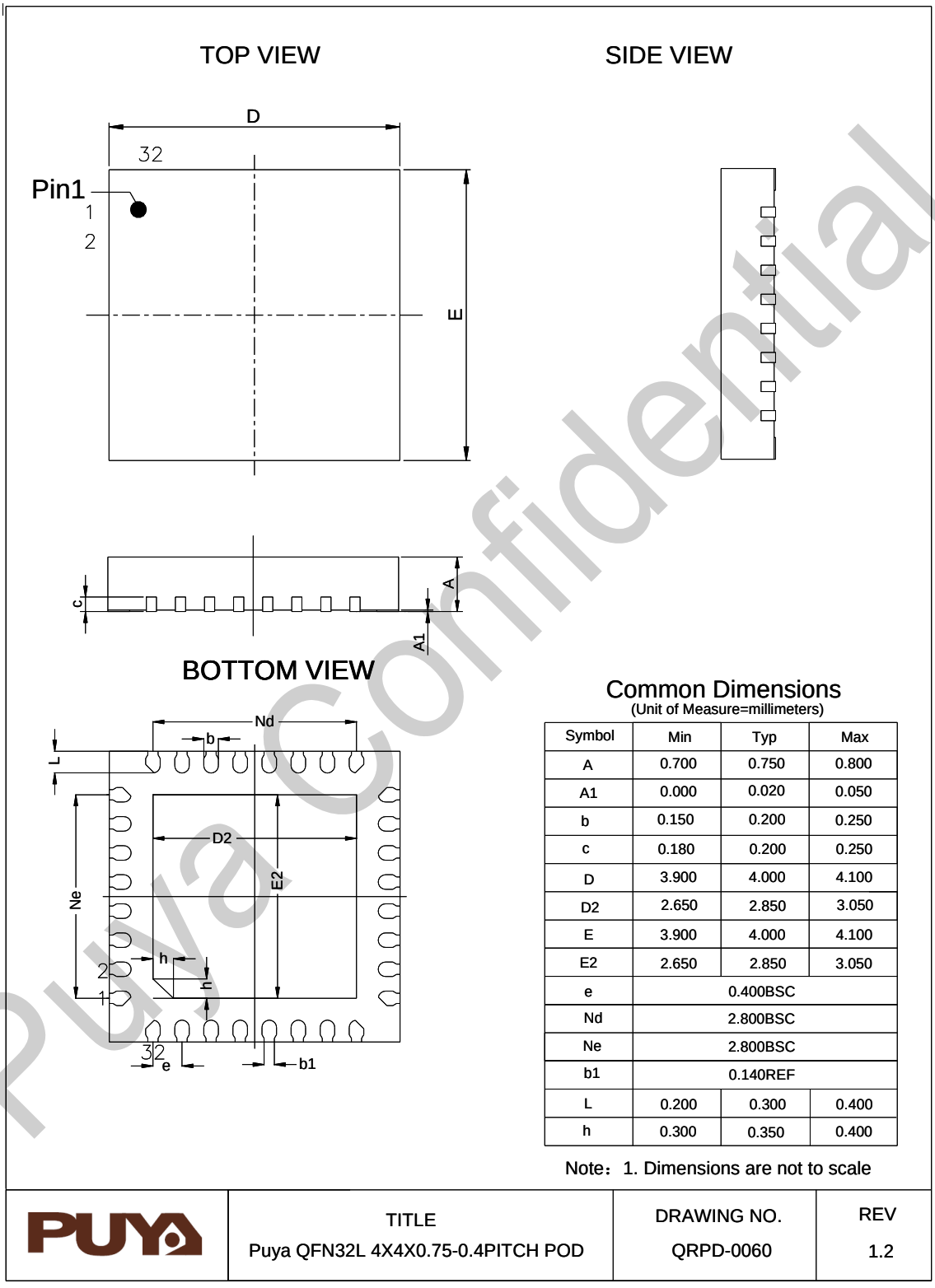
Figure 5-5 MOS schematic diagram

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6. Package information

6.1. QFN32 package size



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.650	2.850	3.050
E	3.900	4.000	4.100
E2	2.650	2.850	3.050
e	0.400BSC		
Nd	2.800BSC		
Ne	2.800BSC		
b1	0.140REF		
L	0.200	0.300	0.400
h	0.300	0.350	0.400

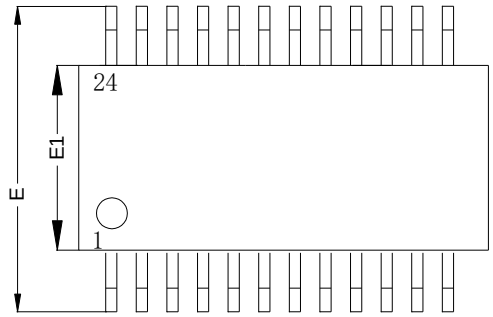
Note：1. Dimensions are not to scale

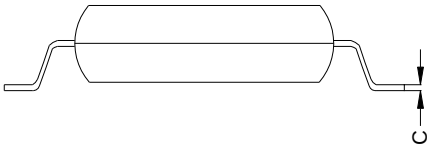
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PUYA	Puya QFN32L 4X4X0.75-0.4PITCH POD	QRPD-0060	1.2

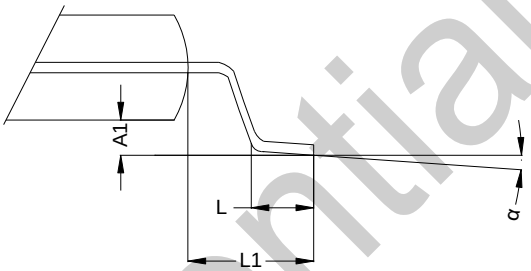
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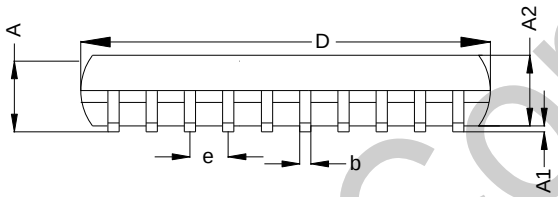
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6.2. SSOP24 package size









Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.750
A1	0.100	-	0.250
A2	1.300	1.450	1.600
b	0.230	-	0.310
c	0.190	-	0.250
D	8.450	8.600	8.750
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	0.635BSC		
h	0.300	-	0.500
L	0.400	-	1.270
L1		1.400REF	
θ	0	-	8°

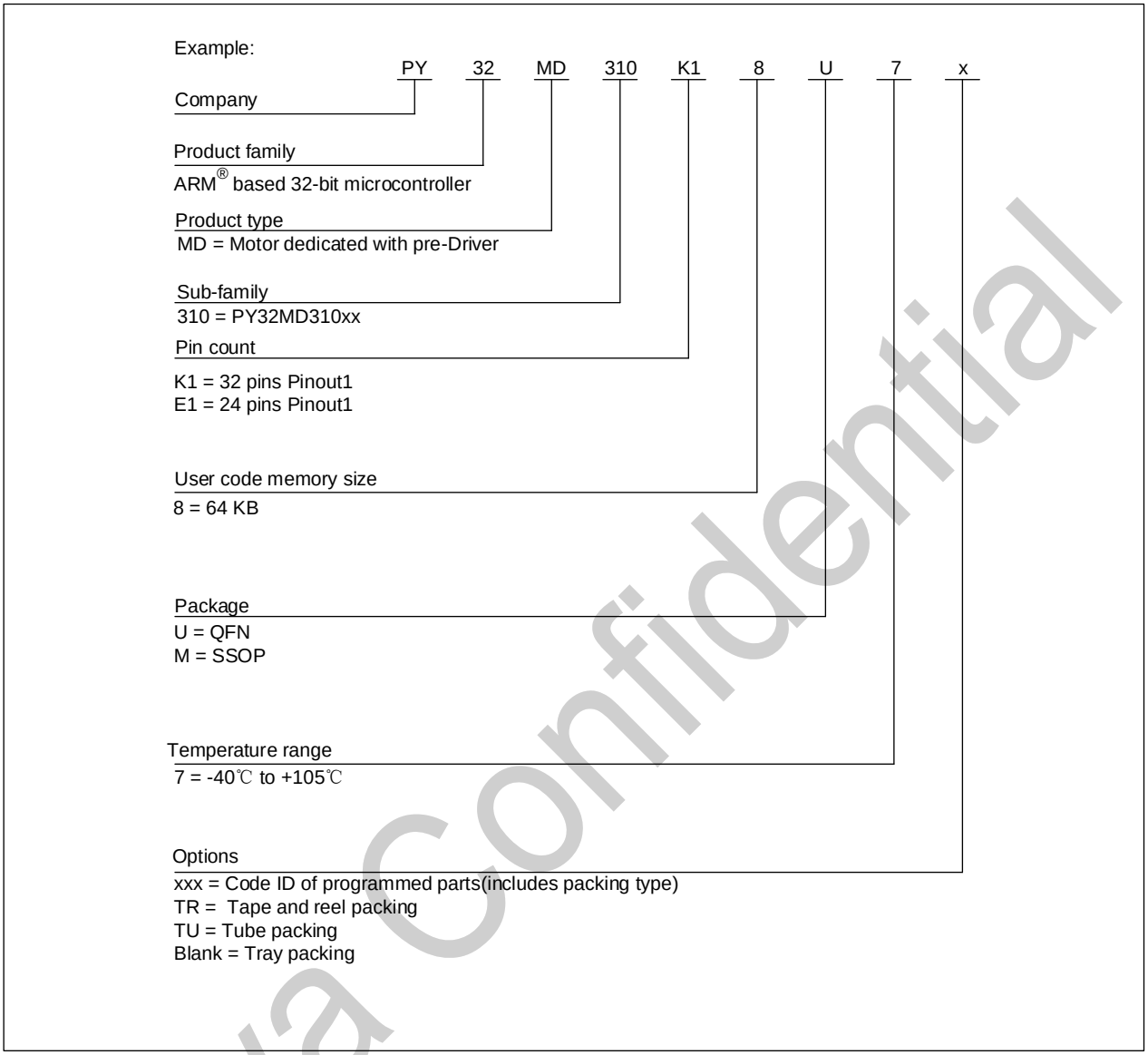
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya SSOP24 POD	QRPD-0045	1.1

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7. Ordering information



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8. Version history

Version	Date	Descriptions
V1.0	2023.12.01	Initial version
V1.1	2023.12.15	Updated Table 6-3 Gate driver electrical characteristics
V1.2	2024.01.29	Junction temperature range: -40 to 110℃ adjusted to -40 to 125℃
V1.3	2024.11.15	1. MCU operating voltage range adjusted: 2.0 to 5.5 V 2. Update the measured parameters
V1.4	2025.02.24	Added product PY32MD310E18M7
V1.5	2025.12.31	Added Table 6-5 MOSFET $V_{GS(th)}$ minimum limit
V1.6	2026.06.09	Added note on Flash erase/write restrictions

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