PY32F031 Datasheet

32-bit ARM® Cortex®-M0+ Microcontroller

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Puya Semiconductor (Shanghai) Co., Ltd.

Features

- Core
  - — 32-bit ARM® Cortex®-M0+
  - — Frequency up to 72 MHz
- Memories
  - — Up to 64 KB Flash memory
  - — Up to 8 KB SRAM
  - — 128 bytes User OTP Data
- Clock management
  - — 4/8/16/22.12/24 MHz High-speed internal RC oscillator (HSI)
  - — 32.768 kHz Low-speed internal RC oscillator (LSI)
  - — 4 to 32 MHz High-speed external crystal oscillator (HSE)
  - — 32.768 kHz Low-speed external crystal oscillator (LSE)
  - — PLL (x2,x3)
- Power management and reset
  - — Operating voltage: 1.7 to 5.5 V
  - — Low-power modes: Sleep, Stop
  - — Power-on/power-down reset (POR/PDR)
  - — Brown-out reset (BOR)
  - — Programmable voltage detector (PVD)
- General-purpose input and output (I/O)
  - — Up to 44 I/Os, all available as external interrupts
- 3-channel DMA controller
- 1 x 12-bit ADC
  - — Up to 10 external and 5 internal channels
  - — Input voltage conversion range: 0 to V_{CC}
  - — Internal reference voltage: 1.024/1.5/2.048/2.5 V
- 4*18/8*14 LCD
- Timers
  - — 1 x 16-bit advanced-control timer (TIM1)
  - — 3 x 16-bit general-purpose timer (TIM14/TIM16/TIM17)
  - — 1 x 32-bit general-purpose timer (TIM2)
  - — 1 x low power timer (LPTIM), supporting wake-up from Stop mode
  - — 1 x independent watchdog timer (IWDG)
  - — 1 x window watchdog timer (WWDG)
  - — 1 x SysTick timer
  - — 1 x IRTIM
- RTC
- Communication interfaces
  - — 2 x serial peripheral interface(SPI), 1 with I^2S
  - — 3 x universal synchronous/asynchronous receiver/transmitters (USARTs), supporting automatic baud rate detection, 1 with LIN capability.
  - — 2 x I^2C interface, supporting Standard mode (100 kHz), Fast mode (400 kHz), Fast mode plus (1 MHz); with 7-bit addressing mode
- Hardware CRC-32 module
- 2 x comparators
- 2 x operational amplifier
- 32-bit Hardware divider (DIV)
- CORDIC for trigonometric functions acceleration (square root, sine/cosine and arctangent)
- Unique UID
- Serial wire debug (SWD)
- Operating temperature:
  - — -40 to 85 °C (x6 version)
  - — -40 to 105 °C (x7 version)
- Packages: LQFP48, QFN48(6*6), QFN48(5*5), QFN40, LQFP32, QFN32(5*5), QFN32(4*4), TSSOP20 and DFN8 (2*2*0.45)

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1. Introduction

The PY32F031 microcontrollers incorporate a 32-bit ARM® Cortex®-M0+ core operating at up to 72 MHz frequency, embedded memories with up to 64 KB Flash and 8 KB SRAM, available in multiple package options. The PY32F031 integrates I^2C, SPI, and USART and other communication peripherals, one 12-bit ADC, four 16-bit timers, one 32-bit timers, two comparators, two operational amplifiers, and one LCD driver.

The PY32F031 series operate from a 1.7 V to 5.5 V power supply over the -40 °C to +85 °C or -40 °C to +105 °C temperature range, and provides Sleep and Stop low-power modes to address a variety of power-sensitive applications.

These features make the PY32F031 microcontrollers suitable for a wide range of applications such as controllers, portable devices, PC peripherals, gaming and GPS platforms, as well as industrial applications.

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Table 1-1 PY32F031x6 series product features and peripheral counts

Peripherals		PY32F031C18T6	PY32F031C18U6	PY32F031C28U6	PY32F031H18U6	PY32F031K18T6	PY32F031K18U6	PY32F031F18P6	PY32F031L18D6
Flash (KB)		64	64	64	64	64	64	64	64
SRAM (KB)		8	8	8	8	8	8	8	8
Timers	Advanced control	1 *16-bit							
	General purpose	3*16-bit, 1*32-bit							
	Low power timer	1							
	SysTick	1							
	Watchdog	2							
Comm. interfaces	SPI (I^2S)	2(1)							1(1)
	I^2C	2							1
	USART (LIN)	3(1)							1(1)
DMA		3 ch							
RTC		Yes							
GPIOs		44	44	44	38	30	30	18	7
ADC (external + internal)		10+5	10+5	10+5	10+5	10+5	10+5	9+5	3+5
Comparators		2							1
OPA		2							-
LCD		4*18 / 8*14						-	-
HDIV		Yes							
CORDIC		Yes							
Max. CPU frequency		72 MHz							
Operating voltage		1.7 to 5.5 V							
Operating temperature		-40 to 85 °C							
Packages		LQFP48	QFN48(6*6)	QFN48(5*5)	QFN40	LQFP32	QFN32(5*5)	TSSOP20	DFN8(2*2)

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Table 1-2 PY32F031x7 series product features and peripheral counts

Peripherals		PY32F031C18T7	PY32F031K28U7
Flash (KB)		64	64
SRAM (KB)		8	8
Timers	Advanced-control	1 *16-bit	
	General-purpose	3*16-bit, 1*32-bit	
	Low power timer	1	
	SysTick	1	
	Watchdog	2	
Comm. interfaces	SPI (I^2S)	2(1)	
	I^2C	2	
	USART (LIN)	3(1)	
DMA		3 ch	
RTC		Yes	
GPIOs		44	30
ADC		10+5	
Comparators		2	
Operational amplifier		2	
LCD		4*18 / 8*14	
HDIV		Yes	
CORDIC		Yes	
Max. CPU frequency		72 MHz	
Operating voltage		1.7 to 5.5 V	
Operating temperature		-40 to 105 °C	
Packages		LQFP48	QFN32(4*4)

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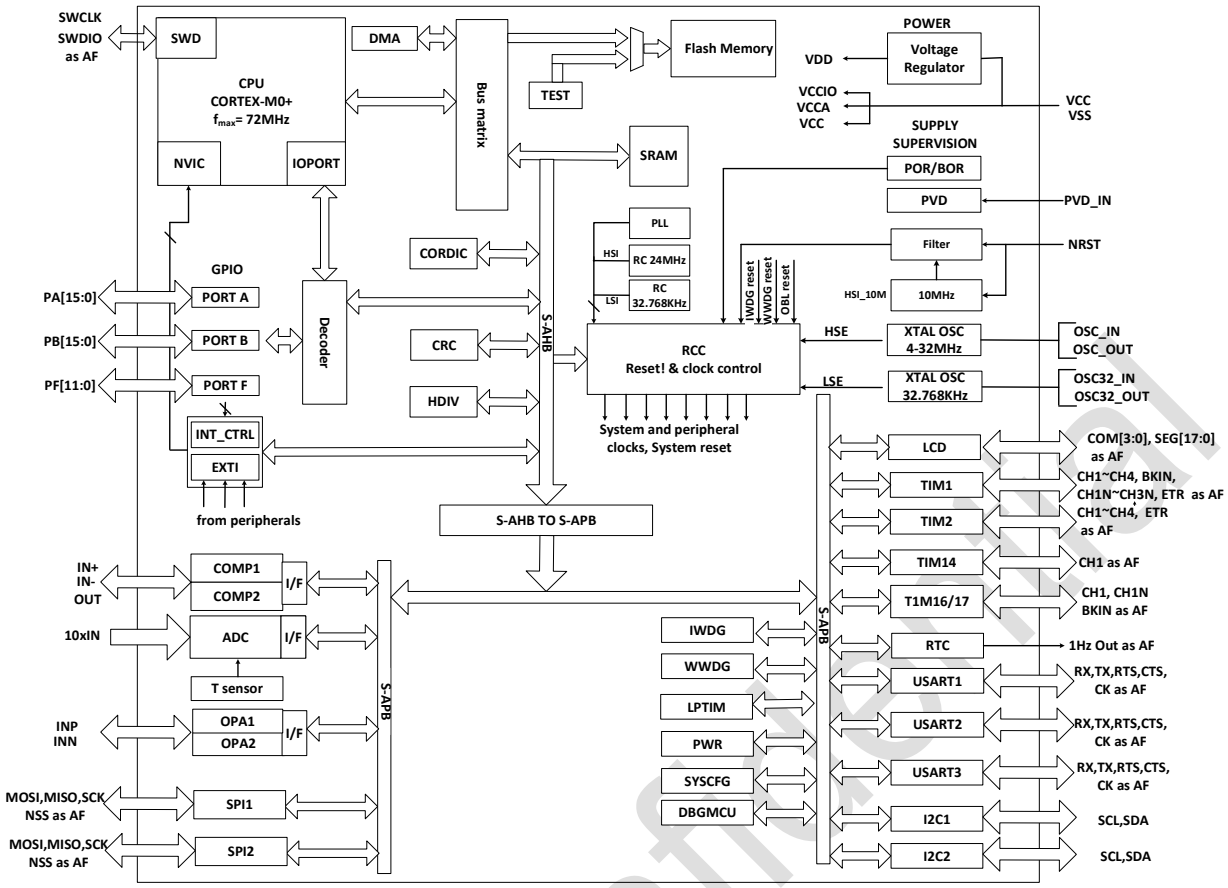


Figure 1-1 System block diagram

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2. Functional overview

2.1. Arm®-Cortex®-M0+ core

The Arm® Cortex®-M0+ is an Arm 32-bit Cortex processor designed for embedded applications. It provides developers with significant benefits, including:

- Simple architecture for easy learning and programming
- Ultra-low power consumption for energy-efficient operation
- Reduced code density

The Arm® Cortex®-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. It delivers high performance through a streamlined instruction set and hardware enhancements like a single-cycle multiplier which outperforms 8/16-bit MCUs in code efficiency.

The Arm® Cortex®-M0+ is tightly coupled with a Nested Vectored Interrupt Controller (NVIC).

2.2. Memories

Embedded 8 KB SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits).

The Flash memory is composed of two distinct physical areas:

- The Main flash memory consists of application and user data
- 4 KB of Information block:
  - Factory config. bytes
  - Option bytes
  - UID bytes
  - User OTP Data
  - System memory

The protection of Main flash memory includes the following mechanisms:

- Read protection (RDP) blocks external access
- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 4 KB.
- Option byte write protection is a special design for unlock.

2.3. Boot modes

At startup, the BOOT0 pin and the boot configuration bit nBOOT1 (stored in option bytes) are used to select one of the three boot options in the following table:

Table 2-1 Boot configuration

Boot mode configuration		Mode
nBOOT1 bit	BOOT0 pin	
X	0	Boot from Main flash

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Boot mode configuration		Mode
nBOOT1 bit	BOOT0 pin	
1	1	Boot from System memory
0	1	Boot from SRAM

The Boot loader is located in the System memory and is used to reprogram the Flash memory by using USART.

2.4. Clock management

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. After the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- A 4/8/16/22.12/24 MHz configurable internal high precision HSI clock
- A 32.768 kHz configurable LSI clock
- A 4 to 32 MHz HSE clock.
- A 32.768 kHz LSE clock
- PLL clock which can be fed with HSE or HSI clocks.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The maximum frequency of the AHB and the APB domains is 72 MHz.

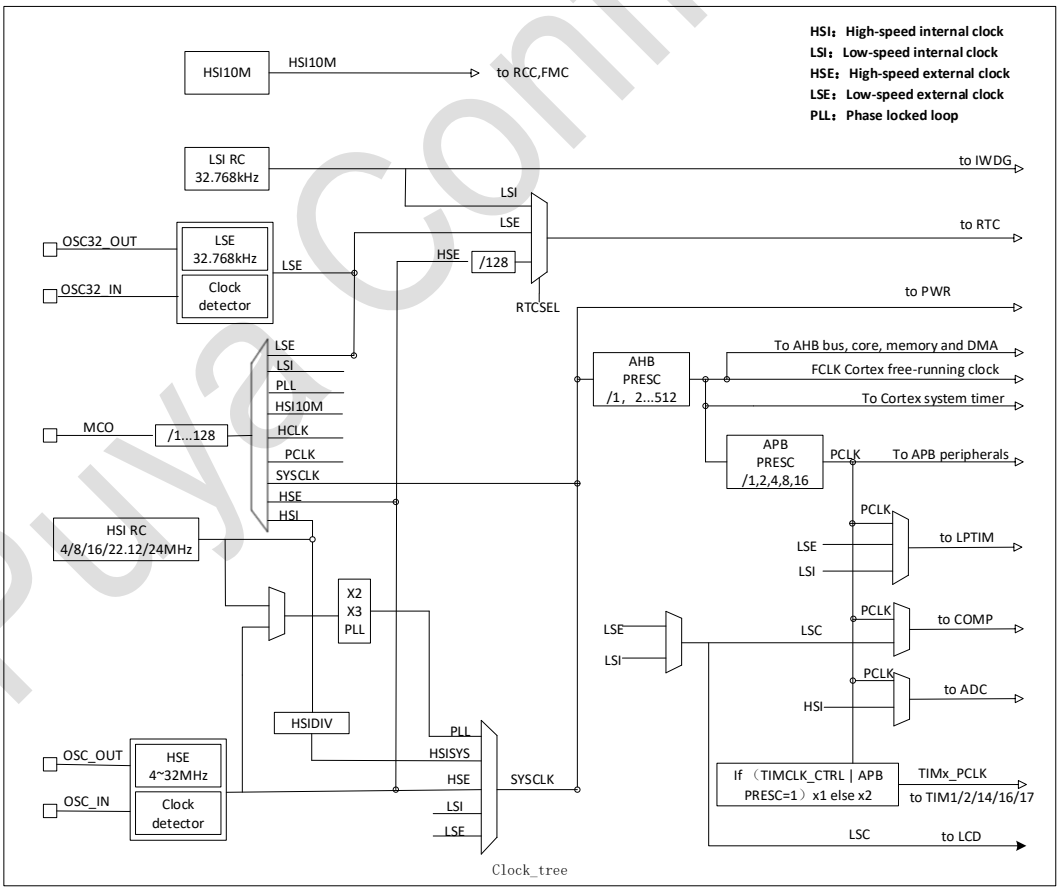


Figure 2-1 System clock structure diagram

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2.5. Power management

2.5.1. Power block diagram

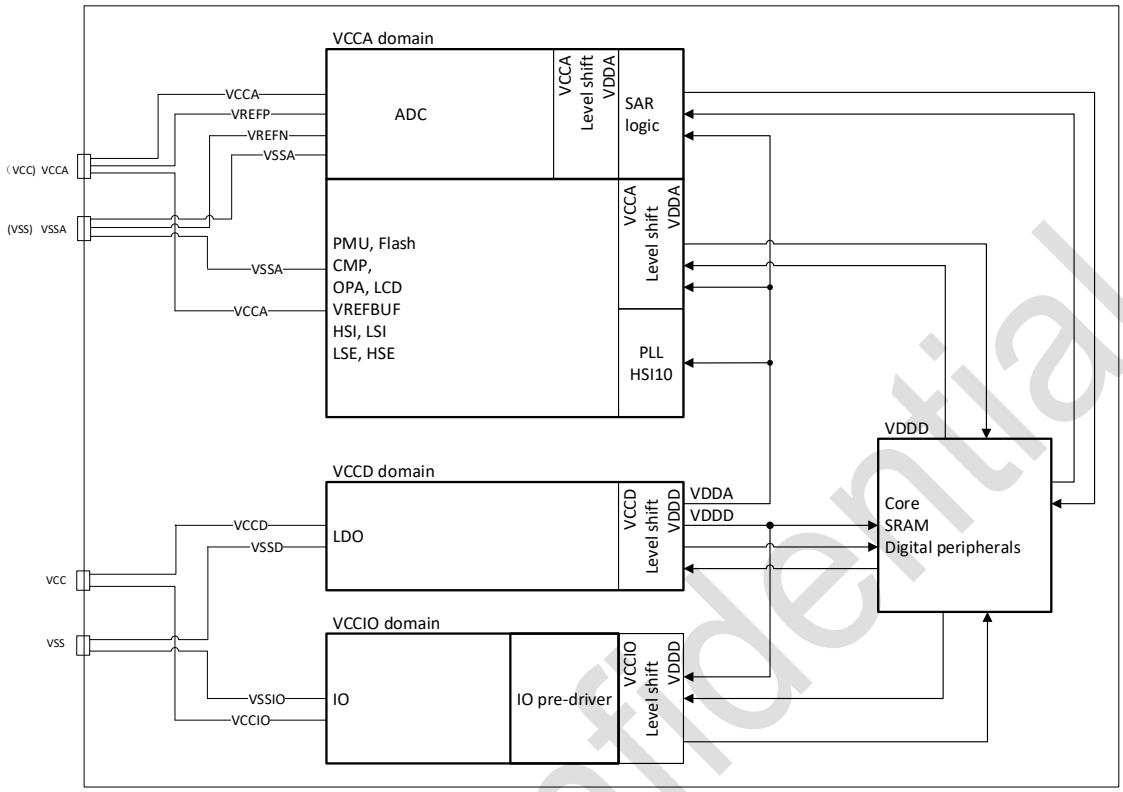


Figure 2-2 Power block diagram

Table 2-2 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	1.7 to 5.5 V	Power supply range: 1.7 to 5.5 V. The power is supplied to the device through the power pins, with the power supply module comprising: Partial analog circuits.
2	V_{CCA}	1.7 to 5.5 V	Powers for most analog modules, sourced from V_{CC}.
3	V_{CCIO}	1.7 to 5.5 V	Power to IO from V_{CC}
4	V_{DDD}	1.2 V	From VR output and powers the standby mode wake-up circuit and IWDG module. When the MR is powered, it outputs 1.2 V. According to the software configuration, when entering the Stop or Standby mode, it powered by MR, LPR and DLPR.

2.5.2. Power monitoring

2.5.2.1. Power-on/power-down reset (POR/PDR)

The Power-on reset (POR) and Power-down reset (PDR) module is designed in the device to provide power-on and power-down reset for the device. The module keeps working in all modes.

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2.5.2.2. Brown-out reset (BOR)

In addition to POR/PDR, BOR (Brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte.

When the BOR is enabled, the BOR threshold can be selected by the option byte.

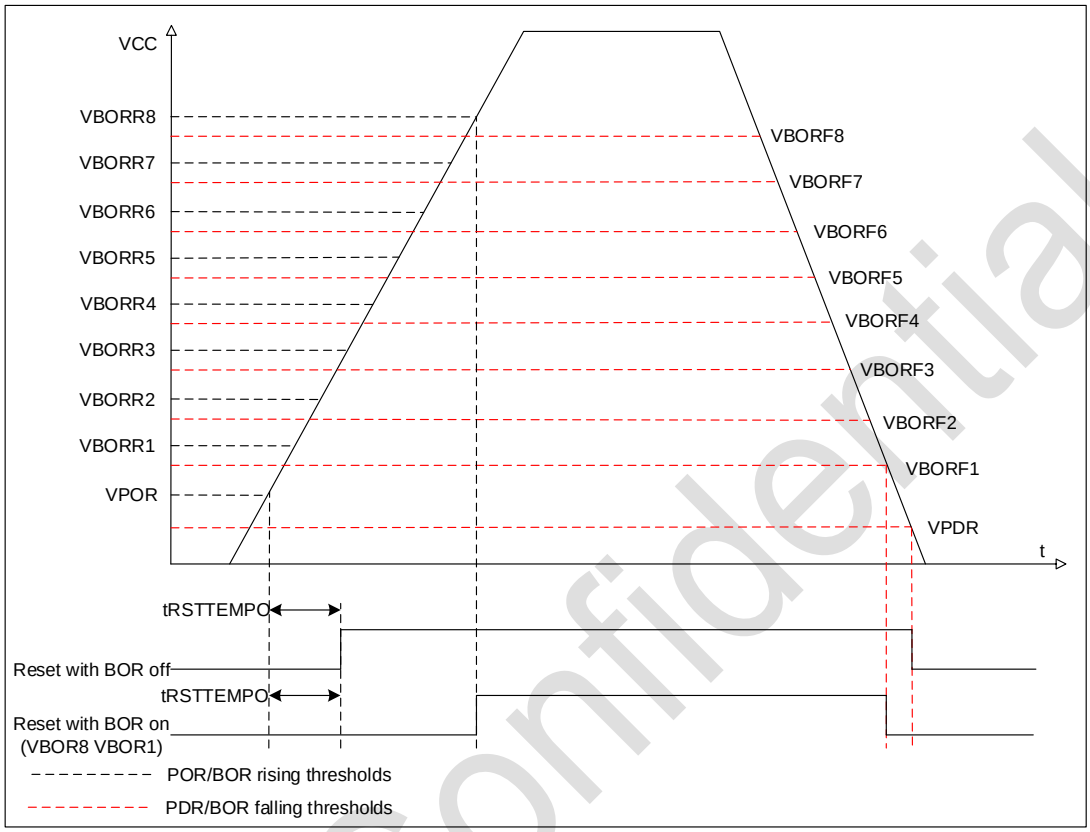


Figure 2-3 POR/PDR/BOR threshold

2.5.2.3. Programmable voltage detector (PVD)

Programmable voltage detector (PVD) module can monitor the V_{CC} power supply (or monitor the voltage on the PB7 pin), with the detection point configurable by registers. When V_{CC} is higher or lower than the detection point of PVD, the corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when V_{CC} rises above the detection point of PVD, or V_{CC} falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

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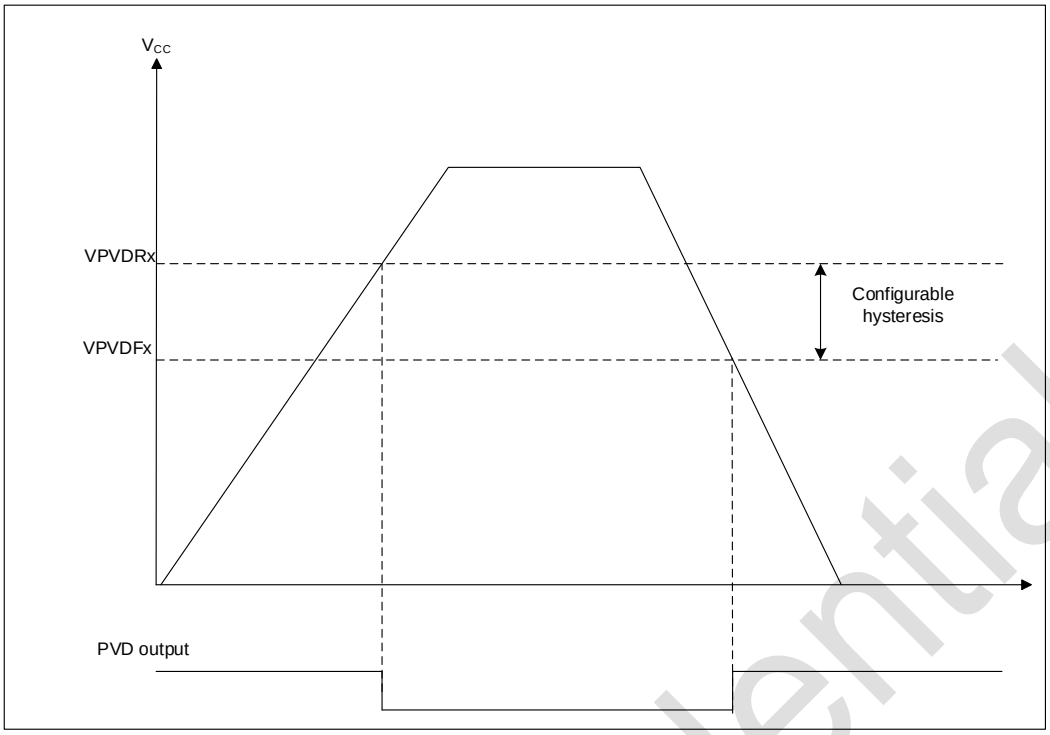


Figure 2-4 PVD threshold

2.5.3. Voltage regulator

The regulator has two operating modes:

- MR (Main regulator) is used in Run mode.
- LPR (Low power regulator) provides an option for even lower power consumption in Stop mode.

2.5.4. Low-power mode

In addition to the Run mode, the device has two low-power modes:

- **Sleep mode:** Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works
- **Stop mode:** In this mode, SRAM and register contents are retained. PLL, HSI and HSE are turned off and most module clocks in the V_{DDD} domain are disabled. GPIO, PVD, COMP output, RTC, and LPTIM can wake up the Stop mode.

2.6. Reset

- Two resets are designed in the device: power reset and system reset.

2.6.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out reset (BOR)

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2.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load (OBL) reset

2.7. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input (floating, pull-up or pull-down and analog) or as peripheral alternate function. The I/O configuration can be locked.

2.8. Hardware divider (DIV)

Hardware divider is a 32-bit signed/unsigned integer hardware divider.

The hardware divider supports the following features:

- Configurable signed/unsigned division calculation
- 32-bit dividend, 32-bit divisor
- Output 32-bit quotient and 32-bit remainder
- Divide-by-zero warning flag bit, end-of-division flag bit
- 16 clock cycles to complete a division operation
- Write the divisor register to trigger the start of the division circuit
- After writing the divisor, wait for the calculation-complete flag; then read the quotient and remainder registers

2.9. CORDIC digital signal processor

The CORDIC digital signal processor provides hardware acceleration for mathematical functions, commonly used in applications such as motor control, metering, and signal processing. A hardware-accelerated computing module that includes square root operations and trigonometric functions (sine/cosine, arctangent), supporting fixed-point square root and trigonometric operations. Trigonometric functions support 360°/2^16 operation precision.

2.9.1. Hardware square root

The radicand is a 32-bit unsigned number, and the square root is a 16-bit unsigned number.

- 16 bus cycles completed
- Configurable signed/unsigned division calculation

2.9.2. Sine/Cosine and arctangent operations

The trigonometric CORDIC module has a bit width of 16 bits, in Q15 fixed-point format.

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2.10. DMA

Direct memory access (DMA) is used to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations. The DMA controller have 3 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- Single AHB Master
- Support peripherals to memory, the memory to the peripherals, memory to memory and peripherals to peripheral data transmission
- On-chip memory devices, such as Flash, SRAM, AHB and APB peripherals, as the source and target
- All DMA channel can be independently configured:
  - Each channel is associated either with a DMA request signal from a peripheral or with a software trigger in a memory-to-memory transfer. This configuration is done by software.
  - The priority between requests is programmable by software (4 levels per channel: very high, high, medium and low) and, in equal cases, by hardware (such as a request for channel 1 taking precedence over a request for channel 2).
  - The transfer sizes of the source and destination are independent (byte, half word and word), simulating packing and unpacking. The source and target addresses must be aligned by data size.
  - Programmable number of data to be transferred: 0 to 65535
- Each channel generates an interrupt request. Each interrupt request is caused by one of three DMA events: transfer completion, half-transfer, or transfer error.

2.11. Interrupts

The PY32F031 handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.11.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is

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called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Support 1 NMI
- Support 28 maskable external interrupts
- Support 6 Cortex-M0+ exceptions
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.11.2. Extended interrupt (EXTI)

- EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from Stop mode.
- The EXTI controller has multiple channels, including up to 44 GPIOs multiplexed using 16 EXTI lines, 1 PVD output, 2 COMP outputs, as well as RTC and LPTIM Wake-up signals. GPIO, PVD and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 15 channel through the select signal.
- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.12. Analog-to-digital converter (ADC)

- The device has a 12-bit SAR-ADC. The module has a total of up to 15 channels to be measured, including 10 external and 5 internal channels. The internal voltage reference: V_{REFBUF} (1.024V, 1.5 V, 2.048 V, 2.5 V) or the power supply voltage.
- Internal channels include T_S, V_{REFINT}, $V_{CC}/3$, OPA1_OUT and OPA2_OUT.
- A/D conversion of the various channels can be performed in single, continuous, or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.
- The channel priority conversion sequence can be set when multiple channels are selected.
- The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.
- An efficient low-power mode is implemented to allow very low consumption at low frequency.

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- An interrupt request is generated when any of the following events occurs: the sampling of a single channel finishes, the conversion of a single channel completes, the entire conversion sequence ends, the analog watchdog detects a voltage outside the programmed thresholds, or a data-overrun condition arises.

2.13. Comparators (COMP)

The device integrates two general-purpose comparators (COMP), which can also be used in combination with Timer. Comparators can be used as:

- Triggered by analog signal to wake-up function from low-power mode
- Analog signal conditioning
- Cycle by cycle current control loop when comparators are connected with PWM output from timer.

COMP main features:

- Each comparator has configurable positive or negative input for flexible voltage selection:
  - Multiple I/O pins
  - Power supply V_{CC}
  - Output of the temperature sensor
  - 64-step voltage division supporting internal reference voltage V_{REFBUF} and V_{CC}
  - OPA output as INP input
- Configurable hysteresis function
- Programmable speed and consumption
- The output can be triggered by a connection to the I/O or timer input
  - OCREF_CLR event (cycle by cycle current control)
  - Break for fast PWM shutdown
  - Timer IC input
- COMP1 and COMP2 can be combined into window COMP
- Configurable digital filter

2.14. Operational amplifier (OPA)

The OPA1/2 modules can be flexibly configured for simple amplifier and buffer applications.

2.15. Liquid crystal display (LCD) controller

The LCD controller is a digital controller/driver for monochrome passive liquid crystal displays (LCD), with up to 8 common terminals (COM) and 18 segment terminals (SEG) to drive 72 (4*18) or 122 (8*14) LCD pixels. The exact number of terminals depends on the device pins described in the datasheet.

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2.16. Timers

The different timers feature as blow:

Table 2-3 Timer characteristics

Timer type	Timer	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Complementary outputs
Advanced-control timer	TIM1	16-bit	Up, down, up/down	1 to 65536	Yes	4	3
General-purpose timers	TIM2	32-bit	Up, down, up/down	1 to 65536	Yes	4	-
	TIM14	16-bit	Up	1 to 65536	-	1	-
	TIM16,TIM17	16-bit	Up	1 to 65536	Yes	1	1

2.16.1. Advanced-control timer

- 16-bit auto-reload counter with up, down, or up/down counting capability
- 16-bit programmable divider, allowing the clock frequency of the counter to be divided by 1 to 65536.
- Up to 4 independent channels
  - Input capture
  - Output compare
  - PWM generation (edge or center-aligned mode)
  - Single pulse mode output
  - Retriggerable single-pulse mode output
- Complementary outputs with programmable dead time
- Synchronization circuit using external signals to control timers and interconnect timers
- Repetition counter to update the timer registers only after a given number of cycles of the counter.
- Output signal of the timer can be set as reset and known state by break input.
- Interrupt/DMA occurs on the following events
  - Update: Counter overflow (up/down), counter initialization (by software or internal/external trigger)
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Support for incremental (quadrature) encoders and Hall sensor circuits for positioning
- Trigger input for external clock or cycle-by-cycle current management

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- The counter can be frozen in MCU debug mode.

2.16.2. General-purpose timers

2.16.2.1. TIM2

- The TIM2 general-purpose timer consists of a 32-bit auto-reload counter driven by a 32-bit programmable prescaler. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.
- TIM2 can work with the TIM1 by the Timer Link.
- TIM2 supports the DMA function.
- The counter can be frozen in MCU debug mode.

2.16.2.2. TIM14

- The general-purpose timer TIM14 is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- The counter can be frozen in MCU debug mode.

2.16.2.3. TIM16/TIM17

- TIM16 and TIM17 consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM16/TIM17 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- TIM16/TIM17 have complementary outputs with dead time.
- TIM16/TIM17 supports DMA function.
- The counter can be frozen in MCU debug mode.

2.16.3. Low power timer

- LPTIM is a 16-bit upcounter with a 3-bit prescaler
- Support single-shot and continuous modes.
- LPTIM can be configured as a Stop mode wake-up source.
- The counter can be frozen in MCU debug mode.

2.16.4. IWDG

- Independent watchdog (IWDG) is integrated in the device, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.
- The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.
- IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.

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- Controlling of option byte can enable IWDG hardware mode.
- IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.
- The counter can be frozen in MCU debug mode.

2.16.5. WWDG

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in MCU debug mode.

2.16.6. SysTick timer

The SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.17. Real-time clock (RTC)

- The RTC is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.
- RTC is a 32-bit programmable counter with a prescaler factor of up to 2^{20} bits.
- RTC counter clock source can be LSE, LSI or HSE/128 and acts as the stop wake-up source.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).
- RTC supports clock calibration.
- RTC can be frozen in MCU debug mode.

2.18. Debug support(DBG)

The MCU DBG module assists the debugger with the following functions:

- Support Sleep mode and Stop mode
- When the CPU enters the HALT mode, the control timer or watchdog stops counting or continues counting

The MCU DBG register also provides ID code which can be accessed by a SW debug interface, or by a user program.

2.19. Inter-integrated circuit interface (I^2C)

The I^2C (Inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode plus (Fm+).

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For specific needs, DMA can be used to reduce the burden on the CPU.

2.20. Universal synchronous/asynchronous receiver transmitter (USART)

The PY32F031 includes 3 USARTs, with USART1 supporting LIN.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baud rate detection
- Programmable data length of 8 or 9 bits
- Configurable STOP bit (1 or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Receive/transmit bytes by DMA buffer
- Transfer detection flag
  - Receive buffer full
  - transmit buffer empty
  - End of transmission flags
- Parity control
  - Transmit parity bit
  - Check the received data byte
- Flagged interrupt sources
  - CTS change

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  - Transmit data register empty
  - Transmission complete
  - Receive full data register
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Detection error
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

2.21. Serial peripheral interface (SPI)

The PY32F031 includes 2 SPIs, with SPI1 supporting I^2S.

SPIs allow the device to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- Master mode baud rate prescaling factors (Max $f_{PCLK}/2$)
- Slave mode frequency (Max $f_{PCLK}/4$)
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Hardware CRC feature for reliable communication
  - In transmit mode, the CRC value can be transmitted as last byte
  - In full-duplex mode, the last received byte is automatically checked for CRC.

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- Motorola mode
- Trigger interrupt-causing Master mode faults, overrun errors and CRC errors
- Two embedded Rx and Tx FIFOs with DMA capability, depth of four, and width of 16 bits (8 bits when data frame is set to 8-bit)

I^2S main features

- Half-duplex communication (only transmitter or receiver)
- Master or slave operations
- 8-bit programmable linear prescaler to reach accurate audio sample frequencies (from 8 kHz to 192 kHz)
- Data format may be 16-bit, 24-bit or 32-bit
- Packet frame is fixed to 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit, 32-bit data frame) by audio channel
- Programmable clock polarity (steady state)
- Underflow flag bits in slave transmit mode and overflow flag bits in master/slave receive mode
- 16-bit register for transmission and reception with one data register for both channel sides
- Support I^2S protocols:
  - I^2S Phillps standard
  - MSB-justified standard (left-justified)
  - LSB-justified standard (right-justified)
  - PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)
- Data direction is always MSB first
- DMA capability for transmission and reception

Master clock may be output to drive an external audio component. Ratio is fixed at 256 × f_S (where f_S is the audio sampling frequency)

2.22. SWD

An ARM SWD interface allows serial debugging tools to be connected to the PY32F031.

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3. Pinouts and pin descriptions

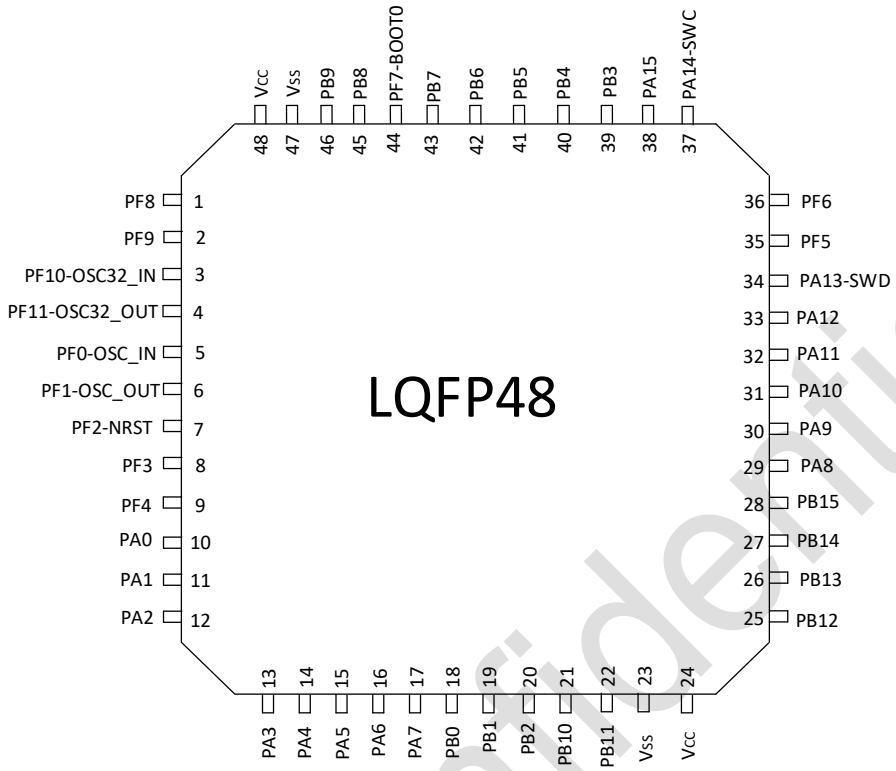


Figure 3-1 LQFP48 Pinout1 PY32F031C1xTx (Top view)

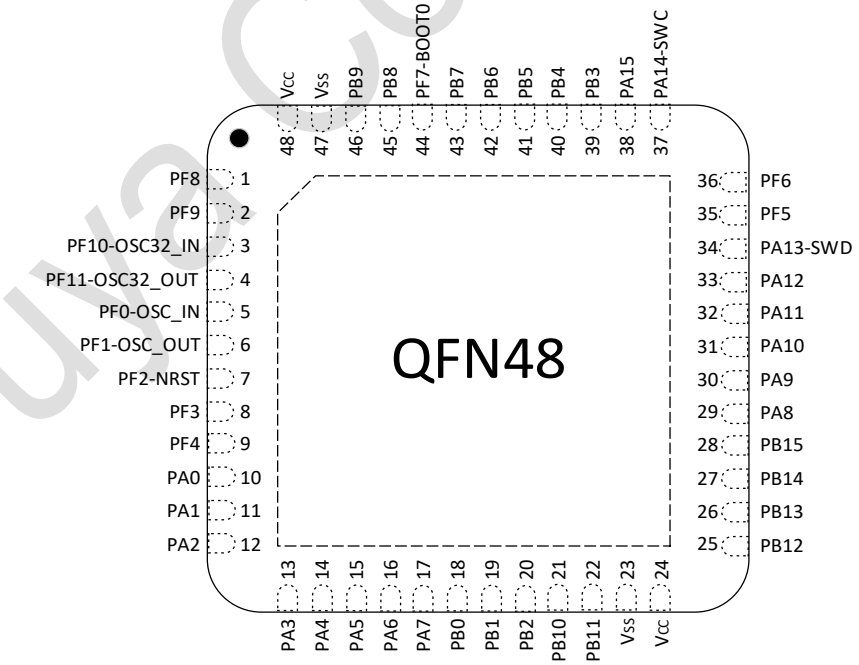


Figure 3-2 QFN48(6*6) Pinout1 PY32F031C1xUx (Top view)

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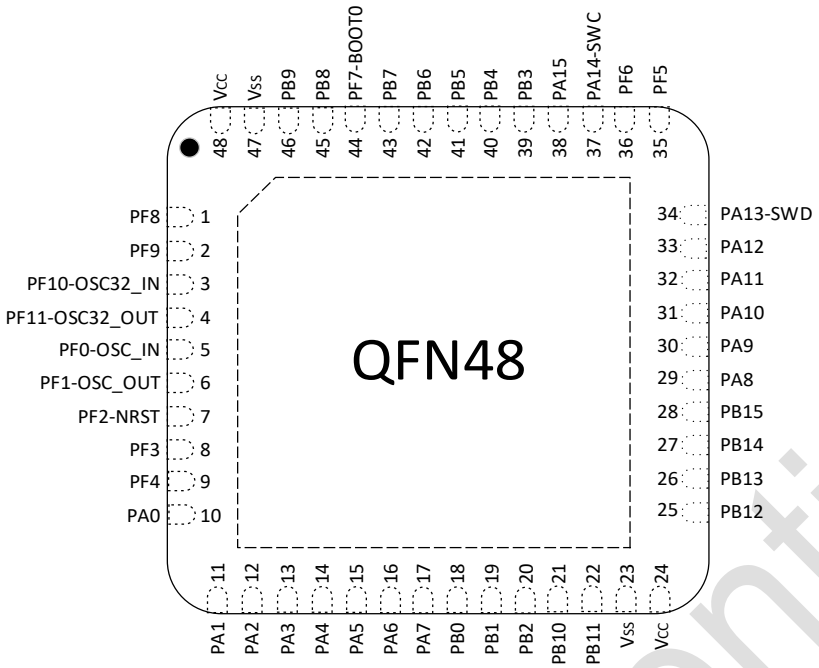


Figure 3-3 QFN48(5*5) Pinout2 PY32F031C2xUx (Top view)

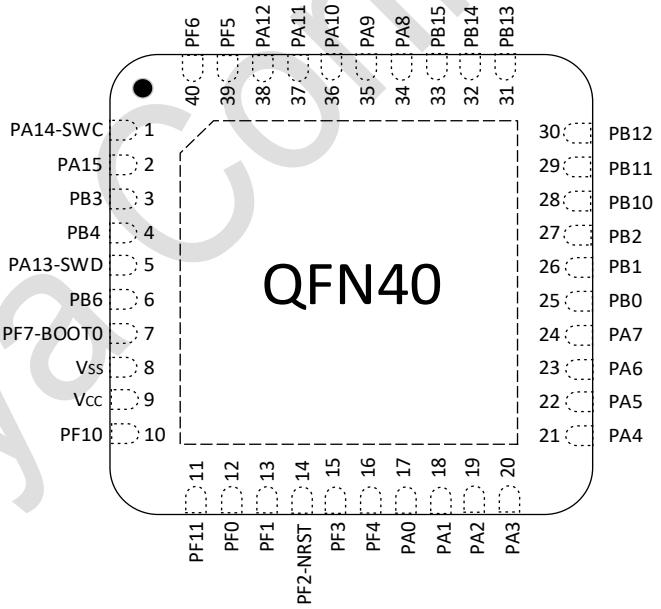


Figure 3-4 QFN40 Pinout1 PY32F031H1xUx (Top view)

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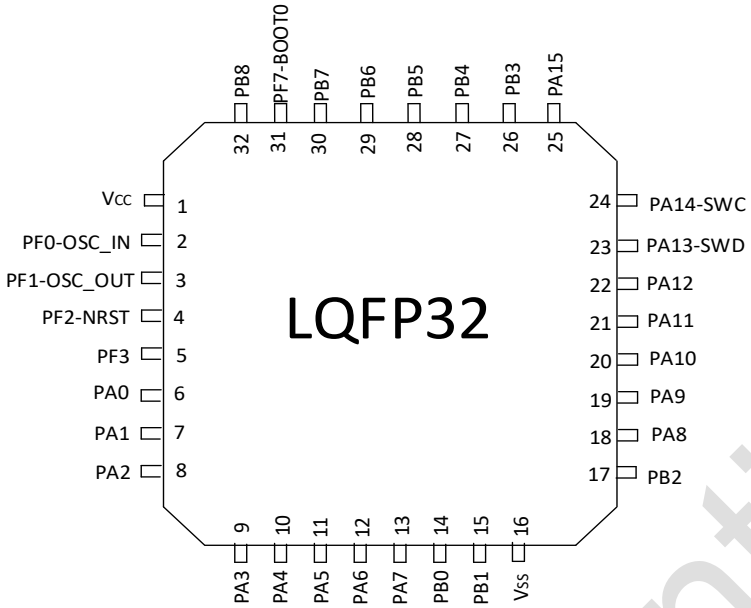


Figure 3-5 LQFP32 Pinout1 PY32F031K1xTx (Top view)

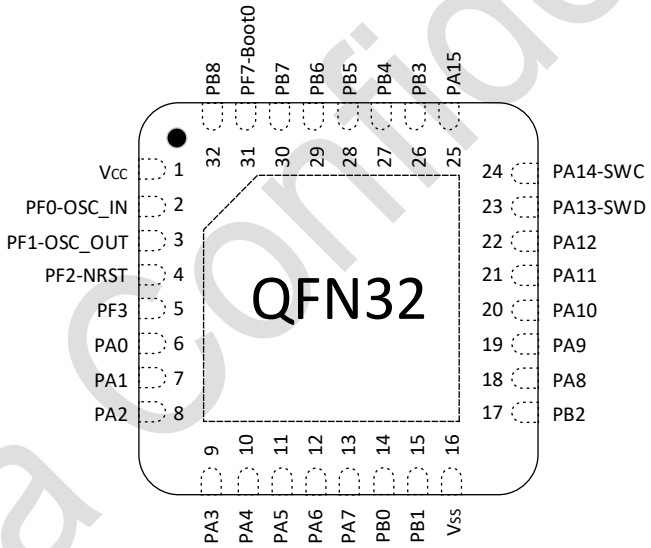


Figure 3-6 QFN32(5*5) Pinout1 PY32F031K1xUx (Top view)

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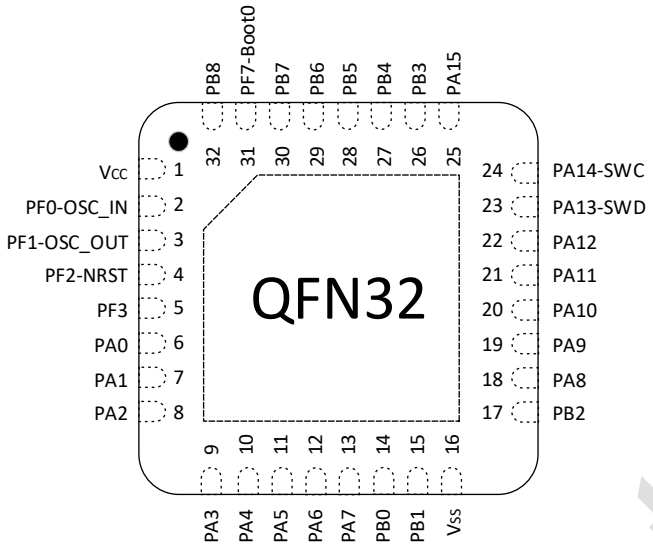


Figure 3-7 QFN32(4*4) Pinout2 PY32F031K2xUx (Top view)

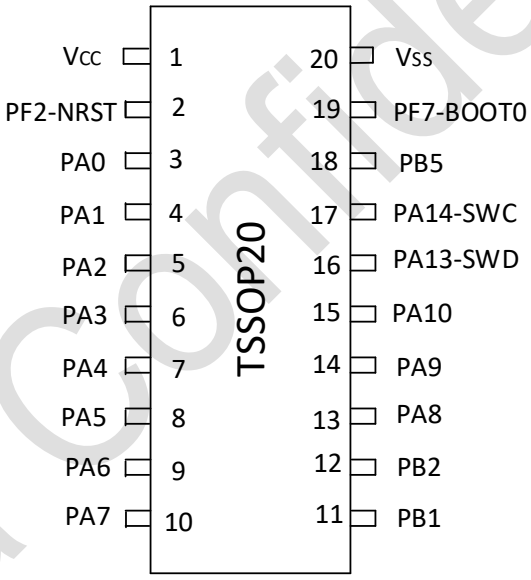


Figure 3-8 TSSOP20 Pinout1 PY32F031F1xPx (Top view)

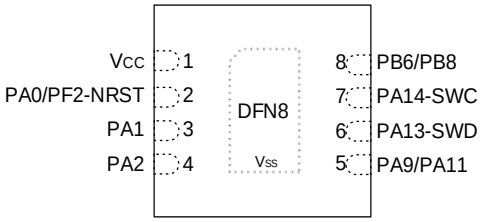


Figure 3-9 DFN8(2*2) Pinout1 PY32F031L1xDx (Top view)

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Table 3-1 Legend/abbreviations used in the pinout table

Timer type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I/O	Input / output pin
		NC	No internal connection
I/O structure		COM	Standard 5 V I/O, with Analog switch function supplied by V_{CCA}
		NRST	Reset pin with internal weak pull-up; analog input/output functions are not supported
		_L	LED COM port supports analog input/output functions
		_F	I^2C Fm+ with analog input function
		_PU	Internal pull-up resistor
Note		-	Unless otherwise specified, all ports are used as analog inputs between and after reset
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers

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Table 3-2 Pin definitions

Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
-	-	-	-	1	PF8	I/O	COM	-	TIM1_CH1 SPI2_MOSI USART2_RX MCO	-
-	-	-	-	2	PF9	I/O	COM	-	TIM2_CH1 TIM1_CH1N SPI2_SCK USART2_TX	LCD_SEG11
-	-	-	10	3	PF10-OSC32_IN	I/O	COM	-	-	OSC32_IN
-	-	-	11	4	PF11-OSC32_OUT	I/O	COM	-	-	OSC32_OUT
-	-	2	12	5	PF0-OSC_IN	I/O	COM_F	-	SPI2_SCK USART2_RX TIM14_CH1 USART1_RX USART2_TX I2C1_SDA I2C2_SDA	OSC_IN LCD_SEG10
-	-	3	13	6	PF1-OSC_OUT	I/O	COM_F	-	SPI2_MISO USART2_TX USART1_TX	OSC_OUT LCD_SEG9

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									USART2_RX	
									I2C1_SCL	
									I2C2_SCL	
									SP1_NSS/I2S1_WS	
									TIM14_CH	
2	2	4	14	7	PF2-NRST	I/O	NRST	(1)	MCO	NRST
									SPI2_MOSI	
									USART2_RX	
									TIM2_CH2	
									TIM1_CH2	
									TIM1_CH1N	
-	-	5	15	8	PF3	I/O	COM	-	USART1_TX	COMP2_INP5 LCD_SEG8
									USART2_TX	
									SPI2_MISO	
									SPI1_NSS/I2S1_WS	
									TIM2_CH3	
									RTC_OUT	
-	-	-	16	9	PF4	I/O	COM	-	-	-
2	3	6	17	10	PA0	I/O	COM_L	-	SPI2_SCK	ADC_IN0 COMP1_INM1 LCD_SEG7
									USART1_CTS	
									USART2_CTS	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									COMP1_OUT	
									TIM1_CH3	
									TIM1_CH1N	
									IR_OUT	
									USART3_CTS	
									USART2_TX	
									SPI1_MISO/I2S1_MCK	
3	4	7	18	11	PA1	I/O	COM	-	SPI1_SCK/I2S1_CK	ADC_IN1 COMP1_INP2 LCD_SEG6
									USART1_RTS	
									USART2_RTS	
									EVENTOUT	
									USART3_RX	
									SPI1_MOSI/I2S1_SD	
									USART2_RX	
									USART3_RTS	
									TIM1_CH4	
									TIM1_CH2N	
									MCO	
4	5	8	19	12	PA2	I/O	COM_F	-	SPI1_MOSI/I2S1_SD	ADC_IN2 COMP2_INM2 LCD_SEG5
									USART1_TX	
									USART2_TX	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									COMP2_OUT	
									SPI1_SCK/I2S1_CK	
									TIM2_CH1	
									I2C1_SDA	
									I2C2_SDA	
-	6	9	20	13	PA3	I/O	COM_F	-	SPI2_MISO	ADC_IN3 COMP2_INP4 LCD_SEG4
									USART1_RX	
									USART2_RX	
									EVENTOUT	
									SPI1_MOSI/I2S1_SD	
									TIM1_CH1	
									I2C1_SCL	
									I2C2_SCL	
-	7	10	21	14	PA4	I/O	COM	-	SPI1_NSS/I2S1_WS	ADC_IN4 COMP2_INP3 LCD_SEG3
									USART1_CK	
									SPI2_MOSI	
									TIM14_CH1	
									USART2_CK	
									ENENTOUT	
									TIM2_CH3	
									USART2_TX	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									USART3_TX	
									RTC_OUT	
-	8	11	22	15	PA5	I/O	COM	-	SPI1_SCK/I2S1_CK	ADC_IN5 COMP2_INP2 LCD_SEG2
									EVENTOUT	
									TIM2_CH2	
									USART2_RX	
									MCO	
-	9	12	23	16	PA6	I/O	COM	-	SPI1_MISO/I2S1_MCK	ADC_IN6
									TIM2_CH1	
									TIM1_BKIN	
									TIM16_CH1	
									COMP1_OUT	
									USART1_CK	
									RTC_OUT	
-	10	13	24	17	PA7	I/O	COM_F	-	SPI1_MOSI/I2S1_SD	ADC_IN7
									TIM2_CH2	
									TIM1_CH1N	
									TIM14_CH1	
									TIM17_CH1	
									EVENTOUT	
									COMP2_OUT	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									USART1_TX	
									USART2_TX	
									I2C1_SDA	
									I2C2_SDA	
									SPI1_MISO/I2S1_MCK	
-	-	14	25	18	PB0	I/O	COM	-	SPI1_NSS/I2S1_WS	ADC_IN8
									TIM2_CH3	
									TIM1_CH2N	
									EVENTOUT	
									COMP1_OUT	
									USART3_CK	
-	11	15	26	19	PB1	I/O	COM	-	TIM14_CH1	ADC_IN9 COMP1_INM0
									TIM2_CH4	
									TIM1_CH3N	
									EVENTOUT	
									USART3_RTS	
-	12	17	27	20	PB2	I/O	COM_L	-	USART1_RX	COMP1_INP1 LCD_SEG1
									USART2_RX	
									TIM1_CH2	
									USART3_RX	
									SPI2_SCK	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
-	-	-	28	21	PB10	I/O	COM_F	-	SPI2_SCK TIM2_CH3 USART3_TX I2C2_SCL I2C1_SCL	-
-	-	-	29	22	PB11	I/O	COM_F	-	TIM2_CH4 USART3_RX EVENTOUT I2C1_SDA I2C2_SDA	-
-	-	-	-	23	V_{SS}	G	-	-	Ground	
-	-	-	-	24	V_{CC}	S	-	-	Digital power supply	
-	-	-	30	25	PB12	I/O	COM	-	SPI2_NSS/I2S1_WS SPI2_NSS TIM1_BKIN EVENTOUT USART3_RTS TIM1_BKIN	-
-	-	-	31	26	PB13	I/O	COM	-	SPI2_SCK TIM1_CH1N SPI1_SCK/I2S1_CK	-

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									USART3_CTS	
-	-	-	32	27	PB14	I/O	COM	-	SPI2_MISO	-
									TIM1_CH2N	
									SPI1_MISO/I2S1_MCK	
									USART3_RTS	
-	-	-	33	28	PB15	I/O	COM	-	SPI2_MOSI	-
									TIM1_CH3N	
									SPI1_MOSI/I2S1_SD	
-	13	18	34	29	PA8	I/O	COM_F	-	SPI2_NSS	OPA1_OUT LCD_SEG0
									USART1_CK	
									TIM1_CH1	
									USART2_CK	
									MCO	
									EVENTOUT	
									USART1_RX	
									USART2_RX	
									SPI1_MOSI/I2S1_SD	
									I2C1_SCL	
									I2C2_SCL	
5	14	19	35	30	PA9	I/O	COM_F	-	SPI2_MISO	OPA1_INP LCD_COM0
									USART1_TX	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									TIM1_CH2	
									USART2_TX	
									MCO	
									I2C1_SCL	
									EVENTOUT	
									I2C1_SDA	
									I2C2_SDA	
									TIM1_BKIN	
									SPI1_SCK/I2S1_CK	
									USART1_RX	
-	15	20	36	31	PA10	I/O	COM_F	-	SPI2_MOSI	OPA1_INN LCD_COM1
									USART1_RX	
									TIM1_CH3	
									TIM17_BKIN	
									USART2_RX	
									I2C1_SDA	
									EVENTOUT	
									I2C1_SCL	
									I2C2_SCL	
									SPI1_NSS/I2S1_WS	
									USART1_TX	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
5	-	21	37	32	PA11	I/O	COM_F	-	SPI1_MISO/I2S1_MCK	LCD_COM2
									USART1_CTS	
									TIM1_CH4	
									EVENTOUT	
									USART2_CTS	
									I2C1_SCL	
									COMP1_OUT	
									I2C2_SCL	
-	-	22	38	33	PA12	I/O	COM_F	-	SPI1_MOSI/I2S1_SD	LCD_COM3
									USART1_RTS	
									TIM1_ETR	
									USART2_RTS	
									EVENTOUT	
									I21C_SDA	
									COMP2_OUT	
									I2C2_SDA	
6	16	23	5	34	PA13-SWDIO	I/O	COM	(2)	SWDIO	-
									IR_OUT	
									EVENTOUT	
									SPI1_MISO/I2S1_MCk	
									TIM1_CH2	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									USART1_RX	
									MCO	
-	-	-	39	35	PF5	I/O	COM_PU	-	IR_OUT	-
									EVENTOUT	
									USART1_RX	
									SPI1_MISO/I2S1_MCK	
									I2C2_SCL	
									I2C2_SDA	
									TIM1_CH2	
-	-	-	40	36	PF6	I/O	COM_PU	-	USART1_TX	-
									TIM1_CH2N	
									USART2_TX	
									EVENTOUT	
									I2C2_SDA	
									I2C2_SCL	
7	17	24	1	37	PA14-SWCLK	I/O	COM	(2)	SWCLK	-
									USART1_TX	
									USART2_TX	
									EVENTOUT	
									MCO	
									SPI1_SCK/I2S1_CK	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									USART3_TX	
-	-	25	2	38	PA15	I/O	COM_L	-	SPI1_NSS/I2S1_WS	OPA2_INN LCD_COM4/SEG17
									USART1_RX	
									USART2_RX	
									EVENTOUT	
									USART3_RX	
-	-	26	3	39	PB3	I/O	COM_L	-	SPI1_SCK/I2S1_CK	OPA2_INP COMP2_INM1 LCD_COM5/SEG16
									TIM1_CH2	
									USART1_RTS	
									USART2_RTS	
									EVENTOUT	
									USART3_RTS	
-	-	27	4	40	PB4	I/O	COM_L	-	SPI1_MISO/I2S1_MCK	OPA2_OUT COMP2_INP1 LCD_COM6/SEG15
									TIM2_CH1	
									USART2_CTS	
									USART1_CTS	
									TIM17_BKIN	
									EVENTOUT	
									USART3_CTS	
-	18	28	-	41	PB5	I/O	COM_L	-	SPI1_MOSI/I2S1_SD	LCD_COM7/SEG14
									TIM2_CH2	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									TIM16_BKIN	
									USART2_CK	
									USART1_CK	
									COMP1_OUT	
									USART3_CK	
									TIM1_CH1	
8	-	29	6	42	PB6	I/O	COM_FL	-	USART1_TX	COMP2_INP0 LCD_SEG13
									TIM1_CH3	
									TIM16_CH1N	
									USART2_TX	
									SPI2_MISO	
									I2C1_SCL	
									EVENTOUT	
									I2C2_SCL	
-	-	30	-	43	PB7	I/O	COM_FL	-	USART1_RX	PVD_IN COMP2_INM0 LCD_SEG12
									SPI2_MOSI	
									TIM17_CH1N	
									USART2_RX	
									I2C1_SDA	
									EVENTOUT	
									I2C2_SDA	

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Packages					Reset	Pin type	I/O structure	Notes	Pin functions	
DFN8 L1	TSSOP20 F1	LQFP32 K1 /QFN32 K1 / K2	QFN40 H1	LQFP48 C1 /QFN48 C1 / C2					Alternate functions	Additional functions
									TIM1_CH2	
-	19	31	7	44	PF7-BOOT0	I/O	COM	(3)	-	BOOT0
8	-	32	-	45	PB8	I/O	COM_F	-	SPI2_SCK	COMP1_INP0
									TIM16_CH1	
									I2C1_SCL	
									I2C2_SCL	
									USART2_TX	
									EVENTOUT	
									USART1_TX	
									SPI2_NSS	
									I2C1_SDA	
									I2C2_SDA	
									TIM17_CH1	
									IR_OUT	
-	-	-	-	46	PB9	I/O	COM	-	TIM17_CH1	-
									EVENTOUT	
									IROUT	
-	20	16	8	47	V_{SS}	G	-	-	Ground	
1	1	1	9	48	V_{CC}	S	-	-	Digital power supply	

1. Configured by option bytes to choose PF2 or NRST.
2. After reset, PA13 and PA14 are configured as SWDIO and SWCLK AF functions, the former has an internal pull-up resistor and the latter has an internal pull-down resistor activated.

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3. PF7-BOOT0 defaults to digital input mode and pull-down is enabled.
4. Two IO ports are lead out on the same pin, only one of the IO ports can be used at the same time, and the other IO must be configured in analog mode (MODEy [1: 0] is 0B11).

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3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-3 Port A alternate functions mapping

Port A	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	SPI2_SCK	USART1_CTS	-	-	USART2_CTS	-	-	COMP1_OUT	-	USART2_TX	SPI1_MISO/ I2S1_MCK	USART3_CTS	-	TIM1_CH3	TIM1_CH1N	IR_OUT
PA1	SPI1_SCK/ I2S1_CK	USART1_RTS	-	-	USART2_RTS	-	-	EVENTOUT	USART3_RX	USART2_RX	SPI1_MOSI/ I2S1_SD	USART3_RTS	-	TIM1_CH4	TIM1_CH2N	MCO
PA2	SPI1_MOSI/ I2S1_SD	USART1_TX	-	-	USART2_TX	-	-	COMP2_OUT	-	-	SPI1_SCK/ I2S1_CK	I2C2_SDA	I2C1_SDA	TIM2_CH1	-	-
PA3	SPI2_MISO	USART1_RX	-	-	USART2_RX	-	-	EVENTOUT	-	-	SPI1_MOSI/ I2S1_SD	I2C2_SCL	I2C1_SCL	TIM1_CH1	-	-
PA4	SPI1_NSS/ I2S1_WS	USART1_CK	SPI2_MOSI	-	TIM14_CH1	USART2_CK	-	EVENTOUT	USART3_TX	USART2_TX	-	-	-	TIM2_CH3	-	RTC_OUT
PA5	SPI1_SCK/ I2S1_CK	-	-	-	-	-	-	EVENTOUT	-	USART2_RX	-	-	-	TIM2_CH2	-	MCO
PA6	SPI1_MISO/ I2S1_MCK	TIM2_CH1	TIM1_BKIN	-	-	TIM16_CH1	-	COMP1_OUT	USART1_CK	-	-	-	-	-	-	RTC_OUT
PA7	SPI1_MOSI/ I2S1_SD	TIM2_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT	USART1_TX	USART2_TX	SPI1_MISO/ I2S1_MCK	I2C2_SDA	I2C1_SDA	-	-	-
PA8	SPI2_NSS	USART1_CK	TIM1_CH1	-	USART2_CK	MCO	-	EVENTOUT	USART1_RX	USART2_RX	SPI1_MOSI/ I2S1_SD	I2C2_SCL	I2C1_SCL	-	-	-
PA9	SPI2_MISO	USART1_TX	TIM1_CH2	-	USART2_TX	MCO	I2C1_SCL	EVENTOUT	USART1_RX	-	SPI1_ SCK/ I2S1_CK	I2C2_SDA	I2C1_SDA	TIM1_BKIN	-	-
PA10	SPI2_MOSI	USART1_RX	TIM1_CH3	-	USART2_RX	TIM17_BKIN	I2C1_SDA	EVENTOUT	USART1_TX	-	SPI1_NSS/ I2S1_WS	I2C2_SCL	I2C1_SCL	-	-	-
PA11	SPI1_MISO/ I2S1_MCK	USART1_CTS	TIM1_CH4	-	USART2_CTS	EVENTOUT	I2C1_SCL	COMP1_OUT	-	-	-	I2C2_SCL	-	-	-	-
PA12	SPI1_MOSI/ I2S1_SD	USART1_RTS	TIM1_ETR	-	USART2_RTS	EVENTOUT	I2C1_SDA	COMP2_OUT	-	-	-	I2C2_SDA	-	-	-	-
PA13	SWDIO	IR_OUT	-	-	-	-	-	EVENTOUT	USART1_RX	-	SPI1_MISO/ I2S1_MCK	-	-	TIM1_CH2	-	MCO
PA14	SWCLK	USART1_TX	-	-	USART2_TX	-	-	EVENTOUT	USART3_TX	-	SPI1_SCK/ I2S1_CK	-	-	-	-	MCO
PA15	SPI1_NSS/ I2S1_WS	USART1_RX	-	-	USART2_RX	-	-	EVENTOUT	USART3_RX	-	-	-	-	-	-	-

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3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-4 Port B alternate function mapping

Port B	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	SPI1_NSS/ I2S1_WS	TIM2_CH3	TIM1_CH2N	-	-	EVENTOUT	-	COMP1_OUT	-	-	-	USART3_CK	-	-	-	-
PB1	TIM14_CH1	TIM2_CH4	TIM1_CH3N	-	-	-	-	EVENTOUT	-	-	-	USART3_RTS	-	-	-	-
PB2	USART1_RX	-	TIM1_CH2	USART2_RX	-	-	-	-	USART3_RX	-	SPI2_SCK	-	-	-	-	-
PB3	SPI1_SCK/ I2S1_CK	TIM1_CH2	-	USART1_RTS	USART2_RTS	-	-	EVENTOUT	USART3_RTS	-	-	-	-	-	-	-
PB4	SPI1_MISO/ I2S1_MCK	TIM2_CH1	-	USART1_CTS	USART2_CTS	TIM17_BKIN	-	EVENTOUT	USART3_CTS	-	-	-	-	-	-	-
PB5	SPI1_MOSI/ I2S1_SD	TIM2_CH2	TIM16_BKIN	USART1_CK	USART2_CK	-	-	COMP1_OUT	USART3_CK	-	-	-	-	TIM1_CH1	-	-
PB6	USART1_TX	TIM1_CH3	TIM16_CH1N	SPI2_MISO	USART2_TX	-	I2C1_SCL	EVENTOUT	-	-	-	I2C2_SCL	-	-	-	-
PB7	USART1_RX	SPI2_MOSI	TIM17_CH1N	-	USART2_RX	-	I2C1_SDA	EVENTOUT	-	-	-	I2C2_SDA	-	TIM1_CH2	-	-
PB8	-	SPI2_SCK	TIM16_CH1	-	USART2_TX	I2C2_SCL	I2C1_SCL	EVENTOUT	USART1_TX	-	-	SPI2_NSS	I2C1_SDA	TIM17_CH1	I2C2_SDA	IR_OUT
PB9	-	-	TIM17_CH1	-	-	-	-	EVENTOUT	-	-	-	-	-	-	-	IR_OUT
PB10	SPI2_SCK	-	TIM2_CH3	USART3_TX	-	-	-	-	-	-	-	I2C2_SCL	I2C1_SCL	-	-	-
PB11	-	-	TIM2_CH4	USART3_RX	-	-	-	EVENTOUT	-	-	-	I2C2_SDA	I2C1_SDA	-	-	-
PB12	SPI1_NSS/ I2S1_WS	SPI2_NSS	TIM1_BKIN	-	-	-	-	EVENTOUT	-	-	-	USART3_RTS	-	TIM1_BKIN	-	-
PB13	SPI2_SCK	-	TIM1_CH1N	-	-	-	-	-	-	-	SPI1_SCK/ I2S1_CK	USART3_CTS	-	-	-	-
PB14	SPI2_MISO	-	TIM1_CH2N	-	-	-	-	-	-	-	SPI1_MISO/ I2S1_MCK	USART3_RTS	-	-	-	-
PB15	SPI2_MOSI	-	TIM1_CH3N	-	-	-	-	-	-	-	SPI1_MOSI/ I2S1_SD	-	-	-	-	-

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3.3. Alternate functions selected through GPIOF_AFR registers for port F

Table 3-5 Port F alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	-	-	TIM14_CH1	SPI2_SCK	USART2_RX	-	-	-	USART1_RX	USART2_TX	-	I2C2_SDA	I2C1_SDA	-	-	-
PF1	-	-	-	SPI2_MISO	USART2_TX	-	-	-	USART1_TX	USART2_RX	SPI1_NSS/ I2S1_WS	I2C2_SCL	I2C1_SCL	TIM14_CH1	-	-
PF2	-	TIM2_CH2	TIM1_CH2	SPI2_MOSI	USART2_RX	-	MCO	-	-	-	-	-	-	TIM1_CH1N	-	-
PF3	USART1_TX	-	-	SPI2_MISO	USART2_TX	-	-	-	-	-	SPI1_NSS/ I2S1_WS	-	-	TIM2_CH3	-	RTC_OUT
PF4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PF5	-	IR_OUT	-	-	-	-	-	EVENTOUT	USART1_RX	-	SPI1_MISO / I2S1_MCK	I2C2_SCL	I2C2_SDA	TIM1_CH2	-	-
PF6	-	USART1_TX	TIM1_CH2N	-	USART2_TX	-	-	EVENTOUT	-	-	-	I2C2_SDA	I2C2_SCL	-	-	-
PF7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PF8	-	-	TIM1_CH1	SPI2_MOSI	USART2_RX	-	MCO	-	-	-	-	-	-	-	-	-
PF9	-	TIM2_CH1	TIM1_CH1N	SPI2_SCK	USART2_TX	-	-	-	-	-	-	-	-	-	-	-
PF10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PF11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

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4. Memory mapping

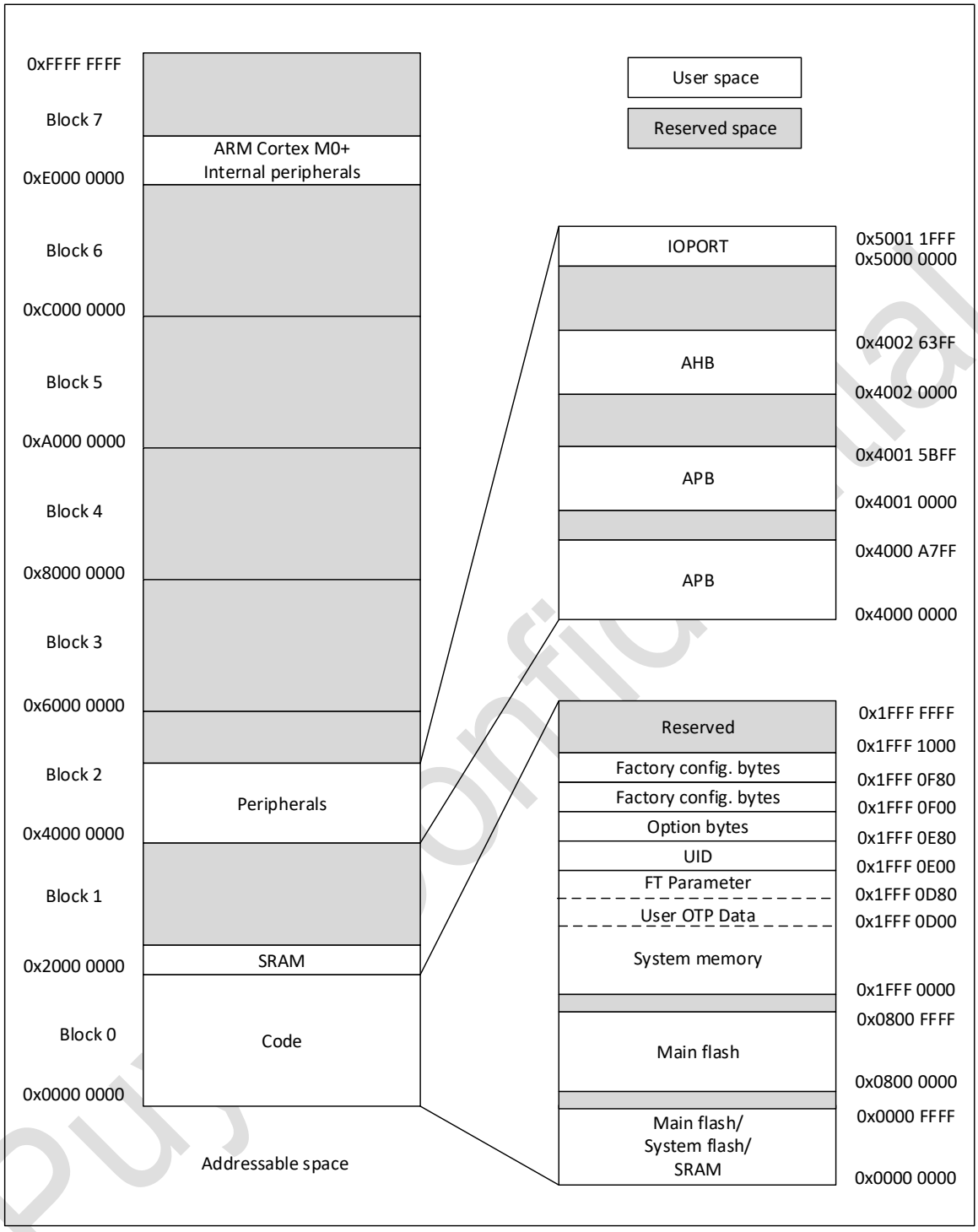


Figure 4-1 Memory mapping

Table 4-1 Memory boundary address

Type	Boundary address	Size	Memory area	Description
SRAM	0x2000 2000-0x3FFF FFFF	-	Reserved	-
	0x2000 0000-0x2000 1FFF	8 KB	SRAM	-
Code	0x1FFF 1000-0x1FFF FFFF	-	Reserved	-
	0x1FFF 0F80-0x1FFF 0FFF	128 bytes	Factory config. bytes	-
	0x1FFF 0F00-0x1FFF 0F7F	128 bytes	Factory config. bytes	-

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Type	Boundary address	Size	Memory area	Description
	0x1FFF 0E80-0x1FFF 0EFF	128 bytes	Option bytes	Option bytes information
	0x1FFF 0E00-0x1FFF 0E7F	128 bytes	UID	Unique ID
	0x1FFF 0D80-0x1FFF 0DFF	128 bytes	FT parameter	-
	0x1FFF 0D00-0x1FFF 0D7F	128 bytes	User OTP Data	User OTP
	0x1FFF 0000-0x1FFF 0CFF	3.25 KB	System memory	Store Boot loader
	0x0801 0000-0x1FFE FFFF	-	Reserved	-
	0x0800 0000-0x0800 FFFF	64 KB	Main flash memory	-
	0x0001 0000-0x07FF FFFF	-	Reserved	-
	0x0000 0000-0x0000 FFFF	64 KB	Selection based on Boot configuration: 1) Main flash memory 2) System flash memory 3) SRAM	-

1. The address is marked as Reserved, which cannot be written, read as 0, and a response error is generated.

Table 4-2 Peripheral register address

Bus	Boundary address	Size	Peripheral
-	0xE000 000-0xE00F FFFF	1 MB	M0+
IOPORT	0x5000 1800-0x5FFF FFFF	-	Reserved
	0x5000 1400-0x5000 17FF	1 KB	GPIOF
	0x5000 0800-0x5000 13FF	-	Reserved
	0x5000 0400-0x5000 07FF	1 KB	GPIOB
	0x5000 0000-0x5000 03FF	1 KB	GPIOA
AHB	0x4002 3C00-0x4FFF FFFF	-	Reserved
	0x4002 3800-0x4002 3BFF	1 KB	HDIV
	0x4002 3400-0x4002 37FF	1 KB	CORDIC
	0x4002 3000-0x4002 33FF	1 KB	CRC
	0x4002 2400-0x4002 2FFF	-	Reserved
	0x4002 2000-0x4002 23FF	1 KB	Flash
	0x4002 1C00-0x4002 1FFF	-	Reserved
	0x4002 1800-0x4002 1BFF	1 KB	EXTI
	0x4002 1400-0x4002 17FF	-	Reserved
	0x4002 1000-0x4002 13FF	1 KB	RCC
	0x4002 0400-0x4002 0FFF	-	Reserved
	0x4002 0000-0x4002 03FF	1 KB	DMA
APB	0x4001 5C00-0x4001 FFFF	-	Reserved
	0x4001 5800-0x4001 5BFF	1 KB	DBG
	0x4001 4C00-0x4001 57FF	-	Reserved
	0x4001 4800-0x4001 4BFF	1 KB	TIM17
	0x4001 4400-0x4001 47FF	1 KB	TIM16
	0x4001 3C00-0x4001 43FF	-	Reserved
	0x4001 3800-0x4001 3BFF	1 KB	USART1

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Bus	Boundary address	Size	Peripheral
	0x4001 3400-0x4001 37FF	-	Reserved
	0x4001 3000-0x4001 33FF	1 KB	SPI1
	0x4001 2C00-0x4001 2FFF	1 KB	TIM1
	0x4001 2800-0x4001 2BFF	-	Reserved
	0x4001 2400-0x4001 27FF	1KB	ADC
	0x4001 0400-0x4001 23FF	-	Reserved
	0x4001 0300-0x4001 03FF	1KB	OPA
	0x4001 0200-0x4001 02FF		COMP1 and COMP2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 8000-0x4000 FFFF	-	Reserved
	0x4000 7C00-0x4000 7FFF	1 KB	LPTIM
	0x4000 7400-0x4000 7BFF	-	Reserved
	0x4000 7000-0x4000 73FF	1 KB	PWR
	0x4000 5C00-0x4000 6FFF	-	Reserved
	0x4000 5800-0x4000 5BFF	1 KB	I2C2
	0x4000 5400-0x4000 57FF	1 KB	I2C1
	0x4000 4C00-0x4000 53FF	-	Reserved
	0x4000 4800-0x4000 4BFF	1 KB	USART3
	0x4000 4400-0x4000 47FF	1 KB	USART2
	0x4000 3C00-0x4000 43FF	-	Reserved
	0x4000 3800-0x4000 3BFF	1 KB	SPI2
	0x4000 3400-0x4000 37FF	-	Reserved
	0x4000 3000-0x4000 33FF	1 KB	IWDG
	0x4000 2C00-0x4000 2FFF	1 KB	WWDG
	0x4000 2800-0x4000 2BFF	1 KB	RTC
	0x4000 2400-0x4000 27FF	1 KB	LCD
	0x4000 2000-0x4000 23FF	1 KB	TIM14
	0x4000 0400-0x4000 1FFF	-	Reserved
	0x4000 0000-0x4000 03FF	1 KB	TIM2

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5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A(max) (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation.

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A = 25 °C and V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95 % of the devices have an error less than or equal to the value indicated (measured value ±2σ).

5.1.3. Power supply diagram

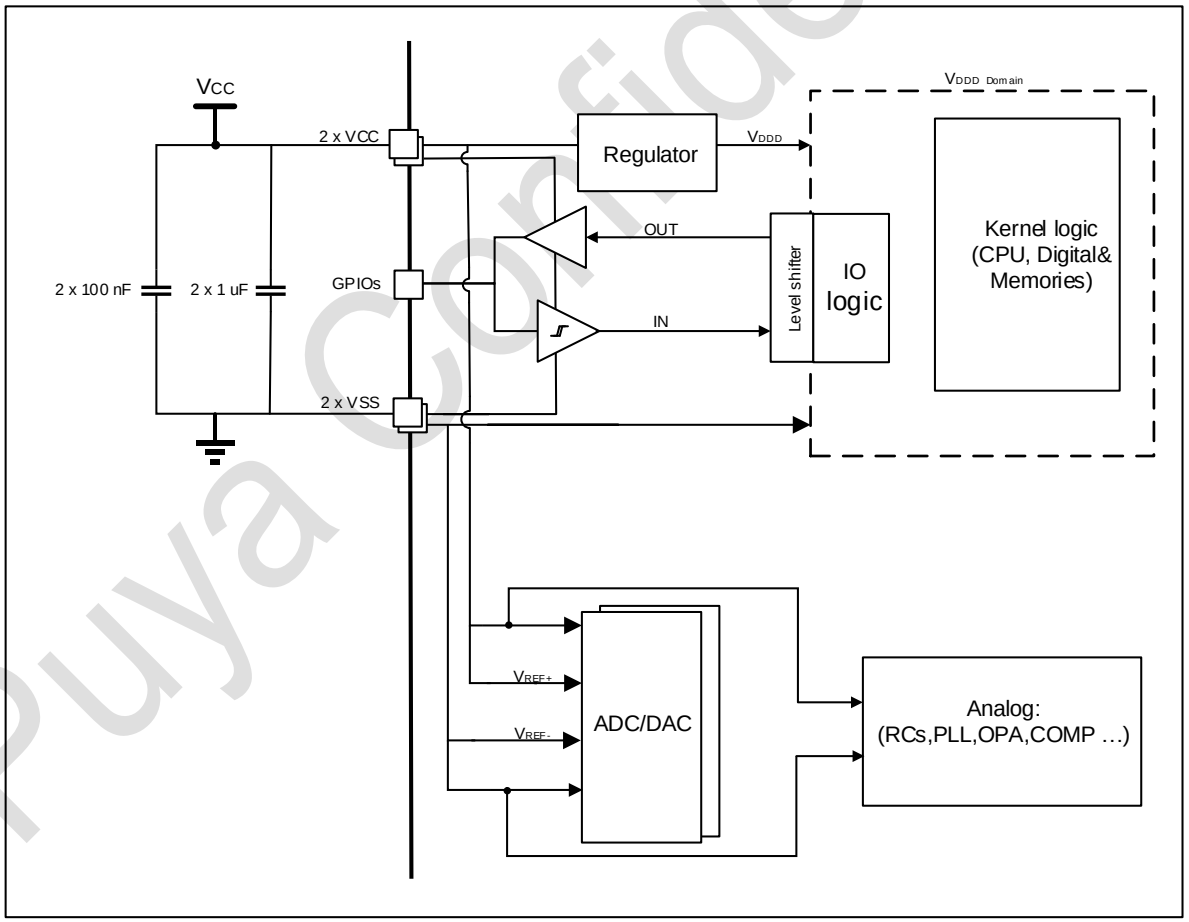


Figure 5-1 Power supply diagram

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5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Descriptions	Min	Max	Unit
V_{CC}	External mains power supply	-0.3	6.25	V
V_{IN}	Input voltage of other pins	-0.3	V_{CC}+0.3	V

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.

Table 5-2 Current characteristics

Symbol	Descriptions	Max	Unit
ΣI_{VCC}	Total current into sum of all V_{CC} power lines (source)(1)	150	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
$\Sigma I_{IO(PIN)}$(2)	Total output current sunk by sum of all I/Os and control pins	110	
	Total output current sourced by sum of all I/Os and control pins	110	
$I_{IO(PIN)}$(2)	Output current sunk by any I/O and control pin except COM_L I/O	30	
	Output current sunk by any COM_L I/O	90	
	Output current sourced by any I/O and control pin	30	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.

Table 5-3 Thermal characteristics

Symbol	Descriptions	Conditions	Value	Unit
T_{STG}	Storage temperature range	-	-65 to +150	°C
T_J	Maximum junction temperature	-	+150	°C

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK}	Internal APB clock frequency	-	0	72	MHz
V_{CC}	Standard operating voltage	-	1.7	5.5	V
V_{IN}	I/O input voltage	-	-0.3	V_{CC}+0.3	V
T_A	Ambient temperature	x6 version	-40	85	°C
		x7 version	-40	105	
T_J	Junction temperature	x6 version	-40	90	°C
		x7 version	-40	110	

5.3.2. Operating conditions at power-on / power-down

Table 5-5 Operating conditions at power-on / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise rate	-	10	∞	μs/V
	V_{CC} fall rate	-	30	∞	

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5.3.3. Embedded reset and PVD module characteristics

Table 5-6 POR/PDR/BOR module characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization	-	-	4.0	7.5	ms
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.53(2)	1.63	1.70	V
		Falling edge	1.50	1.60	1.68(2)	
V_{BOR1}	BOR1 threshold	Rising edge	1.70(2)	1.80	1.90	V
		Falling edge	1.60	1.70	1.80(2)	
V_{BOR2}	BOR2 threshold	Rising edge	1.90(2)	2.00	2.10	V
		Falling edge	1.80	1.90	2.00(2)	
V_{BOR3}	BOR3 threshold	Rising edge	2.10(2)	2.20	2.30	V
		Falling edge	2.00	2.10	2.20(2)	
V_{BOR4}	BOR4 threshold	Rising edge	2.30(2)	2.40	2.50	V
		Falling edge	2.20	2.30	2.40(2)	
V_{BOR5}	BOR5 threshold	Rising edge	2.50(2)	2.60	2.70	V
		Falling edge	2.40	2.50	2.60(2)	
V_{BOR6}	BOR6 threshold	Rising edge	2.70(2)	2.80	2.90	V
		Falling edge	2.60	2.70	2.80(2)	
V_{BOR7}	BOR7 threshold	Rising edge	2.90(2)	3.00	3.10	V
		Falling edge	2.80	2.90	3.00(2)	
V_{BOR8}	BOR8 threshold	Rising edge	3.10(2)	3.20	3.30	V
		Falling edge	3.00	3.10	3.20(2)	
$V_{POR_PDR_hyst}$(1)	POR/PDR hysteresis	-	-	30	-	mV
$I_{CC\ (BOR)}$ (1)	BOR consumption	-	-	0.6	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

Table 5-7 PVD module characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	PVD0 threshold	Rising edge	1.74(2)	1.84	1.94	V
		Falling edge	1.64	1.74	1.84(2)	
V_{PVD1}	PVD1 threshold	Rising edge	1.94(2)	2.04	2.14	V
		Falling edge	1.84	1.94	2.04(2)	
V_{PVD2}	PVD2 threshold	Rising edge	2.12(2)	2.22	2.32	V
		Falling edge	2.02	2.12	2.22(2)	
V_{PVD3}	PVD3 threshold	Rising edge	2.32(2)	2.42	2.52	V
		Falling edge	2.22	2.32	2.42(2)	
V_{PVD4}	PVD4 threshold	Rising edge	2.55(2)	2.65	2.75	V
		Falling edge	2.45	2.55	2.65(2)	
V_{PVD5}	PVD5 threshold	Rising edge	2.75(2)	2.85	2.95	V
		Falling edge	2.65	2.75	2.85(2)	
V_{PVD6}	PVD6 threshold	Rising edge	2.95(2)	3.05	3.15	V
		Falling edge	2.85	2.95	3.05(2)	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD7}	PVD7 threshold	Rising edge	3.15(2)	3.25	3.35	V
		Falling edge	3.05	3.15	3.25(2)	
$V_{PVD_BOR_hyst}$(1)	PVD hysteresis	-	-	100	-	mV
$I_{CC\ (PVD)}$ (1)	PVD power consumption	-	-	0.6	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

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5.3.4. Supply current characteristics

Table 5-8 Current consumption in Run mode

Symbol	Conditions					Typ(1)			Max(1)			Unit
	Code	Run	System clock	Frequency	Peripheral clock	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{CC} (Run)	While(1)	Flash	HSI、PLL(x3)	72 MHz	ON	6.26	12.48	16.54	6.93	16.71	34.02	mA
					OFF	4.28	8.77	14.92	4.47	12.05	26.78	
			HSI、PLL(x2)	48 MHz	ON	4.81	9.67	15.42	5.10	13.15	28.49	
					OFF	3.42	7.09	12.99	3.55	9.89	23.63	
			HSI	24 MHz	ON	2.74	5.78	11.30	2.82	8.25	21.06	
					OFF	2.10	4.55	9.60	2.16	6.71	18.18	
				16 MHz	ON	1.95	4.28	9.27	2.00	6.38	17.56	
					OFF	1.52	3.48	8.02	1.57	5.38	14.95	
				8 MHz	ON	1.18	2.80	7.00	1.21	4.53	12.53	
					OFF	0.98	2.34	6.32	0.99	3.95	10.88	
				4 MHz	ON	0.75	1.84	5.48	0.76	3.31	9.00	
					OFF	0.64	1.54	4.94	0.65	2.91	8.04	
			HSE bypass、PLL(x3)	72 MHz	ON	6.30	12.01	16.34	6.99	15.97	32.15	
					OFF	4.27	8.16	13.98	4.57	11.09	25.46	
			HSE bypass、PLL(x2)	48 MHz	ON	4.82	9.17	14.87	5.22	12.36	27.28	
					OFF	3.50	6.56	12.45	3.68	9.05	22.71	
			HSE bypass	32 MHz	ON	4.84	6.63	11.33	4.71	9.17	22.20	
					OFF	3.62	5.05	10.07	3.88	7.19	19.52	
				8 MHz	ON	1.39	2.63	7.04	1.44	4.17	12.68	
					OFF	1.18	2.23	6.46	1.23	3.68	11.31	
				1 MHz	ON	0.64	1.17	4.41	0.67	2.33	7.40	
					OFF	0.61	1.12	4.25	0.64	2.28	7.19	
			LSI	32.768 kHz (SLEEP_EN = 0)	ON	0.19	0.33	2.08	0.20	1.30	3.77	
					OFF	0.19	0.33	2.06	0.20	1.30	3.76	
				32.768 kHz (SLEEP_EN = 1)	ON	0.12	0.23	1.59	0.13	1.18	2.96	
					OFF	0.12	0.23	1.58	0.13	1.18	2.94	

1. Data based on characterization results, not tested in production.

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Table 5-9 Current consumption in Run mode

Symbol	Conditions					Typ(1)			Max(1)			Unit
	Code	Run	System clock	Frequency	Peripheral clock	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 25 °C	T_A = 85 °C	T_A =105 °C	
I_{CC} (Run)	While(1)	SRAM	HSI、PLL(x3)	72 MHz	ON	6.22	12.01	16.57	6.70	16.00	34.01	mA
					OFF	4.18	8.01	14.67	4.35	10.90	26.89	
			HSI、PLL(x2)	48 MHz	ON	4.50	8.67	15.22	4.70	11.75	28.05	
					OFF	3.21	6.07	12.56	3.30	8.45	23.27	
			HSI	24 MHz	ON	2.23	4.22	10.10	2.30	6.13	19.34	
					OFF	1.60	3.07	8.28	1.65	4.72	15.78	
				16 MHz	ON	1.58	3.04	8.25	1.63	4.69	15.72	
					OFF	1.16	2.27	6.98	1.20	3.74	12.72	
				8 MHz	ON	0.93	1.83	6.24	0.96	3.19	10.93	
					OFF	0.71	1.39	5.44	0.74	2.64	9.13	
				4 MHz	ON	0.61	1.17	4.92	0.63	2.37	8.20	
					OFF	0.50	0.94	4.25	0.52	2.07	7.18	
			HSE bypass、PLL(x3)	72 MHz	ON	6.36	11.92	16.38	6.87	15.80	32.52	
					OFF	4.32	8.07	14.14	4.52	10.93	25.80	
			HSE bypass、PLL(x2)	48 MHz	ON	4.64	8.69	14.60	4.86	11.71	26.87	
					OFF	3.35	6.15	11.97	3.47	8.51	22.35	
			HSE bypass	32 MHz	ON	2.95	5.45	11.11	3.07	7.63	21.15	
					OFF	2.12	3.90	9.10	2.22	5.70	17.51	
				8 MHz	ON	1.15	2.16	6.38	1.20	3.58	11.34	
					OFF	0.94	1.77	5.72	0.98	3.11	9.88	
				1 MHz	ON	0.61	1.18	4.36	0.64	2.35	7.36	
					OFF	0.58	1.13	4.21	0.61	2.29	7.14	
			LSI	32.768 kHz (SLEEP_EN = 0)	ON	0.19	0.40	2.04	0.20	1.40	3.93	
					OFF	0.19	0.40	1.86	0.20	1.40	3.91	
				32.768 kHz (SLEEP_EN = 1)	ON	0.10	0.25	1.45	0.11	1.21	2.87	
					OFF	0.10	0.24	1.44	0.11	1.21	2.86	

1. Data based on characterization results, not tested in production.

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Table 5-10 Current consumption in Sleep mode

Symbol	Conditions			Typ(1)			Max(1)			Unit
	System clock	Frequency	Peripheral clock	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{CC}(Sleep)	HSI、PLL(x3)	72 MHz	ON	4.56	8.73	15.17	4.67	11.37	28.11	mA
			OFF	2.33	4.29	10.20	2.40	5.77	19.57	
	HSI、PLL(x2)	48 MHz	ON	3.45	6.50	12.99	3.53	8.54	24.01	
			OFF	1.99	3.64	9.24	2.05	4.96	17.74	
	HSI	24 MHz	ON	1.72	3.20	8.54	1.77	4.42	16.37	
			OFF	0.98	1.89	6.29	1.01	2.83	11.05	
		16 MHz	ON	1.24	2.37	7.12	1.28	3.42	13.09	
			OFF	0.74	1.46	5.44	0.77	2.29	9.11	
		8 MHz	ON	0.75	1.48	5.50	0.78	2.32	9.22	
			OFF	0.50	0.96	4.10	0.52	1.67	6.92	
		4 MHz	ON	0.52	1.00	4.23	0.54	1.72	7.10	
			OFF	0.39	0.74	3.36	0.41	1.39	5.83	
	HSE bypass、PLL(x3)	72 MHz	ON	4.64	8.67	14.65	4.81	11.23	26.80	
			OFF	2.44	4.36	9.76	2.54	5.82	18.69	
	HSE bypass、PLL(x2)	48 MHz	ON	3.56	6.52	12.48	3.67	8.52	22.98	
			OFF	2.11	3.71	8.88	2.19	5.02	17.00	
	HSE bypass	32 MHz	ON	3.57	5.37	10.97	4.02	7.42	19.62	
			OFF	2.77	3.38	8.50	3.47	4.88	14.83	
		8 MHz	ON	0.97	1.78	5.78	1.01	2.67	9.94	
			OFF	0.72	1.34	4.85	0.76	2.11	8.09	
		1 MHz	ON	0.59	1.08	4.08	0.61	1.79	7.02	
			OFF	0.56	1.02	3.90	0.58	1.71	6.77	
	LSI	32.768 kHz (SLEEP_EN = 0)	ON	0.19	0.37	1.74	0.20	0.92	3.72	
			OFF	0.18	0.37	1.73	0.20	0.92	3.70	
		32.768 kHz (SLEEP_EN = 1)	ON	0.10	0.22	1.18	0.11	0.74	2.64	
			OFF	0.10	0.22	1.17	0.11	0.74	2.63	

1. Data based on characterization results, not tested in production.

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Table 5-11 Current consumption in Stop mode

Symbol	Conditions				Typ(1)			Max(1)			Unit
	V_{CC}	LDO mode	LSI	Peripheral clock	T_A = 85 °C	T_A = 85 °C	T_A = 85 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{CC}(Stop)	1.7 to 5.5 V	MR	ON	RTC+IWDG+LPTIM	88.6	218.0	1269.3	95.9	736.7	2671.4	μA
				IWDG	88.5	217.7	1268.1	95.8	736.3	2668.7	
				LPTIM	88.5	217.6	1269.4	95.8	736.1	2667.2	
				RTC	88.5	217.7	1268.0	95.8	736.2	2662.3	
			OFF	Peripheral OFF	88.4	217.2	1267.6	95.8	736.0	2662.1	
		LPR	ON	RTC+IWDG+LPTIM	4.2	39.4	290.7	4.9	68.3	722.1	
				IWDG	4.1	39.2	290.2	4.8	67.4	719.2	
				LPTIM	4.1	39.2	290.2	4.8	68.0	716.8	
				RTC	4.1	39.1	290.2	4.8	67.4	715.7	
			OFF	Peripheral OFF	4.0	39.1	290.0	4.7	67.2	715.6	

1. Data based on characterization results, not tested in production.

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5.3.5. Wake-up time from low-power mode

Table 5-12 Wake-up time from low-power mode

Symbol	Parameter(1)	LDO mode	Conditions	Typ(2)	Max	Unit
$t_{WMSLEEP}$	Wake-up from Sleep mode	-	-	10.0	-	CPU cycles
t_{WUSTOP}	Wake-up from Stop mode	MR	Run program in Flash HSI (24 MHz) as system clock FLS_SLPTIIME[1:0] = 00	6.5	-	μs
			Run program in Flash HSI (8 MHz) as system clock FLS_SLPTIIME[1:0] = 00	9.4	-	
		LPR	Run program in Flash HSI (24 MHz) as system clock FLS_SLPTIIME[1:0] = 00	10.2	-	
			Run program in Flash HSI (8 MHz) as system clock FLS_SLPTIIME[1:0] = 00	13.1	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data based on characterization results, not tested in production.

5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the device stops working, the corresponding I/O is used as a standard GPIO.

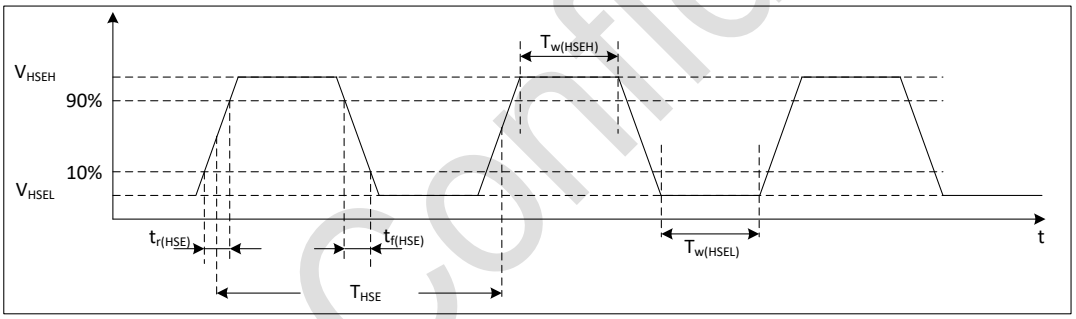


Figure 5-2 High-speed external clock timing diagram

Table 5-13 High-speed external clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	1	8	32	MHz
V_{HSEH}	Input pin high level voltage	0.7*V_{CC}	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	Vss	-	0.3*V_{CC}	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	High or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Rise or fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

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5.3.6.2. Low-speed external clock generated from an external source

In the bypass mode of LSE (the LSEBYP of RCC_BDCR is set), the low-speed start-up circuit in the device stops working, and the corresponding I/O is used as a standard GPIO.

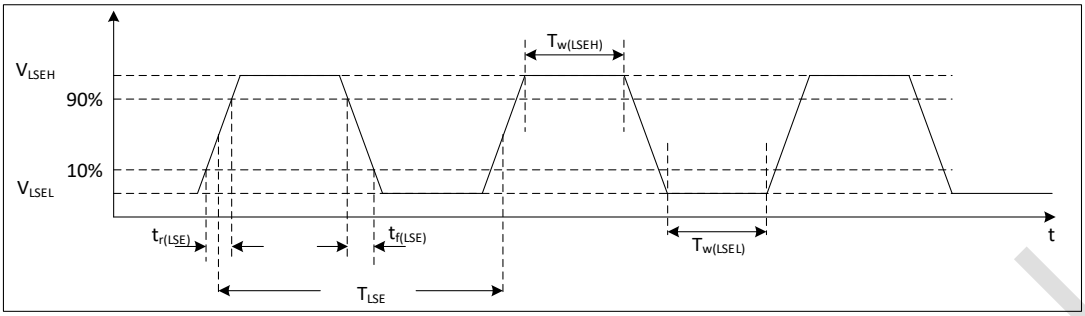


Figure 5-3 Low-speed external clock timing diagram

Table 5-14 Low-speed external clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	32.768	1000	kHz
V_{LSEH}	Input pin high level voltage	0.7*V_{CC}	-	-	V
V_{LSEL}	Input pin low level voltage	-	-	0.3*V_{CC}	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	High or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Rise or fall time	-	-	50	ns

1. Guaranteed by design, not tested in production.

5.3.6.3. High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with 4 to 32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-15 HSE oscillator characteristics

Symbol	Parameter	Conditions (1)(5)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
I_{CC}(4)	HSE current consumption	Startup time	-	-	5.5	mA
		R_m= 150 Ω, C_L= 10 pF@8 MHz HSE_DRV [1:0] = 01	-	0.67	-	
		R_m= 60 Ω, C_L= 20 pF@16 MHz HSE_DRV [1:0] = 10	-	1.31	-	
		R_m= 60 Ω, C_L= 9 pF@24 MHz HSE_DRV [1:0] = 10	-	1.35	-	
		Rm=60 Ω, C_L= 9 pF@24 MHz HSE_DRV [1:0] = 11	-	1.80	-	
		R_m = 40 Ω, C_L = 10 pF@32 MHz HSE_DRV [1:0] = 11	-	1.86	-	
$t_{SU(HSE)}$(3)(4)	Startup time	R_m= 150 Ω, C_L= 10 pF@8 MHz HSE_DRV [1:0] = 01	-	1.23	-	ms
		R_m= 60 Ω, C_L= 20 pF@16 MHz HSE_DRV [1:0] = 10	-	1.67	-	
		R_m= 60 Ω, C_L= 9 pF@24 MHz HSE_DRV [1:0] = 10	-	0.44	-	
		R_m= 60 Ω, C_L= 9 pF@24 MHz HSE_DRV [1:0] = 11	-	0.35	-	
		R_m = 40 Ω, C_L = 10 pF@32 MHz HSE_DRV [1:0] = 11	-	0.33	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.

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2. Guaranteed by design, not tested in production.
3. $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state, measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another.
4. Data based on characterization results, not tested in production.
5. HSE_DRV[1:0] = 00 is reserved which needs to be adjusted for use.

5.3.6.4. Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-16 LSE oscillator characteristics

Symbol	Parameter	Conditions (1)(5)	Min(2)	Typ	Max(2)	Unit
I_{CC}(4)	LSE current consumption	R_m= 80 kΩ, C_L= 6 pF LSE_DRIVER [1:0] = 01	-	770	-	nA
		R_m= 70 kΩ, C_L= 12 pF LSE_DRIVER [1:0] = 10	-	1010	-	
		R_m= 70 kΩ, C_L= 12 pF LSE_DRIVER [1:0] = 11	-	1370	-	
$t_{SU(LSE)}$(3)(4)	Startup time	R_m= 80 kΩ, C_L= 6 pF LSE_DRIVER [1:0] = 01	-	218.3	-	ms
		R_m= 70 kΩ, C_L= 12 pF LSE_DRIVER [1:0] = 10	-	234.2	-	
		R_m= 70 kΩ, C_L= 12 pF LSE_DRIVER [1:0] = 11	-	184.7	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable, measured for a standard crystal/resonator, which may vary greatly from crystal to resonator.
4. Data based on characterization results, not tested in production.
5. LSE_DRIVER[1:0] = 00 is reserved which needs to be adjusted for use.

5.3.7. High-speed internal (HSI) RC oscillator

Table 5-17 HSI RC oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	T_A= 25 °C, V_{CC}= 3.3 V	23.76	24	24.24	MHz
			21.90	22.12	22.34	
			15.84	16	16.16	
			7.92	8	8.08	
			3.96	4	4.04	
$\Delta_{Temp(HSI)}$	HSI frequency drift over temperature	T_A = 25 °C	-1(2)	-	1(2)	%
		T_A = 0 to 85 °C	-2(2)	-	2(2)	
		T_A = -40 to 105 °C	-3(2)	-	3.5(2)	
f_{TRIM}(1)	HSI trimming step	-	0.02	0.1	0.2	%
D_{HSI}(1)	Duty cycle	-	45(1)	-	55(1)	%
$t_{Stab(HSI)}$	HSI stabilization time	4 MHz	-	2.1	4(1)	μs
		8 MHz	-	1.9	-	
		16 MHz	-	1.5	-	
		22.12 MHz	-	1.5	-	
		24 MHz	-	1.5	-	
$I_{CC(HSI)}$(2)	HSI power consumption	4 MHz	-	120	-	μA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		8 MHz	-	150	-	
		16 MHz	-	250	-	
		22.12 MHz	-	330	-	
		24 MHz	-	350	-	

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.8. Low-speed internal (LSI) RC oscillator

Table 5-18 LSI RC oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	T_A = 25 °C, V_{CC} = 3.3 V	-3	-	3	%
$\Delta_{Temp(LSI)}$	LSI frequency drift over temperature	T_A = 0 to 85 °C	-10(2)	-	10(2)	%
		T_A= -40 to 105 °C	-18(2)	-	18(2)	
f_{TRIM}(1)	LSI trimming step	-	-	0.2	-	%
$t_{Stab(LSI)}$ (1)	LSI stabilization time	-	-	150	-	μs
$I_{CC(LSI)}$(1)	LSI power consumption	-	-	300	-	nA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.9. Phase locked loop (PLL) characteristics

Table 5-19 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	T_A=25 °C, V_{CC}=3.3 V, PLL*2	16(1)	-	24(1)	MHz
		T_A=25 °C, V_{CC}=3.3 V, PLL*3	22(1)	-	24(1)	
f_{PLL_OUT}	PLL output clock	T_A=25 °C, V_{CC}=3.3 V	32(1)	-	72	MHz
Jitter	Period jitter	-	-	-	0.3(1)	ns
t_{LOCK}	PLL lock time	f_{PLL_IN}=24 MHz	-	15	40(1)	μs

1. Guaranteed by design, not tested in production.

5.3.10. Memory characteristics

Table 5-20 Memory characteristics(2)

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}	Page programming time	-	1.5	2.0	ms
t_{ERASE}	Page/sector/mass erase time	-	3.5	4.5	ms
I_{CC}	Page programming supply current	-	2.1	2.9	mA
	Page/sector/mass erase supply current	-	2.1	2.9	

1. Guaranteed by design, not tested in production.
2. Attention: During Flash erase/write operations, code cannot be executed from SRAM, otherwise the CPU will stop functioning.

Table 5-21 Memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 to 85 °C	100	kcycles
		T_A = 85 to 105 °C	10	
t_{RET}	Data retention time	10 kcycles T_A = 55 °C	20	Year

1. Data based on characterization results, not tested in production.

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5.3.11. EFT characteristics

Table 5-22 EFT characteristics

Symbol	Parameter	Conditions	Grade
EFT to Power	-	IEC61000-4-4	4A

5.3.12. ESD & LU characteristics

Table 5-23 ESD&LU characteristics

Symbol	Parameter	Conditions	Typ	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	8	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	ESDA/JEDEC JS-002-2018	2	kV
LU	Static latch-up	JESD78E	200	mA

5.3.13. I/O port characteristics

Table 5-24 I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{CC}= 1.7 to 5.5 V	0.7*V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC}= 1.7 to 5.5 V	-	-	0.3*V_{CC}	V
V_{hys}(1)	Schmitt trigger hysteresis	-	-	200	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	-	30	50	70	kΩ
R_{PD}	Weak pull-down equivalent resistor	-	30	50	70	kΩ
C_{IO}(1)	Pin capacitance	-	-	5	-	pF
$t_{ns(EXTI)}$(1)	Input filter width	ENI=1, ENS=1	3	-	15	ns
$t_{ns(I2C)}$(1)	I^2C input filter width	ENI=1, EIIC=1	50	-	300	ns

1. Guaranteed by design, not tested in production.

Table 5-25 Output voltage characteristics(4)

Symbol	Parameter(3)	Driver	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level for a COM I/O pin (except COM_L IO)	GPIOx_OSPEEDR = 11	I_{OL} = 20 mA, V_{CC} ≥ 5.0 V	-	0.6	V
			I_{OL} = 8 mA, V_{CC} ≥ 2.7 V	-	0.4	
			I_{OL} = 4 mA, V_{CC} = 1.8 V	-	0.5	
	Output low level voltage for an I/O pin(COM_L)(2)	GPIOx_OSPEEDR = 11, EHS = 1	I_{OL} = 80 mA, V_{CC} ≥ 3.3 V	-	0.8	
			I_{OL} = 60 mA, V_{CC} ≥ 3.3 V	-	0.5	
			I_{OL} = 40 mA, V_{CC} ≥ 3.3 V	-	0.5	
			I_{OL} = 20 mA, V_{CC} ≥ 3.3 V	-	0.5	
V_{OH}(1)	Output high level voltage for an I/O pin	GPIOx_OSPEEDR = 11	I_{OH} = 20 mA, V_{CC} ≥ 5.0 V	V_{CC}-0.6	-	V
			I_{OH} = 8 mA, V_{CC} ≥ 2.7 V	V_{CC}-0.4	-	
			I_{OH} = 4 mA, V_{CC} = 1.8 V	V_{CC}-0.5	-	

1. These I/O types refer to the terms and symbols defined by pins.
2. COM_L IO current (80 mA/60 mA/40 mA/20 mA) can be set by software.
3. Data based on characterization results, not tested in production.
4. The combined maximum current across all output pins (including contributions from both V_{OL} and V_{OH} states) must not exceed the $\Sigma I_{IO(PIN)}$ maximum rating specified in Table 5-2 Current characteristics.

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5.3.14. ADC characteristics

Table 5-26 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	1.7	-	5.5	V
I_{CC} (1)	V_{cc} pin current	f_s = 1 Msps	-	350	-	μA
f_{ADC}	ADC clock frequency	V_{CC} = 1.7 to 5.5 V	0.8	-	8(2)	MHz
		V_{CC} = 2.3 to 5.5 V	0.8	-	16(2)	
f_S	Sampling rate	V_{CC} = 1.7 to 5.5 V	-	-	0.5	Msps
		V_{CC} = 2.3 to 5.5 V	-	-	1	
C_{ADC}(1)	Internal sample and hold capacitor	-	-	5	8	pF
R_{AIN}(1)(3)	External input impedance	-	-	-	31	kΩ
R_{ADC}(1)	Sampling switch resistance	-	-	-	2.5	kΩ
t_{CAL}(1)	Calibration time	f_{ADC} = 16 MHz	4.375	-	7.4375	μs
			70	-	119	$1/f_{ADC}$
t_{samp}(1)	Sampling time	f_{ADC} = 16 MHz	0.219	-	14.970	μs
			3.5	-	239.5	$1/f_{ADC}$
t_{samp_setup}(1)	Sampling time for internal channels	-	20	-	-	μs
t_{conv}(1)	Total conversion time	-	12	-	248	$1/f_{ADC}$
t_{eoc}(1)	End of conversion time	-	0.5			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. When using external triggering, an additional delay of $1/f_{PCLK2}$ is required.

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error be low 1/4 of LSB. N = 12 (from 12-bit resolution).

Table 5-27 R_{AIN} max for f_{ADC}=16 MHz(1)

Ts (cycles)	t_S (μs)	R_{AIN} Max (kΩ)
3.5	0.21	0.3
5.5	0.34	1.9
7.5	0.46	3.5
13.5	0.84	8.3
28.5	1.78	20.4
41.5	2.59	30.9
134.5	8.41	-
239.5	14.96	-

1. Guaranteed by design, not tested in production.

Table 5-28 ADC static characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.7 V≤ V_{REFP} = V_{CC} ≤5.5 V, f_{ADC} ≤ 8 MHz	-	4	5	LSB
EO	Offset error		-	2	3	
EG	Gain error		-	4	8	
DNL	Differential nonlinearity		-	4	5	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INL	Integral nonlinearity		-	3	5	
ET	Total unadjusted error	2.3 V≤ V_{REFP} = V_{CC} ≤5.5 V, f_{ADC} ≤ 16 MHz	-	3	5	
EO	Offset error		-	2	3	
EG	Gain error		-	4	8	
DNL	Differential nonlinearity		-	2	3	
INL	Integral nonlinearity		-	2.5	4	

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

Table 5-29 ADC dynamic characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	1.7 V≤ V_{REFP} = V_{CC} ≤5.5 V, f_{ADC} ≤ 8 MHz	9.0	9.5	-	LSB
SINAD	Signal to noise and distortion ratio		56.0	59.0	-	
SNR	Signal to noise ratio		56.5	59.3	-	
SFDR	Spurious free dynamic range		67.0	74.8	-	
THD	Total harmonic distortion		-	-71.0	-64.0	
ENOB	Effective number of bits	2.3 V≤ V_{REFP} = V_{CC} ≤5.5 V, f_{ADC} ≤ 16 MHz	9.2	9.7	-	
SINAD	Signal to noise and distortion ratio		57.3	60.1	-	
SNR	Signal to noise ratio		57.7	61.0	-	
SFDR	Spurious free dynamic range		69.2	75.0	-	
THD	Total harmonic distortion		-	-72.0	-65.3	

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.15. Comparator characteristics

Table 5-30 Comparator characteris(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	Supply voltage	-		1.7	-	5.5	V
V_{IN}	Input voltage range	-		0	-	V_{CC}	V
t_{START}	Startup time	High-speed mode		-	-	5	µs
		Medium-speed mode		-	-	15	
t_D	Propagation delay	High-speed mode	200 mV step 100 mV over-drive	-	40	70	ns
			>200 mV step 100 mV over-drive	-	-	85	
		Medium-speed mode	200 mV step 100 mV over-drive	-	0.9	2.3	µs
			>200 mV step 100 mV over-drive	-	-	3.4	
V_{offset}	Offset voltage	-		-	±5	-	mV
I_{CC}	Operating current	High-speed mode	Static	-	250	400	µA
			With 50 kHz and ±100 mV overdrive square signal	-	250	-	
		Medium-speed mode	Static	-	5	7.5	
			With 50 kHz and ±100 mV overdrive square signal	-	6	-	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{sleep}	Sleep power consumption	-	-	-	1	-	nA

1. Guaranteed by design, not tested in production.

5.3.16. Operational amplifier characteristics

Table 5-31 Operational amplifier characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	2.2	-	5.5	V
V_i	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0.2	-	V_{CC}-0.2	V
I_O	Output current	-	-	-	1	mA
R_L	Load resistor	-	5	-	-	kΩ
C_L	Capacitive load	-	-	-	25	pF
t_{start}	Initialization time	-	-	-	20	μs
V_{IO}	Input offset voltage	$R_L \geq 5$ kΩ, $C_L \leq 25$ pF	-	±8	-	mV
UGBW	Unit gain bandwidth	$V_{CC} = 3.3$ V, $V_i = V_o = V_{CC}/2$, $R_L \geq 5$ kΩ, $C_L \leq 25$ pF	-	5(1)	-	MHz
SR	Slew rate	$R_L \geq 5$ kΩ, $C_L \leq 25$ pF	-	8	-	V/μs

1. Guaranteed by design, not tested in production.

5.3.17. Temperature sensor characteristics

Table 5-32 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±2	±5	℃
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/℃
V_{30}	Voltage at 30 °C (±5 °C)	0.73	0.76	0.79	V
t_{START}(1)	Start up time entering in continuous mode	-	70	120	μs
t_{samp_setup} (1)	ADC sampling time when reading the temperature	20	-	-	μs

1. Guaranteed by design, not tested in production.

5.3.18. LCD controller characteristics

Table 5-33 LCD controller characteristics

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
I_{LCD}(1)(3)	LCD supply current	External resistor drive mode	-	0.6	-	μA
		Internal low drive resistive mode	-	4	-	
		Internal middle drive resistive mode	-	7.5	-	
		Internal high drive resistive mode	-	10	-	
R_H(2)	Low drive resistance	-	-	1080	-	kΩ
R_M(2)	Middle drive resistance	-	-	540	-	
R_L(2)	High drive resistance	-	-	360	-	
V_{LCDH}	LCD adjustable highest level voltage	-	-	V_{CC}	-	V
V_{LCD3}	LCD highest level voltage	-	-	V_{LCDH}	-	
V_{LCD2}	LCD 2/3 level voltage	-	-	2/3*V_{LCDH}	-	
V_{LCD1}	LCD 1/3 level voltage	-	-	1/3*V_{LCDH}	-	

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Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{LCD0}	LCD lowest level voltage	-	-	V_{SS}	-	
ΔV_{LCD}(3)	LCD voltage deviation	T_A = -40 to 105 °C	-	-	±50	mV

1. LCD enabled with V_{CC} = 3.3 V, 1/4 duty, 1/3 bias, scan frequency 256 Hz, all pixels active, no LCD connected.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

5.3.19. Embedded voltage reference characteristics

Table 5-34 Embedded internal voltage reference (V_{REFINT}) characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.15	1.2	1.25	V
$t_{start_VREFINT}$	Start time of V_{REFINT}	-	10	15	μs
$T_{coeff_VREFINT}$	Temperature coefficient of V_{REFINT}	-	200	-	ppm/°C
I_{VCC}(1)	V_{REFINT} current consumption from V_{CC}	-	12	20	μA

1. Guaranteed by design, not tested in production.

5.3.20. ADC voltage reference buffer

Table 5-35 ADC voltage reference buffer (V_{REFBUF}) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REF25}	2.5 V voltage reference buffer	T_A= 25 °C, V_{CC}=3.3 V	2.47	2.5	2.53	V
V_{REF20}	2.048 V voltage reference buffer	T_A= 25 °C, V_{CC}=3.3 V	2.02	2.048	2.076	V
V_{REF15}	1.5 V voltage reference buffer	T_A= 25 °C, V_{CC}=3.3 V	1.48	1.5	1.52	V
V_{REF10}	1.024 V voltage reference buffer	T_A= 25 °C, V_{CC}=3.3 V	1.01	1.024	1.038	V
T_{coeff}(1)	Temperature coefficient of V_{REFBUF}	T_A = -40 to 105 °C	-	200	-	ppm/°C

5.3.21. Timer characteristics

Table 5-36 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.888	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	
Res_{TIM}	Timer resolution time	TIM1/14/16/17	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter internal clock period	-	-	2^{16}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	910	μs
	32-bit counter internal clock period	-	-	2^{32}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s

Table 5-37 LPTIM characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PRESC[2:0]	Min	Max	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.946	
/8	3	0.2441	15997.338	
/16	4	0.4883	32001.229	
/32	5	0.9766	64002.458	
/64	6	1.9531	127998.362	

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Prescaler	PRESC[2:0]	Min	Max	Unit
/128	7	3.9063	256003.277	

Table 5-38 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 5-39 WWDG characteristics (timeout period at 72 MHz PCLK)

Prescaler	WDGTB[1:0]	Min	Max	Unit
1*4096	0	0.057	3.641	ms
2*4096	1	0.114	7.282	
4*4096	2	0.228	14.564	
8*4096	3	0.455	29.127	

5.3.22. Communication interfaces

5.3.22.1. I²C interface characteristics

I²C interface meets the requirements of the I²C bus specification and reference manual:

- Standard-mode (Sm): 100 kHz
- Fast-mode (Fm): 400 kHz
- Fast-mode plus (Fm+): 1 MHz

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-40 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50	260	ns

5.3.22.2. SPI characteristics

Table 5-41 SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Full-duplex mode	Transmit only or receive only	-	36	MHz
			Simultaneous transmit and receive	-	24	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF		-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode		2*Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode		2*Tpclk	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, presc = 2		Tpclk-2	Tpclk+1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode		1	-	ns
		Slave mode		3	-	
$t_{h(MI)}$	Data input hold time	Master mode		5	-	ns
$t_{h(SI)}$		Slave mode		2	-	
$t_{a(SO)}$	Data output access time	Slave mode		0	3*Tpclk	ns
$t_{dis(SO)}$	Data output end time	Slave mode		2*Tpclk	-	ns

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Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	0	20	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	2	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	1	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

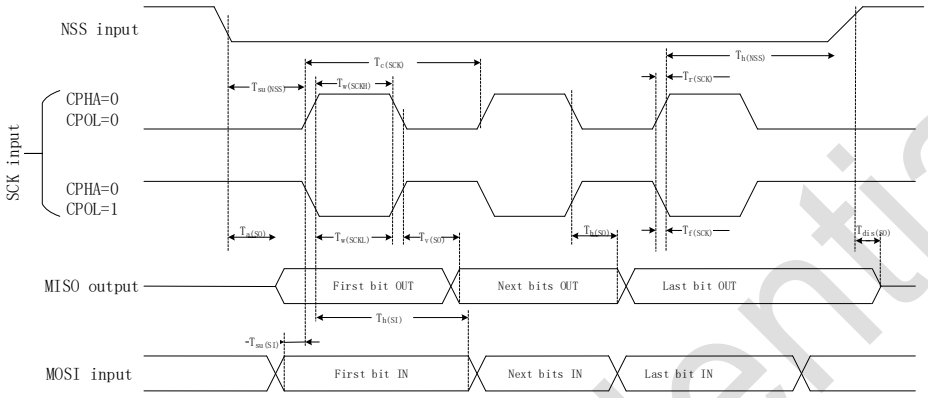


Figure 5-4 SPI timing diagram – Slave mode and CPHA=0

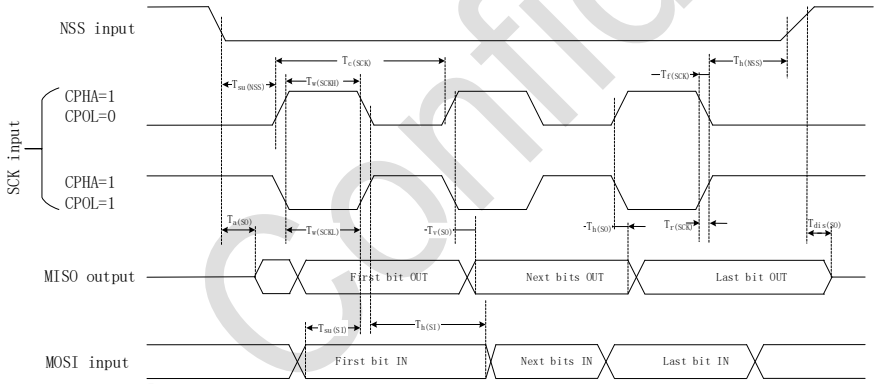


Figure 5-5 SPI timing diagram – Slave mode and CPHA=1

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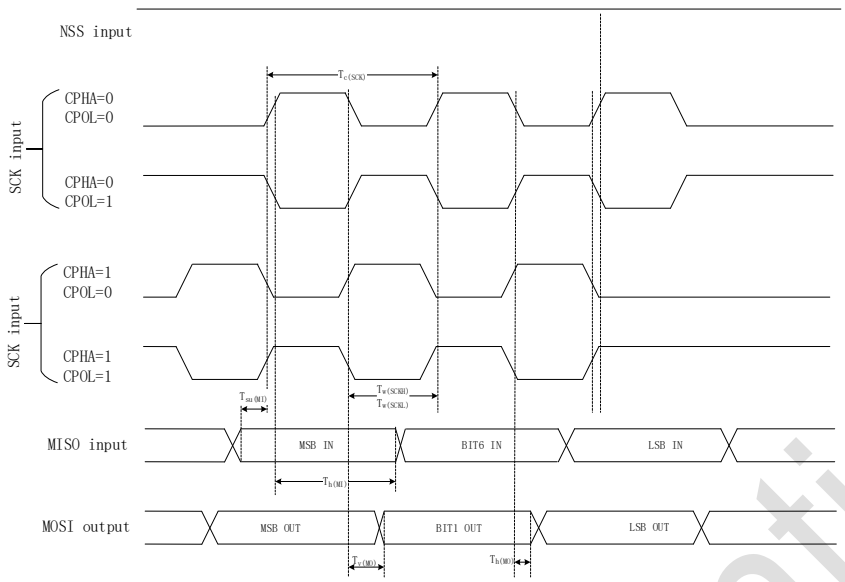


Figure 5-6 SPI timing diagram–Master mode

5.3.22.3. I²S characteristics

Table 5-42 I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_S	I²S audio sampling frequency	-	8	192	kHz
f_{MCLK}	I²S main clock output	-	256 x f_s	256 x f_s	kHz
f_{CK} $1/t_{c(CK)}$	I²S clock frequency	Master mode	-	64 x f_s	kHz
		Slave mode	-	64 x f_s	
D_{CK}	I²S clock duty cycle	Slave receiver	30	70	%
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load:C_L = 50 pF	-	8	ns
$t_{v(WS)}$	WS valid time	Master mode	-	2	
$t_{h(WS)}$	WS hold time	Master mode	3	-	
		Slave mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	4	-	
$t_{su(SD_MR)}$	Data input setup time	Master mode	3	-	
$t_{su(SD_SR)}$		Slave mode	4	-	
$t_{h(SD_MR)}$	Data input hold time	Master mode	5	-	
$t_{h(SD_SR)}$		Slave mode	2	-	
$t_{v(SD_ST)}$	Data output valid time	Slave mode (after enable edge)	-	20	
$t_{v(SD_MT)}$		Master mode (after enable edge)	-	5	
$t_{h(SD_ST)}$	Data output hold time	Slave mode (after enable edge)	2	-	
$t_{h(SD_MT)}$		Master mode (after enable edge)	1	-	

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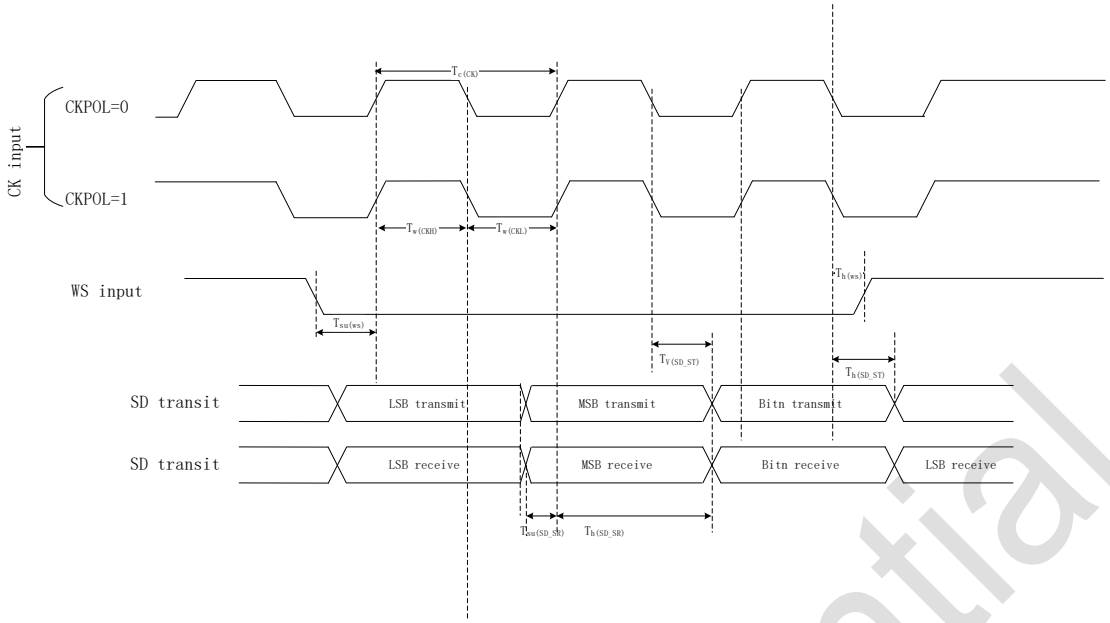


Figure 5-7 I²S timing diagram-Slave mode(Philips protocol)

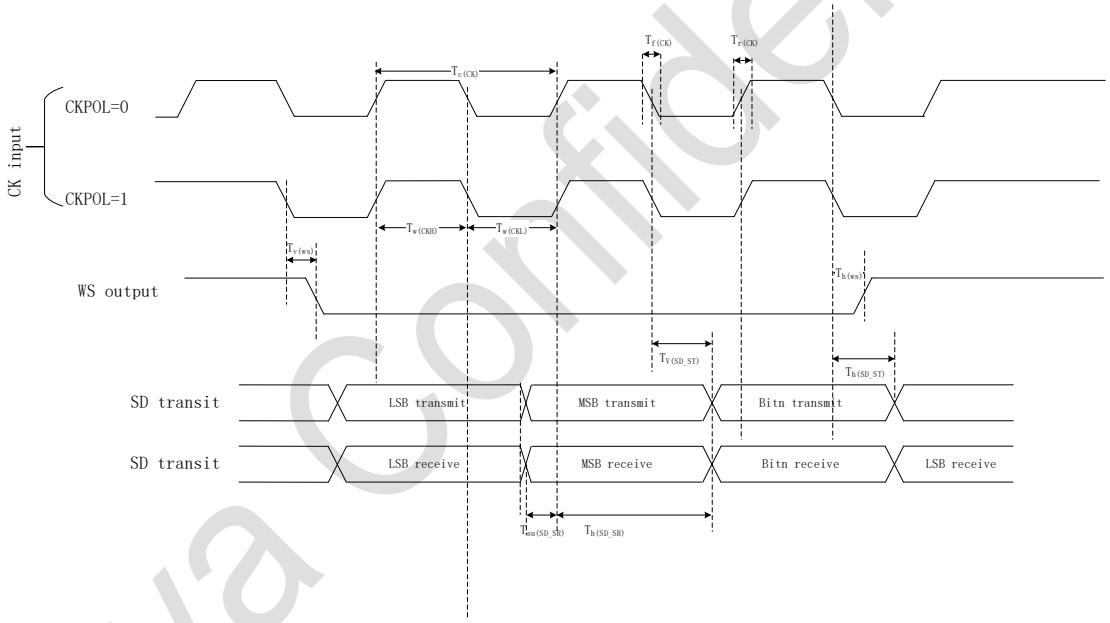


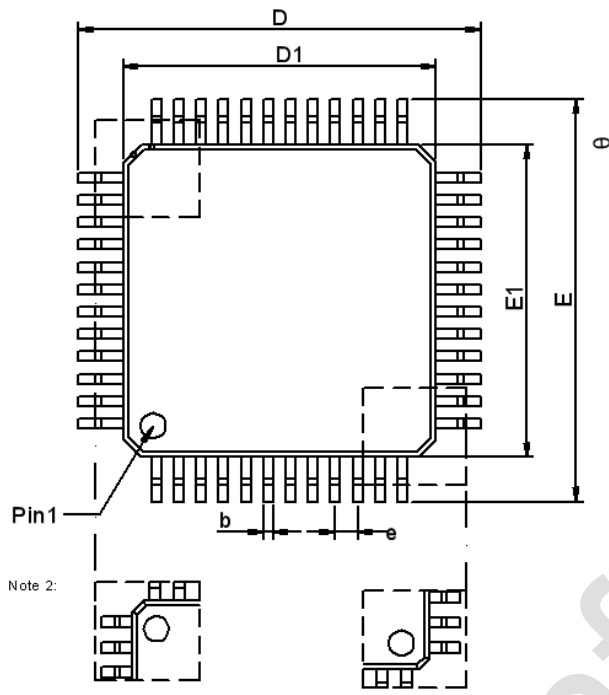
Figure 5-8 I²S timing diagram-Master mode(Philips protocol)

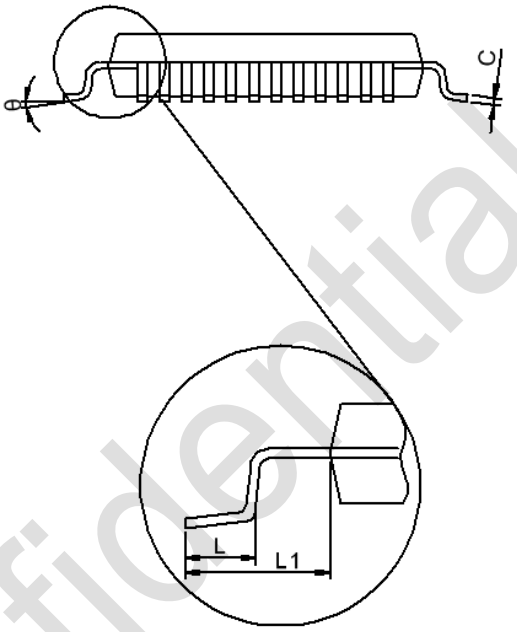
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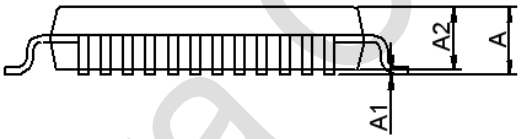
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6. Package information

6.1. LQFP48 package size







Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	8.800	9.000	9.200
D1	6.900	7.000	7.100
E	8.800	9.000	9.200
E1	6.900	7.000	7.100
e		0.500BSC	
L	0.450	-	0.750
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

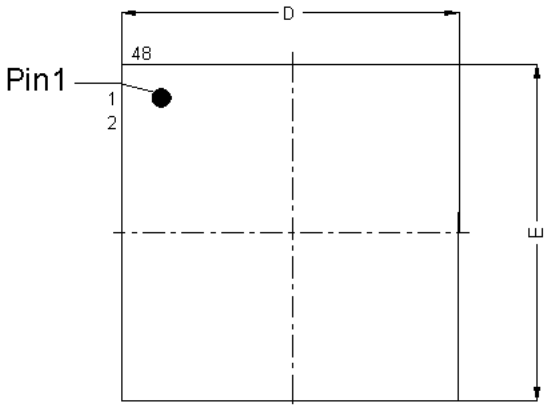
	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP48L 7x7X1.4-0.5PITCH	QRPD-0050	1.1

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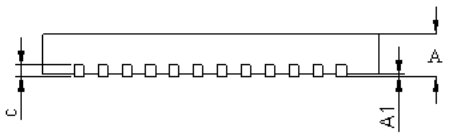
6.2. QFN48 (6*6) package size

TOP VIEW

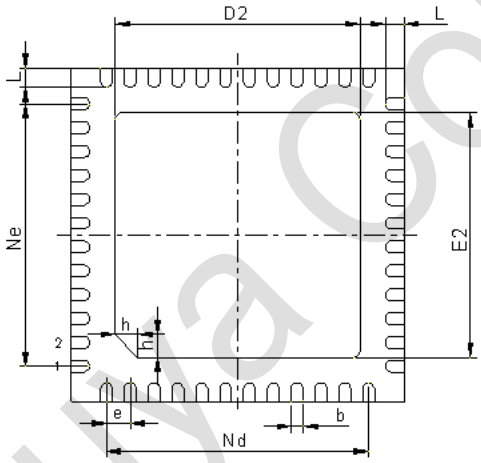


SIDE VIEW





BOTTOM VIEW



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c		0.200REF	
D	5.900	6.000	6.100
D2	4.100	4.300	4.500
E	5.900	6.000	6.100
E2	4.100	4.300	4.500
e		0.400BSC	
Nd		4.400BSC	
Ne		4.400BSC	
L	0.300	0.400	0.500
h	0.300	0.350	0.400

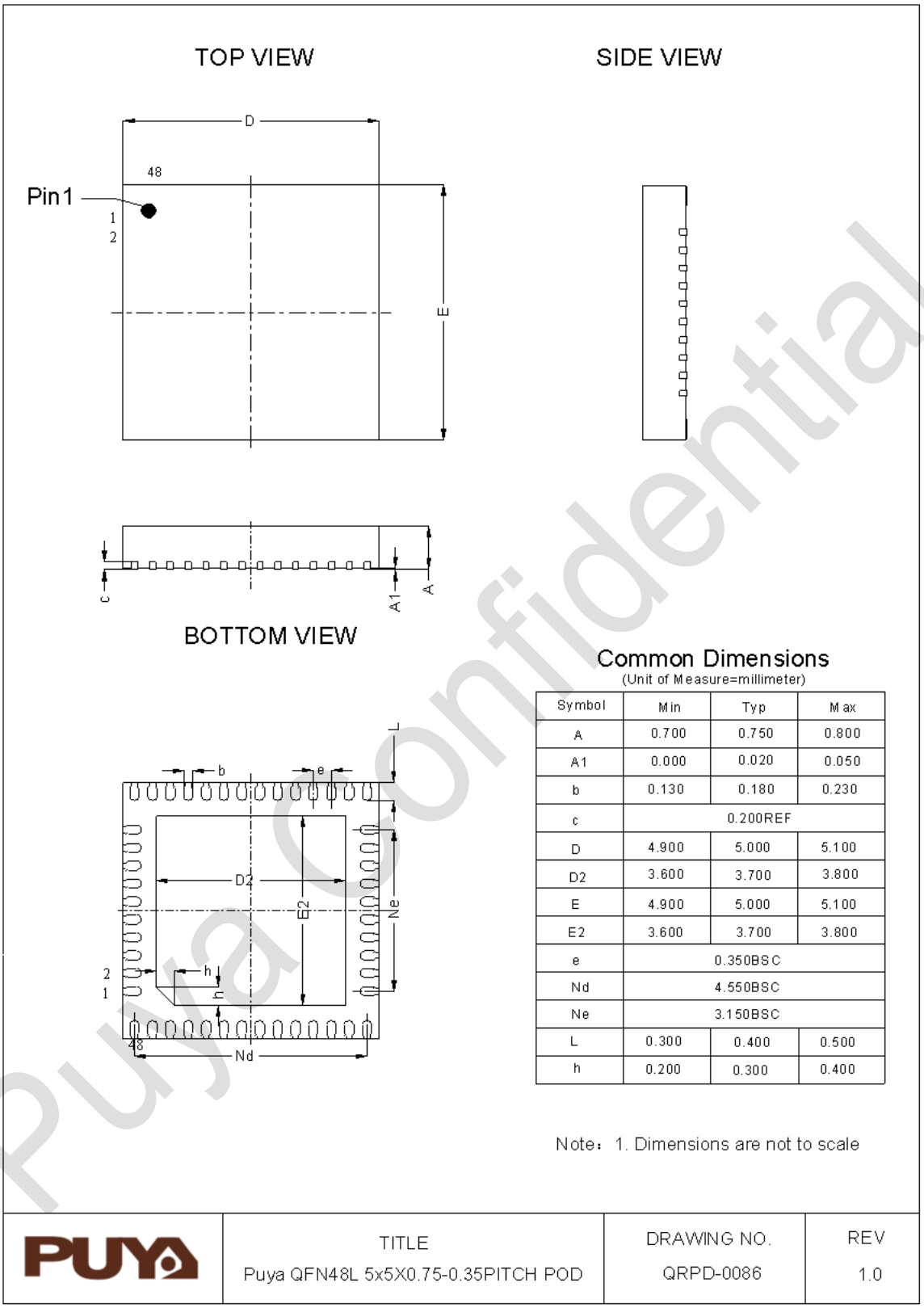
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN48L 6X6X0.75-0.4PITCH POD	QRPD-0056	1.1

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6.3. QFN48 (5*5) package size



Common Dimensions
(Unit of Measure=millimeter)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.130	0.180	0.230
c	0.200REF		
D	4.900	5.000	5.100
D2	3.600	3.700	3.800
E	4.900	5.000	5.100
E2	3.600	3.700	3.800
e	0.350BSC		
Nd	4.550BSC		
Ne	3.150BSC		
L	0.300	0.400	0.500
h	0.200	0.300	0.400

Note：1. Dimensions are not to scale

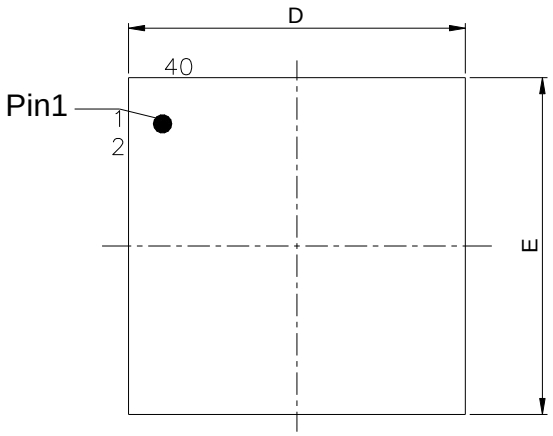
	TITLE	DRAWING NO.	REV
PUYA	Puya QFN48L 5x5X0.75-0.35PITCH POD	QRPD-0086	1.0

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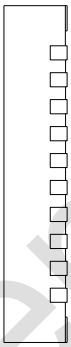
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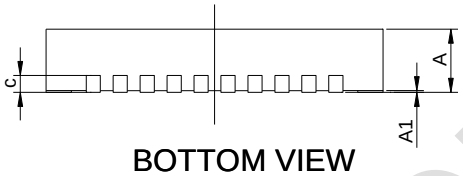
6.4. QFN40 package size

TOP VIEW

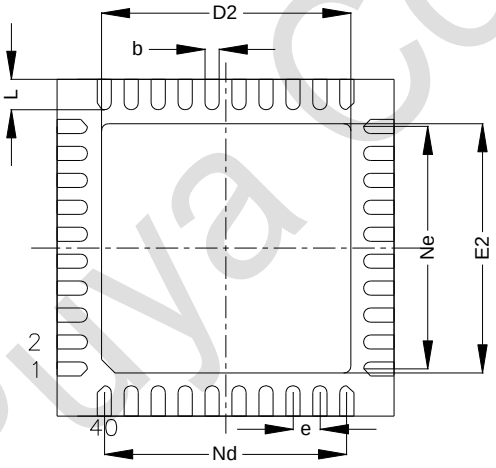


SIDE VIEW





BOTTOM VIEW



Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	-	0.020	0.050
b	0.150	0.200	0.250
c	0.200REF		
D	4.900	5.000	5.100
D2	3.600	3.700	3.800
E	4.900	5.000	5.100
E2	3.600	3.700	3.800
e	0.400BSC		
Nd	3.600BSC		
Ne	3.600BSC		
L	0.350	0.400	0.450

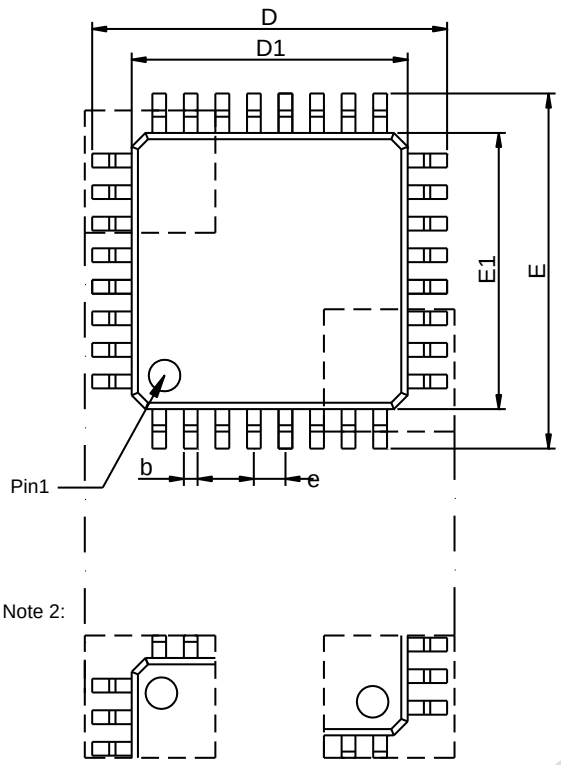
Note：1. Dimensions are not to scale

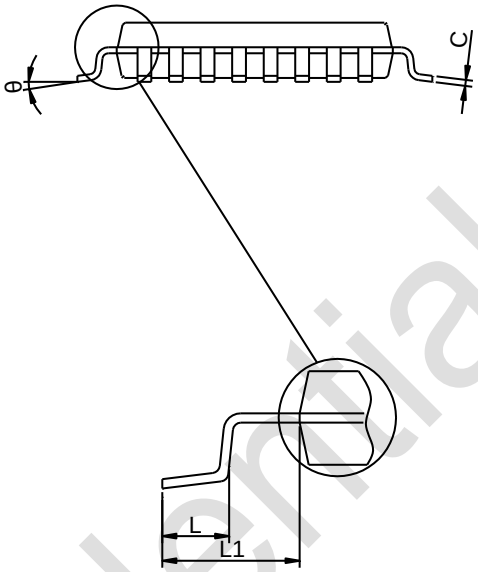
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PUYA	Puya QFN40L 5X5X0.75-0.4PITCH POD	QRPD-0075	1.1

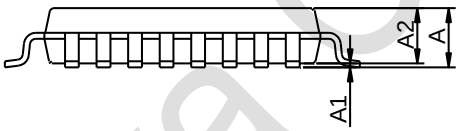
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6.5. LQFP32 package size







Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.300	-	0.450
c	0.100	-	0.200
D	8.800	9.000	9.200
D1	6.800	7.000	7.200
E	8.800	9.000	9.200
E1	6.800	7.000	7.200
e		0.800BSC	
L	0.450	-	0.750
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

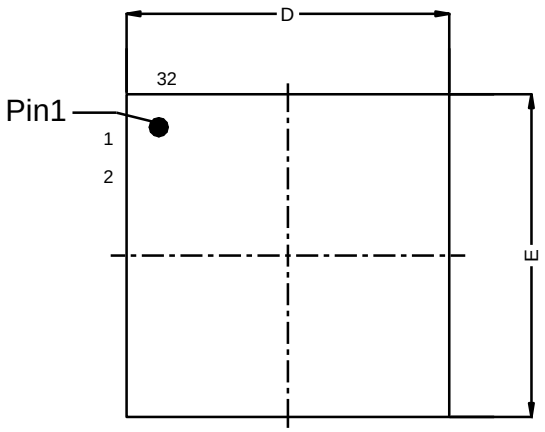
	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP32L 7x7X1.4-0.8PITCH	QRPD-0040	1.0

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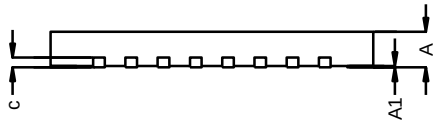
6.6. QFN32(5*5) package size

TOP VIEW

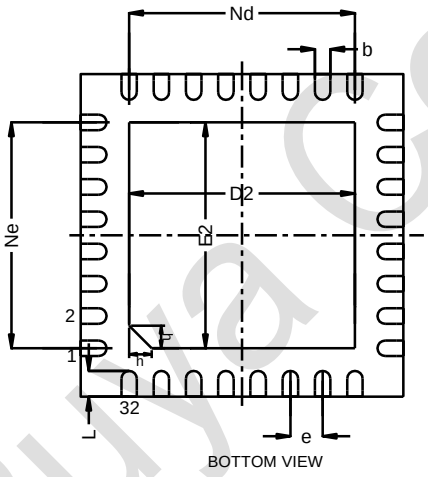


SIDE VIEW





BOTTOM VIEW



Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0	0.020	0.050
b	0.180	0.250	0.300
c		0.200REF	
D	4.900	5.000	5.100
D2	3.400	3.500	3.600
E	4.900	5.000	5.100
E1	3.400	3.500	3.600
e		0.500BSC	
Nd		3.500BSC	
L	0.350	0.400	0.450
h	0.300	0.350	0.400

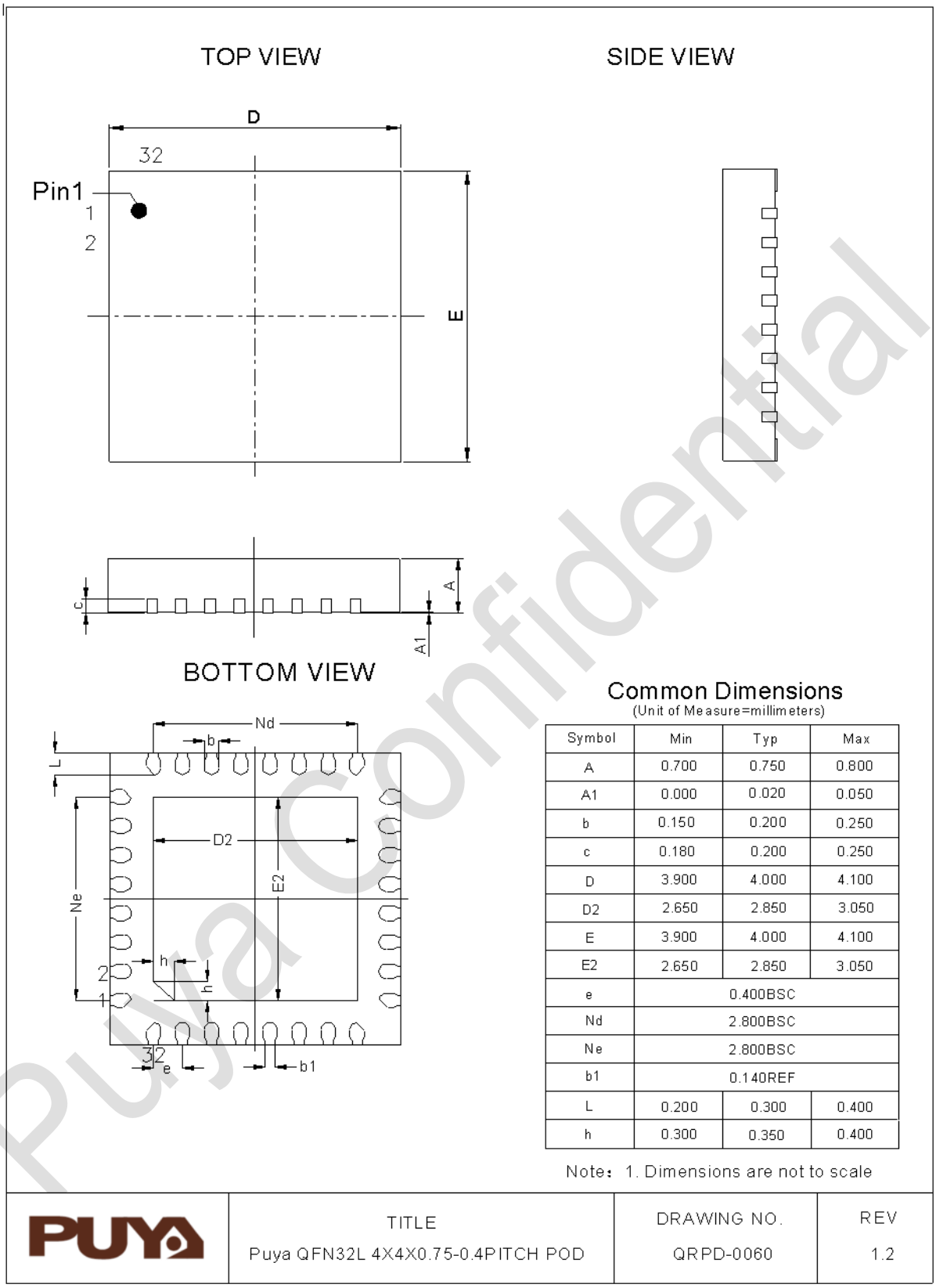
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN32L 5x5X0.75-0.5PITCH POD	QRPD-0042	1.0

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6.7. QFN32(4*4) package size



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.650	2.850	3.050
E	3.900	4.000	4.100
E2	2.650	2.850	3.050
e	0.400BSC		
Nd	2.800BSC		
Ne	2.800BSC		
b1	0.140REF		
L	0.200	0.300	0.400
h	0.300	0.350	0.400

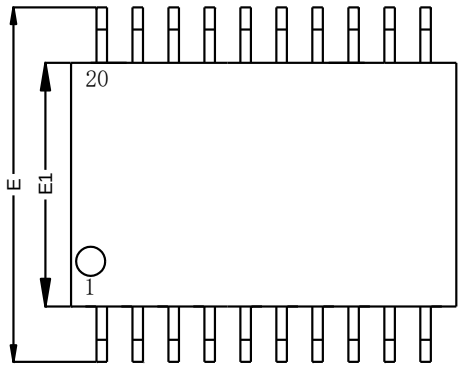
Note：1. Dimensions are not to scale

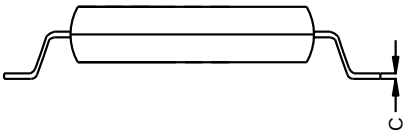
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PUYA	Puya QFN32L 4X4X0.75-0.4PITCH POD	QRPD-0060	1.2

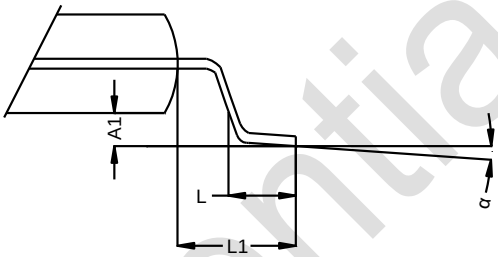
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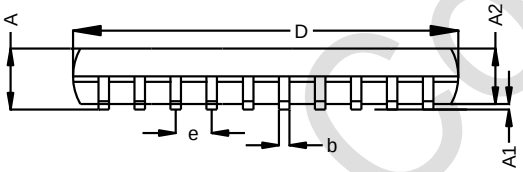
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6.8. TSSOP20 package size









Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
b	0.200	-	0.280
c	0.090	-	0.200
D	6.400	6.500	6.600
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	0.650BSC		
L	0.450	0.600	0.750
L1	1.000REF		
θ	0	-	8°

Note：1. Dimensions are not to scale

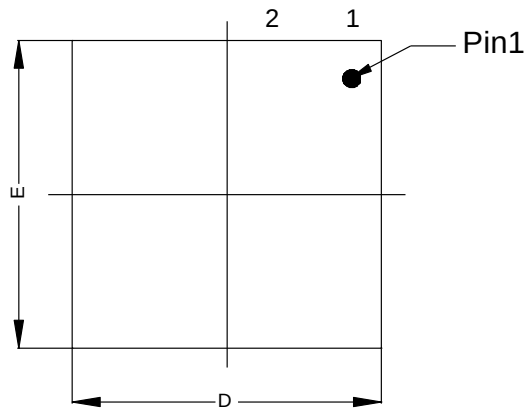
PUYA	TITLE Puya TSSOP20 POD	DRAWING NO. QRPD-0043	REV 1.0

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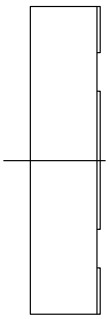
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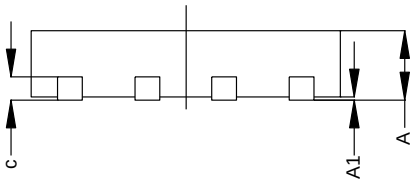
6.9. DFN8(2*2*0.45) package size

TOP VIEW

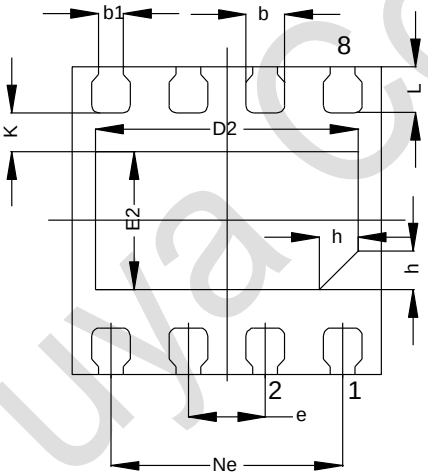


SIDE VIEW





BOTTOM VIEW



Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.400	0.450	0.500
A1	0.000	0.020	0.050
b	0.200	0.250	0.300
b1	0.110	0.160	0.210
c	0.100	0.150	0.200
D	1.900	2.000	2.100
D2	1.600	1.700	1.800
e	0.500BSC		
Ne	1.500BSC		
E	1.900	2.000	2.100
E2	0.800	0.900	1.000
L	0.250	0.300	0.350
h	0.200	0.250	0.300
K	0.200	0.250	0.300

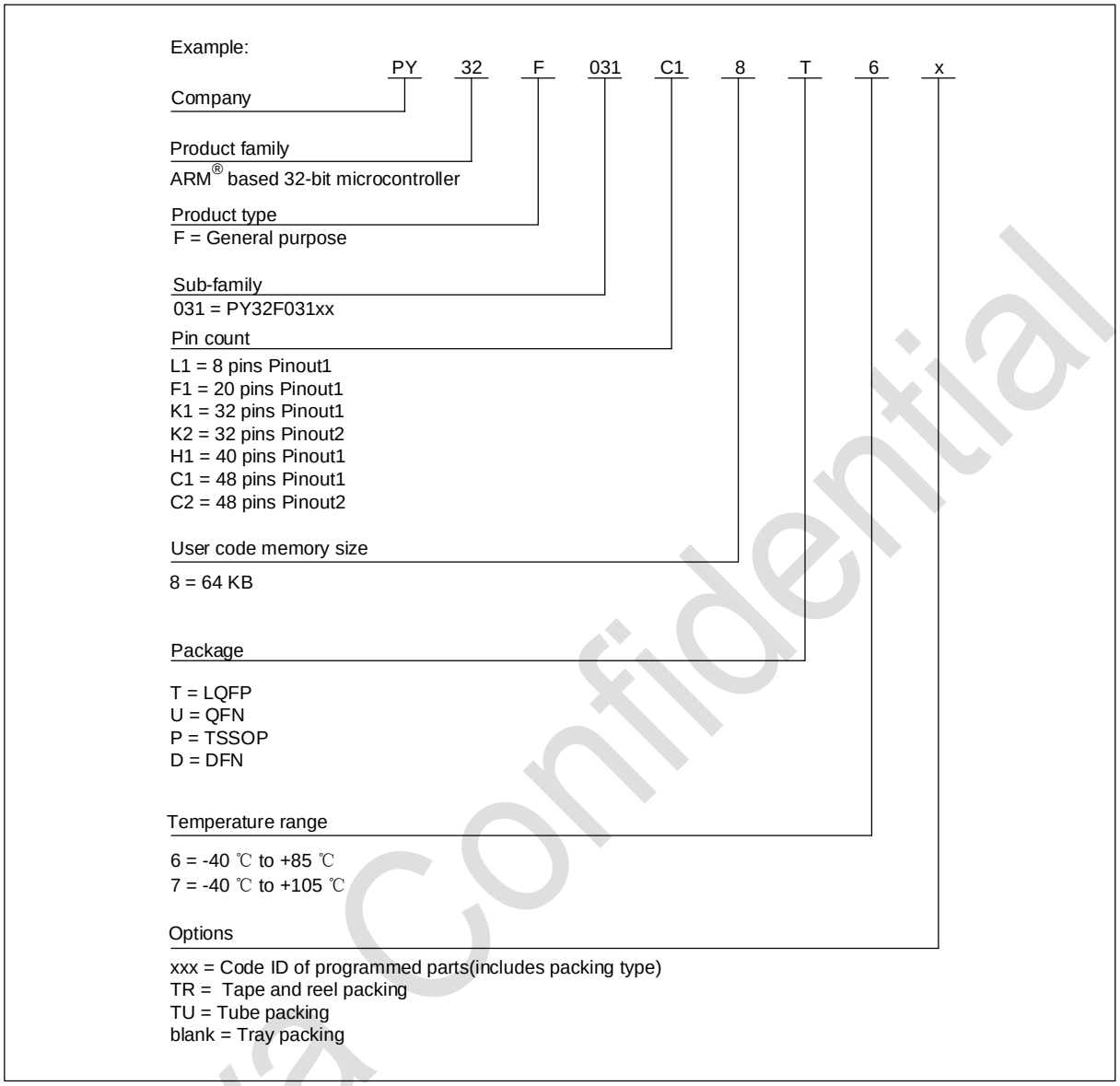
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya DFN8L 2X2X0.45-0.5PITCH POD	QRPD-0083	1.0

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7. Ordering information



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8. Version history

Version	Date	Descriptions
V1.0	2026.02.09	Initial version

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