PY32F002B Datasheet

32-bit ARM® Cortex®-M0+ Microcontroller

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Features

- Core
  - — 32-bit ARM® Cortex®-M0+ CPU
  - — Frequency up to 24 MHz
- Memories
  - — Up to 24 KB Flash memory
  - — Up to 3 KB SRAM
- Clock management
  - — 24 MHz High-speed internal RC oscillator (HSI)
  - — 32.768 kHz Low-speed internal RC oscillator (LSI)
  - — 32.768 kHz Low-speed external crystal oscillator (LSE)
  - — External clock input
- Power management and reset
  - — Operating voltage: 1.7 to 5.5 V
  - — Low power modes: Sleep/Stop
  - — Power-on/power-down reset (POR/PDR)
  - — Brown-out reset (BOR)
- General-purpose input and output (I/O)
  - — Up to 18 I/Os, all available as external interrupts
- 1 x 12-bit ADC
  - — Up to 8 external channels and 2 internal channels
  - — Voltage reference options: embedded 1.5 V/2.048 V/2.5 V and V_{CC}
- Timers
  - — 1 x 16-bit advanced-control timer (TIM1)
  - — 1 x 16-bit general-purpose timer (TIM14)
  - — 1 x low power timer (LPTIM), supports wake-up from Stop mode
  - — 1 x independent watchdog timer (IWDG)
  - — 1 x SysTick timer
- Communication interfaces
  - — 1 x serial peripheral interface (SPI)
  - — 1 x universal synchronous/asynchronous transceiver (USART) with automatic baud rate detection
  - — 1 x I^2C interface, supporting Standard mode(100 kHz), Fast mode (400 kHz), 7-bit addressing mode
- Hardware CRC-32 module
- 2 x comparators
- Unique UID
- Serial wire debug (SWD)
- Operating temperature:-40 to 85 °C, -40 to 105 °C
- Packages: QFN20, TSSOP20, SOP20、QFN16,SOP16, SOP14,SOP8

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1. Introduction

The PY32F002B incorporates the high-performance 32-bit ARM® Cortex®-M0+ core operating at up to 24 MHz frequency,embedded memories with up to 24 KB Flash and 3 KB SRAM, available in multiple package options. The PY32F002B integrates I²C, SPI, USART and other communication peripherals, one 12-bit ADC, two 16-bit timers, and two comparators.

The PY32F002B operates in the -40 to 85 °C or -40 to 105 °C temperature ranges from a 1.7 to 5.5 V power supply. The PY32F002B provides Sleep/Stop low-power operating modes for different low-power applications.

These features make the PY32F002B suitable for a wide range of applications such as controllers, portable devices, PC peripherals, gaming and GPS platforms, as well as industrial applications.

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Table 1-1 PY32F002Bx6 Series Product Planning and Features

Peripherals		PY32F002BF15U6	PY32F002BF15P6	PY32F002BW15S6	PY32F002BD15S6
Flash (KB)		24			
SRAM (KB)		3			
Timers	Advanced	1 (16-bit)			
	General purpose	1 (16-bit)			
	Low-power	1			
	SysTick	1			
	Watchdog	1			
Comm. interfaces	SPI	1			
	I^2C	1			
	USART	1			
GPIOs		18	18	14	12
12-bit ADC (external+internal)		8+2	8+2	7+2	7+2
Comparators		2			
Max. CPU frequency		24 MHz			
Operating Temperature		-40 ~ 85 °C			
Operating Voltage		1.7 ~ 5.5 V			
Package		QFN20	TSSOP20	SOP16	SOP14

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Table 1-2 PY32F002Bx7 Series Product Planning and Features

Peripherals		PY32F002BF15U7	PY32F002BF15P7	PY32F002BF15S7	PY32F002BW15U7	PY32F002BW15S7	PY32F002BD15S7	PY32F002BL15S7
Flash (Kbyte)		24	24	24	24	24	24	24
SRAM (Kbyte)		3	3	3	3	3	3	3
Timers	Advanced	1 (16-bit)						
	General purpose	1 (16-bit)						
	Low-power	1						
	SysTick	1						
	Watchdog	1						
Comm. interfaces	SPI	1						
	I^2C	1						
	USART	1						
GPIOs		18	18	18	14	14	12	6
12-bit ADC (external+internal)		8+2	8+2	8+2	8+2	7+2	7+2	6+2
Comparators		2	2	2	2	2	2	1
Max. CPU frequency		24 MHz						
Operating temperature		-40 ~ 105 °C						
Operating voltage		1.7 ~ 5.5 V						
Package		QFN20	TSSOP20	SOP20	QFN16	SOP16	SOP14	SOP8

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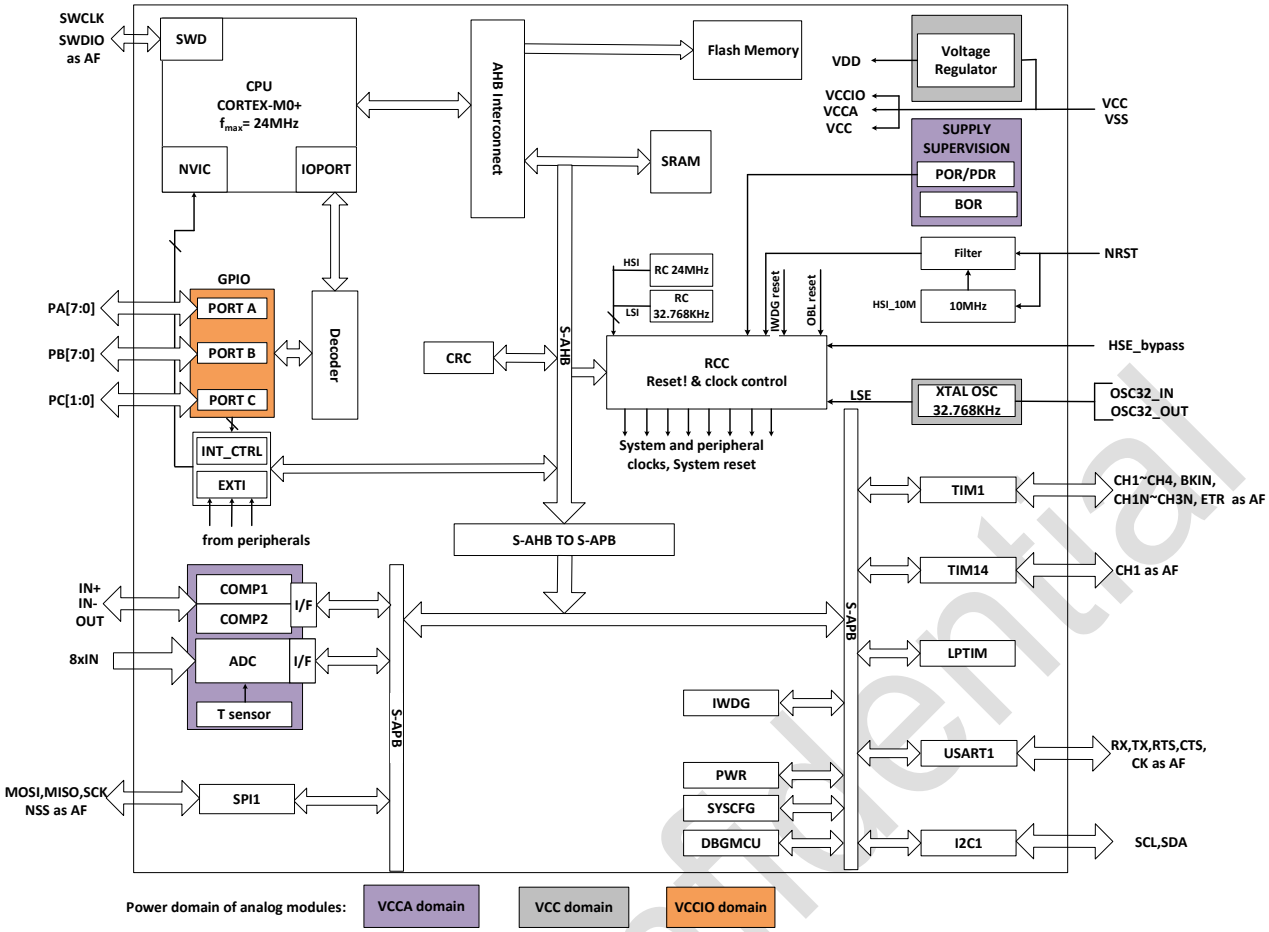


Figure 1-1 System block diagram

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2. Functional overview

2.1. Arm® Cortex®-M0+ core

The Arm® Cortex®-M0+ is an Arm 32-bit Cortex processor designed for embedded applications. It provides developers with significant benefits, including:

- Simple architecture for easy learning and programming
- Ultra-low power consumption for energy-efficient operation
- Reduced code density

The Arm® Cortex®-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. It delivers high performance through a streamlined instruction set and hardware enhancements like a single-cycle multiplier. Outperforms 8/16-bit MCUs in code efficiency.

The Arm® Cortex®-M0+ is tightly coupled with a Nested Vectored Interrupt Controller (NVIC).

2.2. Memories

Embedded SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits).

The Flash memory is composed of two distinct physical areas:

- 24 KB of Main flash area for user programs and data. In addition, a maximum of 4 KB Load flash can be set as a user boot loader according to customer configuration.
- 768 Bytes of Information area:
  - Option bytes
  - UID bytes
  - Factory config bytes
  - USER OTP memory

The protection of Main flash area includes the following mechanisms:

- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 4 KB.
- Option byte write protection is a special design for unlock.
- SDK (Software design kit) protection is used to protect the access of specific program areas.

2.3. Boot modes

At startup, the nBOOT0 pin and nBOOT1 (stored in option bytes) are used to select one of the three boot options in the following table:

Table 2-1 Boot configuration

Boot mode configuration		Mode	
nBOOT1 bit	**nBOOT0 bit**	**Boot memory size == 0**	**Boot memory size ! = 0**
X	0	Boot from Main flash	Boot from Main flash
0	1	Boot from SRAM	Boot from SRAM
1	1	N/A	Boot from Load flash

2.4. Clock management

System clock selection is performed on startup, however the internal RC 24 MHz oscillator is selected as default CPU clock on reset. After the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- A 24 MHz configurable internal high precision HSI clock
- A 32.768 kHz configurable LSI clock
- A 32.768 kHz LSE clock.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The maximum frequency of the AHB and the APB domains is 24 MHz.

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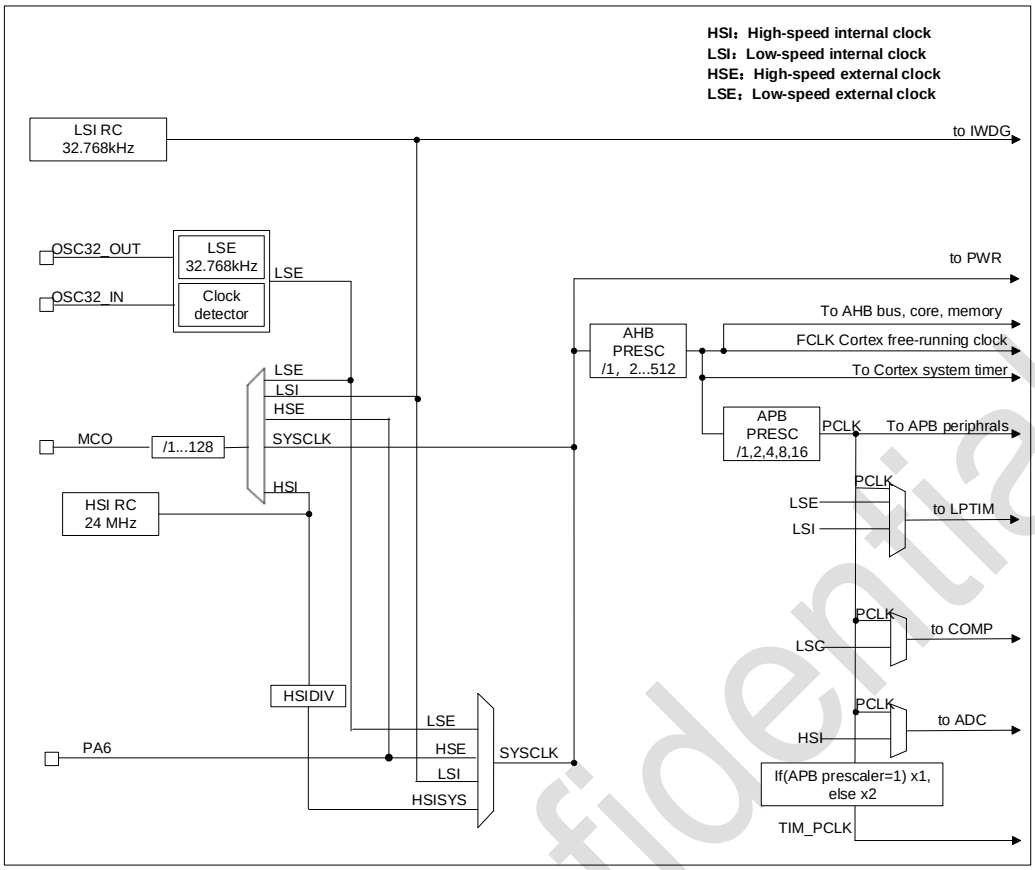


Figure 2-1 System clock structure diagram

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2.5. Power management

2.5.1. Power block diagram

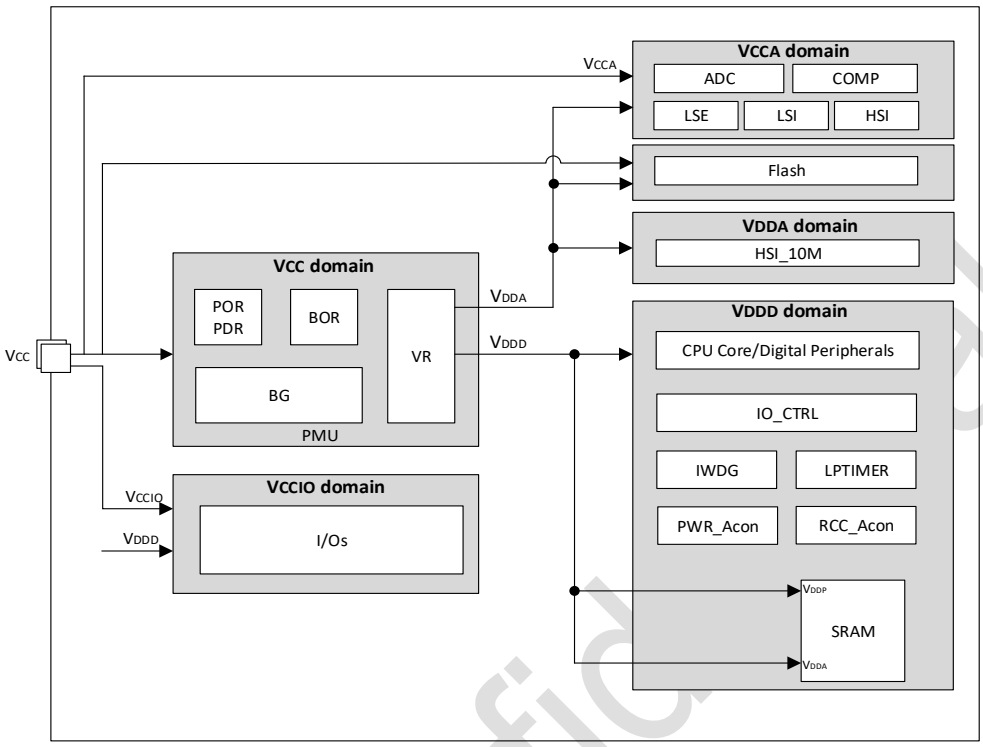


Figure 2-2 Power block diagram

Table 2-2 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	1.7 to 5.5 V	The power is supplied to the chip through the power pins, with the power supply module comprising: Partial analog circuits
2	V_{CCA}	1.7 to 5.5 V	Powers for most analog modules, sourced from the V_{CC} PAD (a dedicated power PAD can also be designed separately).
3	V_{CCIO}	1.7 to 5.5 V	Power to IO from V_{CC} PAD

2.5.2. Power monitoring

2.5.2.1. Power on reset/power-down reset (POR/PDR)

The Power-on reset (POR) and Power-down reset (PDR) module is designed in the chip to provide power-on and power-down reset for the chip. The module keeps working in all modes.

2.5.2.2. Brown-out reset (BOR)

In addition to POR/ PDR, BOR (Brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte.

When the BOR is turned on, the BOR threshold can be selected by the option byte and both the rising and falling detection points can be individually configured.

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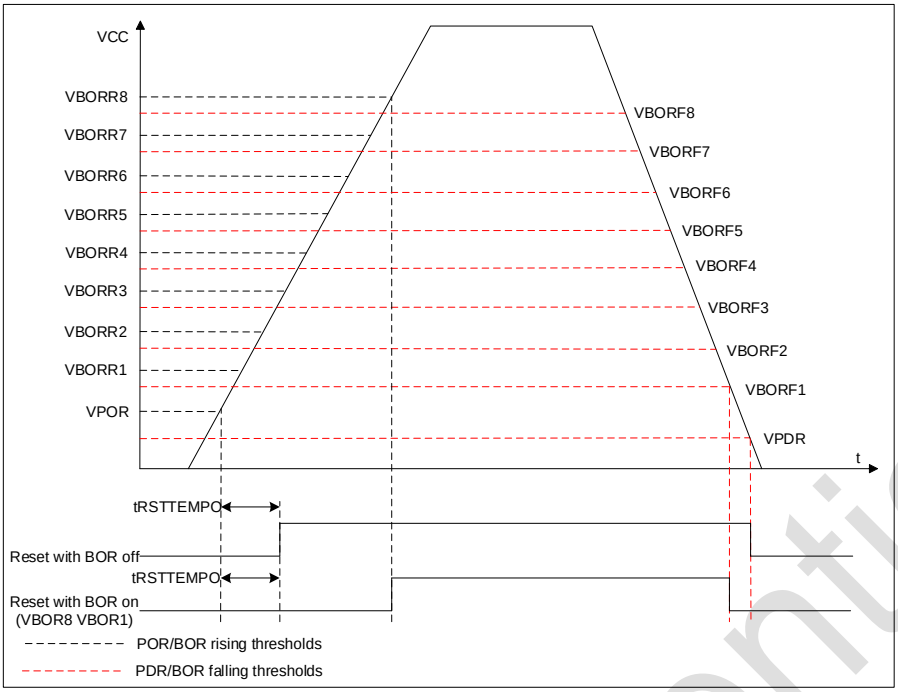


Figure2-3 POR/PDR/BOR threshold

2.5.3. Voltage regulator

The regulator has two operating modes:

- MR (Main regulator) is used in normal operating mode (Run).
- LPR (Low power regulator) provides an option for even lower power consumption in Stop mode.

2.5.4. Low-power mode

In addition to the normal operating mode, the chip has two low-power modes:

- **Sleep** mode: Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works.
- **Stop** mode: the contents of SRAM and registers are maintained and HSI is turned off. GPIO, IWDG, nRST and LPTIM can wake up Stop mode.

2.6. Reset

Two resets are designed in the chip: power reset and system reset.

2.6.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out reset (BOR)

2.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load (OBL) reset
- Power Reset (POR/PDR, BOR)

2.7. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating,pull-up/down,analog) or as peripheral alternate function. The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

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2.8. Interrupts and events

The PY32F002B handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.8.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Support 1 NMI
- Support 13 maskable external interrupts
- Support 6 Cortex-M0+ exceptions
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.8.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from Stop mode.

The EXTI controller has multiple channels, including up to 18 GPIOs can be connected to the 8 EXTI lines, 2 COMP outputs, and a LPTIM wake-up signals. GPIO and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 7 channel through the select signal.

- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.9. Analog-to-digital converter (ADC)

The PY32F002B has a 12-bit SARADC. The module has a total of up to 10 channels to be measured, including 8 external channels and 2 internal channels. The ADC internal voltage reference: V_{REFBUF} (1.5 V, 2.048 V, 2.5 V) or the power supply voltage V_{CC}.

The internal channels are:T_{S_VIN}, V_{REFINT}.

- A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.
- The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.
- An efficient low-power mode is implemented to allow very low consumption at low frequency.
- Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers.

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2.10. Comparators (COMP)

General purpose comparators are integrated in the chip, which can be used in combination with Timers. Comparators can be used as:

- Triggered by analog signal to wake-up function from low-power mode
- Analog signal conditioning
- Cycle by cycle current control loop when comparators are connected with PWM output from timer.

2.10.1. COMP main features

- Each comparator has configurable positive or negative input for flexible voltage selection
  - Multiple I/O pins
  - Power supply V_{CC} and 15 submultiple values provided by voltage divider (1/16, 2/16... 15/16)
  - The internal reference buffer (1.5 V, 2.048 V, 2.5 V) and 15 submultiple values (1/16, 2/16... 15/16) provided by voltage divider
- The output can be triggered by a connection to the I/O or timer input
  - OCREF_CLR event (cycle by cycle current control)
  - Brakes for fast PWM shutdown

2.11. Timers

The different timers feature as blow:

Table 2-3 Timer characteristics

Timer type	Timers	Counter resolution	Counter type	Prescaler	Capture/compare channels	Complementary outputs
Advanced-control	TIM1	16-bit	up,down, up/down	1 to 65536	4	3
General-purpose	TIM14	16-bit	up	1 to 65536	1	-

2.11.1. Advanced-control timer (TIM1)

The advanced-control timer (TIM1) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0 to 100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the Timer Link feature for synchronization or event chaining.

2.11.2. General-purpose timer(TIM14)

- The general-purpose timer TIM14 is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- The counter can be frozen in debug mode.

2.11.3. Low power timer

- LPTIM is a 16 -bit upcounter with a 3-bit prescaler and support a single count.
- LPTIM can be configured as a Stop mode wake-up source.
- The counter can be frozen in debug mode.

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2.11.4. IWDG

Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

- The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.
- IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.
- Controlling of option byte can enable IWDG hardware mode.
- IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.
- The counter can be frozen in debug mode.

2.11.5. SysTick timer

SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.12. Inter-integrated circuit interface (I^2C)

The I^2C (Inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I^2C bus. It provides multimaster capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm) and Fast-mode (Fm) .

I^2C features:

- Multimaster capability: can be master or slave
- Support different communication speeds
  - Standard mode (Sm): up to 100 kHz
  - Fast mode (Fm): up to 400 kHz
- As master
  - Generate clock
  - Generation of start and stop
- As Slave
  - Programmable I^2C address detection
  - Discovery of the STOP bit
- 7-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I^2C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching
- Software reset
- Analog noise filter function

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2.13. Universal synchronous/asynchronous receiver transmitter (USART)

The USART provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate shared by transmit and receive, up to 3 Mbit/s(8 times oversampling)
- Automatic baud rate detection
- Programmable data length of 8 or 9 bits
- Configurable STOP bits (1 or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Transfer detection flag
  - Receive buffer full
  - Send empty buffer
  - End of transmission flags
- Parity control
  - Transmit parity bit
  - Check the received data byte
- Flagged interrupt sources
  - CTS change
  - Transmit data register empty
  - Transmission complete
  - — Receive full data register
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Detection error
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

2.14. Serial peripheral interface (SPI)

The SPI allow the chip to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)

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- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- 8 master mode baud rate prescale factors (max 12 MHz)
- Slave mode frequency (max 3 MHz)
- Both master and Slave modes can be managed by software or hardware NSS: dynamic change of master/slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Interrupt-causing Master mode faults or overloads
- 2 x 32-bit Rx and Tx FIFOs

2.15. SWD

An ARM SWD interface allows serial debugging tools to be connected to the PY32F002B.

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3. Pinouts and pin descriptions

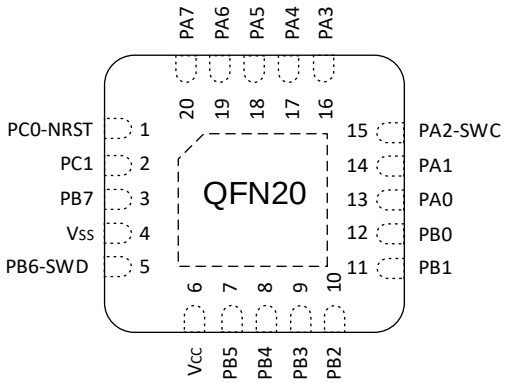


Figure 3-1 QFN20 Pinout1 PY32F002BF15Ux(Top view)

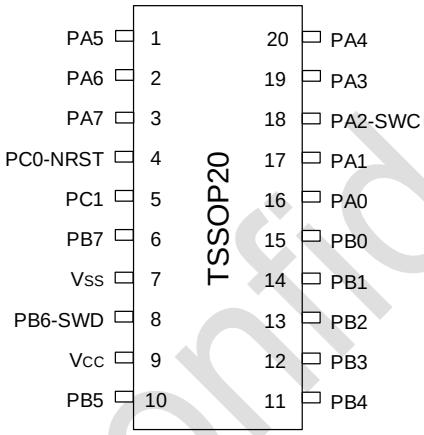


Figure 3-2 TSSOP20 Pinout1 PY32F002BF15Px(Top view)

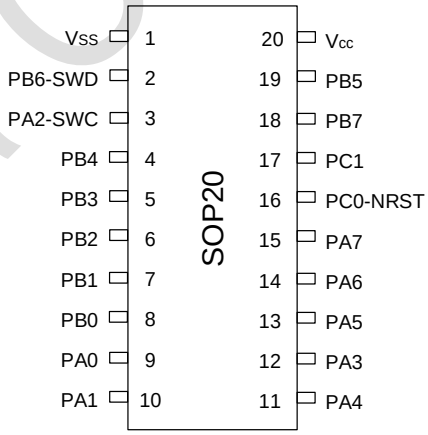


Figure 3-3 SOP20 Pinout1 PY32F002BF15Sx(Top view)

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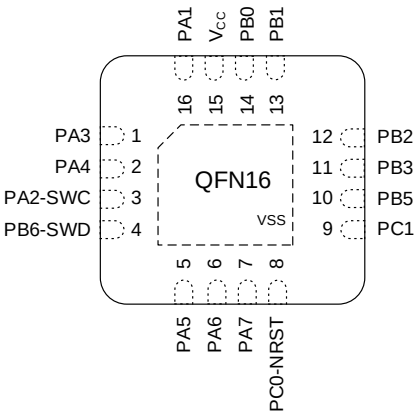


Figure 3-4 QFN16 Pinout1 PY32F002BW15Ux(Top view)

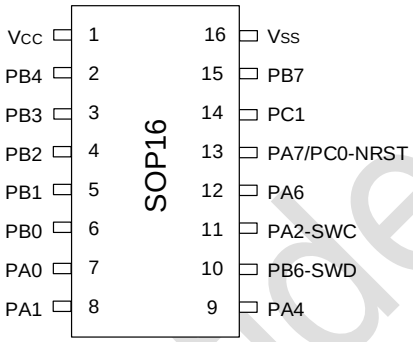


Figure 3-5 SOP16 Pinout1 PY32F002BW15Sx(Top view)

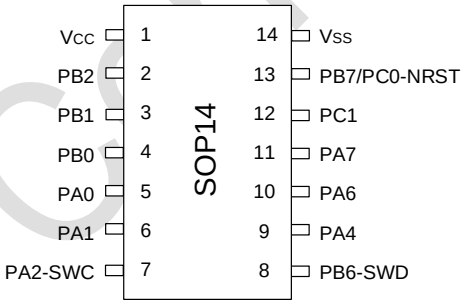


Figure 3-6 SOP14 Pinout1 PY32F002BD15Sx(Top view)



Figure 3-7 SOP8 Pinout1 PY32F002BL15Sx(Top view)

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Table 3 -1 Legend/abbreviations used in the pinout table

Timer type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I/O	Input / output pin
		NC	No internal connection
I/O structure		COM	Standard 5 V I/O, with Analog switch function supplied by V_{CC}
		NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		-	Unless otherwise specified, all ports are used as analog inputs be- tween and after reset
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers

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Table 3-2 QFN20/TSSOP20/SOP20 pin definition

Package type			Reset	Port type	Port structure	Port function	
QFN20 F1	TSSOP20 F1	SOP20 F1				Multiplexing function	Additional features
18	1	13	PA5	**I/O**	COM	USART_CK TIM1_CH1 TIM14_CH1	
19	2	14	PA6	I/O	COM	SPI_NSS USART_TX EVENTOUT	ADC_IN3 External_clock_in
20	3	15	PA7	I/O	COM	SPI_MOSI USART_TX USART_RX TIM1_CH4 MCO	ADC_IN4
1	4	16	PC0-NRST(1)(3)	I/O	NRST	SWDIO TIM1_CH1N EVENTOUT	NRST ADC_IN5
2	5	17	PC1	I/O	COM	SPI_MISO	OSC32IN
3	6	18	PB7	I/O	COM	SPI_MOSI TIM14_CH1	OSC32OUT
4	7	1	V_{SS}	S		Ground	
5	8	2	PB6(SWDIO)(2)	I/O	COM	SPI_MISO USART_TX I^2C_SDA SWDIO	ADC_IN6
6	9	20	V_{CC}	S		Digital power supply	
7	10	19	PB5	I/O	COM	SPI_NSS USART_RX TIM1_CH3 TIM14_CH1	
8	11	4	PB4	I/O	COM	USART_TX I^2C_SDA TIM1_BKIN	
9	12	5	PB3	I/O	COM	USART_CK I^2C_SCL TIM1_ETR CMP1_OUT	
10	13	6	PB2	I/O	COM	SPI_SCK USART_CTS	

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Package type			Reset	Port type	Port structure	Port function	
QFN20 F1	TSSOP20 F1	SOP20 F1				Multiplexing function	Additional features
						TIM1_CH1N	
						TIM1_CH3	
11	14	7	PB1	I/O	COM	USART_RTS	ADC_IN0 CMP1_INP CMP1_INM
						TIM1_CH2N	
						TIM1_CH4	
						MCO	
12	15	8	PB0	I/O	COM	SPI_SCK	ADC_IN7 CMP1_INM
						USART_CK	
						TIM1_CH2	
						TIM1_CH3N	
13	16	9	PA0	I/O	COM	SPI_MOSI	
						TIM1_CH1	
14	17	10	PA1	I/O	COM	SPI_MISO	
						TIM1_CH2	
15	18	3	PA2(SWCLK)[2][3]	I/O	COM	USART_RX	
						I^2C_SCL	
						SWCLK	
						TIM1_CH4	
						CMP2_OUT	
16	19	12	PA3	I/O	COM	USART_TX	ADC_IN1 CMP2_INP CMP2_INM
						TIM1_CH2	
17	20	11	PA4	I/O	COM	USART_RX	ADC_IN2 CMP2_INM
						TIM1_CH3	
						TIM14_CH1	

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Table 3-3 QFN16/SOP16/SOP14/SOP8 pin definition

Package type				Reset	Port type	Port structure	Port function	
QFN16 W1	SOP16 W1	SOP14 D1	SOP8 L1				Multiplexing function	Additional features
6	12	10	6	PA6(4)	I/O	COM	SPI_NSS USART_TX EVENTOUT	ADC_IN3 External_clock_in
7	13	11	7	PA7(4)	I/O	COM	SPI_MOSI USART_TX USART_RX TIM1_CH4 MCO	ADC_IN4
8	13	13	6	PC0-NRST(1)(3)(4)	I/O	RST	SWDIO TIM1_CH1N EVENTOUT	NRST ADC_IN5
9	14	12	7	PC1(4)	I/O	COM	SPI_MISO	OSC32IN
-	15	13	-	PB7(4)	I/O	COM	SPI_MOSI TIM14_CH1	OSC32OUT
-	16	14	8	V_{SS}	S		Ground	
4	10	8	5	PB6(SWDIO)(2)	I/O	COM	SPI_MISO USART_TX I^2C_SDA SWDIO	ADC_IN6
15	1	1	1	V_{CC}	S		Digital power supply	
10	-	-	-	PB5	I/O	COM	SPI_NSS USART_RX TIM1_CH3 TIM14_CH1	
-	2	-	-	PB4	I/O	COM	USART_TX I^2C_SDA TIM1_BKIN	
11	3	-	-	PB3	I/O	COM	USART_CK I^2C_SCL TIM1_ETR CMP1_OUT	
12	4	2	-	PB2	I/O	COM	SPI_SCK USART_CTS TIM1_CH1N TIM1_CH3	
13	5	3	2	PB1	I/O	COM	USART_RTS	ADC_IN0

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Package type				Reset	Port type	Port structure	Port function	
QFN16 W1	SOP16 W1	SOP14 D1	SOP8 L1				Multiplexing function	Additional features
							TIM1_CH2N	CMP1_INM CMP1_INP
							TIM1_CH4	
							MCO	
14	6	4	3	PB0	I/O	COM	SPI_SCK	ADC_IN7 CMP1_INM
							USART_CK	
							TIM1_CH2	
							TIM1_CH3N	
-	7	5	-	PA0	I/O	COM	SPI_MOSI	
							TIM1_CH1	
16	8	6	-	PA1	I/O	COM	SPI_MISO	
							TIM1_CH2	
3	11	7	4	PA2(SWCLK)(2)(3)	I/O	COM	USART_RX	
							I^2C_SCL	
							SWCLK	
							TIM1_CH4	
							CMP2_OUT	
1	-	-	-	PA3	I/O	COM	USART_TX	ADC_IN1 CMP2_INP CMP2_INM
							TIM1_CH2	
2	9	9	-	PA4	I/O	COM	USART_RX	ADC_IN2 CMP2_INM
							TIM1_CH3	
							TIM14_CH1	
5	-	-	-	PA5	I/O	COM	USART_CK	
							TIM1_CH1	
							TIM14_CH1	

1. Selecting PC0 or NRST/SWDIO is configured through option bytes.
2. After reset (when option byte configures 0/0,0/1,1/0),the two pins of PB6 and PA2 are configured as SWDIO and SWCLK AF function, the former internal pull-up resistor, the latter pull-down resistor is activated.
3. After reset (when option byte configures 1/1),the two pins of PC0 and PA2 are configured as SWDIO and SWCLK AF function,the former internal pull-up resistor, the latter pull-down resistor is activated.
4. Both IO ports lead out on the same pin, only either IO port can be used at the same time, and the other IO must be configured in analog mode (MODEy[1:0] is 0B11).

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3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-4 Port A alternate functions mapping

PortA	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI_MOSI	-	TIM1_CH1	-	-	-	-	-
PA1	SPI_MISO	-	TIM1_CH2	-	-	-	-	-
PA2	SWC	USART_RX	TIM1_CH4	-	CMP2_OUT	-	I^2C_SCL	-
PA3	-	USART_TX	TIM1_CH2	-	-	-	-	-
PA4	-	USART_RX	TIM1_CH3	-	-	TIM14_CH1	-	-
PA5	-	USART_CK	TIM1_CH1	-	-	TIM14_CH1	-	-
PA6	SPI_NSS	USART_TX	-	-	-	-	-	EVENTOUT
PA7	SPI_MOSI	USART_TX	TIM1_CH4	USART_RX	MCO	-	-	-

3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3 -5 Port B alternate function mapping

PortB	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI_SCK	USART_CK	TIM1_CH2	TIM1_CH3N	-	-	-	-
PB1	-	USART_RTS	TIM1_CH2N	TIM1_CH4	MCO	-	-	-
PB2	SPI_SCK	USART_CTS	TIM1_CH1N	TIM1_CH3	-	-	-	-
PB3	-	USART_CK	TIM1_ETR	-	CMP1_OUT	-	I^2C_SCL	-
PB4	-	USART_TX	TIM1_BKIN	-	-	-	I^2C_SDA	-
PB5	SPI_NSS	USART_RX	TIM1_CH3	-	-	TIM14_CH1	-	-
PB6	SWD	USART_TX	SPI_MISO	-	-	-	I^2C_SDA	-
PB7	SPI_MOSI	-	-	-	-	TIM14_CH1	-	-

3.3. Alternate functions selected through GPIOC_AFR registers for port C

Table 3-6 Port C alternate function mapping

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	SWD	-	TIM1_CH1N	-	-	-	-	EVENTOUT
PC1	SPI_MISO	-	-	-	-	-	-	-

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4. Memory mapping

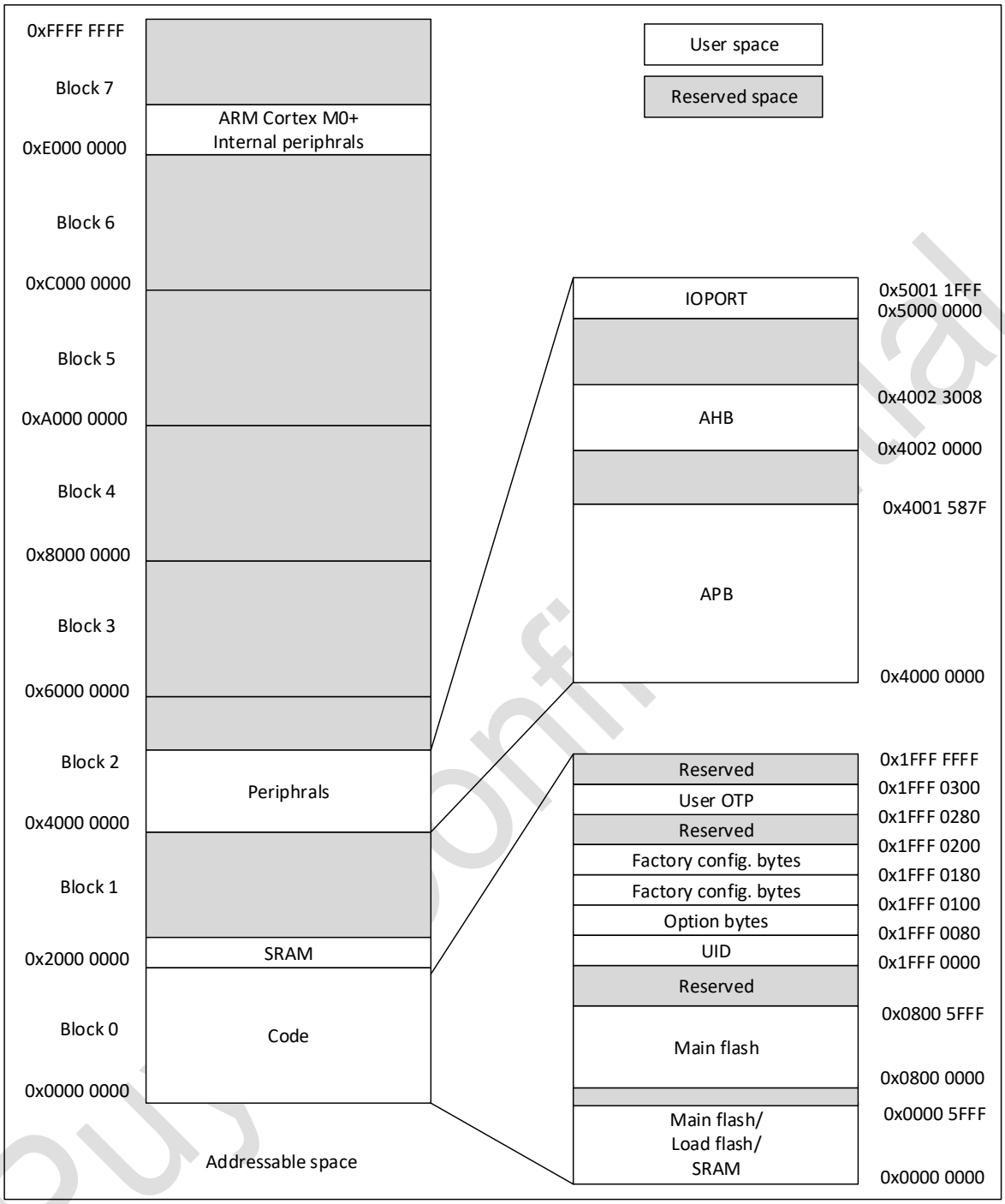


Figure 4-1 Memory mapping

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Table 4-1 Memory boundary address

Type	Boundary address	Size	Memory area	Descriptions
SRAM	0x2000 C000-0x3FFF FFFF	-	Reserved (1)	-
	0x2000 0000-0x2000 0BFF	3 KB	SRAM	-
Code	0x1FFF 0300-0x1FFF FFFF	-	Reserved	-
	0x1FFF 0280-0x1FFF 02FF	128 Bytes	USER OTP memory	Store user data
	0x1FFF 0180-0x1FFF 01FF	128 Bytes	Factory configuration bytes 1	Store trimming data (including HSI trimming) and power-on verification code reading
	0x1FFF 0100-0x1FFF 017F	128 Bytes	Factory configuration bytes 0	HSI trimming data, Flash erase/write time configuration parameters
	0x1FFF 0080-0x1FFF 00FF	128 Bytes	Option bytes	Option bytes information
	0x1FFF 0000-0x1FFF 007F	128 Bytes	UID	Unique ID
	0x0800 6000-0x1FFE FFFF	-	Reserved	-
	0x0800 0000-0x0800 5FFF	24 KB	Main flash	-
	0x0000 6000-0x07FF FFFF	-	Reserved	-
	0x0000 0000-0x0000 5FFF	24 KB	Based on Boot configuration: 1.Main flash 2.Load flash 3.SRAM	-

The address is marked as **Reserved**, which cannot be written, read as 0, and a response error is generated.

Table 4-2 Peripheral register address

Bus	Boundary address	Size	Peripherals
	0xE000 0000-0xE00F FFFF	-	M0+
IOPORT	0x5000 0C00-0x5FFF FFFF	-	Reserved
	0x5000 0800-0x5000 0BFF	1 KB	GPIOC
	0x5000 0400-0x5000 07FF	1 KB	GPIOB
	0x5000 0000-0x5000 03FF	1 KB	GPIOA
AHB	0x4002 3400-0x4FFF FFFF	-	Reserved
	0x4002 300C-0x4002 33FF	1 KB	Reserved
	0x4002 3000-0x4002 3008		CRC
	0x4002 2400-0x4002 2FFF	-	Reserved
	0x4002 2000-0x4002 23FF	1 KB	Flash
	0x4002 1C00-0x4002 1FFF	-	Reserved
	0x4002 1900-0x4002 1BFF	1 KB	Reserved
	0x4002 1800-0x4002 18FF		EXTI
	0x4002 1400-0x4002 17FF	-	Reserved
	0x4002 1080-0x4002 13FF	1 KB	Reserved
	0x4002 1000-0x4002 107F		RCC
	0x4002 0000-0x4002 0FFF	-	Reserved
APB	0x4001 5C00-0x4001 FFFF	-	Reserved
	0x4001 5880-0x4001 5BFF	1 KB	Reserved

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Bus	Boundary address	Size	Peripherals
	0x4001 5800-0x4001 587F		DBG
	0x4001 3C00-0x4001 57FF	-	Reserved
	0x4001 381C-0x4001 3BFF	1 KB	Reserved
	0x4001 3800-0x4001 3018		USART1
	0x4001 3400-0x4001 37FF	-	Reserved
	0x4001 3010-0x4001 33FF	1 KB	Reserved
	0x4001 3000-0x4001 300C		SPI1
	0x4001 2C50-0x4001 2FFF	1 KB	Reserved
	0x4001 2C00-0x4001 2C4C		TIM1
	0x4001 2800-0x4001 2BFF	-	Reserved
	0x4001 270C-0x4001 27FF	1 KB	Reserved
	0x4001 2400-0x4001 2708		ADC
	0x4001 0400-0x4001 23FF	-	Reserved
	0x4001 0220-0x4001 03FF	1 KB	Reserved
	0x4001 0200-0x4001 021F		COMP1/2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 8000-0x4000 FFFF	-	Reserved
	0x4000 7C28-0x4000 7FFF	1 KB	Reserved
	0x4000 7C00-0x4000 7C24		LPTIM
	0x4000 7400-0x4000 7BFF	-	Reserved
	0x4000 7018-0x4000 73FF	1 KB	Reserved
	0x4000 7000-0x4000 7014		PWR
	0x4000 5800-0x4000 6FFF	-	Reserved
	0x4000 5434-0x4000 57FF	1 KB	Reserved
	0x4000 5400-0x4000 5430		I^2C
	0x4000 3400-0x4000 53FF	-	Reserved
	0x4000 3014-0x4000 33FF	1 KB	Reserved
	0x4000 3000-0x4000 0010		IWDG
	0x4000 2400-0x4000 2FFF	-	Reserved
	0x4000 2054-0x4000 23FF	1 KB	Reserved
	0x4000 2000-0x4000 0050		TIM14
	0x4000 0000-0x4000 1FFF	-	Reserved

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5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A(max) (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation.

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A = 25 °C and V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95 % of the devices have an error less than or equal to the value indicated.

5.1.3. Power supply scheme

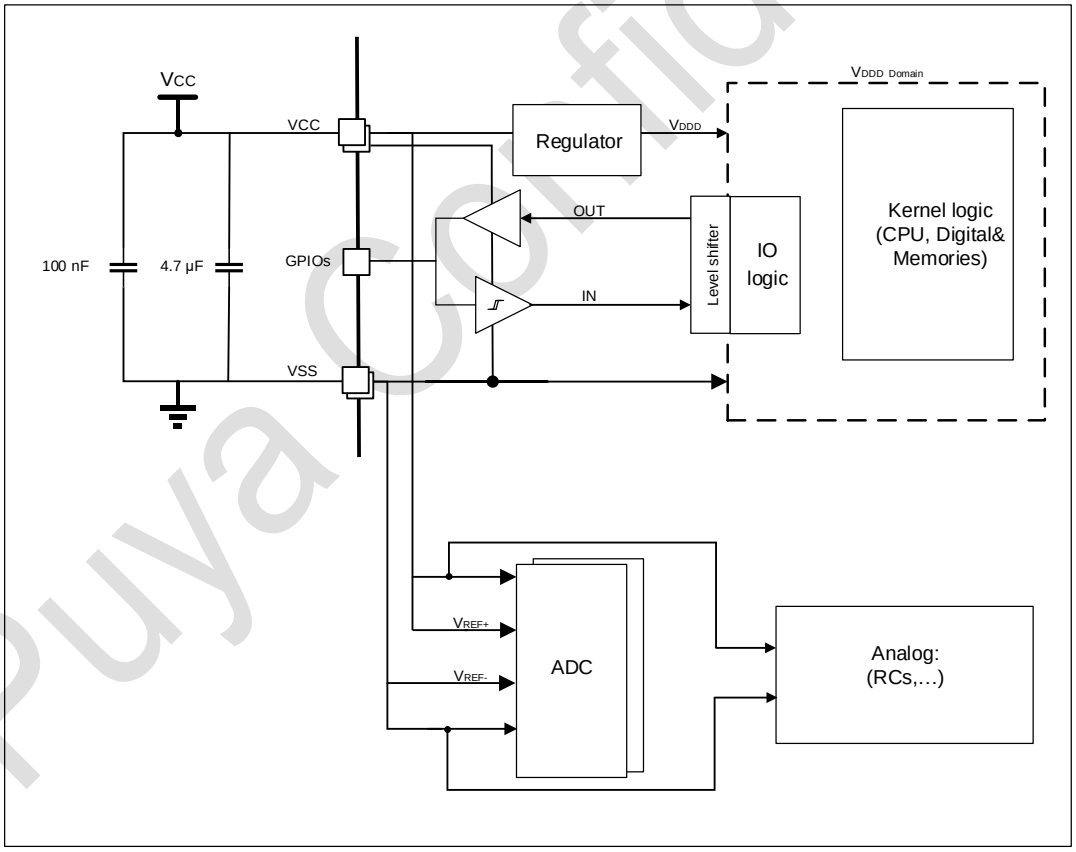


Figure 5 -1 Power supply scheme

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5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Descriptions	Min	Max	Unit
V_{CC}	External mains power supply	-0.3	6.25	V
V_{IN}	Input voltage of other pins	-0.3	V_{CC}+0.3	V

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.

Table 5-2 Current characteristics

Symbol	Descriptions	Max	Unit
ΣI_{VCC}	Total current into sum of all V_{CC} power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink) (1)	120	mA
$I_{IO(PIN)}$(2)	Output current sunk by any I/O and control pin	30	mA
	Output current source by any I/O and control pin	30	
$\Sigma I_{IO(PIN)}$(2)	Total output current sunk by sum of all I/Os and control pins	100	mA
	Total output current sourced by sum of all I/Os and control pins	100	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.

Table 5-3 Thermal characteristics

Symbol	Descriptions	Conditions	Value	Unit
T_{STG}	Storage temperature range	-	-65 to +150	°C
T_O	Operating temperature range	x6 version	-40 to +85	°C
		X7 version	-40 to +105	

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	24	MHz
f_{PCLK}	Internal APB clock frequency	-	0	24	MHz
V_{CC}	Standard operating voltage	-	1.7	5.5	V
V_{IN}	I/O input voltage	-	-0.3	V_{CC}+0.3	V
T_A	Ambient temperature	x6 version	-40	85	°C
		X7 version	-40	105	
T_J	Junction temperature	x6 version	-40	90	°C
		X7 version	-40	110	

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5.3.2. Operating conditions at power-on/power-down

Table 5-5 Operating conditions at power-on/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise rate	-	0	∞	μs/V
	V_{CC} fall rate	-	20	∞	

5.3.3. Embedded reset

Table 5-6 Embedded reset characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization	-	-	4.0	7.5	ms
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.5(2)	1.6	1.7	V
		Falling edge	1.45	1.55	1.65(2)	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	50	-	mV
V_{BOR}	BOR threshold	BOR_LEV[2:0]=000 (Rising edge)	1.7(2)	1.8	1.9	V
		BOR_LEV[2:0]=000 (Falling edge)	1.6	1.7	1.8(2)	
		BOR_LEV[2:0]=001 (Rising edge)	1.9(2)	2	2.1	
		BOR_LEV[2:0]=001 (Falling edge)	1.8	1.9	2(2)	
		BOR_LEV[2:0]=010 (Rising edge)	2.1(2)	2.2	2.3	
		BOR_LEV[2:0]=010 (Falling edge)	2	2.1	2.2(2)	
		BOR_LEV[2:0]=011 (Rising edge)	2.3(2)	2.4	2.5	
		BOR_LEV[2:0]=011 (Falling edge)	2.2	2.3	2.4(2)	
		BOR_LEV[2:0]=100 (Rising edge)	2.5(2)	2.6	2.7	
		BOR_LEV[2:0]=100 (Falling edge)	2.4	2.5	2.6(2)	
		BOR_LEV[2:0]=101 (Rising edge)	2.7(2)	2.8	2.9	
		BOR_LEV[2:0]=101 (Falling edge)	2.6	2.7	2.8(2)	
		BOR_LEV[2:0]=110 (Rising edge)	2.9(2)	3	3.1	
		BOR_LEV[2:0]=110 (Falling edge)	2.8	2.9	3(2)	
		BOR_LEV[2:0]=111 (Rising edge)	3.1(2)	3.2	3.3	
		BOR_LEV[2:0]=111 (Falling edge)	3	3.1	3.2(2)	
$V_{_BOR_hyst}$	BOR hysteresis	-	-	100	-	mV

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

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5.3.4. Supply current characteristics

Table 5-7 Current consumption in Run mode

Symbol	Conditions						Typ(1)	Max(1)		Unit
	System clock	Frequency	Code	Run	Peripheral clock	Flash sleep		T_A= 85 °C	T_A = 105 °C	
I_{CC}(Run)	HSI	24 MHz	While(1)	Flash	ON	DISABLE	1.1	1.4	1.5	mA
					OFF	DISABLE	0.9	1.0	1.1	
	LSI	32.768 kHz			ON	DISABLE	160.4	240	270	µA
					OFF	DISABLE	159.6	240	270	
		32.768 kHz			ON	ENABLE	108.3	160	190	
					OFF	ENABLE	107.7	160	190	

1. Data based on characterization results, not tested in production.

Table 5-8 Current consumption in Sleep mode

Symbol	Conditions				Typ(1)	Max(1)		Unit
	System clock	Frequency	Peripheral clock	Flash sleep		T_A = 85 °C	T_A= 105 °C	
I_{CC}(Sleep)	HSI	24 MHz	ON	DISABLE	0.8	0.9	0.95	mA
			OFF	DISABLE	0.5	0.56	0.6	
	LSI	32.768 kHz	ON	DISABLE	159.3	240	270	µA
			OFF	DISABLE	158.9	240	270	
		32.768 kHz	ON	ENABLE	85.3	140	170	
			OFF	ENABLE	84.8	140	170	

1. Data based on characterization results, not tested in production.

Table 5-9 Current consumption in Stop mode

Symbol	Conditions				Typ(1)	Max(1)		Unit
	V_{CC}	MR/LPR	LSI	Peripheral clock		T_A = 85 °C	T_A = 105 °C	
I_{CC}(Stop)	1.7 to 5.5 V	Regulator in MR mode (LPR = 00)	OFF	OFF	75.3	130	170	µA
		Regulator in LPR mode (LPR = 01)	ON	IWDG+LPTIM	1.7	20	40	
				IWDG	1.7	20	40	
				LPTIM	1.7	20	40	
			OFF	OFF	1.5	19	38	

1. Data based on characterization results, not tested in production.

5.3.5. Wake-up time from low-power mode

Table 5-10 Wake-up time from low-power mode

Symbol	Parameter(1)	Conditions		Typ(2)	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode to Run mode	-		6	-	CPU cycles
t_{WUSTOP}	Wake-up from Stop mode to Run mode in Flash	Regulator in MR (LPR = 00)	System clock HSI = 24 MHz	7.4	-	µs
		Regulator in LPR (LPR = 01)	System clock HSI = 24 MHz	11	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data based on characterization results, not tested in production.

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5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In HSE bypass mode (HSEEN of RCC_CR is set), the corresponding IO acts as an external clock input port.

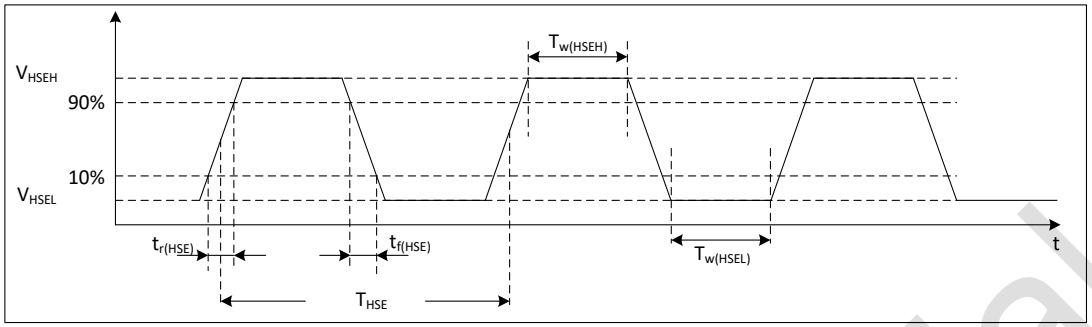


Figure 5-2 High-speed external clock timing diagram

Table 5-11 High-speed external clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	1	8	32	MHz
V_{HSEH}	Input pin high level voltage	0.7*V_{CC}	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	V_{SS}	-	0.3*V_{CC}	V
$t_{W(HSEH)}$ $t_{W(HSEL)}$	High or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Rise or fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

5.3.6.2. Low-speed external clock generated from an external source

In the bypass mode of LSE (the LSEBYP of RCC_BDCR is set), the low-speed start-up circuit in the chip stops working, and the corresponding I/O is used as a standard GPIO.

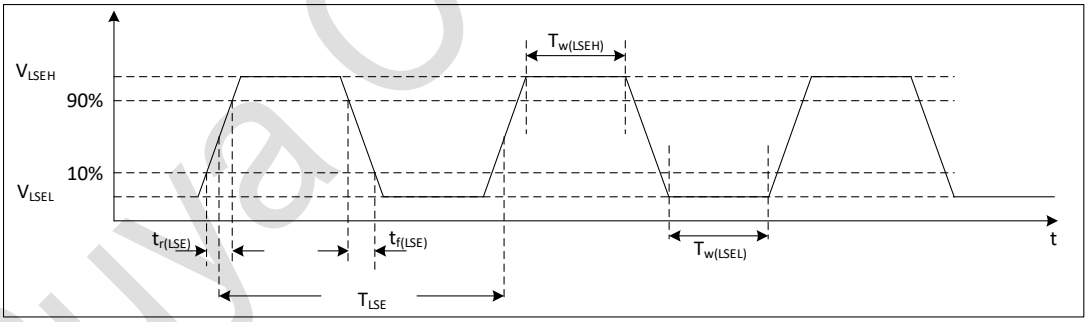


Figure 5-3 Low-speed external clock timing diagram

Table 5-12 Low-speed external clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	32.768	1000	kHz
V_{LSEH}	Input pin high level voltage	0.7*V_{CC}	-	-	V
V_{LSEL}	Input pin low level voltage	-	-	0.3*V_{CC}	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	High or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Rise or fall time	-	-	50	ns

1. Guaranteed by design, not tested in production.

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5.3.6.3. Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-13 LSE oscillator characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
I_{CC}[4]	LSE current consumption	LSE_DRIVER [1:0] = 00[3]	-	-	-	μA
		LSE_DRIVER [1:0] = 01, Rm = 70 Ω,C_L = 6 pF	-	0.8	-	
		LSE_DRIVER [1:0] = 10, Rm = 50, C_L = 12 pF	-	1.1	-	
		LSE_DRIVER [1:0] = 11, Rm = 50 Ω, C_L = 12 pF	-	1.4	-	
$t_{SU(LSE)}$[4] [5]	Startup time	LSE_DRIVER [1:0] = 00[3]	-	-	-	s
		LSE_DRIVER [1:0] = 01, Rm = 70 Ω, C_L = 6 pF	-	0.28	-	
		LSE_DRIVER [1:0] = 10, Rm = 50 Ω, C_L = 12 pF	-	0.42	-	
		LSE_DRIVER [1:0] = 11, Rm = 50 Ω, C_L = 12 pF	-	0.3	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. Reserved is reserved and is not recommended.
4. $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable, measured for a standard crystal/resonator, which may vary greatly from crystal to resonator.
5. Data based on characterization results, not tested in production.

5.3.7. High-speed internal (HSI) RC oscillator

Table 5-14 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	T_A = 25 °C, V_{CC} = 3.3 V	23.83[2]	24	24.17[2]	MHz
$\Delta_{Temp(HSI)}$	HSI frequency drift over temperature	T_A = -20 to 85 °C	-2[2]	-	2[2]	%
		T_A = -40 to 105 °C	-3[2]	-	3[2]	
f_{TRIM}[1]	HSI trimming accuracy	-	-	0.1	-	%
D_{HSI}[1]	Duty cycle	-	45	-	55	%
$t_{Stab(HSI)}$	HSI stabilization time	-	-	2	4[1]	μs
$I_{CC(HSI)}$ [2]	HSI power consumption	24 MHz	-	193	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.8. Low-speed internal (LSI) RC oscillator

Table 5-15 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	T_A = 25 °C,V_{CC} = 3.3 V	31.6	32.768	33.6	kHz
$\Delta_{Temp(LSI)}$	LSI frequency drift over temperature	T_A = 0 to 105 °C	-15[2]	-	15[2]	%
		T_A = -40 to 105 °C	-20[2]	-	20[2]	
f_{TRIM}[1]	LSI trimming accuracy	-	-	0.2	-	%
$t_{Stab(LSI)}$ [1]	LSI stabilization time	-	-	150	-	μs
$I_{CC(LSI)}$ [1]	LSI power consumption	-	-	210	-	nA

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1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.9. Memory characteristics

Table 5-16 Memory characteristics

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}	Page programming time	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase time	-	3.5	5.0	ms
I_{CC}	Page programming supply current	-	2.1	2.9	mA
	Page/sector/mass erase supply current	-	2.1	2.9	

1. Guaranteed by design, not tested in production.

Table 5-17 Memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 to 85 °C	100	kcycle
		T_A = 85 to 105 °C	10	
t_{RET}	Data retention time	10 kcycle T_A = 55 °C	20	Year
		1 kcycle T_A = 85 °C	10	

1. Data based on characterization results, not tested in production.

5.3.10. EFT characteristics

Table 5-18 EFT characteristics

Symbol	Parameter	Conditions	Grade
EFT to Power	-	IEC61000-4-4	4A

5.3.11. ESD & LU characteristics

Table 5-19 ESD&LU characteristics

Symbol	Parameter	Conditions	Typ	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	6	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	ESDA/JEDEC JS-002-2018	1	kV
LU	Static Latch-up class	JESD78E	200	mA

5.3.12. Port characteristics

Table 5-20 Port static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{CC} = 1.7 to 5.5 V	0.7*V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC} = 1.7 to 5.5 V	-	-	0.3*V_{CC}	V
V_{hys}(1)	Schmitt trigger hysteresis	-	-	200	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	-	30	50	70	kΩ
R_{PD}	Weak pull-down equivalent resistor	-	30	50	70	kΩ
C_{IO}(1)	Pin capacitance	-	-	5	-	pF
$t_{ns(EXTI)}$ (1)	Input filter width(EXTI)	ENI=1, ENS=1	3	5	10	ns
$t_{ns(I2C)}$ (1)	Input filter width(I²C)	ENI=1, EIIC=1	70	90	120	ns

1. Guaranteed by design, not tested in production.

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Table 5-21 Output voltage characteristics(3)

Symbol	Parameter(2)	Conditions		Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin	GPIOx_OSPEEDR = 11	I_{OL} = 20 mA, V_{CC} ≥ 5.0 V	-	0.4	V
			I_{OL} = 8 mA, V_{CC} ≥ 2.7 V	-	0.4	
			I_{OL} = 4 mA, V_{CC} = 1.8 V	-	0.5	
V_{OH} (1)	Output high level voltage for an I/O pin	GPIOx_OSPEEDR = 11	I_{OH} = 18 mA, V_{CC} ≥ 5.0 V	V_{CC}–0.6	-	V
			I_{OH} = 8 mA, V_{CC} ≥ 2.7 V	V_{CC}–0.4	-	
			I_{OH} = 4 mA, V_{CC} = 1.8 V	V_{CC}–0.5	-	

1. These I/O types refer to the terms and symbols defined by pins.
2. Data based on characterization results, not tested in production.
3. The combined maximum current across all output pins (including contributions from both V_{OL} and V_{OH} states) must not exceed the $\Sigma I_{IO(PIN)}$ maximum rating specified in Table 5-2 Current Characteristics.

5.3.13. ADC characteristics

Table 5-22 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	ADC supply voltage	-	1.8	-	5.5	V
I_{CC}	Current consumption from V_{CC}	f_s = 0.75 Msps	-	300	-	μA
C_{ADC}(1)	Internal sampling and holding capacitor	-	-	5	8	pF
R_{AIN}(1)(3)	External input impedance	-	-	-	31	kΩ
R_{ADC}(1)	Sampling switch resistance	-	-	-	2.5	kΩ
f_{ADC}	ADC clock frequency	V_{REF+} = V_{CC} = 1.8 to 2.3 V	0.8	3	6(2)	MHz
		V_{REF+} = V_{CC} = 2.3 to 5.5 V	0.8	6	12(2)	
f_S	Sampling rate	V_{REF+} = V_{CC} = 1.8 to 2.3 V	0.05	-	0.375	Msps
		V_{REF+} = V_{CC} = 2.3 to 5.5 V	0.05	-	0.75	
t_{CAL}(1)	Calibration time	f_{ADC} = 12 MHz	5.83	-	9.92	μs
			70	-	119	$1/f_{ADC}$
t_{samp}(1)	Sampling time	f_{ADC} = 6 MHz V_{CC} = 1.8 to 2.3 V	0.438	-	29.94	μs
			3.5	-	239.5	$1/f_{ADC}$
		f_{ADC} = 12 MHz V_{CC} = 2.3 to 5.5 V	0.292	-	19.96	μs
			3.5	-	239.5	$1/f_{ADC}$
t_{samp_int}(1)	Sampling time for internal channels	-	20	-	-	μs
t_{conv}(1)	Total conversion time	V_{CC} = 1.8 to 5.5 V	12	-	248	$1/f_{ADC}$
t_{eoc}(1)	Conversion end time	V_{CC} = 1.8 to 5.5 V	0.5			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. Equation 1: R_{AIN} maximum formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

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Table 5-23 R_{AIN} max for f_{ADC} = 12 MHz(1)

Ts (cycles)	t_S (μs)	R_{AIN} max (kΩ)
3.5	0.29	0.3
5.5	0.46	1.9
7.5	0.62	3.5
13.5	1.12	8.3
28.5	2.37	20.4
41.5	3.46	30.9
134.5	11.21	-
239.5	15.96	-

1. Guaranteed by design, not tested in production.

Table 5-24 ADC accuracy(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	f_{ADC} = 12 MHz, V_{REF+} = V_{CC} = 2.3 to 5.5 V	-	±10.0	-	LSB
EO	Offset error		-	± 3.0	-	LSB
EG	Gain error		-	± 5.0	-	LSB
DNL	Differential linearity error		-	± 1.5	-	LSB
INL	Integral linearity		-	± 6.5	-	LSB
ENOB	Effective number of bits		-	9.0	-	bit

1. ADC DC accuracy values are measured after internal calibration.
2. Data based on characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

5.3.14. Comparator characteristics

Table 5-25 Comparator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}(1)	Input voltage range	-		0	-	V_{CC}-1.5	V
t_{START}(1)	Start-up time	-		-	-	5	μs
t_D(1)	Propagation delay	200 mV step,100mV over-drive	Output from low to high	-	200	-	ns
			Output from high to low	-	150	-	
V_{offset}(1)	Offset voltage	-		-	±5	-	mV
V_{hys}(1)	Hysteresis voltage	No hysteresis		-	0	-	mV
I_{CC}(2)	Current consumption from V_{CC}	-		-	50	-	μA

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

5.3.15. Temperature sensor characteristics

Table 5-26 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30 °C (±5 °C)	0.74	0.76	0.78	V
t_{START}(1)	Start-up time entering in continuous mode	-	70	120	μs
t_{S_setup} (1)	ADC sampling time when reading the temperature	20	-	-	μs

1. Guaranteed by design, not tested in production.

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5.3.16. Embedded internal voltage reference (V_{REFINT}) characteristics

Table 5-27 Internal voltage reference (V_{REFINT}) characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$t_{start_VREFINT}$	Start time of V_{REFINT}	-	10	15	μs
$T_{coeff_VREFINT}$	Temperature coefficient of V_{REFINT}	-	-	100(1)	ppm/°C
I_{REFINT}	V_{REFINT} Current consumption	-	12	20	μA

1. Guaranteed by design, not tested in production.

5.3.17. Internal voltage reference buffer(V_{REFBUF}) characteristics

Table 5-28 Internal voltage reference buffer (V_{REFBUF}) characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REF25}	2.5 V internal reference buffer	T_A = 25 °C, V_{CC} = 3.3 V	2.425	2.5(2)	2.575	V
V_{REF20}	2.048 V internal reference buffer	T_A = 25 °C, V_{CC} = 3.3 V	1.988	2.048(2)	2.108	V
V_{REF15}	1.5 V internal reference buffer	T_A = 25 °C, V_{CC} = 3.3 V	1.485	1.5(2)	1.515	V
$T_{coefft_VREFBUF}$	Temperature coefficient of V_{REFBUF}	T_A = -40 to 105 °C	-	-	120(1)	ppm/°C
$t_{start_VREFBUF}$	Start time of V_{REFBUF}	-	-	10	15	μs

1. Guaranteed by design, not tested in production.
2. 1.5 V internal reference buffer precision value storage address: 0x1FFF002E.
   2.048 V internal reference buffer precision value storage address: 0x1FFF0032.
   2.5 V internal reference buffer precision value storage address: 0x1FFF0036.
   eg: Reading the 16-bit value 0x1501 from address 0x1FFF002E indicates a reference voltage precise value of 1.501 V.

5.3.18. COMP voltage reference characteristics

Table 5-29 V_{REFCMP} for comparator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔV_{abs}	Absolute deviation	-	-	-	±0.5	LSB
$t_{start_VREFCMP}$	Start time of V_{REFCMP}	-	-	10	15	μs

1. Guaranteed by design, not tested in production.

5.3.19. Timer characteristics

Table 5-30 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	41.667	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 24 MHz	-	12	
Res_{TIM}	Timer resolution time	TIM1/14	-	16	bit
$t_{COUNTER}$	16-bit counter internal clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	0.041667	2730	μs

Table 5-31 LPTIM characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PRESC[2:0]	Min	Max	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	

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Prescaler	PRESC[2:0]	Min	Max	Unit
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

Table5-32 WDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

5.3.20. Communication interfaces

5.3.20.1. I²C interface characteristics

I²C interface meets the requirements of the I²C bus specification and user manual:

- Standard mode (Sm): 100 kbit/s
- Fast mode (Fm): 400 kbit/s

Table 5-33 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

5.3.20.2. SPI characteristics

Table 5-34 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	12(1)	MHz
		Slave mode	-	3(2)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode, presc = 8	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-1	Tpclk+1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	ns
		Slave mode	3	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	5.5	-	ns
		Slave mode	4	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	34	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	16	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	4.5	ns

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Symbol	Parameter	Conditions	Min	Max	Unit
$t_{h(SO)}$ $t_{h(MO)}$	Data output hold time	Slave mode (after enable edge)	6	-	ns
		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

1. The test condition for this parameter is full-duplex mode.
2. The test condition of Parameter is single-wire mode, and the maximum is 0.75 MHz in full-duplex mode.

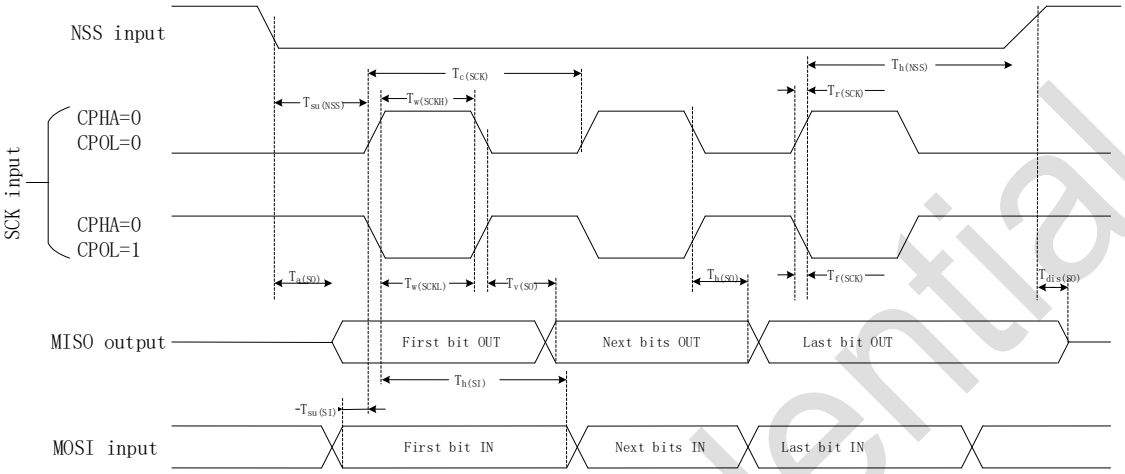


Figure 5-4 SPI timing diagram–Slave mode and CPHA=0

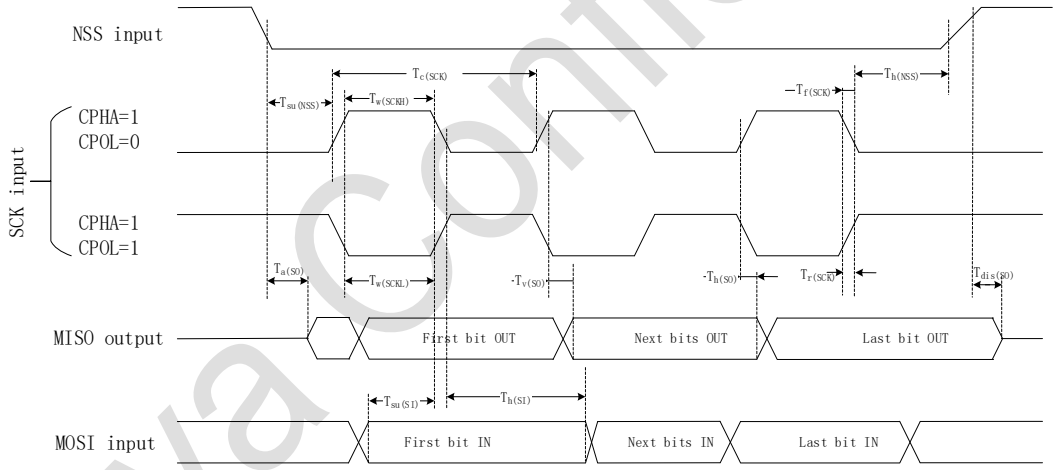


Figure 5-5 SPI timing diagram–Slave mode and CPHA=1

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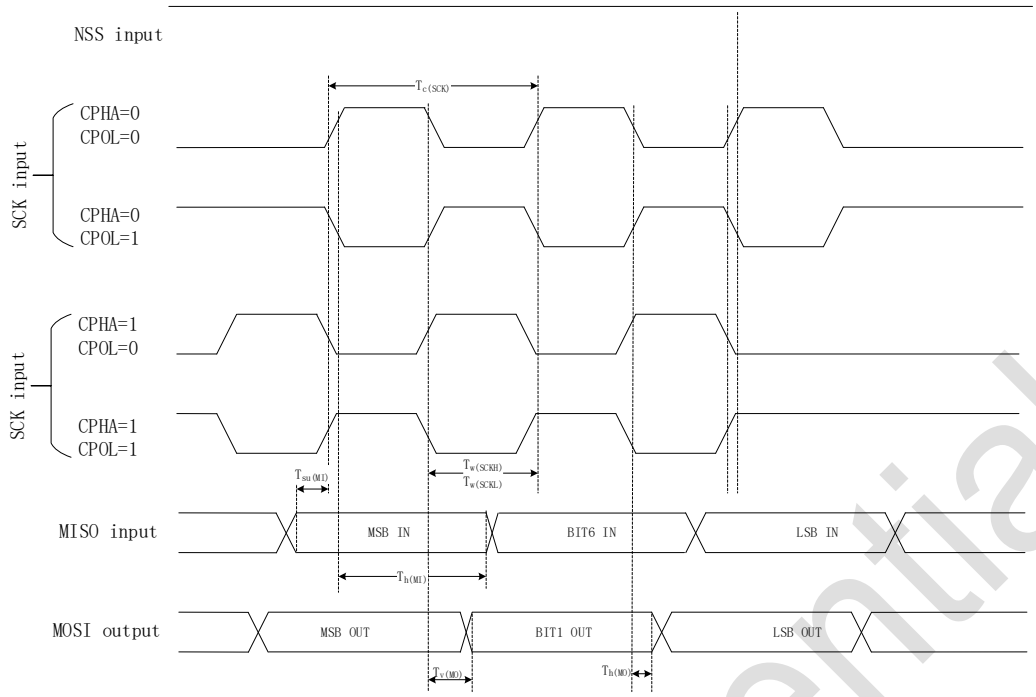


Figure 5-6 SPI timing diagram–Master mode

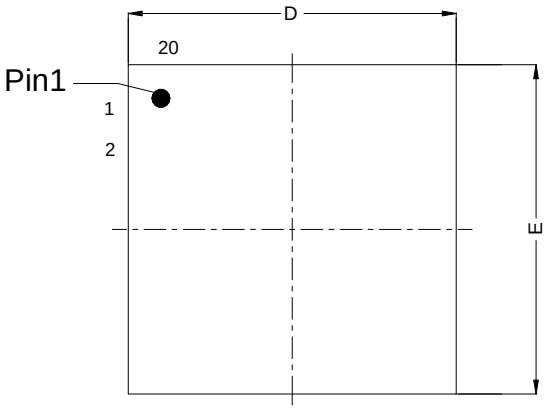
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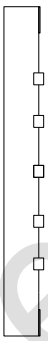
6. Package information

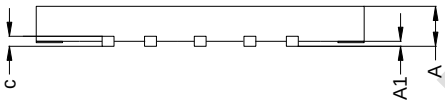
6.1. QFN20(3*3*0.5) package size

TOP VIEW

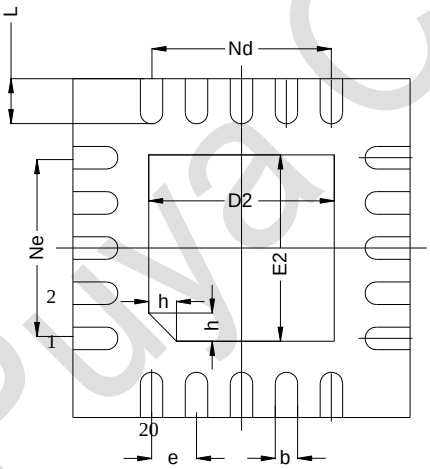


SIDE VIEW





BOTTOM VIEW



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.450	0.500	0.550
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c		0.127REF	
D	2.900	3.000	3.100
D2	1.600	1.700	1.800
E	2.900	3.000	3.100
E2	1.600	1.700	1.800
e		0.400BSC	
Nd		1.600BSC	
Ne		1.600BSC	
L	0.300	0.350	0.400
h	0.250	0.300	0.350

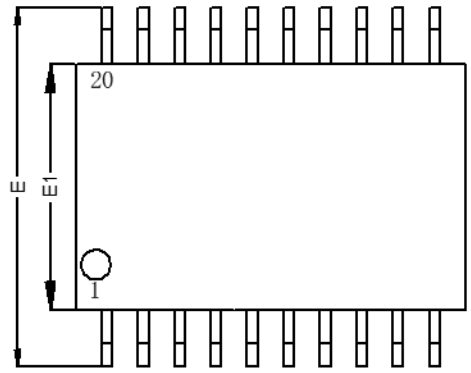
Note：1. Dimensions are not to scale

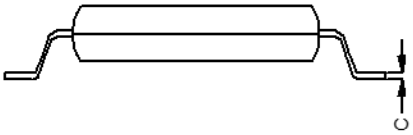
	TITLE	DRAWING NO.	REV
PUYA	Puya QFN20L 3x3X0.50-0.4PITCH POD	QRPD-0054	1.0

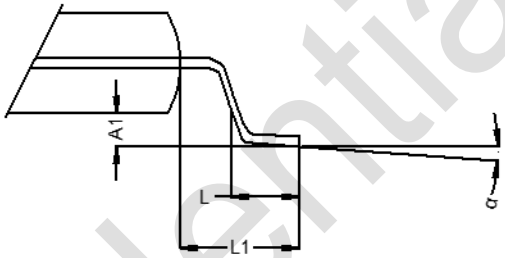
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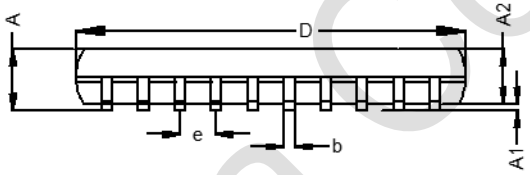
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6.2. TSSOP20 package size









Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
b	0.200	-	0.280
c	0.090	-	0.200
D	6.400	6.500	6.600
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	0.650BSC		
L	0.450	0.600	0.750
L1	1.000REF		
θ	0	-	8°

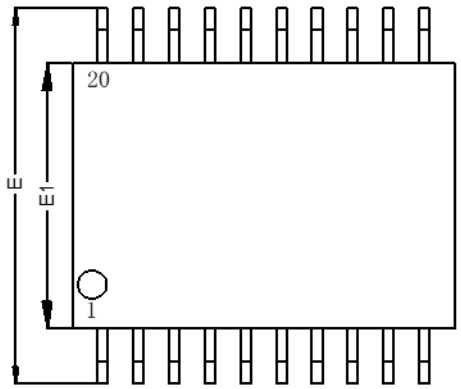
Note：1. Dimensions are not to scale

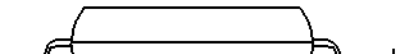
	TITLE	DRAWING NO.	REV
PUYA	Puya TSSOP20 POD	QRPD-0043	1.0

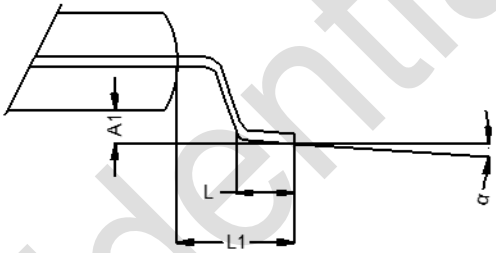
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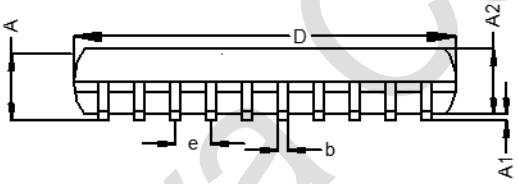
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6.3. SOP20 package size









Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	2.650
A1	0.100	-	0.300
A2	2.100	2.300	2.500
b	0.330	-	0.510
c	0.200	-	0.330
D	12.600	12.800	13.000
E	10.100	10.300	10.500
E1	7.400	7.500	7.600
e	1.275BSC		
h	0.300	-	0.500
L	0.400	-	1.270
L1		1.400REF	
θ	0	-	8°

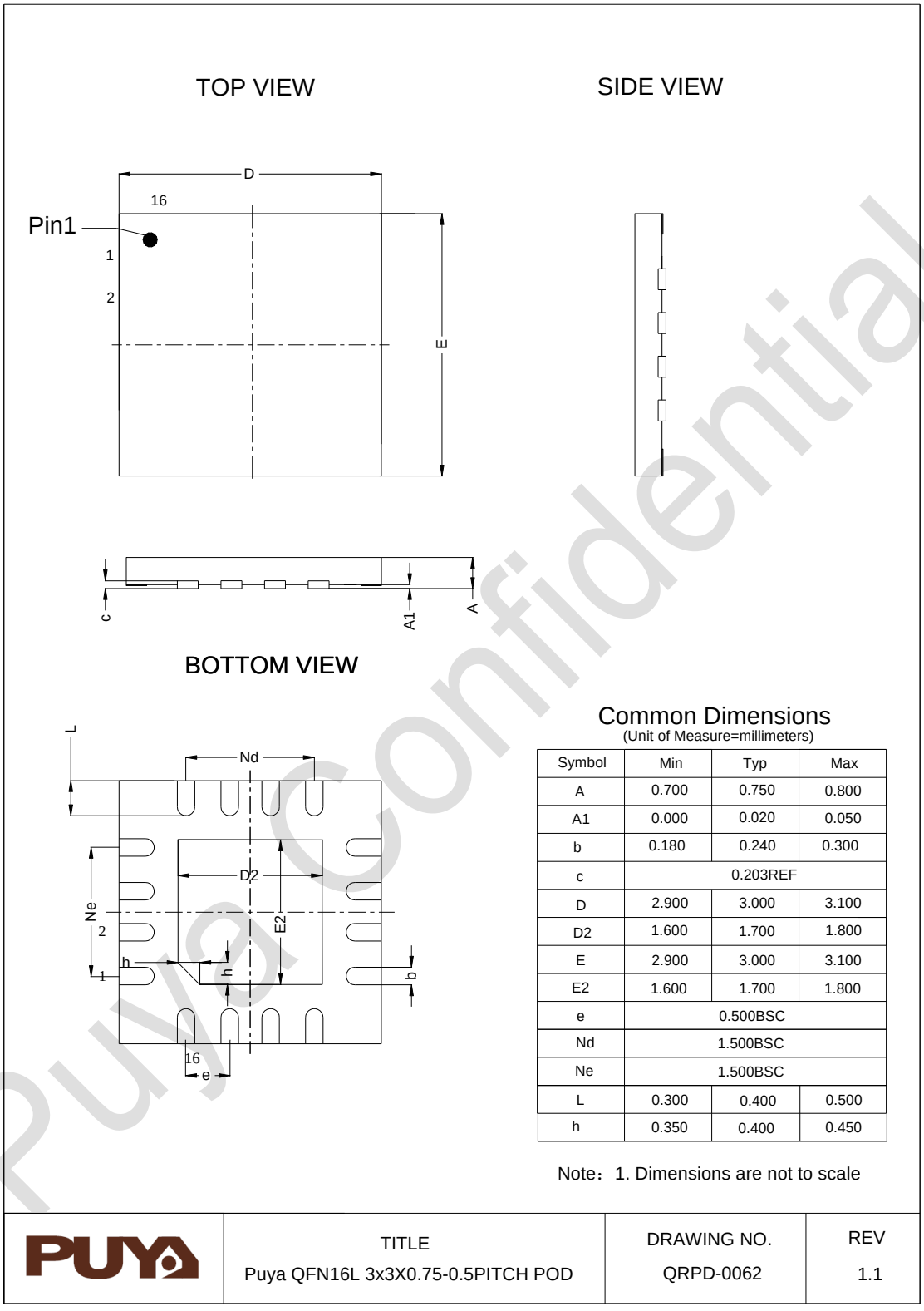
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya SOP20 POD	QRPD-0048	1.0

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6.4. QFN16 package size



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.180	0.240	0.300
c		0.203REF	
D	2.900	3.000	3.100
D2	1.600	1.700	1.800
E	2.900	3.000	3.100
E2	1.600	1.700	1.800
e		0.500BSC	
Nd		1.500BSC	
Ne		1.500BSC	
L	0.300	0.400	0.500
h	0.350	0.400	0.450

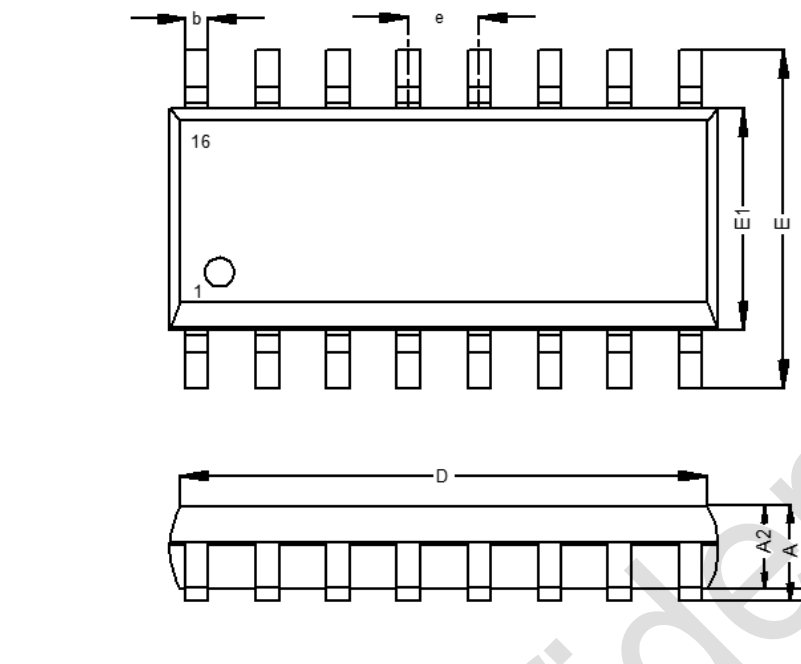
Note：1. Dimensions are not to scale

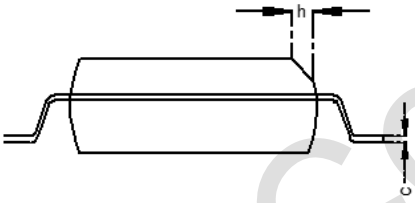
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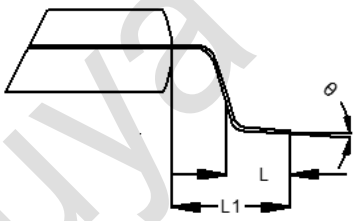
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6.5. SOP16 package size







Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.30	-	-
b	0.31	-	0.51
c	0.10	-	0.25
D	9.80	-	10.20
E	5.80	-	6.20
E1	3.80	-	4.20
e	1.27BSC		
L	0.40	-	1.27
L1	1.05REF		
θ	0	-	8°
h	0.25	-	0.50

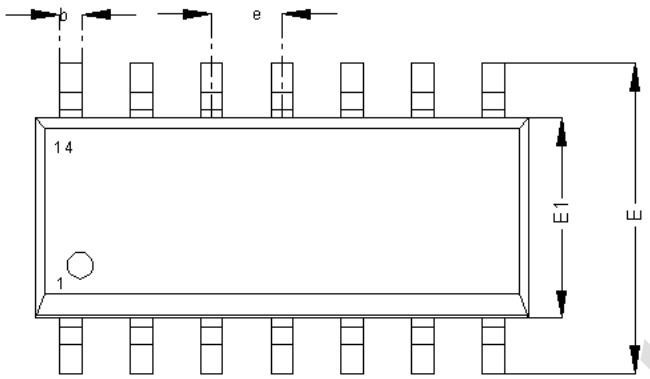
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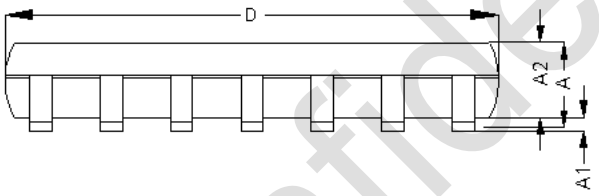
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PUYA	PUYA SOP16 (150mil) POD	QRPD-0001	1.1

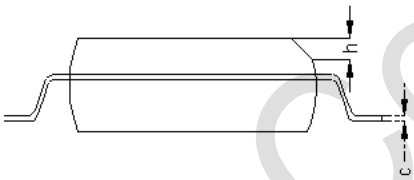
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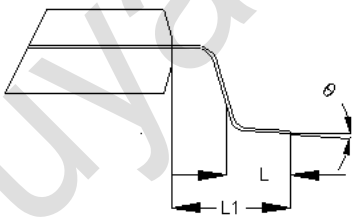
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6.6. SOP14 package size









Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
b	0.35	-	0.50
c	0.19	-	0.25
D	8.50	8.60	8.70
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.40	-	0.80
θ	0	-	8°
h	0.30	-	0.50
L1	1.05REF		

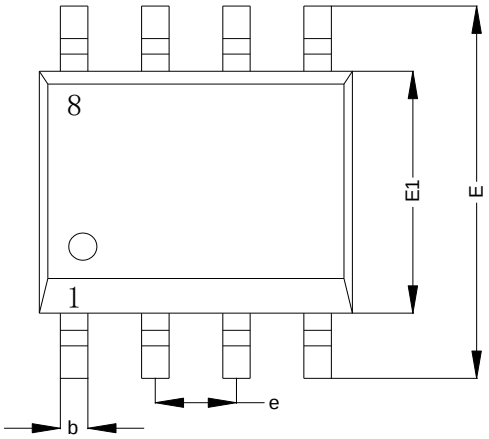
Note：Dimensions are not to scale.

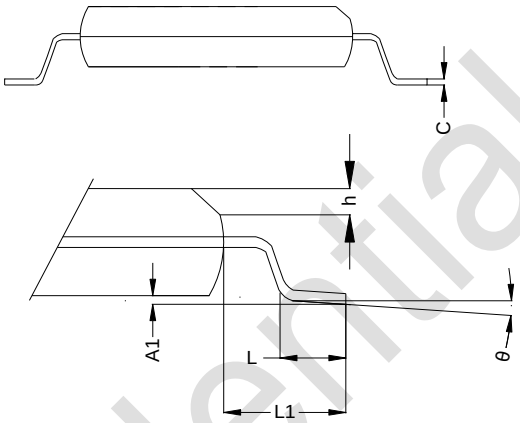
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PUYA	PUYA SOP14 (150mil) POD	QRPD-0070	1.1

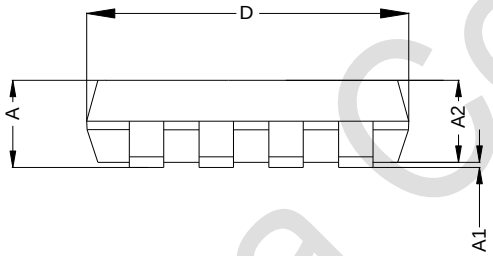
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6.7. SOP8 package size







Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	1.350	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.170	-	0.250
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	-	1.270	-
L	0.400	-	1.270
L1	-	1.050	-
θ	0	-	8°
h	0.25	-	0.50

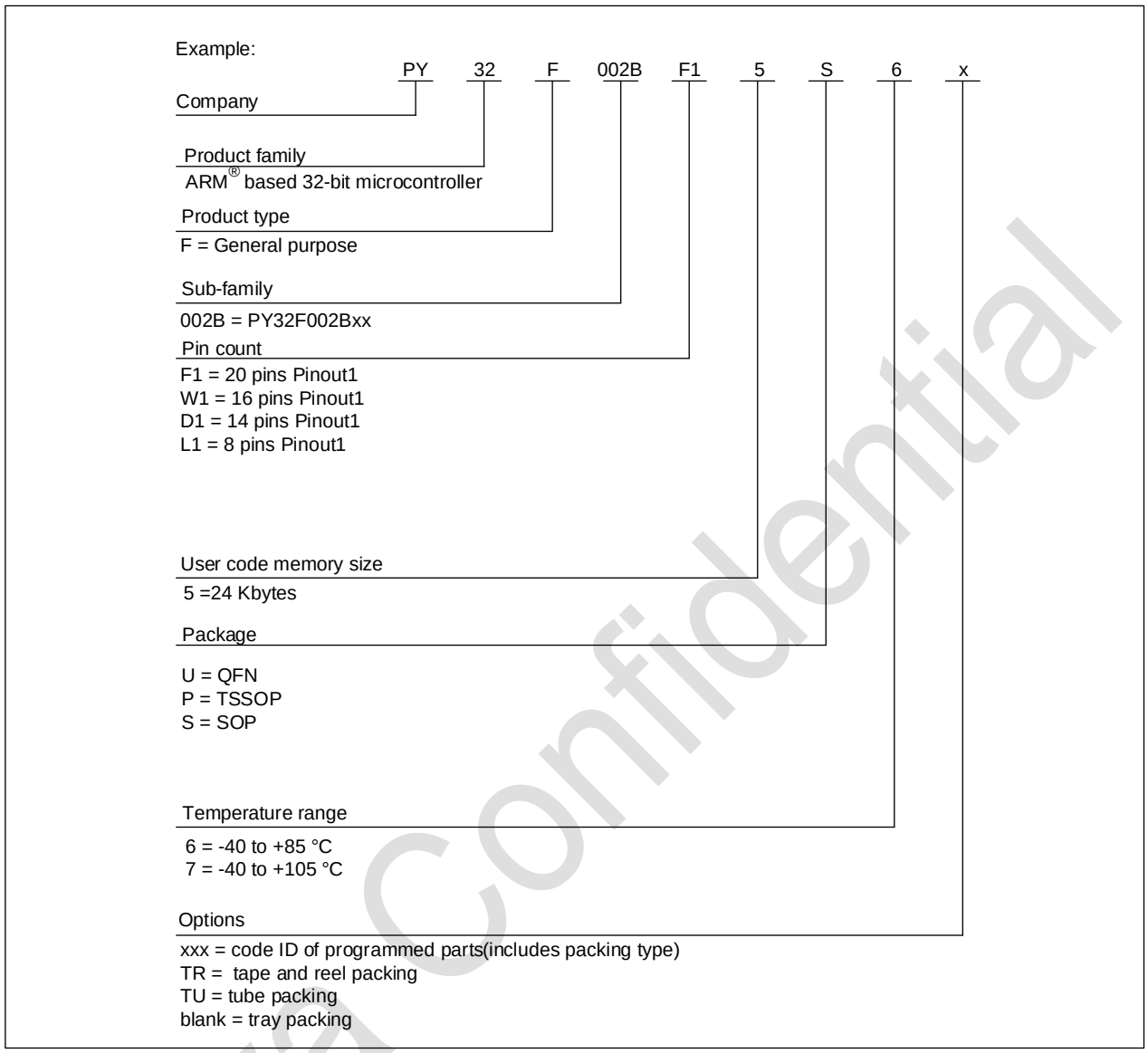
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya SOP8（150mil）POD	QRPD-0004	1.1

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7. Ordering information



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8. Version history

Version	Date	Description
V0.1	2022.12.16	Beta version
V0.2	2023.01.02	1. Update Table 1-1/3-1/ 3-2
V0.3	2023.02.11	1. Update Table 1-1/3-1/3-2
V0.4	2023.03.15	1. Update Table 1-1/3-1
V0.5	2023.03.22	1. Update 1.0.Introduction section
V0.6	2023.05.10	1. Update SOP16/SOP14 pinout,Table 3-2
V0.7	2023.06.07	1. Update Table 5-9 2. Update Table 3-1
V0.8	2023.07.12	1. Update 2.3 and 2.9 section
V0.9	2023.12.21	1. Update Table 5-6 2. Update 2.0.Functional overview section
V1.0	2024.06.28	Initial version
V1.1	2024.08.22	1. Add SOP20 package 2. Update Table 5-11 External high-speed clock features 3. Update QFN16 / SOP 14 / SOP8 package information
V1.2	2024.11.11	1. Delete QFN20(3*3*0.55) package information
V1.7	2025.08.06	1. Consist with the Chinese version No.
V1.8	2025.08.20	1. Replacement of the company logo mark

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