Migration from P25Q40H to P25Q40SH SPI Flash Application Note

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The document provides conversion guidelines for migrating from the P25Q40H to the P25Q40SH SPI Flash,and discusses the specification differences.



Puya Semiconductor (Shanghai) Co., Ltd

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深圳市满度科技有限公司 Tel:150-1290-5940
Web:www.manduic.com Email:sales@manduic.com

1 Introduction

PUYA P25Q40SH Flash is a feature rich and cost-optimized serial peripheral interface (SPI) non-volatile NOR flash family. This application note provides conversion guidelines for migrating from the P25Q40H to the P25Q40SH Flash.

This application note is based on information available to date from datasheets and other application notes publicly available from PUYA. Please refer also to the latest relevant specifications. The document discusses the specification differences when migrating from P25Q40H to P25Q40SH.

2 Feature Comparison and Differences

PUYA P25Q40H products are well suited for migration to PUYA P25Q40SH products. Some of the reasons are compatible pinouts, packages, command set, and 4KB sector structure. Both P25Q40H and P25Q40SH devices support Single (Standard) I/O, Dual I/O, and Quad I/O modes. The main differences between P25Q40H and P25Q40SH are listed in the table below:

Table 2-1. High Level Feature Support Comparison

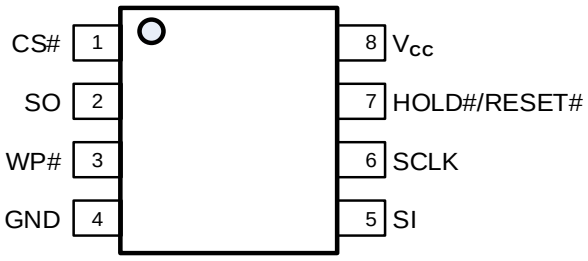
Feature / Parameter	P25Q40H	P25Q40SH
Supple Voltage	2.3V-3.6V	2.3V-3.6V
Single (Standard) IO Operations	√	√
Dual IO Operations	√	√
Quad IO Operations	√	√
QPI	not support	√
Standard Normal Read SCK Frequency (max)	55 MHz	55 MHz
Standard Fast Read SCK Frequency (max)	104 MHz	104 MHz
Dual Fast Read SCK Frequency (max)	104 MHz	104 MHz
Quad Fast Read SCK Frequency (max)	104 MHz	104 MHz
Software Protection	√	√
Individual Block Protection	not support	√
One Time Programmable Region(s)	3 x 512 Bytes	3 x 512 Bytes
Buffer access	not support	√
Erase(PE,SE,BE) time Typ.	8ms	16ms
Erase(CE) time Typ.	8ms	16ms
Configure Register	not support	√
Temperature Range Option	-40C to +85C	-40C to +85C

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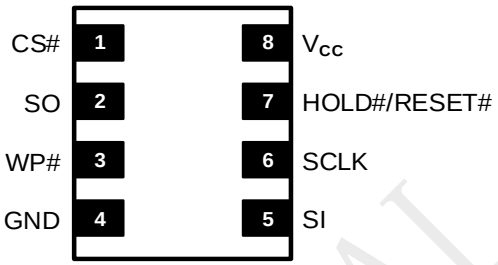
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2.1 Hardware Package

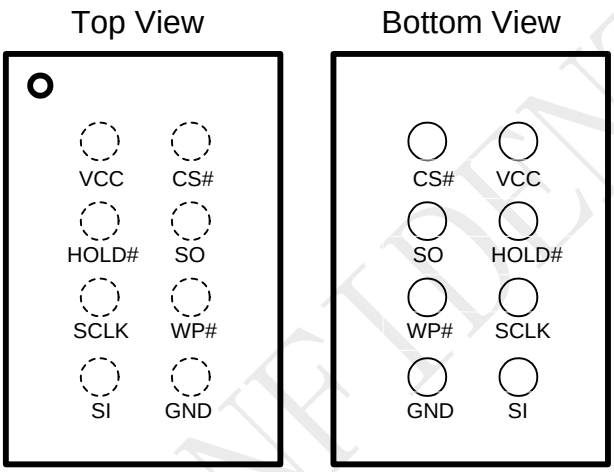
The pinouts of P25Q40H and P25Q40SH are identical.



8-PIN SOP (150mil/208mil) and TSSOP



8-Land USON (3x2/3x4/1.5x1.5mm)/ WSON (6x5mm)



8-Ball WLCSP Ball Assignment

Table 2-1-1 Pin Descriptions

No.	Symbol	Extension	Remarks
1	CS#		Chip select
2	SO	SIO1	Serial data output for 1 x I/O Serial data input and output for 4 x I/O read mode
3	WP#	SIO2	Write protection active low Serial data input and output for 4 x I/O read mode
4	GND	-	Ground of the device
5	SI	SIO0	Serial data input for 1x I/O Serial data input and output for 4 x I/O read mode
6	SCLK	-	Serial interface clock input
7	HOLD#/RESET#	SIO3	Hardware Reset Pin Active low or to pause the device without deselecting the device Serial data input and output for 4 x I/O read mode
8	Vcc	-	Power supply of the device

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2.2 IO Mode

Both P25Q40H and P25Q40SH support Single, Dual, Quad SPI. P25Q40SH supports QPI, while P25Q40H does not.

2.3 Status Registers

Both PUYA P25Q40H and P25Q40SH have two status registers: SR1 and SR2.
Only non-volatile status register bits SRP0, BP4, BP3, BP2, BP1, BP0 (Status Register-1), CMP, LB3, LB2, LB1, QE, SRP1 (Status Register-2) can be written. All other status register bit locations are read-only and will not be affected by the Write Status Register instruction.

Table 2-3-1. Status Register Bits Assignments

SR Bits	P25Q40H	P25Q40SH	Function
S15	SUS1	SUS	SUS: Erase\Program Suspend status SUS1: Erase Suspend status
S14	CMP	CMP	Complement Protect
S13	LB3	LB3	Security Lock Bits
S12	LB2	LB2	
S11	LB1	LB1	
S10	SUS2	EP_FAIL	SUS2: Program Suspend status EP_FAIL: the status of the last Program/Erase operation
S9	QE	QE	Quad Enable
S8	SRP1	SRP1	Status Register Protect
S7	SRP0	SRP0	
S6	BP4	BP4	Block Protect Bits
S5	BP3	BP3	
S4	BP2	BP2	
S3	BP1	BP1	
S2	BP0	BP0	
S1	WEL	WEL	Write Enable
S0	WIP	WIP	Write In Progress

Table 2-3-2. Write Status Register

P/N	Commands	Abbr.	Code	ADR Bytes	DMY Bytes	Data Bytes	Function
P25Q40H / P25Q40SH (with ordering option "D")	Write Status Register	WRSR	01h	0	0	2	Write data to status registers
P25Q40SH	Write Status Register	WRSR	01h	0	0	1	Write data to status registers
	Write Status Register-1	WRSR1	31h	0	0	1	Write data to status registers-1

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2.4 Configure Registers

P25Q40SH supports Configure Register, while P25Q40H does not.

Table 2-4-1. Configure Register Bits Assignments

SR Bits	P25Q40SH	Function
Bit7	HOLD/RST	HOLD/RST: /HOLD or /RESET function select
Bit6	DRV1	the output driver strength for the Read operations
Bit5	DRV0	
Bit4	MPM1	the Multi Page Mode
Bit3	MPM0	
Bit2	WPS	Write Protect scheme
Bit1	DC	the Dummy Cycle bit
Bit0	DLP	Data Learning Pattern Enable bit

Table 2-4-2. Write Configure Register

P/N	Commands	Abbr.	Code	ADR	DMY	Data	Function
				Bytes	Bytes	Bytes	
P25Q40SH	Write Configure Register	WRCR	11h	0	0	1	Write data to configuration register

2.5 Active Status Interrupt

P25Q40H supports the ASI command to simplify the readout of the WIP bit, while P25Q40SH does not. It is useful for these ultra low power applications by avoid reading WIP bit continuously after erase or program operation.

2.6 Block Protection Scheme

Both PUYA P25Q40H and P25Q40SH (WPS=0) support Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits define the section of the memory array that can be read but not change. P25Q40SH also support Individual Block/Sector protection, and it is only valid when WPS=1.

2.7 Buffer Access

P25Q40SH supports Buffer access, while P25Q40H does not.

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3 Command Set Comparison

Both P25Q40H and P25Q40SH share similar instructions (op-codes) in their command-set, which determine a compatible set of internal algorithms. Nevertheless, not all commands are supported when comparing one with the other.

Table below shows a comparison summary of the command set of P25Q40H and P25Q40SH. Please refer to the data sheet for more information.

Table 3-1 Command Sets Compare List

Commands	Abbr.	Code	P25Q40H	P25Q40SH
Read				
Read Array (fast)	FREAD	0Bh	√	√
Read Array (low power)	READ	03h	√	√
Read Dual Output	DREAD	3Bh	√	√
Read 2x I/O	2READ	BBh	1 dummy bytes	1\2 dummy bytes
Read Quad Output	QREAD	6Bh	√	√
Read 4x I/O	4READ	EBh	3 dummy bytes	3\5 dummy bytes
Read Word 4IO	WREAD	E7h	not support	√
Program and Erase				
Page Erase	PE	81h	√	√
Sector Erase (4K bytes)	SE	20h	√	√
Block Erase (32K bytes)	BE32	52h	√	√
Block Erase (64K bytes)	BE64	D8h	√	√
Chip Erase	CE	60h	√	√
		C7h	√	√
Page Program	PP	02h	√	√
Dual-IN Page Program	2PP	A2h	√	not support
Quad page program	QPP	32h	√	√
Program/Erase Suspend	PES	75h	√	√
		B0h	√	not support
Program/Erase Resume	PER	7Ah	√	√
		30h	√	not support
Protection				
Write Enable	WREN	06h	√	√
Write Disable	WRDI	04h	√	√
Volatile SR Write Enable	VWREN	50h	√	√
Individual Block Lock	SBLK	36h	not support	√
Individual Block Unlock	SBULK	39h	not support	√
Read Block Lock Status	RDBLOCK	3Dh	not support	√
Global Block Lock	GBLK	7Eh	not support	√
Global Block Unlock	GBULK	98h	not support	√
Security				
Erase Security Registers	ERSCUR	44h	√	√
Program Security Registers	PRSCUR	42h	√	√
Read Security Registers	RDSCUR	48h	√	√

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Status Register				
Read Status Register	RDSR	05h	√	√
Read Status Register-1	RDSR1	35h	√	√
Read Configure Register	RDCR	15h	not support	√
Active Status Interrupt	ASI	25h	√	not support
Write Status Register	\	\	Please refer to Table 2-3-2	
Write Configure Register	\	\	Please refer to Table 2-4-2	
Data Buffer				
Buffer clear	BFCR	9Eh	not support	√
Buffer Load	BFLD	9Ah	not support	√
Buffer Read	BFRD	9Bh	not support	√
Buffer Write	BFWR	9Ch	not support	√
Buffer to Main Memory Page Program	BFPP	9Dh	not support	√
Other Commands				
Reset Enable	RSTEN	66h	√	√
Reset	RST	99h	√	√
Enable QPI	QPIEN	38h	not support	√
Read Manufacturer/device ID	RDID	9Fh	√	√
Read Manufacture ID	REMS	90h	√	√
Dual Read Manufacture ID	DREMS	92h	√	√
Quad Read Manufacture ID	QREMS	94h	√	√
Deep Power-down	DP	B9h	√	√
Release Deep Power-down / Read Electronic ID	RDP/RES	ABh	√	√
Set burst length	SBL	77h	√	√
Read SFDP	RDSFDP	5Ah	√	√
Release read enhanced		FFh	√	√
Read unique ID	RUID	4Bh	√	√
Other				
STR QPI Instructions	\	\	not support	√

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Tel:150-1290-5940
Email:sales@manduic.com

4 DC Comparison

Table 10. P25Q40H DC Typical Value @25C

Sym.	Parameter	Conditions	Typ.(3.0V)	Units
I_{DPD}	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc	0.3	uA
I_{SB}	Standby current	CS#, HOLD#, WP#=VIH all inputs at CMOS levels	9	uA
I_{CC1}	Low power read current (03h)	f=1MHz; SO=Open	0.5	mA
		f=33MHz; SO=Open	1	mA
I_{CC2}	Read current (0Bh)	f=50MHz; SO=Open	1	mA
		f=85MHz; SO=Open	1.5	mA
I_{CC3}	Program current	CS#=Vcc	1.5	mA
I_{CC4}	CE Erase current	CS#=Vcc	2	mA

Table 10. P25Q40SH DC Typical Value @25C

Sym.	Parameter	Conditions	Typ.(3.0V)	Units
I_{DPD}	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc	0.6	uA
I_{SB}	Standby current	CS#, HOLD#, WP#=VIH all inputs at CMOS levels	10	uA
I_{CC1}	Read current(STR) (1, 2, 4 IO)	f=33MHz(03h); IOUT=0mA	2	mA
		f=85MHz; IOUT=0mA	5	mA
		f=120MHz; IOUT=0mA	6	mA
I_{CC2}	Program current	CS#=Vcc	2.5	mA
I_{CC3}	Erase current	CS#=Vcc	2.5	mA

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5 AC Comparison

5.1 Erase/Program Timing

PUYA P25Q40H has much shorter Erase time for page/sector/block/chip.

Table 5-1 AC parameters for program and erase

Sym.	Parameter (1.65V to 3.6V)	P25Q40H			P25Q40SH			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$T_{ESL(6)}$	Erase Suspend Latency			30			30	us
$T_{PSL(6)}$	Program Suspend Latency			30			30	us
$T_{PRS(4)}$	Latency between Program Resume and next Suspend	20			20			us
$T_{ERS(5)}$	Latency between Erase Resume and next Suspend	20			20			us
t_{PP}	Page program time (up to 256 bytes)		2	3		2	3	ms
t_{PE}	Page erase time		8	12		16	30	ms
t_{SE}	Sector erase time		8	12		16	30	ms
t_{BE1}	Block erase time for 32K bytes		8	12		16	30	ms
t_{BE2}	Block erase time for 64K bytes		8	12		16	30	ms
t_{CE}	Chip erase time		8	12		16	30	ms

6 Conclusion

Migrating from P25Q40H to P25Q40SH is straightforward and requires minimal accommodation in regards to either system software or hardware.
Additionally, P25Q40SH support more functions such as QPI mode, Individual block protection, Buffer access, etc. P25Q40H SPI flash has much shorter erase time.

7 Reference Documents

Table 7-1 shows the datasheet versions used for comparison in this application note. For the most current specification, please refer to the Website at: http://www.puyasemi.com/

Table 7-1 Datasheet Version Table

Datasheet	Location	Versions
P25Q40H	Website	V1.8
P25Q40SH	Website	V1.1

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Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

8 Revision History

Rev.	Date	Description	Author
V1.0	2020.12.01	Preliminary release	LSQ

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