P25D64SH

Ultra-Low Power, 64M-bit

Serial Multi I/O Flash Memory Datasheet

Performance Highlight

- *Wide Supply Range from 2.3 to 3.6V for Read, Erase and Program*
- *Ultra-Low Power consumption for Read, Erase and Program*
- *X1, X2 Multi I/O Support*
- *High reliability with 100K cycling and 10Year-retention*

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1 Overview

General

- **Single 2.3V to 3.60V supply**
- **Industrial Temperature Range -40C to 85C**
- **Serial Peripheral Interface (SPI) Compatible: Mode 0 and Mode 3**
- **Single, Dual SPI**
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
- **Flexible Architecture for Code and Data Storage**
  - Uniform 256-byte Page Program
  - Uniform 256/512/1024-byte Page Erase
  - Uniform 4K-byte Sector Erase
  - Uniform 32K/64K-byte Block Erase
  - Full Chip Erase
- **Hardware Controlled Locking of Protected Sectors by WP Pin**
- **One Time Programmable (OTP) Security Register**
  - 3*1024-Byte Security Registers with OTP Lock
- **128 bits unique ID for each device**
- **Fast Program and Erase Speed**
  - 2ms Page program time
  - 16ms Page erase time
  - 16ms 4K-byte sector erase time
  - 16ms 32K/64K-byte block erase time
- **JEDEC Standard Manufacturer and Device ID Read Methodology**
- **Ultra-Low Power Consumption**
  - 0.3uA Deep Power Down current (typical)
  - 10.0uA Standby current (typical)
  - 2.5mA Active Read current at 33MHz, 4IO (typical)
  - 3.0mA Active Program or Erase current (typical)
- **High Reliability**
  - 100,000 Program / Erase Cycles
  - 10-year Data Retention
- **Industry Standard Green Package Options**
  - 8-Lead SOP (150mil/208mil)
  - 8-Pad USON(3x2x0.55mm)
  - KGD for SiP

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2 Description

The P25D64SH is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer-based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the device, with its page erase granularity it is ideal for data storage as well, eliminating the need for additional data storage devices.

The erase block sizes of the device have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large sectored and large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

The device also contains an additional 3*1024-byte security registers with OTP lock (One-Time Programmable), can be used for purposes such as unique device serialization, system-level Electronic Serial Number (ESN) storage, locked key storage, etc.

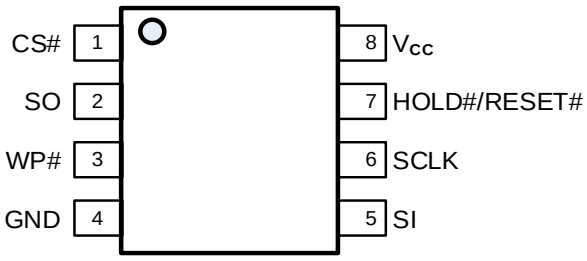
Specifically designed for use in many different systems, the device supports read, program, and erase operations with a wide supply voltage range of 2.3V to 3.6V. No separate voltage is required for programming and erasing.

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3 Pin Definition

3.1 Pin Configurations



8-PIN SOP (150mil/208mil)

3.2 Pin Descriptions

No.	Symbol	Extension	Pull Up	Remarks
1	CS#	-	-	Chip select
2	SO	SIO1	-	Serial data output for 1 x I/O Serial data input and output for 2 x I/O read mode
3	WP#	-	-	Write protection active low
4	GND	-	-	Ground of the device
5	SI	SIO0	-	Serial data input for 1x I/O Serial data input and output for 2 x I/O read mode
6	SCLK	-	-	Serial interface clock input
7	HOLD#/ RESET#	-	-	Hardware Reset Pin Active low or to pause the device without deselecting the device
8	VCC	-	-	Power supply of the device

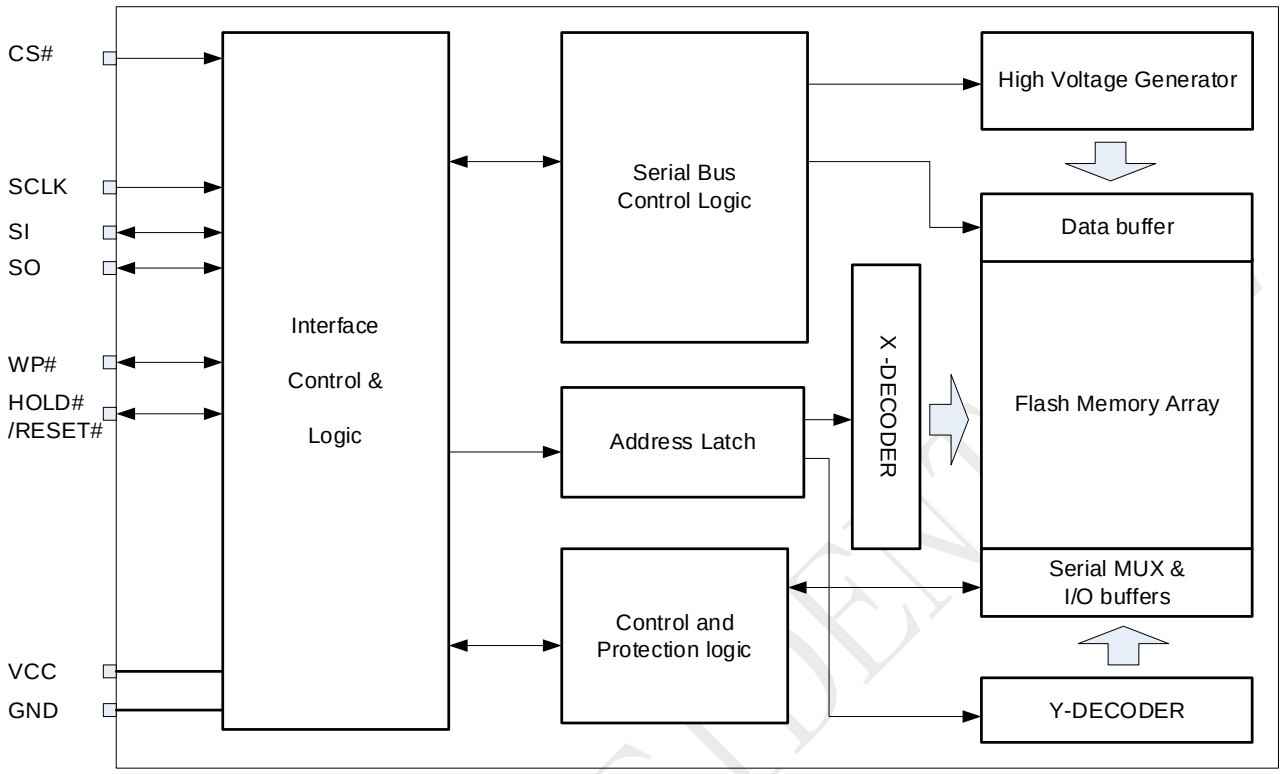
Notes:

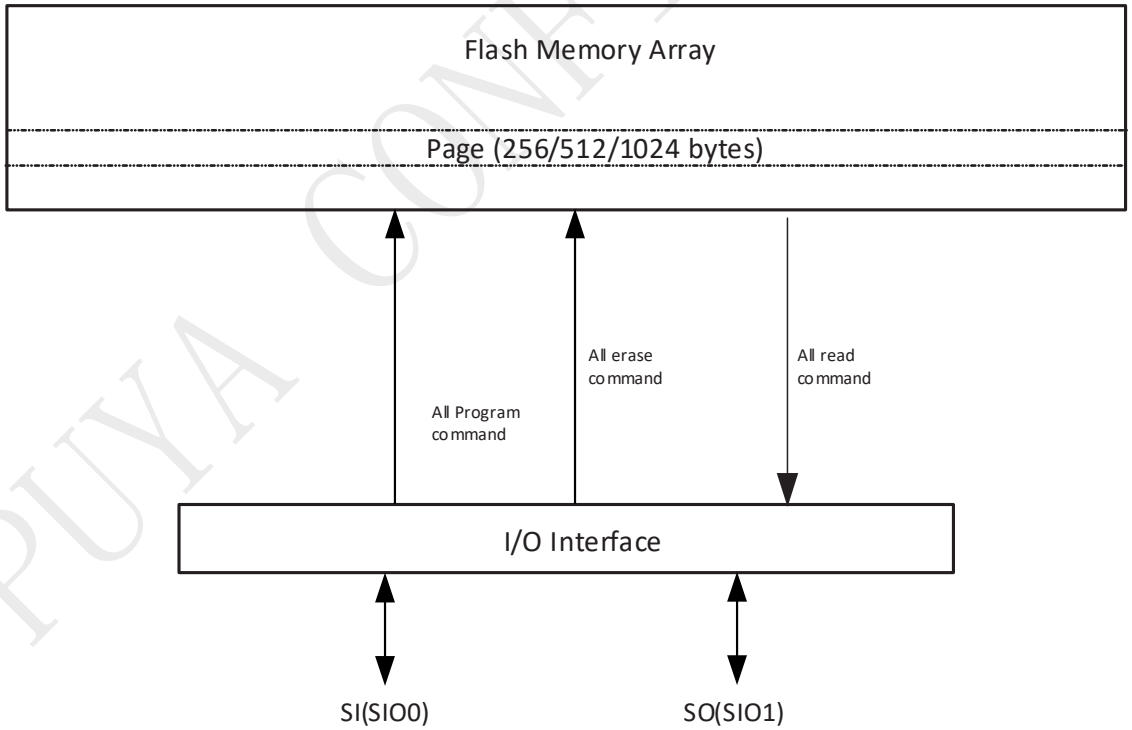
1. SIO0 and SIO1 are used for Standard and Dual SPI instructions.
2. WP# and HOLD#/RESET# pin with weak pull up

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4 Block Diagram





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5 Electrical Specifications

5.1 Absolute Maximum Ratings

- Storage Temperature .....-65°C to +150°C
- Operation Temperature .....-40°C to +85°C
- Maximum Operation Voltage..... 4.0V
- Voltage on Any Pin with respect to Ground.....-0.6V to VCC+0.5V
- DC Output Current .....5.0 mA

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Pin Capacitance [1]

Symbol	Parameter	Max	Units	Test Condition
C_{OUT}	Output Capacitance	8	pF	V_{OUT}=GND
C_{IN}	Input Capacitance	6	pF	V_{IN}=GND

Note:

1. Test Conditions: T_A= 25°C, F = 1MHz, Vcc = 3.0V.

Figure 5-1 Input Test Waveforms and Measurement Level

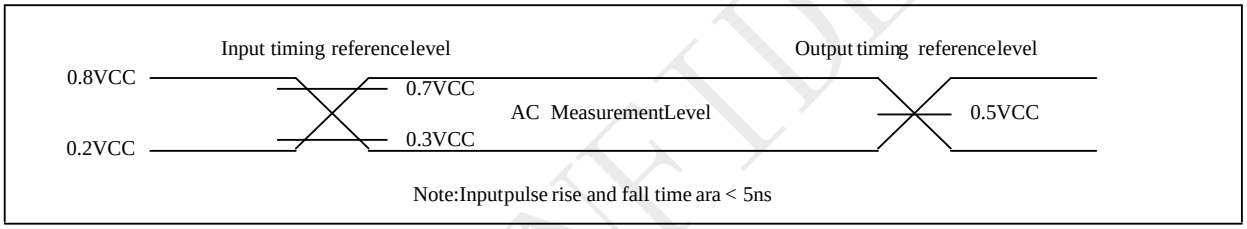
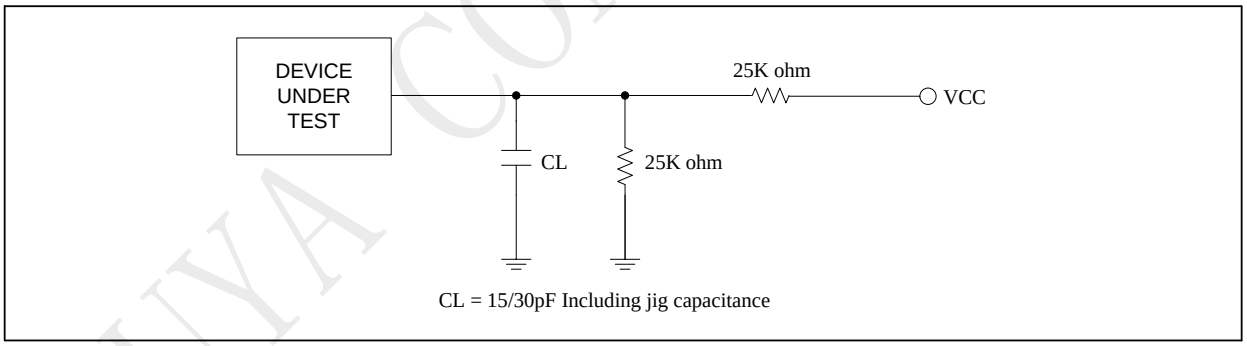


Figure 5-2 Output Loading



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5.2 DC Characteristics

Table 5-2 DC parameters (Ta=-40°C ~ +85°C)

Symbol	Parameter	Conditions	2.3V~3.6V			Units
			Min	Typ	Max	
I_{DPD}	Deep power down current	CS#=VCC, all other inputs at 0V or VCC		0.3	5.0	uA
I_{SB}	Standby current	CS#, HOLD#, WP#=VIH all inputs at CMOS levels		10.0	18.0	uA
I_{CC1}	Low power read current (03h)	f=1MHz; IOUT=0mA		0.3	0.5	mA
		f=33MHz; IOUT=0mA		1.5	3.0	mA
I_{CC2_DC}	All Read	IOUT=0mA		0.3	0.5	mA
I_{CC2_AC}	Read current, SPI(STR, x1)	IOUT=0mA		0.04	0.06	mA/MHz
	Read current, DSPI(STR, x2)	IOUT=0mA		0.052	0.08	mA/MHz
I_{CC3}	Program current	CS#=VCC		3.0	5.0	mA
I_{CC4}	Erase current	CS#=VCC		3.0	5.0	mA
I_{LI}	Input load current	All inputs at CMOS level			2.0	uA
I_{LO}	Output leakage	All inputs at CMOS level			2.0	uA
V_{IL}	Input low voltage		-0.5		0.3Vcc	V
V_{IH}	Input high voltage		0.7Vcc		Vcc+0.3	V
V_{OL}	Output low voltage	IOL=100uA			0.2	V
V_{OH}	Output high voltage	IOH=-100uA	Vcc- 0.2			V

Note

1. Typical values measured at 3.0V @ 25°C for the 2.3V to 3.6V range.
2. $I_{CC2}=I_{CC2_DC} + I_{CC2_AC} * f_{SCLK}$

Figure 5-3 Maximum Overshoot Waveform



During DC conditions, input or I/O signals should remain equal to or between VSS and VCC. During voltage transitions, inputs or I/Os may negative overshoot to –0.6V or positive overshoot to VCC + 0.5 V, for periods up to 20 ns.

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5.3 AC Characteristics

Table 5-3-1 AC parameters (Ta=-40°C ~ +85°C)

Symbol	Alt.	Parameter	2.3V~3.6V			Units
			Min	Typ	Max	
fSCLK	fC	Clock Frequency for all instructions except for special marking			120	MHz
fRSCLK	fR	Clock Frequency for READ instructions			55	MHz
fTSCLK	fT	Clock Frequency for 2READ, DREAD instructions			120	MHz
tCH (1)	tCLH	Clock High Time	3.7			ns
tCL (1)	tCLL	Clock Low Time, 45% x (1/fSCLK)	3.7			ns
tCH (1)	tCLH	Clock High Time for READ instructions	8			ns
tCL (1)	tCLL	Clock Low Time for READ instructions	8			ns
tCLCH (4)		Clock Rise Time (peak to peak)	0.1			v/ns
tCHCL (4)		Clock Fall Time (peak to peak)	0.1			v/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5			ns
tDVCH	tDSU	Data in Setup Time	2			ns
tCHDX	tDH	Data in Hold Time	3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	5			ns
tSHSL	tCSH	CS# Deselect Time from Read to next Read	20			ns
		CS# Deselect Time from Write, Erase, Program to Read Status Register	30			ns
tSHQZ (4)	tDIS	Output Disable Time			6	ns
tCLQV	tV	Clock Low to Output Valid Loading 30pF	1.5		6	ns
		Clock Low to Output Valid Loading 15pF	1.5		5	ns
tCLQX	tHO	Output Hold Time	0.8			ns
tHLCH		HOLD# Active Setup Time (relative to SCLK)	5			ns
tCHHH		HOLD# Active Hold Time (relative to SCLK)	5			ns
tHHCH		HOLD# Not Active Setup Time (relative to SCLK)	5			ns
tCHHL		HOLD# Not Active Hold Time (relative to SCLK)	5			ns
tHHQX	tLZ	HOLD# to Output Low-Z			6	ns
tHLQZ	tHZ	HOLD# to Output High-Z			6	ns
tWHSL(3)		Write Protect Setup Time	20			ns
tSHWL(3)		Write Protect Hold Time	100			ns
tDP		CS# High to Deep Power-down Mode			3	us
tRES1		CS# High to Standby Mode Without Electronic Signature Read			8	us
tRES2		CS# High to Standby Mode with Electronic Signature Read			8	us
tW		Write Status Register Cycle Time		8	12	ms
tReady		Reset recovery time (for erase/program operation except WRSR)	30			us
		Reset recovery time (for WRSR operation)		8	12	ms
tBL		Load memory page data to buffer time(256Byte)			60	us
		Load memory page data to buffer time(512Byte)			120	us
		Load memory page data to buffer time(1024Byte)			240	us
tBC		Clear Page Buffer time			0.3	us

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Table 5-3-2 SPI Read Command Performance Comparison (MHz)

Read command	Dummy Cycles (VCC=2.3V~3.6V)			
	4	6	8	10
FREAD	-	-	120	-
DREAD	-	-	120	-
2READ	104	-	120	-

5.4 AC Characteristics for Program and Erase

Table 5-4 AC parameters from program and erase (Ta=-40°C ~ +85°C)

Symbol	Parameter	2.3V ~ 3.6V			Units
		Min	Typ	Max	
t_{PP}	Page program time (up to 256/512/1024 bytes)		1.6	2.5	ms
t_{PE}	Page erase time		16	25	ms
t_{SE}	Sector erase time		16	25	ms
t_{BE1}	Block erase time for 32K bytes		16	25	ms
t_{BE2}	Block erase time for 64K bytes		16	25	ms
t_{CE}	Chip erase time		256	400	ms

Note

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction.
4. The value guaranteed by characterization, not 100% tested in production.

Figure 5-4 Serial Input Timing

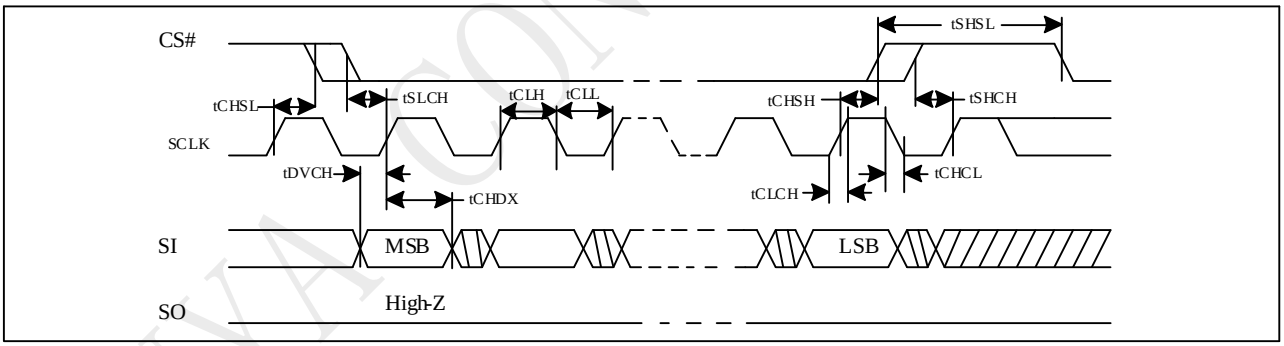
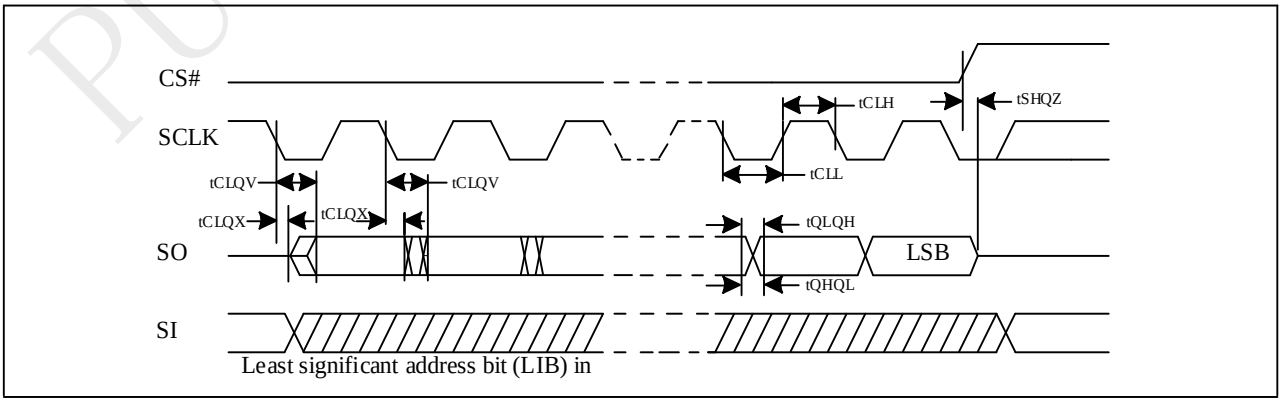


Figure 5-5 Output Timing



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Figure 5-6 Hold Timing

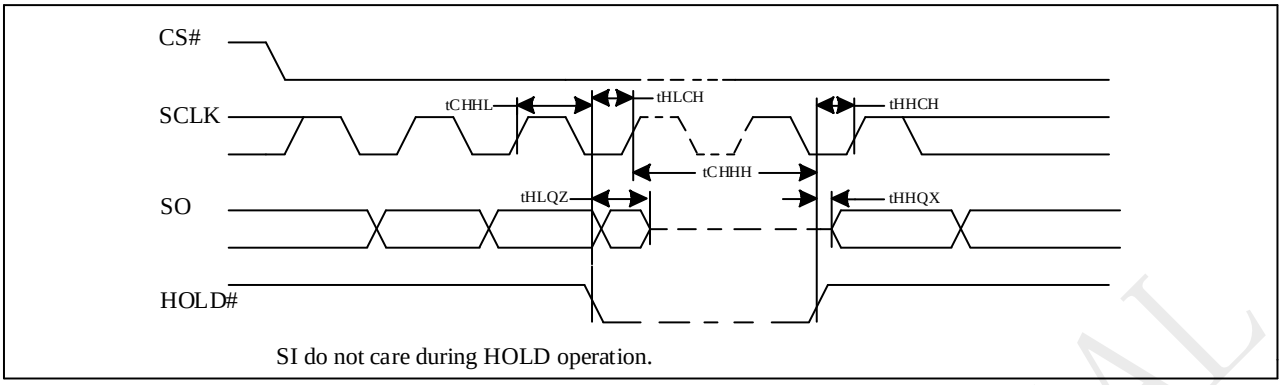
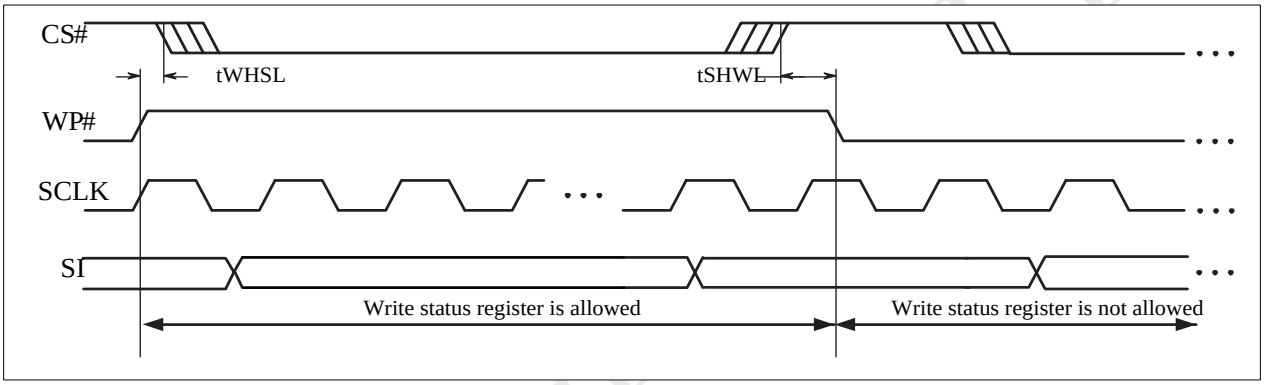


Figure 5-7 WP Timing



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5.5 Operation Conditions

At Device Power-Up and Power-Down

AC timing illustrated in "Figure AC Timing at Device Power-Up" and "Figure Power-Down Sequence" are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 5-8 AC Timing at Device Power-Up

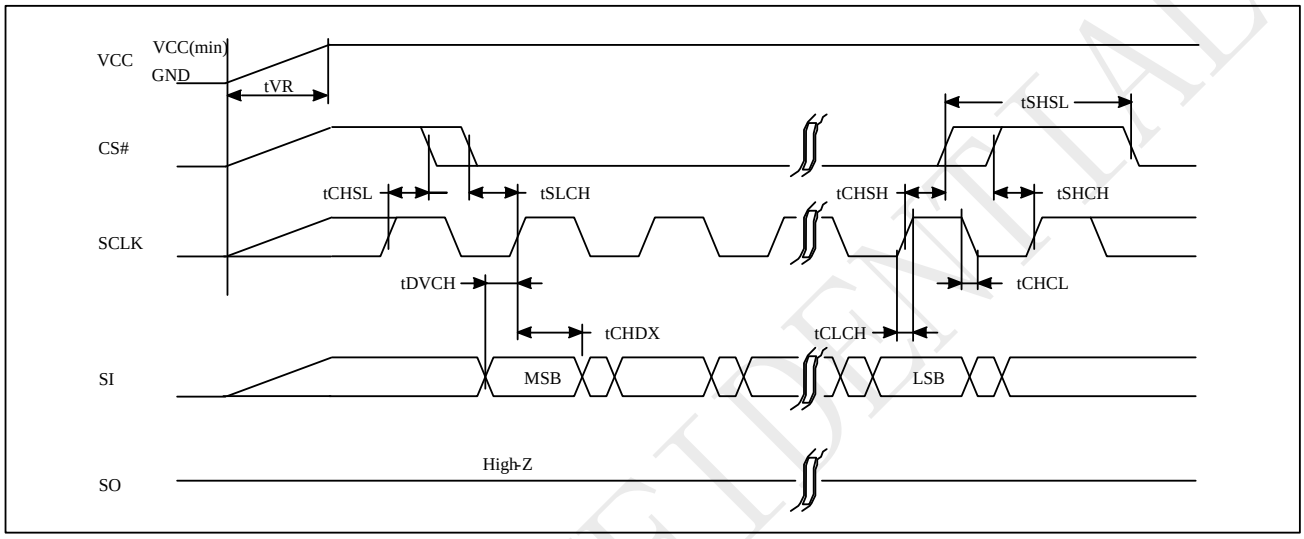
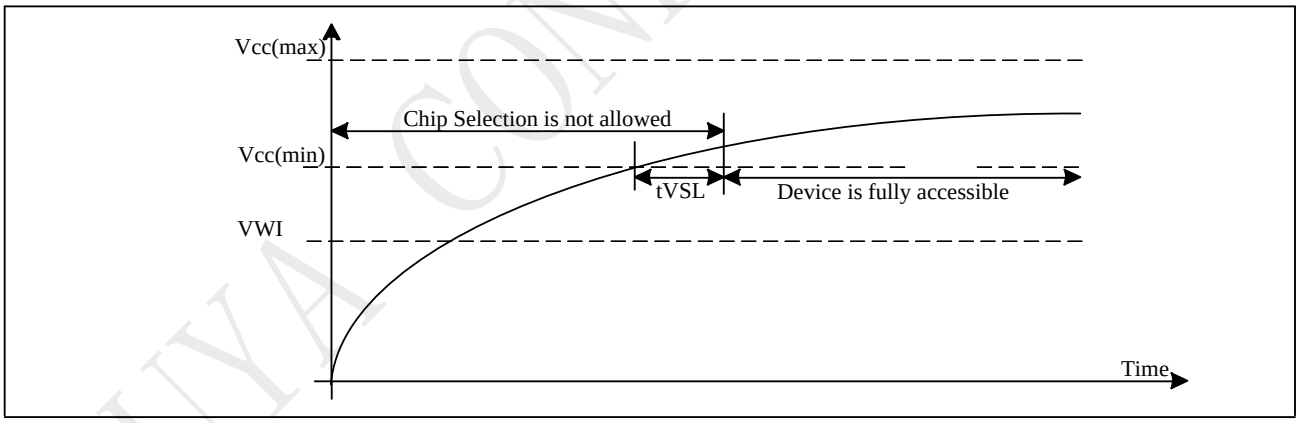


Figure 5-9 Power-up Timing



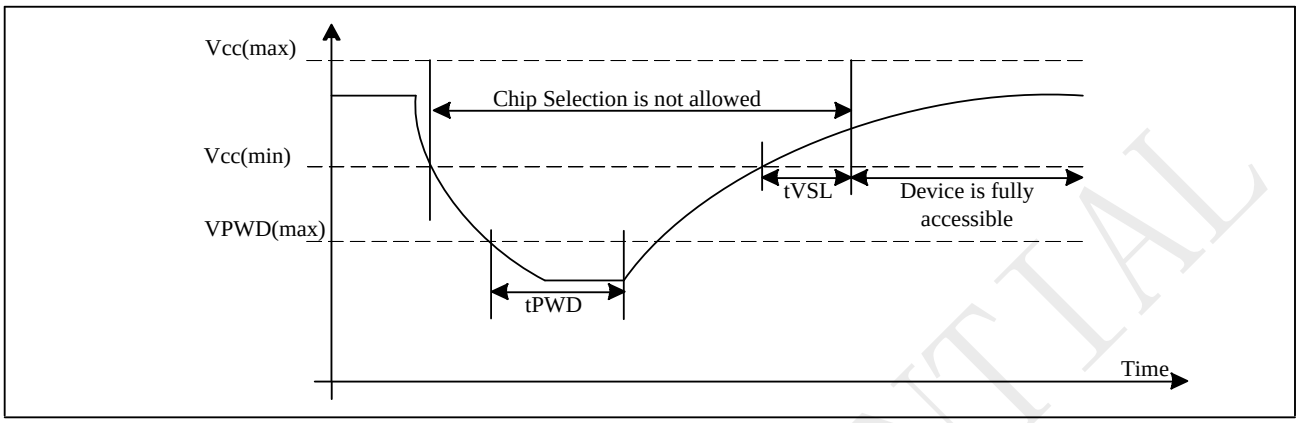
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Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of flash device must below VPWD for at least tPWD timing. Please check the table below for more detail.

Figure 5-10 Power down-up Timing



Symbol	Parameter	Min	Max	Units
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		1	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC (min.) to device operation	150		us
tVR	VCC Rise Time	1	500000	us/V
VWI	Write Inhibit Voltage	1.2	1.55	V

Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFH). The Status Register contains 00H (all Status Register bits are 0), the Configure Register contains 40H, and the Nonvolatile/Volatile Configure Register2 contains FFH.

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6 Data Protection

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.
The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.
In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.
• Power-on reset: to avoid sudden power switch by system power supply transition, the power-on reset may protect the Flash.
• Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
• Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
• Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits define the section of the memory array that can be read but not change.
• Hardware Protection Mode: WP# going low to protected the BP0~BP4bits and SRP0~1bits
• Deep Power-Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except the Release form Deep Power-Down Mode command.

Protected Area Sizes

Table 6-1. P25D64SH Protected Area Sizes (WPS=0, CMP bit = 0)

Status Register					Memory content			
BP4	BP3	BP2	BP1	BP0	Blocks	Adesses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	126 to 127	7E0000h – 7FFFFFh	128KB	Upper 1/64
0	0	0	1	0	124 to 127	7C0000h – 7FFFFFh	256KB	Upper 1/32
0	0	0	1	1	120 to 127	780000h – 7FFFFFh	512KB	Upper 1/16
0	0	1	0	0	112 to 127	700000h – 7FFFFFh	1MB	Upper 1/8
0	0	1	0	1	97 to 127	600000h – 7FFFFFh	2MB	Upper 1/4
0	0	1	1	0	64 to 127	400000h – 7FFFFFh	4MB	Upper 1/2
0	1	0	0	1	0 to 1	000000h – 01FFFFh	128KB	Lower 1/64
0	1	0	1	0	0 to 3	000000h – 03FFFFh	256KB	Lower 1/32
0	1	0	1	1	0 to 7	000000h – 07FFFFh	512KB	Lower 1/16
0	1	1	0	0	0 to 15	000000h – 0FFFFFh	1MB	Lower 1/8
0	1	1	0	1	0 to 31	000000h – 1FFFFFh	2MB	Lower 1/4
0	1	1	1	0	0 to 63	000000h – 3FFFFFh	4MB	Lower 1/2
X	X	1	1	1	0 to 127	000000h – 7FFFFFh	8MB	ALL
1	0	0	0	1	127	7FF000h – 7FFFFFh	4KB	U - 1/2048
1	0	0	1	0	127	7FE000h – 7FFFFFh	8KB	U - 1/1024
1	0	0	1	1	127	7FC000h – 7FFFFFh	16KB	U - 1/512
1	0	1	0	X	127	7F8000h – 7FFFFFh	32KB	U - 1/256

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1	0	1	1	0	127	7F8000h – 7FFFFFh	32KB	U - 1/256
1	1	0	0	1	0	000000h – 000FFFh	4KB	L - 1/2048
1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/1024
1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/512
1	1	1	0	X	0	000000h – 007FFFh	32KB	L - 1/256
1	1	1	1	0	0	000000h – 007FFFh	32KB	L - 1/256

Table 6-2. P25D64SH Protected Area Sizes (WPS=0, CMP bit = 1)

Status Register					Memory content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
X	X	0	0	0	0 to127	000000h - 7FFFFFh	8MB	ALL
0	0	0	0	1	0 to125	000000h –7DFFFFh	8064KB	Lower 63/64
0	0	0	1	0	0 to123	000000h – 7BFFFFh	7936KB	Lower 31/32
0	0	0	1	1	0 to119	000000h –77FFFFh	7680KB	Lower 15/16
0	0	1	0	0	0 to111	000000h –6FFFFFh	7MB	Lower 7/8
0	0	1	0	1	0 to95	000000h –5FFFFFh	6MB	Lower 3/4
0	0	1	1	0	0 to63	000000h - 3FFFFFh	4MB	Lower 1/2
0	1	0	0	1	2to127	020000h - 7FFFFFh	8064KB	Upper 63/64
0	1	0	1	0	4to127	040000h - 7FFFFFh	7936KB	Upper 31/32
0	1	0	1	1	8to127	080000h - 7FFFFFh	7680KB	Upper 15/16
0	1	1	0	0	16to127	100000h - 7FFFFFh	7MB	Upper 7/8
0	1	1	0	1	32to127	200000h - 7FFFFFh	6MB	Upper 3/4
0	1	1	1	0	64to127	400000h - 7FFFFFh	4MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to127	000000h – 7FEFFFh	8188KB	L - 2047/2048
1	0	0	1	0	0 to 127	000000h – 7FDFFFh	8184KB	L - 1023/1024
1	0	0	1	1	0 to127	000000h – 7FBFFFh	8176KB	L - 511/512
1	0	1	0	X	0 to 127	000000h – 7F7FFFh	8160KB	L – 255/256
1	0	1	1	0	0 to 127	000000h – 7F7FFFh	8160KB	L - 255/256
1	1	0	0	1	0 to 127	001000h – 7FFFFFh	8188KB	L - 2047/2048
1	1	0	1	0	0 to 127	002000h – 7FFFFFh	8184KB	L - 1023/1024
1	1	0	1	1	0 to 127	004000h – 7FFFFFh	8176KB	L - 511/512
1	1	1	0	X	0 to 127	008000h – 7FFFFFh	8160KB	L – 255/256
1	1	1	1	0	0 to 127	008000h – 7FFFFFh	8160KB	L - 255/256

Note:

1. X=don't care

2. If any erase or program command specifies a memory that contains protected data portion, this command will be ignored.

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7 Device Operation

Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

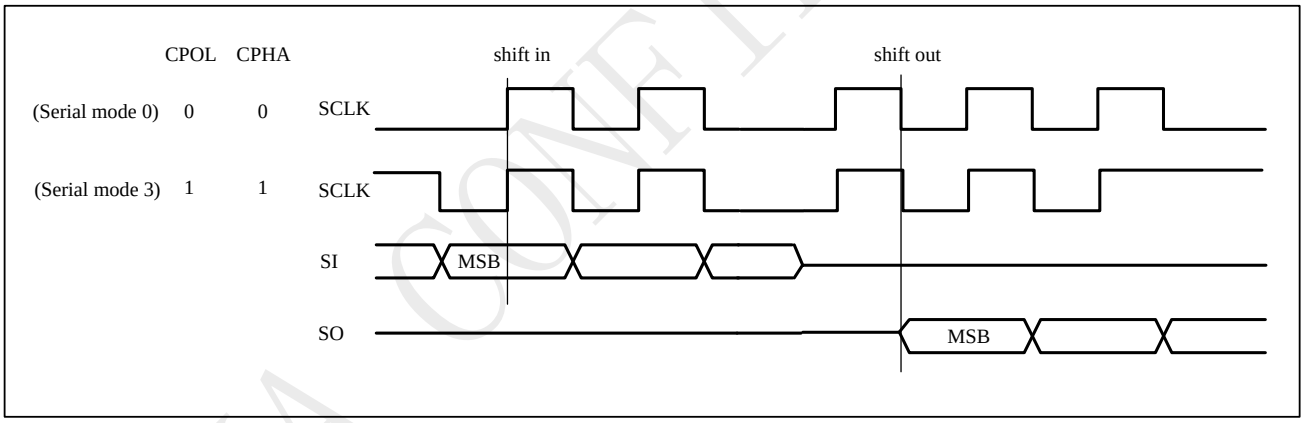
When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of serial peripheral interface mode 0 and mode 3 is shown as Figure 8-1.

For the following instructions: RDID, RDSR, RDSR2, RDCR2, VRDCR, RDSCUR, READ, FREAD, DREAD, 2READ, RDSFDP, RES, REMS, DREMS, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, WRCR, WRCR2, VWRCR, PE, SE, BE32K, BE, CE, PP, DP, ERSCUR, PRSCUR, RSTEN, RST, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

During the progress of Write Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Register, Program, Erase.

Figure 8-1 Serial Peripheral Interface Modes Supported

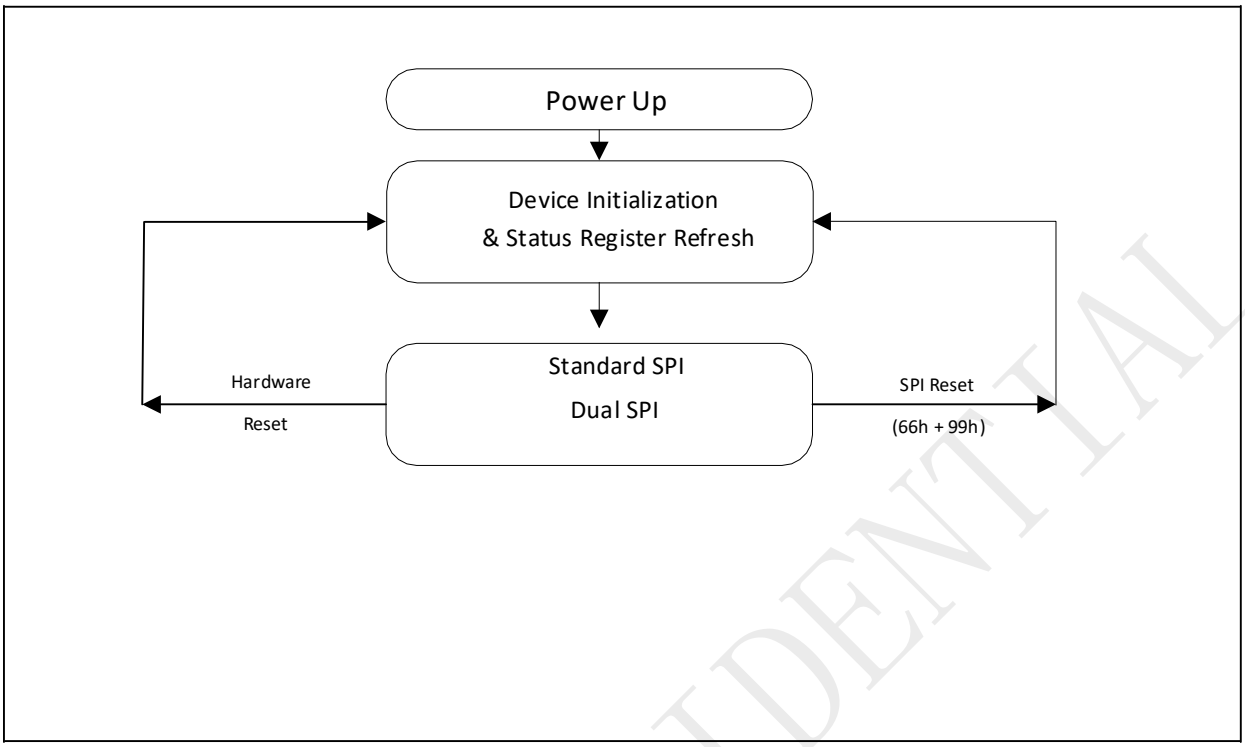


Note:

CPOL indicates clock polarity of serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which serial mode is supported.

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Standard SPI

The P25D64SH features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The P25D64SH supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH, BBH, 92H) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Software Reset

The P25D64SH can be reset to the initial power-on state by a software Reset sequence, either in SPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS (tReady) to reset. No command will be accepted during the reset period.

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8 Memory Address Mapping

The memory array can be erased in three levels of granularity including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions.

Each device has	Each block has	Each sector has	Each page has	
8M	64/32K	4K	256	bytes
32K	256/128	16	-	pages
2048	16/8	-	-	sectors
128/256	-	-	-	blocks

P25D64SH Memory Organization

Block	Sector	Address range	
127	2047	7FF000H	7FFFFFH
	……	……	……
	2032	7F0000H	7F0FFFH
126	2031	7EF000H	7EFFFFH
	……	……	……
	2016	7E0000H	7E0FFFH
……	……	……	……
	……	……	……
	……	……	……
……	……	……	……
	……	……	……
	……	……	……
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

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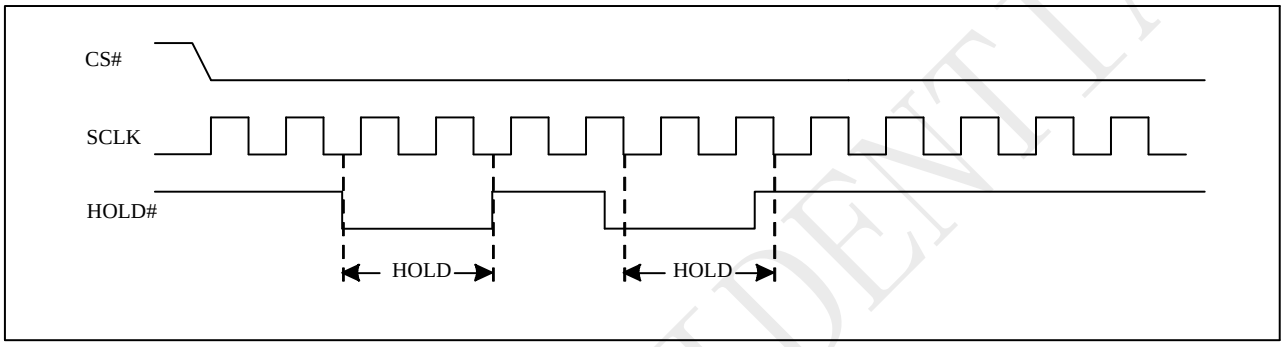
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9 Hold Feature

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

Figure 9-1 Hold Condition Operation



During the HOLD operation, the Serial Data Output (SO) is high impedance when Hold# pin goes low and will keep high impedance until Hold# pin goes high. The Serial Data Input (SI) is don't care if both Serial Clock (SCLK) and Hold# pin goes low and will keep the state until SCLK goes low and Hold# pin goes high. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

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10 Commands

10.1 Commands listing

Figure 10-1 Command set (Standard/Dual/Quad SPI)

Commands	Abbr.	Code	ADR Bytes	DMY Cycles	Data Bytes	Function description
Read						
Read Array (fast)	FREAD	0BH	3	8	1+	n bytes read out until CS# goes high
Read Array (low power)	READ	03H	3	0	1+	n bytes read out until CS# goes high
Read Dual Output	DREAD	3BH	3	8	1+	n bytes read out by Dual output
Read 2IO	2READ	BBH	3	4(8)	1+	n bytes read out by 2IO
Program and Erase						
Page Erase	PE	81H	3	0	0	erase selected page
Sector Erase (4K bytes)	SE	20H	3	0	0	erase selected sector
Block Erase (32K bytes)	BE32	52H	3	0	0	erase selected 32K block
Block Erase (64K bytes)	BE	D8H	3	0	0	erase selected 64K block
Chip Erase	CE	60H/C7H	0	0	0	erase whole chip
Page Program	PP	02H	3	0	1+	program selected page
Protection						
Write Enable	WREN	06H	0	0	0	sets the write enable latch bit
Write Disable	WRDI	04H	0	0	0	resets the write enable latch bit
Volatile SR Write Enable	VWREN	50H	0	0	0	Write enable for volatile SR
Security						
Erase Security Registers	ERSCUR	44H	3	0	0	Erase security registers
Program Security Registers	PRSCUR	42H	3	0	1+	Program security registers
Read Security Registers	RDSCUR	48H	3	8	1+	Read value of security register

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Command set (Standard/Dual/Quad SPI)

Commands	Abbr.	Code	ADR Bytes	DMY cycle	Data Bytes	Function
Status Register						
Read Status Register	RDSR	05h	0	0	1	read out status register
Read Status Register-1	RDSR1	35h	0	0	1	Read out status register-1
Read Configure Register	RDCR	15h	0	0	1	Read out configure register
Write Status Register	WRSR	01h	0	0	1-2	Write data to status registers-0 and status registers-1
Write Status Register-1	WRSR1	31h	0	0	1	Write data to status registers-1
Write Configure Register	WRCR	11H	0	0	1	Write data to configure register
Other Commands						
Reset Enable	RSTEN	66H	0	0	0	Enable reset
Reset	RST	99H	0	0	0	Reset
Read Manufacturer/device ID	RDID	9FH	0	0	1 to 3	output JEDEC ID: 1-byte manufacturer ID & 2-byte device ID
Read Manufacture ID	REMS	90H	3	0	1+	Read manufacturer ID/device ID data
Dual Read Manufacture ID	DREMS	92H	3	4	1+	Dual output read manufacture/device ID
Deep Power-down	DP	B9H	0	0	0	enters deep power-down mode
Release Deep Power-down/Read Electronic ID	RDP/RES	ABH	3	0	1	Read electronic ID data
Set burst length	SBL	77H	0	0	0	Set burst length
Read SFDP	RDSFDP	5AH	3	8	1+	Read SFDP parameter
Release read enhanced	RSEN	FFH				Release from read enhanced
Read unique ID	RUID	4BH	3	8	1+	Read unique ID
No Operation	NOP	00H	0	0	0	

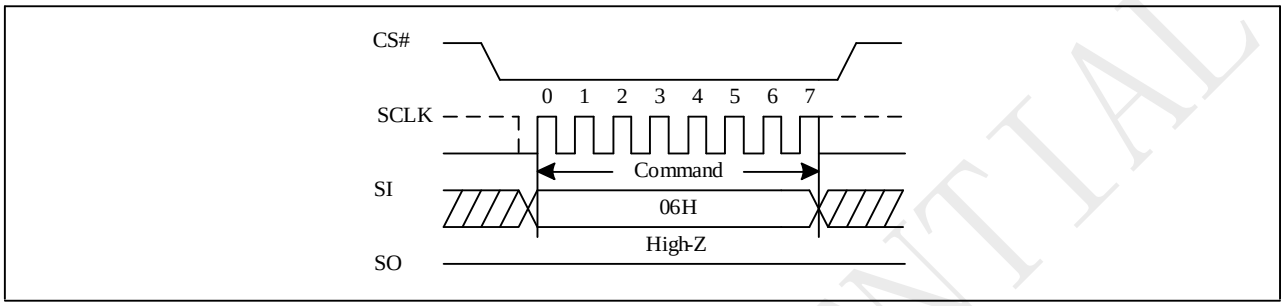
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10.2 Write Enable (06H)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL)bit. For those instructions like PP, PE, SE, BE32K, BE, CE, WRSR, WRSR1, WRCR, ERSCUR, PRSCUR which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.
The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high.

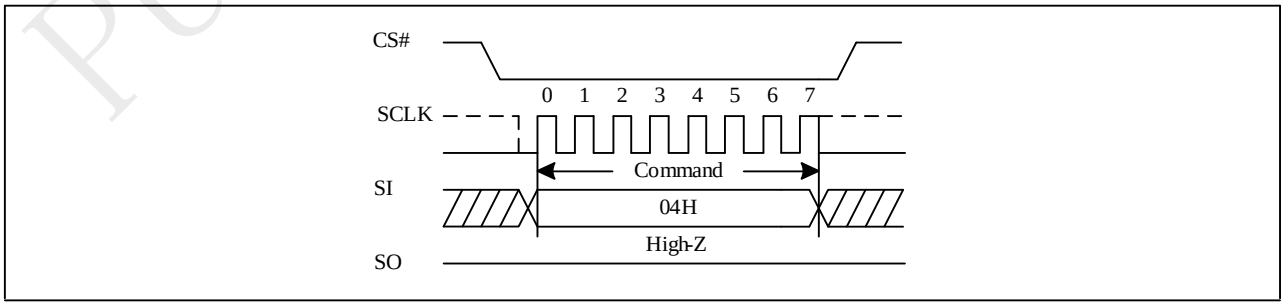
Figure 10-2 Write Enable (WREN) Sequence (Command 06)



10.3 Write Disable (04H)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.
The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high.
The WEL bit is reset by following situations:
- Power-up
- Write Disable (WRDI) instruction completion
- Write Register (WRSR/WRSR1/WRCR) instruction completion
- Page Program (PP) instruction completion
- Page Erase (PE) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE32K, BE) instruction completion
- Chip Erase (CE) instruction completion
- Erase Security Register (ERSCUR) instruction completion
- Program Security Register (PRSCUR) instruction completion
- Reset (RST) instruction completion

Figure 10-3 Write Disable (WRDI) Sequence (Command 04)



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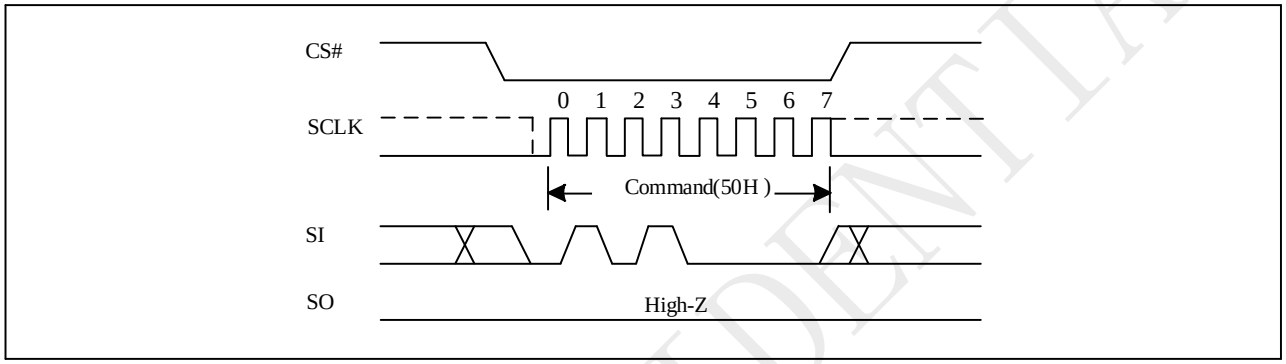
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10.4 Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

The sequence of issuing Write Enable for Volatile Status Register instruction is: CS# goes low→ sending Write Enable for Volatile Status Register instruction code→ CS# goes high.

Figure 10-4 Write Enable for Volatile Status Register Sequence (Command 50h)

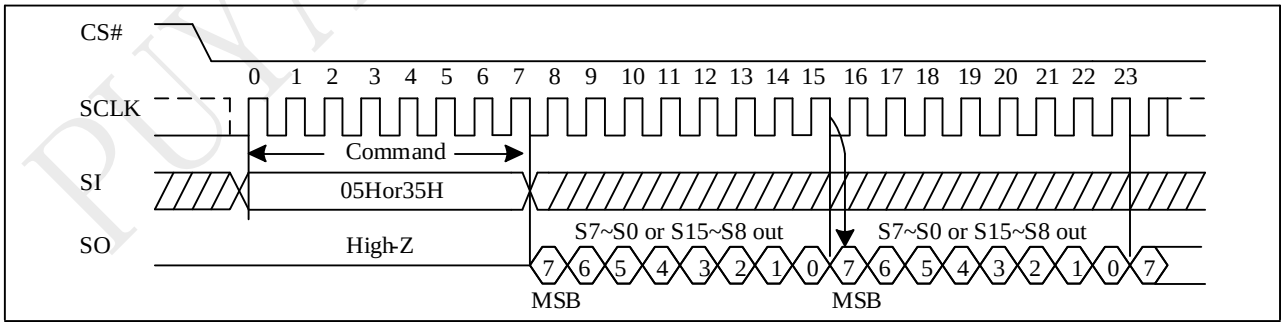


10.5 Read Status Register (05H/35H)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress. For command code “05H”, the SO will output Status Register-0 bits S7~S0. The command code “35H”, the SO will output Status Register-1 bits S15~S8.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO. The SIO [3:1] are "don't care".

Figure 10-5 Read Status Register (RDSR) Sequence (Command 05 or 35)



Status Register-0

BIT	S7	S6	S5	S4	S3	S2	S1	S0
Definition	SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP
Volatile	N	N	N	N	N	N	R	R
Default	0	0	0	0	0	0	0	0

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Status Register-1

BIT	S15	S14	S13	S12	S11	S10	S9	S8
Definition	—	CMP	LB3	LB2	LB1	EP_FAIL	—	SRP1
Volatile	R	N	O	O	O	R	N	N
Default	0	0	0	0	0	0	0	0

Note：V for volatile; N for Non-volatile; O for One Time Program; R for Read Only.

The definition of the status register bits is as below:

WIP bit.

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table “Protected Area Sizes”) becomes protected against Page Program (PP), Page Erase (PE), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, only if the Block Protect (BP4, BP3, BP2, BP1 and BP0) are set to “None protected”.

SRP1, SRP0 bits.

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one-time programmable protection

SRP1	SRP0	WP#	Status Register	Description
0	0	x	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1. (Default)
0	1	0	Hardware Protected	WP#=0, the Status Register locked and can’t be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	x	Power Supply Lock-Down (1)	Status Register is protected and can’t be written to again until the next Power-Down, Power-Up cycle.
1	1	x	One Time Program (2)	Status Register is permanently protected and can’t be written to.

NOTE:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact PUYA for details.

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EP_FAIL bit.

The Erase/Program Fail bit is a read only bit which shows the status of the last Program/Erase operation. The bit will be set to "1" if the program/erase operation failed or interrupted by reset or the program/erase region was protected. It will be automatically cleared to "0" if the next program/erase operation succeeds. Please note that it will not interrupt or stop any operation in the flash memory.

LB3, LB2, LB1, bits.

The LB3, LB2, LB1, bits are non-volatile One Time Program (OTP) bits in Status Register (S13-S11) that provide the write protect control and status to the Security Registers. The default state of LB3-LB1are0, the security registers are unlocked. The LB3-LB1 bits can be set to 1 individually using the Write Register instruction. The LB3-LB1bits are One Time Programmable, once its set to 1, the Security Registers will become read-only permanently.

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the table “Protected Area Size” for details. The default setting is CMP=0.

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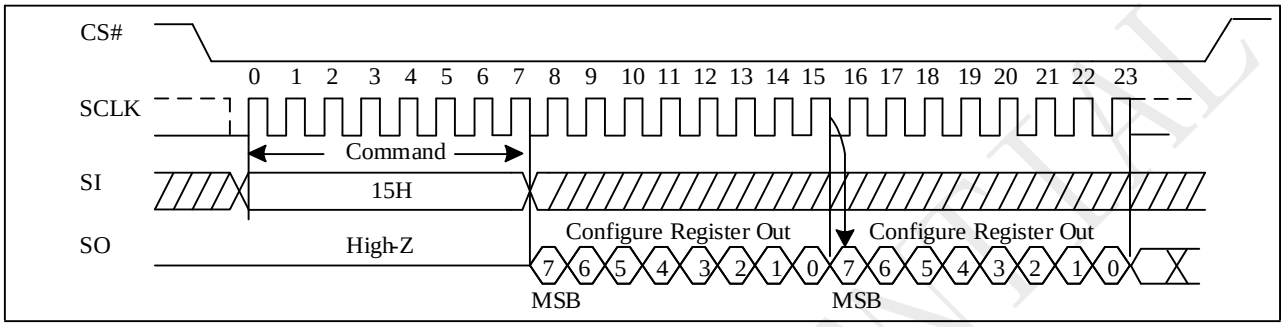
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10.6 Read Configure Register (15H)

The RDCR instruction is for reading Configure Register Bits. The Read Configure Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configure Register data out on SO. The SIO [3:1] are "don't care".

Figure 10-6 Read Status Register (RDCR) Sequence (Command 15h)



Configure Register

BIT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Definition	HOLD/RST	reserved	reserved	MPM1	MPM0	reserved	DC	reserved
Volatile	N	-	-	V	V	-	V	-
Default	0	0	0	0	0	0	0	0

Note：V for volatile; N for Non-volatile; R for Read Only.

HOLD/RST bit.

The HOLD/RST bit is a nonvolatile Read/Write bit in the Configure Register which is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET.

MPM bit.

The Multi Page Mode (MPM) bits are volatile Read/Write bits which allows Quad/Dual Page operation.

MPM1, MPM0	Page Size
0,0(default)	256byte
0,1	512byte
1,0	1024byte
1,1	Reserved

The page size is defined by MPM bits as above table.

When the MPM bits are set to (0,0) (Default) the page size is 256bytes. When the MPM bits are set to (0,1), the page size is 512bytes. When the MPM bits are set to (1,0), the page size is 1024bytes.

This bit controls the page programming buffer address wrap point. Legacy SPI devices generally have used a 256 Byte page programming buffer and defined that if data is loaded into the buffer beyond the 256 Byte locations, the address at which additional bytes are loaded would be wrapped to address zero of the buffers. The P25D64SH provides a 512/1024 Byte page programming buffer that can increase programming performance. For legacy software compatibility, this configuration bit provides the option to continue the wrapping behavior at the 256 Byte boundary or to enable full use of the available 512/1024 Byte buffer by not wrapping the load address at the 256 Byte boundary. When the MPM bits are set to (0,1), the page erase

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instruction (81h) will erase the data of the chosen Dual Page to be "1". When the MPM bits are set to (1,0), the page erase instruction (81h) will erase the data of the chosen Quad Page to be "1".

When ERSCUR or PRSCUR, MPM1/MPM0 must be set to 00.

DC bit

The Dummy Cycle (DC) bit is a volatile bit. The Dummy Cycle (DC) bit can be used to configure the number of dummy clocks for “SPI 2 X IO Read (BBH)” command.

Table Dummy Cycle Table

		DC bit	Number of dummy	Max Read Freq.
SPI command	BBH SPI	0(default)	4	104MHz
		1	8	120MHz

10.7 Write Status Register (01H/31H)

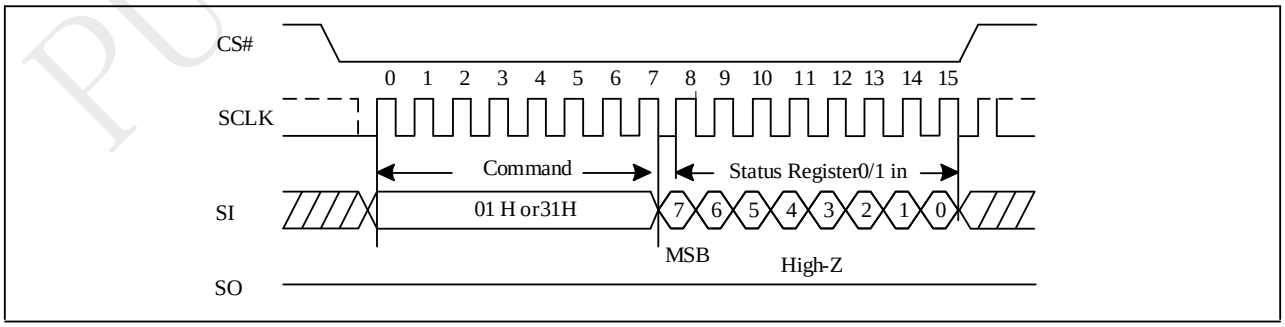
The Write Status Register (WRSR) and Write Status Register-1 (WRSR1) commands allow new values to be written to the Status Register-0 and Status Register-1. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The WRSR and WRSR1 command has no effect on S15, S10, S1 and S0 of the Status Register. CS# must be driven high after the eighth bit or sixteen bit (just for WRSR command) of the data byte has been latched in. If not, the command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The WRSR command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table6-1 and Table6-2. The WRSR and WRSR1 commands also allow the user to set or reset the Status Register Protect (SRP0 and SRP1) bits respectively in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP0 and SRP1) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high.

Figure 10-7 Write Status Register (WRSR) Sequence (Command 01h or 31h)

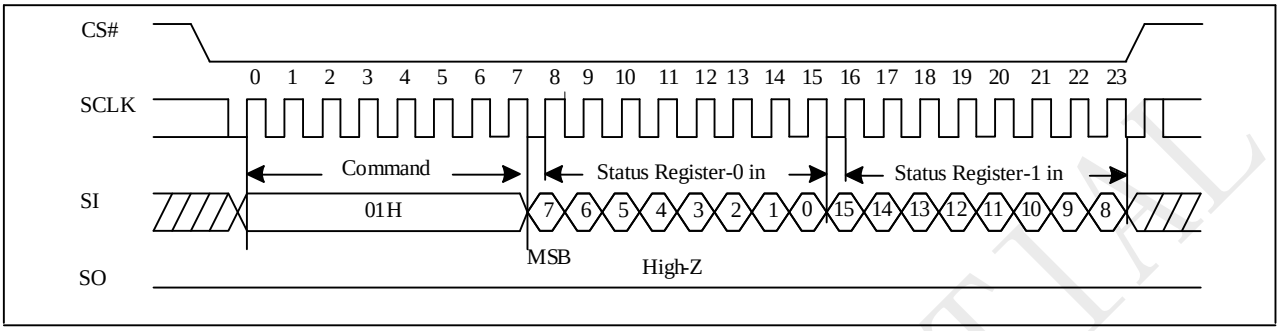


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To be backward compatible to Puya's previous serial flash product, The Write Status Register (WRSR) command also support to write Status Register-0 and Status Register-1 in same time. To complete this function, CS# must be driven high after the sixteenth bit of the data byte has been latched in. If CS# is driven high after the eighth clock, the Write Status Register (01h) command will only program the Status Register-0, the Status Register-1 will not be affected (Previous product will clear CMP bits).

Figure 10-7b Write Status Register (WRSR) with 2 Byte data Sequence (SPI)



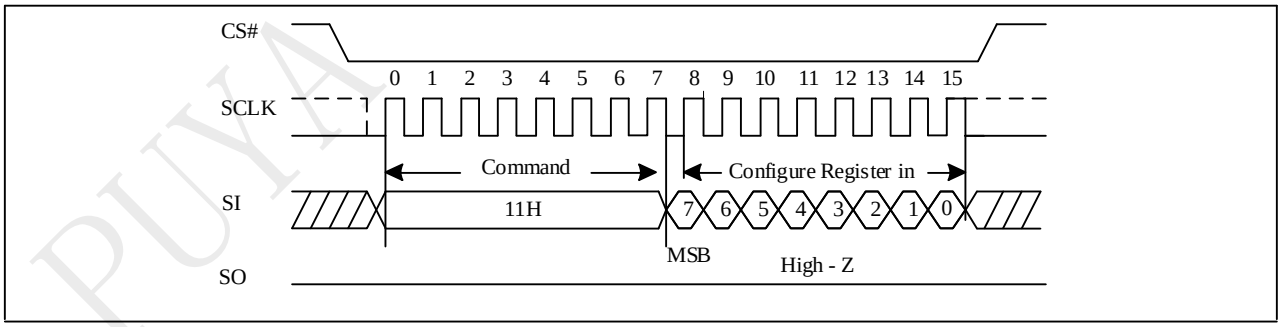
10.8 Write Configure Register (11H)

The Write Configure Register (WRCR) command allows new values to be written to the Configure Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The sequence of issuing WRCR instruction is: CS# goes low→ sending WRCR instruction code→ Configure Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Configure Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 10-8 Write Configure Register (WRCR) Sequence (Command 11h)



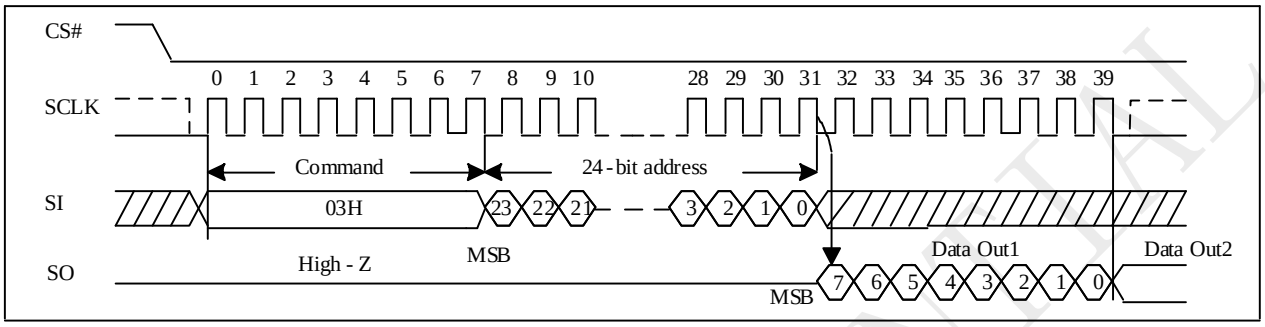
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10.9 Read Data Bytes (03H)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

Figure 10-9 Read Data Bytes (READ) Sequence (Command 03h)

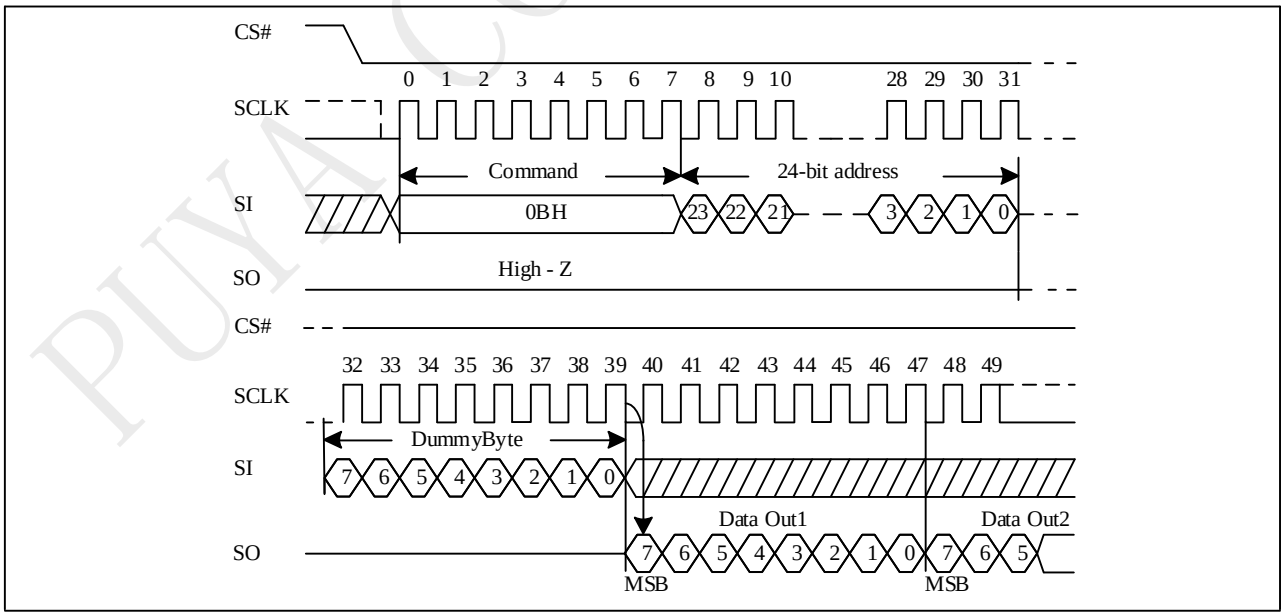


10.10 Fast Read (0BH)

The FAST READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FREAD instruction. The address counter rolls over to 0 when the highest address has been reached.

While Program/Erase/Write Status Register cycle is in progress, FREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10-10Fast Read (FREAD) Sequence (Command 0Bh)



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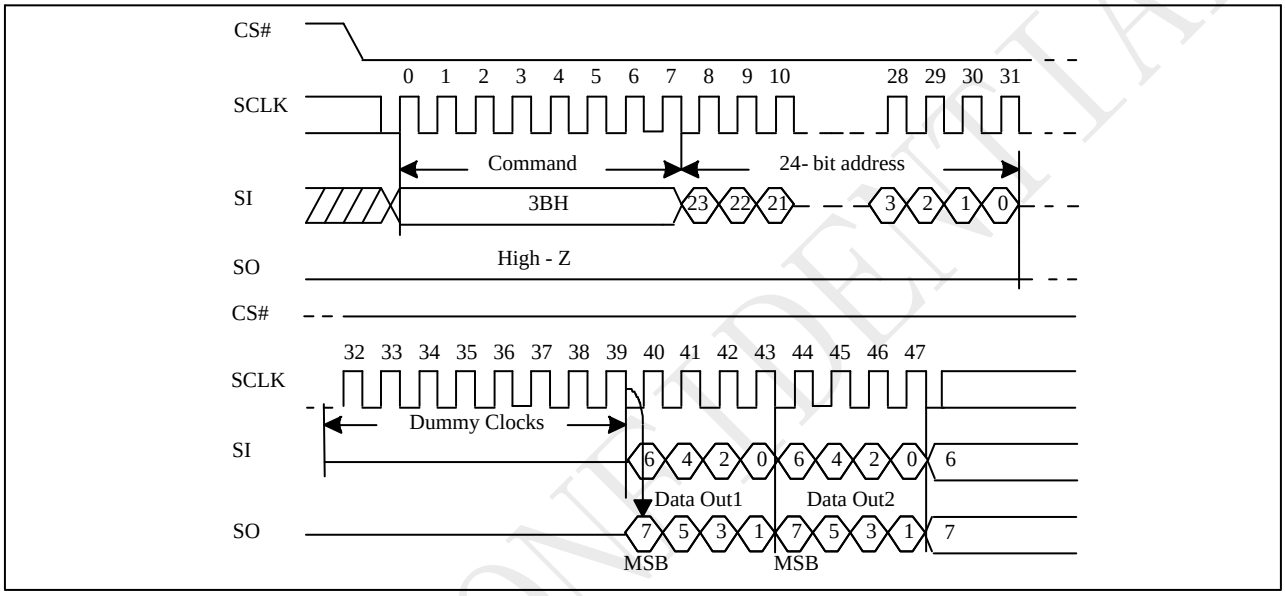
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10.11 Dual Read (3BH)

The DREAD instruction enables double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10-11 Dual Read Mode Sequence (Command 3Bh)



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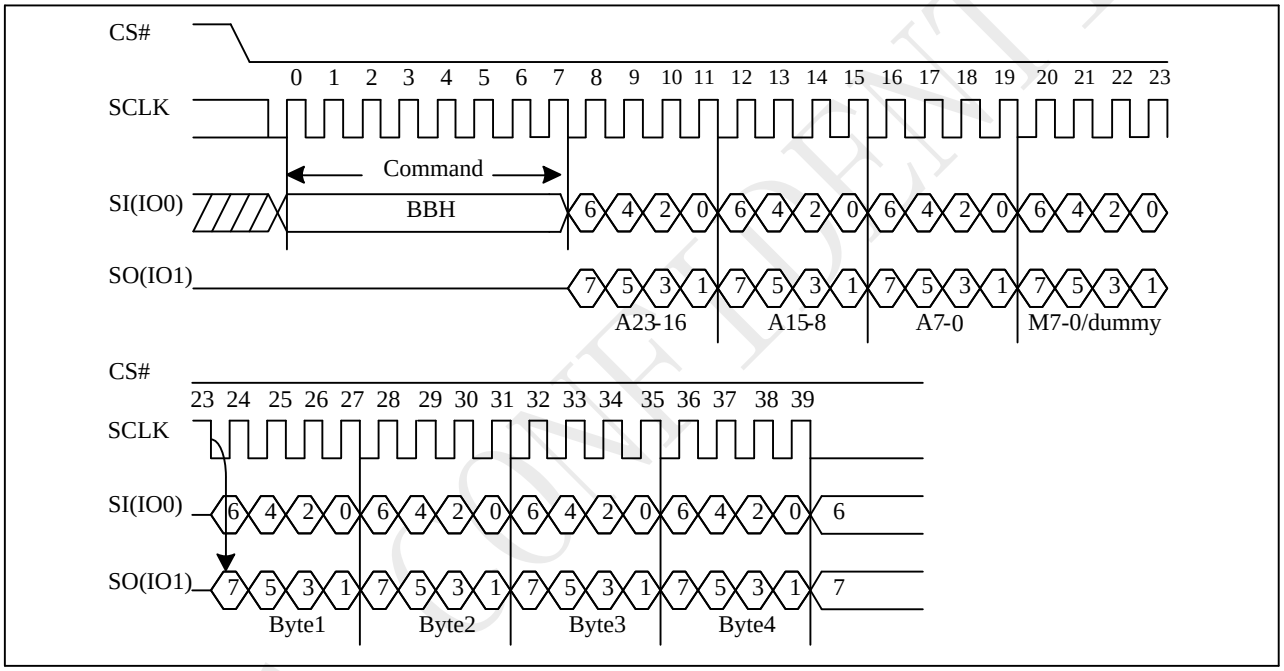
10.12 2IO Read (BBH)

The 2READ instruction enables Double Transfer Rate of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached.

Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10-12 2IO Read Sequence (Command BBM5-4 ≠ (1,0))



Note:
1. M [5-4] = (1,0) is inhibited.

2IO Continuous Read

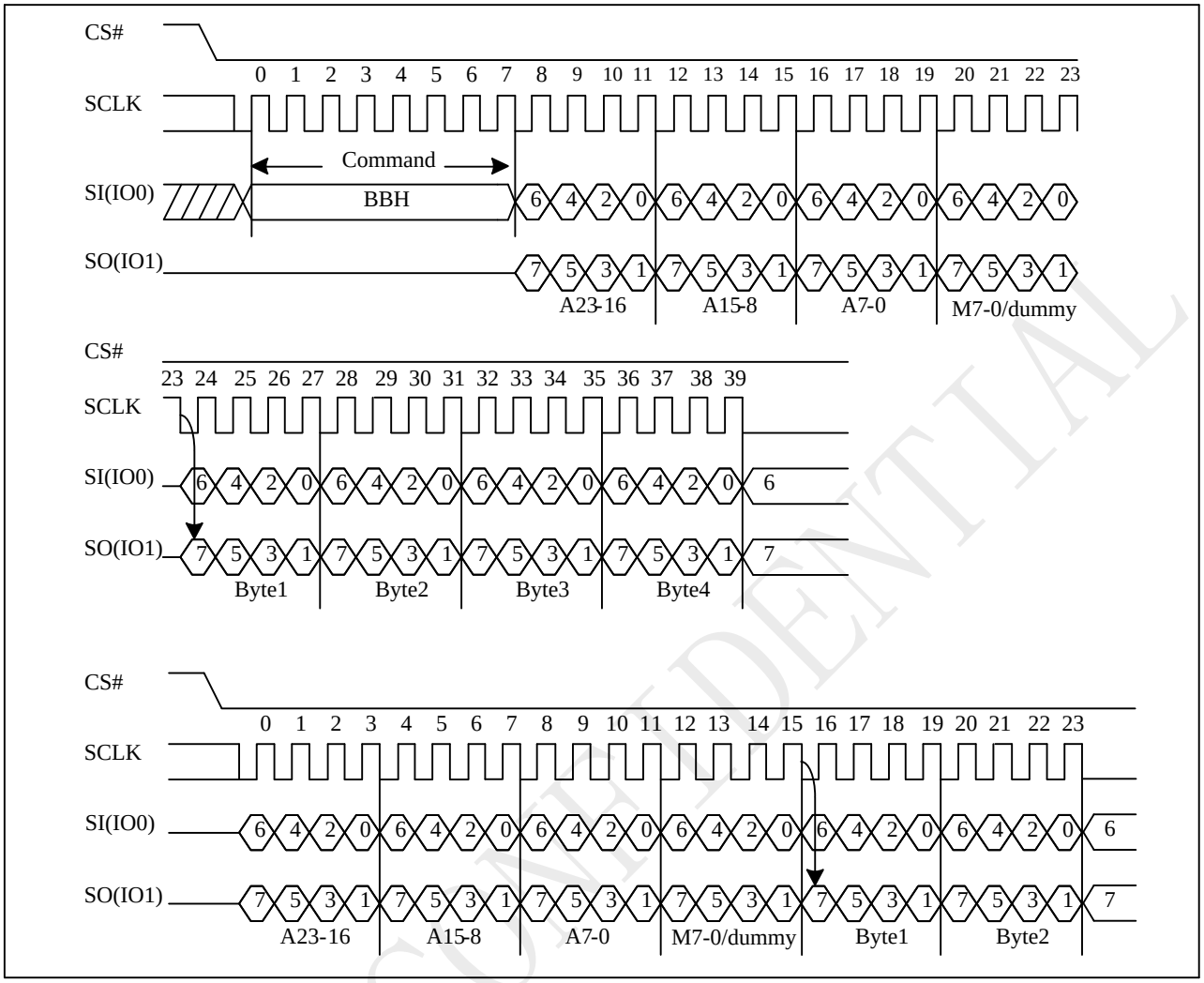
"BBH" command supports 2IO Continuous Read which can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next 2IO Read command (after CS# is raised and then lowered) does not require the BBH command code.

If the "Continuous Read Mode" bits (M5-4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command.

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Figure 10-12a 2IO Continue Read (M5-4 = (1,0))



Note:

1. 2IO Continue Read, if M5-4 = 1, 0. If not using Continue Read recommend to set M5-4 ≠ 1, 0.

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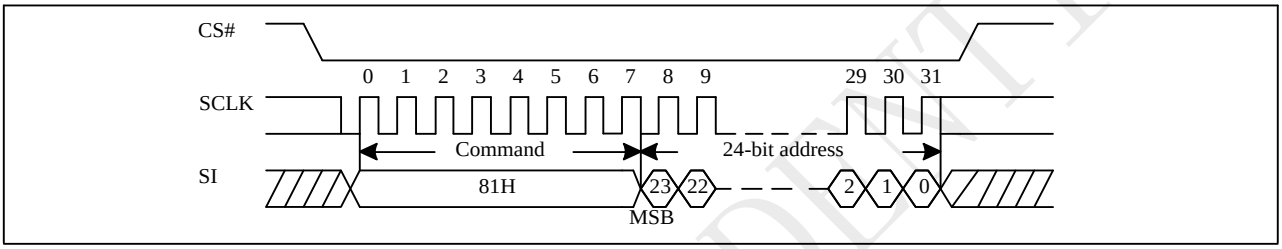
10.13 Page Erase (81H)

The Page Erase (PE) instruction is for erasing the data of the chosen Page to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Erase (PE). The self-timed Page Erase Cycle time (tPE) is initiated as soon as Chip Select (CS#) goes high. The Write in progress (WIP) bit still can be check out during the Page Erase cycle is in progress. The WIP sets 1 during the tPE timing, and sets 0 when Page Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

To perform a Page Erase with the standard page size (256 bytes), an instruction of 81h must be clocked into the device followed by three address bytes comprised of 2-page address bytes that specify the page in the main memory to be erased, and 1 dummy byte.

The sequence of issuing PE instruction is: CS# goes low→ sending PE instruction code→3-byte address on SI→ CS# goes high.

Figure 10-13 Page Erase Sequence (Command 81h)



10.14 Sector Erase (20H)

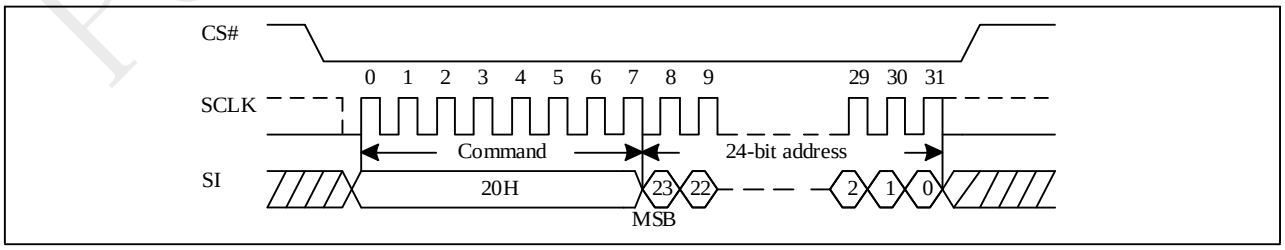
The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL)bit before sending the Sector Erase (SE).

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP4, BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

Any address of the sector is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

Figure 10-14 Sector Erase (SE) Sequence (Command 20h)



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10.15 Block Erase (52H)

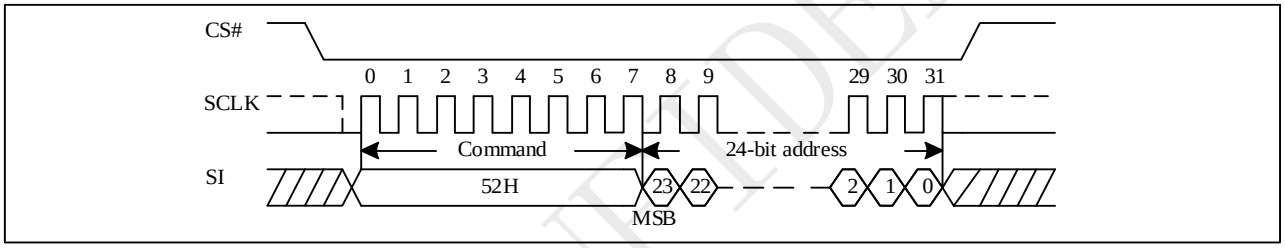
The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K).

The self-timed Block Erase Cycle time (tBE1) is initiated as soon as Chip Select (CS#) goes high. The Write in progress (WIP) bit still can be check out during the Block Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Any address of the block is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP4, BP3, BP2, BP1, BP0 bits, the array data will be protected (no change) and the WEL bit still be reset.

Figure 10-15 Block Erase 32K(BE32K) Sequence (Command 52h)



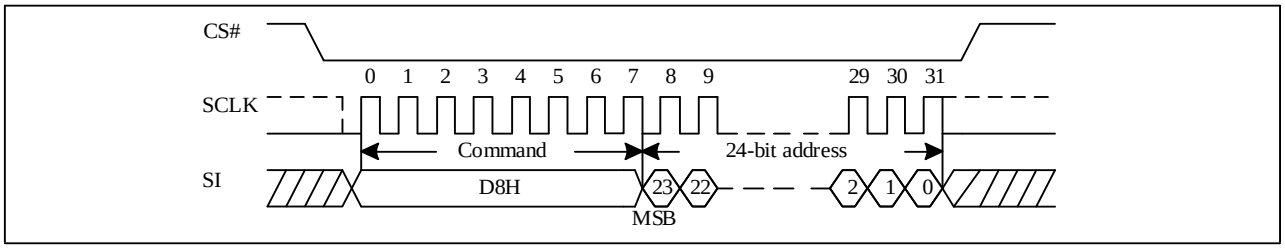
10.16 Block Erase (D8H)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE).

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Block Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP4, BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

Any address of the block is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Figure 10-16 Block Erase (BE) Sequence (Command D8h)



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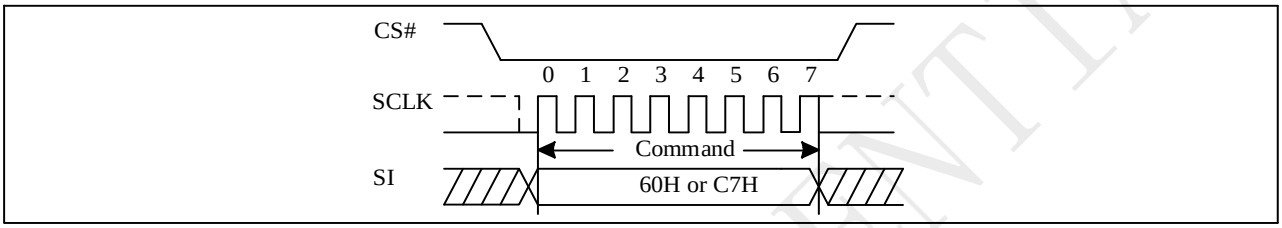
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10.17 Chip Erase (60H/C7H)

The Chip Erase (CE) instruction is for erasingthedataofthewholechiptobe"1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP4, BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when all Block Protect (BP4, BP3, BP2, BP1, BP0) are set to “None protected”.

Figure 10-17 Chip Erase (CE) Sequence (Command 60 or C7)



10.18 Page Program (02H)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0(The eight least significant address bits) should be set to 0.If the eight least significant address bits(A7-A0) are not all 0,all transmitted data going beyond the end of the current page are programmed from the start address of the same page(from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page without effect on other address of the same page.

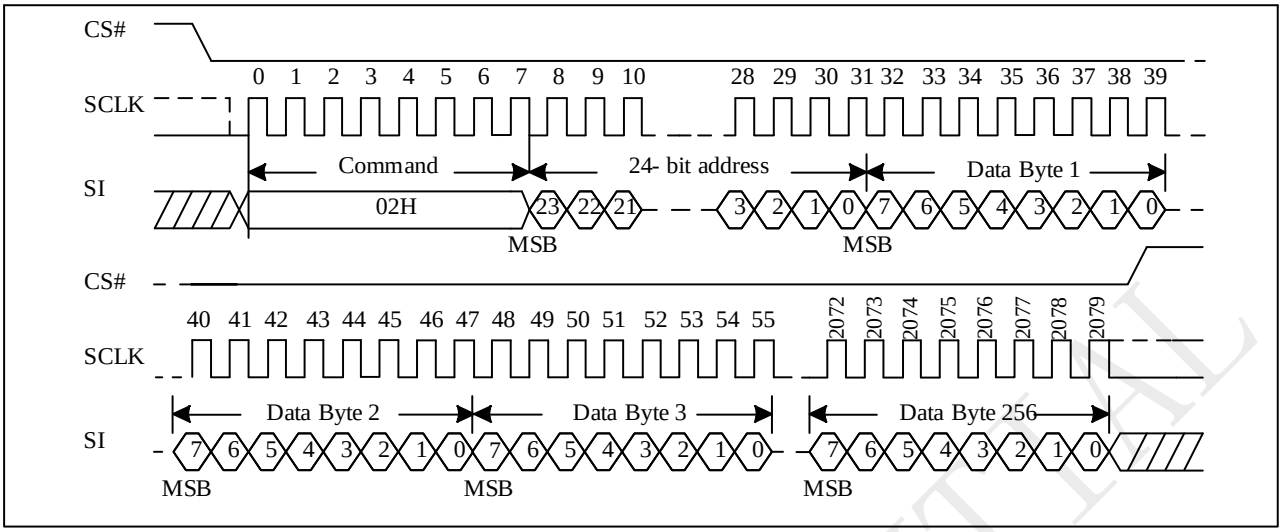
The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP4, BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed. The SIO [3:1] are "don't care".

The CS# must be kept low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

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Figure 10-18 Page Program (PP) Sequence (Command 02h)



10.19 Erase Security Registers (44H)

The product provides three 1024-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

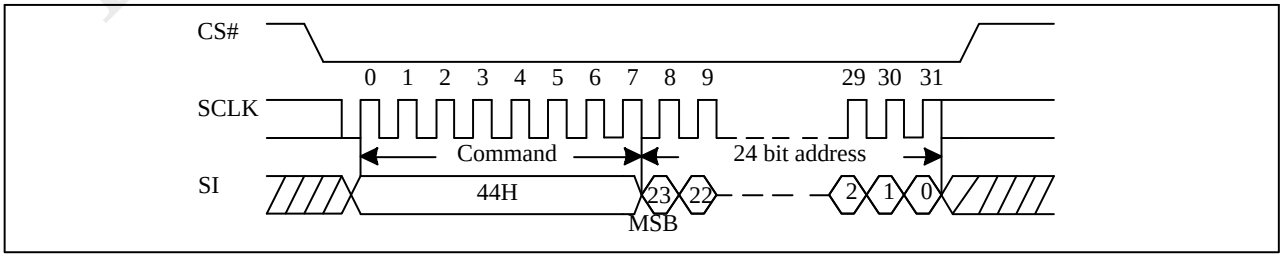
The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. The Security Registers Lock Bit (LB3-1) in the Status Register can be used to OTP protect the security registers.

Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-16	A15-12	A11-10	A9-0
Security Register #1	00H	0001	00	Don't care
Security Register #2	00H	0010	00	Don't care
Security Register #3	00H	0011	00	Don't care

Figure 10-19 Erase Security Registers (ERSCUR) Sequence (Command 44)



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10.20 Program Security Registers (42H)

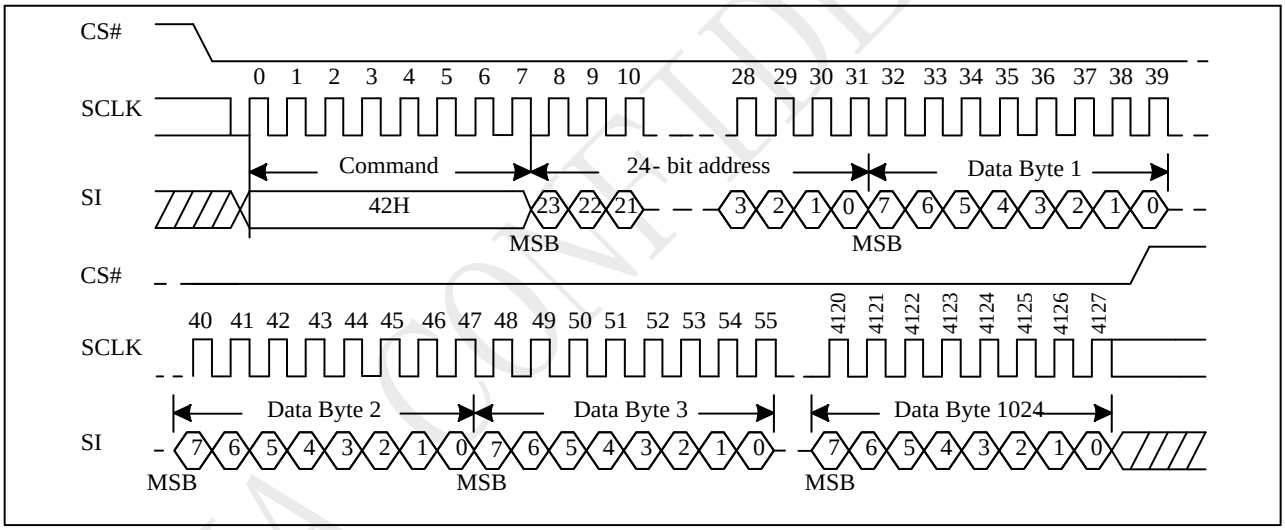
The Program Security Registers command is similar to the Page Program command. It allows from 1 to 1024 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command.

As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed.

If the Security Registers Lock Bit (LB3-1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-16	A15-12	A11-10	A9-0
Security Register #1	00H	0001	00	Byte Address
Security Register #2	00H	0010	00	Byte Address
Security Register #3	00H	0011	00	Byte Address

Figure 10-20 Program Security Registers (PRSCUR) Sequence (Command 42h)



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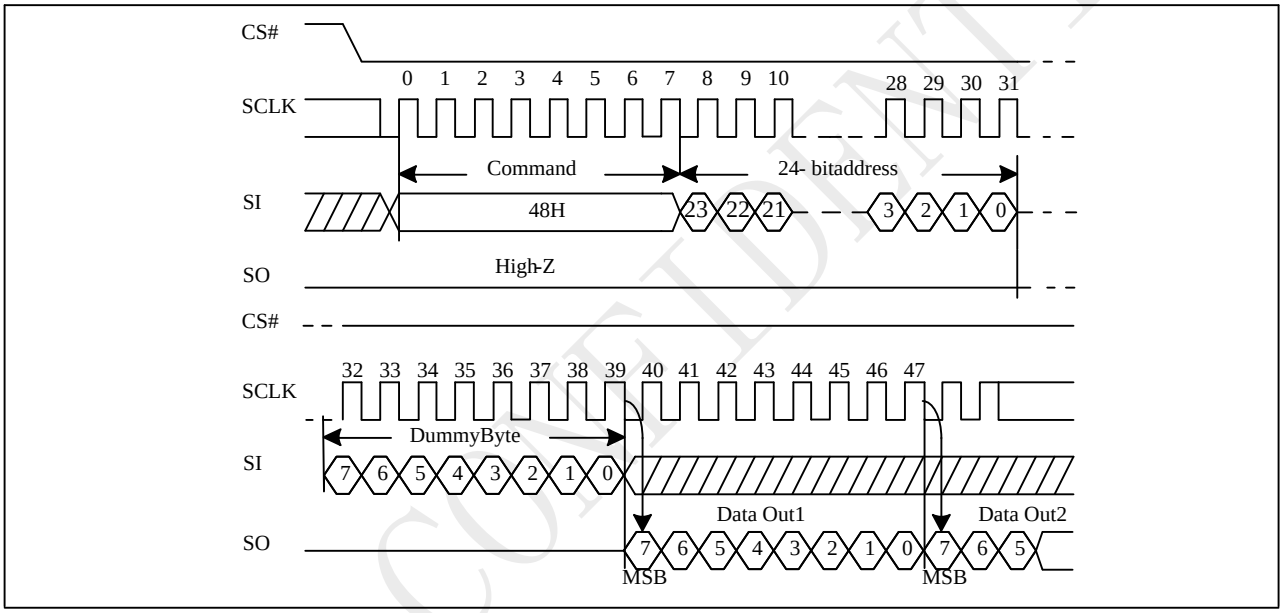
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10.21 Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by address bytes and dummy cycles, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-16	A15-12	A11-10	A9-0
Security Register #1	00H	0001	00	Byte Address
Security Register #2	00H	0010	00	Byte Address
Security Register #3	00H	0011	00	Byte Address

Figure 10-21Read Security Registers(RDSCUR) Sequence (Command 48)



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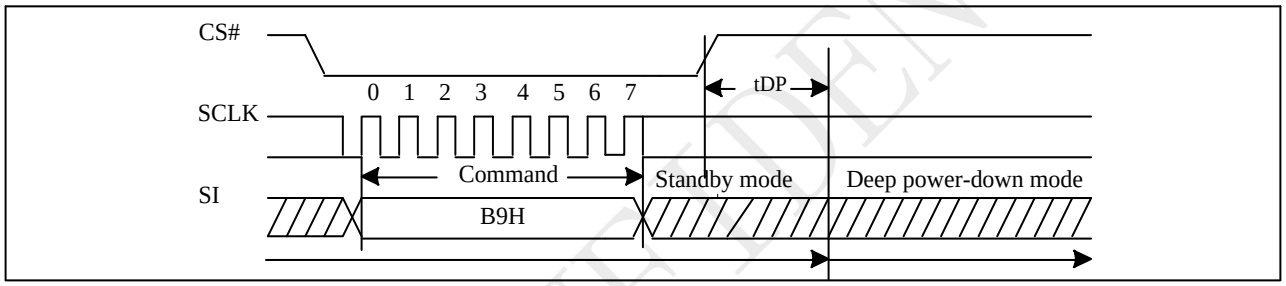
10.22 Deep Power-down (B9H)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instructions: CS# goes low → sending DP instruction code → CS# goes high.

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP), Read Electronic Signature (RES) instruction and reset instruction. (RES instruction to allow the ID been read out). When Power- down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not be executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

Figure 10-22 Deep Power-down (DP) Sequence (Command B9h)



10.23 Release from Deep Power-Down (ABH), Read Electronic Signature (ABH)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven high, the device is put in the Stand-by Power mode. If the device was not previously int he Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max). Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/ write cycle in progress.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2 (max). Once in the standby mode, the device waits to be selected, so it can be receiving, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-Down Mode.

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Figure 10-23Read Electronic Signature (RES) Sequence (Command ABh)

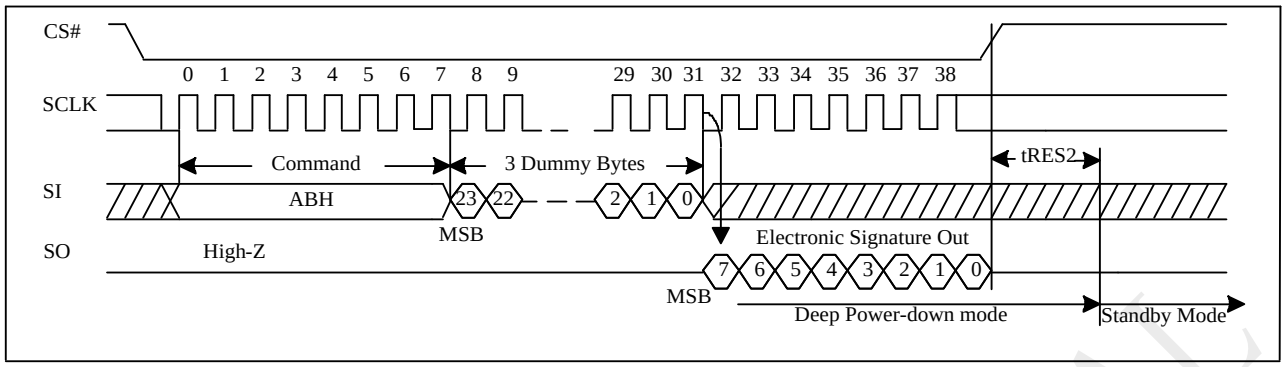
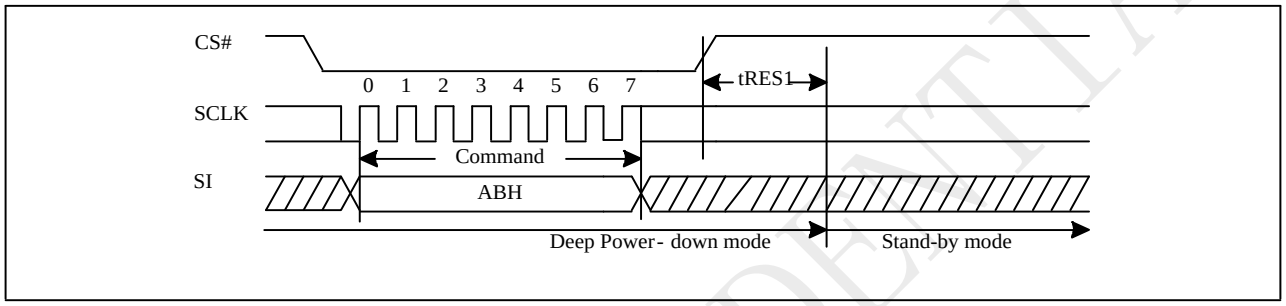


Figure 10-23a Release from Deep Power-down (RDP) Sequence (Command ABH)

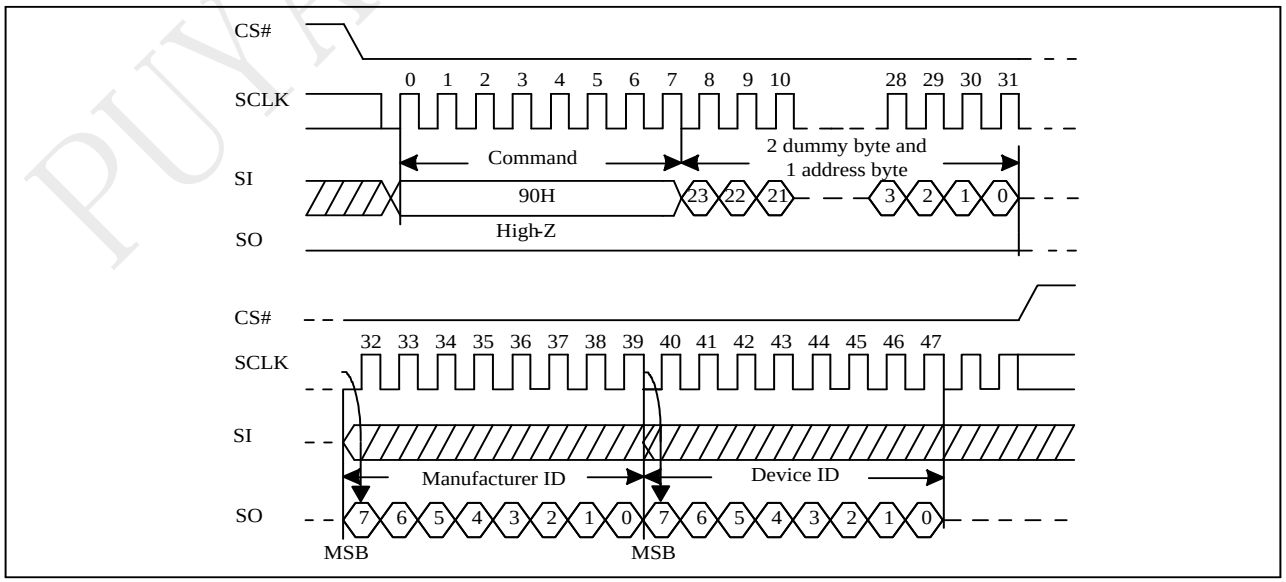


10.24 Read Electronic Manufacturer ID & Device ID (90H)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in "Table ID Definitions".

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7~A0). After which the manufacturer ID for PUYA (85h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 10-24 Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90h)



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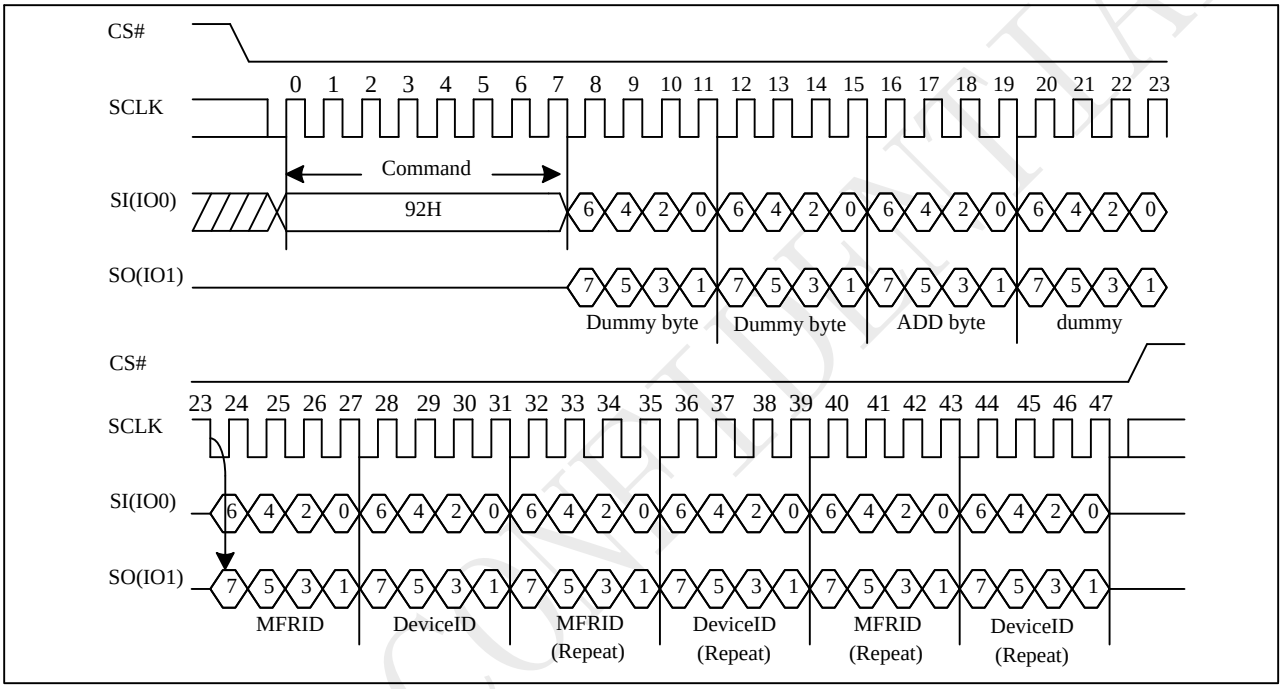
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10.25 Dual I/O Read Electronic Manufacturer ID & Device ID (92H)

The DREMS instruction is similar to the REMS command and returns the JEDEC assigned manufacturer ID which takes two pins: SIO0, SIO1 as address input and ID output I/O

The instruction is initiated by driving the CS# pin low and shift the instruction code "92h "followed by two dummy bytes and one byte's address(A7~A0). After which, the Manufacturer ID for PUYA (85h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high

Figure 10-25 DUAL I/O Read Electronic Manufacturer & Device ID (DREMS) Sequence (Command 92h)



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10.26 Read Identification (9FH)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The PUYA Manufacturer ID and Device ID are list as "Table. ID Definitions".

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 10-26 Read Identification (RDID) Sequence (Command 9Fh)

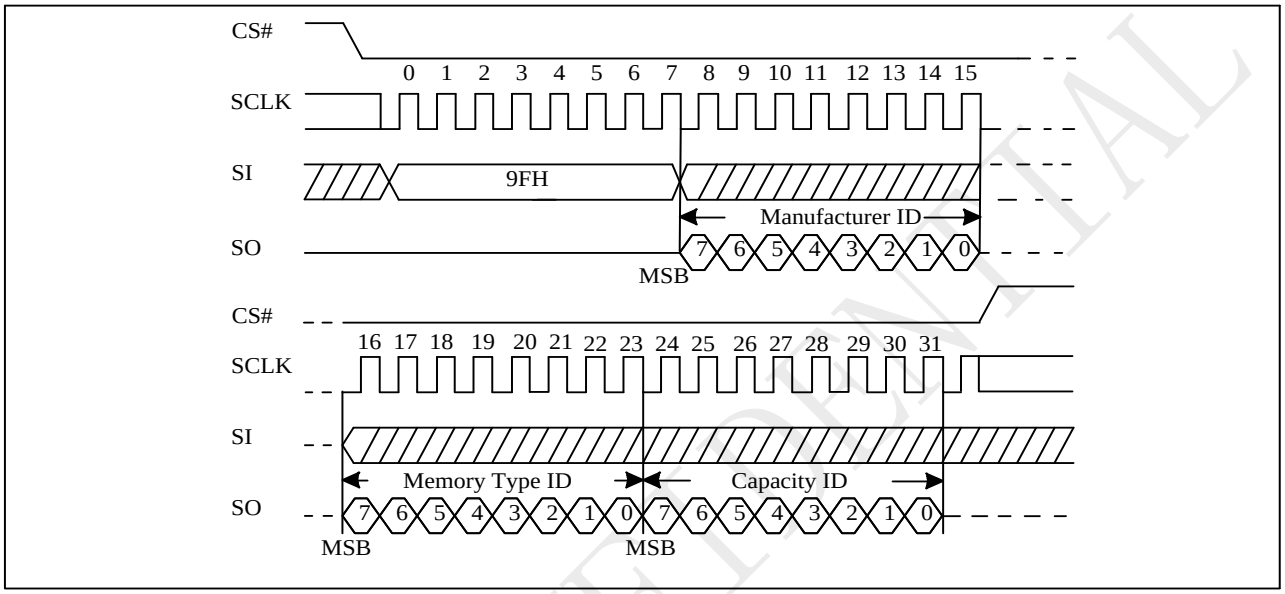


Table ID Definitions

P25D64SH	RDID command	manufacturer ID	memory type	memory density
		85	60	17
	RES command	electronic ID		
		16		
	REMS command	manufacturer ID		device ID
		85		16

10.27 No Operation (NOP)

The "No Operation" command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

10.28 Software Reset (66H/99H)

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

The SIO [3:1] are "don't care".

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

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Figure 10-28Software Reset Recovery

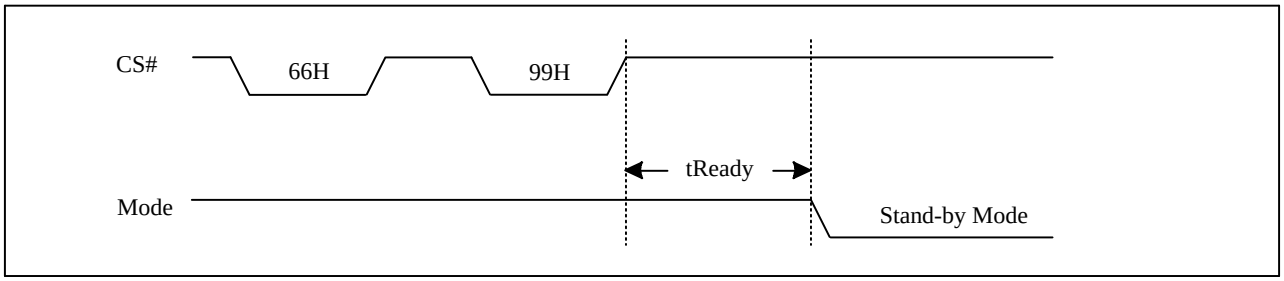
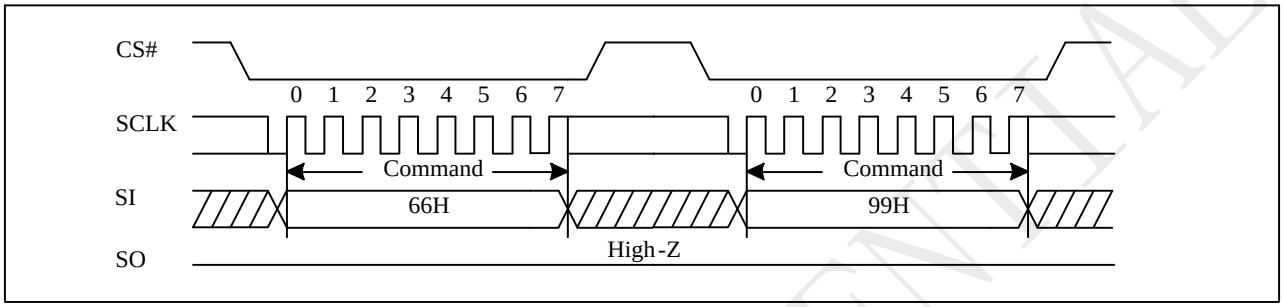


Figure 10-28aReset Sequence



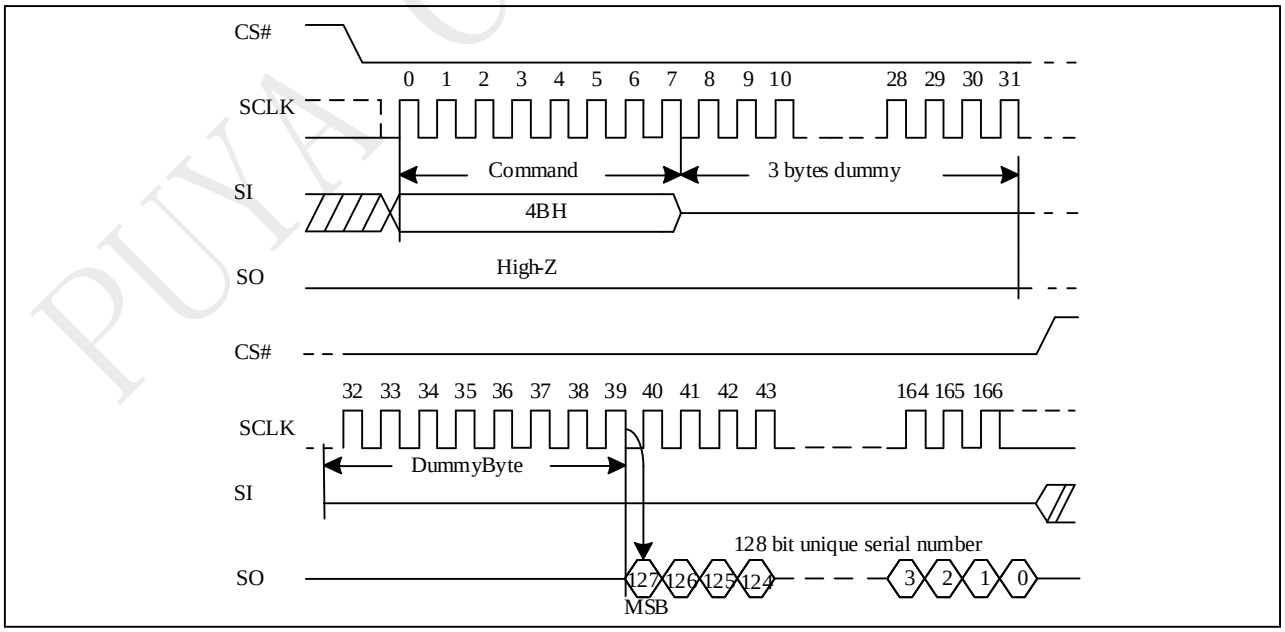
10.29 Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each P25Dxx device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low →sending Read Unique ID command →Dummy Byte1 →Dummy Byte2 →Dummy Byte3 →Dummy Byte4→128bit Unique ID Out →CS# goes high.

The command sequence is show below.

Figure 10-29 Read Unique ID (RUID) Sequence (Command 4BH)



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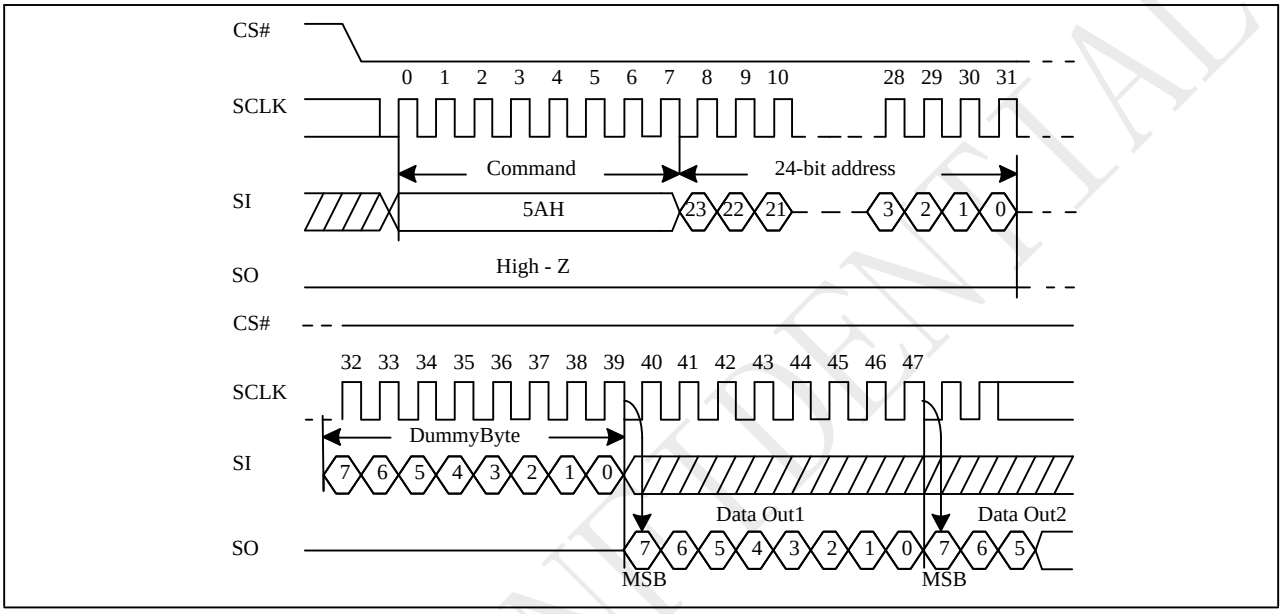
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10.30 Read SFDP Mode (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

SFDP is a JEDEC Standard, JESD216B.

Figure 10-30Read Serial Flash Discoverable Parameter (RDSFDP) Sequence



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Serial Flash Discoverable Parameter (SFDP) Table

Table Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	00H	00H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number (PUYADevice Manufacturer ID)	It is indicates PUYA manufacturer ID	10H	07:00	85H	85H
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of PUYA Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

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Table Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1- 2) Fast Read	0=Not support, 1=Support	32H	16	1b	91H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1-2- 2) FastRead	0=Not support, 1=Support		20	1b	
(1-4- 4) Fast Read	0=Not support, 1=Support		21	0b	
(1-1- 4) Fast Read	0=Not support, 1=Support		22	0b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	03FFFFFFH	
(1-4- 4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	38H	04:00	00000b	00H
(1-4- 4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	000b	
(1-4- 4) Fast Read Opcode		39H	15:08	FFH	FFH
(1-1- 4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3AH	20:16	00000b	00H
(1-1- 4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1-1- 4) Fast Read Opcode		3BH	31:24	FFH	FFH

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Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1-1- 2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1- 2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1-2- 2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3EH	20:16	00000b	80H
(1-2- 2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	100b	
(1-2- 2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2- 2) Fast Read	0=not support 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4- 4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFFH	0xFFH
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2- 2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2- 2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4AH	20:16	00000b	00H
(4-4- 4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4- 4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	52H	23:16	08H	08H
Sector Type 4 erase Opcode		53H	31:24	81H	81H

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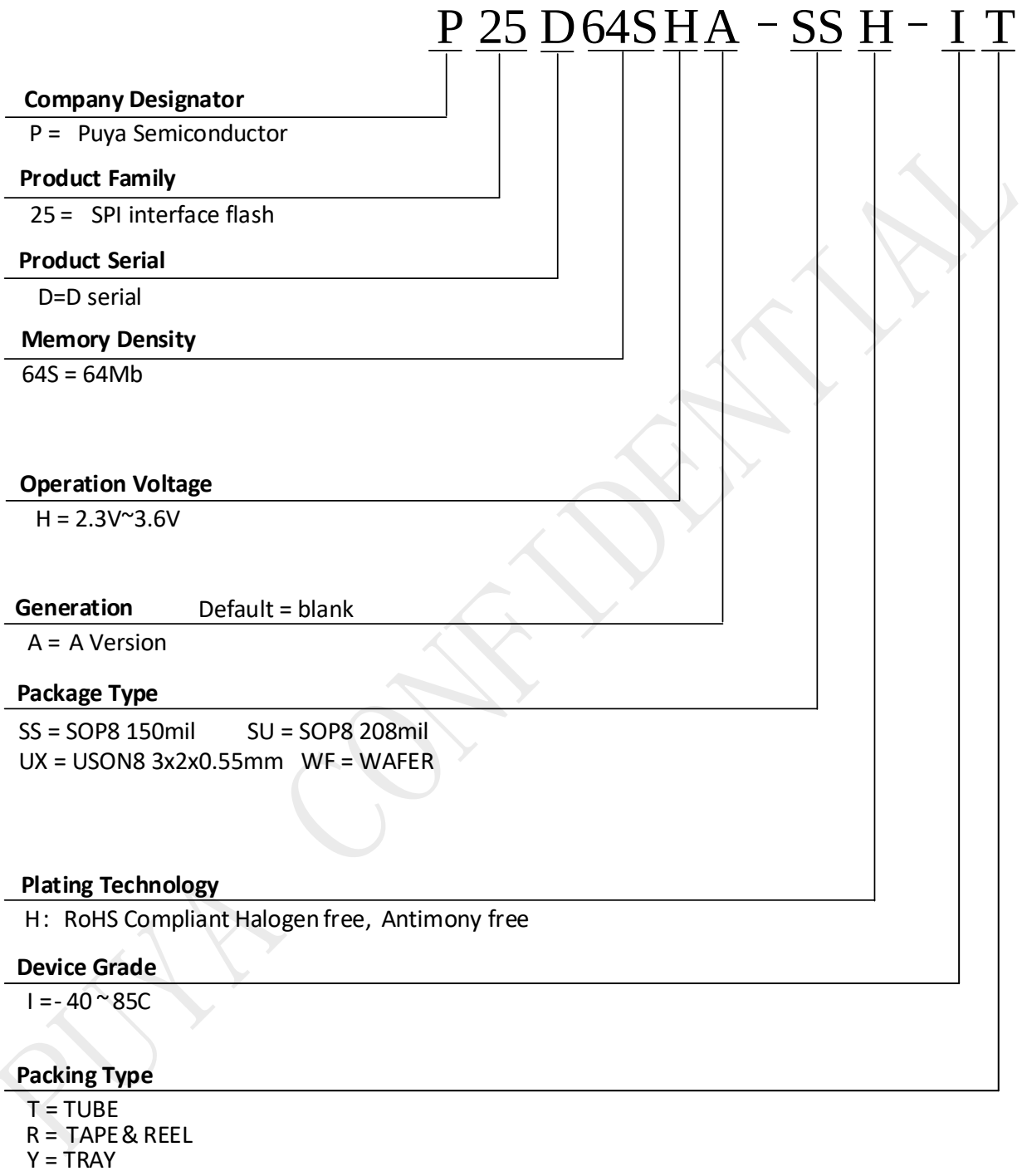
Table Parameter Table (1): PUYA Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	61H:60H	15:00	3600H	3600H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2350H=2.350V 2700H=2.700V	63H:62H	31:16	2300H	2300H
HW Reset# pin	0=not support 1=support	65H:64H	00	0b	F99EH
HW Hold# pin	0=not support 1=support		01	1b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H) before Reset cmd.		11:04	1001 1001b (99H)	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap Around Read mode	0=not support 1=support		15	1b	
Wrap - Around Read mode Opcode		66H	23:16	77H	77H
Wrap - Around Read data length	08H:support 8B wraparound read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	67H	31:24	64H	64H
Individual block lock	0=not support 1=support	6BH:68H	00	1b	E8D9H
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	36H	
Individual blocklock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	1b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

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11 Ordering Information



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12 Valid Part Numbers and Top Marking

The following table provides the valid part numbers for the P25D64SH Flash Memory. Please contact PUYA for specific availability by density and package type. PUYA Flash memories use a 14-digit Product Number for ordering.

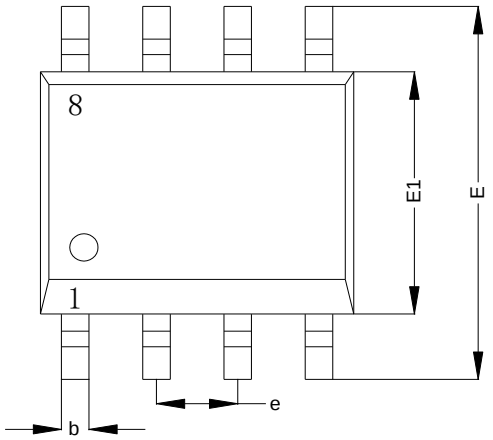
Package Type	Product Number	Density	Top Side Marking	Temp.	Packing Type
SS SOP8 150mil	P25D64SH-SSH-IT	64M-bit	P25D64SH xxxxxxx	85C	Tube
SS SOP8 150mil	P25D64SH-SSH-IR	64M-bit	P25D64SH xxxxxxx	85C	Reel
SU SOP8 208mil	P25D64SH-SUH-IT	64M-bit	P25D64SH xxxxxxx	85C	Tube
SU SOP8 208mil	P25D64SH-SUH-IR	64M-bit	P25D64SH xxxxxxx	85C	Reel
UX USON8 3x2mm	P25D64SH-UXH-IR	64M-bit	PD64S Hxxx	85C	Reel

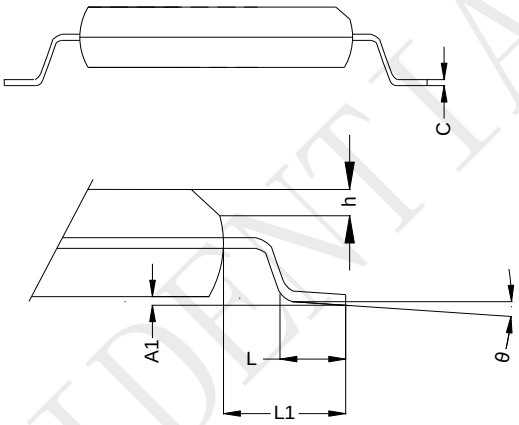
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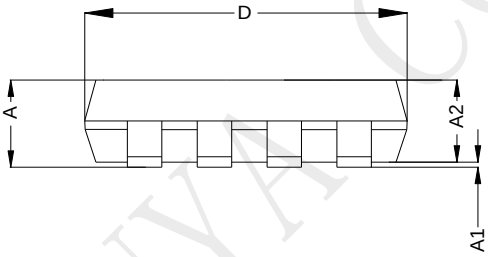
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13 Package Information

13.1 8-Lead SOP(150mil)







Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	1.350	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.170	-	0.250
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	-	1.270	-
L	0.400	-	1.270
L1	-	1.050	-
θ	0	-	8°
h	0.25	-	0.50

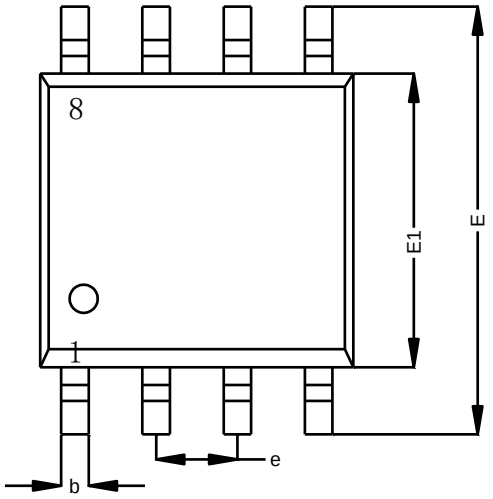
Note：1. Dimensions are not to scale

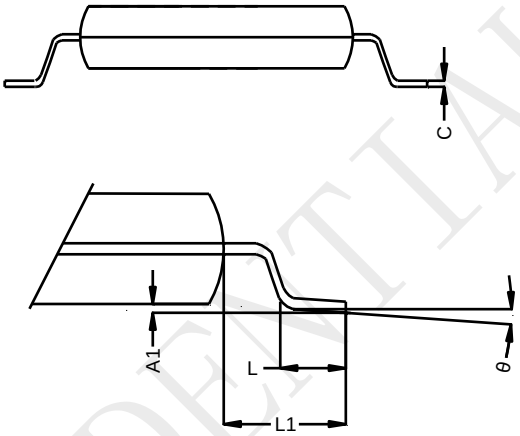
	TITLE	DRAWING NO.	REV
PUYA	Puya SOP8（150mil）POD	QRPD-0004	1.1

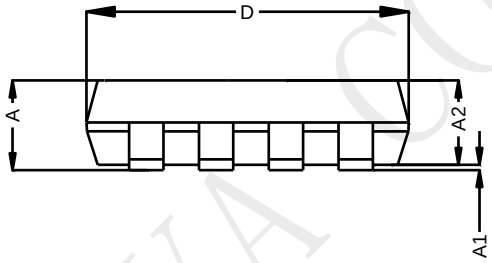
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13.2 8-Lead SOP(208mil)







Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	2.150
A1	0.050	-	0.250
A2	1.700	-	1.900
b	0.310	-	0.510
c	0.150	-	0.250
D	5.130	5.230	5.330
E	7.800	7.900	8.000
E1	5.180	5.280	5.380
e	-	1.270	-
L	0.500	-	0.800
L1	-	1.310	-
θ	0	-	8°

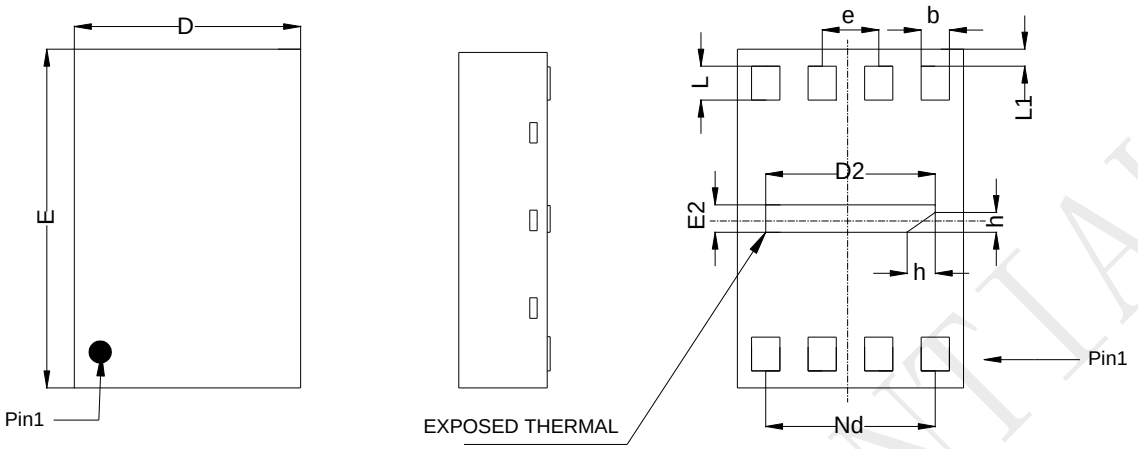
Note：1. Dimensions are not to scale

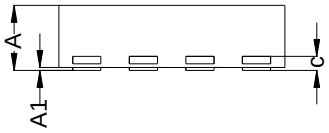
	TITLE	DRAWING NO.	REV
PUYA	Puya SOP8(208MIL) POD	QRPD-0005	1.0

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13.3 8-Pad USON(3x2x0.55mm)





Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
e	0.50BSC		
L	0.30	0.35	0.40
h	0.05	0.15	0.25
Nd		1.50BSC	
L1	0.05	0.10	0.15
c	0.10	0.15	0.20

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya USON8L 2x3x0.55-0.5PITCH POD	QRPD-0009	1.0

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14 Revision History

Rev.	Date	Description	Note
1.0	2022-01-11	Initial Release	-
1.1	2023-11-22	Update Overshoot Waveform Add V_{IL} Min and V_{IH} Max value Add UX (USON8 3x2x0.55mm) package type Format update: delete date in homepage; update IMPORTANT NOTICE	-

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