NOVOSENSE

NST175 0.5°C Accurate Temperature Sensor with I²C and SMBus Interface

Datasheet 1.21

Description

The NST175 is a lower power, higher accuracy digital temperature sensors ideal for negative temperature coefficient (NTC) and positive temperature coefficient (PTC) thermistor replacement. NST175 Compatible with two-wire SMBus and I²C interfaces, supports up to 27 devices address and provides SMBus Reset and Alert function. The NST175 also feature a SMBus Alert function. The devices offer a typical accuracy of 0.5 °C without requiring calibration or external component signal conditioning. The NST175 temperature sensors are highly linear and do not require complex calculations or look-up tables to derive the temperature. The on-chip 12-bit analog-to-digital converter (ADC) offers resolutions down to 0.0625°C. NST175 device works over a temperature range of –55°C to 125°C, which makes it suitable for onboard and off board applications in automotive, industrial, and consumer markets. The NST175 is very low power device, which can be applied in IoT. The NST175 is available in an SOIC-8 package and an MSOP-8 package.

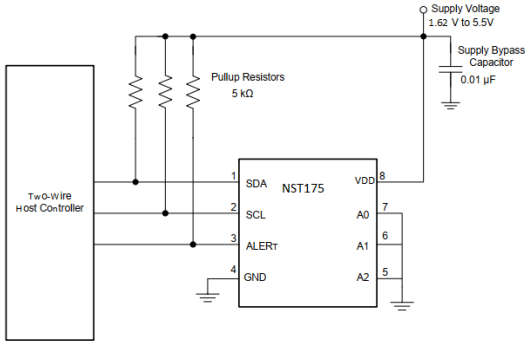
Applications

- General System Thermal Management
- Computer Peripheral Thermal Protection
- Notebook Computers
- Industrial Internet of Things (IoT)
- Communications Infrastructure
- Power-system monitors
- Thermal protection
- Environmental Monitoring and HVAC

Features：

- High Accuracy Over –55°C to 125°C Wide Temperature Range
  - ✓ -20 °C ~ 85 °C : ± 0.5 °C (Typical)
  - ✓ -20 °C ~ 85 °C : ± 1 °C (Maximum)
  - ✓ -55 °C ~-20 °C: ± 2 °C (Maximum)
  - ✓ 85 °C ~125 °C: ± 2 °C (Maximum)
- Proportional to Temperature with 0.0625°C Resolution
- Power up Defaults Permit Stand-Alone Operation as Thermostat
- Supports up to 27 Device Addresses
- Supply Operation range from 1.62V to 5.5V
- Operating current: 30uA(Typical)
- Shutdown current: 0.1μA (Typical)
- Digital Interface: SMBus, I²C
- Package
  - ✓ MSOP(8) (3mm x 3mm)
  - ✓ SOIC(8)（4.9mm x 3.91mm）

Typical Application



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1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Voltage Pin (VDD)	VDD	-0.3		6.5	V	
Voltage at A0, A1and A2 Pins	A0，A1，A2	-0.3		6.5	V	
Voltage at OS, SCL and SDA Pins	ALERT,SCL, SDA	-0.3		6.5	V	
Storage temperature		-60		155	℃	
Operation temperature	$TB_{operation}$	-55		125	℃	
Maximum junction temperature				155	℃	
ESD susceptibility	HBM	±5			KV	
	CDM	±1			KV	

2.0 ELECTRICAL CHARACTERISTICS

2.1. Electrical characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply						
Supply voltage Range	VDD	1.62	3.3	5.5	V	
Pull up resistor Range	R_{pu}	0.5	5	10	KΩ	
Supply sensitivity			16		m℃/V	
Operation current	Iconv		30	60	uA	Conversion
Shutdown current	I_{SD}		0.1		uA	Serial bus inactive
	I_{SD}		10		uA	Serial bus active, SCL frequency = 400 kHz
Temperature Range and Resolution						
Temperature Range		-55		125	℃	
Resolution			0.0625		℃	
Accuracy		-1	0.5	1	℃	From -20℃ to 85℃
		2		2	℃	From -50℃ to -20℃
		2		2	℃	From 85℃ to125℃

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Conversion time	T_{CONV}		24	32	ms	For VDD<2V，the max conversion time 64 ms.
ALERT Output Saturation Voltage				0.5	V	I_{OUT} = 4 mA
ALERT Delay		1		6	conversion	
High limit Default Temperature	T_H		80		℃	
Low limit Default Temperature	T_L		75		℃	
Time out time	$T_{TIMEOUT}$		54		ms	
Digital DC Characteristic						
$V_{IN(1)}$ Logical "1" Input Voltage	VH	VDD*0.7		VDD+0.3	V	
$V_{IN(0)}$ Logical "0" Input Voltage	VL	-0.3		VDD*0.3	V	
$I_{IN(1)}$ Logical "1" Input Current				1	uA	
$I_{IN(0)}$ Logical "0" Input Current				-1	uA	
C_{IN} All Digital Inputs	C_{IN}		5		pF	
I_{OH} High Current Level Output Open drain leakage	I_{OH}			1	uA	V_{OH}=5V
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL=}$ 3 mA;
Thermal response						
Stirred oil thermal response time to 63% of final value (package only)			0.75		s	MSOP（8）
Drift						
Drift[1]			0.1		℃	

Notes： 1. Drift data is based on a 1000-hour stress test at +125°C with V_{DD} = 5.5V.

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2.2. I²C Timing Diagram

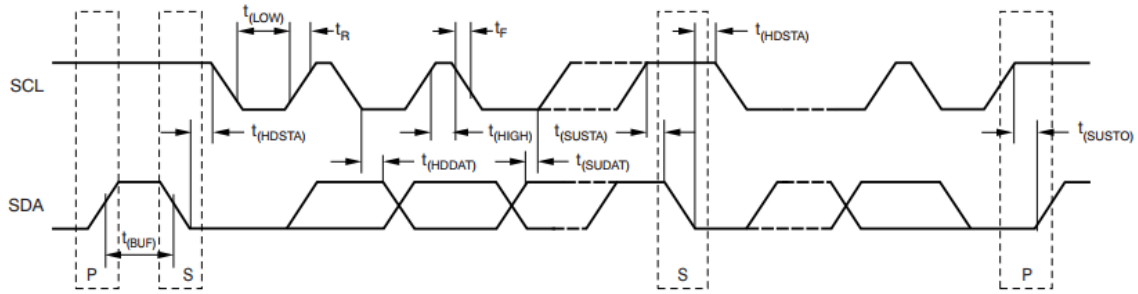


Figure 2.1 I²C Timing Diagram

2.3. I²C Timing characteristics

Parameters	*Symbol*	*FAST MODE*		*HIGH-SPEED MODE*		*Unit*	*Comments*
		Min	*Max*	*Min*	*Max*		
SCL operating frequency	F_{SCL}	0.001	0.4	0.001	2	MHz	
Bus-free time between STOP and START conditions	$t_{(BUF)}$	1300		160		ns	
Hold time after repeated START condition; after this period, the first clock is generated	$t_{(HDSTA)}$	600		160		ns	
Repeated START condition setup time	$t_{(SUSTA)}$	600		160		ns	
STOP condition setup time	$t_{(SUSTO)}$	600		160		ns	
Data hold time	$T_{(HDDAT)}$	4	900	4	120	ns	
Data setup time	$T_{(SUDAT)}$	100		10		ns	
SCL clock low period	$T_{(LOW)}$	1300		280		ns	
SCL clock high period	$T_{(HIGH)}$	600		60		ns	
Data fall time	t_FD		300		150	ns	
Clock rise time	t_{RC}		300		40	ns	
			1000			ns	
Clock fall time	t_{FC}		300		40	ns	

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3.0 TYPICAL CHARACTERISTICS

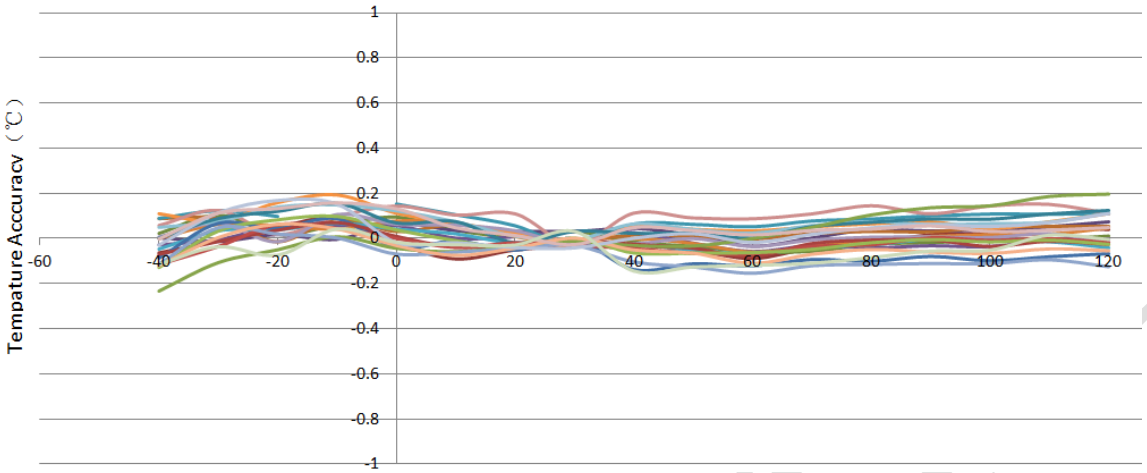


Figure 3.1 Using MSOP8 test, VDD= 3.3V

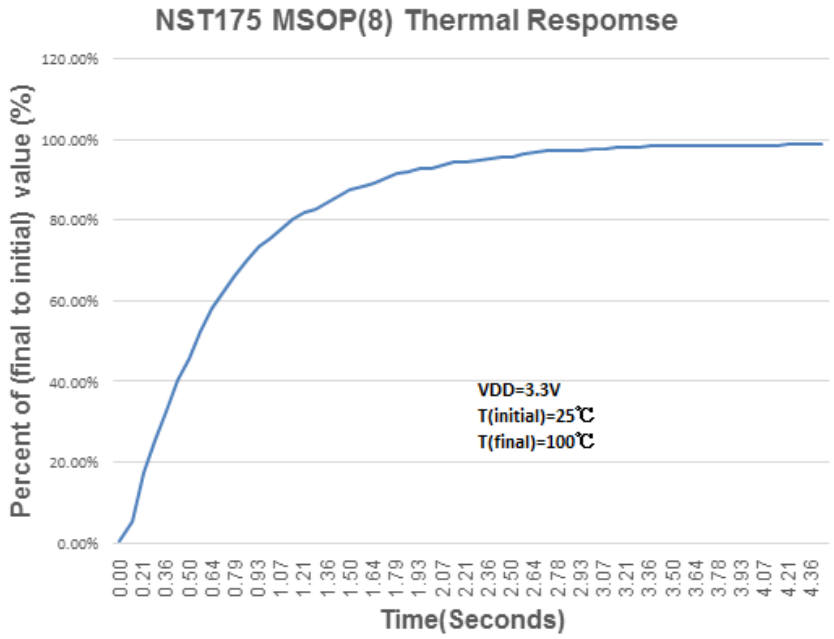


Figure 3.2 Temperature Step Response （VDD= 3.3V,MSOP(8)）

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4.0 FUNCTION DESCRIPTION

4.1. FUNCTION DESCRIPTION

The NST175 temperature sensor incorporates a band-gap type temperature sensor and 12-bit ADC (sigma-delta ADC). The temperature data output of the NST175 is available at all times via the I²C bus. A digital comparator is also incorporated that compares a series of readings, the number of which is user-selectable, to user-programmable setpoint and hysteresis values. The comparator trips the ALERT Output line, which is programmable for mode and polarity. The NST175 has an integrated low-pass filter on both the SDA and the SCL line. These filters increase communications reliability in noisy environments.

The NST175 also has a bus fault timeout feature. If the SDA line is held low for longer than $T_{TIMEOUT}$ (see specification) the NST175 will reset to the IDLE state (SDA set to high impedance) and wait for a new start condition. The TIMEOUT feature is not functional in Shutdown Mode.

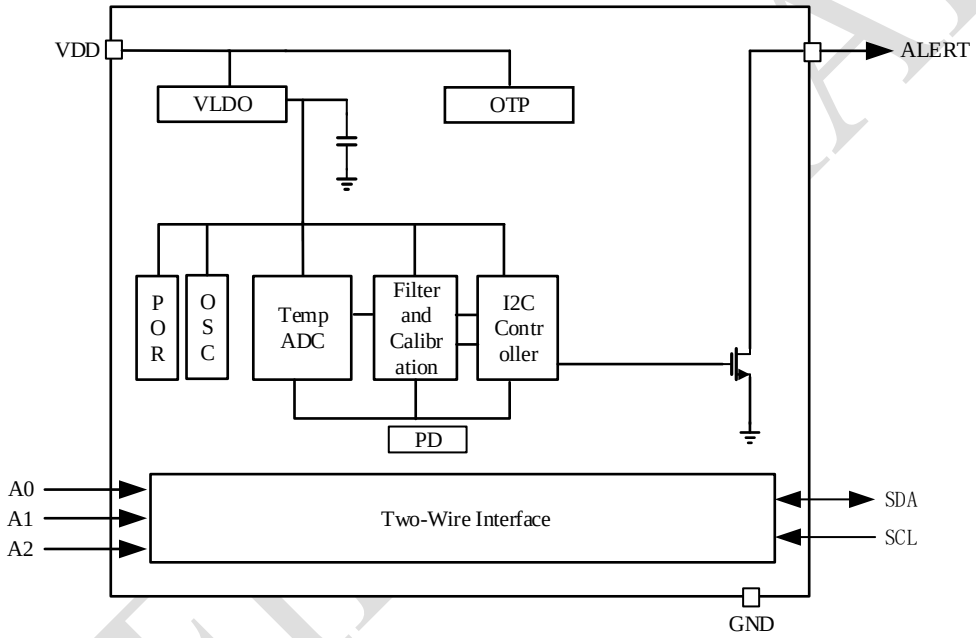


Figure 4.1 NST175 Functional Block Diagram

4.2. Feature Description

4.2.1 Digital Temperature Sensor

The NST175 is an industry-standard digital temperature sensor with an integrated sigma-delta ADC and I²C interface. The NST175 provides 12-bit digital temperature readings with an accuracy of ± 0.5°C from –25°C to 85°C and ± 2° Cover –55°C to 125°C.

The NST175 operates with a single supply from 1.62 V to 5.5 V. Communication is accomplished over a 2-wire interface which operates up to 400 kHz in I²C fast mode and 2MHz in I²C High speed mode. The NST175 has three address pins, allowing up to 27 devices to operate on the same 2-wire bus. The NST175 has a dedicated over-temperature output with programmable High temperature limit and Low temperature limit. This output has programmable fault tolerance, which allows the user to define the number of consecutive error conditions that must occur before ALERT is activated.

The digital output from each temperature measurement conversion is stored in the read-only Temperature register. The Temperature register of the NST175 is a 12-bit read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are listed in Table 4.5 and Table 4.6. The first 12 bits are used to indicate temperature with all remaining bits equal to zero. Data format for temperature is listed in Table 4.1. Negative numbers are represented in binary twos complement format. Following power-up or reset, the Temperature register reads 0°C until the first conversion is complete.

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The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits (MSBs) in the Temperature register are used with the unused least significant bits (LSBs) set to zero.

Table 4.1. Temperature Data Format

TEMPERATURE (℃)	DIGITAL OUTPUT	
	BINARY	HEX
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
-0.25	1111 1111 1100	FFC
-25	1110 0111 0000	E70
-55	1100 1001 0000	C90

4.2.2 Serial Interface

The NST175 operate only as slave devices on the SMBus, two-wire, and I^2C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The NST175 support the transmission protocol for fast (up to 400 kHz) and high-speed (up to 2 MHz) modes. All data bytes are transmitted MSB first.

4.2.2.1 Bus Overview

The device that initiates the transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a high to low logic level when SCL is high. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer SDA must remain stable when SCL is high because any change in SDA when SCL is high is interpreted as a control signal.

When all data are transferred, the master generates a STOP condition indicated by pulling SDA from low to high when SCL is high.

4.2.2.2 Serial Bus Address

To communicate with the NST175, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

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The NST175 features three address pins to allow up to 27 devices to be addressed on a single bus interface. Table 4.2 describes the pin logic levels used to properly connect up to 27 devices. A 1 indicates the pin is connected to the supply (VDD); a 0 indicates the pin is connected to GND; float indicates the pin is left unconnected. The state of pins A0, A1, and A2 is sampled on every bus communication and must be set prior to any activity on the interface.

Table 4.2. Address Pins and Slave Addresses for the NST175

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111
Float	0	0	1110000
Float	0	Float	1110001
Float	0	1	1110010
Float	1	0	1110011
Float	1	Float	1110100
Float	1	1	1110101
Float	Float	0	1110110
Float	Float	1	1110111
0	Float	0	0101000
0	Float	1	0101001
1	Float	0	0101010
1	Float	1	0101011
0	0	Float	0101100
0	1	Float	0101101
1	0	Float	0101110
1	1	Float	0101111
0	Float	Float	0110101
1	Float	Float	0110110
Float	Float	Float	0110111

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4.2.2.3 Writing and Reading to the NST175

Accessing a particular register on the NST175 devices is accomplished by writing the appropriate value to the Pointer register. The value for the Pointer register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the NST175 requires a value for the Pointer register.

When reading from the NST175 devices, the last value stored in the Pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer register. This action is accomplished by issuing a slave addresses byte with the R/$\overline{W}$ bit low, followed by the Pointer register byte. No additional data are required.

The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 4.5 for details of this sequence. If repeated reads from the same register are desired, the Pointer register bytes do not have to be continually sent because the NST175 remember the Pointer register value until the value is changed by the next write operation.

Register bytes are sent MSB first, followed by the LSB.

4.2.2.4 Slave mode operations

The NST175 can operate as a slave receiver or slave transmitter.

4.2.2.4.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The NST175 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer register. The NST175 then acknowledges reception of the Pointer register byte. The next byte or bytes are written to the register addressed by the Pointer register. The NST175 acknowledge reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

4.2.2.4.2 Slave Transmitter Mode

The first byte is transmitted by the master and is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

4.2.2.5 SMBus Alert Function

The NST175 support the SMBus Alert function. When the NST175 are operating in interrupt mode (TM = 1), the ALERT pin of the NST175 can be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the NST175 is active, the devices acknowledge the SMBus Alert command and respond by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. This bit is high if the temperature is greater than or equal to T_{HIGH}. This bit is low if the temperature is less than T_{LOW}. See Figure 4.6 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determine which device clears its ALERT status. If the NST175 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the NST175 loses the arbitration, its ALERT pin remains active.

4.2.2.6 General Call

The NST175 respond to a two-wire general call address (0000000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000100, NST175 latch the status of their address pins, but do not reset. If the second byte is 00000110, the NST175 latch the status of their address pins and reset their internal registers to their power-up values.

4.2.2.7 High-Speed Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The NST175 devices do not acknowledge this byte, but do switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode,

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allowing transfers at up to 2 MHz（For VDD<1.8V, the Hs-mode up to 1.6 MHz）. After the Hs-mode master code is issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the NST175 switch the input and output filter back to fast-mode operation.

4.2.2.8 Time-out Function

The NST175 resets the serial interface if either SCL or SDA is held low for 54 ms (typical) between a START and STOP condition. The NST175 releases the bus if it is pulled low and waits for a START condition. To avoid activating the time-out function, a communication speed of at least 1 kHz must be maintained for the SCL operating frequency.

4.2.3 I²C Timing Diagram

The NST175 devices are two-wire, SMBus, and I²C interface-compatible. Figure 4.2 to Figure 4.6 describe the various operations on the NST175. The following list provides bus definitions. Parameters for Figure 4.2 are defined in the *Timing Requirements*.

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating Not-Acknowledge on the last byte that is transmitted by the slave.

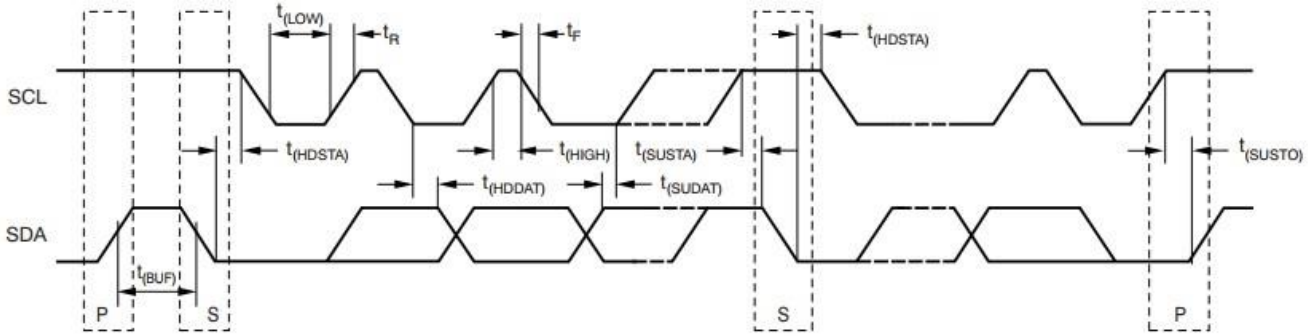


Figure 4.2. Two-Wire Timing Diagram

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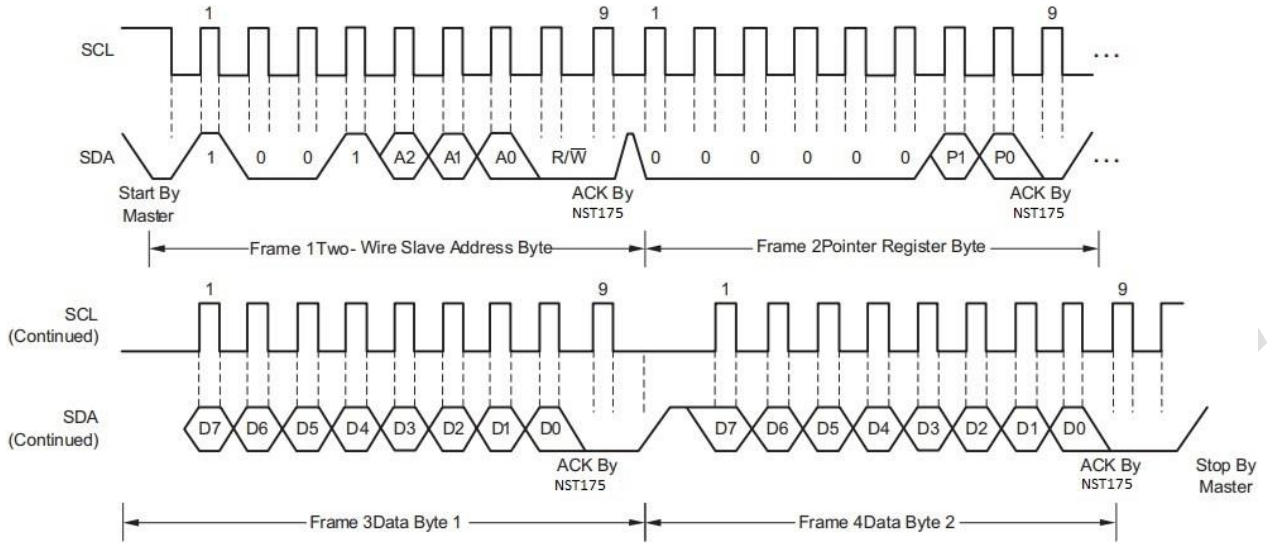


Figure 4.3. Two-Wire Timing Diagram for the NST175 Write Word Format

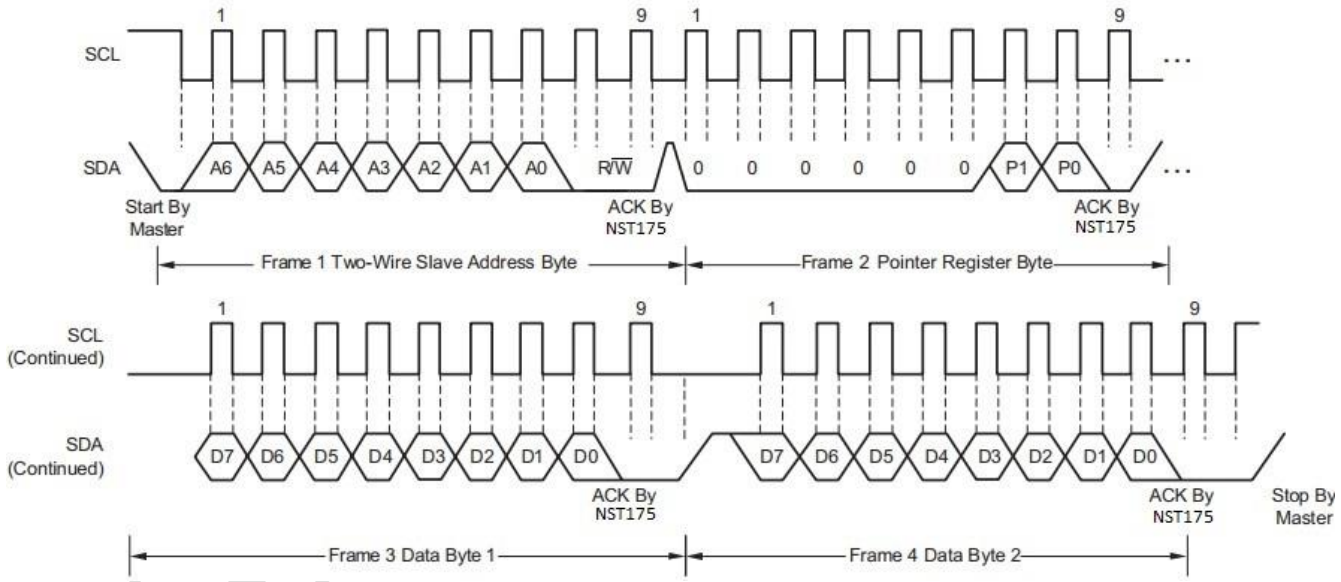


Figure 4.4. Two-Wire Timing Diagram for the NST175 Write Word Format

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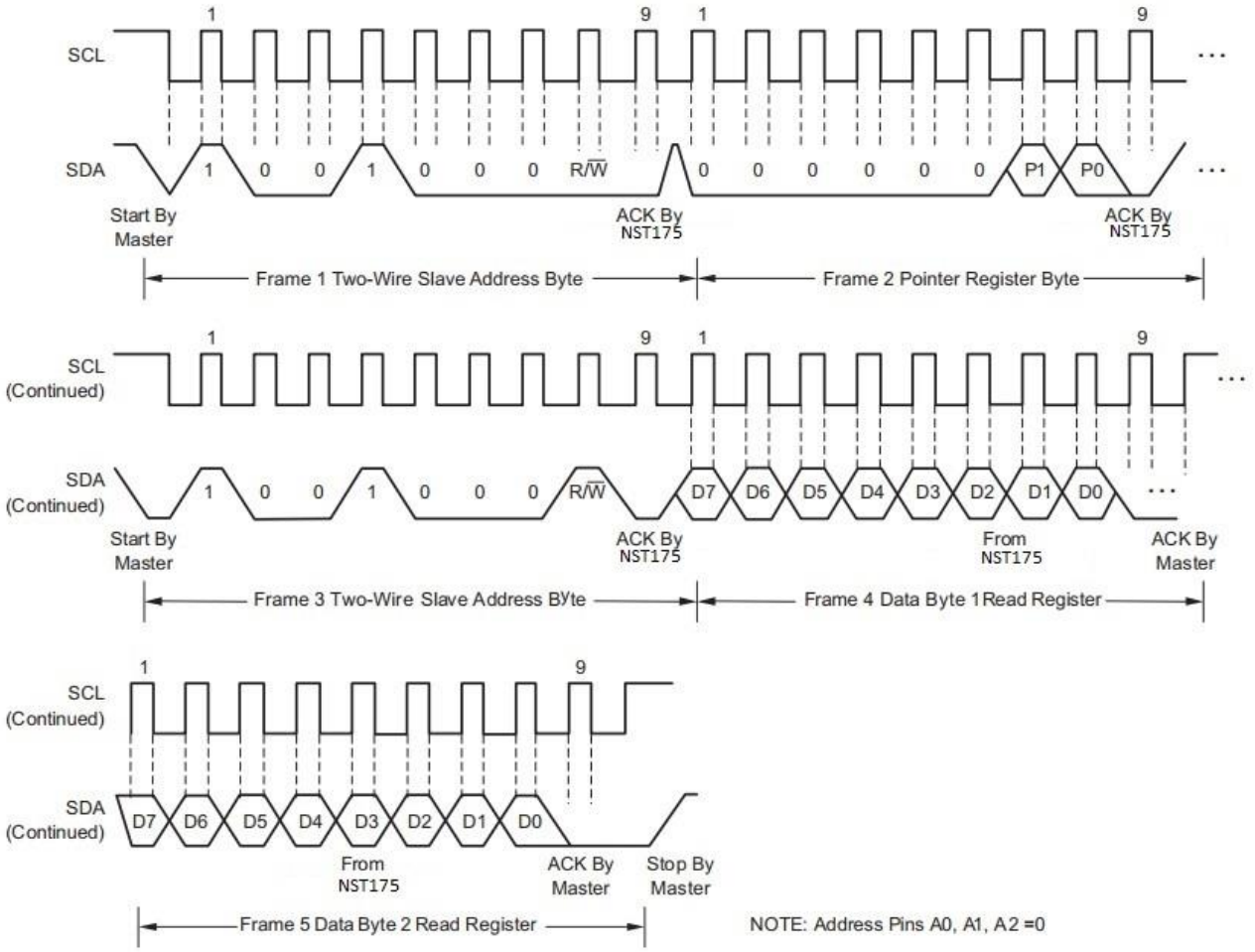


Figure 4.5. Two-Wire Timing Diagram for Read Word Format

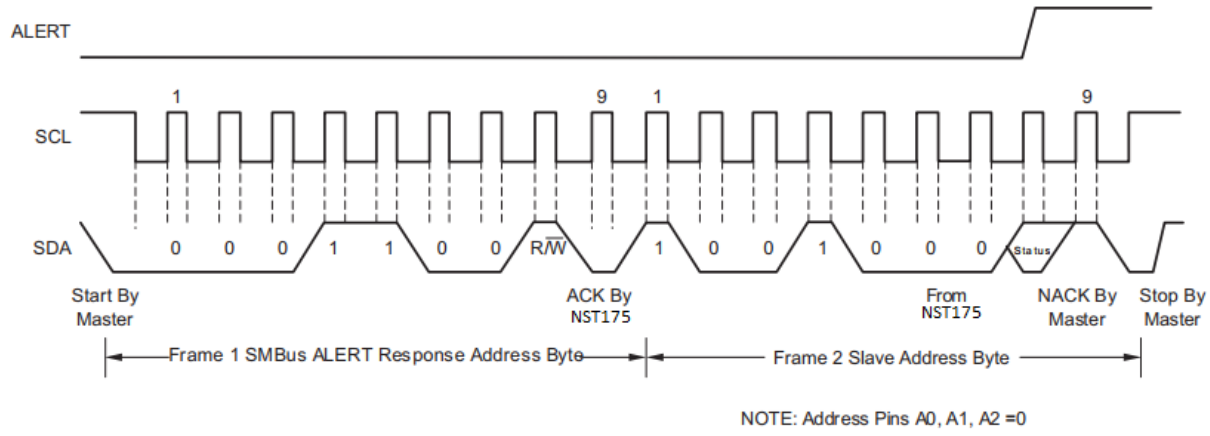


Figure 4.6. Timing Diagram for SMBus ALERT

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4.3 Device Functional Modes

4.3.1 Shutdown Mode (SD)

The shutdown mode of the NST175 devices lets the user save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 0.1 μA. Shutdown mode is enabled when the SD bit is 1; the device shuts down when the temperature conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

For the NST175, the TIMEOUT feature is turned off in Shutdown Mode.

4.3.2 One-shot (OS)

The NST175 feature a one-shot temperature measurement mode. When the device is in shutdown mode, writing 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the NST175 when continuous temperature monitoring is not required. When the configuration register is read, the OS always reads zero.

4.3.3 Thermostat Mode (TM)

The thermostat mode bit of the NST175 indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the High and Low Limit Registers section.

4.3.3.1 Comparator Mode (TM = 0)

In comparator mode (TM = 0), the ALERT pin is activated when the temperature equals or exceeds the value in the T(HIGH) register and remains active until the temperature falls below the value in the TLOW register. For more information on the comparator mode, see the High and Low Limit Registers section.

4.3.3.2 Interrupt Mode (TM = 1)

In interrupt mode (TM = 1), the ALERT pin is activated when the temperature exceeds T_{HIGH} or goes below T_{LOW} registers. The ALERT pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the High and Low Limit Registers section.

4.4 Programming

4.4.1 Pointer Register

Figure 4.7 shows the internal register structure of the NST175. The 8-bit Pointer register of the devices is used to address a given data registers. The Pointer register uses the two LSBs to identify which of the data registers must respond to a read or write command. Table 4.3 identifies the bits of the Pointer register byte. Table 4.4 describes the pointer address of the registers available in the NST175. Power-up reset value of P2/P1/P0 is 00.

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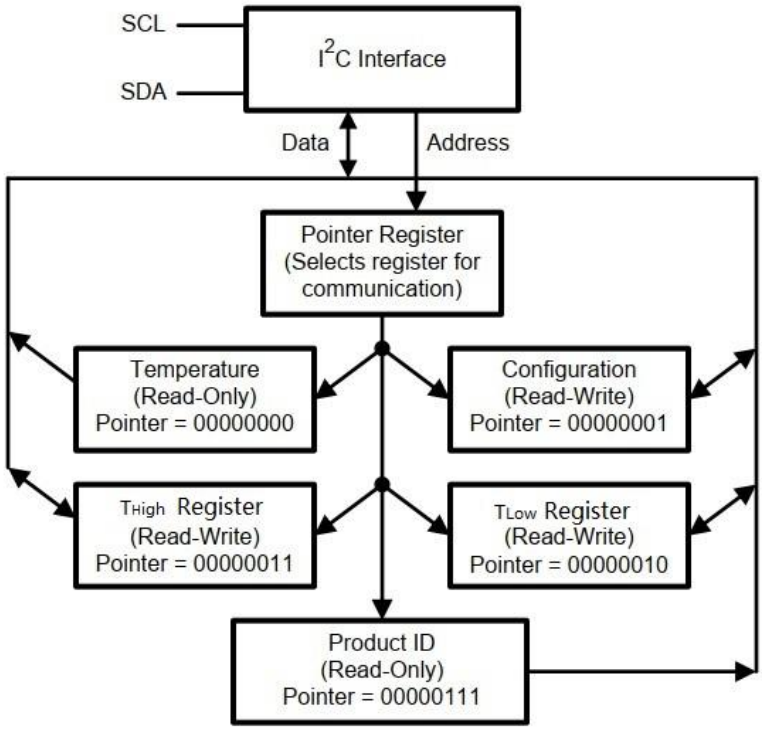


Figure 4.7. Internal Register Structure of the NST175

4.4.1.1 Pointer Register Byte (pointer = N/A) [reset = 00h]

Table 4.3. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	Register bit		

4.4.1.2 Pointer Addresses of the NST175

Table 4.4. Pointer Addresses of the NST175

P2	P1	P0	TYPE	REGISTER
0	0	0	R only default	Temperature register
0	0	1	R/W	Configuration register
0	1	0	R/W	T_{LOW} register
0	1	1	R/W	T_{HIGH} register
1	1	1	R only	Product ID Register

4.4.2 Temperature Register

The Temperature register of the NST175 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 4.5 and Table 4.6. Byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal

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to zero. The least significant byte does not have to be read if that information is not needed. Following power-up or reset value, the Temperature register reads 0°C until the first conversion is complete.

Table 4.5. Byte 1 of the Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 4.6. Byte 1 of the Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

4.4.3 Configuration Register

The Configuration register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format of the Configuration register for the NST175 is shown in Table 4.7, followed by a breakdown of the register bits. The power-up or reset value of the Configuration register are all bits equal to 0.

Table 4.7. Configuration Register Format

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD

4.4.3.1 Shutdown Mode (SD)

The shutdown mode of the NST175 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 0.1 μA. Shutdown mode is enabled when the SD bit is 1; the device shuts down when the current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

4.4.3.2 Thermostat Mode (TM)

The thermostat mode bit of theNST175 indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the High and Low Limit Registers section.

4.4.3.3 Polarity (POL)

The polarity bit of the NST175 lets the user adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is illustrated in Figure 4.8.

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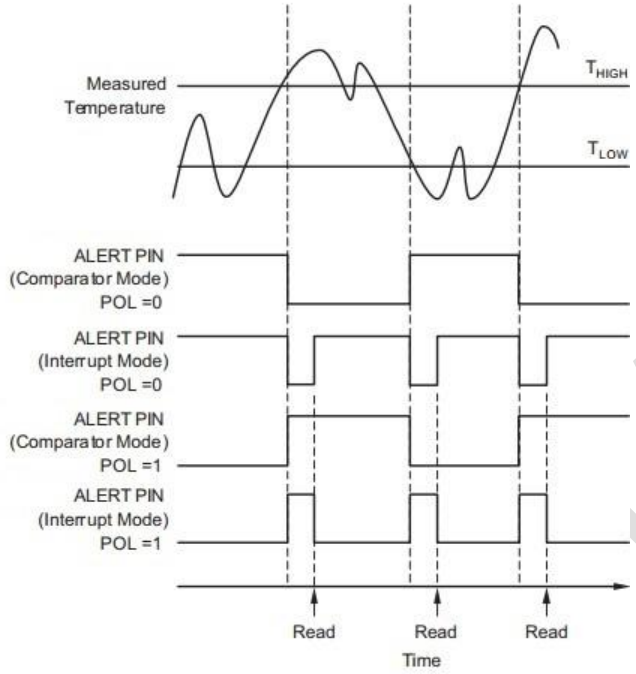


Figure 4.8. Output Transfer Function Diagrams

4.4.3.4 Fault Queue (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 4.8 defines the number of measured faults that can be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the High and Low Limit Registers section.

Table 4.8. Fault Settings of the NST175

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

4.4.3.5 Converter Resolution (R1/R0)

The converter resolution bits control the resolution of the internal ADC converter. This control allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 4.9 identifies the resolution bits and the relationship between resolution and conversion time

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Table 4.9. Resolution of the NST175

R1	R0	Resolution	Conversion time（Typical）
0	0	9bit(0.5℃)	24ms
0	1	10bit(0.25℃)	24ms
1	0	11bit（0.125）	24ms
1	1	12bit（0.0625）	24ms

4.4.3.6 One-Shot (OS)

The NST175 feature a one-shot temperature measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the NST175 when continuous temperature monitoring is not required. When the configuration register is read, the OS always reads zero.

4.4.3.7 High and Low Limit Registers

In comparator mode (TM = 0), the ALERT pin of the NST175 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode. When the ALERT pin is cleared, it only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert response address. When the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the general call reset command. This action also clears the state of the internal registers in the device by returning the device to comparator mode (TM = 0)

Both operational modes are represented in Figure 4.8. Table 4.10, Table 4.11, Table 4.12, and Table 4.13 describe the format for the T_{HIGH} and T_{LOW} registers. The most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are:

T_{HIGH} = 80°C and T_{LOW} = 75°C

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature register.

Table 4.10. Byte 1 of the T_{HIGH} Register

D7	D6	D5	D4	D3	D2	D1	D0
H11	H10	H9	H8	H7	H6	H5	H4

Table 4.11. Byte 2 of the T_{HIGH} Register

D7	D6	D5	D4	D3	D2	D1	D0
H3	H2	H1	H0	0	0	0	0

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Table 4.12. Byte 1 of the T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4

Table 4.13. Byte 2 of the T_{LOW} Register

D7	D6	D5	D4	D3	D2	D1	D0
L3	L2	L1	L0	0	0	0	0

All 12 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

4.4.3.8 PRODID: Product ID Register (Read-Only) Pointer Address: 07h

Table 4.14. Product ID Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	0	0	1

D4--D7 Product Identification Nibble. Always returns Ah to uniquely identify this part as the NST175.

D0--D3 Die Revision Nibble. Returns 1h to uniquely identify the revision level as one.

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5.0 TYPICAL APPLICATION

5.1 Application information

The NST175 devices are used to measure the PCB temperature of the location it is mounted. The NST175 feature SMBus, two-wire, and I²C interface compatibility, with the NST175 allowing up to 27 devices on one bus and the NST75 allowing up to eight devices on one bus. The NST175 feature an SMBus Alert function. The NST175 require no external components for operation except for pullup resistors on SCL, SDA, and ALERT, although a 0.1-µF bypass capacitor is recommended.

The sensing device of theNST175 device is the device itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

5.2 Typical application

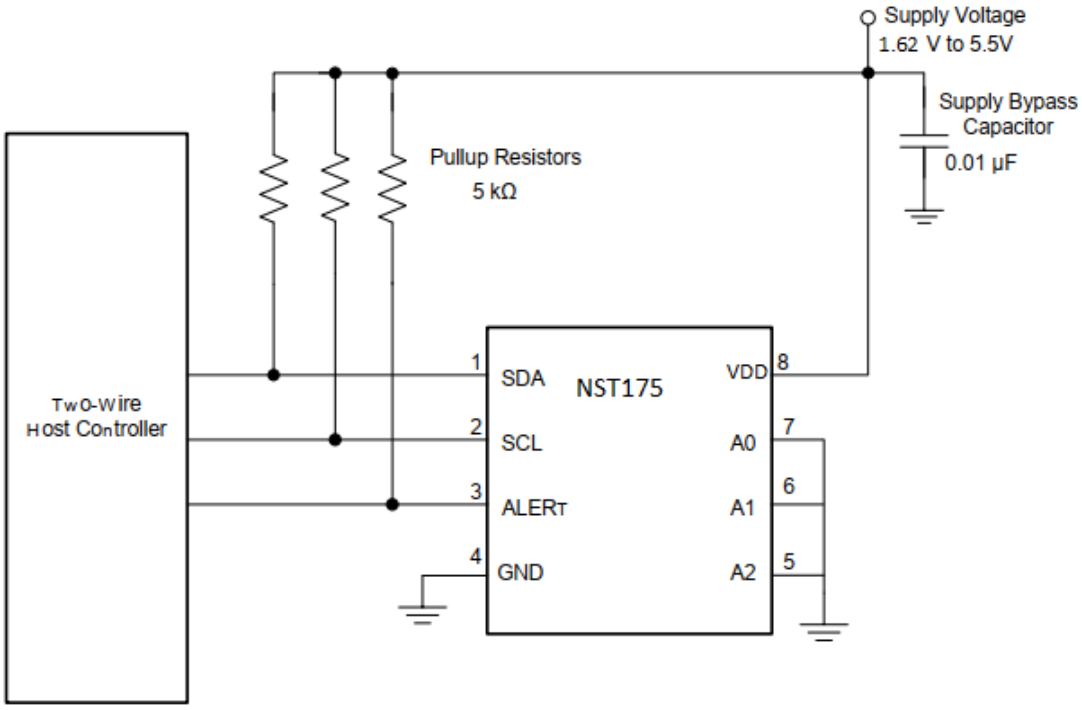


Figure 5.1. Typical Connections of the NST175

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6.0 PACKAGE INFORMATION

6.1 Pinout description

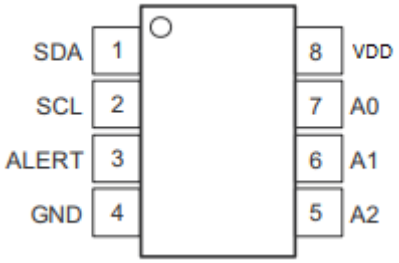


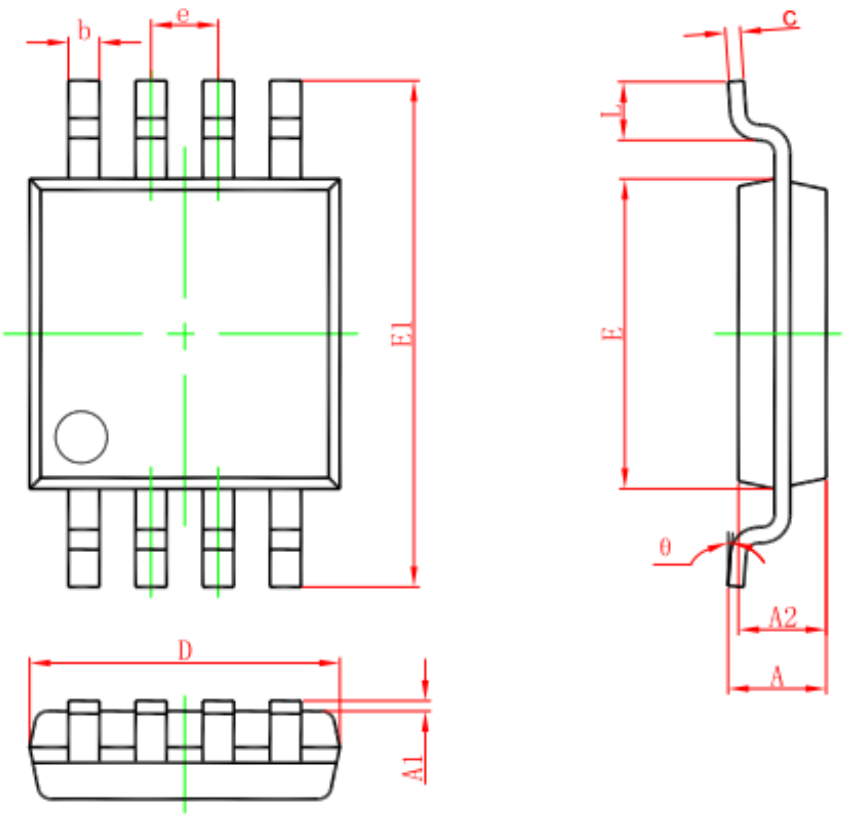
Table 6.1 MSOP(8) function

Pinout		Type	Description
Name	NO.		
SDA	1	I/O	Serial data. Open-drain output; requires a pullup resistor
SCL	2	I	Serial clock. Open-drain output; requires a pullup resistor.
ALERT	3	O	Over temperature alert. Open-drain output; requires a pullup resistor.
GND	4	GND	Ground
A2	5	I	Address select. Connect to GND, VDD or leave these pins floating.
A1	6		
A0	7		
VDD	8	Power	Supply voltage, 1.62 V to 5.5 V

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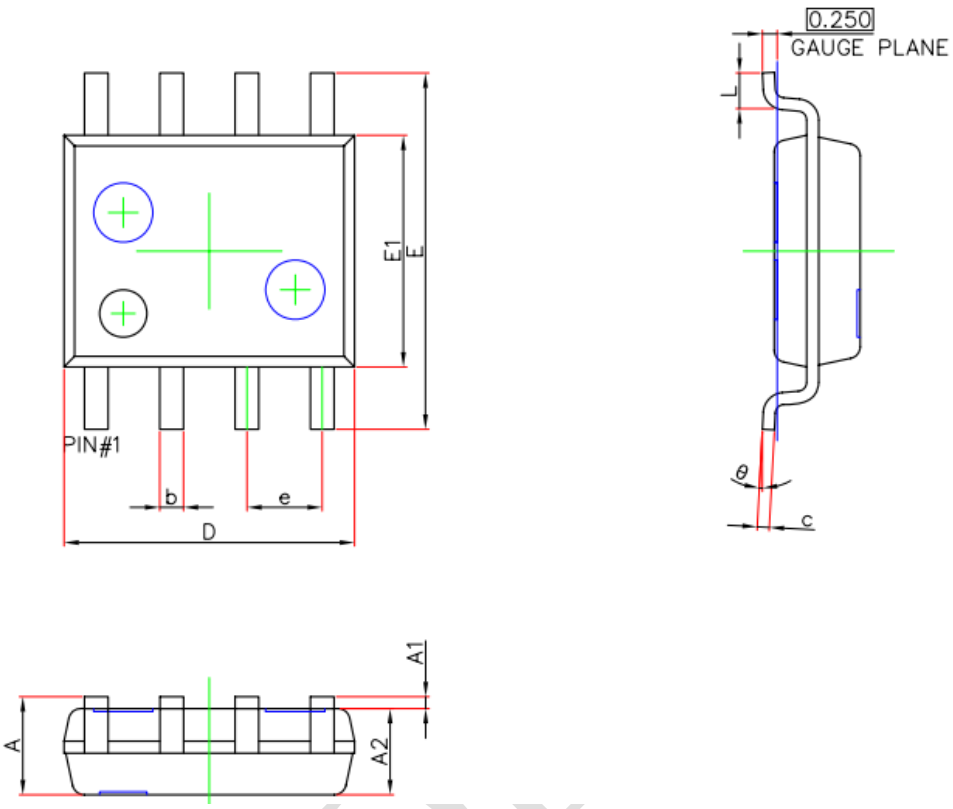
6.2 MSOP（8） package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

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6.3 SOP（8） package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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7.0 ORDER INFORMATION

Type	Unit	Marking	Description
NST175H-QMSR	4000ea/Reel	NST175	MSOP8 package，Reel
NST175H-QSPR	4000ea/Reel	NST175	SOP8 package，Reel

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8.0 REVISION HISTORY

Revision	Description	Date
1.0	Initial Version	2019/4/20
1.1	MP Version	2019/9/12
1.2	Revise ordering infomation	2019/11/27
1.21	Revise ordering information	2020/2/12

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