NSi1306

High Reliability Reinforced Isolated Sigma-Delta Modulator

Datasheet (EN) 1.4

Product Overview

The NSI1306 is a high performance Σ-Δ modulator with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of ±50mV (±64mV full-scale) or ±250mV (±320mV full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The analog input is amplified and continuously sampled by a second-order Σ-Δ modulator and converted to a high speed, single bit data stream. The output data is synchronous to the external clock with a frequency range from 5MHz to 21MHz. By using an appropriate digital filter (such as sinc3 filter) to decimate the bitstream, the device can achieve 16 bits resolution and an 86dB/82.5dB signal to noise ratio (SNR) at 78.125kSPS with a 20MHz master clock.

The fail-safe functions including input common-mode overvoltage detection and missing AVDD detection simplify system-level design and diagnostics.

Key Features

- Up to 5000V_{RMS} Insulation Voltage
- Clock frequency: 5MHz to 21MHz
- ±50mV or ±250mV Linear Input Voltage Range
- Excellent DC Performance:
  - Offset Error: ±50μV or ±100μV (Max)
  - Offset Drift: -0.5~1.5μV/℃ (Max)
  - Gain Error: ±0.2% (Max)
  - Gain Drift: ±40ppm/℃ (Max)
- SNR: 82.5dB or 86dB (Typ)
- High CMTI: 150kV/μs (Typ)
- System-Level Diagnostic Features:
  - AVDD monitoring
  - Input common-mode overvoltage detection
- Operation Temperature: -40℃~125℃
- RoHS-Compliant Packages:
  - SOP8(300mil)
  - SOP16(300mil)

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval IEC60950-1 standard
- DIN VDE V 0884-11:2017-01

Applications

- Shunt current monitoring
- AC motor controls
- Power and solar inverters
- Uninterruptible Power Suppliers
- Automotive onboard chargers

Device Information

Part Number	*Package*	*Body Size*
NSI1306x-DSWVR	SOP8(300mil)	5.85mm × 7.50mm
NSI1306x-DSWR	SOP16(300mil)	10.30mm × 7.50mm

Functional Block Diagrams

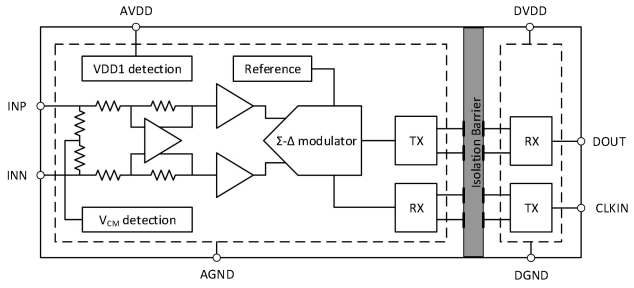


Figure 1. NSi1306 Block Diagram

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1. Pin Configuration and Functions

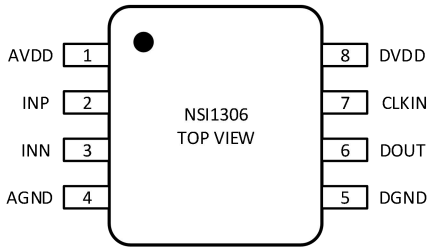


Figure 1.1 NSi1306 Package (SOP8(300mil))

Table 1.1 NSi1306 Pin Configuration and Description

NSi1306 PIN NO.	*SYMBOL*	*FUNCTION*
1	AVDD	Power supply for analog side (3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1306M25 and ±50mV recommended for NSI1306M05)
3	INN	Negative analog input
4	AGND	Analog ground reference
5	DGND	Digital ground reference
6	DOUT	Modulator data output
7	CLKIN	Modulator clock input: 5~21MHz
8	DVDD	Power supply for digital side (3.0V to 5.5V)

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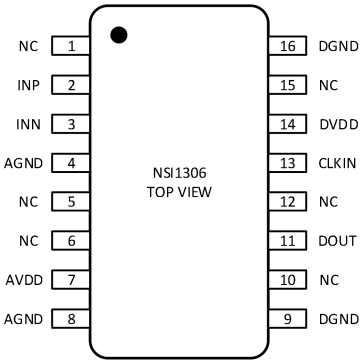


Figure 1.2 NSi1306 Package (SOP16(300mil))

Table 1.2 NSi1306 Pin Configuration and Description

NSi1306 PIN NO.	*SYMBOL*	*FUNCTION*
1	NC	Internally connected to AVDD, this pin can be left floating or tied to AVDD
2	INP	Positive analog input (±250mV recommended for NSI1306M25 and ±50mV recommended for NSI1306M05)
3	INN	Negative analog input
4	AGND	Analog ground reference
5	NC	Not internally connected, this pin can be left floating or tied to AVDD, AGND
6	NC	Not internally connected, this pin can be left floating or tied to AVDD, AGND
7	AVDD	Power supply for analog side (3.0V to 5.5V)
8	AGND	Analog ground reference
9	DGND	Digital ground reference
10	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
11	DOUT	Modulator data output
12	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
13	CLKIN	Modulator clock input: 5~21MHz
14	DVDD	Power supply for digital side (3.0V to 5.5V)
15	NC	Not internally connected, this pin can be left floating or tied to DVDD, DGND
16	DGND	Digital ground reference

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2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	AVDD, DVDD	-0.3		6.5	V
Analog Input Voltage	INP, INN	AGND-6		AVDD+0.5	V
Digital Input Voltage	CLKIN	DGND-0.5		DVDD+0.5	V
Digital Output Voltage	DOUT	DGND-0.5		DVDD+0.5	V
Output current per Output Pin	Io	-10		10	mA
Operating Temperature	T_{OPR}	-40		125	℃
Junction Temperature	T_J	-40		150	℃
Storage Temperature	T_{STG}	-55		150	℃
Electrostatic discharge	HBM (1)	±2000			V
	CDM (2)	±1000			V

(1) Human body model (HBM), per AEC-Q100-002-RevD

(2) Charged device model (CDM), per AEC-Q100-011-RevB

3. Recommended Operating Conditions

Parameters		Symbol	Min	Typ	Max	Unit
Analog Side Power Supply		AVDD	3.0	5.0	5.5	V
Digital Side Power Supply		DVDD	3.0	3.3	5.5	V
NSI1306M05	Differential input voltage before clipping output	$V_{Clipping}$		±64		mV
	Linear differential input full scale voltage	V_{FSR}	-50		50	mV
	Operating common-mode input voltage	V_{CM}	-0.032		0.8	V
NSI1306M25	Differential input voltage before clipping output	$V_{Clipping}$		±320		mV
	Linear differential input full scale voltage	V_{FSR}	-250		250	mV
	Operating common-mode input voltage	V_{CM}	-0.16		0.8	V
Operating Ambient Temperature		T_A	-40		125	℃

4. Thermal Information

Parameters	Symbol	SOP8(300mil)	SOP16(300mil)	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	86	82	℃/W

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Parameters	Symbol	SOP8(300mil)	SOP16(300mil)	Unit
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	28	42	℃/W
Junction-to-board thermal resistance	$R_{\theta JB}$	42	46	℃/W
Junction–to-top characterization parameter	Ψ_{JT}	4	12	℃/W
Junction-to-board characterization parameter	Ψ_{JB}	42	46	℃/W

5. Specifications

5.1. Electrical Characteristics: NSI1306M05

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -50mV to +50mV, and INN = AGND = 0V, T_A = -40℃ to 125℃ and sinc³ filter with OSR=256. Unless otherwise noted, Typical values are at CLKIN=20MHz, AVDD = 5V, DVDD = 3.3V, T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.5	15	mA	
Digital Side Supply Current	IDVDD		2	2.5	mA	
AVDD undervoltage detection threshold voltage	$AVDD_{UV}$	2	2.5	3	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	$CMRR_{dc}$		-95		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
	$CMRR_{ac}$		-99		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
Single-ended input resistance	R_{IN}		4.75		kΩ	INN = AGND
Differential input resistance	R_{IND}		4.9		kΩ	
Input capacitance	C_I		2		pF	
Input bias current	I_{IB}	-24	-23	-20	μA	INP = INN = AGND, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift	TCI_{IB}		±2		nA/°C	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	

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Parameters	Symbol	Min	Typ	Max	Unit	Comments
Offset error	E_O	-50	±2.5	50	μV	INP = INN = AGND
Offset error thermal drift	TCE_O	-0.5	±0.15	0.5	μV/°C	
Gain error	E_G	-0.2%	±0.005%	0.2%		
Gain error thermal drift	TCE_G	-30	±10	30	ppm/°C	
Power supply rejection ratio	PSRR		-106		dB	PSRR vs AVDD, at DC
			-104		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR	78	82.5		dB	f_{IN} = 1kHz
Signal to noise and distortion	SINAD	77	82.5		dB	f_{IN} = 1kHz
Total harmonic distortion	THD		-96	-84	dB	f_{IN} = 1kHz
Spurious-free dynamic range	SFDR	86	100		dB	f_{IN} = 1kHz
Digital Input / Output						
Input current	I_{IN}	0		7	μA	DGND ≤ V_{IN} ≤ DVDD
Input capacitance	C_{IN}		5		pF	
Output load capacitance	C_{LOAD}		30		pF	
High-level input voltage	V_{IH}	0.7×DVDD		DVDD+0.3	V	
Low-level input voltage	V_{IL}	-0.3		0.3×DVDD	V	
High-level output voltage	V_{OH}	DVDD-0.1			V	I_{OH} = -20μA
		DVDD-0.4			V	I_{OH} = -4mA
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 20μA
				0.4	V	I_{OL} = 4mA
Timing						
CLKIN clock frequency	f_{CLKIN}	5		21	MHz	
CLKIN clock period	t_{CLKIN}	47.6		200	ns	
CLKIN clock high time	t_{HIGH}	20	25	120	ns	
CLKIN clock low time	t_{LOW}	20	25	120	ns	
DOUT rising time	t_r			5	ns	C_{LOAD} = 15pF
DOUT falling time	t_f			5	ns	C_{LOAD} = 15pF
DOUT hold time after rising edge of CLKIN	t_H	3.5			ns	C_{LOAD} = 15pF
Rising edge of CLKIN to DOUT valid delay	t_D			15	ns	C_{LOAD} = 15pF

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Parameters	Symbol	Min	Typ	Max	Unit	Comments
Analog setting time	t_{AS}		0.5		ms	AVDD step to 3.0 V with DVDD ≥ 3.0 V, to DOUT valid, 0.1% settling

5.2. Electrical Characteristics: NSI1306M25

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = AGND = 0V, T_A = -40℃ to 125℃ and $sinc^3$ filter with OSR=256. Unless otherwise noted, Typical values are at CLKIN=20MHz, AVDD = 5V, DVDD = 3.3V, T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Analog Side Supply Voltage	AVDD	3.0	5.0	5.5	V	
Digital Side Supply Voltage	DVDD	3.0	3.3	5.5	V	
Analog Side Supply Current	IAVDD		11.4	15.1	mA	
Digital Side Supply Current	IDVDD		1.78	2.5	mA	
AVDD undervoltage detection threshold voltage	$AVDD_{UV}$	1.8	2.3	2.7	V	AVDD falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Common-mode rejection ratio	$CMRR_{dc}$		-106		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
	$CMRR_{ac}$		-104		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
Single-ended input resistance	R_{IN}		19		kΩ	INN = AGND
Differential input resistance	R_{IND}		22		kΩ	
Input capacitance	C_I		2		pF	
Input bias current	I_{IB}	-24	-18	-12	μA	INP = INN = AGND, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift	TCI_{IB}		±1		nA/℃	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
DC Accuracy						
Differential nonlinearity	DNL	-0.99		0.99	LSB	
Integral nonlinearity	INL	-4	±1	4	LSB	
Offset error	E_O	-100	±4.5	100	μV	INP = INN = AGND
Offset error thermal drift	TCE_O	-0.5	±0.15	1.5	μV/℃	
Gain error	E_G	-0.2%	±0.005%	0.2%		
Gain error thermal drift	TCE_G	-40	±20	40	ppm/	

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Parameters	Symbol	Min	Typ	Max	Unit	Comments
					℃	
Power supply rejection ratio	PSRR		-100		dB	PSRR vs AVDD, at DC
			-90		dB	PSRR vs AVDD, 100mV and 10kHz ripple
AC Accuracy						
Signal to noise ratio	SNR	82	86		dB	f_{IN} = 1kHz
Signal to noise and distortion	SINAD	82	86		dB	f_{IN} = 1kHz
Total harmonic distortion	THD		-95	-85	dB	f_{IN} = 1kHz
Spurious-free dynamic range	SFDR	83	100		dB	f_{IN} = 1kHz
Digital Input / Output						
Input current	I_{IN}	0		7	μA	DGND ≤ V_{IN} ≤ DVDD
Input capacitance	C_{IN}		5		pF	
Output load capacitance	C_{LOAD}		30		pF	
High-level input voltage	V_{IH}	0.7×DVDD		DVDD+0.3	V	
Low-level input voltage	V_{IL}	-0.3		0.3×DVDD	V	
High-level output voltage	V_{OH}	DVDD-0.1			V	I_{OH} = -20μA
		DVDD-0.4			V	I_{OH} = -4mA
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 20μA
				0.4	V	I_{OL} = 4mA
Timing						
CLKIN clock frequency	f_{CLKIN}	5		21	MHz	
CLKIN clock period	t_{CLKIN}	47.6		200	ns	
CLKIN clock high time	t_{HIGH}	20	25	120	ns	
CLKIN clock low time	t_{LOW}	20	25	120	ns	
DOUT rising time	t_r			5	ns	C_{LOAD} = 15pF
DOUT falling time	t_f			5	ns	C_{LOAD} = 15pF
DOUT hold time after rising edge of CLKIN	t_H	3.5			ns	C_{LOAD} = 15pF
Rising edge of CLKIN to DOUT valid delay	t_D			15	ns	C_{LOAD} = 15pF
Analog setting time	t_{AS}		0.5		ms	AVDD step to 3.0 V with DVDD ≥ 3.0 V, to DOUT valid, 0.1% settling

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5.3. Typical Performance Characteristics

Unless otherwise noted, test at AVDD = 5V, DVDD = 3.3V, Vin = -250mV to 250mV (NSI1306M25) or -50mV to 50mV (NSI1306M05), CLKIN=20MHz, and sinc^3 filter with OSR=256.

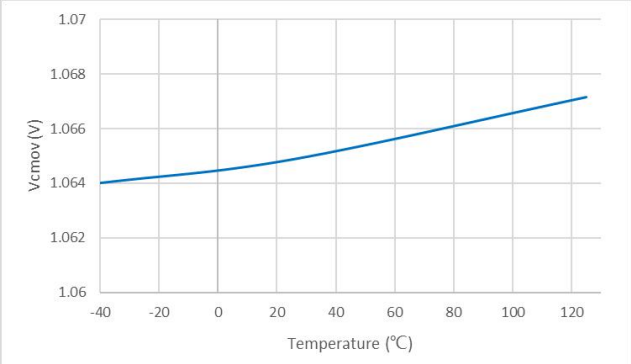


Figure 5.1 Common-Mode Overvoltage Detection Level vs Temperature

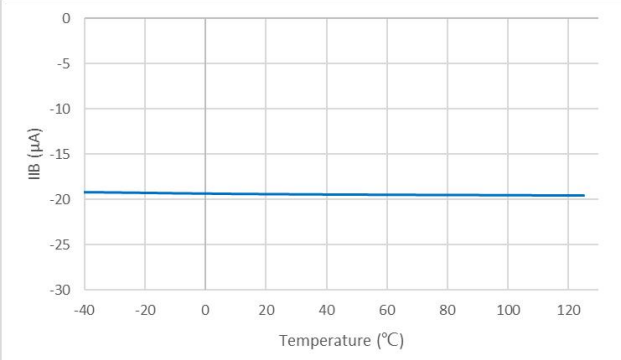


Figure 5.2 Input Bias Current vs Temperature

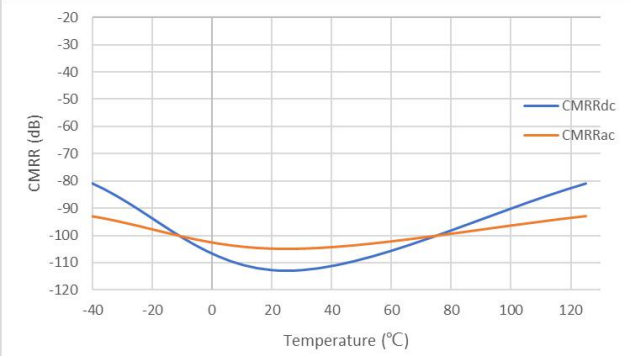


Figure 5.3 Common-Mode Rejection Ratio vs Temperature

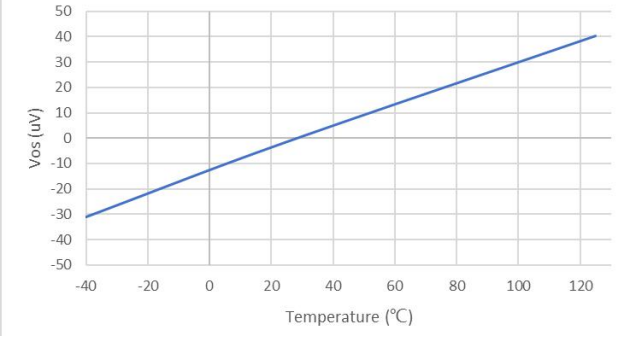


Figure 5.4 Input Offset Voltage vs Temperature

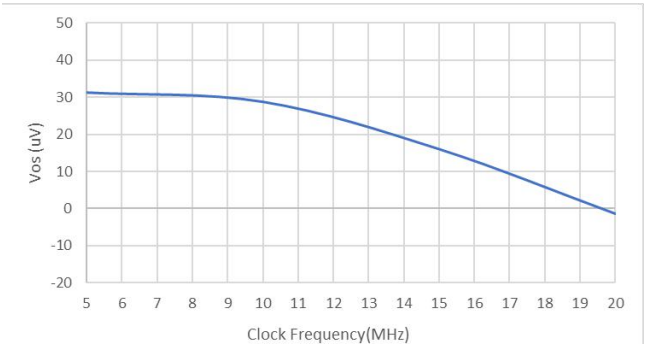


Figure 5.5 Input Offset Voltage vs Clock Frequency

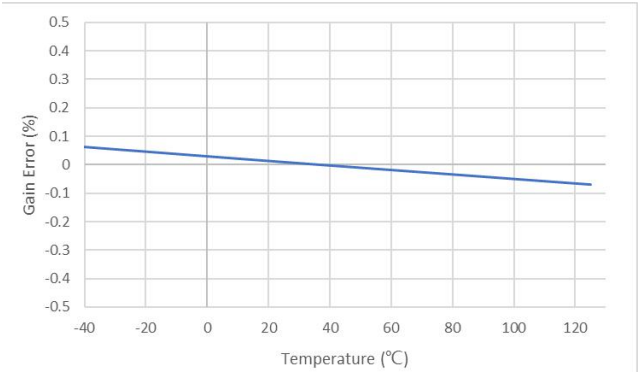


Figure 5.6 Gain Error vs Temperature

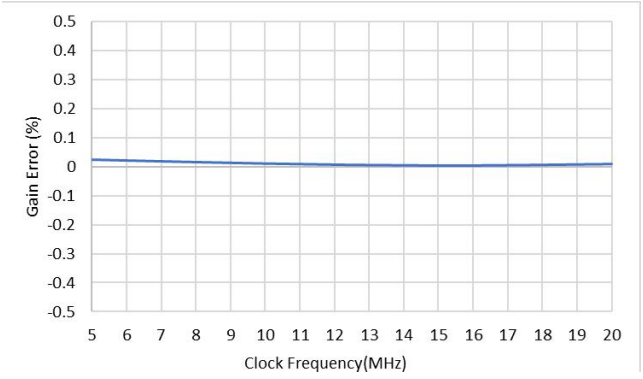


Figure 5.7 Gain Error vs Clock Frequency

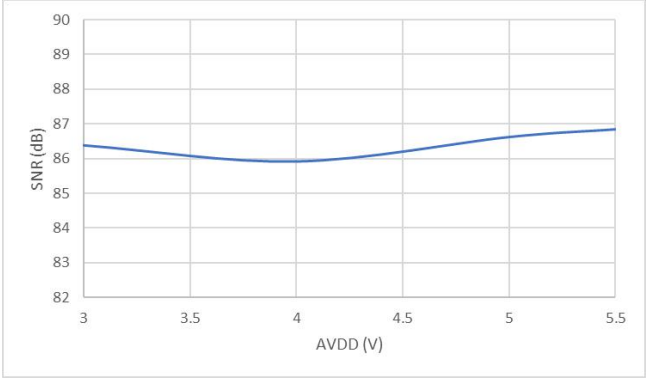


Figure 5.8 Signal-to-Noise Ratio vs Analog Side Supply Voltage

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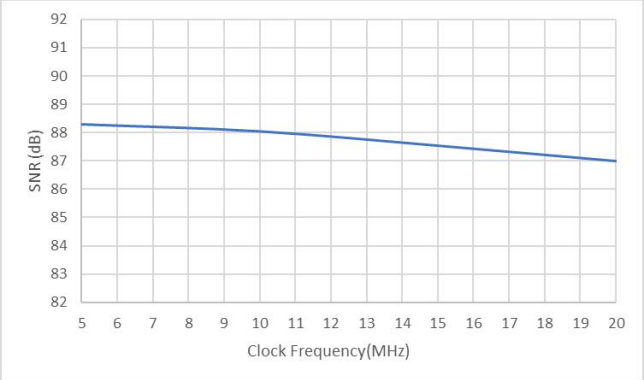


Figure 5.9 Signal-to-Noise Ratio vs Clock Frequency

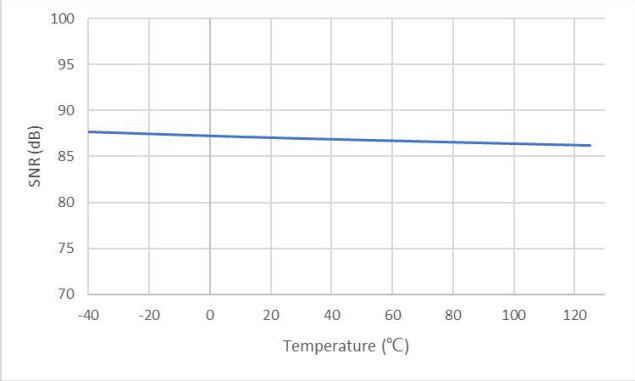


Figure 5.10 Signal-to-Noise Ratio vs Temperature

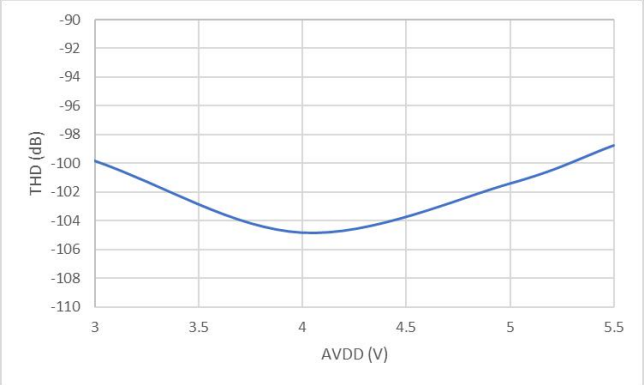


Figure 5.11 Total Harmonic Distortion vs Analog Side Supply Voltage

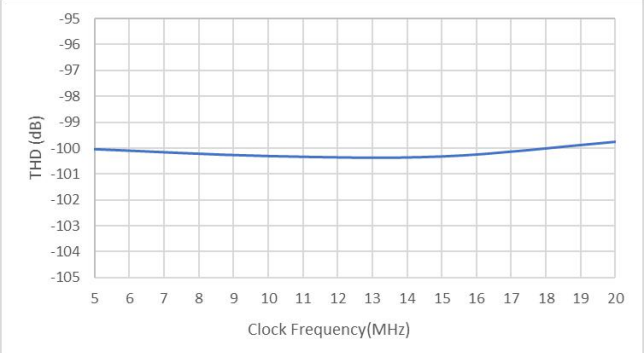


Figure 5.12 Total Harmonic Distortion vs Clock Frequency

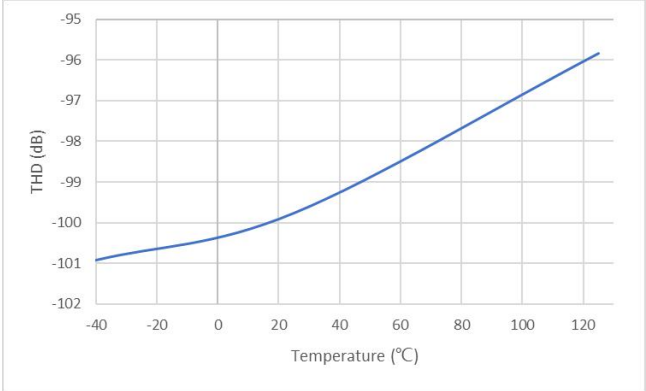


Figure 5.13 Total Harmonic Distortion vs Temperature

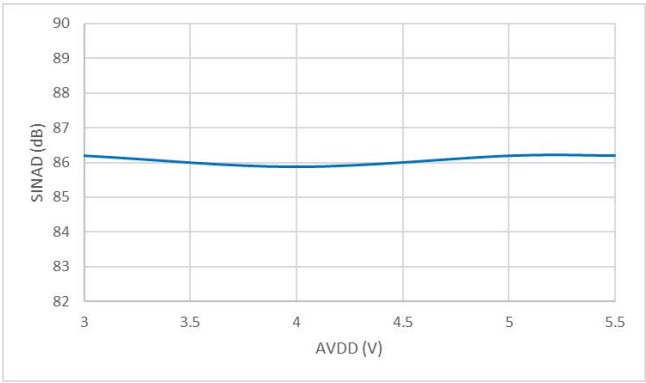


Figure 5.14 Signal-to-Noise + Distortion vs Analog Side Supply Voltage

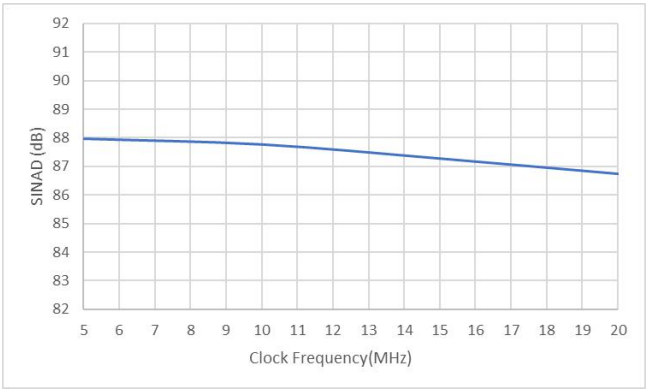


Figure 5.15 Signal-to-Noise + Distortion vs Clock Frequency

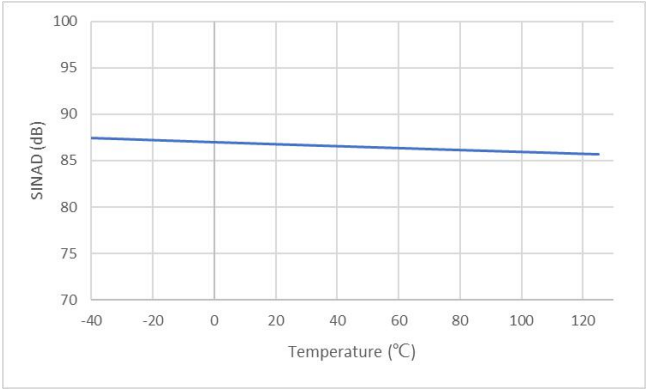


Figure 5.16 Signal-to-Noise + Distortion vs Temperature

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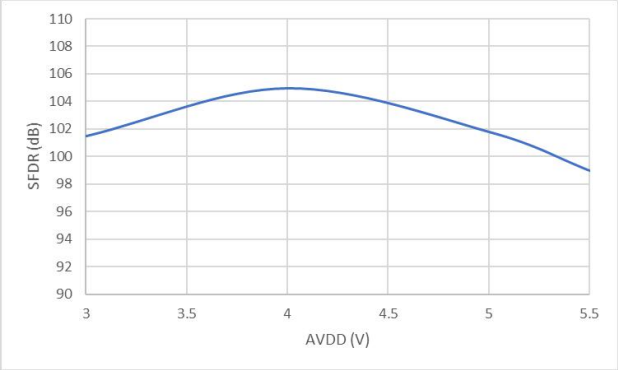


Figure 5.17 Spurious-Free Dynamic Range vs Analog Side Supply Voltage

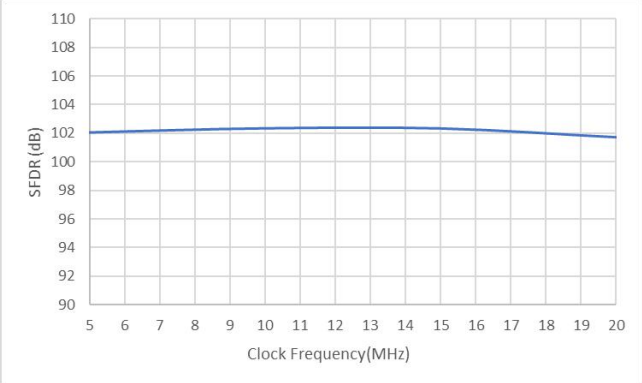


Figure 5.18 Spurious-Free Dynamic Range vs Clock Frequency

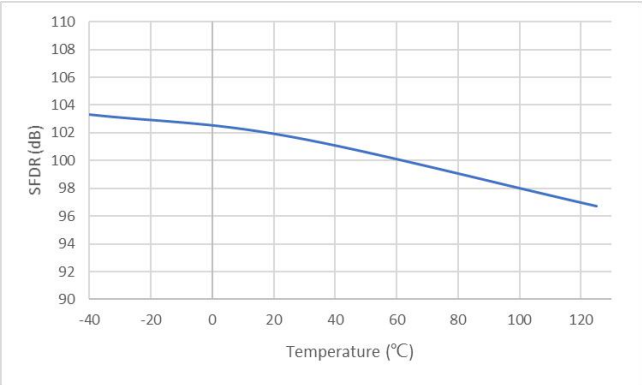


Figure 5.19 Spurious-Free Dynamic Range vs Temperature

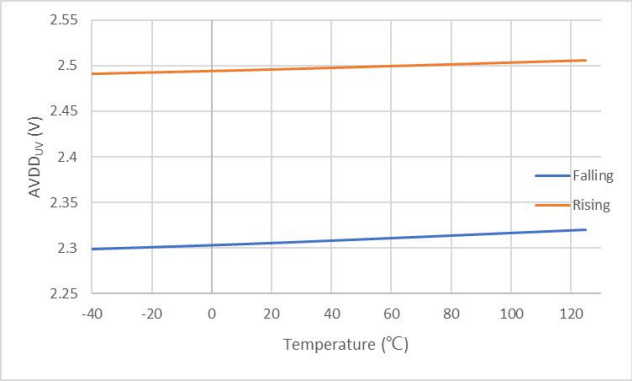


Figure 5.20 Analog Side Under-Voltage Detection Level vs Temperature

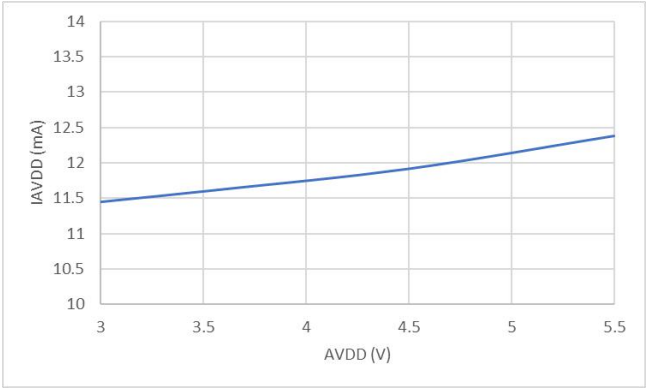


Figure 5.21 Analog Side Supply Current vs Supply Voltage

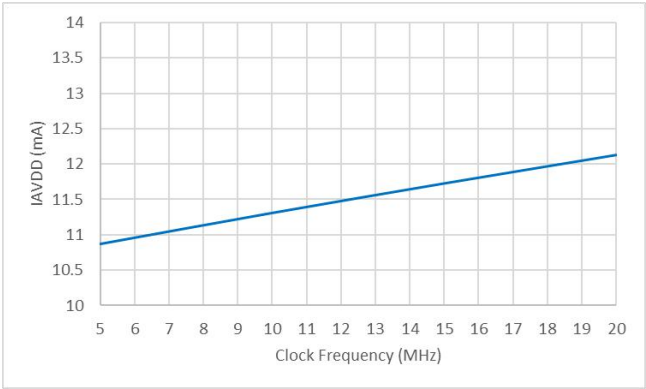


Figure 5.22 Analog Side Supply Current vs Clock Frequency

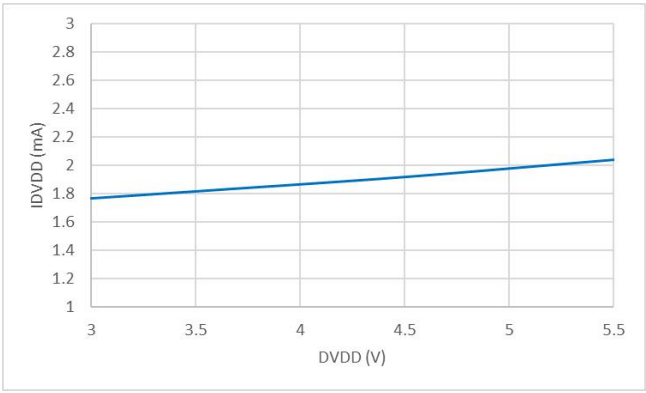


Figure 5.23 Digital Side Supply Current vs Supply Voltage

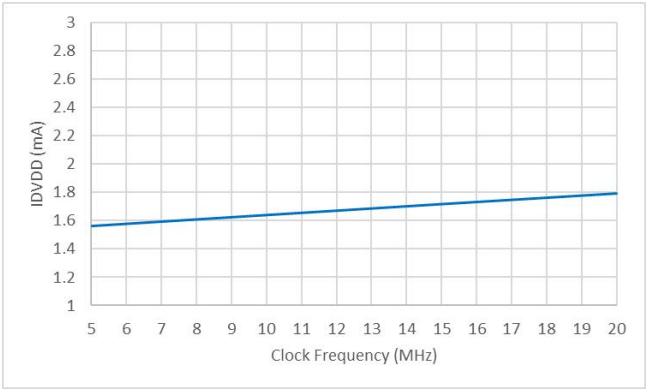


Figure 5.24 Digital Side Supply Current vs Clock Frequency

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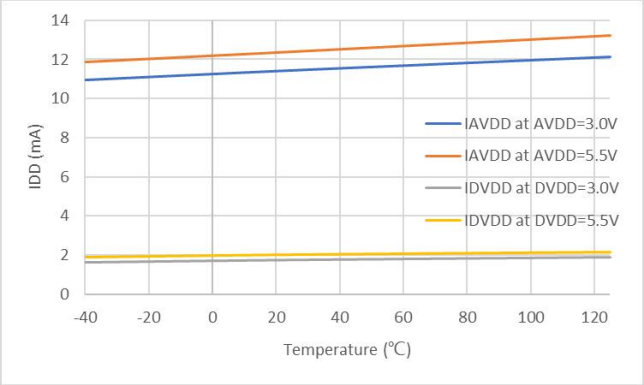


Figure 5.25 Supply Current vs Temperature

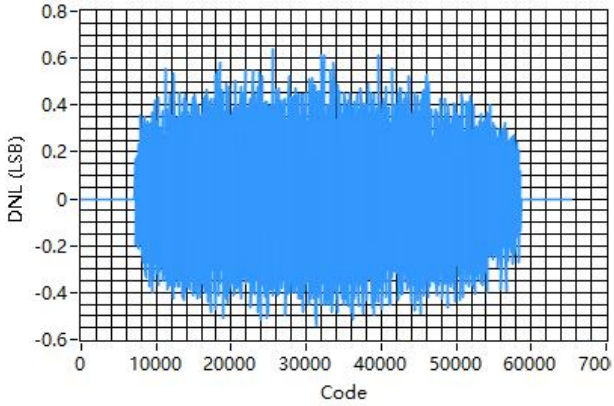


Figure 5.26 Typical Differential Nonlinearity

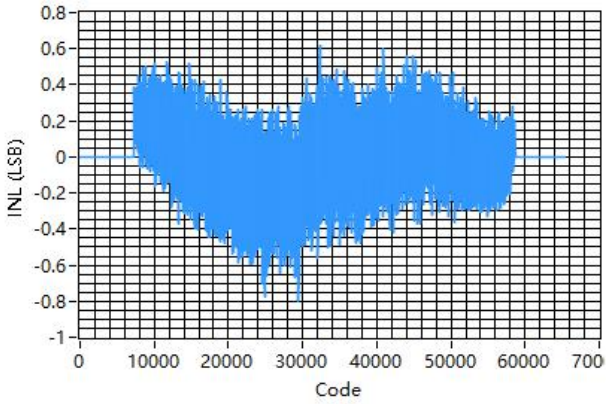


Figure 5.27 Typical Integral Nonlinearity

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6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	CLR	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	32	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

6.2. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
DIN VDE 0110			SOW8	SOW16	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 400Vrms			I to IV	I to IV	
Climatic Classification			40/125/21	40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive isolation voltage		V_{IORM}	2121	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	1500	V_{RMS}
	DC Voltage		2121	2121	V_{DC}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	3977	3977	V_{PEAK}
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	V_{IORM} × 1.6 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	3394	3394	V_{PEAK}
After Input and /or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2= $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	2545	2545	V_{PEAK}
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	8000	8000	V_{PEAK}

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Description	Test Condition	Symbol	Value		Unit
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST}=V_{IOSM} \times 1.6$	V_{IOSM}	6250	6250	V_{PEAK}
Isolation resistance	VIO =500V, $T_{amb}=T_s$	R_{IO}	$>10^9$	$>10^9$	Ω
	VIO =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	0.8	pF
Safety input, output, or total power	V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Ps	1430	1524	mW
Safety input, output, or supply current	θ_{JA} = 86℃/W for SOP8, V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Is	260	/	mA
	θ_{JA} = 82℃/W for SOP16, V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃		/	277	mA
Maximum safety temperature		Ts	150	150	℃
UL1577					
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	V_{ISO}	5000	5000	V_{RMS}

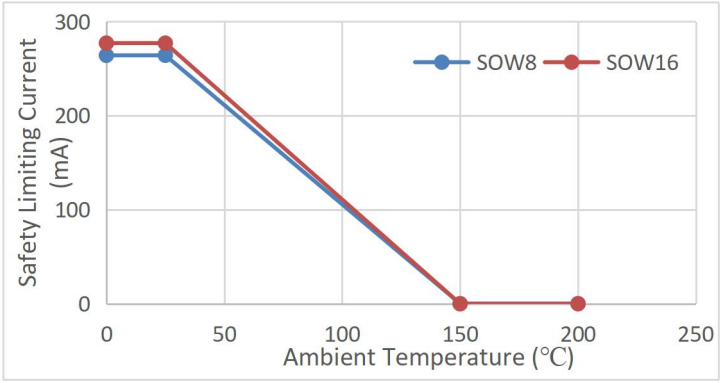


Figure 6.1 NSi1306 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSi1306 are approved or pending approval by the organizations listed in table.

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforce Insulation 2121Vpeak, V_{IOSM}=6250Vpeak	Reinforced insulation
Certificate No.E500602	Certificate No.E500602 for	Certificate No.40052820	CQC20001264939

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UL		VDE	CQC
	SOW8 package File pending for SOW16 package		

7. Function Description

7.1. Overview

The NSI1306 is a high performance isolated modulator that accept fully-differential input. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ-Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator convert the analog input signal to a digital bitstream. The drivers (called TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier that separate external clock, as shown in the Functional Block Diagram.

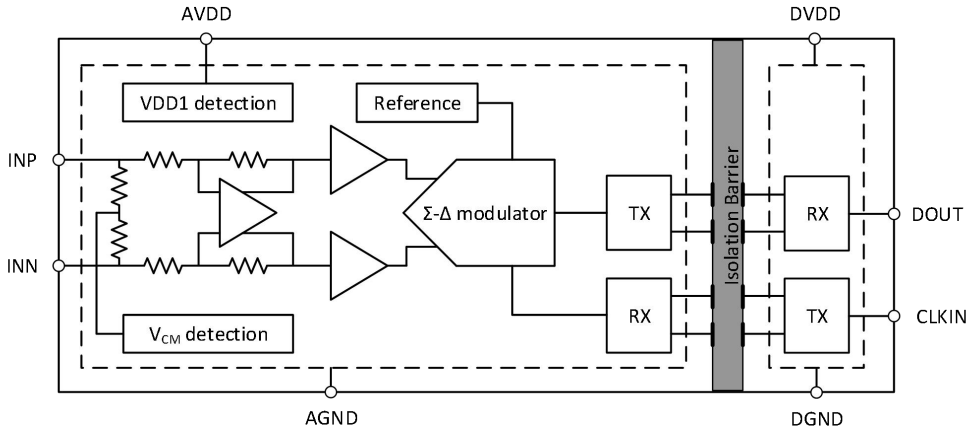


Figure 7.1 Function Block Diagram

7.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range AGND – 6 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

7.3. Digital Input

The digital input refers to clock signal which provides the clock for modulator conversion and output data frame clock. The clock signal should be supplied by an external source with a frequency range from 5MHz to 21MHz.

7.4. Digital Output

The digital output provides a stream of ones and zeros that can accurately represents the analog input voltage. Within the linear input range, the density of ones in the bitstream is proportional to the input voltage.

Ideally for a 0V input signal, the modulator outputs a bitstream with 50% high time. For a 250mV input signal (for the NSI1306M25), the modulator outputs a bitstream with 89.06% high time. For a -250mV input signal (for the NSI1306M25), the modulator outputs a bitstream with 10.94% high time.

If the input signal is greater than or equal to 320mV (64 mV for the NSI1306x05), the modulator clips with a steam of all ones. If the input signal is less than or equal to -320mV (–64 mV for the NSI1306x05), the output of the modulator clips with a stream of all zeros. In this case, however, the NSI1306 generates a single 0 (if the input is at positive full-scale) or 1 every 128 clock cycles to indicate proper device function (see section7.5 for more details).

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7.5. Fail-safe Output

NSI1306 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe function will be activated in following conditions:

- When the undervoltage of AVDD is detected (AVDD< $AVDD_{UV}$), DOUT pin output a bitstream of all logic zeros, as shown in Figure 7.2.
- When the overvoltage of common-mode input voltage is detected (V_{CM}>V_{CMov}), DOUT pin output a bitstream of all logic ones, as shown in Figure 7.2.

NOTE: If both of the faults above occur at the same time, DOUT pin output a bitstream of all logic zeros. (AVDD missing has a higher priority).

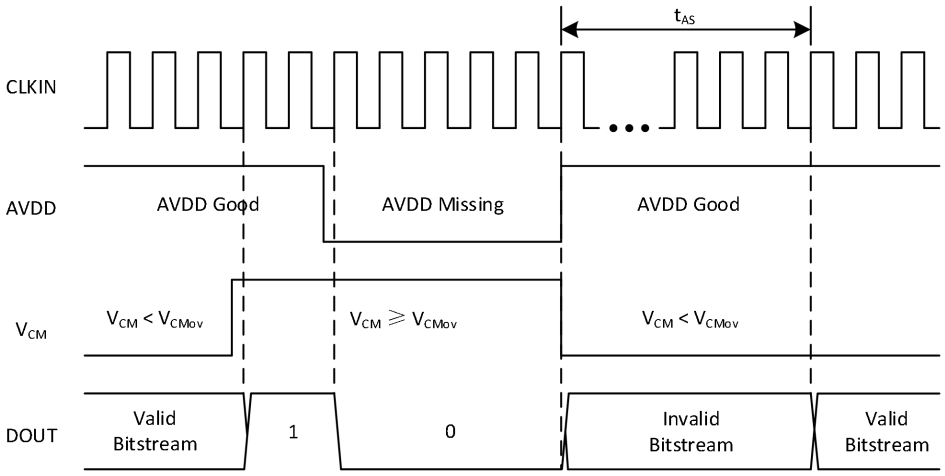


Figure 7.2 Fail-safe output

If an overrange input signal is applied to the NSI1306 ($V_{IN} \geq V_{Clipping}$), the output generates a single 0 or 1 every 128 clock cycles, as shown in Figure 7.3.

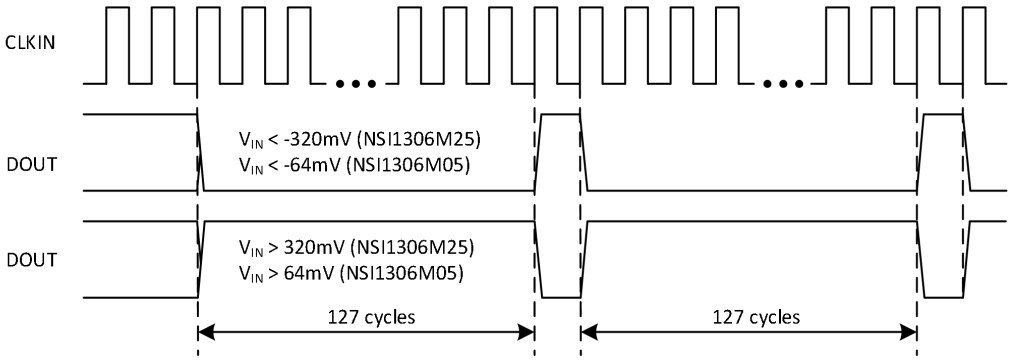


Figure 7.3 Overrange output

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8. Application Note

8.1. Typical Application Circuit

NSI1306 is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 8.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1306 through a RC filter. The internal second-order sigma-delta modulator converts the analog input to a single-bit output stream. The external digital system provides a clock source for the modulator and a digital filter for decimation and quantization noise filtering.

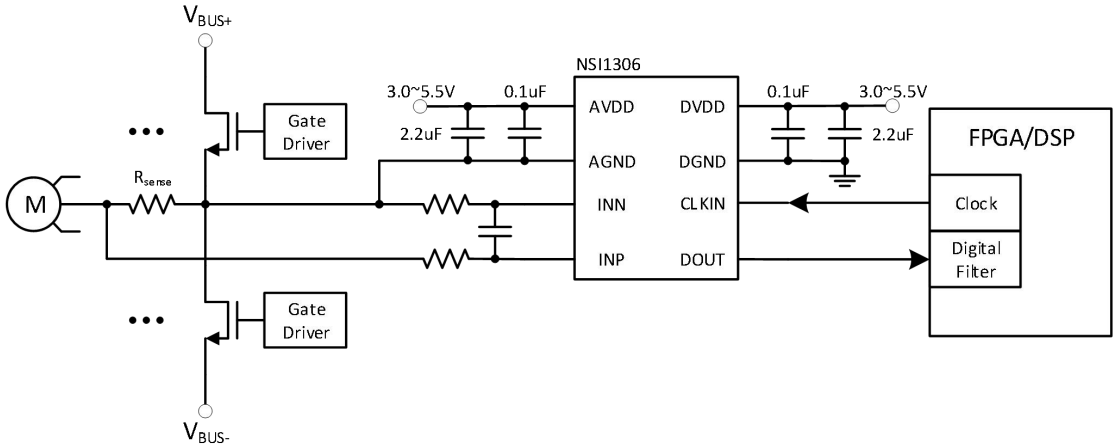


Figure 8.1 Typical application circuit in phase current sensing

8.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq FSR$.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

8.3. Digital Filter

The Σ-Δ modulator a characteristics of noise shaping. Most of the quantization noise is pushed from a low frequency to a higher frequency.

In order to reduce higher-frequency quantization noise, the modulator output is fed to the digital low-pass filter. Subsequently, the signal of interest passes through to the output of the digital filter, while much of the higher-frequency quantization noise is filtered out.

The digital filter serves another function – decimation. It creates a digital output code from the bitstream that the modulator outputs. The ratio of the modulator rate (f_{MOD}) of the delta-sigma modulator to its output data rate (f_{DR}) is the oversampling ratio (OSR). The relationship between f_{DR} and f_{MOD} is:

$$f_{DR} = f_{MOD} / OSR \qquad \text{Equation 8.1}$$

A sinc3 filter is recommended since it's simple and requires less hardware resources. Equation 8.2 describes the transfer function of a sinc filter.

$$H(Z) = \left(\frac{1}{DR}\frac{(1-Z^{-DR})}{(1-Z^{-1})}\right)^{N} \qquad \text{Equation 8.2}$$

where:

DR is the decimation rate;

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N is the sinc filter order.

The filter can be implemented in an FPGA or DSP. The sinc filter creates a digital output code by taking a multi-order moving average of the modulator output over a certain number of modulator clock periods.

The higher the decimation rate, the higher the conversion accuracy, and the lower the output data rate. So, there is a trade-off between accuracy and data rate. All the characterization in this datasheet is tested with a sinc3 filter with an oversampling ratio (OSR) of 256.

The output data size is expressed in Equation 8.3. The 16 most significant bits are used to return a 16-bit result.

$$Data\ Size = N \times \log_2 DR \qquad \text{Equation 8.3}$$

The filter characteristics for a third-order sinc filter are summarized in Table 8.1.

Table 8.1 Sinc3 Filter Characteristics for 20 MHz CLKIN

Decimation Rate (DR)	*Data Output Rate (kHz)*	*Data Size (bits)*	*Filter Response (kHz)*
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

8.4. PCB Layout

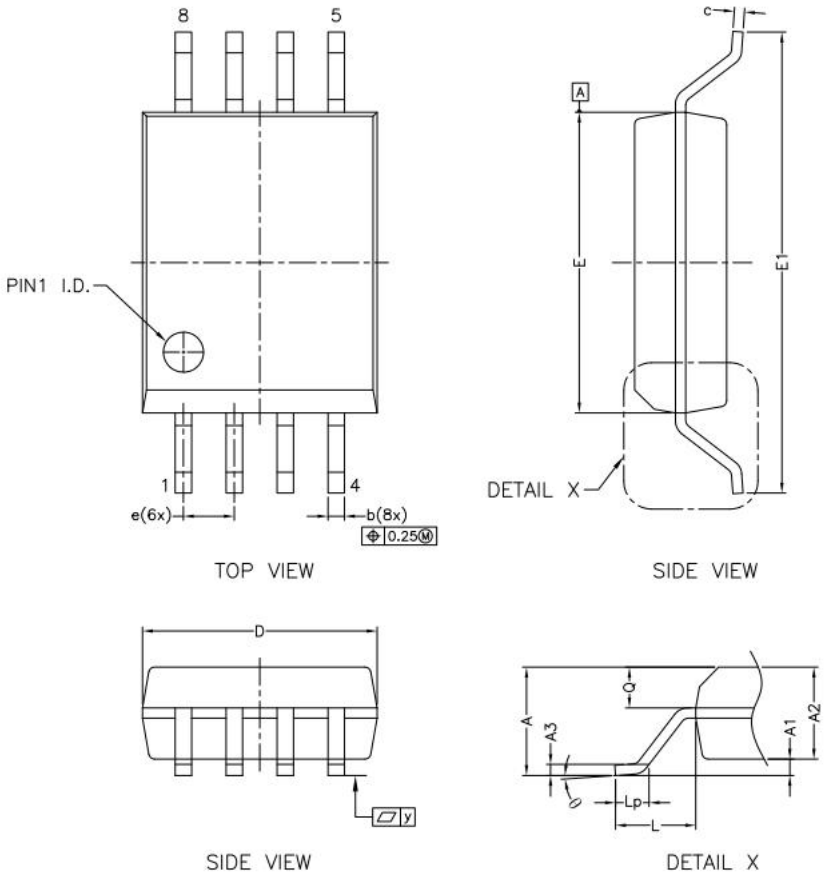
There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1306 requires a 0.1μF bypass capacitor between AVDD and AGND, DVDD and DGND. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1306. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1306. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

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9. Package Information



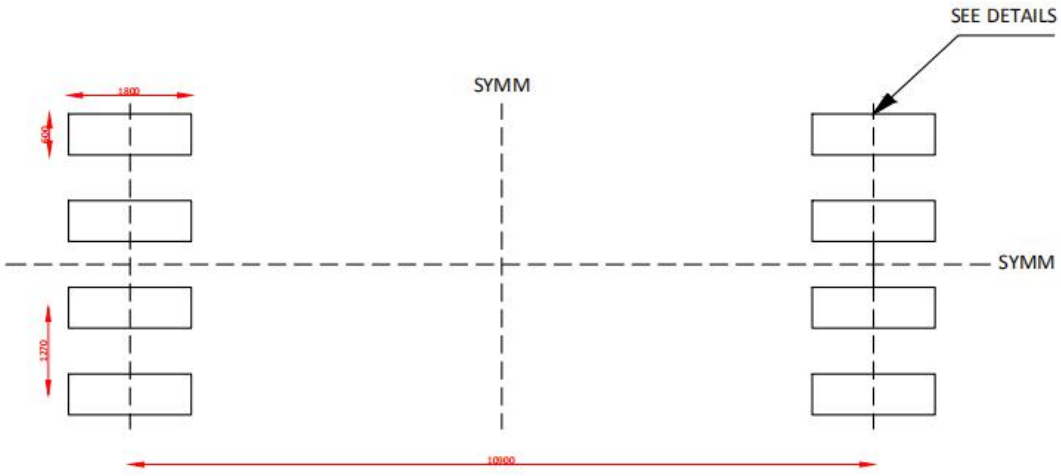
* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

Figure 9.1 SOW8 Package Shape and Dimension in millimeters

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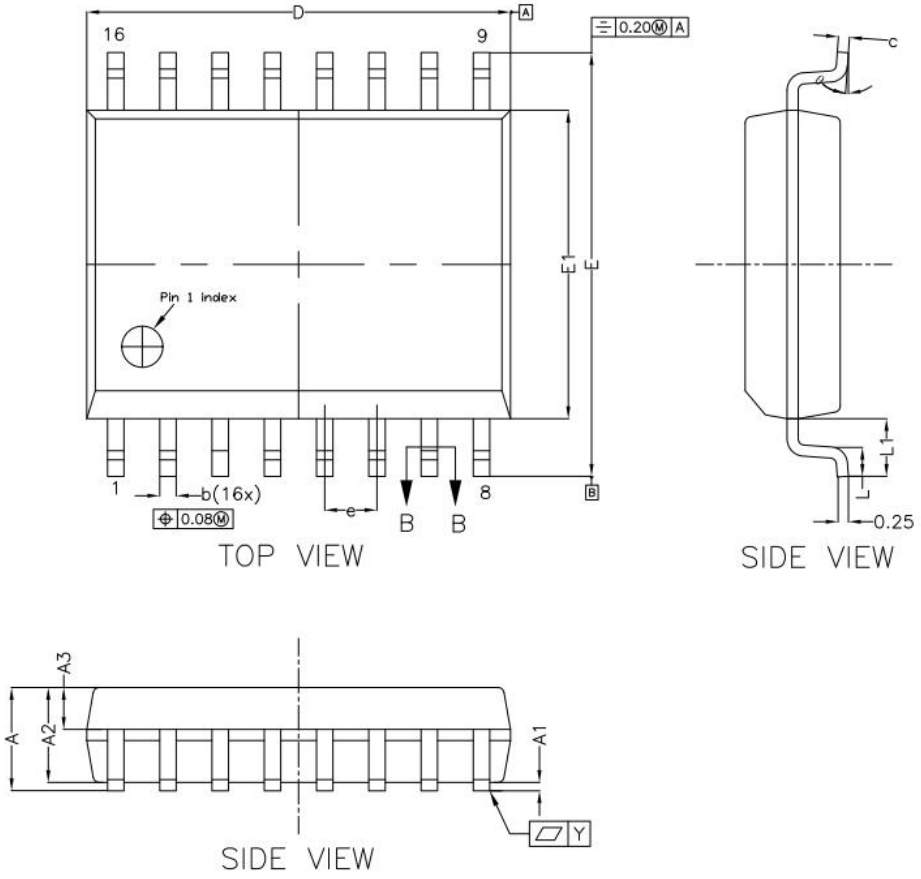
LAND PATTERN EXAMPLE(um)



Figure 9.2 SOW8 Package Board Layout Example

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* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	030
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 9.3 SOW16 package shape and dimension in millimeters

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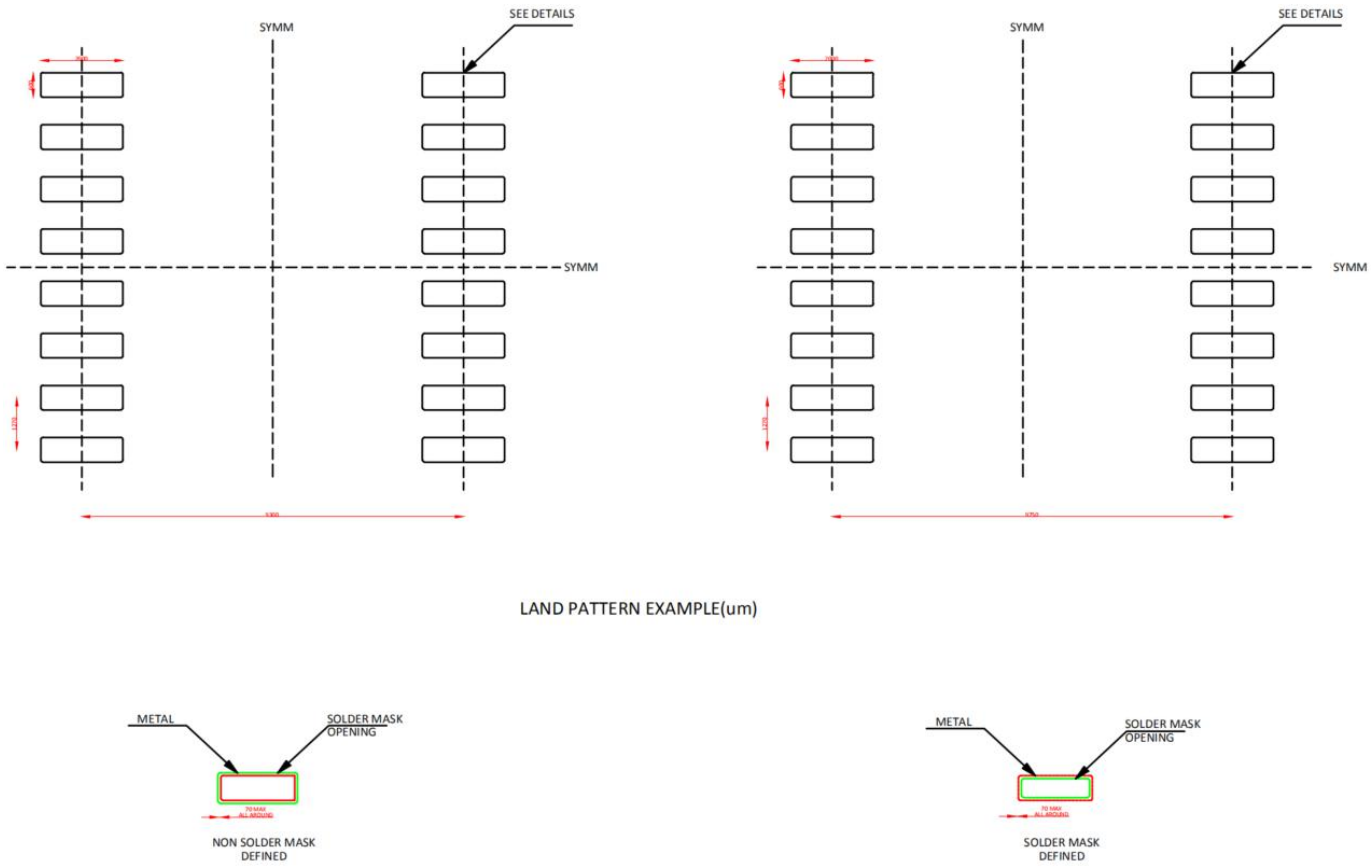


Figure 9.4 SOW16 Package Board Layout Example

10. Ordering Information

Part No.	Isolation Rating(kV)	Linear Input Range(mV)	Moisture Sensitivity Level	Temperature	Automotive	Package Type	Package Drawing	SPQ
NSI1306M05-DSWVR	5	-50 ~ 50	Level-3	-40 to 125℃	NO	SOP8 (300mil)	SOW8	1000
NSI1306M25-DSWVR	5	-250 ~ 250	Level-3	-40 to 125℃	NO	SOP8 (300mil)	SOW8	1000
NSI1306M05-DSWR	5	-50 ~ 50	Level-2	-40 to 125℃	NO	SOP16 (300mil)	SOW16	1000
NSI1306M25-DSWR	5	-250 ~ 250	Level-2	-40 to 125℃	NO	SOP16 (300mil)	SOW16	1000
NSI1306M05-Q1SWVR	5	-50 ~ 50	Level-3	-40 to 125℃	Yes	SOP8 (300mil)	SOW8	1000
NSI1306M25-Q1SWVR	5	-250 ~ 250	Level-3	-40 to 125℃	Yes	SOP8 (300mil)	SOW8	1000
NSI1306M05-Q1SWR	5	-50 ~ 50	Level-2	-40 to 125℃	Yes	SOP16 (300mil)	SOW16	1000
NSI1306M25-Q1SWR	5	-250 ~ 250	Level-2	-40 to 125℃	Yes	SOP16 (300mil)	SOW16	1000

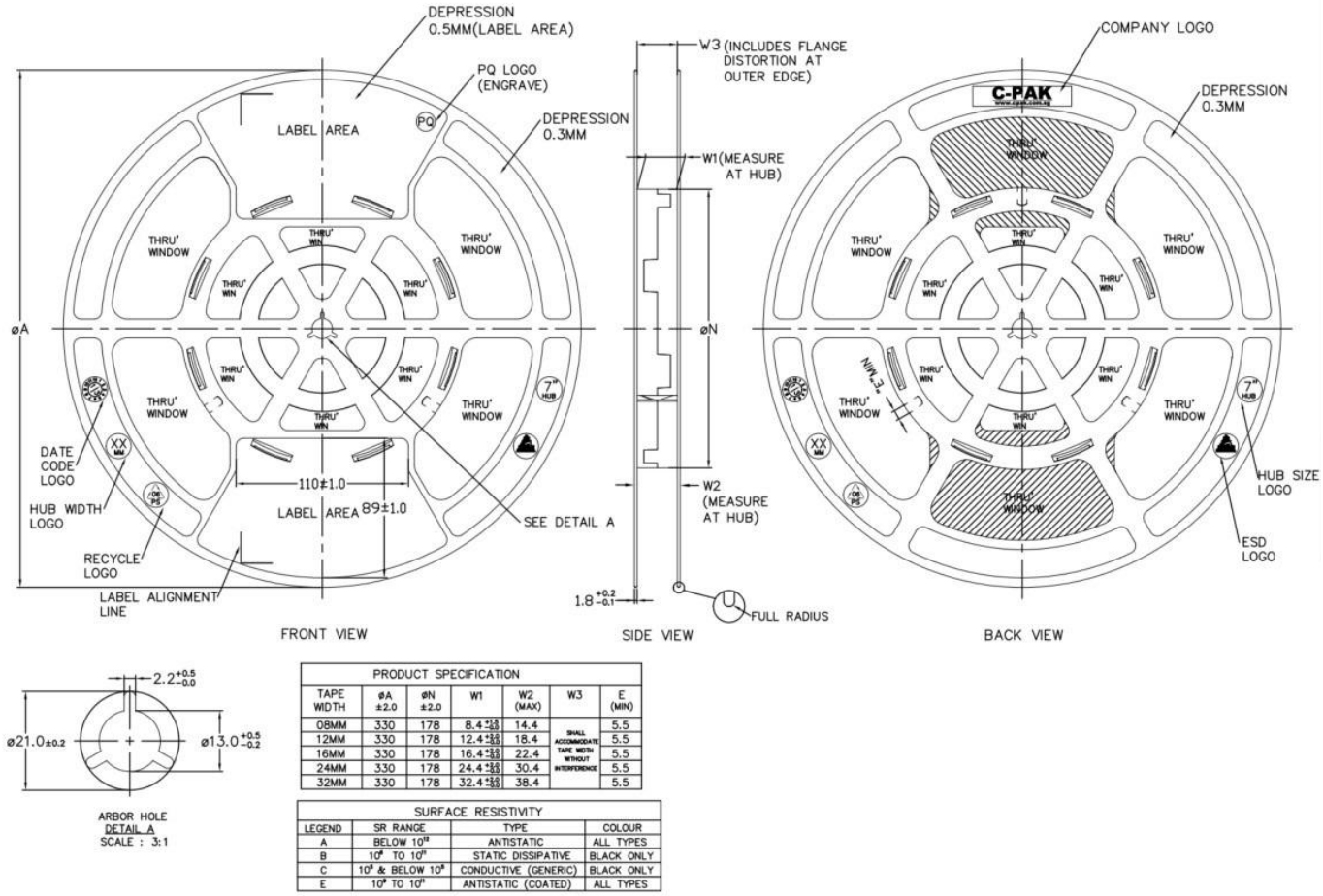
11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSi1306	Click here	Click here	Click here	Click here

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12. Tape and Reel Information



PRODUCT SPECIFICATION

TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY

LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{12}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{3} & BELOW 10^{6}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{6} TO 10^{9}	ANTISTATIC (COATED)	ALL TYPES

Figure 12.1 Tape Information

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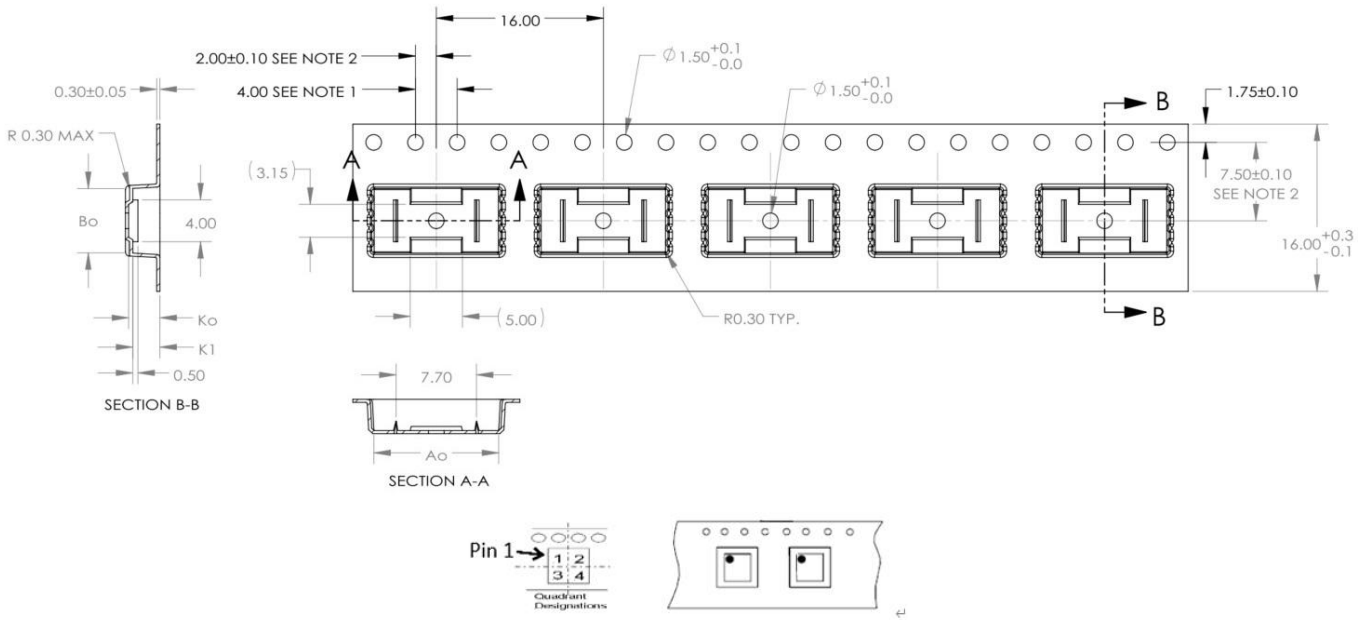
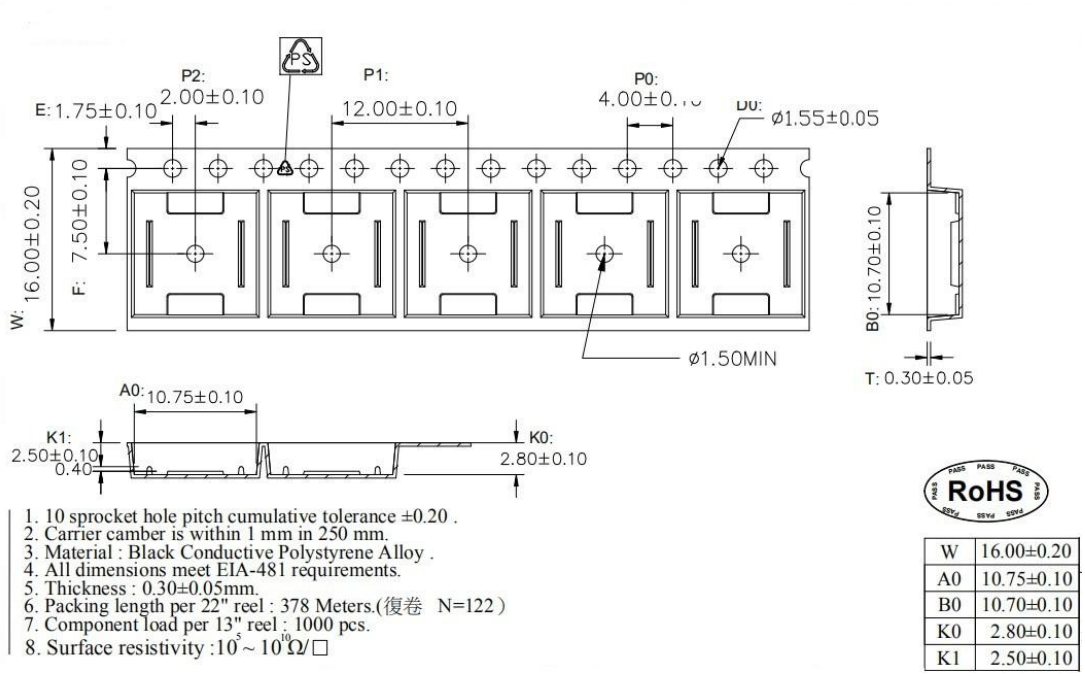


Figure 12.2 Reel Information of SOP8(300mil)



W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

Figure 12.3 Reel Information of SOP16(300mil)

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13. Revision History

Revision	Description	Date
1.0	Initial Release	2020/8/29
1.1	Update VDE Certificate number in 6.3, tape and reel information, and typical application circuit in 8.1	2020/12/28
1.2	Update moisture sensitivity level of NSI1306M05/25 -DSWR Update NSI1306M05 electrical characteristics, add V_{IH} and V_{IL} spec	2021/6/9
1.3	Update description in 7.1 , add SOW8 and SOW16 package layout example	2021/7/8
1.4	Update insulation information in 6.1 and 6.2	2021/7/17

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