MCP Specification

4Gb SLC NAND Flash (X8) + 2Gb LPDDR2 (X32)

4Gb SLC NAND Flash (X8) + 2Gb LPDDR2 (X16)

Nanya Technology Corporation

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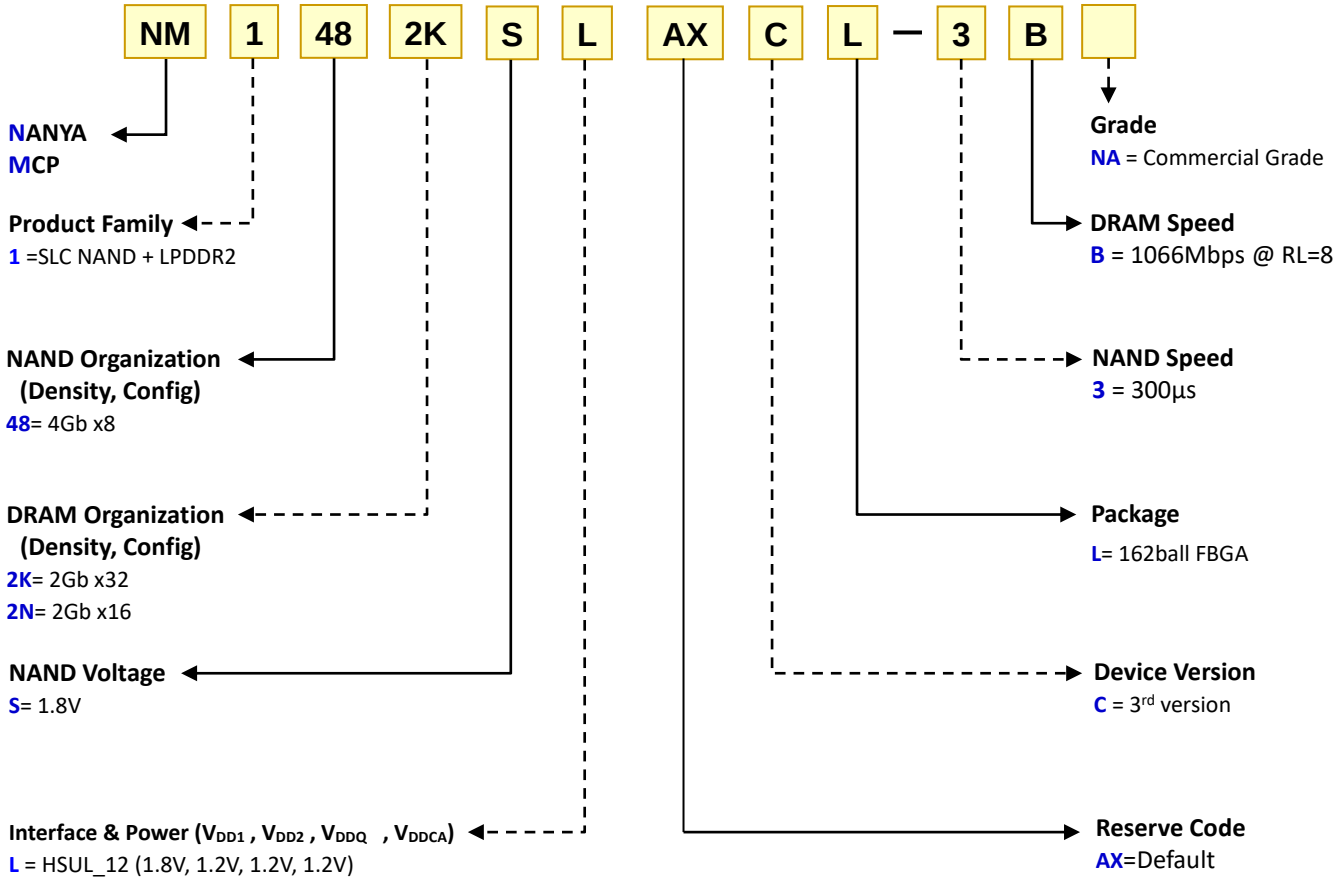
Ordering Information

MCP	NAND				DRAM			
Part Number	Type	Density (Org.)	Program Time	Erase Time	Type	Density (Org.)	Speed	RL
NM1482KSLAXCL-3B	SLC	4Gb (512Mb X 8)	300µs	3.5ms	LPDDR2	2Gb (64Mb X 32)	1066	8
NM1482NSLAXCL-3B[1]	SLC	4Gb (512Mb X 8)	300µs	3.5ms	LPDDR2	2Gb (128Mb X 16)	1066	8

Note 1 Please confirm with NTC for the available schedule.

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NANYA MCP Part Numbering Guide



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Features

MCP

- **Separate SLC NAND and LPDDR2 RAM interfaces**
- **Lead-free (RoHS compliant), Halogen-free and Non-use 5PBTs of TSCA Package :**
  162-ball FBGA 8.00 x 10.50 x 1.00 (mm)
- **Operating temperature range:** –25°C to +85°C

4Gb X8 SLC NAND

- **Voltage Supply(VCC/VCCQ): 1.70V ~ 1.95V**
- **Organization**
  - X8 Memory Cell Array: 4352 x 128K x 8
  - X8 Register: 4352 x 8
  - X8 Page Program: 4352 Bytes
  - X8 Block Erase: (256K + 16K) Bytes
- **Modes**
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy, Multi Page Program, Multi Block Erase, Multi Page Copy, Multi Page Read
- **Mode control**
  - Serial input/output
  - Command control
- **Number of valid blocks**
  - Min 2008 blocks
  - Max 2048 blocks
- **Access time**
  - Cell array to register: 25µs max
  - Serial Read Cycle: 25ns min (CL=30pF)
- **Program/Erase time**
  - Auto Page Program: 300µs/page typical
  - Auto Block Erase: 3.5ms/block typical
- **Operating current**
  - Read (25ns cycle): 30 mA max
  - Program (avg.): 30 mA max
  - Erase (avg.): 30 mA max
  - Standby: 50 µA max
- **8 bit ECC for each 512 Bytes is required.**
- **High Reliability**[1]
  - Endurance: typical 50K cycles (with 8-bit ECC per 512 Byte)
  - Data Retention: 10 Years

2Gb X16/X32 LPDDR2

- **Speed, Addressing and Retention Specification**

Organization	128Mb x 16	64Mb x 32
Speed Grade	1066 / RL=8	1066 / RL=8
Device Type	S4B	S4B
Number of Banks	8	8
Bank Address	BA0-BA2	BA0-BA2
Row	R0-R13	R0-R13
Column	C0-C9	C0-C8
tREFI (us)	3.9	3.9

- **Basis LPDDR2 Compliant**
  - Low Power Consumption
  - Double-data rate on DQs, DQS, DM and CA bus
  - 4n Prefetch Architecture
- **HSUL12 interface and Power Supply**
  - VDD1= 1.70 to 1.95V
  - VDD2/VDDQ/VDDCA = 1.14 to 1.3V
- **Signal Integrity**
  - Configurable DS for system compatibility
  - ZQ calibration for the accuracy of output driver strength over Process, Voltage and Temperature
- **Training for Signals' Synchronization**
  - DQ Calibration offering specific DQ output patterns
- **Data Integrity**
  - DRAM built-in Temperature Sensor for Temperature Compensated Self Refresh (TCSR)
  - Auto Refresh, Self Refresh and PASR Modes
- **Power Saving Modes**
  - Deep Power Down Mode (DPD)
  - Partial Array Self Refresh (PASR)
  - Clock Stop capability during idle period
- **Programmable Function**
  - Output Drive Impedance (34.3/40/48/60/80/120)
  - Burst Lengths (4/8/16)
  - Burst Type (Sequential/Interleaved)
  - Read Latency (3/4/5/6/7/8),Write Latency (1/2/3/4)
  - nWR (3/4/5/6/7/8)

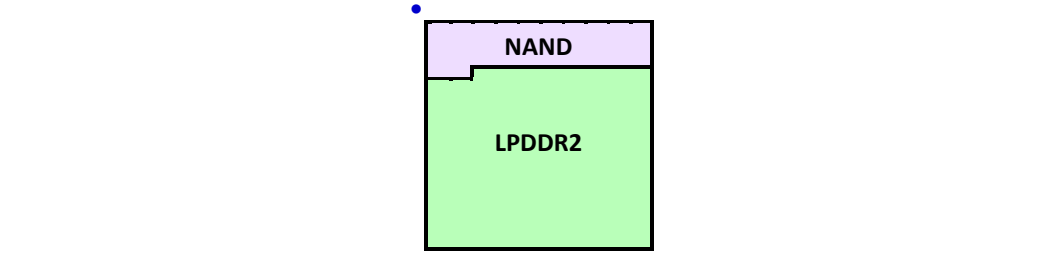
NOTE 1 Please refer to application note item 18.

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Ball Assignment – (162b Flash X 8 + DRAM X 32)

Part Number: NM1482KSLAXCL-XXX

Top View, A1 in Top Left Corner



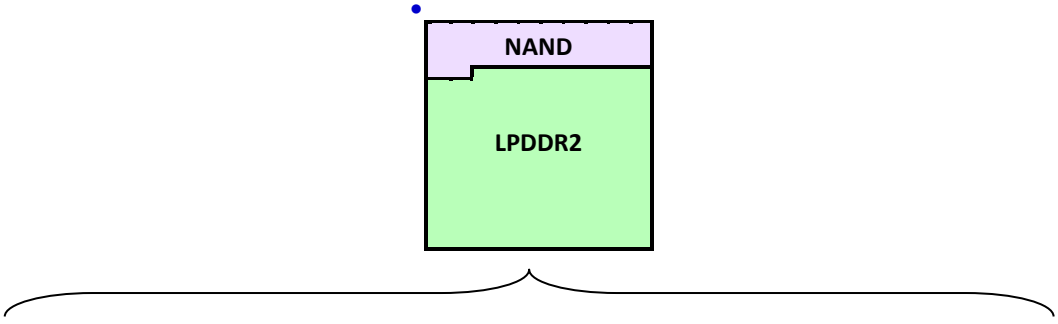
	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU	$\overline{WP}$	CLE	VCC	I/O 4	I/O 7	VCC	DNU	DNU	A
B	DNU	VCC	NC	ALE	$\overline{RE}$	I/O 5	NC	NC	VSS	DNU	B
C	NC	I/O 1	I/O 3	$\overline{WE}$	R/$\overline{B}$	I/O 6	NB	NB	NB	NB	C
D	NC	I/O 0	I/O 2	$\overline{CE}$	NC	NC	NB	NB	NB	NB	D
E	VSS	NC	NC	NB	VDD2	VDD1	DQ31	DQ29	DQ26	DNU	E
F	VDD1	VSS	NC	NB	VSS	VSS	VDDQ	DQ25	VSS	VDDQ	F
G	VSS	VDD2	ZQ	NB	VDDQ	DQ30	DQ27	DQS3	$\overline{DQS3}$	VSS	G
H	VSS	CA9	CA8	NB	DQ28	DQ24	DM3	DQ15	VDDQ	VSS	H
J	VDDCA	CA6	CA7	NB	VSS	DQ11	DQ13	DQ14	DQ12	VDDQ	J
K	VDD2	CA5	VREFCA	NB	$\overline{DQS1}$	DQS1	DQ10	DQ9	DQ8	VSS	K
L	VDDCA	VSS	$\overline{CK}$	NB	DM1	VDDQ	NB	NB	NB	NB	L
M	VSS	NC	CK	NB	VSS	VDDQ	VDD2	VSS	VREFDQ	NB	M
N	CKE	NC	NC	NB	DM0	VDDQ	NB	NB	NB	NB	N
P	$\overline{CS}$	NC	NC	NB	$\overline{DQS0}$	DQS0	DQ5	DQ6	DQ7	VSS	P
R	CA4	CA3	CA2	NB	VSS	DQ4	DQ2	DQ1	DQ3	VDDQ	R
T	VSS	VDDCA	CA1	NB	DQ19	DQ23	DM2	DQ0	VDDQ	VSS	T
U	VSS	VDD2	CA0	NB	VDDQ	DQ17	DQ20	DQS2	$\overline{DQS2}$	VSS	U
V	VDD1	VSS	NC	NB	VSS	VSS	VDDQ	DQ22	VSS	VDDQ	V
W	DNU	NC	NC	NB	VDD2	VDD1	DQ16	DQ18	DQ21	DNU	W
Y	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU	Y
	1	2	3	4	5	6	7	8	9	10	

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Ball Assignment – (162b Flash X 8 + DRAM X 16)

Part Number: NM1282NSLAXAL-XXX

Top View, A1 in Top Left Corner



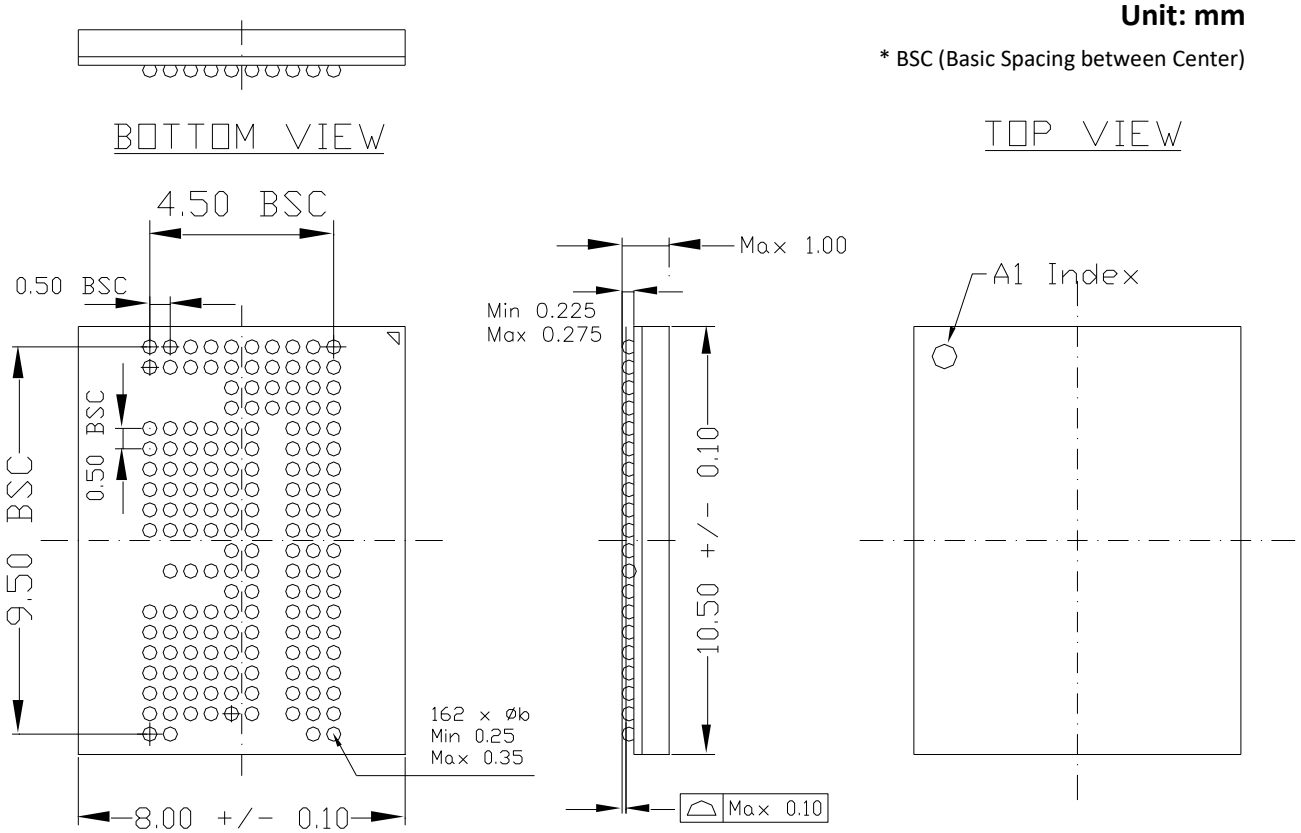
	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU	$\overline{WP}$	CLE	VCC	I/O 4	I/O 7	VCC	DNU	DNU	A
B	DNU	VCC	NC	ALE	$\overline{RE}$	I/O 5	NC	NC	VSS	DNU	B
C	NC	I/O 1	I/O 3	$\overline{WE}$	R/$\overline{B}$	I/O 6	NB	NB	NB	NB	C
D	NC	I/O 0	I/O 2	$\overline{CE}$	NC	NC	NB	NB	NB	NB	D
E	VSS	NC	NC	NB	VDD2	VDD1	NC	NC	NC	DNU	E
F	VDD1	VSS	NC	NB	VSS	VSS	VDDQ	NC	VSS	VDDQ	F
G	VSS	VDD2	ZQ	NB	VDDQ	NC	NC	NC	NC	VSS	G
H	VSS	CA9	CA8	NB	NC	NC	NC	DQ15	VDDQ	VSS	H
J	VDDCA	CA6	CA7	NB	VSS	DQ11	DQ13	DQ14	DQ12	VDDQ	J
K	VDD2	CA5	VREFCA	NB	$\overline{DQS1}$	DQS1	DQ10	DQ9	DQ8	VSS	K
L	VDDCA	VSS	$\overline{CK}$	NB	DM1	VDDQ	NB	NB	NB	NB	L
M	VSS	NC	CK	NB	VSS	VDDQ	VDD2	VSS	VREFDQ	NB	M
N	CKE	NC	NC	NB	DM0	VDDQ	NB	NB	NB	NB	N
P	$\overline{CS}$	NC	NC	NB	$\overline{DQS0}$	DQS0	DQ5	DQ6	DQ7	VSS	P
R	CA4	CA3	CA2	NB	VSS	DQ4	DQ2	DQ1	DQ3	VDDQ	R
T	VSS	VDDCA	CA1	NB	NC	NC	NC	DQ0	VDDQ	VSS	T
U	VSS	VDD2	CA0	NB	VDDQ	NC	NC	NC	NC	VSS	U
V	VDD1	VSS	NC	NB	VSS	VSS	VDDQ	NC	VSS	VDDQ	V
W	DNU	NC	NC	NB	VDD2	VDD1	NC	NC	NC	DNU	W
Y	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU	Y
	1	2	3	4	5	6	7	8	9	10	

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Package Outline Drawing (8.00mm x 10.50mm x 1.00mm)

Unit: mm

* BSC (Basic Spacing between Center)



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Ball Description - 4Gb X8 SLC NAND

Symbol	Type	Function
X8: **I/O[7:0]**	Input/output	**Data Bus:** The I/O0 to 7 pins are used as a port for transferring address, command and input/output data to and from the device. The I/O8 to 15 pins are used as a port for transferring input/ouput data to and from the device. I/O8 to 15 pins must be low level(VIL) when address and command are input.
CLE	Input	**Command Latch Enable:** The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.
ALE	Input	**Address Latch Enable:** The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O ports on the rising edge of $\overline{WE}$ while ALE is High.
$\overline{CE}$	Input	**Chip Enable:** The device goes into a low-power Standby mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state (RY / $\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.
$\overline{RE}$	Input	**Read Enable:** The $\overline{RE}$ signal controls serial data output. Data is available tREA after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address = Address +1) on this falling edge.
$\overline{WE}$	Input	**Write Enable:** The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.
$\overline{WP}$	Input	**Write Protect:** The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used protecting the data during the power-on/off sequence when input signals are invalid.
RY/$\overline{BY}$	Output	**Ready / Busy Output:** The RY / $\overline{BY}$ output signal is used to indicate the operation condition of the device. The RY / $\overline{BY}$ signal is in Busy state (RY / $\overline{BY}$ =L) during the Program, Erase and Read operations and will return to Ready state (RY / $\overline{BY}$ =H) afeter completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to Vccq with an appropriate resister. If RY / $\overline{BY}$ signal is not pulled-up to Vccq (“Open” state), device operation cannot guarantee.
VCC	Supply	**Power**
VSS	Supply	**Ground**
NC	—	**No Connect:** These pins should be left unconnected.

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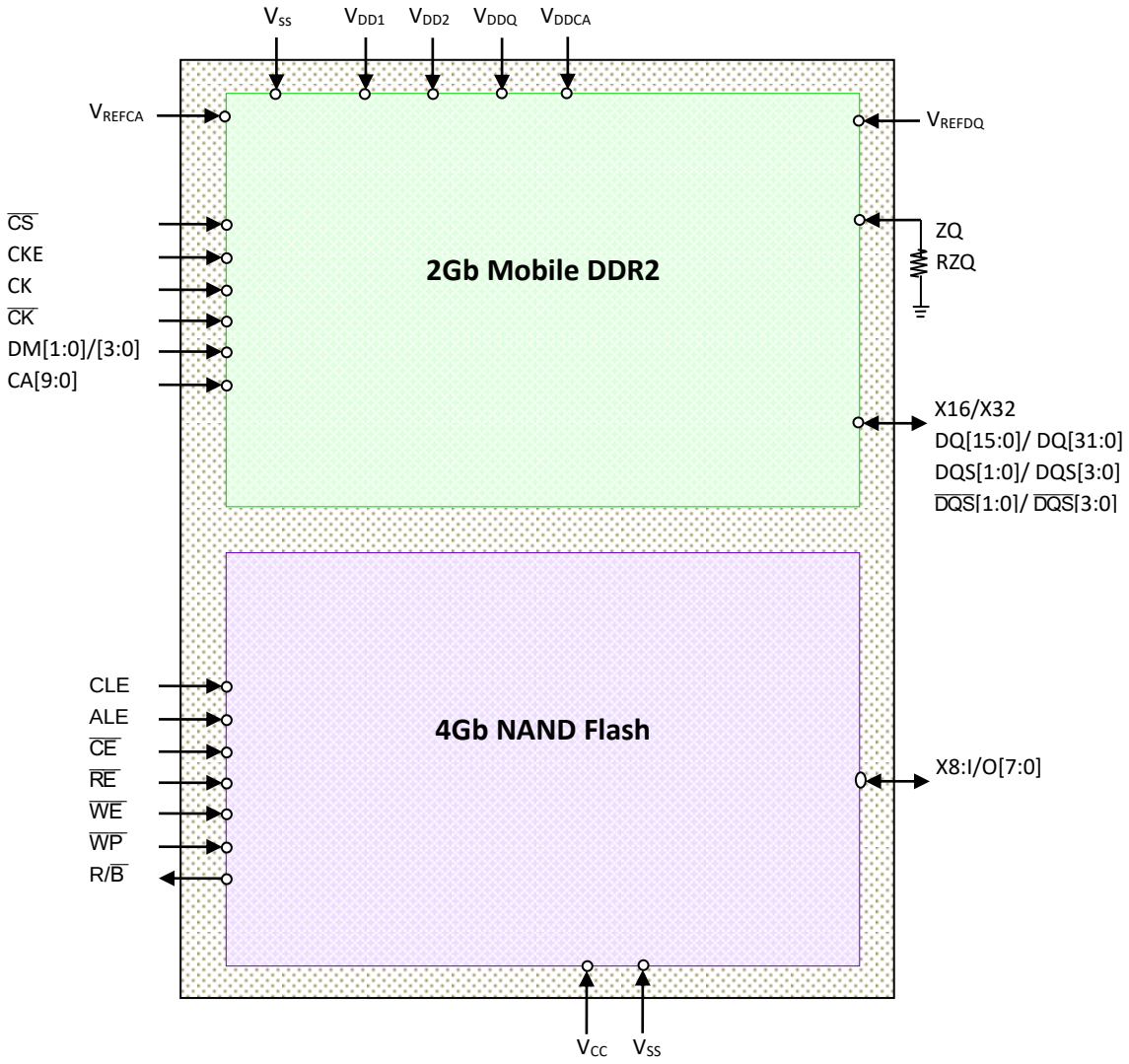
Ball Description - 2Gb X16/X32 LPDDR2

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, $\overline{CS}$ and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK and $\overline{CK}$. The positive Clock edge is defined by the crosspoint of a rising CK and a falling $\overline{CK}$. The negative Clock edge is defined by the crosspoint of a falling CK and a rising $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates internal clock signals, and device input buffers and output drivers. Power saving modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
$\overline{CS}$	Input	**Chip Select:** $\overline{CS}$ is considered part of the command code. $\overline{CS}$ is sampled at the positive Clock edge.
CA0 – CA9	Input	**Command/Address Inputs:** Uni-directional command/address bus inputs. Provide the command and address inputs according to the command truth table. CA is considered part of the command code.
For X16: DM0 – DM1 **For X32:** DM0 – DM3	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matched the DQ and DQS (or $\overline{DQS}$). DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
For X16: DQ0-DQ15 **For X32:** DQ0-DQ31	Input/output	**Data Bus:** Bi-directional Input / Output data bus.
For X16: DQS0-1, $\overline{DQS0\text{-}1}$ **For X32:** DQS0-3, $\overline{DQS0\text{-}3}$	Input/output	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and Differential (DQS and $\overline{DQS}$). It is output with read data and input with write data. DQS is edge-aligned to read data, and centered with write data. DQS0 & $\overline{DQS0}$ corresponds to the data on DQ0-DQ7, DQS1 & $\overline{DQS1}$ corresponds to the data on DQ8-DQ15, DQS2 & $\overline{DQS2}$ corresponds to the data on DQ16-DQ23, DQS3 & $\overline{DQS3}$ corresponds to the data on DQ24-DQ31.
NC	—	**No Connect:** No internal electrical connection is present.
ZQ	Input	**Reference Pin for Output Drive Strength Calibration.** External impedance (240-ohm): this signal is used to calibrate the device output impedance.
V_{DD1}	Supply	**Core Power Supply 1:** Core power supply
V_{DD2}	Supply	**Core Power Supply 2:** Core power supply
V_{DDQ}	Supply	**DQ Power Supply:** Isolated on the die for improved noise immunity.
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, $\overline{CS}$, CK, and $\overline{CK}$ input buffers.
V_{REFDQ}, V_{REFCA}	Supply	**Reference Voltage:** V_{REFDQ} is reference for DQ input buffers. V_{REFCA} is reference for Command / Address input buffers.
V_{SS}	Supply	**Ground**

NOTE 1: The signal may show up in a different symbol but it indicates to the same thing. e.g., /CK = CK# = $\overline{CK}$ = CKb, /DQS = DQS# = $\overline{DQS}$ = DQSb, /CS = CS# = $\overline{CS}$ = CSb.

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Functional Block Diagram



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4Gb(X8) SLC NAND Flash

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Descriptions

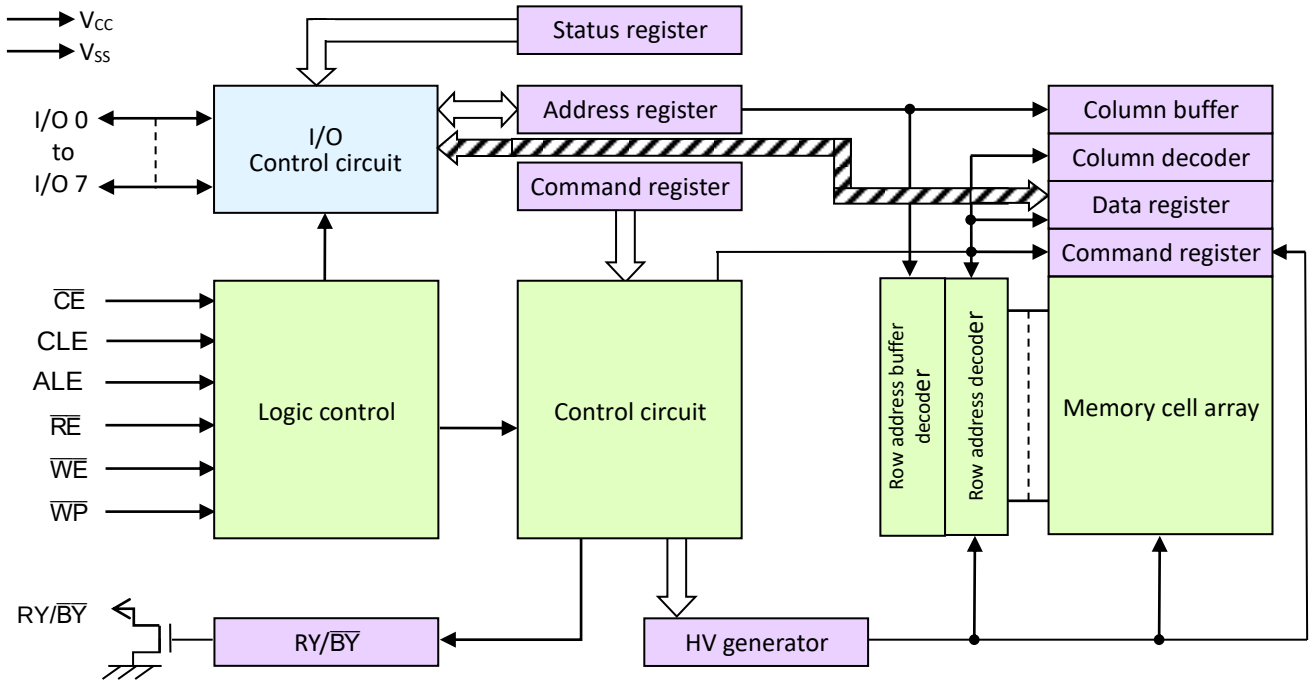
The device is a single 1.8V 4Gbit (4,563,402,752 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^2PROM) organized as X8: (4096 +256) bytes x 64 pages x 2048 blocks.

The device has two 4352-bytes static registers which allow program and read data to be transferred between the register ad the memory cell array in 4352-bytes or 2176-words increments. The Erase operation is implemented in a single block unit (X8=256 Kbytes + 16 Kbytes: 4352 bytes x 64 pages).

The device is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

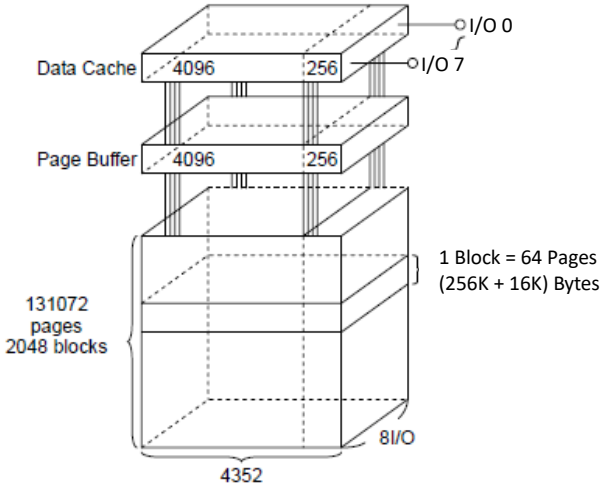
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Function Block Diagram (X8)



Schematic Cell Layout and Address Assignment (X8)

The Program operation works on page units while the Erase operation works on block units



A page consists of 4352 bytes in which 4096 bytes are used for main memory storage and 256 bytes are for redundancy or for other uses.
1 Page = 4352 Bytes
1 Block = 4352 Bytes x 64 Pages = (256K + 16K) Bytes
Capacity = 4352 Bytes x 64 Pages x 2048 Blocks

Array Address (X8)

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	Address
1st cycle	CA_0	CA_1	CA_2	CA_3	CA_4	CA_5	CA_6	CA_7	Column Address
2nd cycle	CA_8	CA_9	CA_{10}	CA_{11}	CA_{12}	L	L	L	Column Address
3rd cycle	PA_0	PA_1	PA_2	PA_3	PA_4	PA_5	PA_6	PA_7	Page Address
4th cycle	PA_8	PA_9	PA_{10}	PA_{11}	PA_{12}	PA_{13}	PA_{14}	PA_{15}	Page Address
5th cycle	PA_{16}	L	L	L	L	L	L	L	Page Address

PA6 to PA16: Block address
PA0 to PA5: NAND address in block

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Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	-0.6 to +2.5	V
V_{IN}	Input Voltage	-0.6 to +2.5	
$V_{I/O}$	Input / Output Voltage	-0.6 to Vcc + 0.3 (≤2.5V)	
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	-55 to +125	°C

Capacitance[1]

(T_A=25℃, f=1.0MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input	V_{IN}=0V	—	10	pF
C_{OUT}	Output	V_{OUT}=0V	—	10	pF

NOTE 1 This parameter is periodically sampled and is not tested for every device.

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Valid Blocks

Symbol	Parameter	Min	Typ.	Max	Unit
N_{VB}	Number of Valid Blocks	2,008	–	2,048	Blocks

NOTE 1 The device occasionally contains unusable blocks.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over lifetime.
The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

NOTE 2 Additional invalid blocks may develop within life time in the device; however, the total valid blocks will not drop below minimum valid blocks during the endurance life.

Recommended DC Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
V_{CC}	Power Supply Voltage	1.70	–	1.95	V
V_{IH}	High Level Input Voltage	V_{CC} x 0.8	–	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	-0.3[1]	–	V_{CC} x 0.2	V

Note 1 -2V (pulse width lower than 20 ns)

DC and Operation Characteristics

(Ta= -25 to 85℃, V_{CC}=1.70 to 1.95V)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_{IL}	Input Leakage Current	V_{IN}=0 to V_{CC}	–	–	±10	µA
I_{LO}	Output Leakage Current	V_{OUT}=0 to V_{CC}	–	–	±10	µA
I_{CCO1}	Serial Read Current	$\overline{CE}$=V_{IL}, I_{OUT}= 0 mA, tcycle=25ns	–	–	30	mA
I_{CCO2}	Programming Current	–	–	–	30	mA
I_{CCO3}	Erasing Current	–	–	–	30	mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} - 0.2 V, $\overline{WP}$ = 0 V/V_{CC}	–	–	50	µA
V_{OH}	High Level Output Voltage	I_{OH} = -0.1mA	V_{CC} - 0.2	–	–	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1mA	–	–	0.2	V
I_{OL} (RY/$\overline{BY}$)	Output Current of (RY/$\overline{BY}$) pin	V_{OL}=0.2V	–	4	–	mA

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AC Characteristics and Recommended Operating Conditions

(Ta= -25 to 85℃, V_{CC}=1.70 to 1.95V)

Symbol	Parameter	Min	Max	Unit
tCLS	CLE Setup Time	12	–	ns
tCLH	CLE Hold Time	5	–	ns
tCS	$\overline{CE}$ Setup Time	20	–	ns
tCH	$\overline{CE}$ Hold Time	5	–	ns
tWP	Write Pulse Width	12	–	ns
tALS	ALE Setup Time	12	–	ns
tALH	ALE Hold Time	5	–	ns
tDS	Data Setup Time	12	–	ns
tDH	Data Hold Time	5	–	ns
tWC	Write Cycle Time	25	–	ns
tWH	$\overline{WE}$ High Hold Time	10	–	ns

AC Characteristics for Operation

Symbol	Parameter	Min	Max	Unit
tWW	$\overline{WP}$ High to $\overline{WE}$ Low	100	–	ns
tRR	Ready to $\overline{RE}$ Falling Edge	20	–	ns
tRW	Ready to $\overline{WE}$ Falling Edge	20	–	ns
tRP	Read Pulse Width	12	–	ns
tRC	Read Cycle Time	25	–	ns
tREA	$\overline{RE}$ Access Time	–	20	ns
tCEA	$\overline{CE}$ Access Time	–	25	ns
tCLR	CLE Low to $\overline{RE}$ Low	10	–	ns
tAR	ALE Low to $\overline{RE}$ Low	10	–	ns
tRHOH	$\overline{RE}$ High to Output Hold Time	25	–	ns
tRLOH	$\overline{RE}$ Low to Output Hold Time	5	–	ns
tRHZ	$\overline{RE}$ High to Output High Impedance	–	60	ns
tCHZ	$\overline{CE}$ High to Output High Impedance	–	20	ns
tCSD	$\overline{CE}$ High to ALE or CLE Don't care	0	–	ns
tREH	$\overline{RE}$ High Hold Time	10	–	ns
tIR	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	–	ns
tRHW	$\overline{RE}$ High to $\overline{WE}$ Low	30	–	ns
tWHC	$\overline{WE}$ High to $\overline{CE}$ Low	30	–	ns
tWHR	$\overline{WE}$ High to $\overline{RE}$ Low	60	–	ns
tR	Memory Cell Array to Starting Address	–	25	µs
tDCBSYR1	Data Cache Busy in Read Cache (following 31h and 3Fh)	–	25	µs
tDCBSYR2	Data Cache Busy in Page Copy (following 3Ah)	–	30	µs
tWB	$\overline{WE}$ High to Busy	–	100	ns
tRST	Device Reset Time (Ready/Read/Program/Erase)	–	5/5/10/500	µs

NOTE 1 tCLS and tALS cannot be shorter than tWP.

NOTE 2 tCS should be longer than tWP + 8ns.

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AC Test Condition

Parameter	Condition
	VCC : 1.70 to 1.95V
Input level	VCC – 0.2 V, 0.2 V
Input pulse rise and fall time	3ns
Input comparison level	Vcc / 2
Output data comparison level	Vcc / 2
Output Load	1 TTL GATE and CL=30pF

NOTE 1 Busy to ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.

Programming / Erasing Characteristics

(Ta= -25 to 85℃, V_{CC}=1.70 to 1.95V)

Symbol	Parameter	Min	Typ.	Max	Unit
tPROG	Average Programming Time	–	300	700	µs
tDCBSYW1	Data Cache Busy Time in Write Cache (following 11h)	–	–	10	µs
tDCBSYW2[1]	Data Cache Busy Time in Write Cache (following 15h)	–	–	700	µs
N	Number of Partial Program Cycles in the Same Page	–	–	4	cycle
tBERASE	Block Erase Time	–	3.5	10	ms

NOTE 1 $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

Data Output

When tREH is long, output buffers are disabled by $\overline{RE}$=High, and the hold time of data output depend on tRHOH (25ns MIN). On this condition, waveforms look like normal serial read mode.

When tREH is short, output buffers are not disabled by $\overline{RE}$ =High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE, ALE, $\overline{CE}$ or falling edge of $\overline{WE}$, and waveforms look like Extended Data Output Mode.

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Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by operations shown in command table. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Mode Selection Table.

Logic Table

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode
H	L	L		H	*	Command Input
L	L	L		H	H	Data Input
L	H	L		H	*	Address Input
L	L	L	H		*	Serial Data Output
*	*	*	*	*	H	During Program (Busy)
*	*	*	*	*	H	During Erase (Busy)
*	*	H	*	*	*	During Read (Busy)
*	*	L	H[1]	H[1]	*	
*	*	*	*	*	L	Program, Erase Inhibit
*	*	H	*	*	0V/V_{CC}	Stand-by

H: V_{IH}, L=V_{IL} *: V_{IH} or V_{IL}.

Note 1: If $\overline{CE}$ is low during read busy. $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to device or read to device. Reset or Status Read command can be input during Read Busy.

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Command Table

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Serial Data Input	80_H	–	
Read	00_H	30_H	
Column Address Change in Serial Data Output	05_H	$E0_H$	
Read with Data Cache	31_H	–	
Read Start for Last Page in Read Cycle with Data Cache	$3F_H$	–	
Auto Page Program	80_H	10_H	
Column Address Change in Serial Data Input	85_H	–	
Auto Program with Data Cache	80_H	15_H	
Multi Page Program	80_H	11_H	
	81_H	15_H	
	81_H	10_H	
Read for Page Copy (2) with Data Out	00_H	$3A_H$	
Auto Program with Data Cache during Page Copy (2)	$8C_H$	15_H	
Auto Program for last page during Page Copy (2)	$8C_H$	10_H	
Auto Block Erase	60_H	$D0_H$	
ID Read	90_H	–	
Status Read	70_H	–	O
Status Read for Multi-Page Program or Multi Block Erase	71_H	–	O
Reset	FF_H	–	O

Read mode operation states

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O0 to I/O15	Power
Output Select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

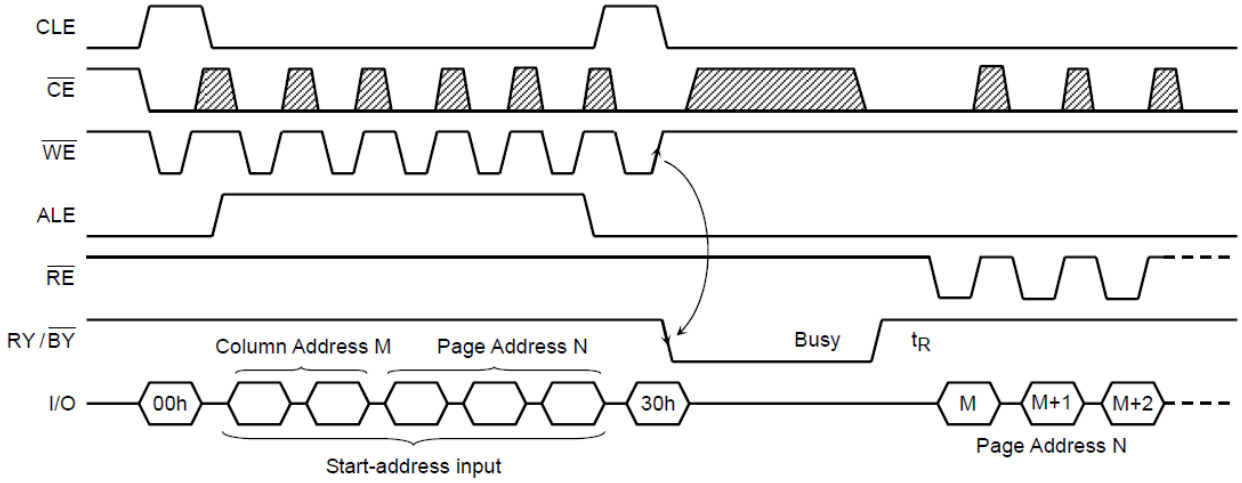
H: V_{IH}, L=V_{IL}

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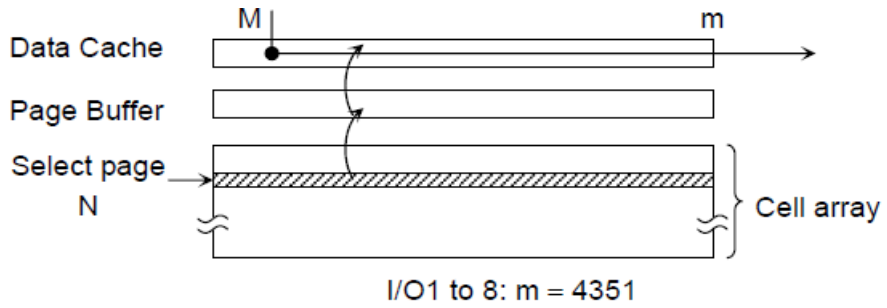
DEVICE OPERATION

Read Mode

Read mode is set when the "00h" and “30h” commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. After initial power on sequence, “00h” command is latched into the internal command register. Therefore read operation after power on sequence is executed by the setting of only five address cycles and “30h” command. Refer to the figures below for the sequence and the block diagram (Refer to the detailed timing chart.).



For X8 :

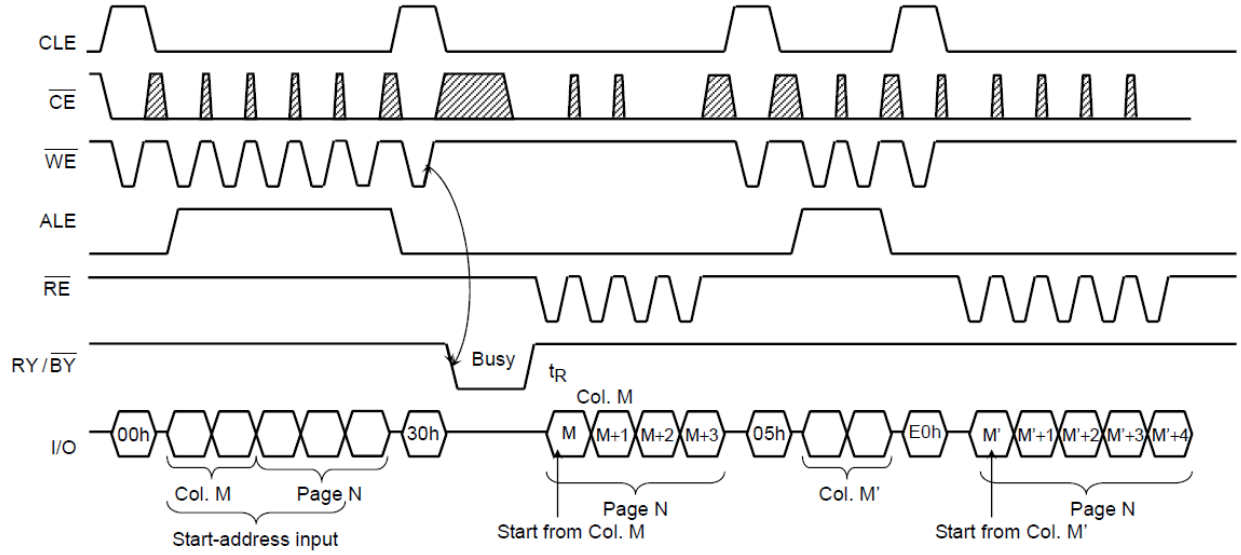


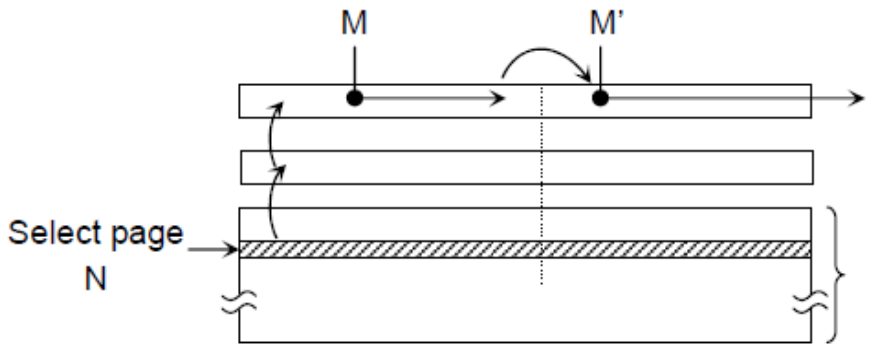
A data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

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Random Column Address Change in Read Cycle





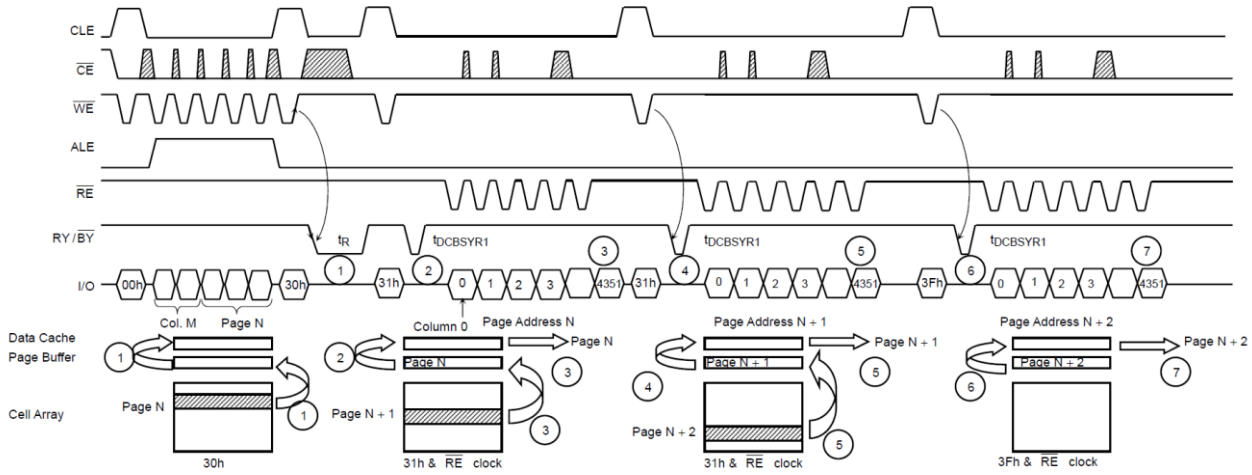
During the serial data output from the Data Cache, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.

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Read Operation with Read Cahe

The device has a Read operation with Data Cache that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning.

For X8 :



If the 31h command is issued to the device, the data content of the next page is transferred to the Page Buffer during serial data out from the Data Cache, and therefore the tR (Data transfer from memory cell to data register) will be reduced.

1 Normal read. Data is transferred from Page N to Data Cache through Page Buffer. During this time period, the device outputs Busy state for tR max.
2 After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to Data Cache from Page Buffer again. This data transfer takes tDCBSYR1 max and the completion of this time period can be detected by Ready/Busy signal.
3 Data of Page N + 1 is transferred to Page Buffer from cell while the data of Page N in Data cache can be read out by $\overline{RE}$ clock simultaneously.
4 The 31h command makes data of Page N + 1 transfer to Data Cache from Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.
This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.
5 Data of Page N + 2 is transferred to Page Buffer from cell while the data of Page N + 1 in Data cache can be read out by $\overline{RE}$ clock simultaneously.
6 The 3Fh command makes the data of Page N + 2 transfer to the Data Cache from the Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.
7 Data of Page N + 2 in Data Cache can be read out, but since the 3Fh command does not transfer the data from the memory cell to Page Buffer, the device can accept new command input immediately after the completion of serial data out.

Multi Page Read Operation

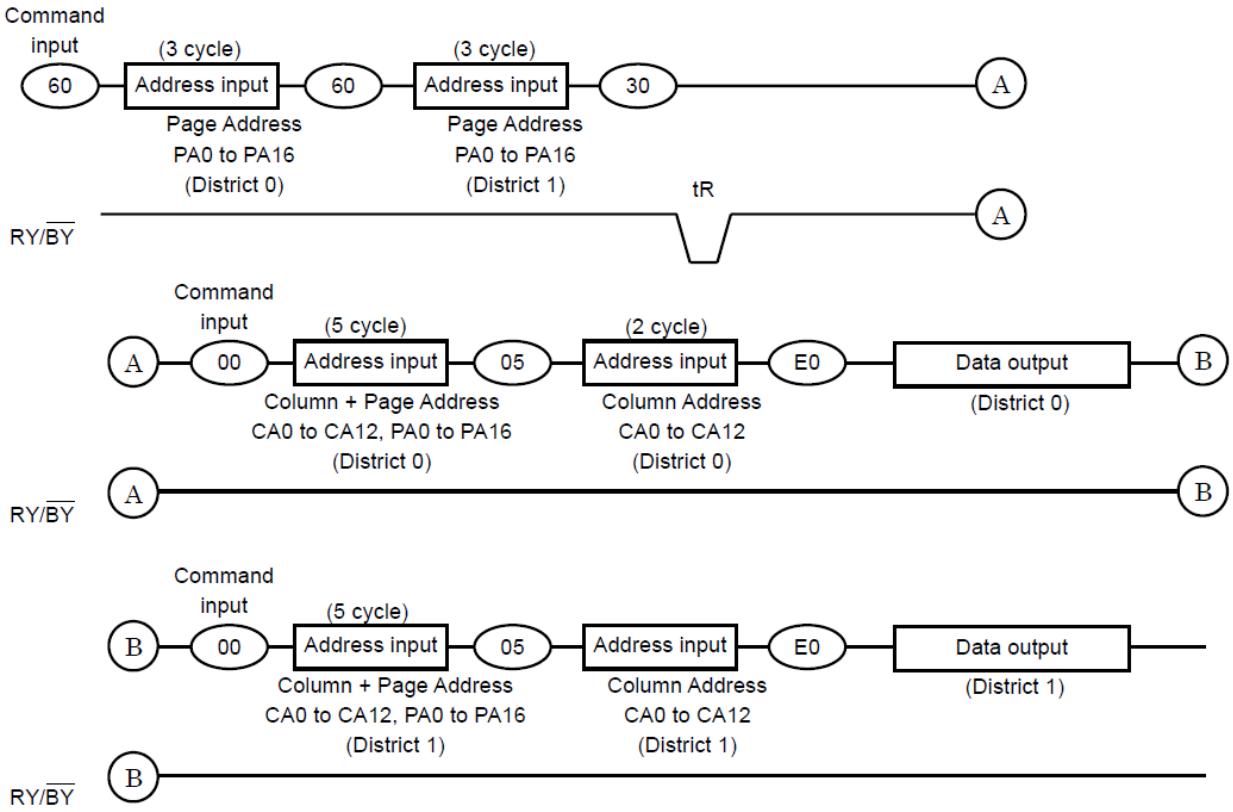
The device has a Multi Page Read operation and Multi Page Read with Data Cache operation.

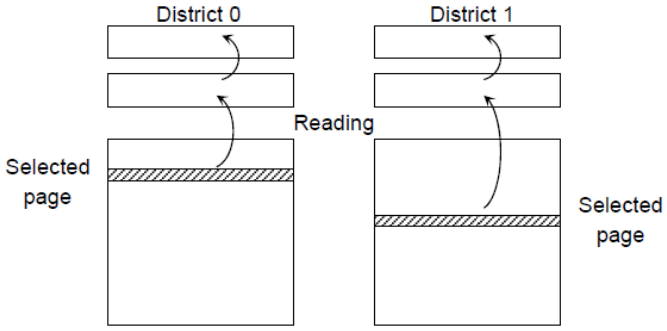
(1) Multi Page Read without Data Cache

The sequence of command and address input is shown below.
Same page address (PA0 to PA5) within each district has to be selected.

For X8 :

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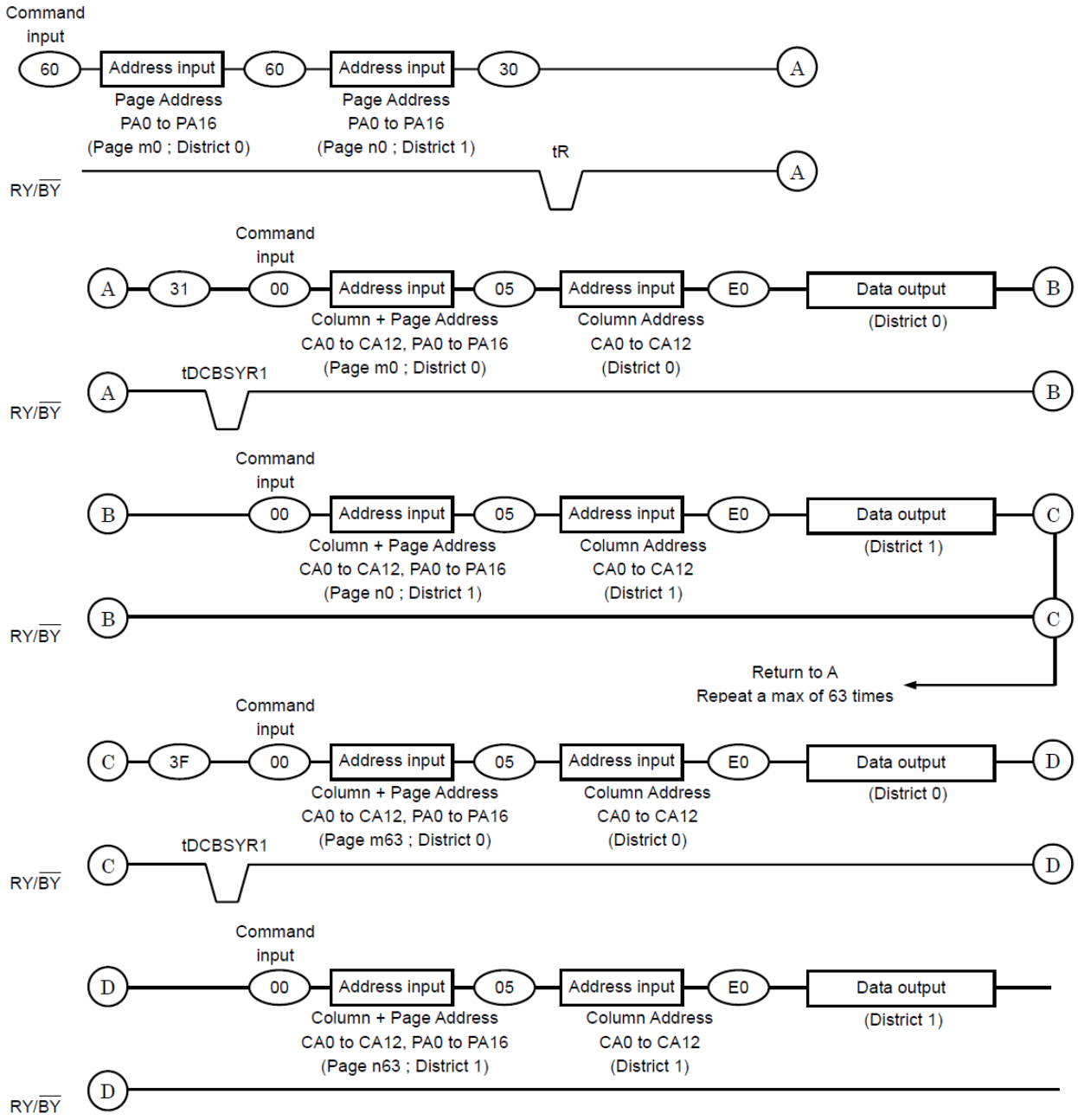
The data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the 2 Districts address information has been latched). The device will be in the Busy state during this transfer period.
After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

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(2) Multi Page Read with Data Cache

When the block address changes (increments) this sequenced has to be started from the beginning.
The sequence of command and address input is shown below.
Same page address (PA0 to PA5) within each district has to be selected.

For X8 :



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(3) Notes

(a) Internal addressing in relation with the Districts

To use Multi Page Read operation, the internal addressing should be considered in relation with the District.

• The device consists from 2 Districts.

• Each District consists from 1024 erase blocks.

• The allocation rule is follows.

District 0: Block 0, Block 2, Block 4, Block 6,⋯, Block 2046

District 1: Block 1, Block 3, Block 5, Block 7,⋯, Block 2047

(b) Address input restriction for the Multi Page Read operation

There are following restrictions in using Multi Page Read;

(Restriction)

Maximum one block should be selected from each District.

Same page address (PA0 to PA5) within two districts has to be selected.

For example;

(60) [District 0, Page Address 0x00000] (60) [District 1, Page Address 0x00040] (30)

(60) [District 0, Page Address 0x00001] (60) [District 1, Page Address 0x00041] (30)

(Acceptance)

There is no order limitation of the District for the address input.

For example, following operation is accepted;

(60) [District 0] (60) [District 1] (30)

(60) [District 1] (60) [District 0] (30)

It requires no mutual address relation between the selected blocks from each District.

(c) $\overline{WP}$ signal

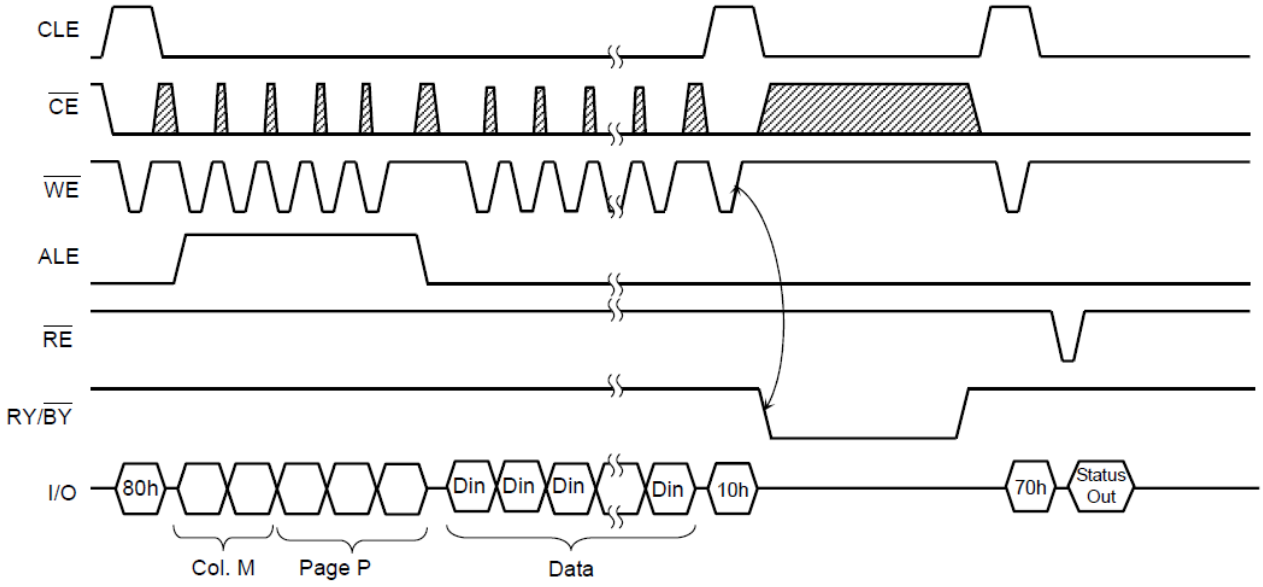
Make sure $\overline{WP}$ is held to High level when Multi Page Read operation is performed

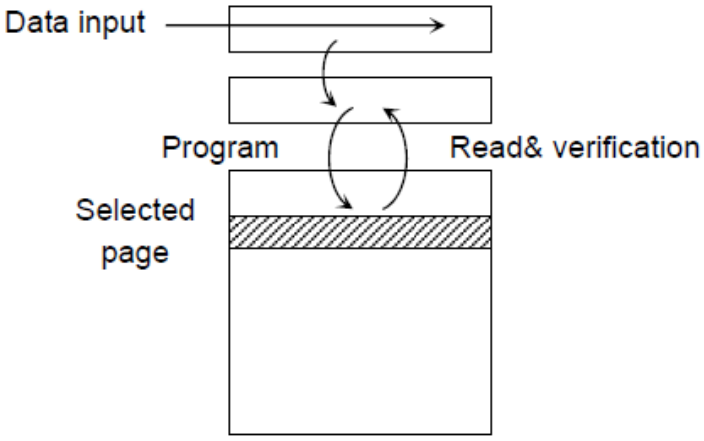
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Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below.

(Refer to the detailed timing chart.)





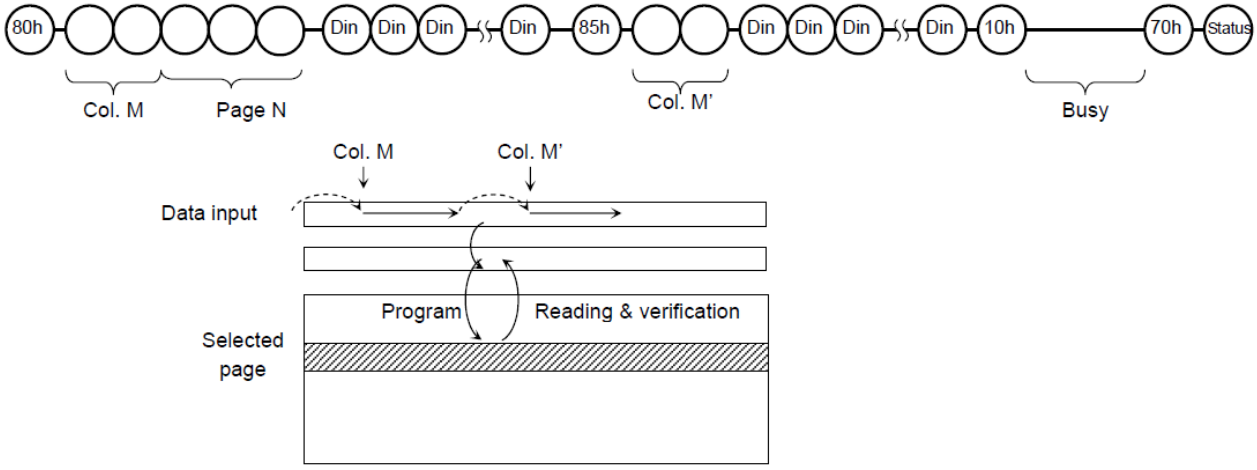
The data is transferred (programmed) from the Data Cache via the Page Buffer to the selected page on the rising edge of $\overline{WE}$ following input of the “10h” command. After programming, the programmed data is transferred back to the Page Buffer to be automatically verified by the device.
If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

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Random Column Address Change in Auto Page Program Operation

The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.

Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.



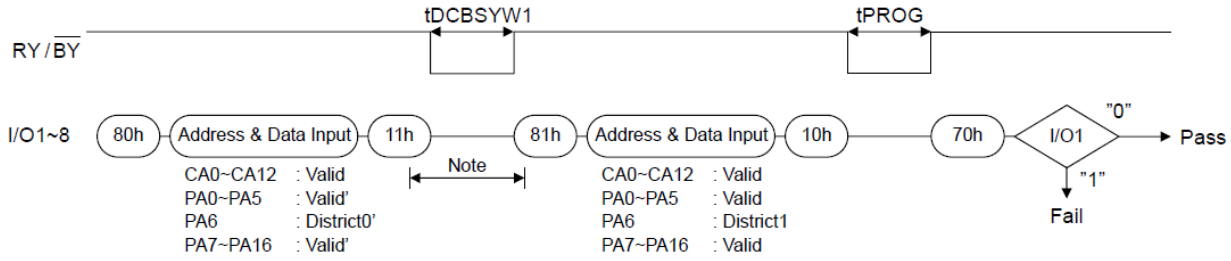
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Multi Page Program

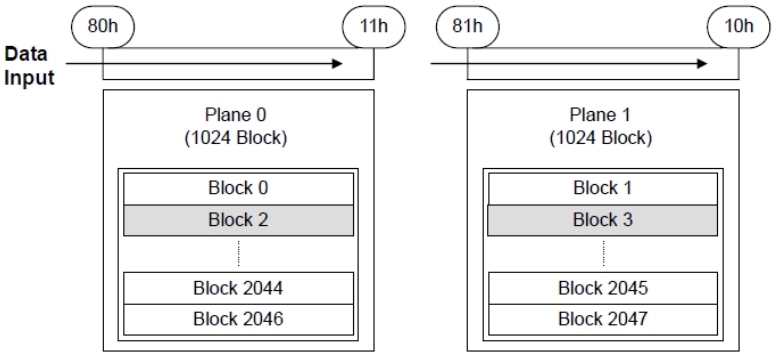
The device has a Multi Page Program, which enables even higher speed program operation compared to Auto Page Program. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

Although two planes are programmed simultaneously, pass/fail is not available for each page by "70h" command when the program operation completes. Status bit of I/O 1 is set to “1” when any of the pages fails. Limitation in addressing with Multi Page Program is shown below.

For X8 :



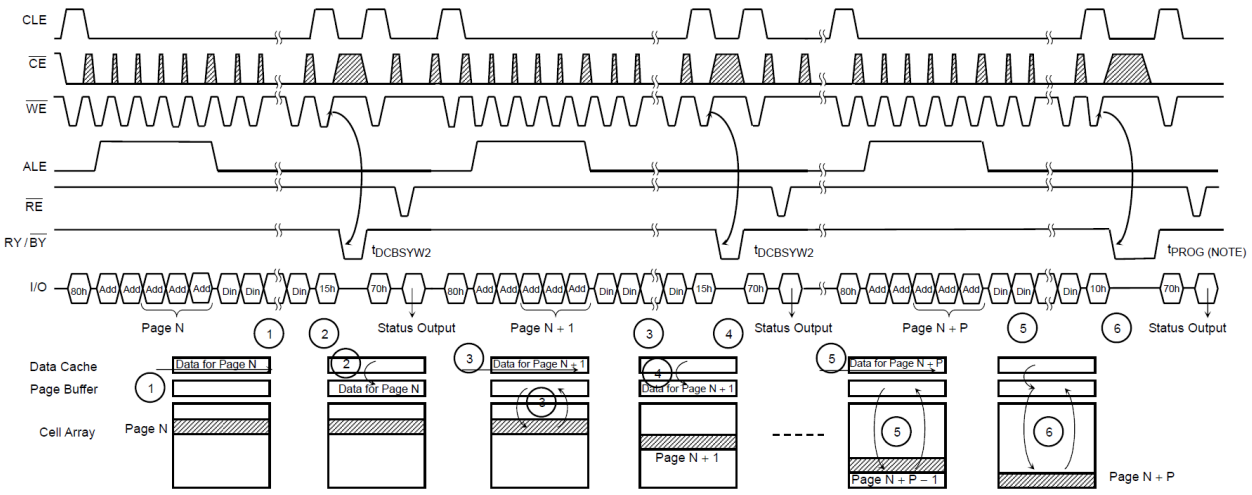
NOTE: Any command between 11h and 81h is prohibited except 70h and FFh.



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Auto Page Program Operation with Data Cache

The device has an Auto Page Program with Data Cache operation enabling the high speed program operation shown below. When the block address changes this sequenced has to be started from the beginning.



Issuing the 15h command to the device after serial data input initiates the program operation with Data Cache

1 Data for Page N is input to Data Cache.

2 Data is transferred to the Page Buffer by the 15h command. During the transfer the Ready/Busy outputs Busy State ($t_{DCBSYW2}$).

3 Data is programmed to the selected page while the data for page N + 1 is input to the Data Cache.

4 By the 15h command, the data in the Data Cache is transferred to the Page Buffer after the programming of page N is completed. The device output busy state from the 15h command until the Data Cache becomes empty. The duration of this period depends on timing between the internal programming of page N and serial data input for Page N + 1 ($t_{DCBSYW2}$).

5 Data for Page N + P is input to the Data Cache while the data of the Page N + P − 1 is being programmed.

6 The programming with Data Cache is terminated by the 10h command. When the device becomes Ready, it shows that the internal programming of the Page N + P is completed.

NOTE: Since the last page programming by the 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following;

t_{PROG} = t_{PROG} for the last page + t_{PROG} of the previous page − (command input cycle + address input cycle + data input cycle time of the last page)

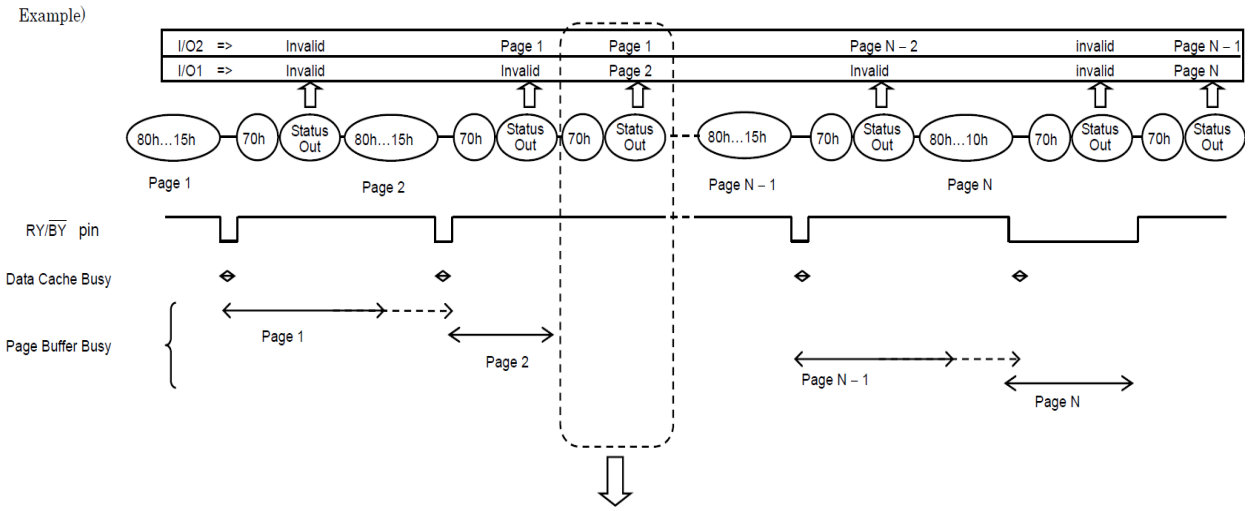
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Pass/fail status for each page programmed by the Auto Page Programming with Data Cache operation can be detected by the Status Read operation.

- I/O1 : Pass/fail of the current page program operation.
- I/O2 : Pass/fail of the previous page program operation.

The Pass/Fail status on I/O1 and I/O2 are valid under the following conditions.

- Status on I/O1: Page Buffer Ready/Busy is Ready State.
  The Page Buffer Ready/Busy is output on I/O6 by Status Read operation or RY / $\overline{BY}$ pin after the 10h command
- Status on I/O2: Data Cache Read/Busy is Ready State.
  The Data Cache Ready/Busy is output on I/O7 by Status Read operation or RY / $\overline{BY}$ pin after the 15h command.



If the Page Buffer Busy returns to Ready before the next 80h command input, and if Status Read is done during this Ready period, the Status Read provides pass/fail for Page 2 on I/O1 and pass/fail result for Page1 on I/O2

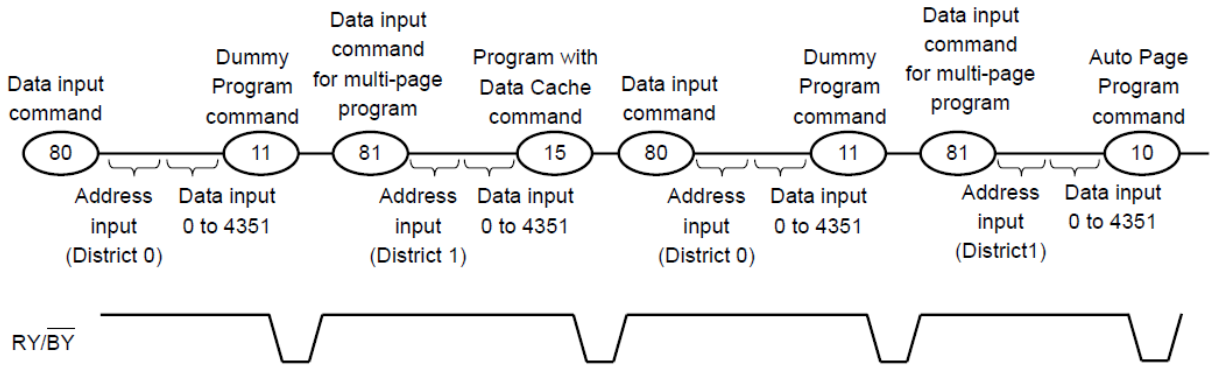
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Multi Page Program with Data Cache

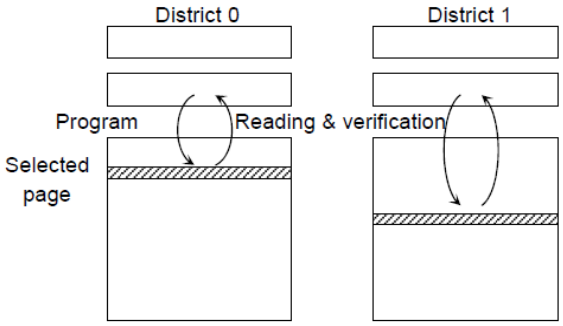
The device has a Multi Page Program with Data Cache operation, which enables even higher speed program operation compared to Auto Page Program with Data Cache as shown below. When the block address changes (increments) this sequenced has to be started from the beginning.

The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

For X8 :



After “15h” or “10h” Program command is input to device, physical programing starts as follows. For details of Auto Program with Data Cache, refer to “Auto Page Program with Data Cache”.

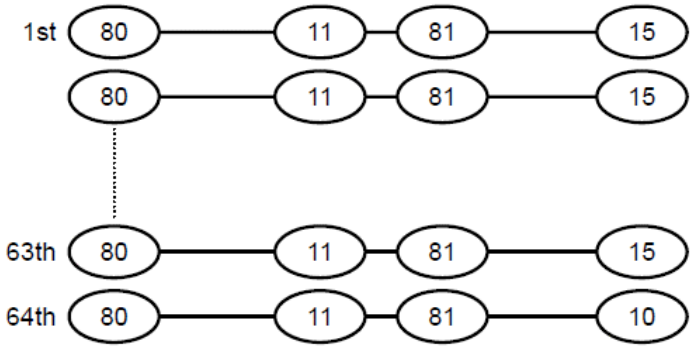


The data is transferred (programmed) from the page buffer to the selected page on the rising edge of $\overline{WE}$ following input of the “15h” or “10h” command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

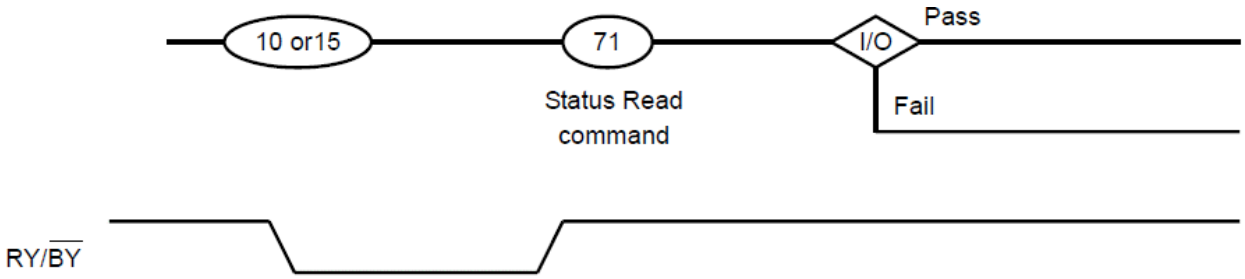
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Starting the above operation from 1st page of the selected erase blocks, and then repeating the operation total 64 times with incrementing the page address in the blocks, and then input the last page data of the blocks, “10h” command executes final programming. Make sure to terminate with 81h-10h- command sequence.

In this full sequence, the command sequence is following.



After the “15h” or “10h” command, the results of the above operation is shown through the “71h”Status Read command.



The 71_H Command Status Description

I/O	Status	Output
I/O 0	Chip Status1 : Pass / Fail	Pass : 0 / Fail : 1
I/O 1	District 0 Chip Status1 : Pass / Fail	Pass : 0 / Fail : 1
I/O 2	District 1 Chip Status2 : Pass / Fail	Pass : 0 / Fail : 1
I/O 3	District 0 Chip Status1 : Pass / Fail	Pass : 0 / Fail : 1
I/O 4	District 1 Chip Status2 : Pass / Fail	Pass : 0 / Fail : 1
I/O 5	Ready / Busy	Busy : 0 / Ready : 1
I/O 6	Data Cache Ready / Busy	Busy : 0 / Ready : 1
I/O 7	Write Protect	Protected : 0 / Not Protected : 1

I/O0 describes Pass/Fail condition of district 0 and 1 (OR data of I/O1 and I/O2). If one of the districts fails during multi page program operation, it shows “Fail”.

I/O1 to I/O4 shows the Pass/Fail condition of each district. For details on “Chip Status 1” and “Chip Status2” refer to section “Status Read”.

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Internal addressing in relation with the Districts

To use Multi Page Program operation, the internal addressing should be considered in relation with the District.

- The device consists from 2 Districts.
- Each District consists from 1024 erase blocks.
- The allocation rule is follows.

District 0: Block 0, Block 2, Block 4, Block 6,⋯, Block 2046

District 1: Block 1, Block 3, Block 5, Block 7,⋯, Block 2047

Address input restriction for the Multi Page Program with Data Cache operation

There are following restrictions in using Multi Page Program with Data Cache;

(Restriction)

Maximum one block should be selected from each District.

Same page address (PA0 to PA5) within two districts has to be selected.

For example;

(80) [District 0, Page Address 0x00000] (11) (81) [District 1, Page Address 0x00040] (15 or 10)

(80) [District 0, Page Address 0x00001] (11) (81) [District 1, Page Address 0x00041] (15 or 10)

(Acceptance)

There is no order limitation of the District for the address input.

For example, following operation is accepted;

(80) [District 0] (11) (81) [District 1] (15 or 10)

(80) [District 1] (11) (81) [District 0] (15 or 10)

It requires no mutual address relation between the selected blocks from each District.

Operating restriction during the Multi Page Program with Data Cache operation

(Restriction)

The operation has to be terminated with “10h” command.

Once the operation is started, no commands other than the commands shown in the timing diagram is allowed to be input except for Status Read command and reset command.

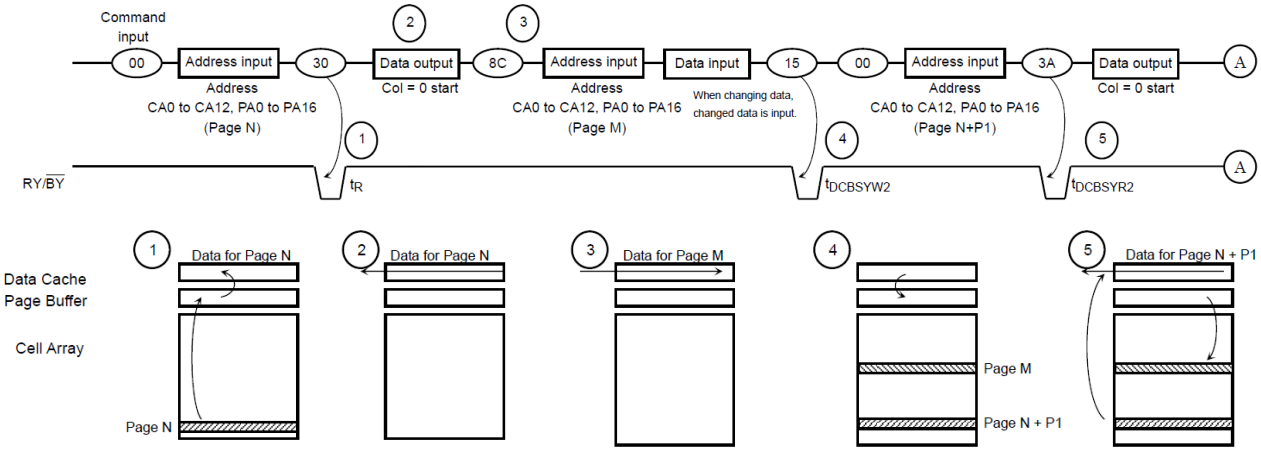
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Page Copy (2)

By using Page Copy (2), data in a page can be copied to another page after the data has been read out.

When the block address changes (increments) this sequenced has to be started from the beginning.

For X8 :



Page Copy (2) operation is as following.

1 Data for Page N is transferred to the Data Cache.

2 Data for Page N is read out.

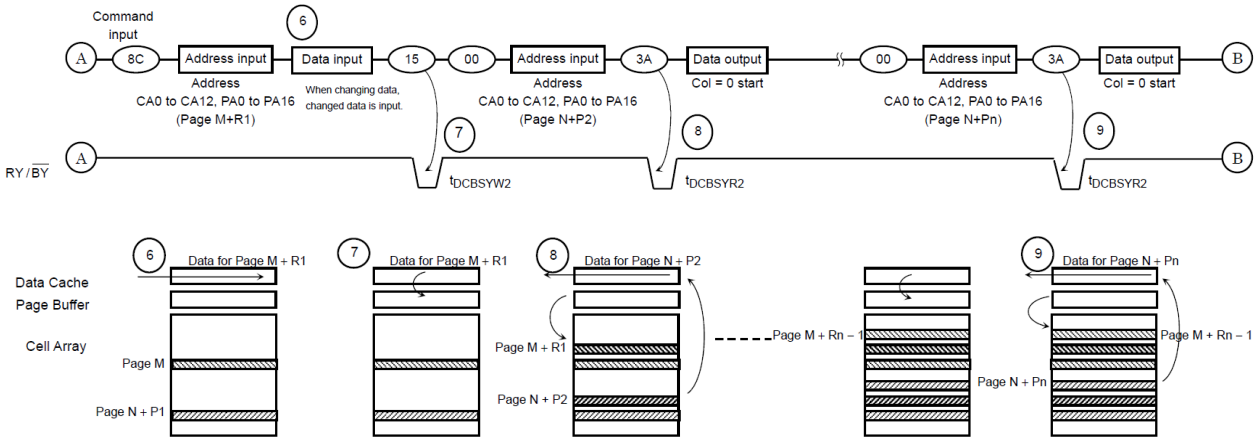
3 Copy Page address M is input and if the data needs to be changed, changed data is input.

4 Data Cache for Page M is transferred to the Page Buffer.

5 After the Ready state, Data for Page N + P1 is output from the Data Cache while the data of Page M is being programmed.

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For X8 :



6 Copy Page address (M + R1) is input and if the data needs to be changed, changed data is input.

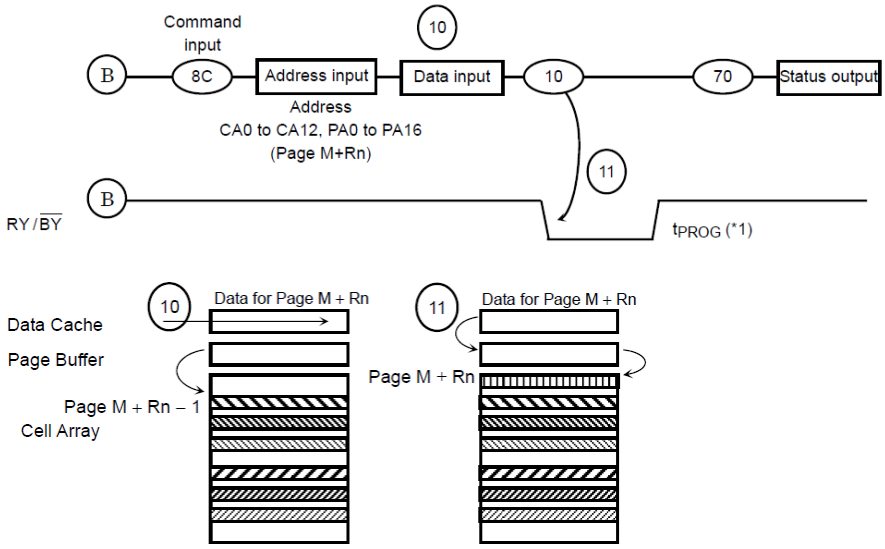
7 After programming of page M is completed, Data Cache for Page M + R1 is transferred to the Page Buffer.

8 By the 15h command, the data in the Page Buffer is programmed to Page M + R1. Data for Page N + P2 is transferred to the Data cache.

9 The data in the Page Buffer is programmed to Page M + Rn − 1. Data for Page N + Pn is transferred to the Data Cache.

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For X8 :



10 Copy Page address (M + Rn) is input and if the data needs to be changed, changed data is input.

11 By issuing the 10h command, the data in the Page Buffer is programmed to Page M + Rn.

(*1) Since the last page programming by the 10h command is initiated after the previous cache program, the tPROG here will be expected as the following,

tPROG = tPROG of the last page + tPROG of the previous page − (command input cycle + address input cycle + data output/input cycle time of the last page)

NOTE) This operation needs to be executed within District-0 or District-1.

Data input is required only if previous data output needs to be altered.

If the data has to be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that needs be changed.

If the data does not have to be changed, data input cycles are not required.

Make sure $\overline{WP}$ is held to High level when Page Copy (2) operation is performed.

Also make sure the Page Copy operation is terminated with 8Ch-10h command sequence

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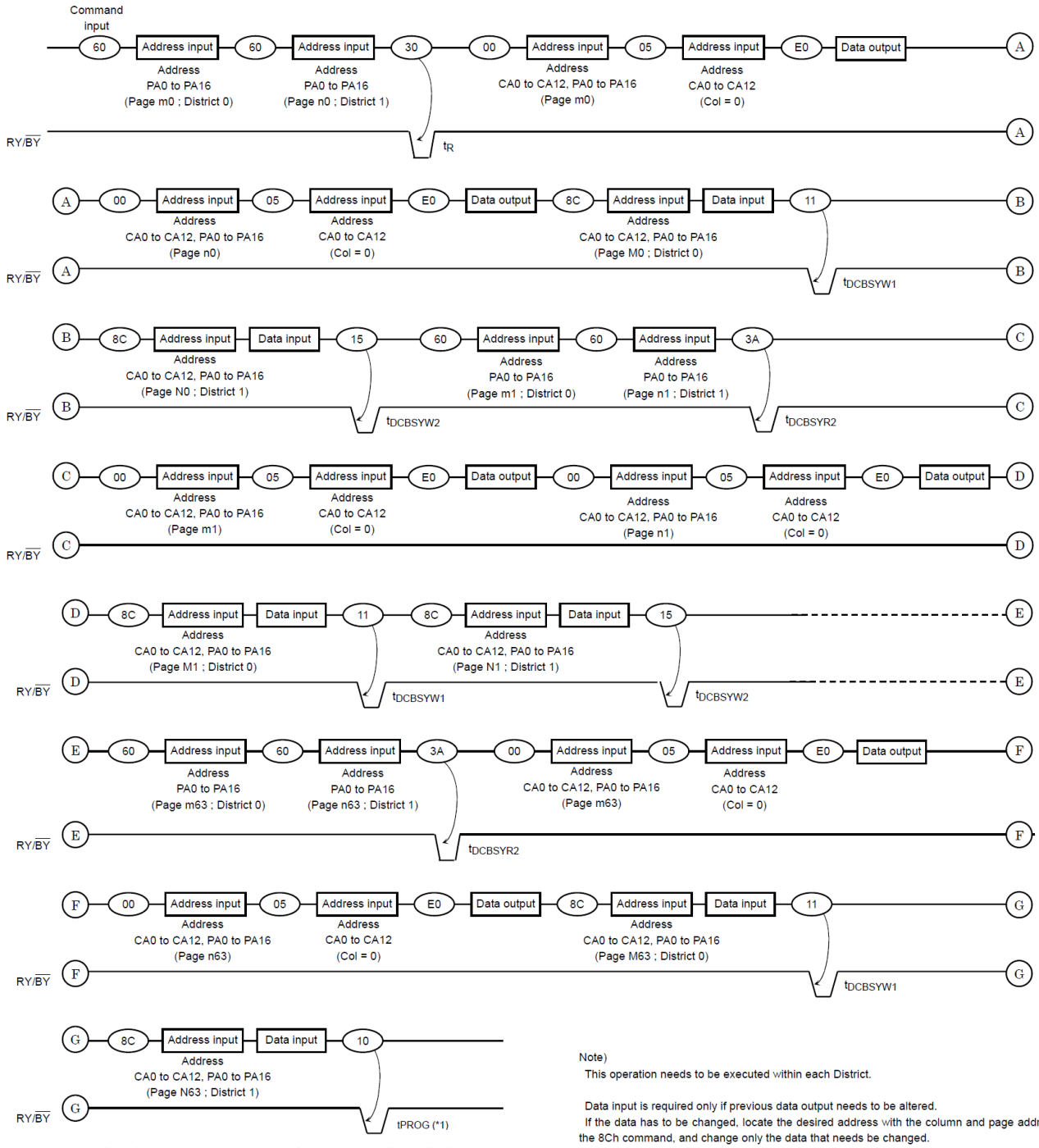
Mutil Page Copy (2)

By using Multi Page Copy (2), data in two pages can be copied to other pages after the data has been read out.

When each block address changes (increments) this sequence has to be started from the beginning.

Same page address (PA0 to PA5) within two districts has to be selected.

For X8 :



(*1) t_{PROG}: Since the last page programming by 10h command is initiated after the previous cache program, the t_{PROG}* during cache programming is given by the following equation.

t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page-A
A = (command input cycle + address input cycle + data output/input cycle time of the last page)
If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

Note)
This operation needs to be executed within each District.

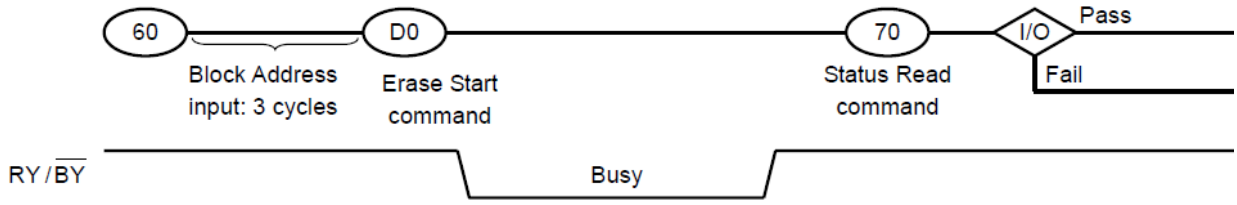
Data input is required only if previous data output needs to be altered.
If the data has to be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that needs be changed.
If the data does not have to be changed, data input cycles are not required.

Make sure $\overline{WP}$ is held to High level when Multi Page Copy (2) operation is performed.
Also make sure the Multi Page Copy operation is terminated with 8Ch-10h command sequence

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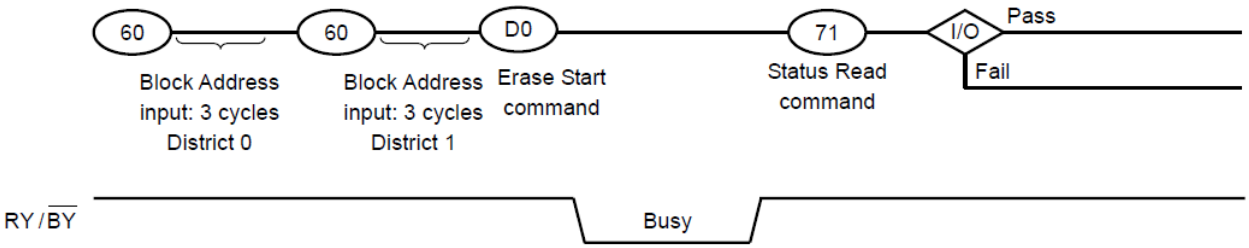
Auto Block Erase

The Auto Block Erase operation starts on the rising edge of WE after the Erase Start command “D0h” which follows the Erase Setup command “60h”. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



Multi Block Erase

The Multi Block Erase operation starts by selecting two block addresses before D0h command as in below diagram. The device automatically executes the Erase and Verify operations and the result can be monitored by checking the status by 71h status read command. For details on 71h status read command, refer to section “Multi Page Program with Data Cache”.



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Internal addressing in relation with the Districts

To use Multi Block Erase operation, the internal addressing should be considered in relation with the District.

- The device consists from 2 Districts.
- Each District consists from 1024 erase blocks.
- The allocation rule is follows.

District 0: Block 0, Block 2, Block 4, Block 6,⋯, Block 2046

District 1: Block 1, Block 3, Block 5, Block 7,⋯, Block 2047

Address input restriction for the Multi Block Erase

There are following restrictions in using Multi Block Erase

(Restriction)

Maximum one block should be selected from each District.

For example;

(60) [District 0] (60) [District 1] (D0)

(Acceptance)

There is no order limitation of the District for the address input.

For example, following operation is accepted;

(60) [District 1] (60) [District 0] (D0)

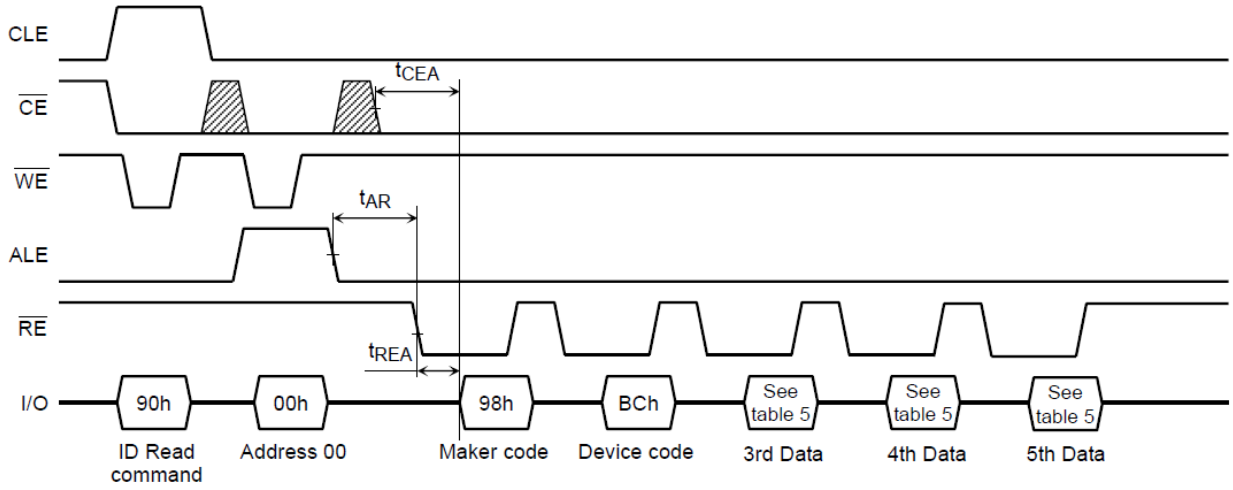
It requires no mutual address relation between the selected blocks from each District.

Make sure to terminate the operation with D0h command. If the operation needs to be terminated before D0h command input, input the FFh reset command to terminate the operation.

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ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:



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ID Definition Table (X8)

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98_H
2nd Data	Device Code	1	0	1	0	1	1	0	0	AC_H
3rd Data	Chip Number, Cell Type	1	0	0	1	0	0	0	0	90_H
4th Data	Page Size, Block Size, I/O Width	0	0	1	0	0	1	1	0	26_H
5th Data	Plane Number	0	1	1	1	0	1	1	0	76_H

3rd ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Reserved		1	0	0	1				

4th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (without redundant area)	1 KB							0	0
	2 KB							0	1
	4 KB							1	0
	8 KB							1	1
Block Size (without redundant area)	64 KB			0	0				
	128 KB			0	1				
	256 KB			1	0				
	512 KB			1	1				
I/O Width	X8		0						
Reserved		0				0	1		

5th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1 Plane					0	0		
	2 Plane					0	1		
	4 Plane					1	0		
	8 Plane					1	1		
Reserved		0	1	1	1			1	0

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Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using $\overline{RE}$ after a “70h” command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

Status Register Definition for 70_H Command

I/O	Page Program	Block Erase	Read	Cache Read	Cache Program	Definition
I/O 0	Pass / Fail	Pass / Fail	Invalid	Invalid	Pass / Fail	Chip Status1 Pass : 0 / Fail : 1
I/O 1	Invalid	Invalid	Invalid	Invalid	Pass / Fail	Chip Status2 Pass : 0 / Fail : 1
I/O 2	0	0	0	0	0	Not Used
I/O 3	0	0	0	0	0	Not Used
I/O 4	0	0	0	0	0	Not Used
I/O 5	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Page Buffer Busy : 0 / Ready : 1
I/O 6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Busy : 0 / Ready : 1
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Write Prot Protected : 0 / Not Protected : 1

NOTE The Pass/Fail status on I/O0 and I/O1 is only valid during a Program/Erase operation when the device is in the Ready state.

Chip Status 1:

During a Auto Page Program or Auto Block Erase operation this bit indicates the pass/fail result.

During a Auto Page Programming with Data Cache operation, this bit shows the pass/fail results of the current page program operation, and therefore this bit is only valid when I/O5 shows the Ready state.

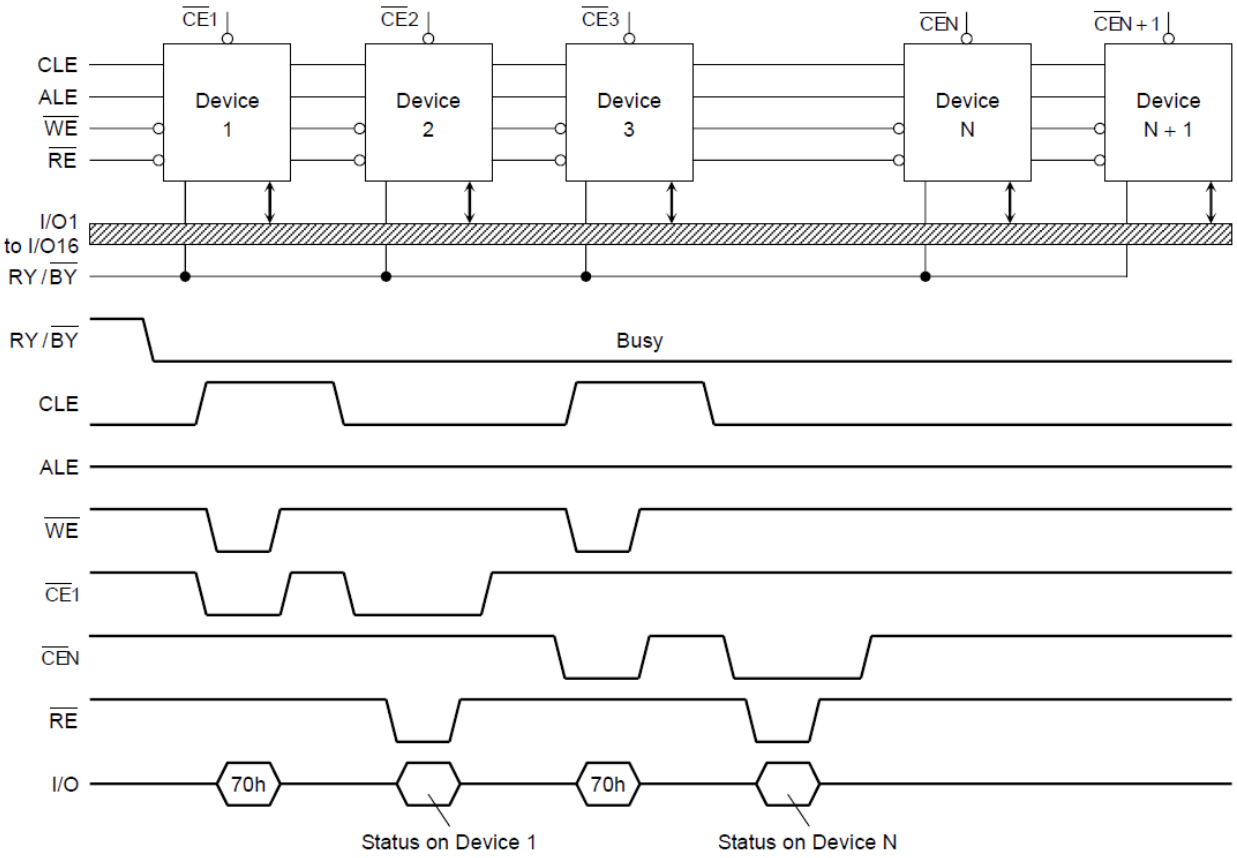
Chip Status 2:

This bit shows the pass/fail result of the previous page program operation during Auto Page Programming with Data Cache. This status is valid when I/O6 shows the Ready State.

The status output on the I/O5 is the same as that of I/O6 if the command input just before the 70h is not 15h or 31h.

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An application example with multiple devices is shown in the figure below.



System Design Note: If the $\overline{RY}$ / $\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

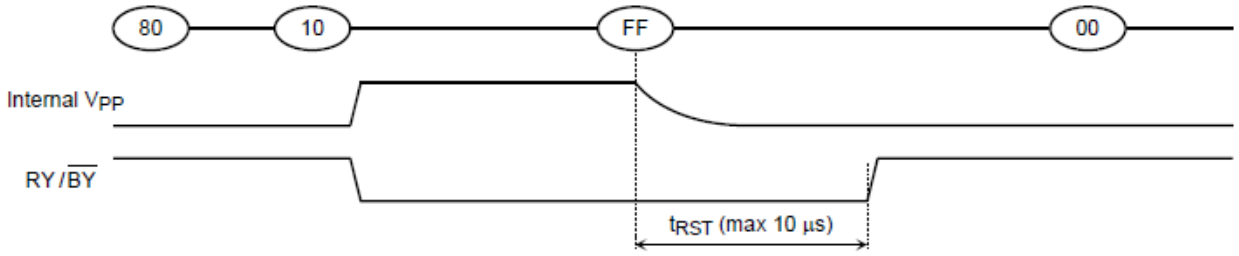
Reset

The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state.

Reset during a Cache Program/Page Copy may not just stop the most recent page program but it may also stop the previous program to a page depending on when the FF reset is input.

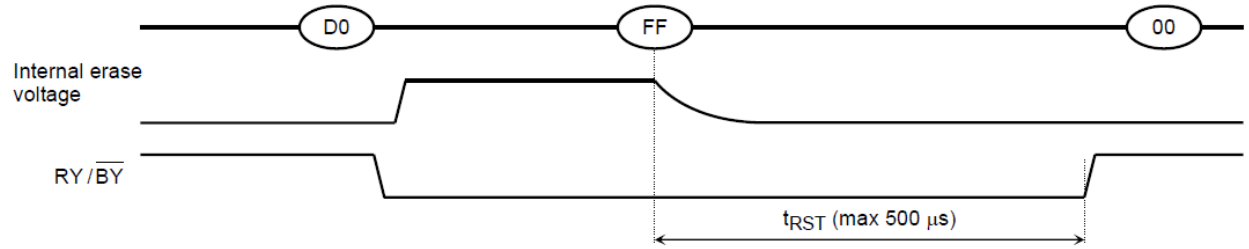
The response to a “FFh” Reset command input during the various device operations is as follows:

When a Reset (FFh) command is input during programming

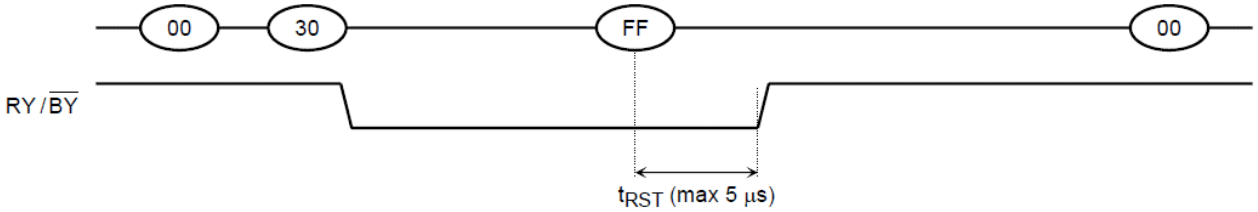


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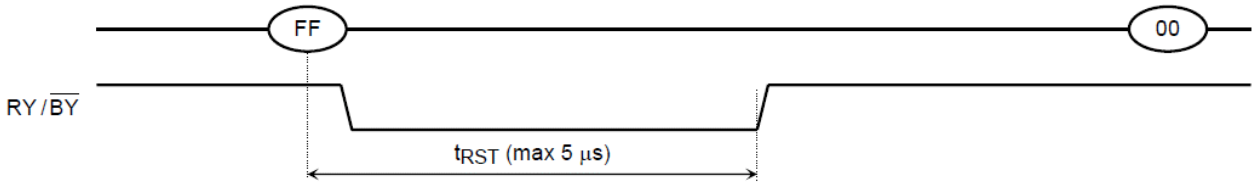
When a Reset (FFh) command is input during erasing



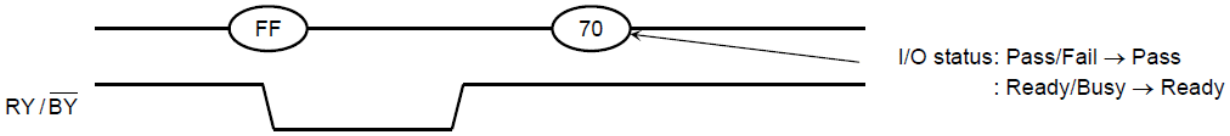
When a Reset (FFh) command is input during Read operation



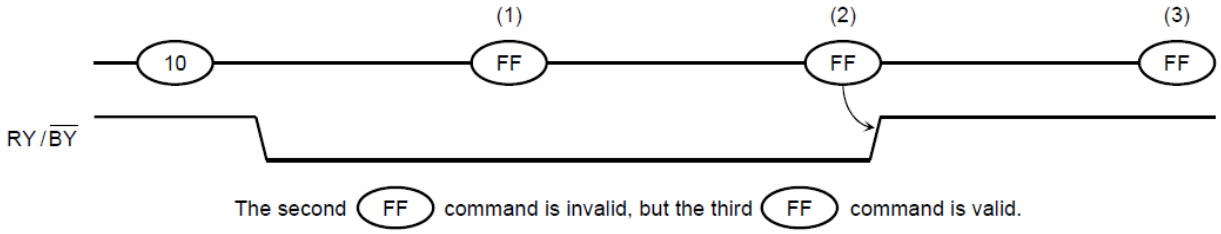
When a Reset (FFh) command is input during Ready



When a Status Read command (70h) is input after a Reset



When two or more Reset commands are input in succession



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APPLICATION NOTES AND COMMENTS

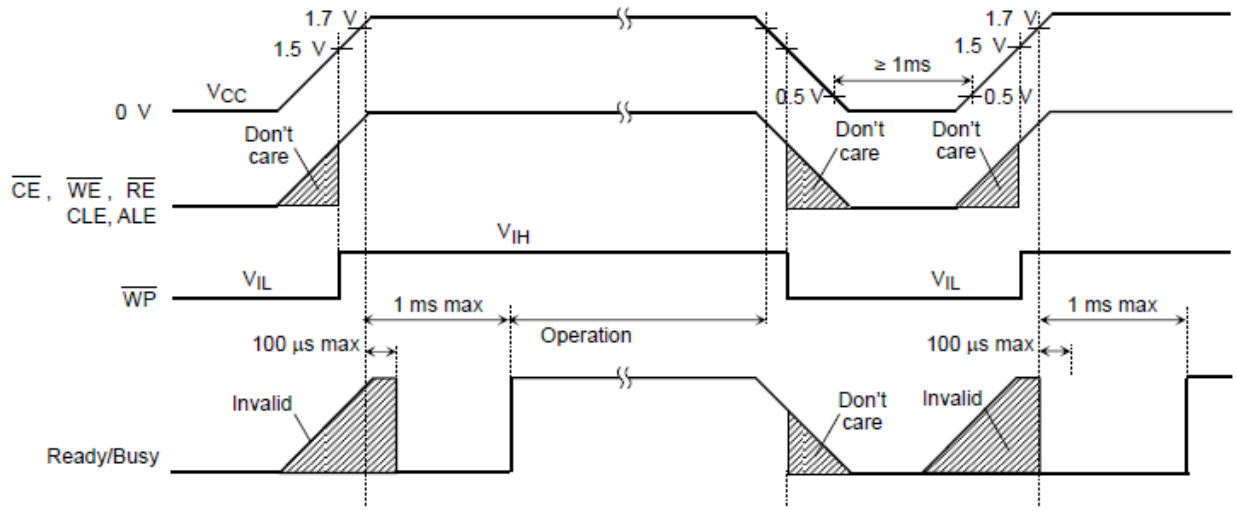
(1)Power-on/off sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence.

During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.

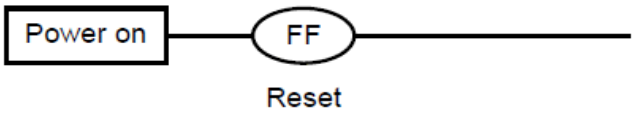
The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off.



(2) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

(3)Power-on Reset

The following sequence is necessary because some input signals may not be stable at power-on.



(4)Prohibition of unspecified commands

The operation commands are listed in Logic Table. Input of a command other than those specified in Logic Table is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

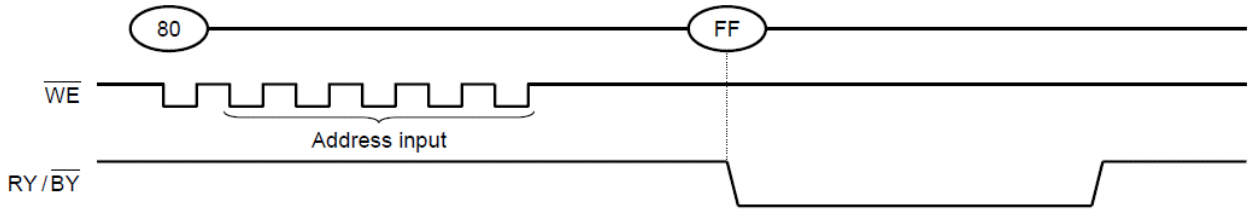
(5)Restriction of commands while in the Busy state

During the Busy state, do not input any command except 70h(71h) and FFh.

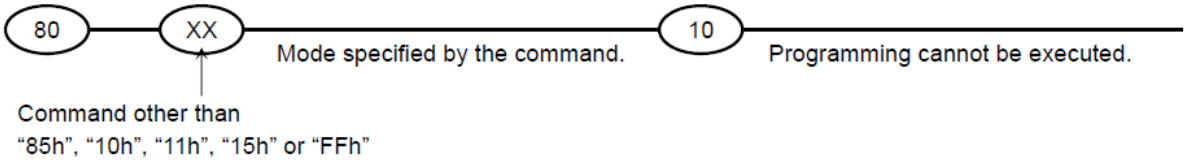
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(6)Acceptable commands after Serial Input command “80h”

Once the Serial Input command “80h” has been input, do not input any command other than the Column Address Change in Serial Data Input command “85h”, Auto Program command “10h”, Multi Page Program command “11h”, Auto Program with Data Cache Command “15h”, or the Reset command “FFh”.

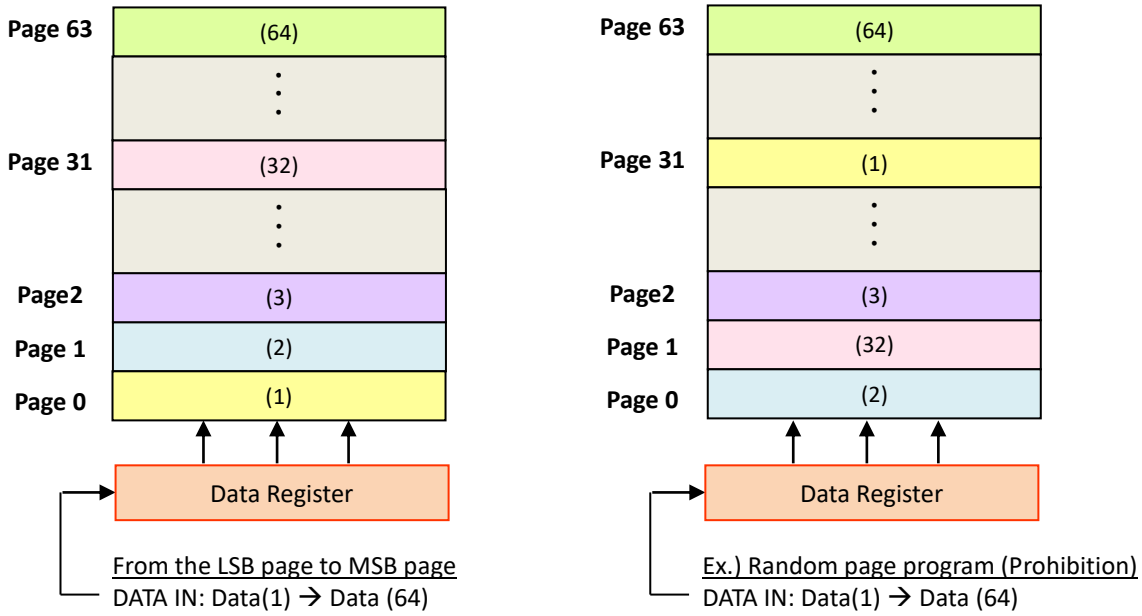


If a command other than “85h” , “10h” , “11h” , “15h” or “FFh” is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.



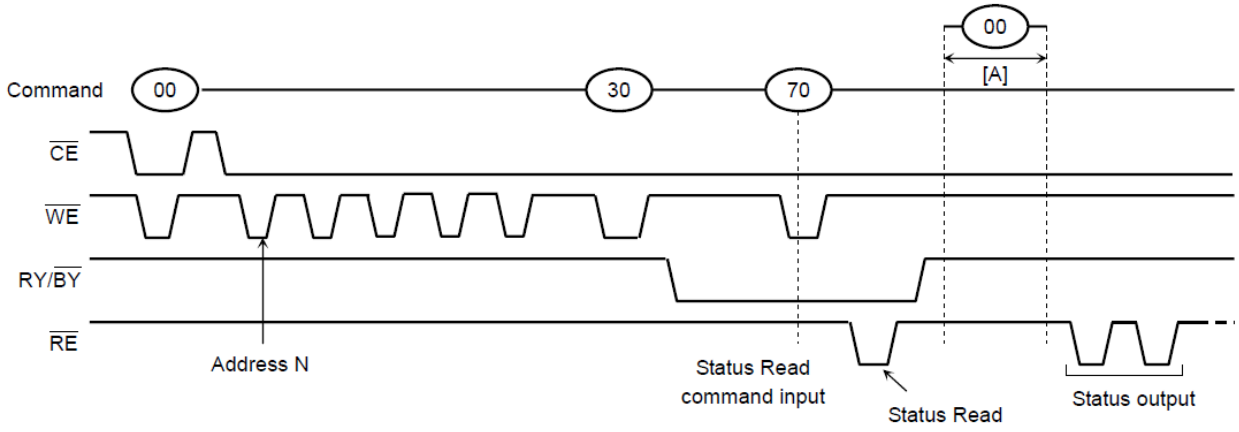
(7)Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.



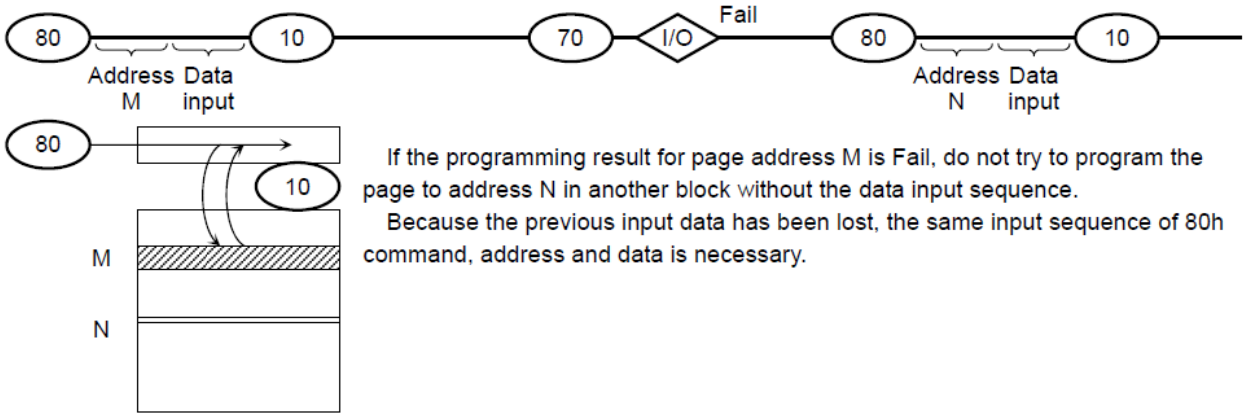
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(8)Status Read during a Read operation



The device status can be read out by inputting the Status Read command “70h” in Read mode. Once the device has been set to Status Read mode by a “70h” command, the device will not return to Read mode unless the Read command “00h” is inputted during [A]. If the Read command “00h” is inputted during [A], Status Read mode is reset, and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

(9)Auto programming failure



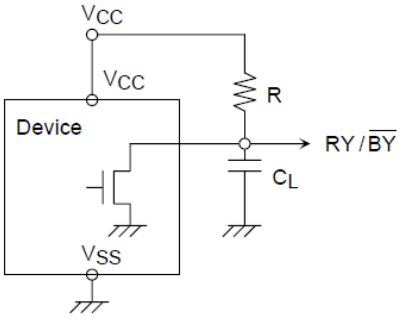
If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.

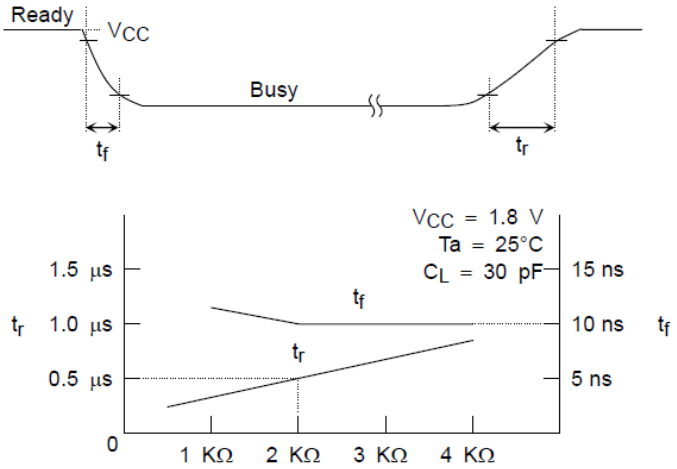
Because the previous input data has been lost, the same input sequence of 80h command, address and data is necessary.

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(10)RY / $\overline{BY}$: termination for the Ready/Busy pin (RY / $\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY / $\overline{BY}$ buffer consists of an open drain circuit.





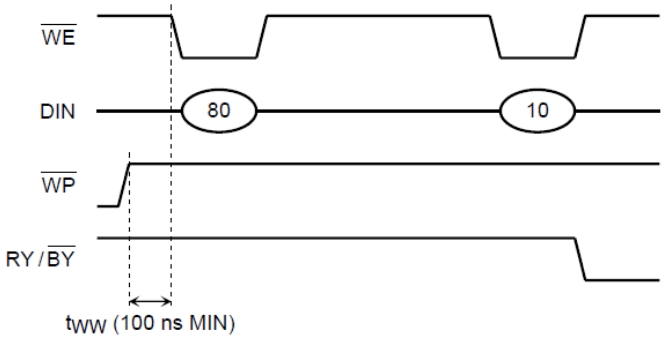
This data may vary from device to device. We recommend that you use this data as a reference when selecting a resistor value.

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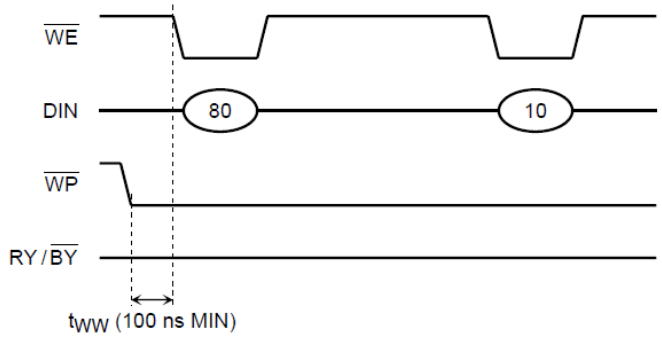
(11)Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when WP goes Low. The operations are enabled and disabled as follows:

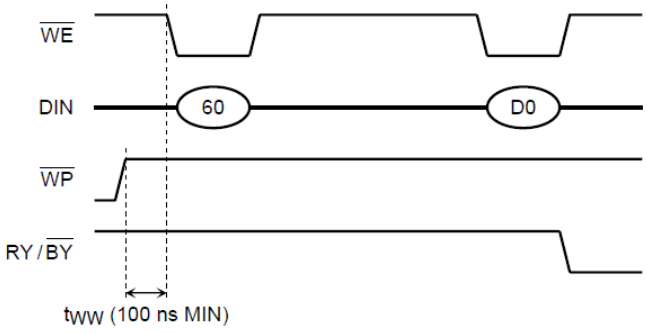
Enable Programming



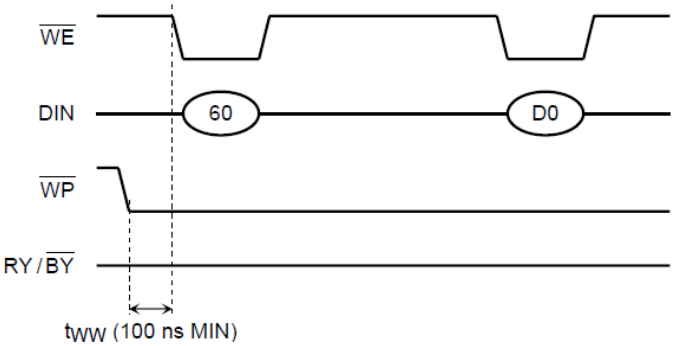
Disable Programming



Enable Erasing



Disable Erasing

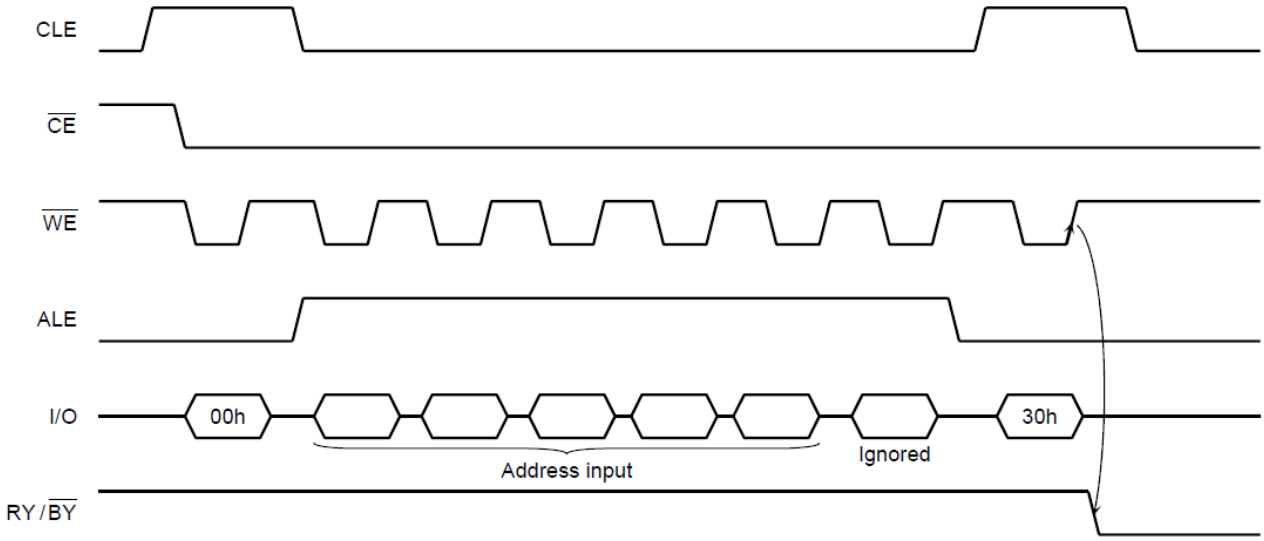


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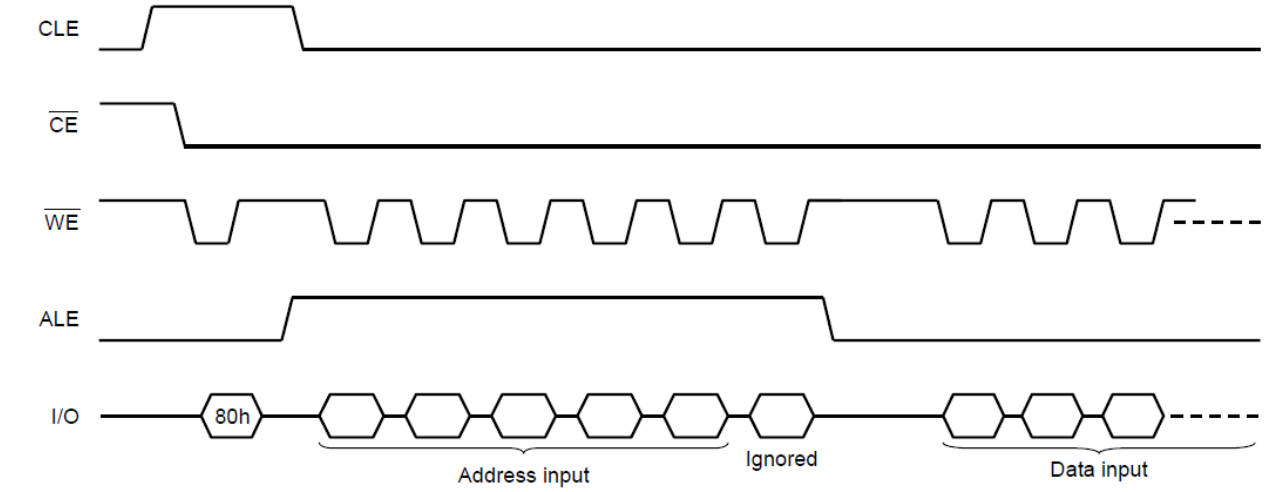
(12)When six address cycles are input

Although the device may read in a sixth address, it is ignored inside the chip.

Read operation



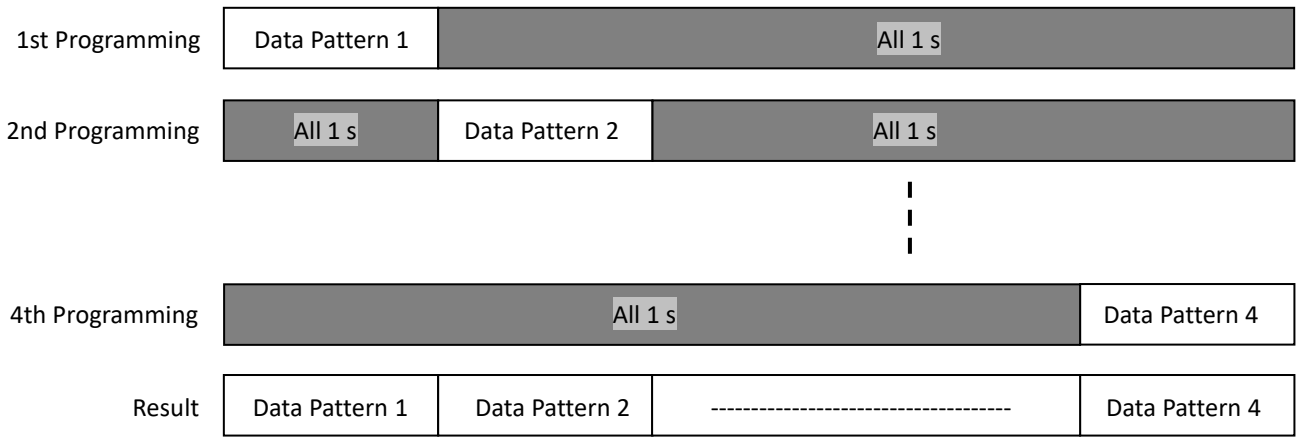
Program operation



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(13)Several programming cycles on the same page (Partial Page Program)

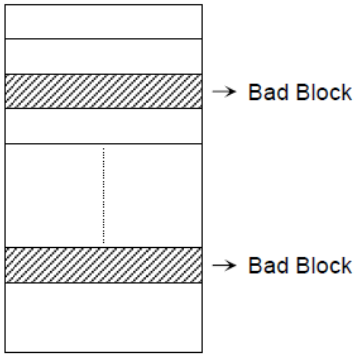
Each segment can be programmed individually as follows:



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(14)Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.
Check if the device has any bad blocks after installation into the system.
Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.
A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

NOTE: Additional invalid blocks may develop within life time in the device; however, the total valid blocks will not drop below minimum valid blocks during the endurance life.

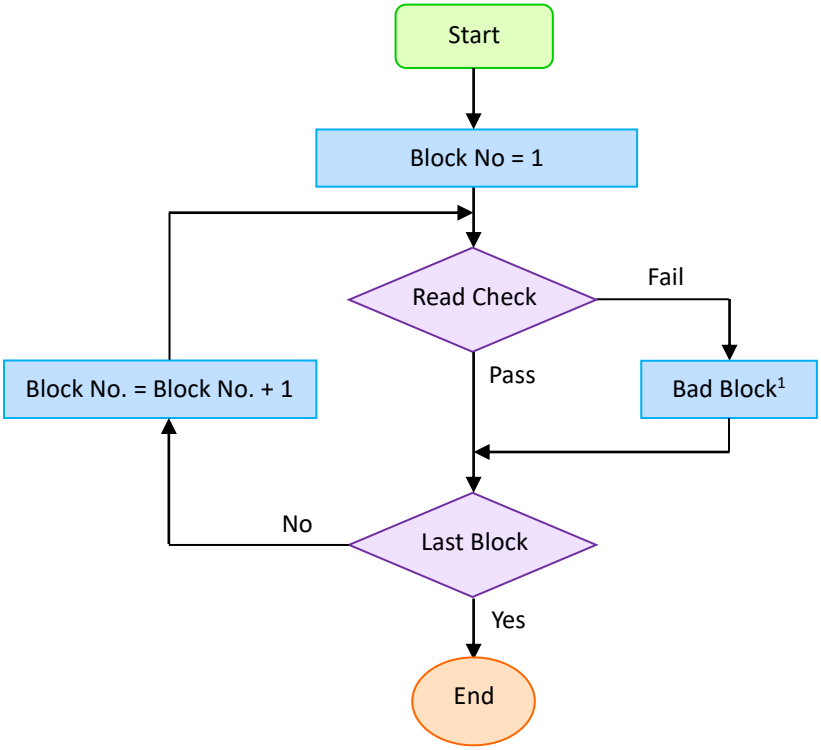
The number of valid blocks over the device lifetime is as follows:

Symbol	Min	Typ.	Max	Unit
Valid(Good) Block Number	2,008	—	2,048	Blocks

Bad Block Test Flow

Regarding invalid blocks, bad block mark is in whole pages.

Please read one column of any page in each block. It makes sure that every invalid block has “0” data at this column. If the data of the column is “0”, define the block as a bad block.



Note1: No erase operation is allowed to detected bad blocks.

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(15)Failure phenomena for Program and Erase Operations

The device may fail during a Program or Erase operation.

The following possible failure modes should be considered when implementing a highly reliable system.

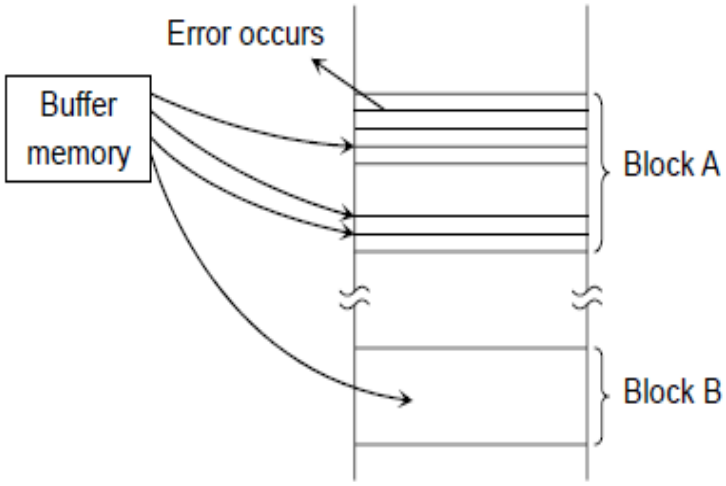
Failure Mode		Detection and Countermeasure Sequence
Block	Erase Failure	Read Status after Erase → Block Replacement
Page	Programming Failure	Read Status after Program → Block Replacement
Read	Bit Error	ECC Correction / Block Refresh

NOTE 1 ECC: Error Correction Code. 8 bit correction per 512 Bytes is necessary.

Block Replacement

Program

When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).



Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(16) The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

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(17)Reliability Guidance

This reliability guidance is intended to notify some guidance related to using NAND flash with 8bit ECC for each 512 bytes. For detailed reliability data, please refer to TOSHIBA's reliability note.

Although random bit errors may occur during use, it does not necessarily mean that a block is bad.

Generally, a block should be marked as bad when a program status failure or erase status failure is detected.

The other failure modes may be recovered by a block erase.

ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

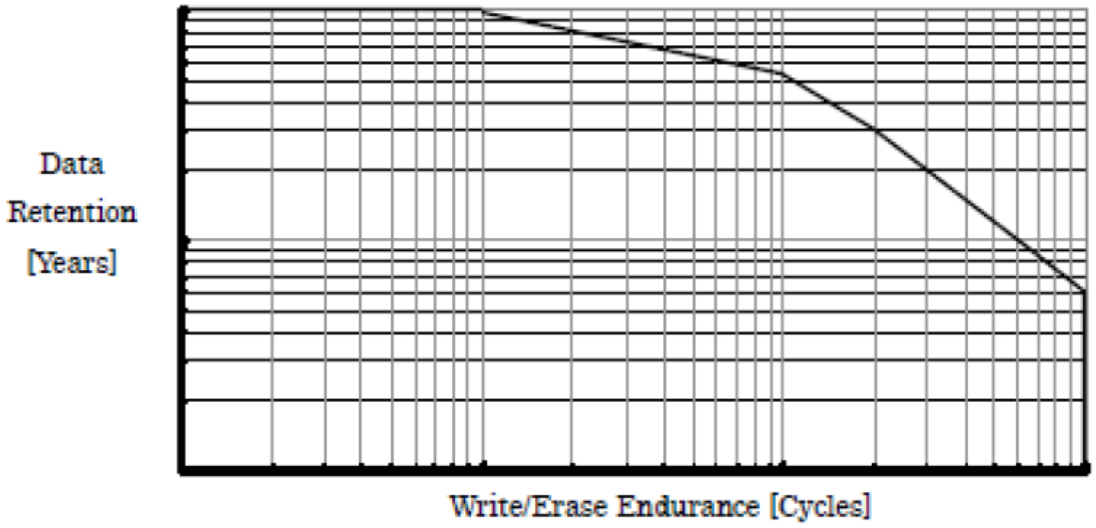
■ Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

■ Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again.

Here is the combined characteristics image of Write/Erase Endurance and Data Retention.



■ Read Disturb

A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

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(18)Endurance Test Guideline

■ Data Background

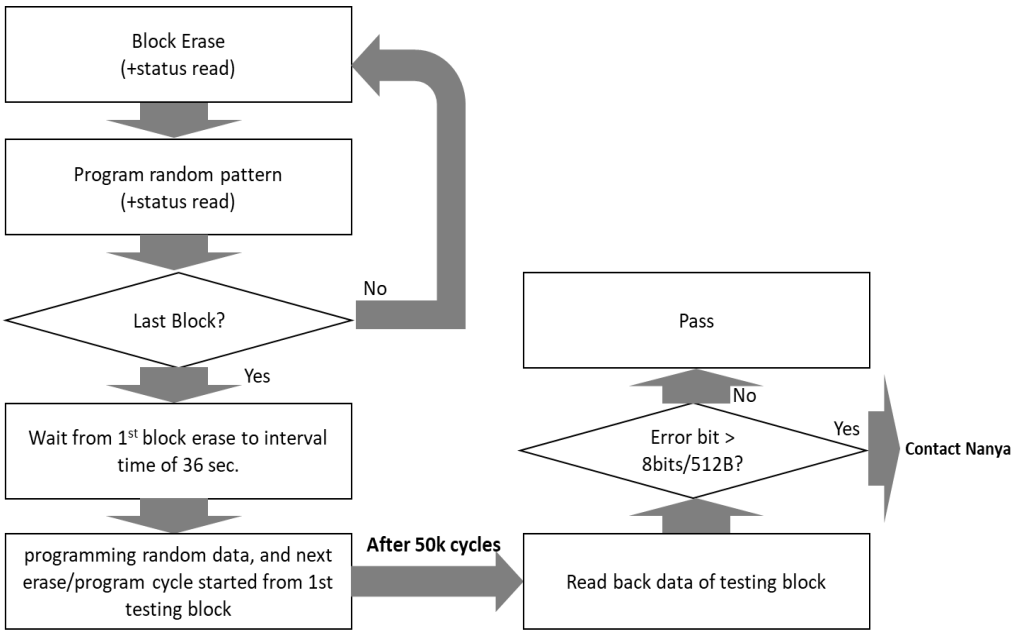
According to the description of JESD22-A117C, if the user performs stress test in the verification process, the data background must be quasi-random to consist with the actual operation scenario, please contact with Nanya if any question in random data.

■ Intentional Interval Time between Cycle

In JESD22-A117C mention, to avoid unrealistic stress during endurance testing it is necessary to insert additional interval time between write/erase cycles. Nanya recommends 36 second interval time between write/erase.

500 hours / 50k (the max cycle spec.) = 36 second.

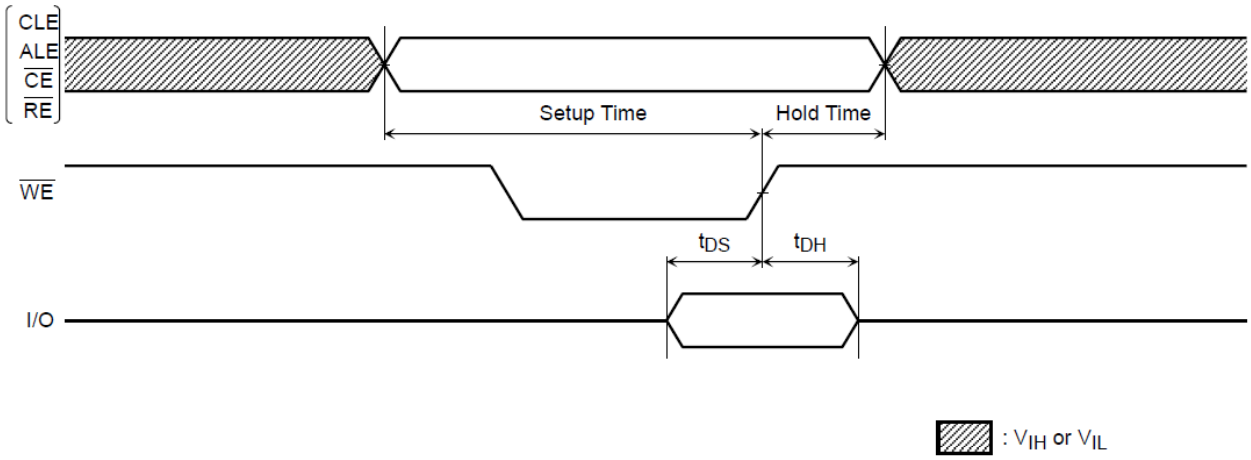
■ Testing Flow



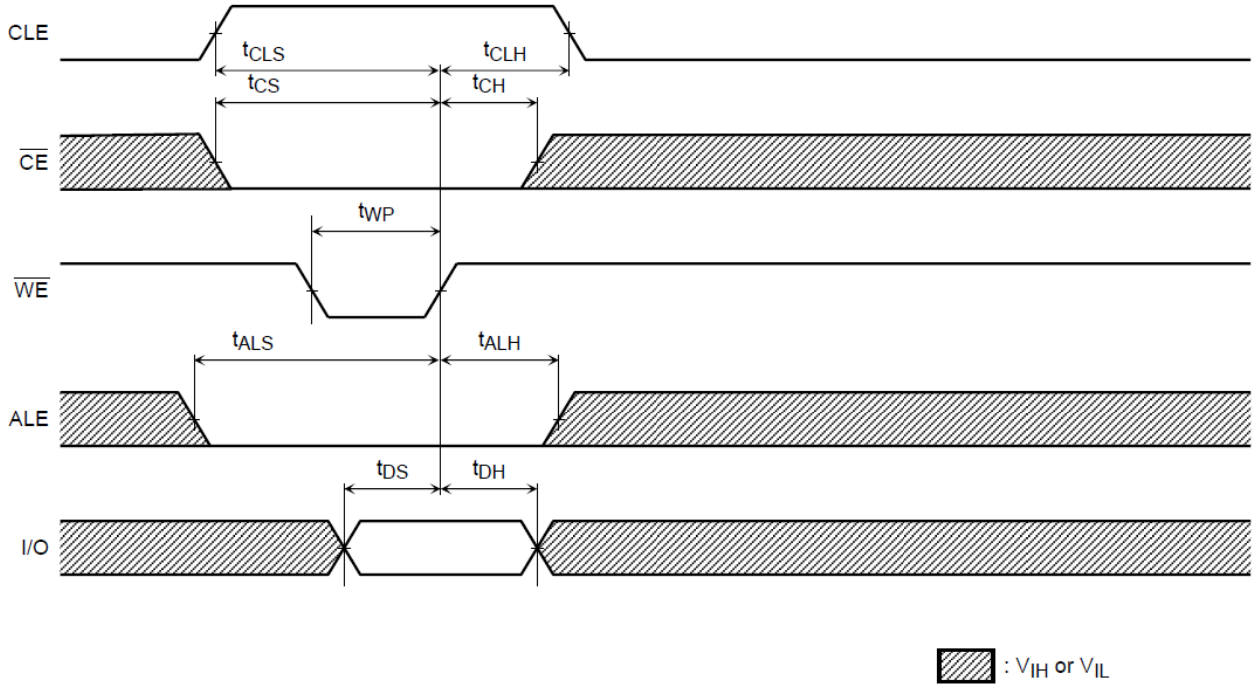
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TIMING DIAGRAMS

Latch Timing Diagram for Command/Address/Data

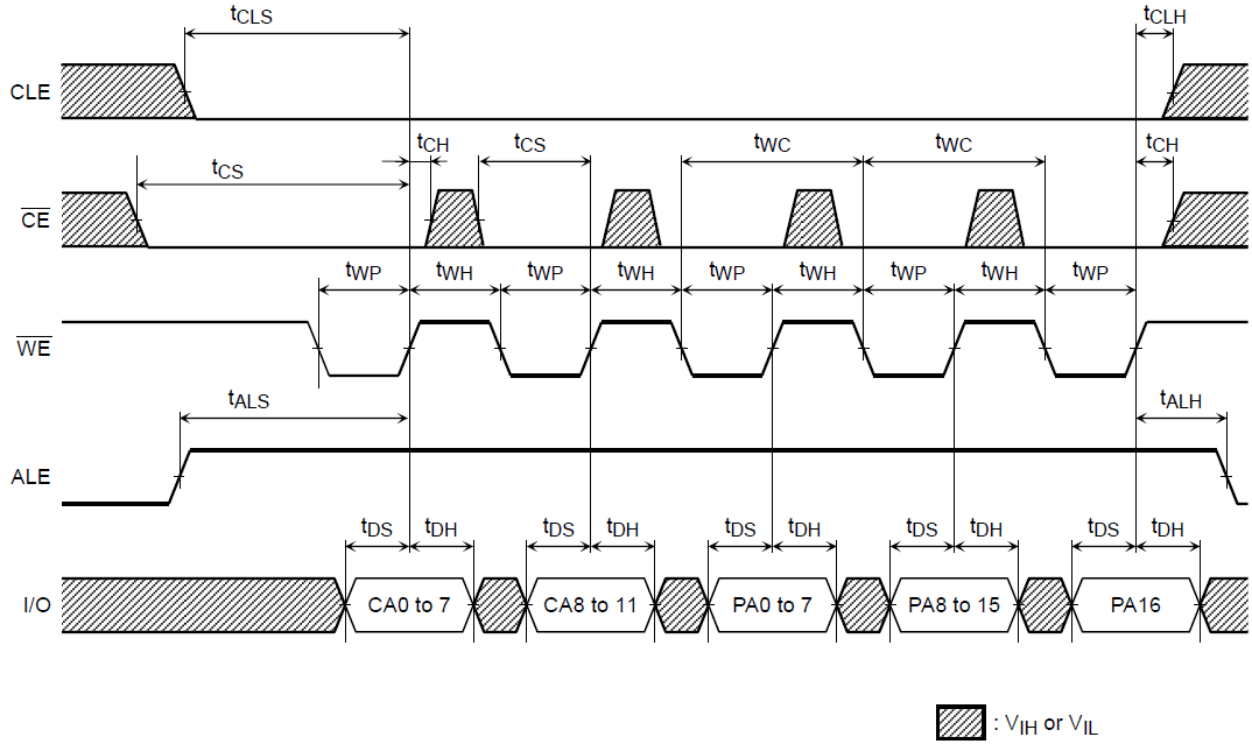


Command Input Cycle Timing Diagram

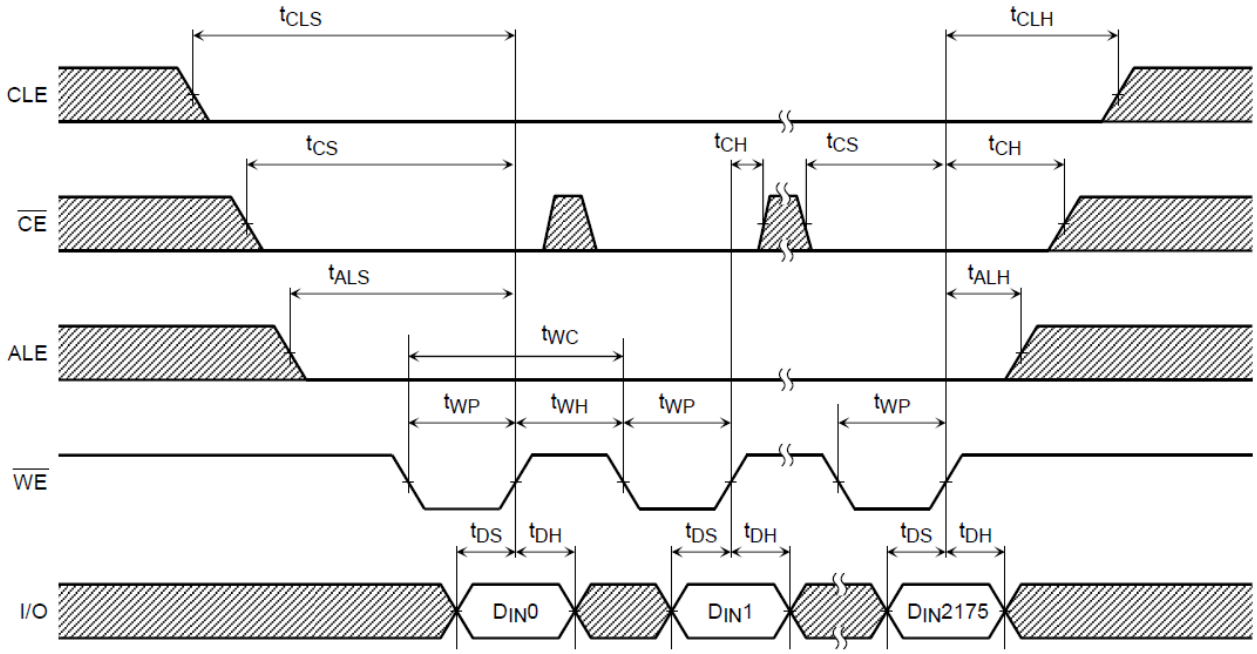


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Address Input Cycle Timing Diagram

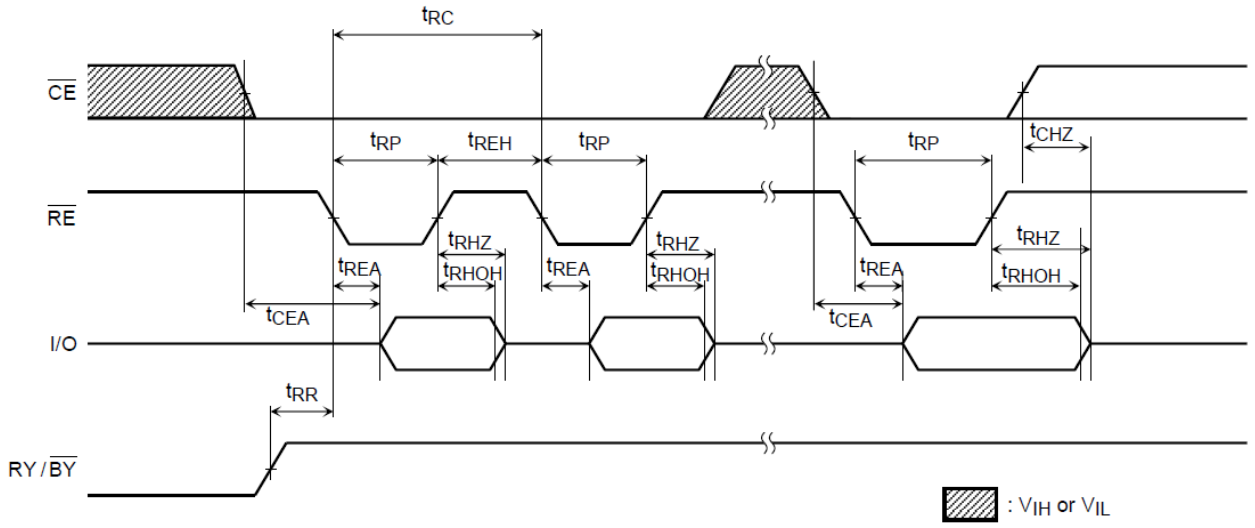


Data Input Cycle Timing Diagram

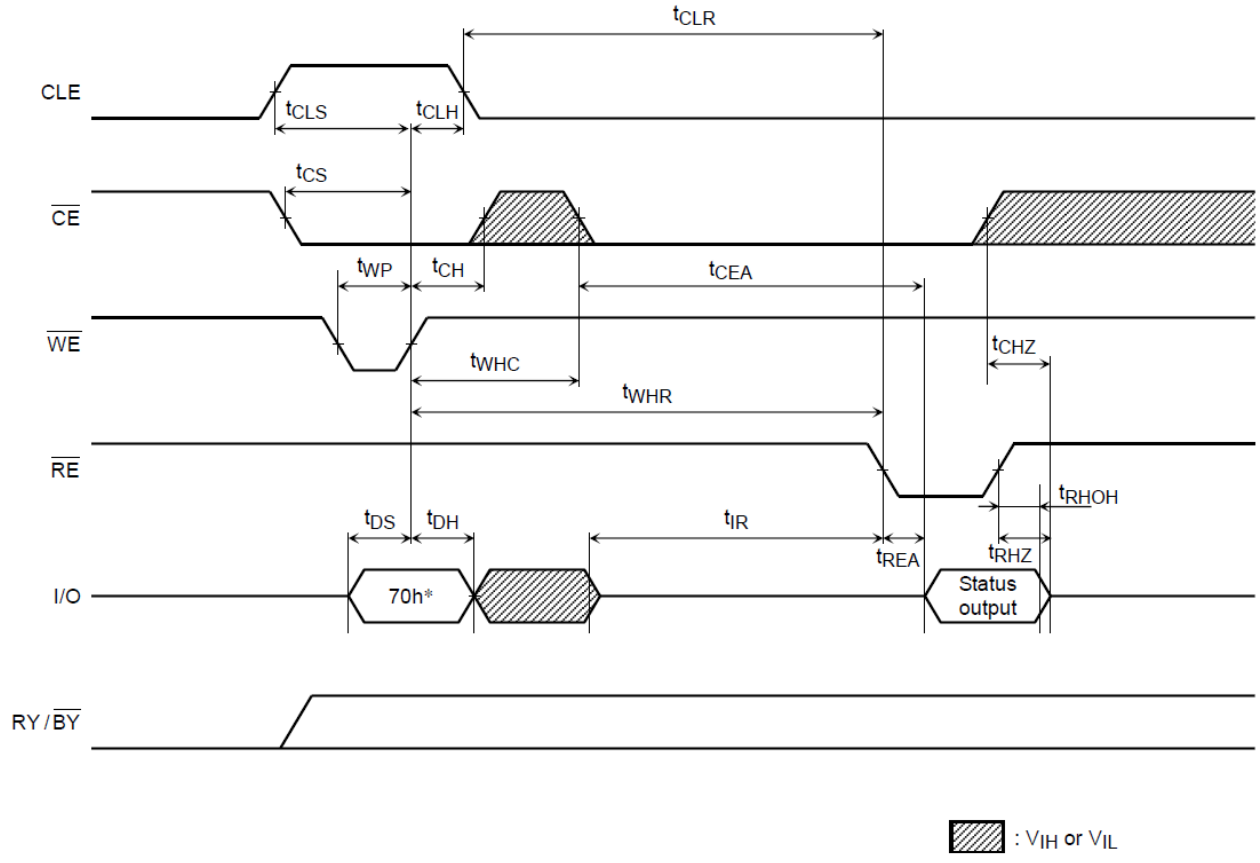


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Serial Read Cycle Timing Diagram



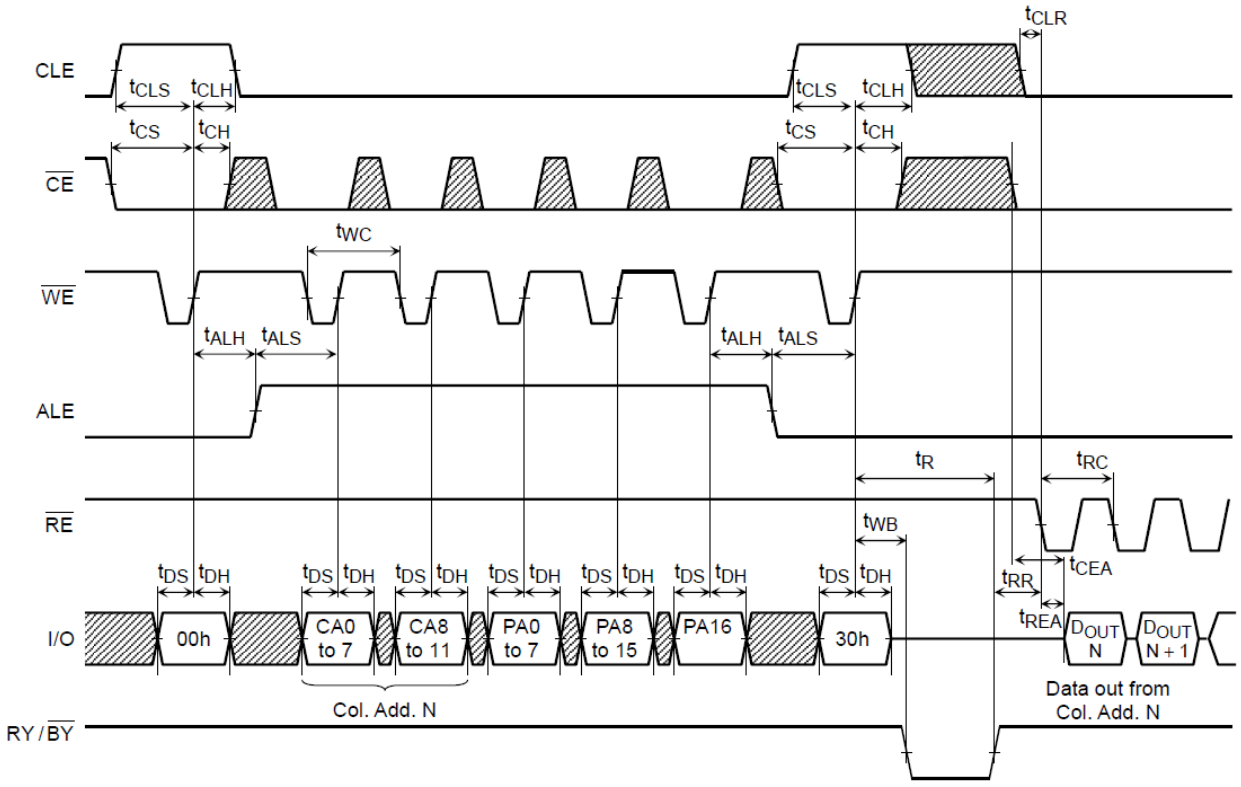
Status Read Cycle Timing Diagram



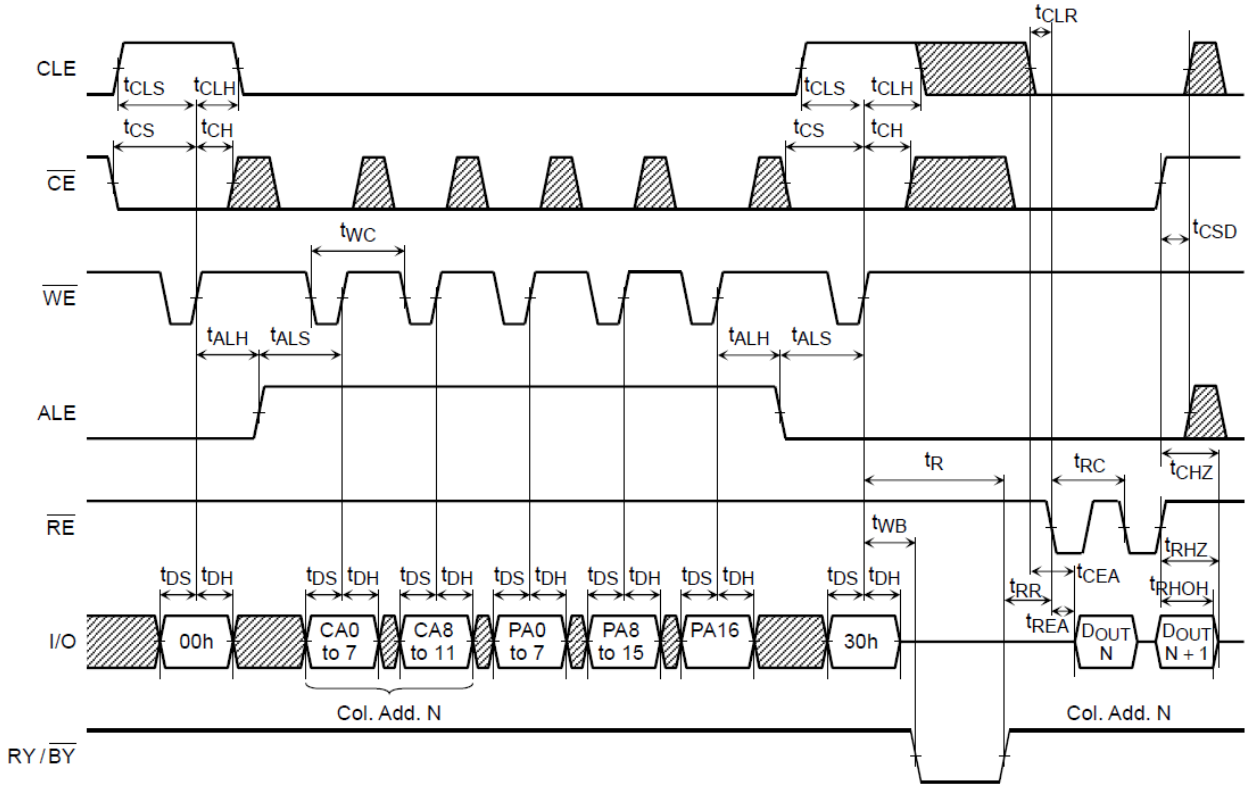
*: 70h represents the hexadecimal number

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Read Cycle Timing Diagram

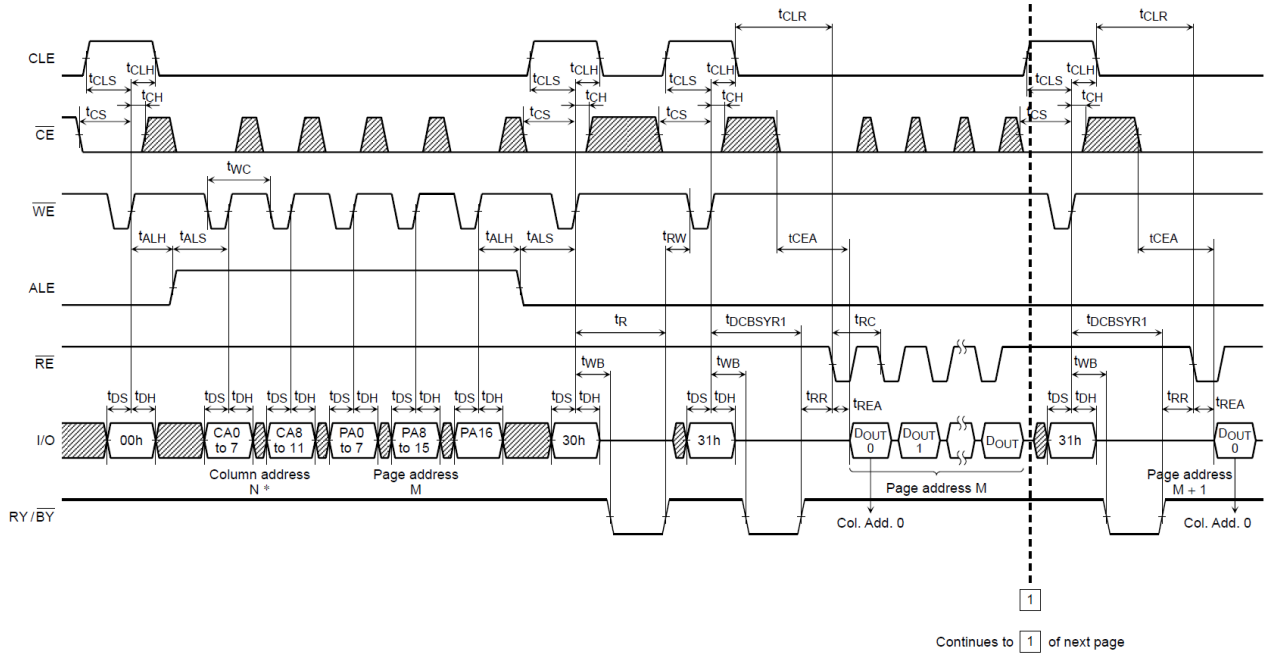


Read Cycle Timing Diagram: When Interrupted by $\overline{CE}$



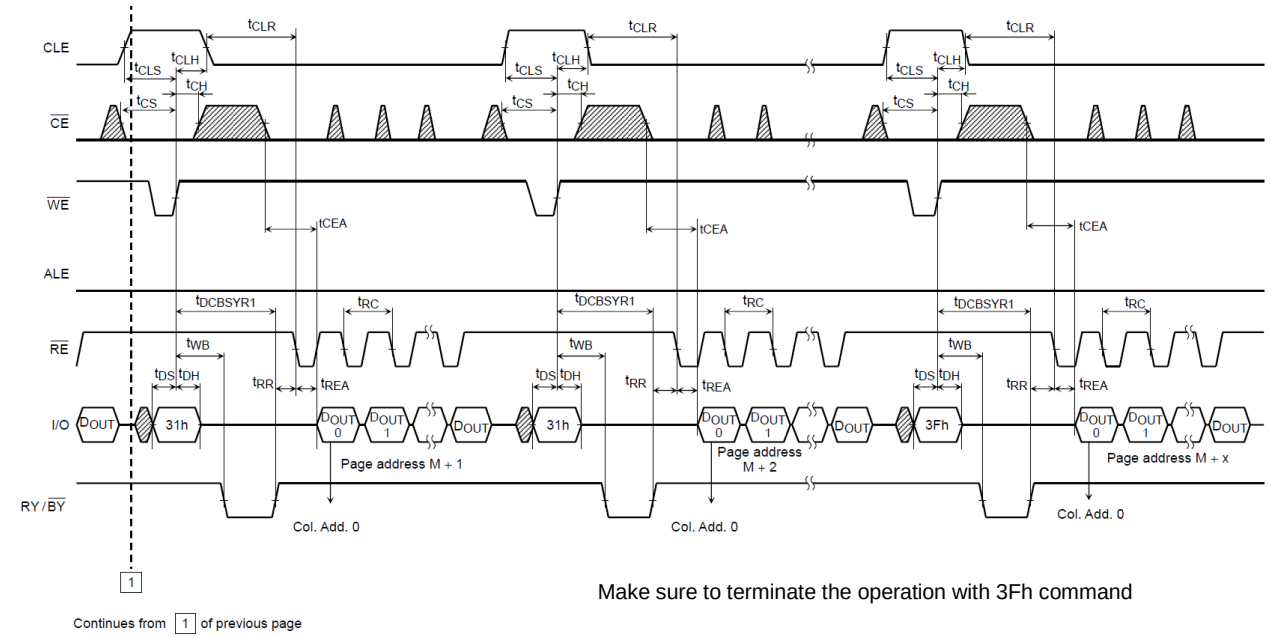
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Read Cycle with Data Cache Timing Diagram (1/2)



*: The column address will be reset to 0 by the 31h command input.

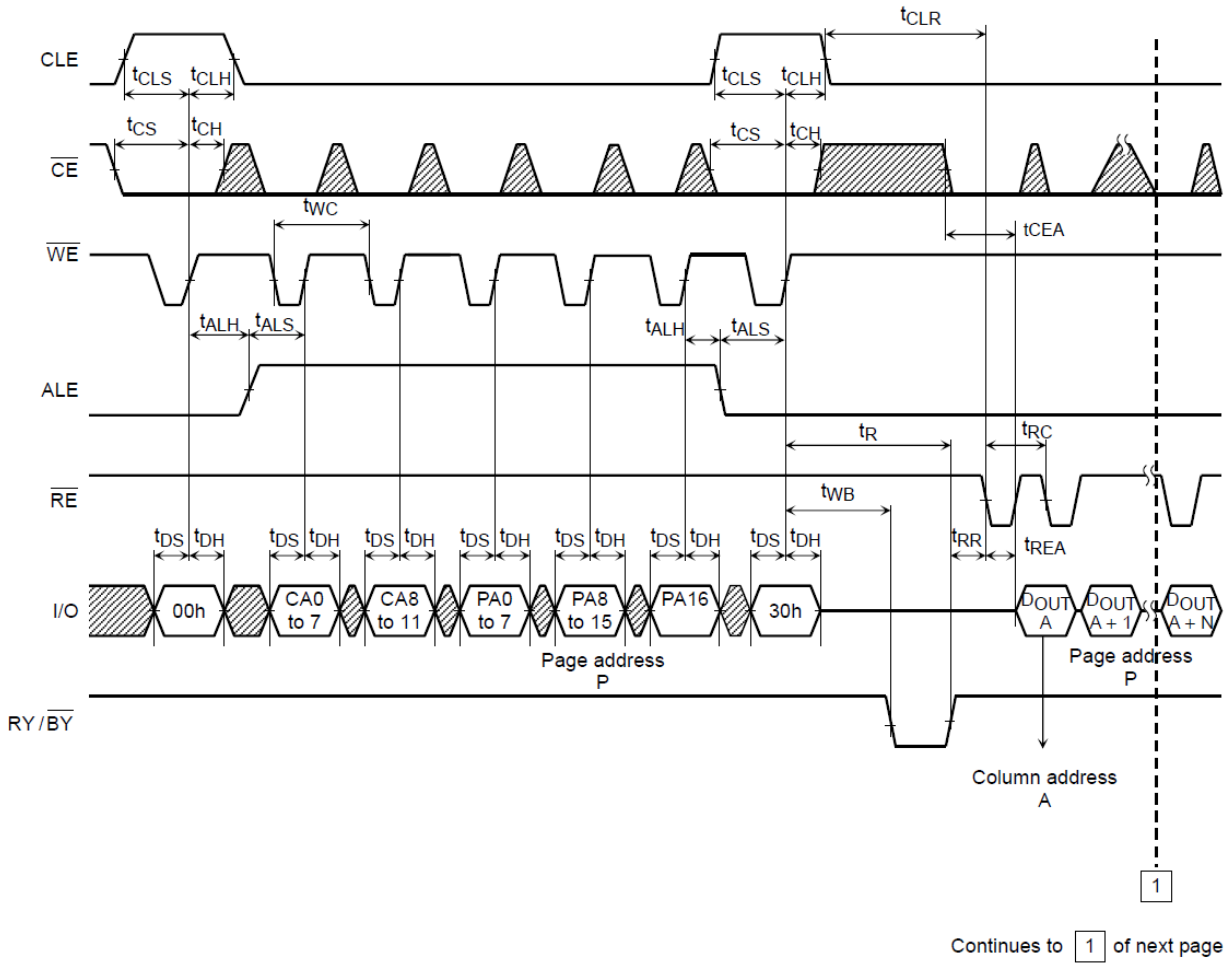
Read Cycle with Data Cache Timing Diagram (2/2)



.

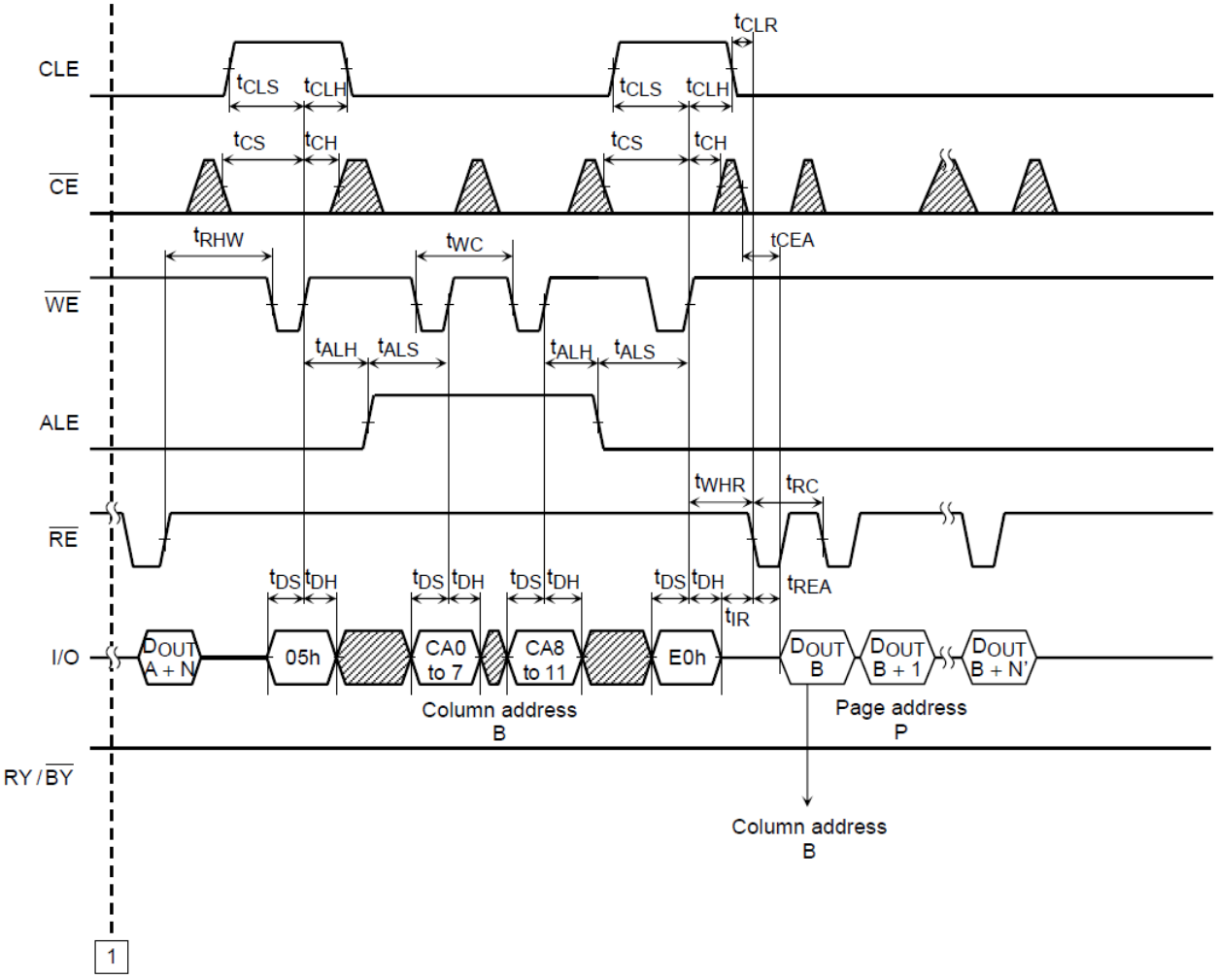
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Column Address Change in Read Cycle Timing Diagram (1/2)



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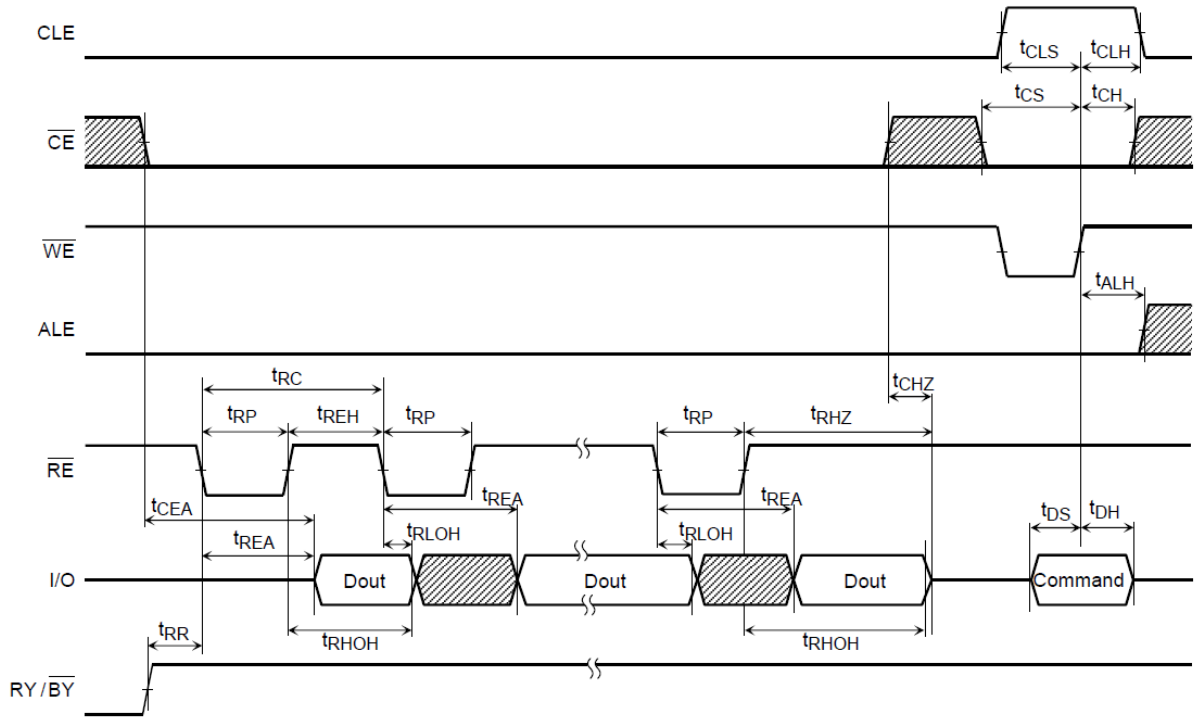
Column Address Change in Read Cycle Timing Diagram (2/2)



Continues from 1 of previous page

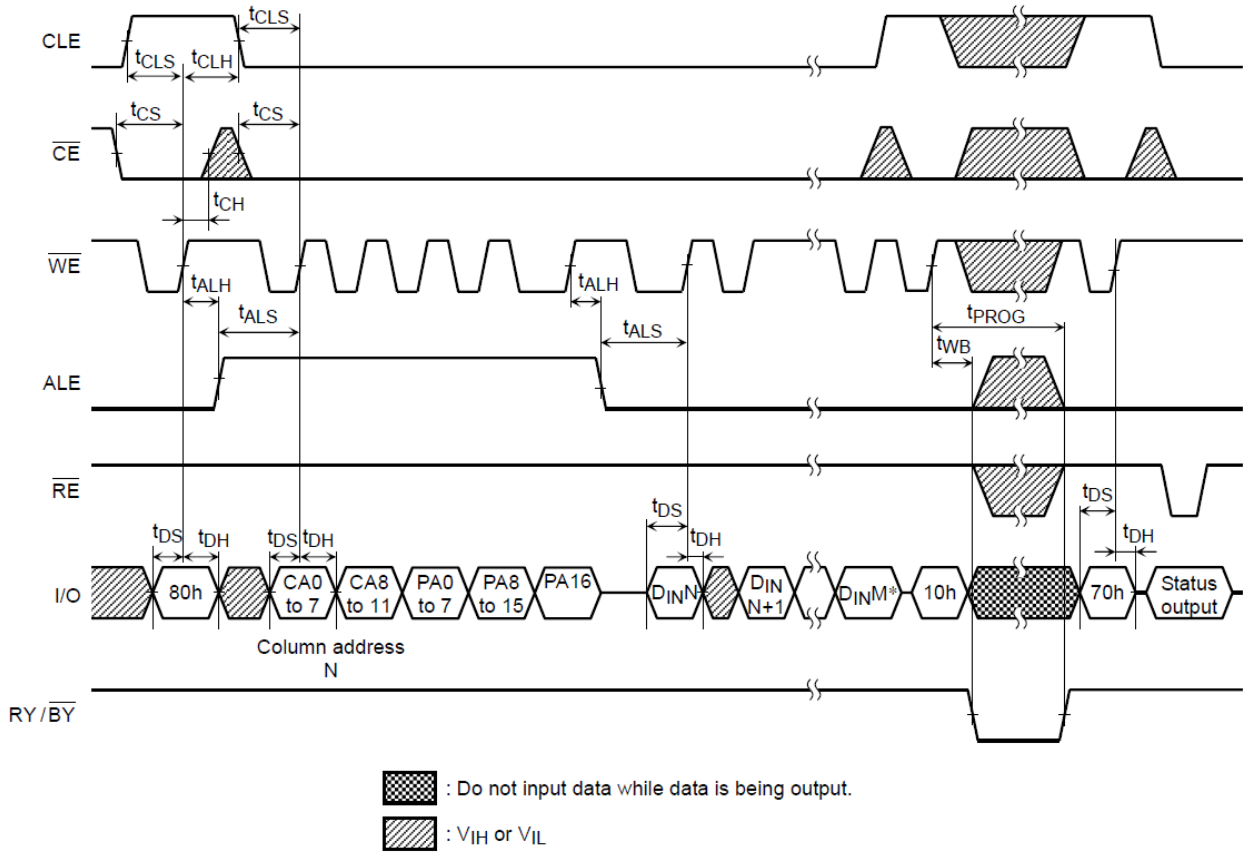
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Data Output Timing Diagram



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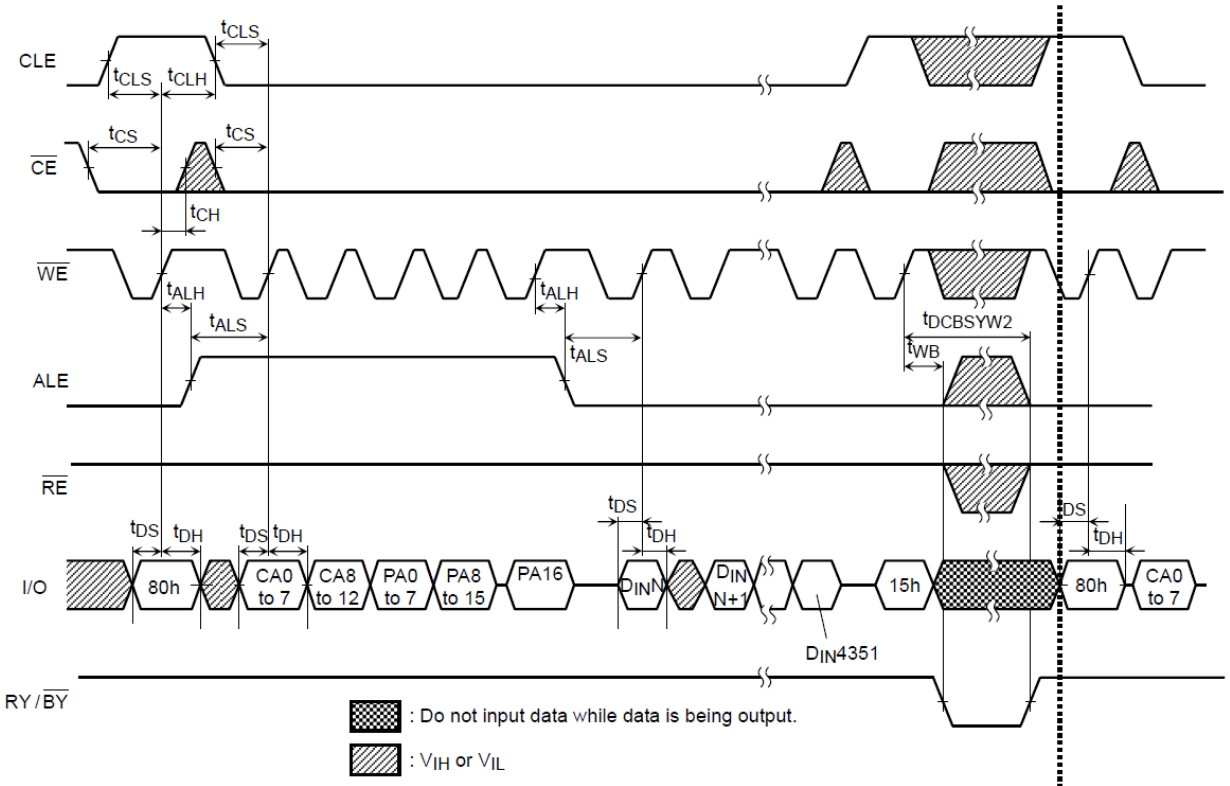
Auto-Program Operation Timing Diagram



*: M: up to 4351 (byte input data for ×8 device).

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Auto-Program Operation with Data Cache Timing Diagram (1/3)



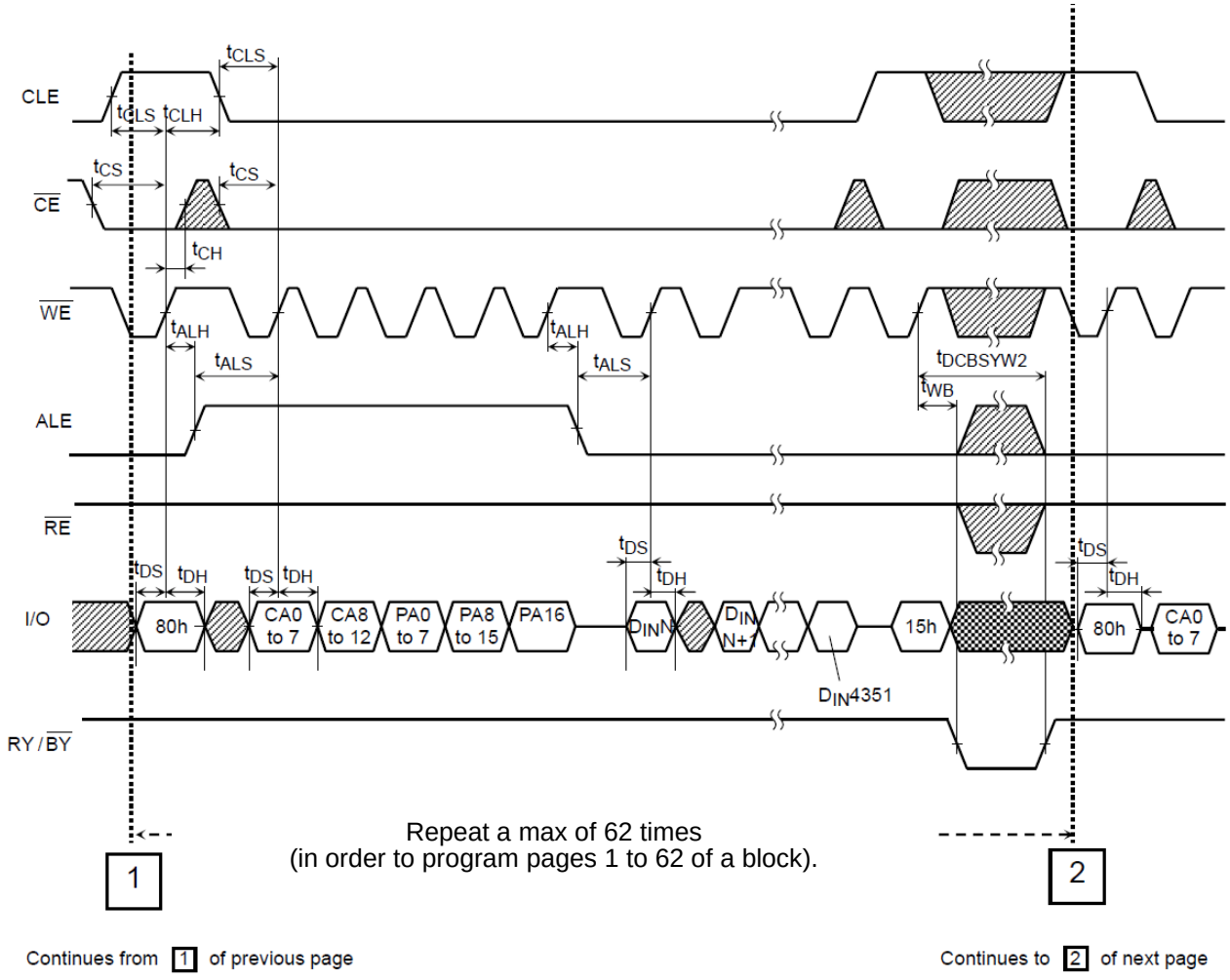
CA0 to CA12 is 0 in this diagram.

1

Continues to 1 of next page

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Auto-Program Operation with Data Cache Timing Diagram (2/3)

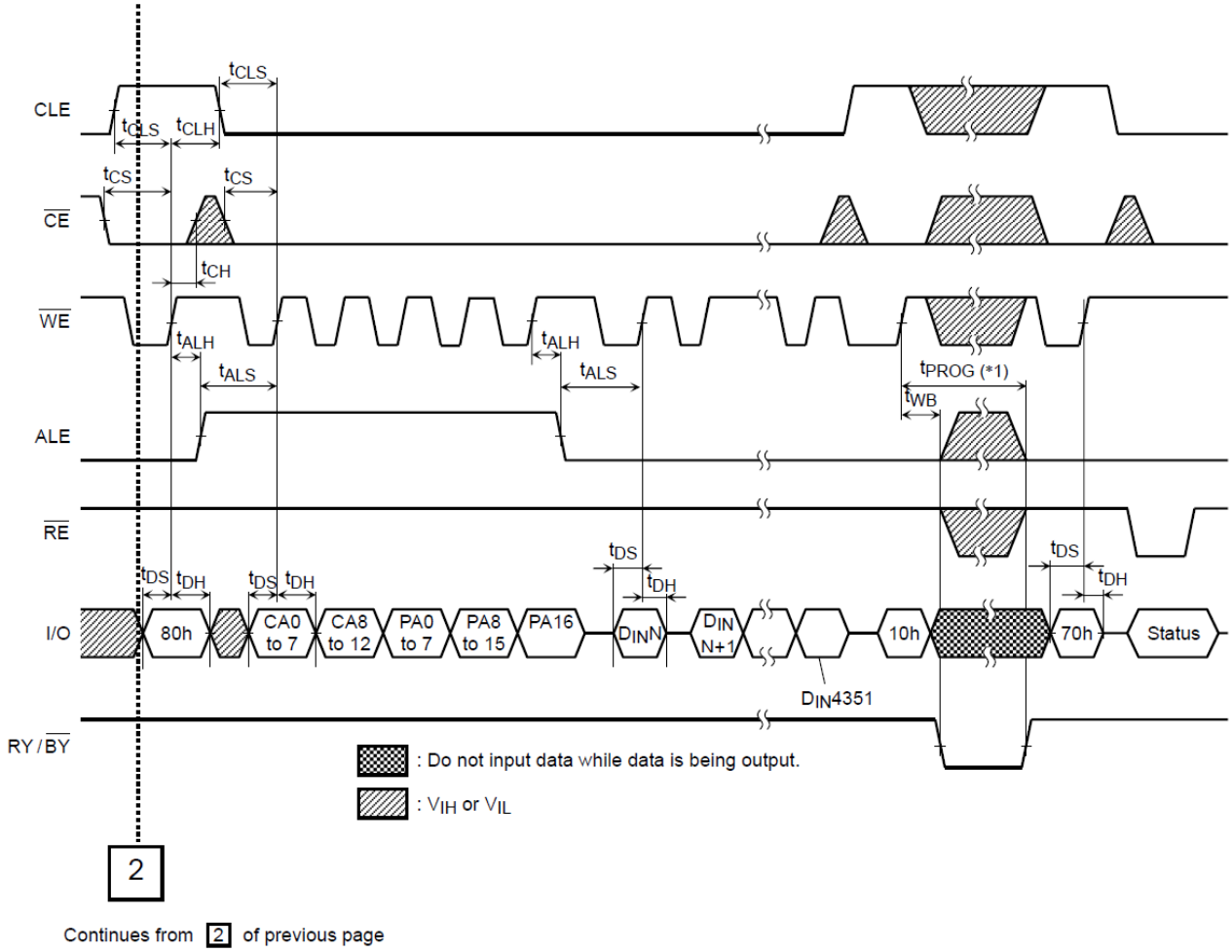


: Do not input data while data is being output.

: V_{IH} or V_{IL}

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Auto-Program Operation with Data Cache Timing Diagram (3/3)



(*1)

tPROG: Since the last page programming by 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following equation.

tPROG = tPROG of the last page + tPROG of the previous page − A

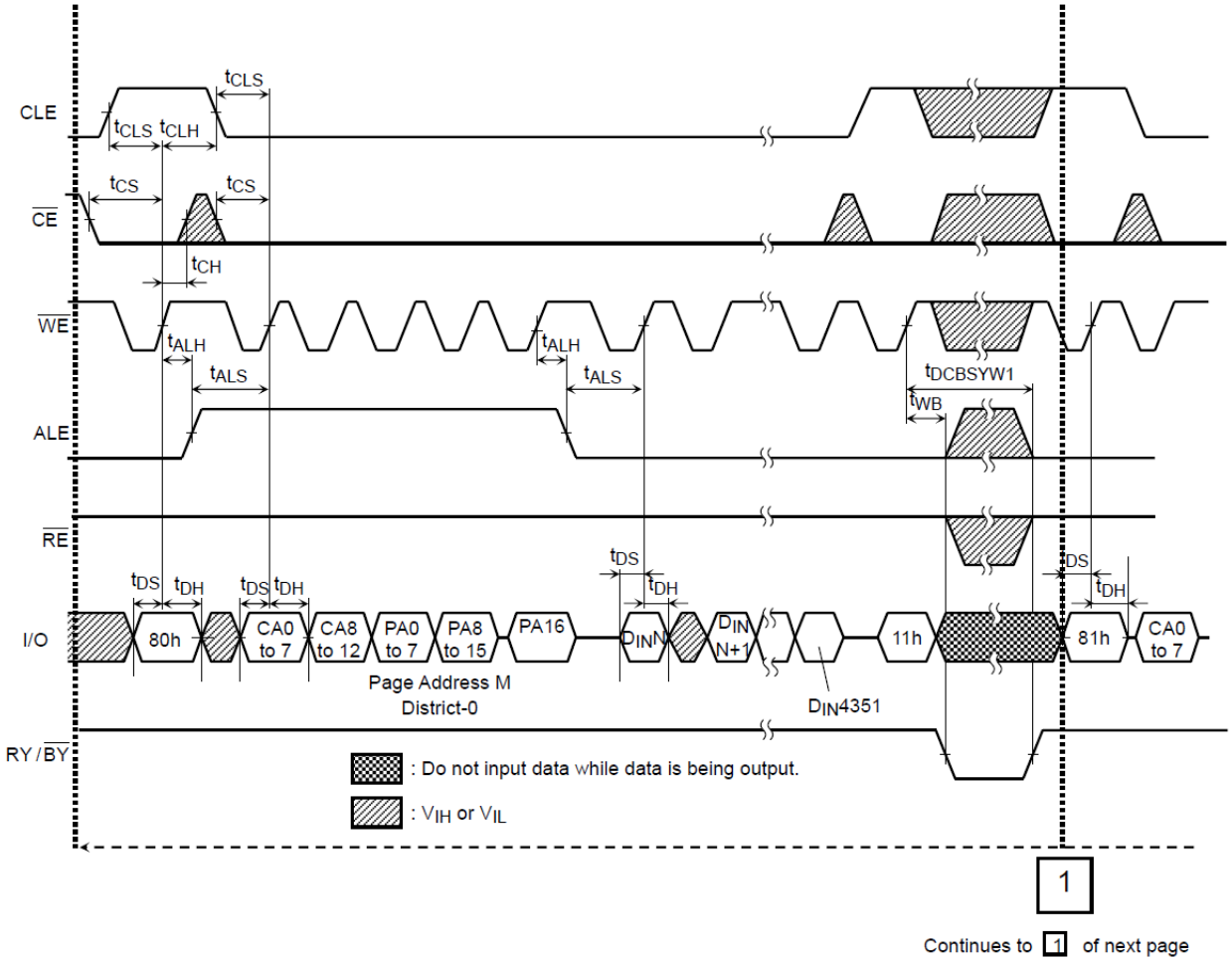
A = (command input cycle + address input cycle + data input cycle time of the last page)

If “A” exceeds the tPROG of previous page, tPROG of the last page is tPROG max.

NOTE : Make sure to terminate the operation with 80h-10h- command sequence.
If the operation is terminated by 80h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

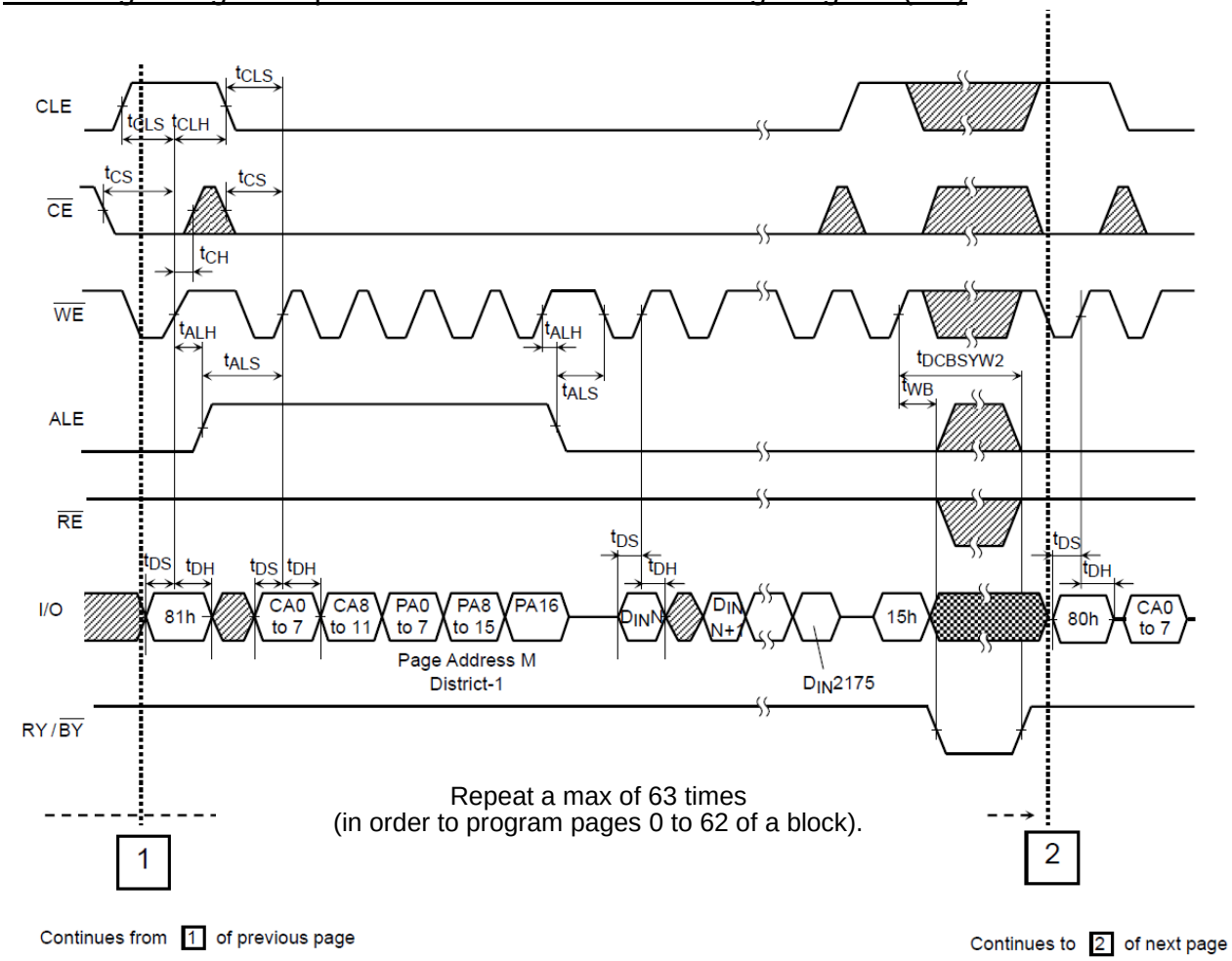
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Multi-Page Program Operation with Data Cache Timing Diagram (1/4)



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Multi-Page Program Operation with Data Cache Timing Diagram (2/4)

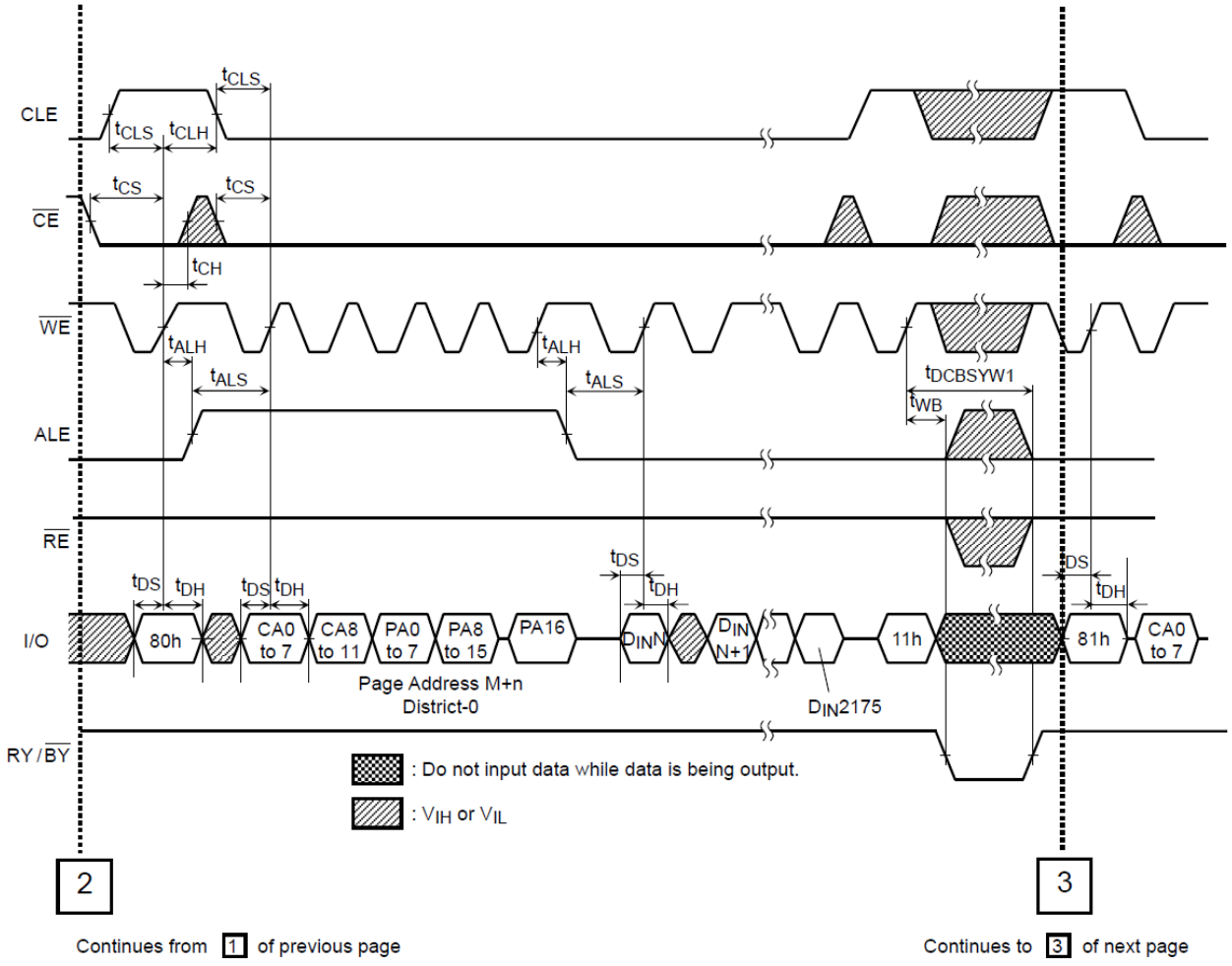


: Do not input data while data is being output.

: V_{IH} or V_{IL}

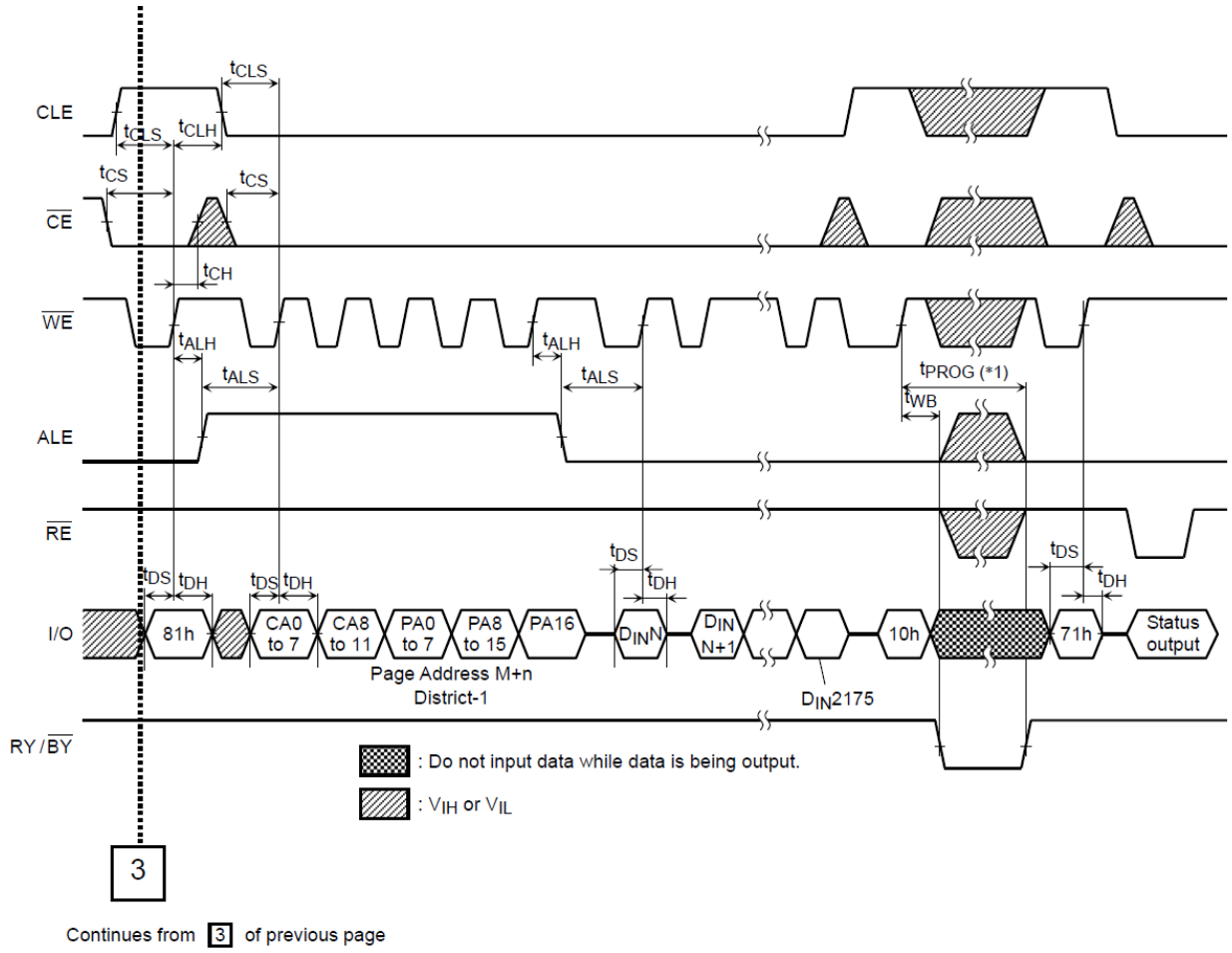
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Multi-Page Program Operation with Data Cache Timing Diagram (3/4)



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Multi-Page Program Operation with Data Cache Timing Diagram (4/4)



(*1)

tPROG: Since the last page programming by 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following equation.

tPROG = tPROG of the last page + tPROG of the previous page − A

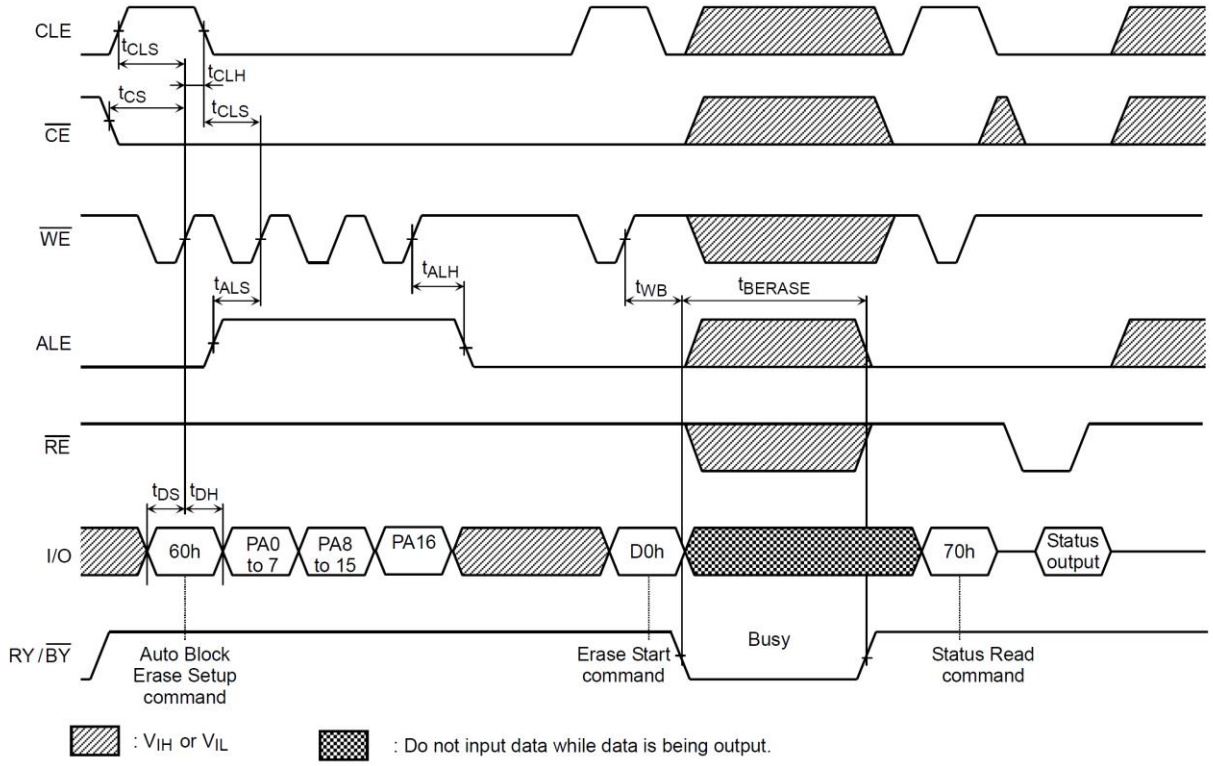
A = (command input cycle + address input cycle + data input cycle time of the last page)

If “A” exceeds the tPROG of previous page, tPROG of the last page is tPROG max.

NOTE : Make sure to terminate the operation with 81h-10h- command sequence.
If the operation is terminated by 81h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status
Read command (70h) and make sure the previous page program operation is completed.
If the page program operation is completed issue FFh reset before next operation.

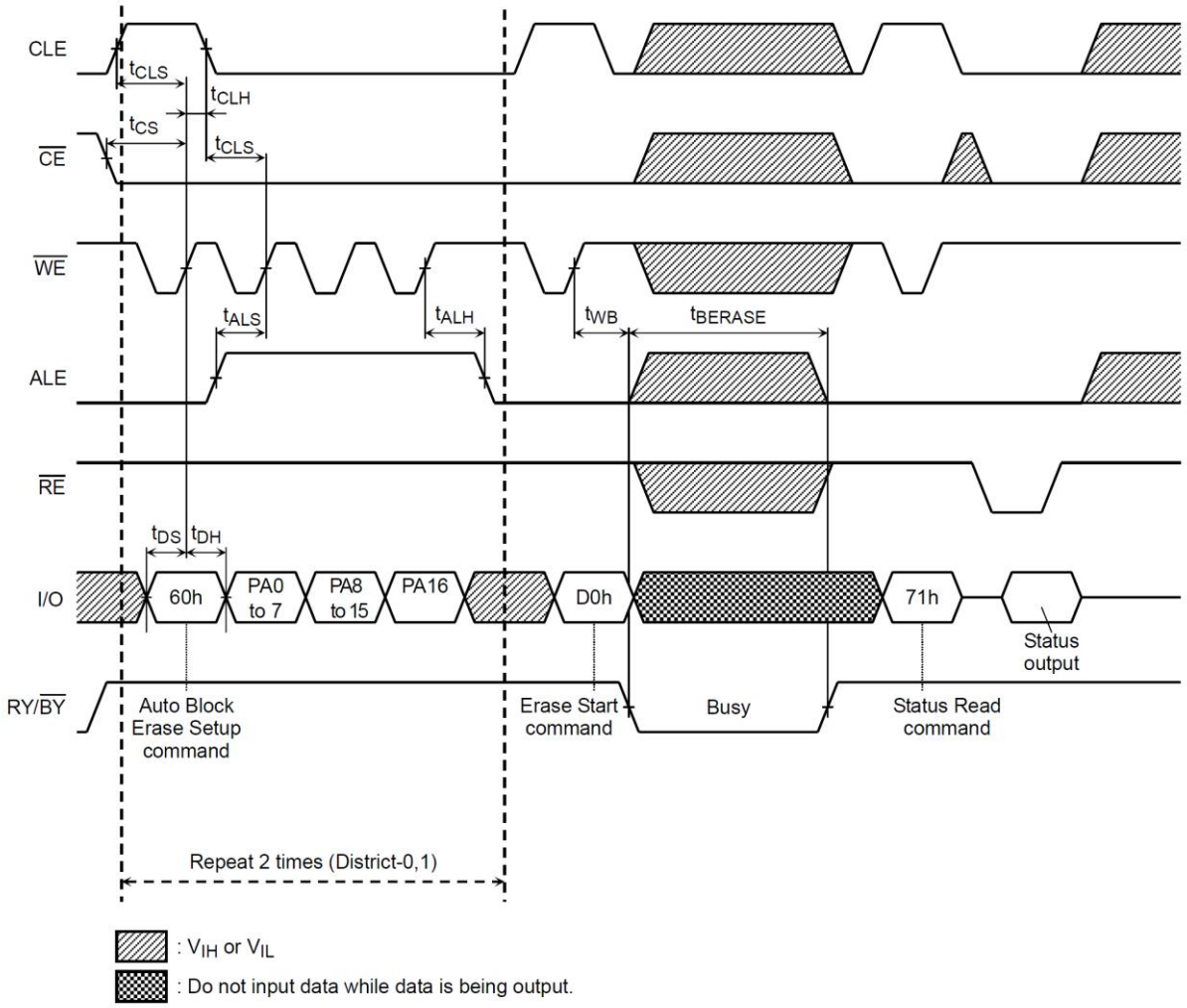
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Auto Block Erase Timing Diagram



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Multi Block Erase Timing Diagram



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ID Read Operation Timing Diagram

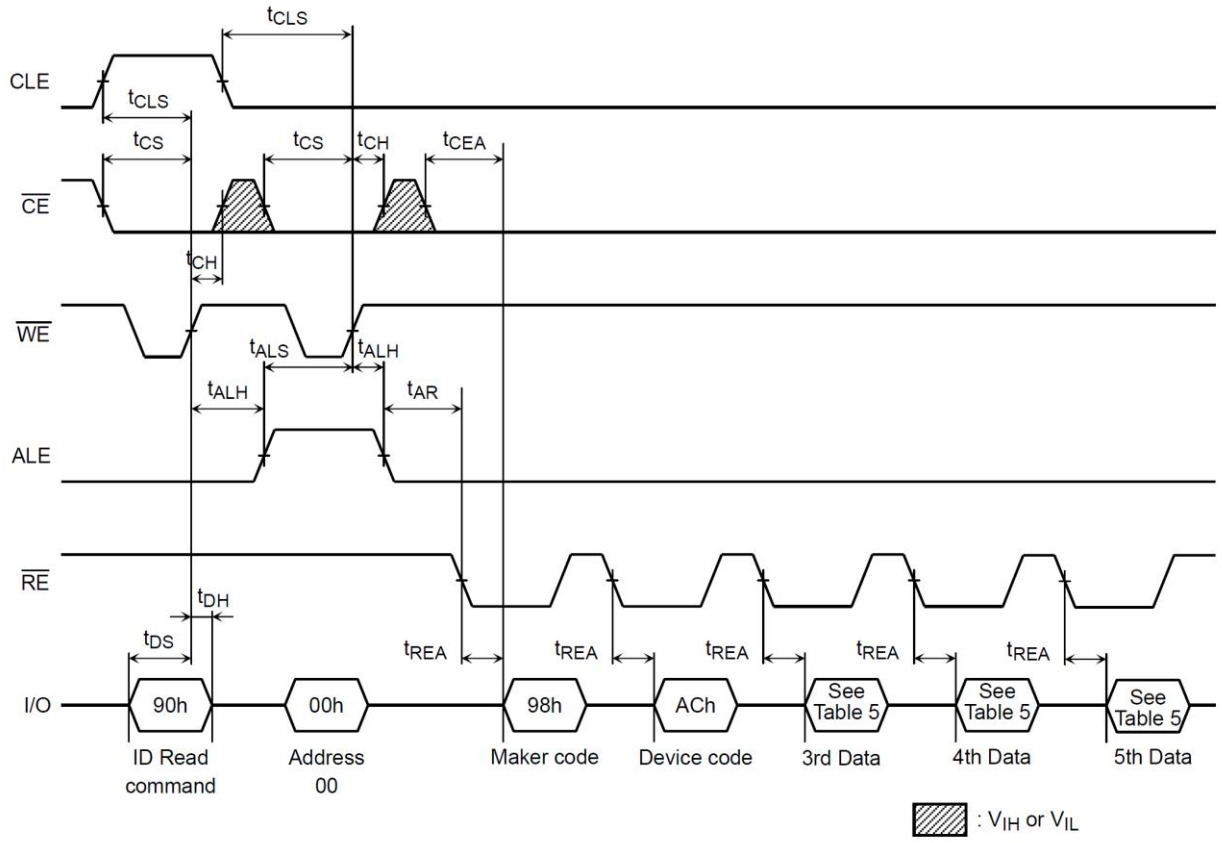


Table 5: ID Definition Table

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2Gb(X16/X32) LPDDR2

Nanya Technology Corp.
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LPDDR2 Descriptions

LPDDR2-S4 uses the double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

To achieve high-speed operation, our LPDDR2-S4 SDRAM uses the double data rate architecture and adopt 4n-prefetch interface designed to transfer two data per clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfer at the I/O pins. Read and write accesses to the LPDDR2-S4 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-S4 devices, accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Active command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

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Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD1}	Voltage on V_{DD1} pin relative to Vss	-0.4	2.3	V
V_{DD2}	Voltage on V_{DD2} pin relative to Vss	-0.4	1.6	V
V_{DDCA}	Voltage on V_{DDCA} pin relative to Vss	-0.4	1.6	V
V_{DDQ}	Voltage on V_{DDQ} pin relative to Vss	-0.4	1.6	V
Vin, Vout	Voltage on any pin relative to Vss	-0.4	1.6	V
Tstg	Storage Temperature (plastic)	-55	+125	°C

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For measurement conditions, refer to the JESD51-2 standard.
3. VDD2 and VDDQ / VDDCA must be within 200mV of each other at all times.
4. Voltage on any I/O may not exceed voltage on VDDQ; Voltage on any CA input may not exceed voltage on VDDCA.
5. VREF must always be less than all other supply voltages.
6. The voltage difference between any VSS pins may not exceed 100mV.

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AC/DC Operating Conditions

DC Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
Power Supply						
V_{DD1}	Core Supply voltage 1	1.70	1.80	1.95	V	
V_{DD2}	Core Supply voltage 2	1.14	1.20	1.30	V	
V_{DDCA}	Input Supply Voltage (Command / Address)	1.14	1.20	1.30	V	
V_{DDQ}	I/O Supply voltage (DQ)	1.14	1.20	1.30	V	
Leakage current						
I_I	Input leakage current Any input 0 ≦ V_{IN} ≦ V_{DDQ} / V_{DDCA}, All other pins not under test = 0V	-2	-	2	uA	1
I_{VREF}	V_{REF} leakage current; V_{REFDQ} = V_{DDQ}/2 or V_{REFCA} = V_{DDCA}/2 (all other pins not under test = 0V)	-1	-	1	uA	1

Notes:

1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.

   Although DM is for input only, the DM leakage shall match the DQ and DQS, $\overline{DQS}$ output leakage specification.

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AC/DC Input Measurement Level

AC and DC Logic Levels for Single-Ended Signals

CA inputs (Address and Command) and $\overline{CS}$ inputs					
Symbol	Parameter	LPDDR2 1066		Unit	Notes
		Min	Max		
$V_{IHCA(AC)}$	AC Input logic HIGH voltage	V_{REFCA} + 220 mV	-	mV	1,3
$V_{IHCA(DC)}$	DC Input logic HIGH voltage	V_{REFCA} + 130 mV	V_{DDCA}	mV	1
$V_{ILCA(AC)}$	AC Input logic LOW voltage	-	V_{REFCA} – 220 mV	mV	1,3
$V_{ILCA(DC)}$	DC Input logic LOW voltage	V_{SS}	V_{REFCA} – 130 mV	mV	1
$V_{REFCA(DC)}$	Reference voltage for CA and $\overline{CS}$ inputs	0.49 x V_{DDCA}	0.51 x V_{DDCA}	V	4,5
Data inputs (DQ & DM)					
$V_{IHDQ(AC)}$	AC Input logic HIGH voltage	V_{REFDQ} + 220 mV	-	mV	2,3
$V_{IHDQ(DC)}$	DC Input logic HIGH voltage	V_{REFDQ} + 130 mV	V_{DDQ}	mV	1
$V_{ILDQ(AC)}$	AC Input logic LOW voltage	-	V_{REFDQ} – 220 mV	mV	2,3
$V_{ILDQ(DC)}$	DC Input logic LOW voltage	V_{SS}	V_{REFDQ} – 130 mV	mV	1
$V_{REFDQ(DC)}$	Reference voltage for DQ and DM inputs	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	4,5
Clock enable inputs (CKE)					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
$V_{IHCKE\ (AC)}$	CKE AC Input HIGH voltage	0.8 * V_{DDCA}	-	V	3
$V_{ILCKE\ (AC)}$	CKE AC Input LOW voltage	-	0.2 * V_{DDCA}	V	3

NOTE 1 For CA and $\overline{CS}$ input only pins. Vref = VrefCA(DC).

NOTE 2 For DQ input only pins. Vref = VrefDQ(DC).

NOTE 3 See “Overshoot and Undershoot Specifications”

NOTE 4 The ac peak noise on VRefCA may not allow VRefCA to deviate from VRefCA(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).

NOTE 5 For reference: approx. VDDCA/2 +/- 12 mV.

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Differential AC and DC Input Levels

Differential Inputs logical levels (CK, $\overline{CK}$ – V_{REF} = $V_{REFCA(DC)}$; DQS, $\overline{DQS}$: V_{REF} = $V_{REFDQ(DC)}$)				
Symbol	Parameter	LPDDR2 1066		Unit
		Min	Max	
$V_{IHdiff(AC)}$	Differential input voltage HIGH AC	2 x ($V_{IH(AC)}$-V_{REF})	Note 3	V
$V_{ILdiff(AC)}$	Differential input voltage LOW AC	Note 3	2 x (V_{REF}-$V_{IL(AC)}$)	V
$V_{IHdiff(DC)}$	Differential input voltage HIGH DC	2 x ($V_{IH(DC)}$-V_{REF})	Note 3	V
$V_{ILdiff(DC)}$	Differential input voltage LOW DC	Note 3	2 x (V_{REF}-$V_{IL(DC)}$)	V

Notes:

1. Used to define a differential signal slew-rate. For CK – $\overline{CK}$ use VIH/VIL(dc) of CA and VREFCA; for DQS – $\overline{DQS}$, use VIH/VIL(dc) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
2. For CK and $\overline{CK}$, use $V_{IH/VIL(AC)}$ of CA and V_{REFCA}; for DQS and $\overline{DQS}$, use $V_{IH/VIL(AC)}$ of DQ and V_{REFDQ}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced voltage level also applies.
3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, and $\overline{DQS}$ must be within the respective limits ($V_{IH(DC)}$max, $V_{IL(DC)}$min) for single-ended signals and must comply with the specified limitations for overshoot and undershoot.

CK, $\overline{CK}$ and DQS, $\overline{DQS}$ Time Requirement before Ring back (t_{DVAC})

Slew Rate (V/ns)	t_{DVAC}(ps) at $V_{IH}/V_{ILdiff(AC)}$ = 440 mV
	Min
>4.0	175
4.0	170
3.0	167
2.0	163
1.8	162
1.6	161
1.4	159
1.2	155
1.0	150
<1.0	150

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Single-Ended Levels for CK, $\overline{CK}$, DQS, $\overline{DQS}$

Symbol	Parameter	LPDDR2 1066		Unit
		Min	Max	
$V_{SEH(AC)}$	Single-ended HIGH level for strobes	(V_{DDQ}/2) + 0.22	Note 3	V
	Single-ended HIGH level for CK, $\overline{CK}$	(V_{DDCA}/2) + 0.22	Note 3	V
$V_{SEL(AC)}$	Single-ended LOW level for strobes	Note 3	(V_{DDQ}/2) - 0.22	V
	Single-ended LOW level for CK, $\overline{CK}$	Note 3	(V_{DDCA}/2) - 0.22	V

Notes:

1. For CK and $\overline{CK}$, use V_{SEH}/$V_{SEL(AC)}$ of CA; for strobes (DQS[3:0] and $\overline{DQS}$[3:0]) use V_{IH}/$V_{IL(AC)}$ of DQ.
2. $V_{IH(AC)}$ and $V_{IL(AC)}$ for DQ are based on V_{REFDQ}; $V_{SEH(AC)}$ and $V_{SEL(AC)}$ for CA are based on V_{REFCA}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced level applies.
3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS0, $\overline{DQS0}$, DQS1, $\overline{DQS1}$, DQS2, $\overline{DQS2}$, DQS3, $\overline{DQS3}$ must be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals, and must comply with the specified limitations for overshoot and undershoot.

Cross-Point Voltage for Differential Input Signals (CK, $\overline{CK}$, DQS, $\overline{DQS}$)

Symbol	Parameter	LPDDR2 1066		Unit
		Min	Max	
$V_{IXCA(AC)}$	Differential input cross-point voltage relative to VDDCA/2 for CK and $\overline{CK}$	-120	+120	mV
$V_{IXDQ(AC)}$	Differential input cross-point voltage relative to VDDQ/2 for DQS and $\overline{DQS}$	-120	+120	mV

Notes:

1. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and it is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
2. For CK and $\overline{CK}$, V_{REF} = $V_{REFCA(DC)}$. For DQS and $\overline{DQS}$, V_{REF} = $V_{REFDQ(DC)}$.

Slew Rate Definitions for Single-Ended Input Signals

Refer to single-ended slew rate definition for address, command and data signals respectively.

Slew Rate Definitions for Differential Input Signals

Description	Defined by	Measured	
		From	To
Differential input slew rate for rising edge (CK, $\overline{CK}$ and DQS, $\overline{DQS}$)	[$V_{IHdiffmin}$ – $V_{ILdiffmax}$] / ΔTR_{diff}	$V_{ILdiffmax}$	$V_{IHdiffmin}$
Differential input slew rate for falling edge (CK, $\overline{CK}$ and DQS, $\overline{DQS}$)	[$V_{IHdiffmin}$ – $V_{ILdiffmax}$] / ΔTF_{diff}	$V_{IHdiffmin}$	$V_{ILdiffmax}$

Notes:

1. The differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must be linear between these thresholds.

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AC/DC Output Measurement Level

Single-Ended AC and DC Output Levels

Symbol	Parameter		LPDDR2 1066	Unit	Notes
$V_{OH(AC)}$	AC output HIGH measurement level (for output slew rate)		VREF + 0.12	V	
$V_{OL(AC)}$	AC output LOW measurement level (for output slew rate)		VREF – 0.12	V	
$V_{OH(DC)}$	DC output HIGH measurement level (for I-V curve linearity)		0.9 x VDDQ	V	1
$V_{OL(DC)}$	DC output LOW measurement level (for I-V curve linearity)		0.1 x VDDQ	V	2
I_{OZ}	Output leakage current (DQ, DM, DQS, $\overline{DQS}$) (DQ, DQS, $\overline{DQS}$ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	Min	-5	uA	
		Max	5	uA	
MMpupd	Delta output impedance between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	
Notes: 1. I_{OH} = –0.1mA 2. I_{OL} = 0.1mA					

Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2 1066	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output HIGH measurement level (for output SR)	+ 0.20 x VDDQ	V	1
$V_{OLdiff(AC)}$	AC differential output LOW measurement level (for output SR)	- 0.20 x VDDQ	V	2
Notes: 1. I_{OH} = –0.1mA 2. I_{OL} = 0.1mA				

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Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown below.

Single-Ended Output Slew Rate Definition

Description	Defined by	Measured	
		From	To
Single-ended output slew rate for rising edge	[$V_{OH(AC)}$ – $V_{OL(AC)}$] / ΔTR_{SE}	$V_{OL(AC)}$	$V_{OH(AC)}$
Single-ended output slew rate for falling edge	[$V_{OH(AC)}$ – $V_{OL(AC)}$] / ΔTF_{SE}	$V_{OH(AC)}$	$V_{OL(AC)}$
Notes: Output slew rate is verified by design and characterization, and may not be subject to production testing.			

Single-Ended Output Slew Rate

Symbol	Parameter	LPDDR2 1066		Unit
		Min	Max	
SRQ_{SE}	Single-ended output slew rate (output impedance = 40Ω ± 30%)	1.5	3.5	V/ns
SRQ_{SE}	Single-ended output slew rate (output impedance = 60Ω ± 30%)	1.0	2.5	V/ns
	Output slew-rate-matching ratio (pull-up to pull-down)	0.7	1.4	

Definitions:

SR = slew rate, Q = query output (similar to DQ = data-in, query-output), se = single-ended signals

NOTE 1 Measured with output reference load.

NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

NOTE 3 The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).

NOTE 4 Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

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Differential Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{Oldiff(AC)}$ and $V_{Ohdiff(AC)}$ for differential signals as shown below.

Differential Output Slew Rate Definition

Description	Defined by	Measured	
		From	To
Differential output slew rate for rising edge	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta TR_{diff}$	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$
Differential output slew rate for falling edge	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / \Delta TF_{diff}$	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$

Notes:

Output slew rate is verified by design and characterization, and may not be subject to production testing.

Differential Output Slew Rate

Symbol	Parameter	LPDDR2 1066		Unit
		Min	Max	
SRQ_{diff}	Differential output slew rate (output impedance = 40Ω ± 30%)	3.0	7.0	V/ns
SRQ_{diff}	Differential output slew rate (output impedance = 60Ω ± 30%)	2.0	5.0	V/ns

Definitions:

SR = slew rate, Q = query output (similar to DQ = data-in, query-output), diff = differential signals

NOTE 1 Measured with output reference load.

NOTE 2 The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).

NOTE 3 Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

AC Overshoot/Undershoot Specification

Parameter		1066	Unit
Maximum peak amplitude provided for overshoot area	Max	0.35	V
Maximum peak amplitude provided for undershoot area	Max	0.35	V
Maximum area above VDD	Max	0.15	V-ns
Maximum area below VSS	Max	0.15	V-ns

Notes:

1. VDD stands for VDDCA for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. VDD stands for VDDQ for DQ, DM, DQS, and $\overline{DQS}$.
2. VSS stands for VSS for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. VSS stands for VSS for DQ, DM, DQS, and $\overline{DQS}$.
3. Values are referenced from actual VDDQ, VDDCA and VSS levels.

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Input / Output Capacitance

T_{OPER}; V_{DDQ} = 1.14-1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V

Symbol	Parameter	LPDDR2 1066		Unit
		Min	Max	
C_{CK}	**Input capacitance :** CK, $\overline{CK}$	1	2	pF
C_{DCK}	**Input capacitance delta :** CK, $\overline{CK}$	0	0.2	pF
C_I	**Input capacitance:** all other input-only pins	1	2	pF
C_{DI}	**Input capacitance delta:** all other input-only pins	-0.4	0.4	pF
C_{IO}	**Input/output capacitance :** DQ, DQS, $\overline{DQS}$, DM	1.25	2.5	pF
C_{DDQS}	**Input/output capacitance delta :** DQS, $\overline{DQS}$	0	0.25	pF
C_{DIO}	**Input/output capacitance delta :** DQ, DM	-0.5	0.5	pF
C_{ZQ}	**Input/output capacitance :** ZQ	0	2.5	pF

Notes:

1. This parameter applies to die devices only (does not include package capacitance).
2. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with VDD1, VDD2, VDDQ and VSS applied; all other pins are left floating.
3. Absolute value of CCK - $\overline{CCK}$.
4. CI applies to $\overline{CS}$, CKE, and CA[9:0].
5. CDI = CI – 0.5 × (CCK + $\overline{CCK}$)
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP[3:0] = 0001B (34.3 ohm typical)
8. Absolute value of CDQS and $\overline{CDQS}$.
9. CDIO = CIO – 0.5 × (CDQS + $\overline{CDQS}$) in byte-lane.
10. Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR2 devices: 5pf.

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IDD Specifications

LPDDR2 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: **tCK = tCK(avg)min; tRC = tRCmin;** **CKE is HIGH;** **$\overline{CS}$ is HIGH between valid commands;** **CA bus inputs are SWITCHING;** **Data bus inputs are STABLE**	IDD01	VDD1	**1**
	IDD02	VDD2	**1**
	IDD0in	VDDCA,VDDQ	**1,4**
Idle power-down standby current: **tCK = tCK(avg)min;** **CKE is LOW;** **$\overline{CS}$ is HIGH;** **All banks/RBs idle;** **CA bus inputs are SWITCHING;** **Data bus inputs are STABLE**	IDD2P1	VDD1	**1**
	IDD2P2	VDD2	**1**
	IDD2P,in	VDDCA,VDDQ	**1,4**
Idle power-down standby current with clock stop: **CK =LOW, $\overline{CK}$ =HIGH;** **CKE is LOW;** **$\overline{CS}$ is HIGH;** **All banks/RBs idle;** **CA bus inputs are STABLE;** **Data bus inputs are STABLE**	IDD2PS1	VDD1	**1**
	IDD2PS2	VDD2	**1**
	IDD2PS,in	VDDCA,VDDQ	**1,4**
Idle non power-down standby current: **tCK = tCK(avg)min;** **CKE is HIGH;** **$\overline{CS}$ is HIGH;** **All banks/RBs idle;** **CA bus inputs are SWITCHING;** **Data bus inputs are STABLE**	IDD2N1	VDD1	**1**
	IDD2N2	VDD2	**1**
	IDD2N,in	VDDCA,VDDQ	**1,4**
Idle non power-down standby current with clock stop: **CK =LOW, $\overline{CK}$ =HIGH;** **CKE is HIGH;** **$\overline{CS}$ is HIGH;** **All banks/RBs idle;** **CA bus inputs are STABLE;** **Data bus inputs are STABLE**	IDD2NS1	VDD1	**1**
	IDD2NS2	VDD2	**1**
	IDD2NSIN	VDDCA,VDDQ	**1**
Active power-down standby current: **tCK = tCK(avg)min;** **CKE is LOW;** **$\overline{CS}$ is HIGH;** **One bank/RB active;** **CA bus inputs are SWITCHING;** **Data bus inputs are STABLE**	IDD3P1	VDD1	**1**
	IDD3P2	VDD2	**1**
	IDD3P,in	VDDCA,VDDQ	**1,4**

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Active power-down standby current with clock stop: **CK=LOW, $\overline{CK}$ =HIGH;** **CKE is LOW;** **$\overline{CS}$ is HIGH;** **One bank/RB active;** **CA bus inputs are STABLE;** **Data bus inputs are STABLE**	IDD3PS1	VDD1	**1**
	IDD3PS2	VDD2	**1**
	IDD3PS,in	VDDCA,VDDQ	**1,4**
Active non power-down standby current: **tCK = tCK(avg)min;** **CKE is HIGH;** **$\overline{CS}$ is HIGH;** **One bank/RB active;** **CA bus inputs are SWITCHING;** **Data bus inputs are STABLE**	IDD3N1	VDD1	**1**
	IDD3N2	VDD2	**1**
	IDD3N,in	VDDCA,VDDQ	**1,4**
Active non power-down standby current with clock stop: **CK=LOW, $\overline{CK}$ =HIGH;** **CKE is HIGH;** **$\overline{CS}$ is HIGH;** **One bank/RB active;** **CA bus inputs are STABLE;** **Data bus inputs are STABLE**	IDD3NS1	VDD1	**1**
	IDD3NS2	VDD2	**1**
	IDD3NS,in	VDDCA,VDDQ	**1,4**
Operating burst read current: **tCK = tCK(avg)min;** **$\overline{CS}$ is HIGH between valid commands;** **One bank/RB active;** **BL = 4; RL = RLmin;** **CA bus inputs are SWITCHING;** **50% data change each burst transf**	IDD4R1	VDD1	**1**
	IDD4R2	VDD2	**1**
	IDD4R,in	VDDCA	**1**
	IDD4RQ	VDDQ	**1,4**
Operating burst write current: **tCK = tCK(avg)min;** **$\overline{CS}$ is HIGH between valid commands;** **One bank/RB active;** **BL = 4; WL = WLmin;** **CA bus inputs are SWITCHING;** **50% data change each burst transfer**	IDD4W1	VDD1	**1**
	IDD4W2	VDD2	**1**
	IDD4W,in	VDDCA,VDDQ	**1,4**
All Bank Refresh Burst current: **tCK = tCK(avg)min;** **CKE is HIGH between valid commands;** **tRC = tRFCabmin;** **Burst refresh;** **CA bus inputs are SWITCHING;** **Data bus inputs are STABLE;**	IDD51	VDD1	**1**
	IDD52	VDD2	**1**
	IDD5IN	VDDCA,VDDQ	**1,4**
All Bank Refresh Average current: **tCK = tCK(avg)min;**	IDD5AB1	VDD1	**1**

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CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDD5AB2	VDD2	**1**
	IDD5AB,in	VDDCA,VDDQ	**1,4**
Per Bank Refresh Average current: tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	IDD5PB1	VDD1	**1,6**
	IDD5PB2	VDD2	**1,6**
	IDD5PB,in	VDDCA,VDDQ	**1,4,6**

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IDD Specifications (Continued)

LPDDR2 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Self refresh current (Standard Temperature Range): **CK=LOW, $\overline{CK}$=HIGH;** **CKE is LOW;** **CA bus inputs are STABLE;** **Data bus inputs are STABLE;** **Maximum 1x Self-Refresh Rate;**	IDD61	VDD1	**1,7**
	IDD62	VDD2	**1,7**
	IDD6IN	VDDCA,VDDQ	**1,4,7**
Deep Power-Down current: **CK=LOW, $\overline{CK}$=HIGH;** **CKE is LOW;** **CA bus inputs are STABLE;** **Data bus inputs are STABLE;**	IDD81	VDD1	**8**
	IDD82	VDD2	**8**
	IDD8IN	VDDCA,VDDQ	**4,8**

Notes:

1. Published IDD values are the maximum of the distribution of the arithmetic mean and are measured at 85℃.
2. IDD current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the extended temperature range.
4. Measured currents are the summation of VDDQ and VDDCA.
5. Guaranteed by design with output load of 5pf and RON = 40Ohm.
6. Per Bank Refresh only applicable for LPDDR2-S4 devices of 1Gb or higher densities
7. This is the general definition that applies to full-array SELF REFRESH.
8. IDD8 are typical values. IDD8 is measured at 25℃.

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IDD Specifications and Measurement Conditions

VDD2/VDDQ/VDDCA = 1.14~1.30V; VDD1 = 1.70~1.95V

Symbol		Supply	1066	Unit
			SDP	
IDD0	I_{DD01}	V_{DD1}	10	mA
	I_{DD02}	V_{DD2}	40	mA
	I_{DD0IN}	V_{DDCA}, V_{DDQ},	6	mA
IDD2P	I_{DD2P1}	V_{DD1}	450	uA
	I_{DD2P2}	V_{DD2}	600	uA
	I_{DD2PIN}	V_{DDCA}, V_{DDQ},	50	uA
IDD2PS	I_{DD2PS1}	V_{DD1}	450	uA
	I_{DD2PS2}	V_{DD2}	600	uA
	$I_{DD2PSIN}$	V_{DDCA}, V_{DDQ},	50	uA
IDD2N	I_{DD2N1}	V_{DD1}	1	mA
	I_{DD2N2}	V_{DD2}	15	mA
	I_{DD2NIN}	V_{DDCA}, V_{DDQ},	6	mA
IDD2NS	I_{DD2NS1}	V_{DD1}	1	mA
	I_{DD2NS2}	V_{DD2}	5	mA
	$I_{DD2NSIN}$	V_{DDCA}, V_{DDQ},	6	mA
IDD3P	I_{DD3P1}	V_{DD1}	1200	uA
	I_{DD3P2}	V_{DD2}	4	mA
	I_{DD3PIN}	V_{DDCA}, V_{DDQ},	100	uA
IDD3PS	I_{DD3PS1}	V_{DD1}	1200	uA
	I_{DD3PS2}	V_{DD2}	4	mA
	$I_{DD3PSIN}$	V_{DDCA}, V_{DDQ},	100	uA
IDD3N	I_{DD3N1}	V_{DD1}	1.2	mA
	I_{DD3N2}	V_{DD2}	20	mA
	I_{DD3NIN}	V_{DDCA}, V_{DDQ},	6	mA
IDD3NS	I_{DD3NS1}	V_{DD1}	1.2	mA
	I_{DD3NS2}	V_{DD2}	7	mA
	$I_{DD3NSIN}$	V_{DDCA}, V_{DDQ},	6	mA

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Symbol		Supply	1066 SDP	Unit
IDD4R	I_{DD4R1}	V_{DD1}	2	mA
	I_{DD4R2}	V_{DD2}	200	mA
	I_{DD4RIN}	V_{DDCA}	6	mA
	I_{DD4RQ}	V_{DDQ}	240	mA
IDD4W	I_{DD4W1}	V_{DD1}	2	mA
	I_{DD4W2}	V_{DD2}	150	mA
	I_{DD4WIN}	V_{DDCA}, $V_{DDQ,}$	25	mA
IDD5	I_{DD51}	V_{DD1}	15	mA
	I_{DD52}	V_{DD2}	110	mA
	I_{DD5IN}	V_{DDCA}, $V_{DDQ,}$	6	mA
IDD5AB	I_{DD5AB1}	V_{DD1}	3	mA
	I_{DD5AB2}	V_{DD2}	20	mA
	$I_{DD5ABIN}$	V_{DDCA}, $V_{DDQ,}$	6	mA
IDD5PB	I_{DD5PB1}	V_{DD1}	3	mA
	I_{DD5PB2}	V_{DD2}	20	mA
	$I_{DD5PBIN}$	V_{DDCA}, $V_{DDQ,}$	6	mA
IDD8	I_{DD81}	V_{DD1}	7.5	uA
	I_{DD82}	V_{DD2}	40	uA
	I_{DD8IN}	V_{DDCA}, $V_{DDQ,}$	10	uA

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IDD Specifications and Measurement Conditions

VDD2/VDDQ = 1.14~1.30V; VDD1 = 1.70~1.95V

IDD6 Partial Array Self-refresh current;

PASR	Supply	1066	Unit
		SDP	
Full Array	V_{DD1}	700	uA
	V_{DD2}	2000	uA
	V_{DDQ}	50	uA
1/2 Array	V_{DD1}	650	uA
	V_{DD2}	1600	uA
	V_{DDQ}	50	uA
1/4 Array	V_{DD1}	600	uA
	V_{DD2}	1400	uA
	V_{DDQ}	50	uA
1/8 Array	V_{DD1}	550	uA
	V_{DD2}	1300	uA
	V_{DDQ}	50	uA

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LPDDR2-S4 Refresh Requirement Parameters

Symbol	Parameter	2Gb(SDP)	Unit
	Number of banks	8	
tREFW	Refresh window: TCASE ≤ 85°	32	ms
R	Required number of REFRESH commands (MIN)	8192	
tREFI	Average time between REFRESH commands	3.9	us
tREFIpb	TCASE ≤ 85°C	0.4875	us
tRFCab	Refresh cycle time	130	ns
tRFCpb	Per-bank REFRESH cycle time	60	ns
tREFBW	Burst REFRESH window = 4 × 8 × tRFCab	4.16	us

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Electrical Characteristics and Recommended AC Timing

V_{DD2},V_{DDQ},V_{DDCA} = 1.14~1.30V; V_{DD1} = 1.70~1.95V

Parameter	Symbol	min/ max	1066	Unit
Clock Timing				
Max. Frequency		~	533	MHz
Average Clock Period	**tCK(avg)**	min	1.875	ns
		max	100	ns
Average high pulse width	**tCH(avg)**	min	0.45	tCK(avg)
		max	0.55	tCK(avg)
Average low pulse width	**tCL(avg)**	min	0.45	tCK(avg)
		max	0.55	tCK(avg)
Absolute Clock Period	**tCK(abs)**	min	tCK(avg)min + tJIT(per),min	ps
Absolute clock HIGH pulse width (with allowed jitter)	**tCH(abs), allowed**	min	0.43	tCK(avg)
		max	0.57	tCK(avg)
Absolute clock LOW pulse width (with allowed jitter)	**tCL(abs), allowed**	min	0.43	tCK(avg)
		max	0.57	tCK(avg)
Parameter	**Symbol**	**min/ max**	**1066**	**Unit**
Clock Period Jitter (with allowed jitter)	**tJIT(per), allowed**	min	-90	ps
		max	90	ps
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	**tJIT(cc), allowed**	max	180	ps
Duty cycle Jitter (with allowed jitter)	**tJIT(duty), allowed**	min	min((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) * tCK(avg)	ps
		max	max((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) * tCK(avg)	ps
Cumulative error across 2 cycles	**tERR(2per),**	min	-132	ps
	allowed	max	132	ps
Cumulative error across 3 cycles	**tERR(3per),**	min	-157	ps
	allowed	max	157	ps
Cumulative error across 4 cycles	**tERR(4per),**	min	-175	ps
	allowed	max	175	ps

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Parameter	Symbol	min/ max	1066	Unit
Cumulative error across 5 cycles	**tERR(5per),**	min	-188	ps
	allowed	max	188	ps
Cumulative error across 6 cycles	**tERR(6per),**	min	-200	ps
	allowed	max	200	ps
Cumulative error across 7 cycles	**tERR(7per),**	min	-209	ps
	allowed	max	209	ps
Cumulative error across 8 cycles	**tERR(8per),**	min	-217	ps
	allowed	max	217	ps
Cumulative error across 9 cycles	**tERR(9per),**	min	-224	ps
	allowed	max	224	ps
Cumulative error across 10 cycles	**tERR(10per),**	min	-231	ps
	allowed	max	231	ps
Cumulative error across 11 cycles	**tERR(11per),**	min	-237	ps
	allowed	max	237	ps
Cumulative error across 12 cycles	**tERR(12per),**	min	-242	ps
	allowed	max	242	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	**tERR(nper),**	min	**t**ERR(nper), allowed, min = (1 + 0.68ln(n)) * **t**JIT(per), allowed, min	ps
	allowed	max	**t**ERR(nper), allowed, max = (1 + 0.68ln(n)) * **t**JIT(per), allowed, max	ps

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Electrical Characteristics and Recommended AC Timing

V_{DD2},V_{DDQ},V_{DDCA} = 1.14~1.30V; V_{DD1} = 1.70~1.95V

Symbol	Parameter	min/ max	min ^{t}CK	Speed Grade 1066	Unit
ZQ calibration parameters					
tZQINIT	Calibration initialization Time	min		1	us
tZQCL	Long (Full) Calibration Time	min	6	360	ns
tZQCS	Short Calibration Time	min	6	90	ns
tZQRESET	Calibration Reset Time	min	3	50	ns
Read parameters					
tDQSCK	DQS output access time from CK, $\overline{CK}$	min		2500	ps
		max		5500	ps
tDQSCKDS	DQSCK Delta Short	max		330	ps
tDQSCKDM	DQSCK Delta Medium	max		680	ps
tDQSCKDL	DQSCK Delta Long	max		920	ps
tDQSQ	DQS-DQ skew, DQS to last DQ valid, per group, per access	max		200	ps
tQHS	Data Hold Skew Factor	max		230	ps
tQSH	DQS output HIGH pulse width	min		tCH(abs) - 0.05	tCK(avg)
tQSL	DQS output LOW pulse width	min		tCL(abs) - 0.05	tCK(avg)
tQHP	Data half period	min		min(tQSH, tQSL)	tCK(avg)
tQH	DQ / DQS output hold time from DQS	min		tQHP - tQHS	ps
Symbol	**Parameter**	**min/ max**	**min ^{t}CK**	**Speed Grade 1066**	**Unit**
Read parameters					
tRPRE	READ Preamble	min		0.9	tCK(avg)
tRPST	READ Postamble	min		tCL(abs) - 0.05	tCK(avg)
tLZ(DQS)	DQS Low-Z from CK	min		$tDQSCK_{min}$ – 300	ps
tLZ(DQ)	DQ Low-Z from CK	min		tDQSCK(MIN) – (1.4 × tQHS(MAX))	ps
tHZ(DQS)	DQS High-Z from CK	max		$tDQSCK_{max}$ – 100	ps
tHZ(DQ)	DQ High-Z from CK	max		tDQSCK(MAX) + (1.4 × tDQSQ(MAX))	ps

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Symbol	Parameter	min/ max	min ^{t}CK	Speed Grade 1066	Unit
Write parameters					
tDH	DQ and DM input hold time (V_{REF} based)	min		210	ps
tDS	DQ and DM input setup time (V_{REF} based)	min		210	ps
tDIPW	DQ and DM input pulse width	min		0.35	tCK(avg)
tDQSS	Write command to 1st DQS latching transition	min		0.75	tCK(avg)
		max		1.25	tCK(avg)
tDQSH	DQS input high-level width	min		0.4	tCK(avg)
tDQSL	DQS input low-level width	min		0.4	tCK(avg)
tDSS	DQS falling edge to CK setup time	min		0.2	tCK(avg)
tDSH	DQS falling edge hold time from CK	min		0.2	tCK(avg)
tWPST	Write postamble	min		0.4	tCK(avg)
tWPRE	Write preamble	min		0.35	tCK(avg)
Symbol	**Parameter**	**min/ max**	**min ^{t}CK**	**Speed Grade 1066**	**Unit**
CKE input parameters					
tCKE	CKE min. pulse width (high and low)	min	3	3	tCK(avg)
tISCKE	CKE input setup time	min		0.25	tCK(avg)
tIHCKE	CKE input hold time	min		0.25	tCK(avg)
Command / Address Input parameters					
tIH	Address and Control input hold time	min		220	ps
tIS	Address and Control input setup time	min		220	ps
tIPW	Address and Control input pulse width	min		0.4	tCK(avg)
Mode register parameters					
tMRR	MODE Register Read command period	min	2	2	tCK(avg)
tMRW	MODE Register Write command period	min	5	5	tCK(avg)
SDRAM core parameters					
RL	Read Latency	min	3	8	tCK(avg)
WL	Write Latency	min	1	4	tCK(avg)
tCKESR	CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	min	3	15	ns
tXSR	Exit SELF REFRESH to first valid command (min)	min	2	$tRFC_{AB}$ +10	ns

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Symbol	Parameter	min/ max	min tCK	Speed Grade 1066	Unit
SDRAM core parameters					
tXP	Exit power-down mode to first valid command	min	2	7.5	ns
tDPD	Minimum Deep Power-Down time	min	-	500	us
tFAW	Four-Bank Activate Window	min	8	50	ns
tWTR	Internal WRITE to READ command delay	min	2	7.5	ns
tRC	ACTIVE to ACTIVE command period	min		tRAS + tRP_{AB} (with all-bank Precharge) tRAS + tRP_{PB} (with per-bank Precharge)	ns
tCCD	CAS-to-CAS delay	min	2	2	tCK(avg)
tRTP	Internal READ to PRECHARGE command delay	min	2	7.5	ns
tRCD	RAS-to-CAS delay	min	3	18	ns
tRAS	Row Active Time	min	3	42	ns
		max	-	70	us
tWR	Write recovery time	min	3	15	ns
tRPpb	PRECHARGE command period (single bank)	min	3	15	ns
tRPab	PRECHARGE command period (all banks – 8bank)	min	3	18	ns
tRRD	ACTIVE *bank-a* to ACTIVE *bank-b* command	min	2	10	ns

Symbol	Parameter	min/ max	min tCK	Speed Grade 1066	Unit
Boot parameters (10MHz ~ 55MHz)					
tCKb	Clock cycle time	min		18	ns
		max		100	ns
tISCKEb	CKE input setup time	min		2.5	ns
tIHCKEb	CKE input hold time	min		2.5	ns
tISb	Input setup time	min		1150	ps

Symbol	Parameter	min/ max	min tCK	Speed Grade 1066	Unit
Boot parameters (10MHz ~ 55MHz)					
tIHb	Input hold time	min		1150	ps
tDQSCKb	Access window of DQS from CK, $\overline{CK}$	min		2.0	ns
		max		10.0	ns
tDQSQb	DQS-DQ skew	max		1.2	ns
tQHSb	Data hold skew factor	max		1.2	ns

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Electrical Characteristics and Recommended AC Timing

(800Mbps and lower than 800Mbps)

V_{DD2}, V_{DDQ} = 1.14~1.30V; V_{DD1} = 1.70~1.95V

Symbol	Parameter	min/ max	Speed Grade 800	Unit
ZQ calibration parameters				
tZQINIT	Calibration initialization Time	min	1	us
tZQCL	Long (Full) Calibration Time	min	360	ns
tZQCS	Short Calibration Time	min	90	ns
tZQRESET	Calibration Reset Time	min	50	ns
Read parameters				
tDQSCK	DQS output access time from CK, $\overline{CK}$	min	2500	ps
		max	5500	ps
tDQSCKDS	DQSCK Delta Short	max	330	ps
tDQSCKDM	DQSCK Delta Medium	max	680	ps
tDQSCKDL	DQSCK Delta Long	max	920	ps
tDQSQ	DQS-DQ skew, DQS to last DQ valid, per group, per access	max	200	ps
tQHS	Data Hold Skew Factor	max	230	ps
tQSH	DQS output HIGH pulse width	min	tCH(abs) - 0.05	tCK(avg)
tQSL	DQS output LOW pulse width	min	tCL(abs) - 0.05	tCK(avg)
tQHP	Data half period	min	min(tQSH, tQSL)	tCK(avg)
tQH	DQ / DQS output hold time from DQS	min	tQHP - tQHS	ps
Symbol	**Parameter**	**min/ max**	**Speed Grade 800**	**Unit**
Read parameters				
tRPRE	READ Preamble	min	0.9	tCK(avg)
tRPST	READ Postamble	min	tCL(abs) - 0.05	tCK(avg)
tLZ(DQS)	DQS Low-Z from CK	min	$tDQSCK_{min}$ – 300	ps
tLZ(DQ)	DQ Low-Z from CK	min	tDQSCK(MIN) – (1.4 × tQHS(MAX))	ps
tHZ(DQS)	DQS High-Z from CK	max	$tDQSCK_{max}$ – 100	ps
tHZ(DQ)	DQ High-Z from CK	max	tDQSCK(MAX) + (1.4 × tDQSQ(MAX))	ps

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Symbol	Parameter	min/ max	Speed Grade 800	Unit
Write parameters				
tDH	DQ and DM input hold time (V_{REF} based)	min	210	ps
tDS	DQ and DM input setup time (V_{REF} based)	min	210	ps
tDIPW	DQ and DM input pulse width	min	0.35	tCK(avg)
tDQSS	Write command to 1st DQS latching transition	min	0.75	tCK(avg)
		max	1.25	tCK(avg)
tDQSH	DQS input high-level width	min	0.4	tCK(avg)
tDQSL	DQS input low-level width	min	0.4	tCK(avg)
tDSS	DQS falling edge to CK setup time	min	0.2	tCK(avg)
tDSH	DQS falling edge hold time from CK	min	0.2	tCK(avg)
tWPST	Write postamble	min	0.4	tCK(avg)
tWPRE	Write preamble	min	0.35	tCK(avg)
Symbol	**Parameter**	**min/ max**	**Speed Grade 800**	**Unit**
CKE input parameters				
tCKE	CKE min. pulse width (high and low)	min	3	tCK(avg)
tISCKE	CKE input setup time	min	0.25	tCK(avg)
tIHCKE	CKE input hold time	min	0.25	tCK(avg)
Command / Address Input parameters				
tIH	Address and Control input hold time	min	220	ps
tIS	Address and Control input setup time	min	220	ps
tIPW	Address and Control input pulse width	min	0.4	tCK(avg)
Mode register parameters				
tMRR	MODE Register Read command period	min	2	tCK(avg)
tMRW	MODE Register Write command period	min	5	tCK(avg)
SDRAM core parameters				
RL	Read Latency	min	8	tCK(avg)
WL	Write Latency	min	4	tCK(avg)
tCKESR	CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	min	6	tCK(avg)
tXSR	Exit SELF REFRESH to first valid command (min)	min	$tRFC_{AB}$ +10	ns

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Symbol	Parameter	min/ max	Speed Grade 800	Unit
SDRAM core parameters				
tXP	Exit power-down mode to first valid command	min	3	tCK(avg)
tDPD	Minimum Deep Power-Down time	min	500	us
tFAW	Four-Bank Activate Window	min	20	tCK(avg)
tWTR	Internal WRITE to READ command delay	min	3	tCK(avg)
tRC	ACTIVE to ACTIVE command period	min	tRAS + tRPAB (with all-bank Precharge) tRAS + tRPPB (with per-bank Precharge)	ns
tCCD	CAS-to-CAS delay	min	2	tCK(avg)
tRTP	Internal READ to PRECHARGE command delay	min	3	tCK(avg)
tRCD	RAS-to-CAS delay	min	8	tCK(avg)
tRAS	Row Active Time	min	17	tCK(avg)
		max	70	us
tWR	Write recovery time	min	6	tCK(avg)
tRPpb	PRECHARGE command period (single bank)	min	8	tCK(avg)
tRPab	PRECHARGE command period (all banks – 8bank)	min	9	tCK(avg)
tRRD	ACTIVE *bank-a* to ACTIVE *bank-b* command	min	4	tCK(avg)

Symbol	Parameter	min/ max	Speed Grade 800	Unit
Temperature Derating				
tDQSCK (derated)	tDQSCK derating	max	5620	ps
tRCD (derated)	Core timing temperature derating	min	tRCD + 1.875	ns
tRC (derated)		min	tRC + 1.875	ns
tRAS (derated)		min	tRAS + 1.875	ns
tRP (derated)		min	tRP + 1.875	ns
tRRD (derated)		min	tRRD + 1.875	ns
Boot parameters (10MHz ~ 55MHz)				
tCKb	Clock cycle time	min	18	ns
		max	100	ns
tISCKEb	CKE input setup time	min	2.5	ns
tIHCKEb	CKE input hold time	min	2.5	ns
tISb	Input setup time	min	1150	ps

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Symbol	Parameter	min/ max	Speed Grade	Unit
			800	
Boot parameters (10MHz ~ 55MHz)				
tIHb	Input hold time	min	1150	ps
tDQSCKb	Access window of DQS from CK, $\overline{CK}$	min	2.0	ns
		max	10.0	ns
tDQSQb	DQS-DQ skew	max	1.2	ns
tQHSb	Data hold skew factor	max	1.2	ns

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CA and $\overline{CS}$ Setup and Hold Base Values

Parameter	Data Rate	Reference
	1066	
tIS (base)	0	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 220$ mV
tIH (base)	90	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 130$ mV

Notes: AC/DC referenced for 1 V/ns CA and $\overline{CS}$ slew rate and 2 V/ns differential CK, $\overline{CK}$ slew rate.

CA and $\overline{CS}$ Setup, Hold, and Derating (Continued)

Derating Values for AC/DC-based tIS/tIH (AC220, DC130)

AC220 DC130 Threshold																	
		CK, $\overline{CK}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA,$\overline{CS}$ Slew rate V/ns	2	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Notes: Cell contents shaded in yellow are defined as “not supported.”

Required time tVAC above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate (V/ns)	tVAC @ 220mV [ps]	
	Min	Max
>2.0	175	–
2.0	170	–
1.5	167	–
1.0	163	–
0.9	162	–
0.8	161	–
0.7	159	–
0.6	155	–
0.5	150	–
<0.5	150	–

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Data Setup and Hold Base Values

Parameter	Data Rate	Reference
	1066	
tDS (base)	-10	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 220$ mV
tDH (base)	80	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 130$ mV

Notes: AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS, $\overline{DQS}$ slew rate.

Derating Values for AC/DC-based tDS/tDH (AC220, DC130)

AC220 DC130 Threshold																	
		DQS, $\overline{DQS}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
DQ,DM Slew rate V/ns	2	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Notes: Cell contents shaded in light purple are defined as “not supported.”

Required time tVAC above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate (V/ns)	tVAC @ 220mV [ps]	
	Min	Max
>2.0	175	–
2.0	170	–
1.5	167	–
1.0	163	–
0.9	162	–
0.8	161	–
0.7	159	–
0.6	155	–
0.5	150	–
<0.5	150	–

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Initialization Timing Parameters

Symbol	Parameter	Value		Unit
		min	max	
^{t}INIT0	Maximum Power Ramp Time	-	20	ms
^{t}INIT1	Minimum CKE low time after completion of power ramp	100	-	ns
^{t}INIT2	Minimum stable clock before first CKE high	5	-	^{t}CK
^{t}INIT3	Minimum idle time after first CKE assertion	200	-	us
^{t}INIT4	Minimum idle time after Reset command, this time will be about 2 x ^{t}RFCab + ^{t}RPab	1	-	us
^{t}INIT5	Maximum duration of Device Auto-Initialization	-	10	us
^{t}ZQINIT	ZQ Initial Calibration	1	-	us
^{t}CKb	Clock cycle time during boot	18	100	ns

Power-Off Timing

Symbol	Parameter	Min	Max	Unit
tPOFF	Maximum power-off ramp time	-	2	s

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Mode Register Assignment

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info	R	(RFU)			RZQI		(RFU)	DI	DAI
1	01_H	Device Feature1	W	nWR (for AP)			WC	BT	BL		
2	02_H	Device Feature2	W	(RFU)					RL & WL		
3	03_H	I/O Config-1	W	(RFU)					DS		
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density			Type		
9	09_H	Test Mode	W	Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11~15	$0B_H$~$0F_H$	(Reserved)		(RFU)							
16	10_H	PASR_BANK	W	Bank Mask (4-Bank or 8-Bank)							
17	11_H	PASR_Seg	W	Segment Mask							
18-19	12_H-13_H	(Reserved)		(RFU)							
20-31	18_H-$1F_H$	Reserved for NVM									
32	20_H	DQ calibration pattern A	R	See “Data Calibration Pattern Description”							
33-39	21_H-27_H	(Do Not Use)									
40	28_H	DQ calibration pattern B	R	See “Data Calibration Pattern Description”							
41-47	29_H-$2F_H$	(Do Not Use)		(DNU)							
48-62	30_H-$3E_H$	(Reserved)		(RFU)							
63	$3F_H$	Reset	W	X							
64-126	40_H-$7E_H$	(Reserved)		(RFU)							
127	$7F_H$	(Do Not Use)		(DNU)							
128-190	80_H-BE_H	(Reserved)		(RFU)							
191	BF_H	(Do Not Use)		(DNU)							
192-254	$C0_H$-FE_H	(Reserved)		(RFU)							
255	FF_H	(Do Not Use)		(DNU)							

Notes:

1. RFU bits shall be set to “0” during Mode Register writes. RFU bits shall be read as “0” during Mode Register reads. All Mode Registers that are specified as RFU shall not be written. Writes to read-only registers shall have no impact on the functionality of the device.
2. All Mode Registers from that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.

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MR0_Device Information (MA<7:0> = 00H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	**00_H**	Device Info	R	(RFU)			**RZQI** (Optional)		(RFU)	**DI**	**DAI**

OP0	**DAI (Device Auto-Initialization Status)**	Read-only	0_B: DAI complete 1_B: DAI still in progress
OP1	**DI (Device Information)**	Read-only	0_B: S2 or S4 SDRAM 1_B: Do Not Use
OP<4:3>	**RZQI (Built in Self Test for RZQ Information)**	Read-only	00_B: RZQ self test not supported 01_B: ZQ-pin may connect to VDDCA or float 10_B: ZQ-pin may short to GND 11_B:ZQ-pin self test completed, no error condition detected (ZQpin may not connect to VDDCA or float nor short to GND)

Notes:

1. RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.

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MR1_Device Feature 1 (MA<7:0> = 01_H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
1	01_H	Device Feature1	W	nWR (for AP)			WC	BT	BL		

OP<2:0>	**BL (Burst Length)**	Write-only	010_B: BL4 (default) 011_B: BL8 100_B: BL16 All others: reserved
OP3	**BT[1] (Burst Type)**	Write-only	0_B: Sequential (default) 1_B: Interleaved
OP4	**WC (Wrap)**	Write-only	0_B: Wrap (default) 1_B: No wrap (allowed for SDRAM BL4 only)
OP<7:5>	**nWR[2] (for AP)**	Write-only	001_B: nWR=3 (default) 010_B: nWR =4 011_B: nWR =5 100_B: nWR =6 101_B: nWR =7 110_B: nWR =8 All others: reserved

Notes:

1. BL16, interleaved is not an official combination to be supported.
2. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU($^tWR/^tCK$).

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Burst Sequence by BL, BT, WC and column address

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BL4																						
x	x	0_B	0_B	wrap	any	4	0	1	2	3												
x	x	1_B	0_B				2	3	0	1												
x	x	x	0_B	nw	any		y	y+1	y+2	y+3												
BL8																						
x	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
x	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
x	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
x	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
x	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
x	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
x	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
x	1_B	1_B	0_B				6	7	4	5	2	3	0	1								
x	x	x	0_B	nw	any		illegal (not allowed)															

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BL16																						
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
x	x	x	0_B		int		illegal (not allowed)															
x	x	x	0_B	nw	any		illegal (not allowed)															

Notes:

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1~C0.
3. For BL=8, the burst address represents C2~C0.
4. For BL=16, the burst address represents C3~C0.
5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary. The variable *y* can start at any address with C0 equal to 0, but must not start at any address shown bellow.

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Non-Wrap Restrictions

Width	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/8Gb
Cannot cross full page boundary				
X16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
X32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
Cannot cross sub-page boundary				
X16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
X32	none	none	None	none

Notes: Non-wrap BL= 4 data orders shown are prohibited.

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MR2_Device Feature 2 (MA<7:0> = 02H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
2	02_H	Device Feature2	W	(RFU)				RL & WL			

OP<3:0>	**RL & WL (Read Latency & Write Latency)**	Write-only	0001_B: RL3 / WL1 (default) 0010_B: RL4 / WL2 0011_B: RL5 / WL2 0100_B: RL6 / WL3 0101_B: RL7 / WL4 0110_B: RL8 / WL4 All others: reserved

MR3_I/O Configuration 1 (MA<7:0> = 03H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
3	03_H	I/O Config-1	W	(RFU)				DS			

OP<3:0>	**DS (Drive Strength)**	Write-only	0000_B: reserved 0001_B: 34.3 ohm typical 0010_B: 40.0 ohm typical (default) 0011_B: 48.0 ohm typical 0100_B: 60.0 ohm typical 0101_B: reserved 0110_B: 80.0 ohm typical 0111_B: 120.0 ohm typical All others: reserved

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MR4_Device Temperature (MA<7:0> = 04H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		

OP<2:0>	**Refresh Rate**	Read-only	000_B: 4x tREFI, 4x tREFIpb, 4x tREFW 001_B: 4x tREFI, 4x tREFIpb, 4x tREFW 010_B: 2x tREFI, 2x tREFIpb, 2x tREFW 011_B: 1x tREFI, 1x tREFIpb, 1x tREFW (<=85C) 100_B: RFU 101_B: 0.25x tREFI, 0.25x tREFIpb, 0.25x tREFW, do not de-rate SDRAM AC timing 110_B: 0.25x tREFI, 0.25x tREFIpb, 0.25x tREFW, de-rate SDRAM AC timing 111_B: SDRAM High temperature operating limit exceeded
OP7	**TUF** **(Temperature Update Flag)**	Read-only	0_B: OP<2:0> value has not changed since last read of MR4. 1_B: OP<2:0> value has changed since last read of MR4.

Notes:

1. A Mode Register Read from MR4 will reset OP7 to “0”.
2. OP7 is reset to “0” at power-up.
3. If OP2 equals “1”, the device temperature is greater than 85C.
4. OP7 is set to “1”, if OP2~OP0 has changed at any time since the last read of MR4.
5. While OP[2:0]=111B, please confirm with NTC.
6. For specified operating temperature range and maximum operating temperature.
7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: tRCD, tRC, tRAS, tRP and tRRD. The tDQSCK parameter must be derated. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
8. The recommended frequency for reading MR4 is provided in “Temperature Sensor”.

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MR5_Basic Configuration-1 (MA<7:0> = 05H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
5	**05_H**	Basic Config-1	R	**Manufacturer ID**							

OP<7:0>	**Manufacturer ID**	Read-only	$0000\ 0000_B$: Reserved $0000\ 0001_B$: Samsung $0000\ 0010_B$: Qimonda $0000\ 0011_B$: Elpida $0000\ 0100_B$: Etron **$0000\ 0101_B$: Nanya** $0000\ 0110_B$: Hynix $0000\ 0111_B$: Mosel $0000\ 1000_B$: Winbond $0000\ 1001_B$: ESMT $0000\ 1010_B$: Reserved $0000\ 1011_B$: Spansion $0000\ 1100_B$: SST $0000\ 1101_B$: ZMOS $0000\ 1110_B$: Intel $1111\ 1110_B$: Numonyx $1111\ 1111_B$: Micron All Others : Reserved

MR6_Basic Configuration-2 (MA<7:0> = 06H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
6	**06_H**	Basic Config-2	R	**Revision ID1**							

OP<7:0>	**Revision ID1**	Read-only	Reserved [1]

Notes:

1. Please contact with NTC for details

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MR7_Basic Configuration-3 (MA<7:0> = 07H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
7	07_H	Basic Config-3	R	Revision ID2							

OP<7:0>	**Revision ID2**	Read-only	Reserved [1]

Notes:

1. Please contact with NTC for details

MR8_Basic Configuration-4 (MA<7:0> = 08H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
8	08_H	Basic Config-4	R	I/O width		Density				Type	

OP<1:0>	**Type**	Read-only	00_B: S4 SDRAM 01_B: S2 SDRAM 10_B: N NVM 11_B: Reserved
OP<5:2>	**Density**	Read-only	0000_B: 64Mb 0001_B: 128Mb 0010_B: 256Mb 0011_B: 512Mb 0100_B: 1Gb 0101_B: 2Gb 0110_B: 4Gb 0111_B: 8Gb 1000_B: 16Gb 1001_B: 32Gb All others: reserved
OP<7:6>	**I/O width**	Read-only	00_B: x32 01_B: x16 10_B: x8 11_B: not used

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MR9_Test Mode (MA<7:0> = 09H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
9	09_H	Test Mode	W	Specific Test Mode							

OP<7:0>	Specific Test Mode	Reserved [1]

Notes:

1. Please contact with NTC for details

MR10_Calibration (MA<7:0> = 0AH)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
10	$0A_H$	IO Calibration	W	Calibration Code							

OP<7:0>	**Calibration Code**	Write-only	0Xff: Calibration command after initialization 0Xab: Long calibration 0x56: Short calibration 0Xc3: ZQ Reset All others: Reserved

Notes:

1. Host processor shall not write MR10 with “Reserved” values.
2. LPDDR2 devices shall ignore calibration command, when a “Reserved” values is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSS through RZQ, either the ZQ calibration function (see “MRW ZQ Calibration Command”) or default calibration (through the ZQ RESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device. Devices that do not support calibration ignore the ZQ calibration command.

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MR11:15_(Reserved) (MA<7:0> = 0BH- 0FH)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
11~15	$0B_H$~$0F_H$	(reserved)		(RFU)							

OP<7:0>	**RFU**	Reserved for Future Use

MR16_PASR_Bank Mask (MA<7:0> = 010H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10_H	PASR_BANK	W	**Bank Mask (4-Bank or 8-Bank)**							

OP<7:0>	**Bank Mask (4-Bank or 8-Bank)**	Write-only	0_B: refresh enable to the bank (=unmasked, default) 1_B: refresh blocked (=masked)

For 4-bank S4 SDRAM, only OP<3:0> are used.

OP	Bank Mask	4 Bank	8 Bank
0	XXXXXXX1	Bank 0	Bank 0
1	XXXXXX1X	Bank 1	Bank 1
2	XXXXX1XX	Bank 2	Bank 2
3	XXXX1XXX	Bank 3	Bank 3
4	XXX1XXXX	-	Bank 4
5	XX1XXXXX	-	Bank 5
6	X1XXXXXX	-	Bank 6
7	1XXXXXXX	-	Bank 7

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MR17_PASR_Segment Mask (MA<7:0> = 11_H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
17	11_H	PASR_Seg	W	Segment Mask							

OP<7:0>	**Segment Mask**	Write-only	0_B: refresh enable to the segment (=unmasked, default) 1_B: refresh blocked (=masked)

This table indicates the range of row addresses in each masked segment. X is don't care for a particular segment.

Segment	OP	Bank Mask	1Gb	2Gb, 4Gb	8Gb
			R12:10	R13:11	R14:12
0	0	XXXXXXX1	000_B		
1	1	XXXXXX1X	001_B		
2	2	XXXXX1XX	010_B		
3	3	XXXX1XXX	011_B		
4	4	XXX1XXXX	100_B		
5	5	XX1XXXXX	101_B		
6	6	X1XXXXXX	110_B		
7	7	1XXXXXXX	111_B		

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MR18:19_(Reserved) (MA<7:0> = 012H- 013H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
18-19	12_H-13_H	(Reserved)		(RFU)							

OP<7:0>	**RFU**	Reserved for Future Use

MR20:31_(Do Not Use) (MA<7:0> = 014H- 01FH)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
20-31	18_H-$1F_H$	Reserved for NVM									

OP<7:0>	**Reserved for NVM**	N/A

MR32_ DQ calibration pattern A (MA<7:0> = 020H)

MR40_ DQ calibration pattern B (MA<7:0> = 028H)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	20_H	DQ calibration pattern A	R	See “Data Calibration Pattern Description”							
40	28_H	DQ calibration pattern B	R	See “Data Calibration Pattern Description”							

OP<7:0>	**DQ calibration pattern A**	See “Data Calibration Pattern Description”
OP<7:0>	**DQ calibration pattern B**	See “Data Calibration Pattern Description”

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MR63_Reset (MA<7:0> = 03FH): MRW only

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
63	3FH	Reset	W	X							

OP<7:0>	**Reset**	X (For additional information on MRW RESET, see “Mode Register Write Command” on Timing Spec)

Do Not Use and Reserved functions

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
17	11H	(reserved)		(RFU)							
33-39	21_H-27_H	(Do Not Use)		(DNU)							
41-47	29H-2FH	(Do Not Use)		(DNU)							
48-62	30H-3EH	(Reserved)		(RFU)							
64-126	40H-7EH	(Reserved)		(RFU)							
127	7FH	(Do Not Use)		(DNU)							
128-190	80H-BEH	(Reserved)		(RFU)							
191	BFH	(Do Not Use)		(DNU)							
192-254	C0H-FEH	(Reserved)		(RFU)							
255	FFH	(Do Not Use)		(DNU)							

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Revision History

Rev	Page	Modified	Description	Released
1.3	-	-	Official Release	09/2016
1.4	P5,7	Ball Assignment	Modify J10:VDDQ (was:VDD)	12/2016
1.5	P22-44	Device Operation	New	04/2018
	P48-59	-	Add Application notes	
1.6	P57,58	-	Correct typo	05/2018
1.7	-	-	Remove NM14F2KSLAXCL-3B	08/2021
1.8	P15,52	-	Add NOTE	02/2022
1.9	P107	MR4	Add 000B, Revise NOTE 5 for 111B	04/2022
2.0	P98-101	Electrical Characteristics and Recommended AC Timing	Add 800Mbps	02/2024
2.1	P4	Features	Add wording, “Non-use 5PBTs of TSCA”	03/2024
	P4,55	Endurance Test Guideline	New application notes	

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