NCA1051

High-speed CAN Transceiver

Datasheet (EN) 1.3

Product Overview

The NCA1051 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The NCA1051 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The NCA1051 provides thermal protection and transmit data dominant time out function.

These features make the NCA1051 an excellent choice for all types of HS-CAN networks, in nodes that do not require a silent mode with wake-up capability via the bus.

Key Features

- Fully compatible with the ISO11898-2 standard
- Ideal passive behavior to the CAN bus when the supply voltage is off
- NCA1051 can be interfaced directly to micro controllers with supply voltage from 3V to 5V
- Bus fault protection of -70V to +70V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Data rate: up to 5Mbps
- Low loop delay: <250ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:

  SOP8

Applications

- 5Mbps operation in highly loaded CAN networks down to 10 kbps networks using TXD DTO
- Industrial automation, control, sensors, and drive systems
- Building, security, and climate control automation
- CAN bus standards such as CANopen、DeviceNet、NMEA2000、ARNIC825、ISO11783 and CANaerospace

Device Information

Part Number	Package	Body Size
NCA1051-DSPR	SOP8	4.90mm × 3.90mm
NCA1051N-DSPR	SOP8	4.90mm × 3.90mm

Functional Block Diagrams

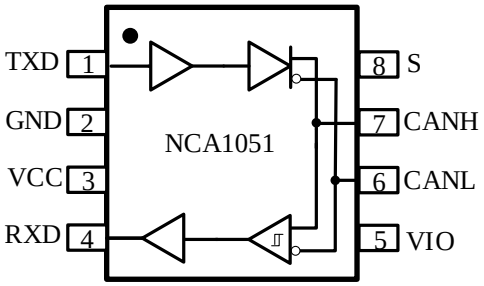


Figure 1. NCA1051 Block Diagram

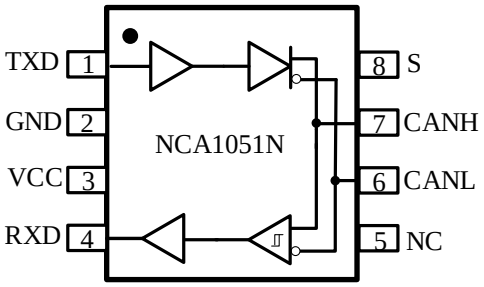


Figure 2. NCA1051N Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS 3

2. ABSOLUTE MAXIMUM RATINGS 4

3. RECOMMENDED OPERATING CONDITIONS 4

4. THERMAL CHARACTERISTICS 5

5. SPECIFICATIONS 6

5.1. ELECTRICAL CHARACTERISTICS 6
5.2. SWITCHING ELECTRICAL CHARACTERISTICS 8
5.3. PARAMETER MEASUREMENT INFORMATION 9

6. FUNCTION DESCRIPTION 13

6.1. OVERVIEW 13
6.2. DEVICE FUNCTIONAL MODES 13
6.3. NORMAL MODE 14
6.4. SILENT MODE 14
6.5. TXD DOMINANT TIME-OUT FUNCTION 14
6.6. CURRENT PROTECTION 14
6.7. OVER TEMPERATURE PROTECTION 14
6.8. VIO OUTPUT SUPPLY 14

7. APPLICATION NOTE 15

7.1. TYPICAL APPLICATION 15

8. PACKAGE INFORMATION 16

9. ORDER INFORMATION 18

10. DOCUMENTATION SUPPORT 18

11. TAPE AND REEL INFORMATION 19

12. REVISION HISTORY 20

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1. Pin Configuration and Functions

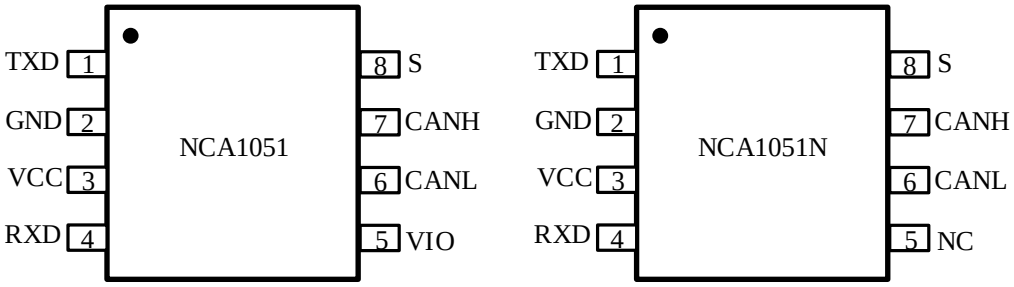


Figure 1.1 NCA1051, NCA1051N Package

Table1.1 NCA1051, NCA1051N Pin Configuration and Description

NCA1051-DSPR PIN NO.	*NCA1051N-DSPR PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	2	GND	Ground
3	3	VCC	Power Supply
4	4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	\	VIO	Logic I/O supply voltage
\	5	NC	Not connected, VIO is equal to VCC in NCA1051N
6	6	CANL	Low-level CAN bus line
7	7	CANH	High-level CAN bus line
8	8	S	S (silent mode) select pin (active high)

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2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit	Comments
Power Supply Voltage	VCC, VIO	-0.3	7	V	
Logic I/O Voltage	TXD, RXD, S	-0.3	7	V	
Differential input voltage	V_{ID}	-27	27	V	
Maximum BUS Pin Voltage	V_{CANH}, V_{CANL}	-70	+70	V	
Operating Temperature	Topr	-40	125	℃	
Junction Temperature	Tj	-40	150	℃	
Storage Temperature	Tstg	-65	150	℃	
System level Electro-Static Discharge	ESD		±5	kV	IEC61000-4-2: Powered contact discharge: CAN bus terminals to GND
	HBM		±8	kV	All pins
	CDM		±2	kV	All pins

3. Recommended Operating Conditions

Parameters	Symbol	min	max	unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
	V_{IO}	3	5.5	V
Differential input voltage	V_{ID}	-3	8	V
CAN bus terminal HIGH level output current	$I_{OH(CAN)}$	-50		mA
CAN bus terminal LOW level output current	$I_{OL(CAN)}$		50	mA
RXD terminal HIGH level output current	$I_{OH(RXD)}$	-2		mA
RXD terminal LOW level output current	$I_{OL(RXD)}$		2	mA

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4. Thermal Characteristics

Parameters	*Symbol*	*SOP8*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	145	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	50	℃/W
Junction-to-board thermal resistance	θ_{JB}	45	℃/W

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5. Specifications

5.1.Electrical Characteristics

(V_{CC}=4.5V~5.5V,V_{IO}=3V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VCC=5V, VIO=3.3V,Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Voltage	V_{CC}	4.5		5.5	V	
undervoltage detection voltage on pin VCC	$V_{uvd(VCC)}$	3.5		4.5	V	
supply voltage on pin VIO	V_{IO}	3		5.5	V	
undervoltage detection voltage on pin VIO	$V_{uvd(VIO)}$	1.5		2.7		
supply current	I_{CC}		45	70	mA	Normal mode, dominant, TXD=0, S=0, R_L=60Ω
			1.7	5	mA	Normal mode, recessive, TXD=V_{IO}, S=0
				2.5	mA	Silent mode, S=V_{IO}, TXD=V_{IO}
supply current on pin VIO	I_{IO}		550	900	uA	Normal mode, dominant, V_{TXD}=0V
				300	uA	Normal/Silent mode, recessive, V_{TXD}=V_{IO}
Thermal-Shutdown Threshold	T_{TS}	155	165	180	℃	
Logic Side[1]						
High level input voltage	V_{IH}	0.7*V_{IO}			V	TXD &S pin
Low level input voltage	V_{IL}			0.3*V_{IO}	V	
High level input current	I_{IH}	-5		5	uA	TXD pin
		1		10	uA	S pin
Low level input current	I_{IL}	-200		-30	uA	TXD pin
		-1		1	uA	S pin
Output High Voltage	V_{OH}	V_{IO}-0.5			V	RXD, I_O=-2mA
Output Low Voltage	V_{OL}			0.4	V	RXD, I_O=2mA
Input Capacitance	C_{IN}		5		pF	TXD pin
Driver						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.8	3.44	4.5	V	S=0, TXD=0V, R_{Load} =60Ω

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Parameters	Symbol	Min	Typ	Max	Unit	Comments
CANL output voltage (Dominant)	$V_{OL(D)}$	0.5	1.33	2.25	V	S=0, TXD=0V, R_{Load} =60Ω
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	0.5*VCC	3	V	TXD=V_{IO}; recessive
		-0.1		0.1	V	Standby mode, no load
Differential output voltage (Dominant)	$V_{OD(D)}$	1.5		3	V	VCC=5V, TXD=0, R_{Load} =60Ω, see Figure 5.1
Differential output voltage (Recessive)	$V_{OD(R)}$	-0.05		0.05	V	VCC=5V, TXD=VIO, R_{Load} =60Ω, see Figure 5.1
		-0.1		0.1	V	VCC=5V, TXD=VIO, NO Load, see Figure 5.1
Dominant short-circuit output current	$I_{O(sc)dom}$	-100		-40	mA	TXD=0V, t < $t_{to(dom)TXD}$, V_{CANH}=-30V
		40		100	mA	TXD=0V, t < $t_{to(dom)TXD}$, V_{CANL}=30V
Recessive short-circuit output current	$I_{O(sc)rec}$	-5		5	mA	Normal/Silent mode; V_{TXD} = V_{IO}; V_{CANH} = V_{CANL} = -27 V to +30 V
Receiver						
Positive-going bus input threshold voltage	V_{IT+}		750	900	mV	$V_{COM(CAN)}$=0V
Negative-going bus input threshold voltage	V_{IT-}	500	650		mV	$V_{COM(CAN)}$=0V
Hysteresis voltage	V_{HYS}		100		mV	
Power-off (unpowered) bus input leakage current	$I_{IOFF(LKG)}$	-5		5	uA	V_{CANH} / V_{CANL} = 5 V, VCC = 0V, VIO= 0 V
Input capacitance to ground	C_I		13		pF	CANH or CANL
Differential input	C_{ID}		5		pF	
Differential input resistance	R_{ID}	30		80	kΩ	
Input resistance	R_{IN}	15	30	40	kΩ	
Input resistance matching	R_{Imatch}	-3		+3	%	CANH=CANL
Common-mode voltage range	V_{COM}	-30		+30	V	

1) VIO is equal to VCC in NCA1051N.

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5.2.Switching Electrical Characteristics

(V_{CC}=4.5V~5.5V,V_{IO}=3V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VCC=5V, VIO=3.3V,Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Loop delay1	T_{loop1}		90	220	ns	Driver input to receiver output, Recessive to Dominant, see Figure 5.7
Loop delay2	T_{loop2}		100	220	ns	Driver input to receiver output, Dominant to Recessive, see Figure 5.7
transmitted recessive bit width	$t_{bit(bus)}$	435		530	ns	$t_{bit(TXD)}$ = 500 ns
		155		210	ns	$t_{bit(TXD)}$ = 200 ns
bit time on pin RXD	$t_{bit(RXD)}$	400		550	ns	$t_{bit(TXD)}$ = 500 ns
		120		220	ns	$t_{bit(TXD)}$ = 200 ns
Driver						
Propagation delay time from TXD to bus dominant	t_{PLH}		65	140	ns	Normal mode, see Figure 5.4
Propagation delay time from TXD to bus recessive	t_{PHL}		65	140	ns	Normal mode, see Figure 5.4
Differential output signal rise time	t_r		21		ns	see Figure 5.4
Differential output signal fall time	t_f		46		ns	see Figure 5.4
Bus dominant time-out time	t_{TXD_DTO}	800	2200	4500	us	see Figure 5.8
Receiver						
Propagation delay time from bus dominant to RXD	t_{PLH}		39	100	ns	see Figure 5.6
Propagation delay time from bus recessive to RXD	t_{PHL}		20	100	ns	see Figure 5.6
RXD signal rise time	t_r		10		ns	see Figure 5.6
RXD signal fall time	t_f		5		ns	see Figure 5.6

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5.3.Parameter Measurement Information

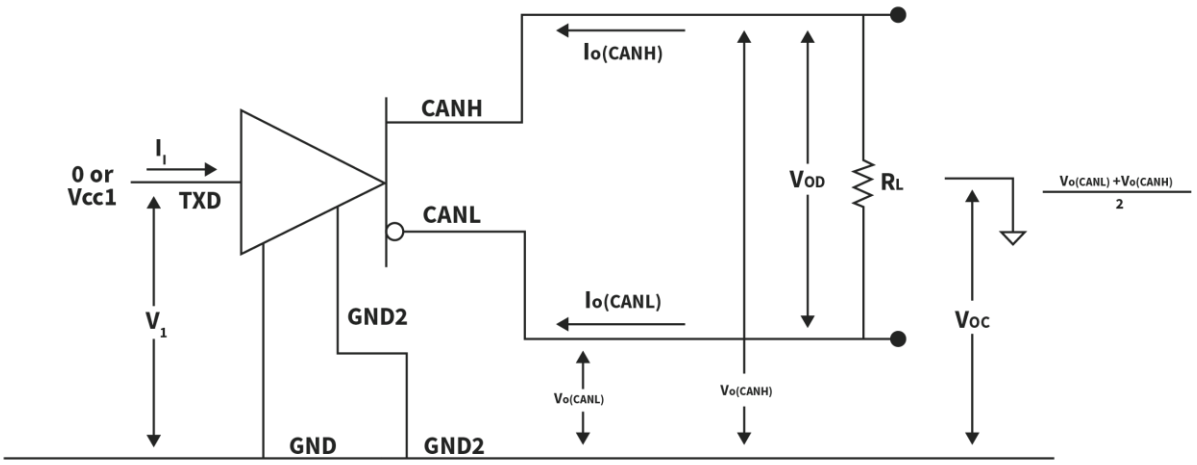


Figure 5.1. Driver Voltage, Current and Test Definitions

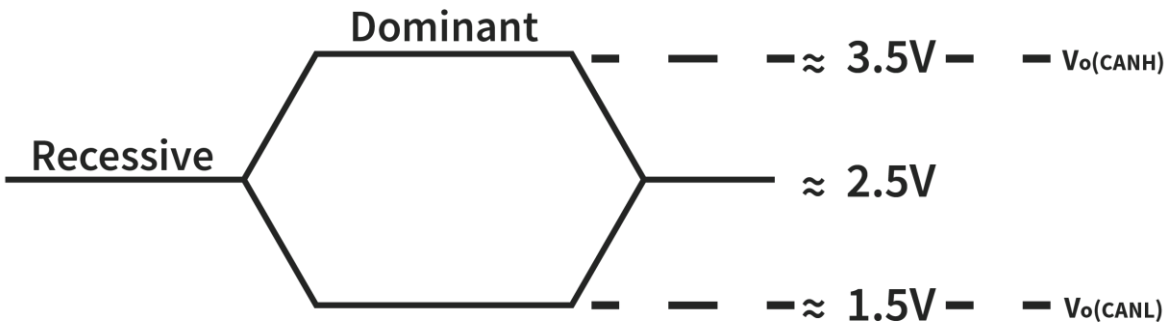


Figure 5.2. Bus Logic State Voltage Definitions

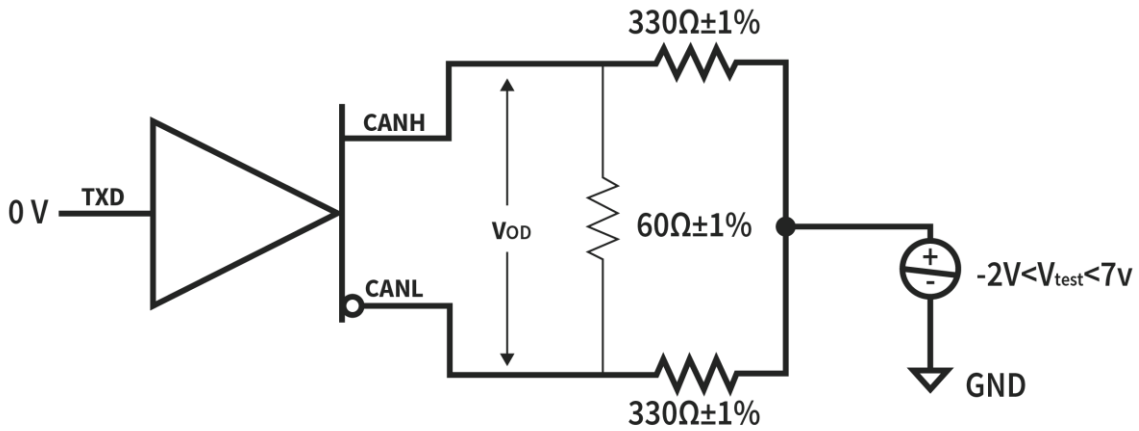
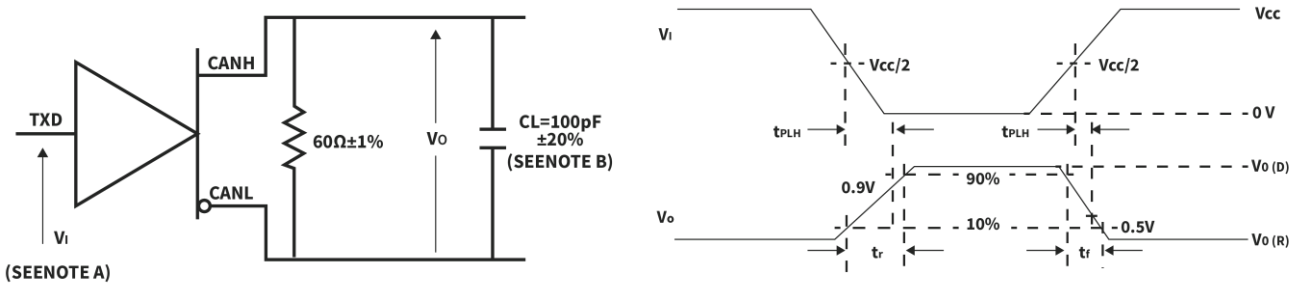


Figure 5.3. Driver V_{OD} With Common-Mode Loading Test Circuit

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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, ZO = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 5.4. Driver Test Circuit and Voltage Waveforms

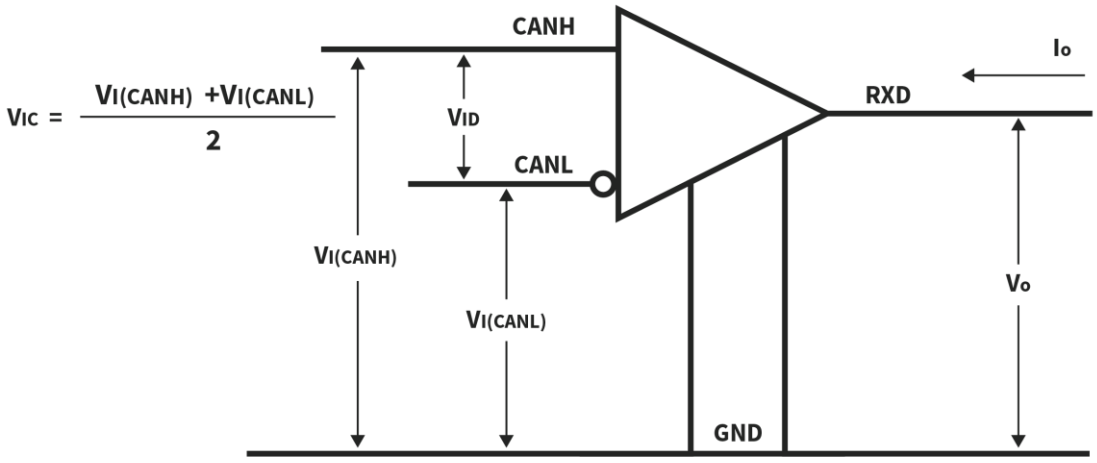
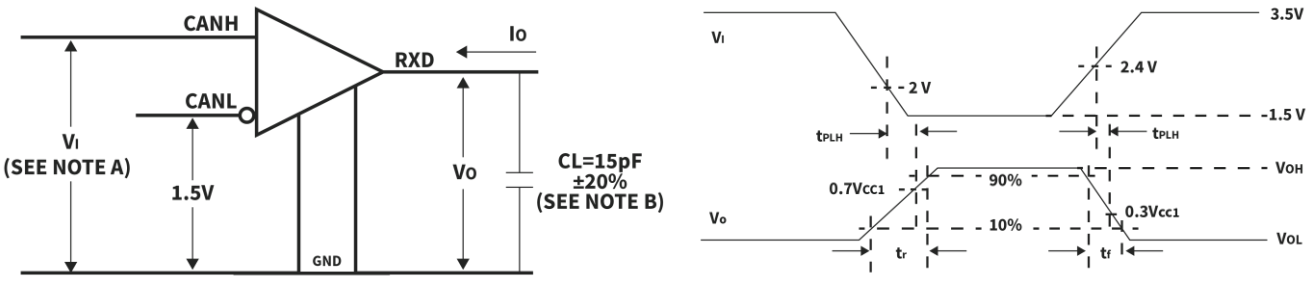


Figure 5.5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.6. Receiver Test Circuit and Voltage Waveforms

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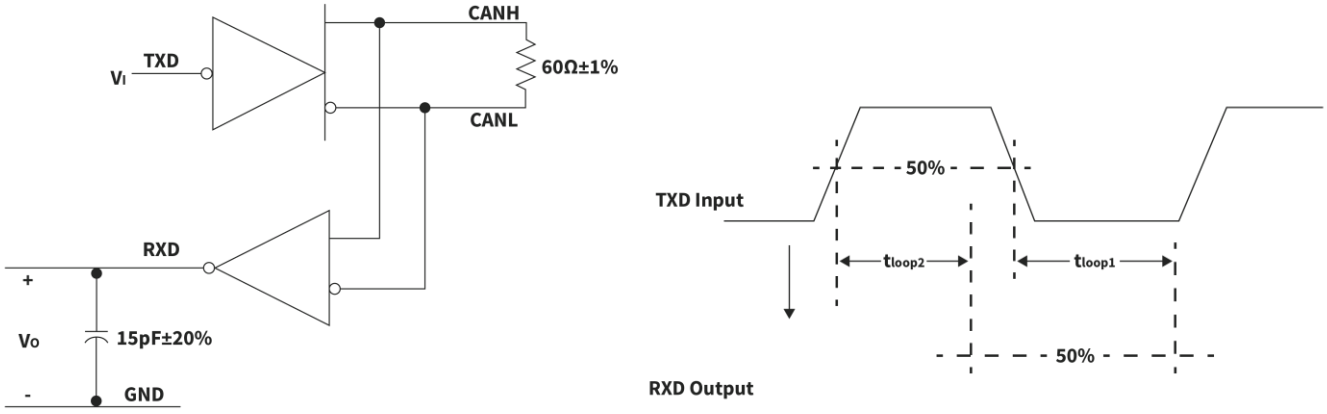
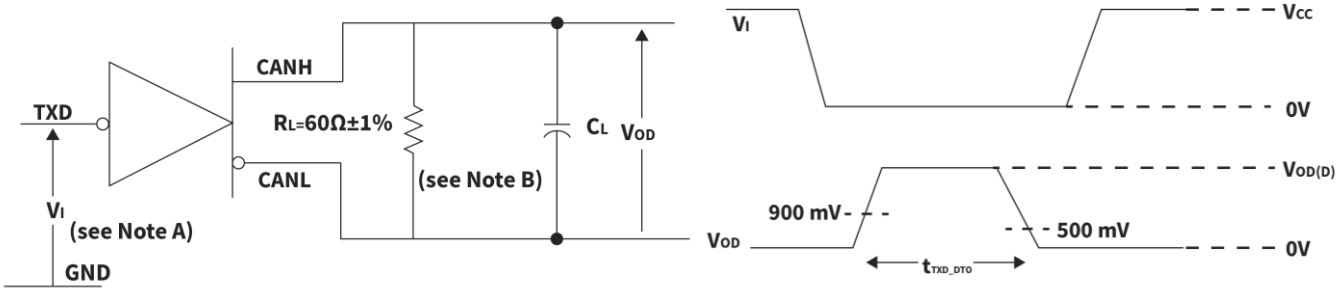


Figure 5.7. t_{LOOP} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.8. Dominant Time-out Test Circuit and Voltage Waveforms

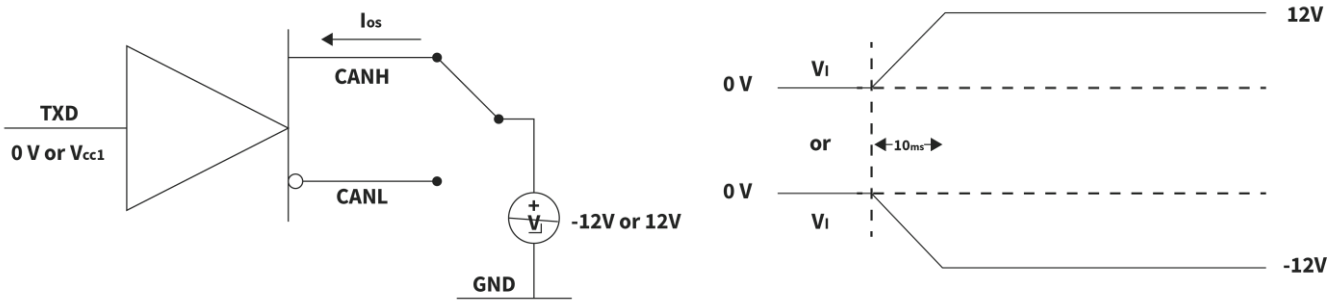


Figure 5.9. Driver Short-Circuit Current Test Circuit and Waveforms

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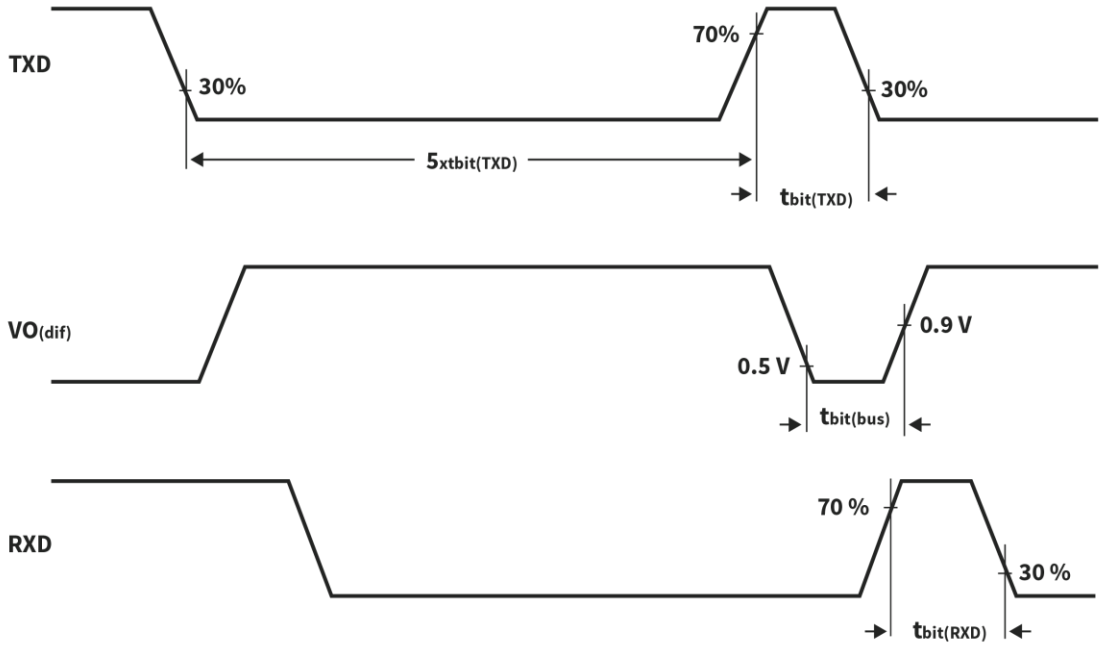


Figure 5.10. $t_{bit(RXD)}$ Test Circuit and Waveforms

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6. Function Description

6.1. Overview

The NCA1051 is a CAN transceiver which fully compatible with the ISO11898-2 standard. The NCA1051 is providing high electromagnetic immunity and low emissions. The data rate of the NCA1051 is up to 5Mbps. The NCA1051 provides thermal protection and transmit data dominant time out function.

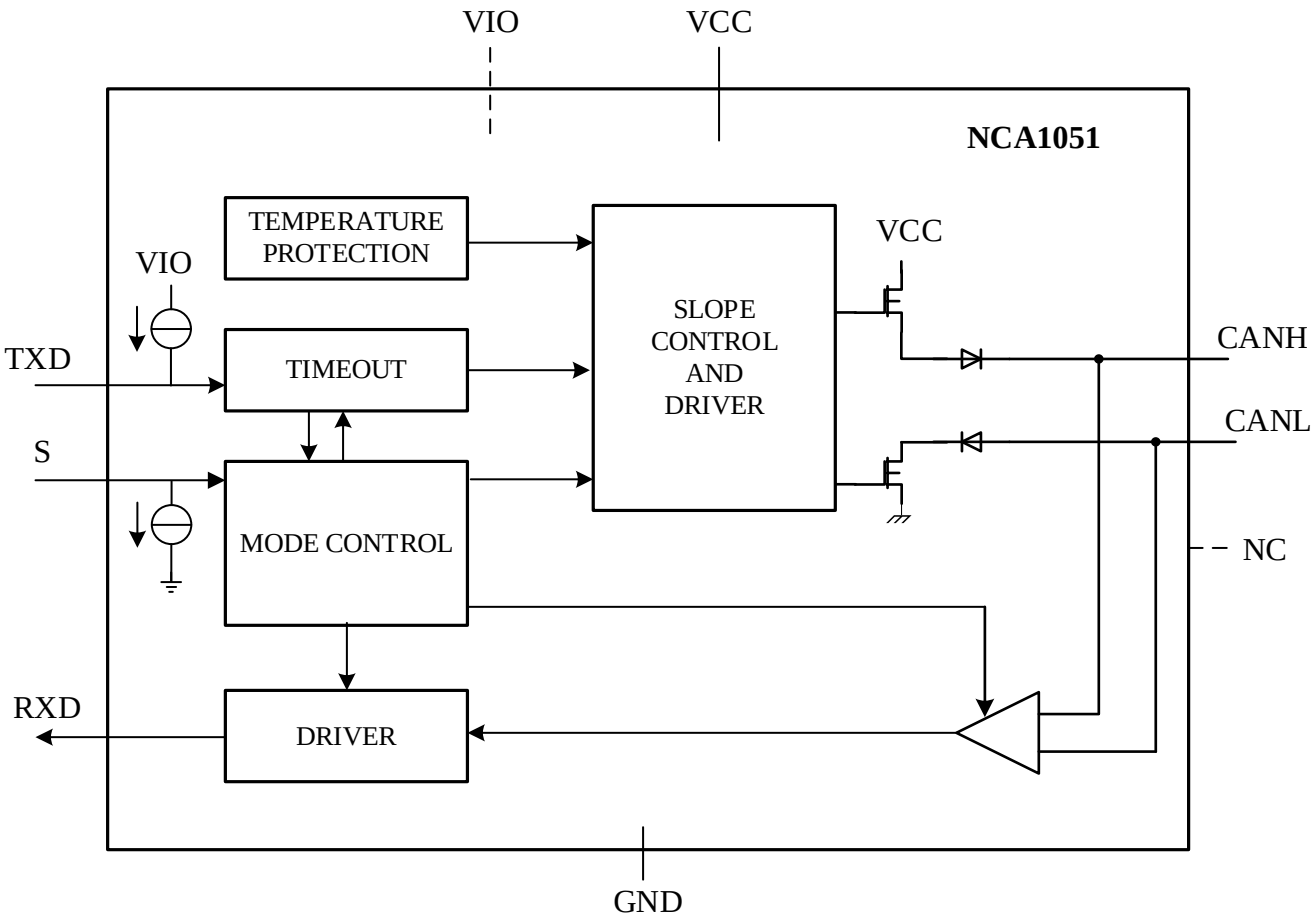


Figure6.1 Block diagram of NCA1051

6.2. Device Functional Modes

Table 6.1. Driver Function Table

TXD	CANH	CANL	BUS STATE
L[1]	H[1]	L[1]	Dominant
H[1]	Z[1]	Z[1]	Recessive
Open	Z[1]	Z[1]	Recessive

[1] H= high level; L=low level; Z= common mode(recessive) bias to $V_{CC}/2$

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Table 6.2. Receiver Function Table

V_{ID}=CANH-CANL	RXD	BUS STATE
V_{ID}≥0.9V	L[1]	Dominant
0.5< V_{ID} <0.9V	Z[1]	Uncertain
V_{ID}≤0.5V	H[1]	Recessive
Open	H[1]	Recessive

[1] H= high level; L=low level; X= uncertain

6.3. Normal mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 6.1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

6.4. Silent mode

A HIGH level on pin S selects Silent mode. In Silent mode the transmitter is disabled, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

6.5. TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state(blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.The TXD dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

6.6. Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

6.7. Over Temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{TS}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{TS} and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

6.8. VIO Output Supply

Pin V_{IO} should be connected to the microcontroller supply voltage (see Figure 7.1). This will adjust the signal levels of pins TXD, RXD and S to the I/O levels of the microcontroller. This sets the signal levels of pins TXD, RXD and S to levels compatible with 3.3 V microcontrollers.

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7. Application Note

7.1. Typical Application

The NCA1051 requires a 0.1 μF bypass capacitors between VCC and GND. The capacitor should be placed as close as possible to the package. The figure7.1 is the basic schematic of NCA1051.

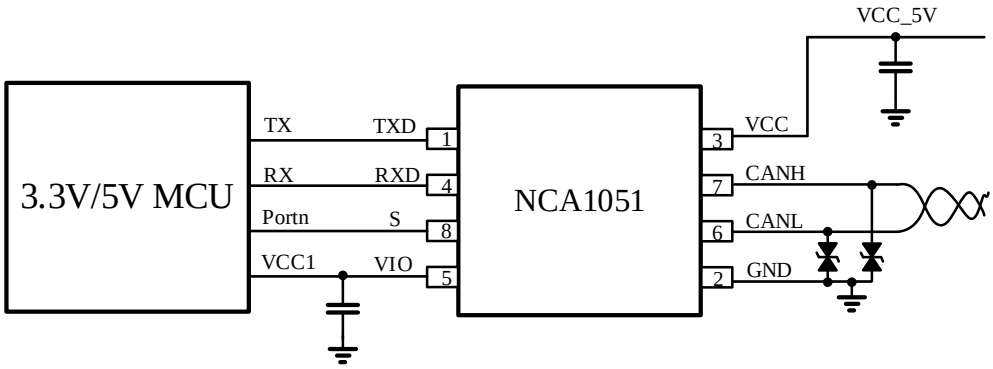
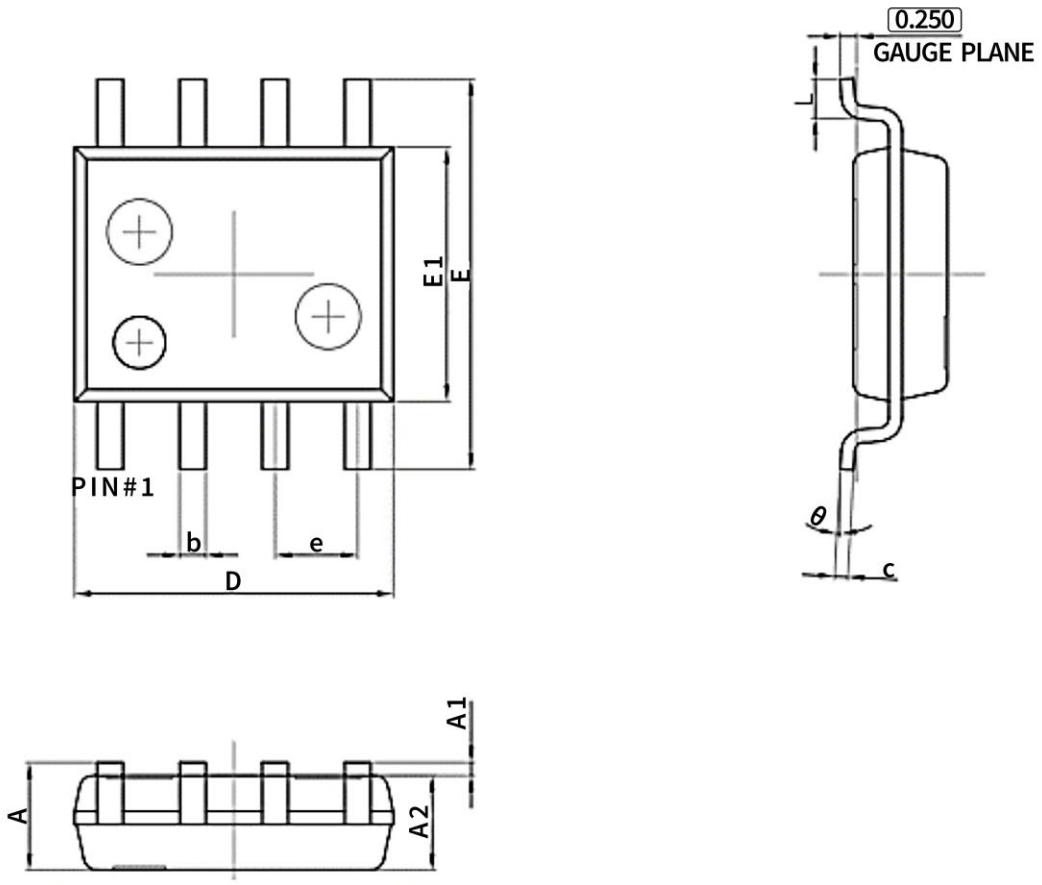


Figure 7.1 Basic schematic of NCA1051

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8. Package Information

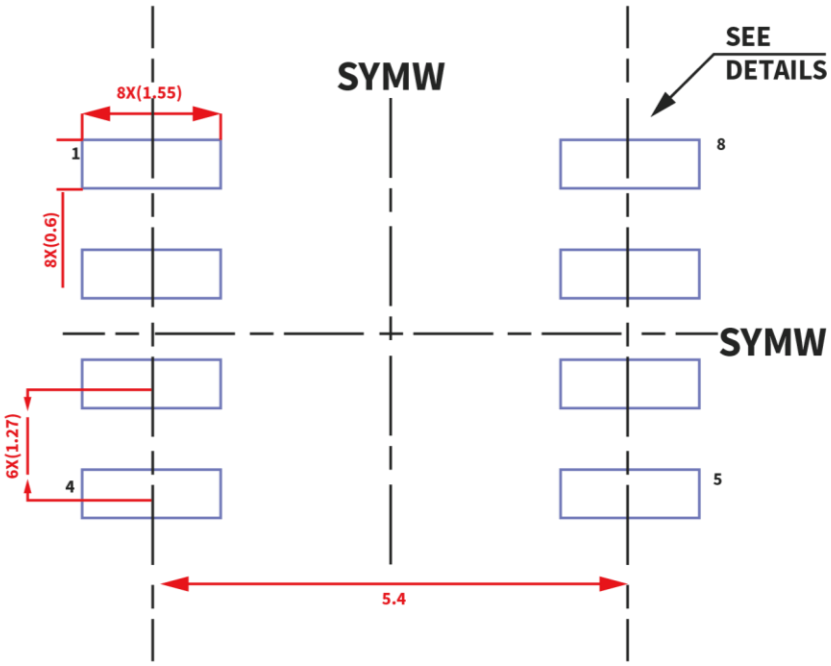


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.500(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

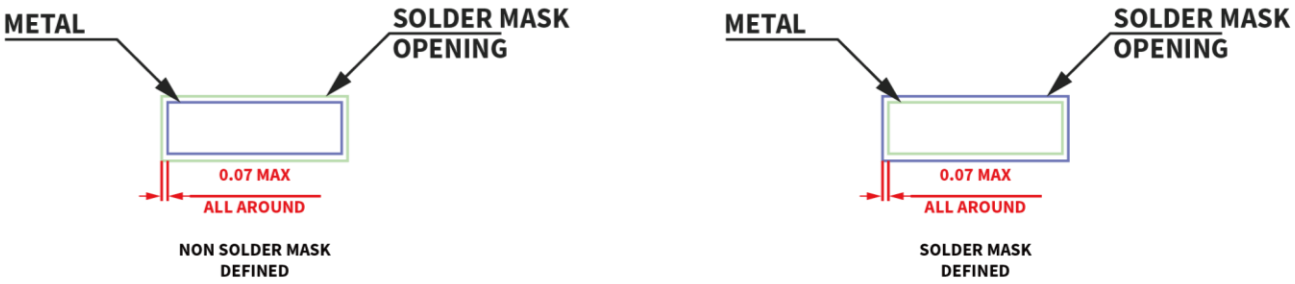
Figure 8.1 SOP8 Package Shape and Dimension in millimeters

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LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 8.2 SOP8 Package Board Layout Example

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9. Order Information

Part Number	*Max Data Rate (Mbps)*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NCA1051N-DSPR	5	-40 to 125℃	3	SOP8(150mil)	SOP8	4000
NCA1051-DSPR	5	-40 to 125℃	3	SOP8(150mil)	SOP8	4000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.						

10. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*
NCA1051	Click here	Click here	Click here

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11. Tape and Reel Information

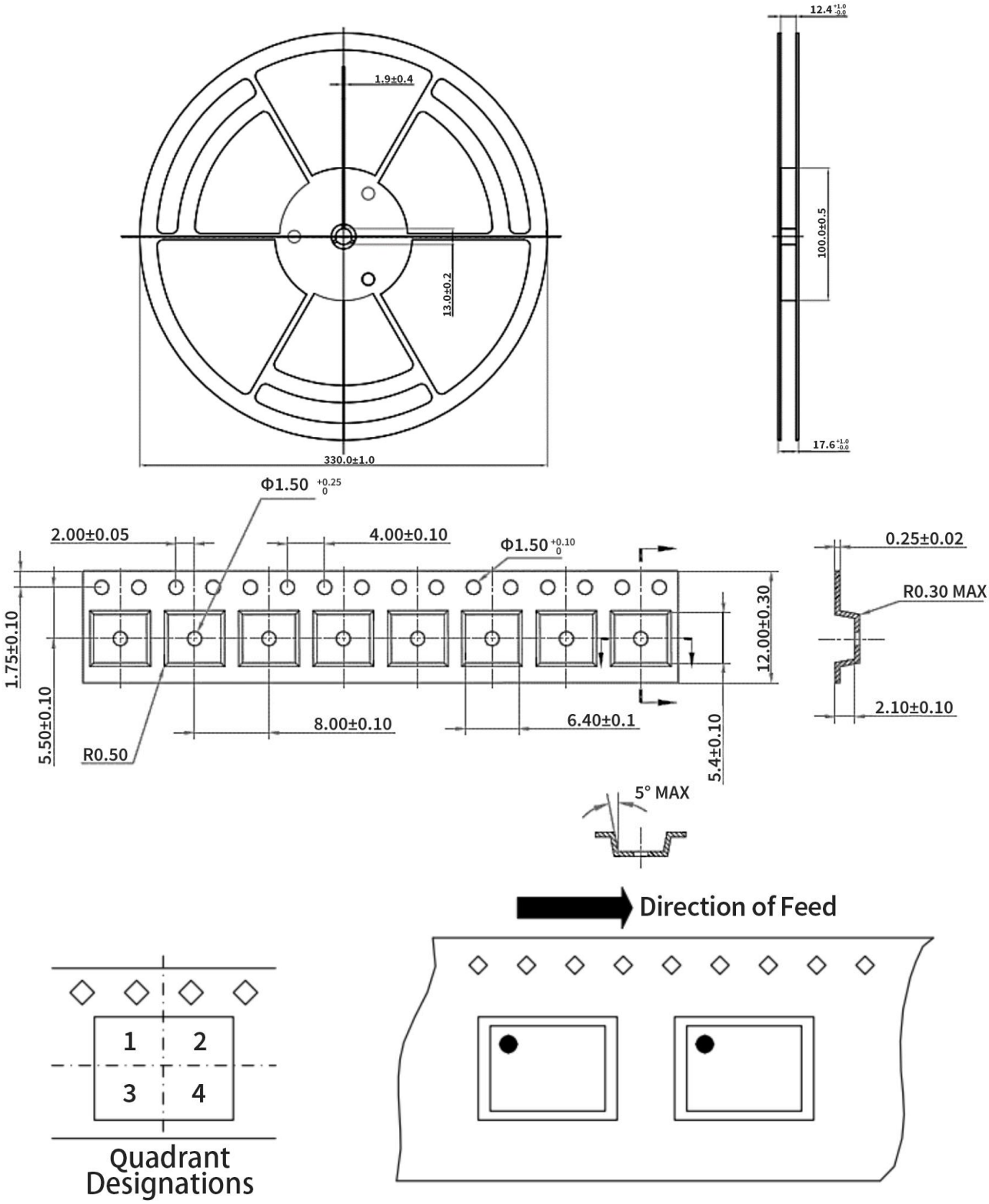


Figure 11.1 Tape and Reel Information of SOP8

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12. Revision History

Revision	Description	Date
1.0	Initial version	2021/12/3
1.1	Update Absolute Maximum Ratings	2021/12/27
1.2	Added description "VIO equals VCC in NCA1051N". Update VOH, VOL. Update VID and IOH/IOL in Absolute Maximum Ratings and Recommended Operating Conditions.	2022/10/12
1.3	One-page information update; thermal characteristics update; figure update	2023/10/26

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