NCA1042

High-speed CAN Transceiver with standby mode

Datasheet (EN) 1.0

Product Overview

The NCA1042 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus, which can support at least 110 CAN nodes. The NCA1042 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The NCA1042 provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- I/O voltage range supports 3.3V and 5V MCU
- Power supply voltage

  VIO: 3V to 5.5V

  VCC: 4.5V to 5.5V
- Bus fault protection of -45V to +45V
- Transmit data (TXD) dominant time out function
- Bus dominant time out function in standby mode
- Very low-current Standby mode with wake-up capability
- Over current and over temperature protection
- Date rate: up to 5Mbps
- Low loop delay: <250ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:

  SOP8

Applications

- 5Mbps operation in highly loaded CAN networks down to 10 kbps networks using TXD DTO
- Industrial automation, control, sensors, and drive systems
- Building, security, and climate control automation
- CAN bus standards such as CANopen、DeviceNet、NMEA2000、ARNIC825、ISO11783 and CANaerospace

Device Information

Part Number	*Package*	*Body Size*
NCA1042-DSPR	SOP8	4.90mm × 3.90mm

Functional Block Diagrams

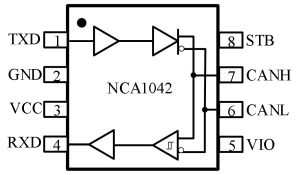


Figure 1. NCA1042 Block Diagram

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1. Pin Configuration And Functions

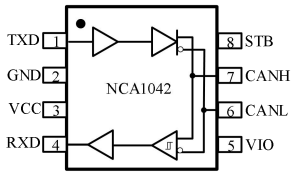


Figure 1.1 NCA1042 Package

Table1.1 NCA1042 Pin Configuration and Description

NCA1042 PIN NO.	SYMBOL	FUNCTION
1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	Ground
3	VCC	Power Supply
4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	VIO	Logic I/O supply voltage
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	STB	STB (standby mode) select pin (active high)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VCC, VIO	-0.3		7	V	
Logic I/O Voltage	TXD, RXD, STB	-0.3		7	V	
Maximum BUS Pin Voltage	V_{CANH}, V_{CANL}	-45		+45	V	
Operating Temperature	Topr	-40		125	℃	
Storage Temperature	Tstg	-40		150	℃	
System level Electro-Static Discharge	ESD			±5	kV	IEC61000-4-2:Powered contact discharge:CAN bus terminals to GND
Human Body Model(HBM) ESD stress voltage				±8	kV	All terminals
Charged Device Model(CDM)ESD stress voltage				±2	kV	All terminals

3. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VCC	4.5		5.5	V

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	VIO	3		5.5	V
RXD terminal HIGH level output current	$I_{OH(RXD)}$	-2			mA
RXD terminal LOW level output current	$I_{OL(RXD)}$			2	mA

4. Thermal Characteristics

Parameters	*Symbol*	*SOW16*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	105.8	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	46.8	℃/W
Junction-to-board thermal resistance	θ_{JB}	48.3	℃/W

5. Specifications

5.1. Electrical Characteristics

(V_{CC}=4.5V~5.5V,V_{IO}=3V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VCC=5V,VIO=3.3V,Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Voltage	V_{CC}	4.5		5.5	V	
undervoltage detection voltage on pin VCC	$V_{uvd(VCC)}$	3.5		4.5	V	
supply voltage on pin VIO	V_{IO}	3		5.5	V	
undervoltage detection voltage on pin VIO	$V_{uvd(VIO)}$	1.5		2.7		
supply current	I_{CC}		45	70	mA	Normal mode,dominant, TXD=0,STB=0,R_L=60 Ω
			1.7	5	mA	Normal mode,recessive, TXD=V_{IO},STB=0
			0.51	5	uA	Standby mode,STB=V_{IO},TXD=V_{IO}
supply current on pin VIO	I_{IO}		525	900	uA	Normal mode,dominant,V_{TXD}=0V
			30	100	uA	Normal mode,recessive,V_{TXD}=V_{IO}
			6.5	15	uA	Standby mode;V_{TXD}=V_{IO}
Thermal-Shutdown Threshold	T_{TS}	155	165	180	℃	
Logic Side						
High level input voltage	V_{IH}	0.7*V_{IO}			V	TXD &STB pin
Low level input voltage	V_{IL}			0.3*V_{IO}	V	TXD &STB pin
High level input current	I_{IH}	-5		5	uA	TXD &STB pin

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Low level input current	I_{IL}	-200		-30	uA	TXD pin
		-15		15	uA	STB pin
Output High Voltage	V_{OH}	0.8*V_{IO}			V	RXD,I_O=-2mA
Output Low Voltage	V_{OL}			0.2*V_{IO}	V	RXD,I_O=2mA
Input Capacitance	C_{IN}		5		pF	TXD pin
Driver						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.8	3.44	4.5	V	STB=0,TXD=0V, R_{Load} =60 Ω
CANL output voltage (Dominant)	$V_{OL(D)}$	0.5	1.33	2.25	V	STB=0,TXD=0V, R_{Load} =60 Ω
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	0.5*VCC	3	V	TXD=V_{IO};recessive;no load
		-0.1		0.1	V	Standby mode,no load
Differential output voltage(Dominant)	$V_{OD(D)}$	1.5		3	V	VCC=5V,TXD=0, R_{Load} =60 Ω , see Figure 5.1
Differential output voltage(Recessive)	$V_{OD(R)}$	-0.05		0.05	V	VCC=5V,TXD=VIO, R_{Load} =60 Ω , see Figure 5.1
		-0.1		0.1	V	VCC=5V,TXD=V_{IO},NO Load, see Figure 5.1
Short- circuit output current	I_{OS}	-105	-44.1		mA	Dominant,CANH=-30V, CANL open, see Figure 5.9
			1.77	5	mA	Recessive,CANH=30V, CANL open, see Figure 5.9
		-5	-2.11		mA	Recessive,CANL=-30V, CANH open, see Figure 5.9
			42.5	105	mA	Dominant,CANL=30V, CANH open, see Figure 5.9
Receiver						
Positive-going bus input threshold voltage	V_{IT+}		750	900	mV	$V_{COM(CAN)}$=0V
Negative-going bus input threshold voltage	V_{IT-}	500	650		mV	$V_{COM(CAN)}$=0V
Hysteresis voltage	V_{HYS}		100		mV	
Power-off (unpowered) bus input leakage current	$I_{IOFF(LKG)}$	-1.5		1.5	uA	V_{CANH} / V_{CANL} = 5 V, VCC = 0V, VIO= 0 V
Input capacitance to ground	C_I		13		pF	CANH or CANL
Differential input	C_{ID}		5		pF	
Differential input resistance	R_{ID}	30		80	k Ω	

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Input resistance	R_{IN}	15	30	40	kΩ	
Input resistance matching	R_{Imatch}	-3		+3	%	CANH=CANL
Common-mode voltage range	V_{COM}	-30		+30	V	

5.2. SWITCHING Electrical Characteristics

(V_{CC}=4.5V~5.5V,V_{IO}=3V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VCC=5V,VIO=3.3V,Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Loop delay1	T_{loop1}		90	220	ns	Driver input to receiver output, Recessive to Dominant, see Figure 5.7
Loop delay2	T_{loop2}		100	220	ns	Driver input to receiver output, Dominant to Recessive, see Figure 5.7
transmitted recessive bit width	$t_{bit(bus)}$	435		530	ns	$t_{bit(TXD)}$ = 500 ns
		155		210	ns	$t_{bit(TXD)}$ = 200 ns
bit time on pin RXD	$t_{bit(RXD)}$	400		550	ns	$t_{bit(TXD)}$ = 500 ns
		120		220	ns	$t_{bit(TXD)}$ = 200 ns
Driver						
Propagation delay time from TXD to bus dominant	t_{PLH}		90		ns	Normal mode,see Figure 5.4
Propagation delay time from TXD to bus recessive	t_{PHL}		65		ns	Normal mode,see Figure 5.4
Differential output signal rise time	t_r		20		ns	see Figure 5.4
Differential output signal fall time	t_f		42		ns	see Figure 5.4
Bus dominant time-out time	t_{TXD_DTO}	800	2000	4000	us	see Figure 5.8
Receiver						
Propagation delay time from bus dominant to RXD	t_{PLH}		21		ns	see Figure 5.6
Propagation delay time from bus recessive to RXD	t_{PHL}		27		ns	see Figure 5.6
RXD signal rise time	t_r		10		ns	see Figure 5.6
RXD signal fall time	t_f		10		ns	see Figure 5.6
Receiver dominant time out	t_{RXD_DTO}	800	2600	4000	us	Standby mode
bus wake-up filter time	$t_{fltr(wake)bus}$	0.5		5	us	Standby mode

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standby to normal mode delay time	$t_{d(stb-norm)}$	7		47	us	standby to normal mode delay time

5.3. Parameter Measurement Information

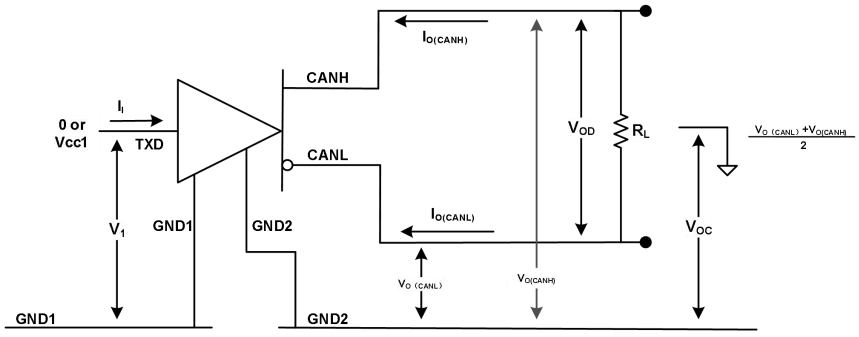


Figure 5.1. Driver Voltage, Current and Test Definitions

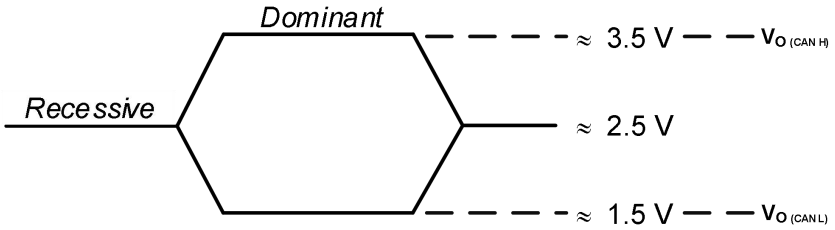


Figure 5.2. Bus Logic State Voltage Definitions

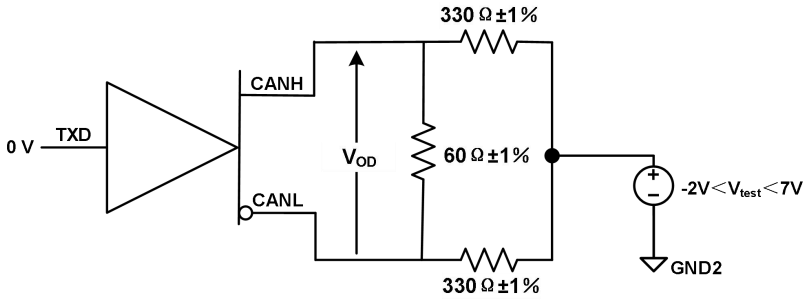
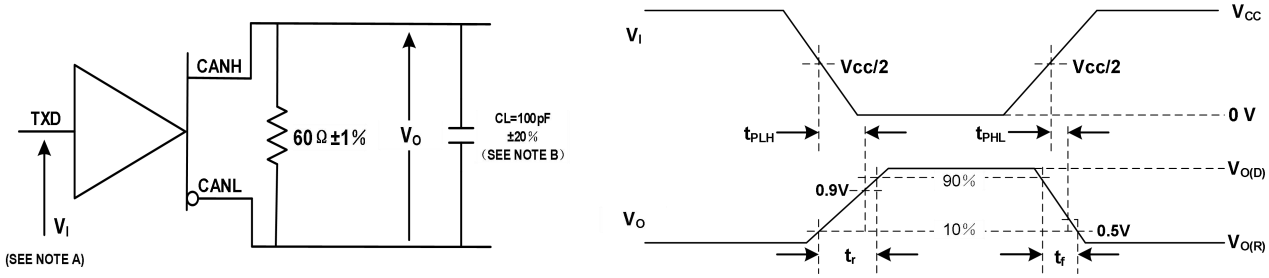


Figure 5.3. Driver V_{OD} With Common-Mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 125 kHz, 50% duty cycle, tr ⩽ 6 ns, tf ⩽ 6 ns, ZO = 50 Ω.

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B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 5.4. Driver Test Circuit and Voltage Waveforms

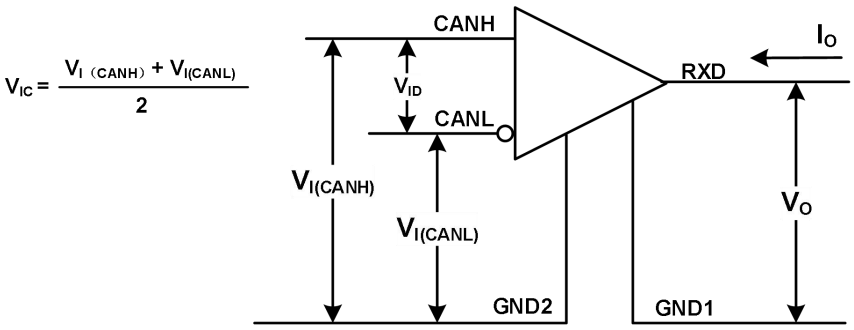
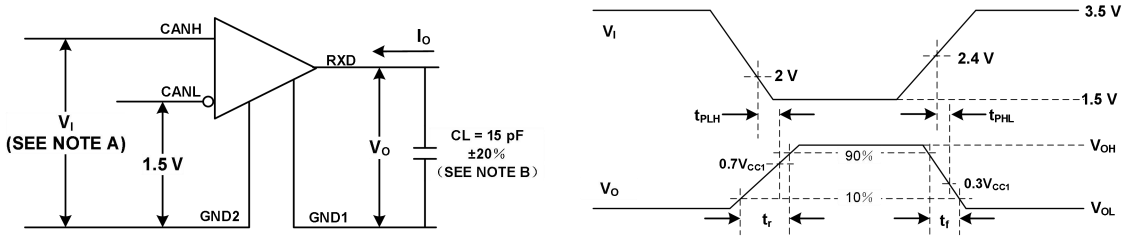


Figure 5.5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 125 kHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.6. Receiver Test Circuit and Voltage Waveforms

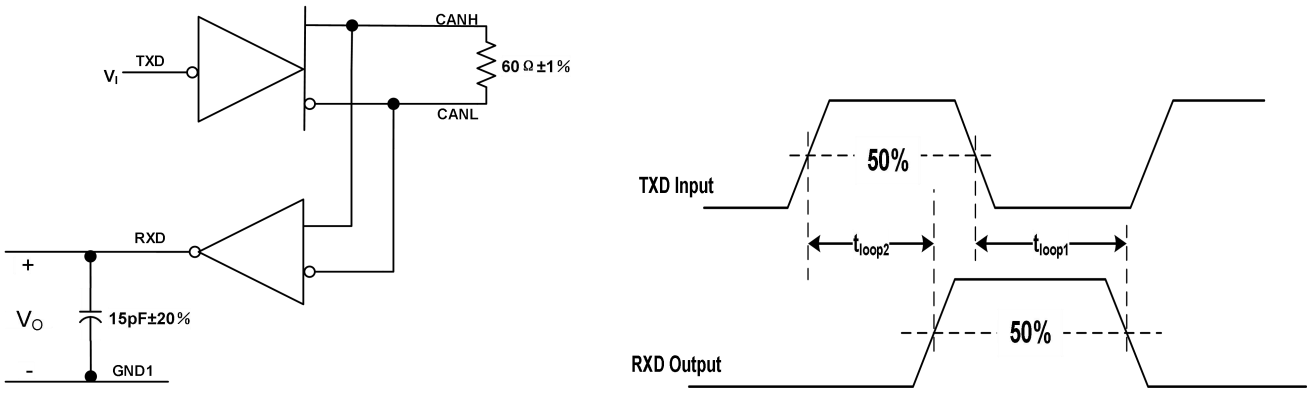
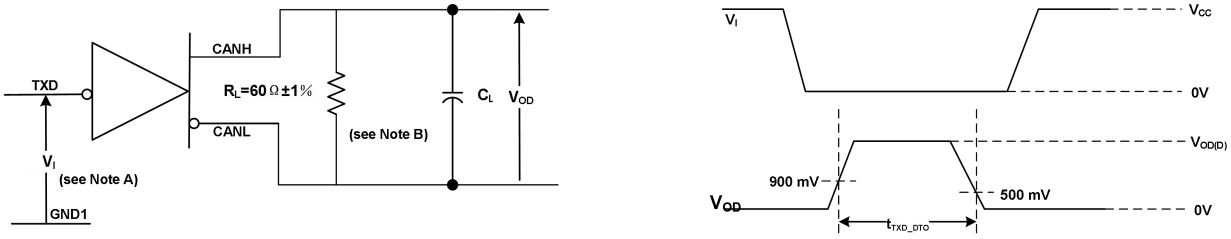


Figure 5.7. t_{LOOP} Test Circuit and Voltage Waveforms

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A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 125 kHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.8. Dominant Time-out Test Circuit and Voltage Waveforms

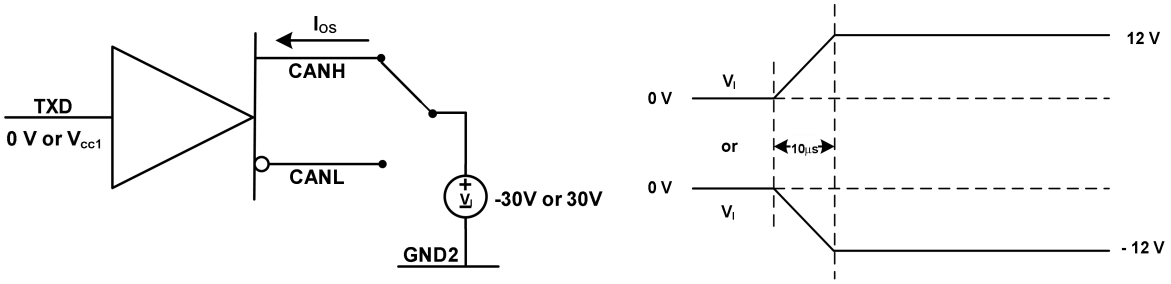


Figure 5.9. Driver Short-Circuit Current Test Circuit and Waveforms

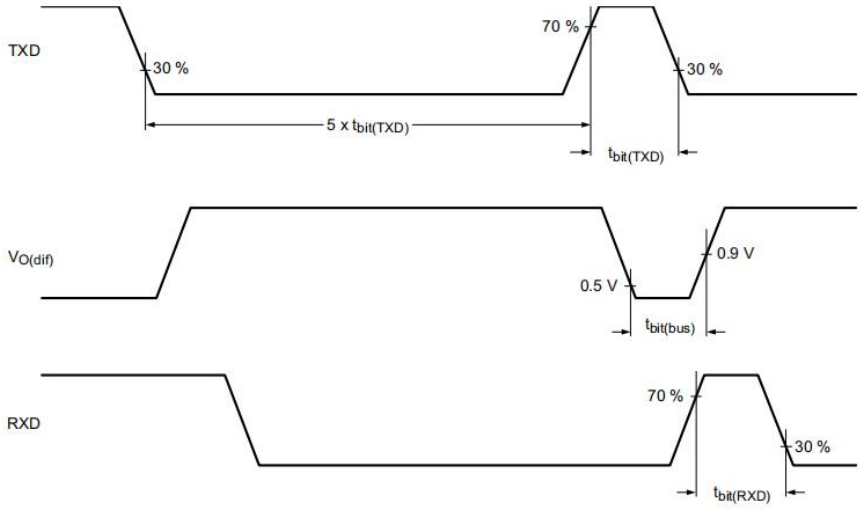


Figure 5.10. $t_{bit(RXD)}$ Test Circuit and Waveforms

6. Function Description

6.1. Overview

The NCA1042 is a CAN transceiver which fully compatible with the ISO11898-2 standard. The NCA1042 is providing high electromagnetic immunity and low emissions. The data rate of the NCA1042 is up to 5Mbps, and it can support at least 110 CAN nodes. The NCA1042 provides thermal protection and transmit data dominant time out function.

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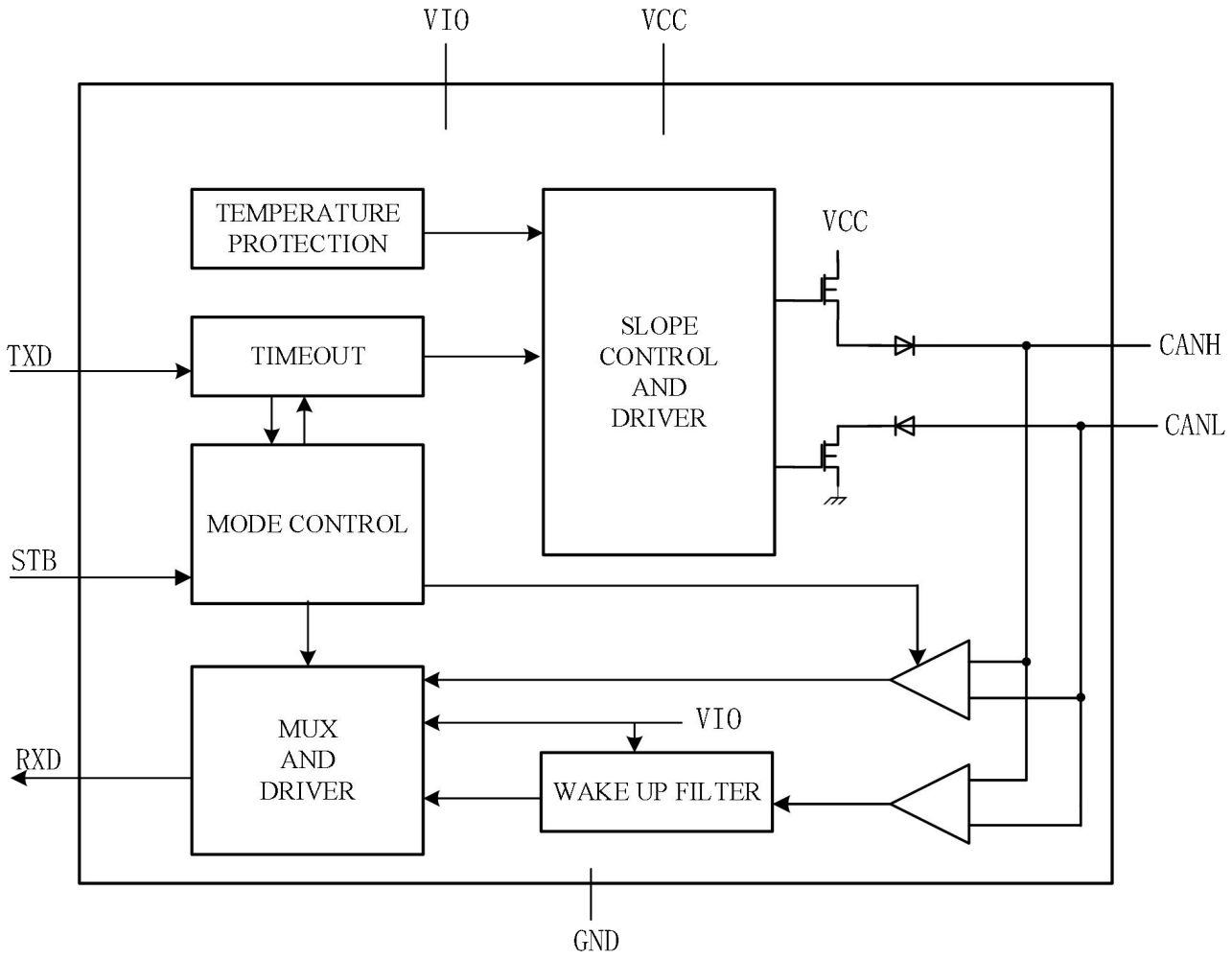


Figure 6.1 Block diagram of NCA1042

6.2. Device Functional Modes

Table 6.1. Driver Function Table

TXD	*CANH*	*CANL*	*BUS STATE*
L[1]	H[1]	L[1]	Dominant
H[1]	Z[1]	Z[1]	Recessive
Open	Z[1]	Z[1]	Recessive

[1] H= high level; L=low level; Z= common mode(recessive) bias to $V_{CC}/2$

Table 6.2. Receiver Function Table

V_{ID}=CANH-CANL	*RXD*	*BUS STATE*
$V_{ID} \geqslant 0.9V$	L[2]	Dominant
$0.5< V_{ID} <0.9V$	X[2]	Uncertain
$V_{ID} \leqslant 0.5V$	H[2]	Recessive

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Open	H[2]	Recessive

[2] H= high level; L=low level; X= uncertain

6.3. Normal mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 6.1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

6.4. Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)}$ bus are reflected on pin RXD. In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by VIO, and is capable of detecting CAN bus activity even if VIO is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

6.5. TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state(blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.The TXD dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

6.6. RXD dominant time-out function

In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than t_{RXD_RTO}, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

6.7. Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

6.8. Over Temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{TS}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{TS} and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

6.9. VIO Output Supply

Pin VIO should be connected to the microcontroller supply voltage (see Figure 7.1). This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. This sets the signal levels of pins TXD, RXD and STB to levels compatible with 3.3 V microcontrollers.

7. Application Note

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7.1. Typical Application

The NCA1042 requires a 0.1 µF bypass capacitors between VCC and GND. The capacitor should be placed as close as possible to the package. The figure7.1 is the basic schematic of NCA1042.

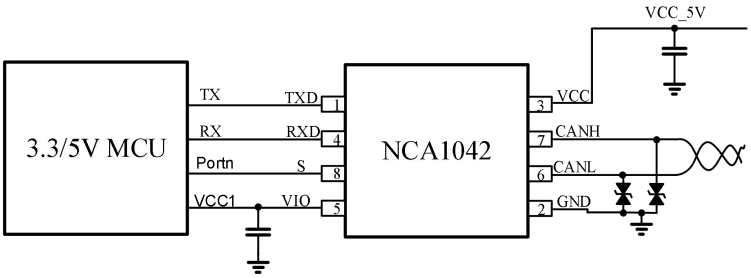
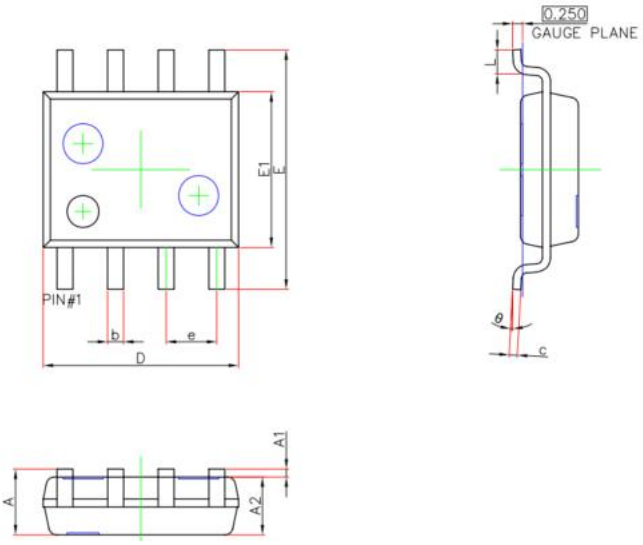


Figure 7.1 Basic schematic of NCA1042

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8. Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Figure 8.1 SOP8 Package Shape and Dimension in millimeters

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9. Order Information

Part Number	*Max Data Rate (Mbps)*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NCA1042-DSPR	5	-40 to 125℃	3	SOP8(150mil)	SOP8	4000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.						

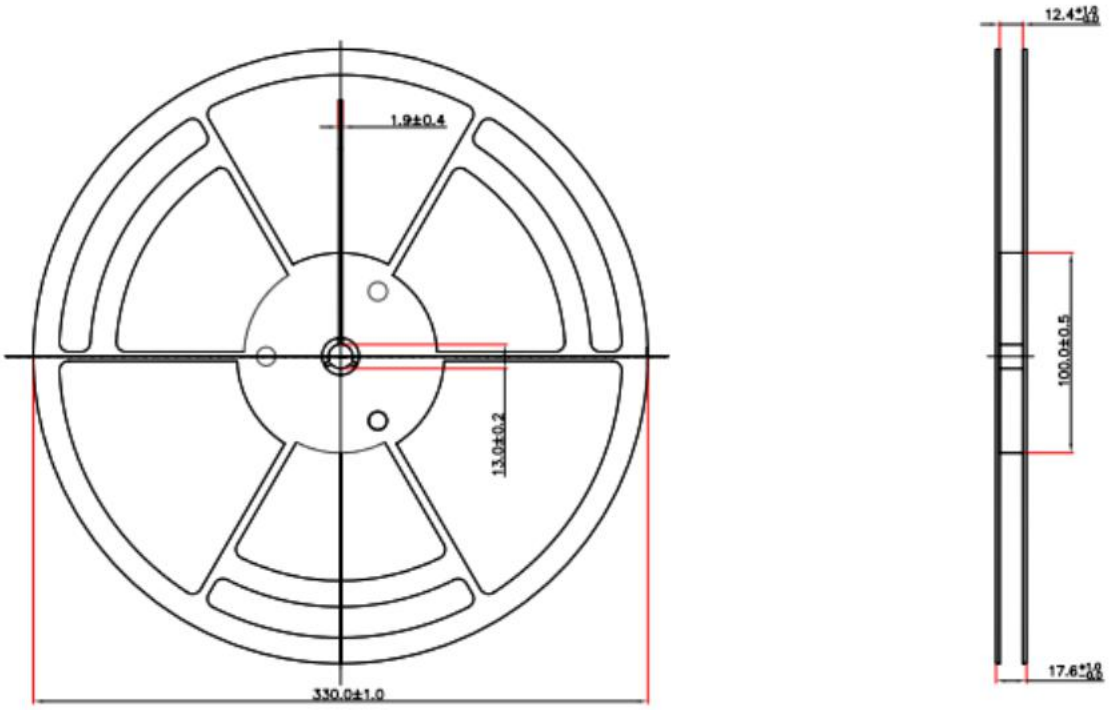
10. Documentation Support

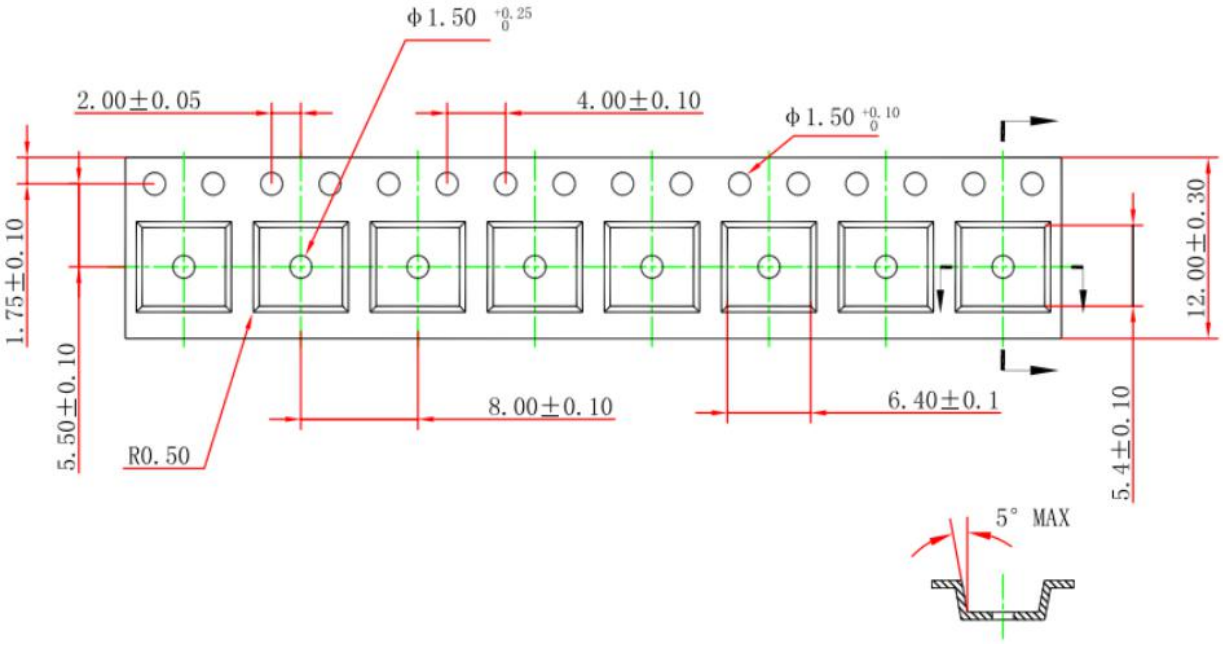
Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NCA1042	Click here	Click here	Click here	Click here

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11. Tape And Reel Information





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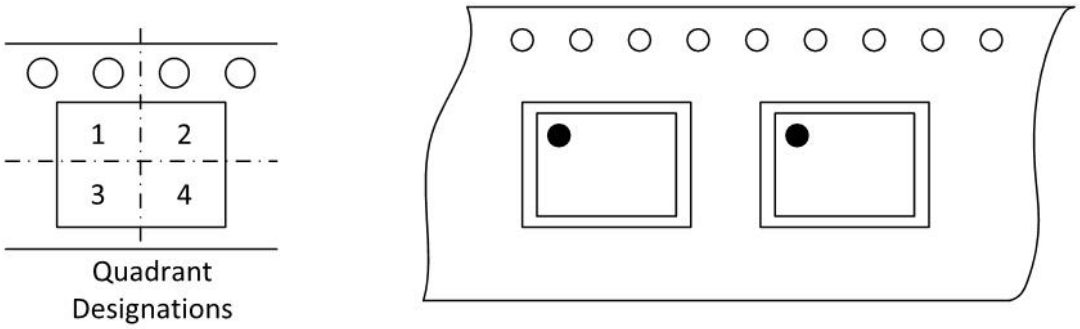


Figure 11.1 Tape and Reel Information of SOP8

12. Revision History

Revision	Description	Date
1.0	Initial version	2021/7/4

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