Comparing Micron MT25QL01GB with Macronix MX66L1G45G

1. Introduction

This application note serves as a guide to compare Micron MT25QL01GB with Macronix MX66L1G45G 3V 1Gb serial NOR flash. The document does not provide detailed information on each individual device,but highlights the similarities and differences between them. The comparison covers the general features, performance, command codes, and other differences.

If common features are used in standard traditional modes, they may need only minimal software modification. Minor pinout and timing differences are reviewed as well.
The information provided in this document is based on datasheets listed in Section 9. Newer versions of the datasheets may override the contents of this document.

2. Features

Both flash device families have similar features and functions as shown in Table 2-1 and 2-2.

Table 2-1: Feature Comparison

Type / Function	Macronix MX66L1G45G	Micron MT25QL01GB
VCC Voltage Range	2.7V-3.6V	2.7V-3.6V
Normal Read Clock Frequency	66MHz	54MHz
Maximum STR Clock Frequency(1)	166MHz	133MHz
Maximum DTR Clock Frequency	83MHz	66MHz
Configurable Dummy Cycles	YES	YES
Sector Size	4KB/32KB/64KB	4KB/32KB/64KB
Program Buffer Size	256Byte	256Byte
Security OTP	512Byte	64Byte
XIP / Performance Enhanced Mode	YES	YES(3)
XIP / Performance Enhanced Mode Set at Power-on	YES	YES(3)
Program/Erase Suspend & Resume	YES	YES
Wrap Around Read Mode	YES	YES
Adjustable Output Driver	YES	YES
Deep Power Down	YES	YES
S/W Reset Command	YES	YES
HOLD#/RESET# Pin	Reset#	Hold#/Reset#
Block Protection Mode (BP bits)	Top/Bottom	Top/Bottom
Individual Sector Protection (Volatile) (2)	YES	YES
Program/Erase Cycles	100K	100K

Notes:
1. Maximum clock frequency with default dummy cycles shown in Table 2-2.
2. Please see App Note section 4-4 for detailed comparison of Individual Sector Protection.
3. Macronix supports 1-4-4 and 4-4-4 mode XIP; Micron supports XIP in all fast read modes.

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Comparing Micron MT25QL01GB with Macronix MX66L1G45G

Both devices support Double Transfer Rate (DTR) mode. While the Micron device supports DTR use with all Read modes, Macronix only supports DTR use in the Fast DTR Read (1-1-1), Dual I/O DTR Read (2DTRD = 1-2-2), and Quad I/O DTR Read (4DTRD SPI = 1-4-4) modes (Table 2-2).

Table 2-2: Read Performance

Read Mode[1]	Macronix MX66L1G45G		Micron MT25QL01GB	
	Default Dummy Cycles	Max Speed @ Default Dummy Cycles[2]	Default Dummy Cycles	Max Speed @ Default Dummy Cycles[2]
Fast Read (1-1-1)	8	133MHz	8	133MHz
Dual Output Read (DREAD = 1-1-2)	8	133MHz	8	133MHz
Dual I/O Read (2READ = 1-2-2)	4	84MHz	8	133MHz
Dual Peripheral Interface (2-2-2)	-	-	8	133MHz
Quad Output Read (QREAD = 1-1-4)	8	133MHz	8	133MHz
Quad I/O SPI Read (4READ SPI = 1-4-4)	6	84MHz	10	125MHz
Quad I/O QPI Read (4READ QPI= 4-4-4)	6	84MHz	10	125MHz
Fast DTR Read (1-1-1)	8	66MHz	6	66MHz
Dual Output DTR Read (1-1-2)	-	-	6	66MHz
Dual I/O DTR Read (2DTRD = 1-2-2)	4	52MHz	6	57MHz
Quad Output DTR Read (1-1-4)	-	-	6	57MHz
Quad I/O SPI DTR Read (4DTRD SPI = 1-4-4)	6	52MHz	8	66MHz
Quad I/O QPI DTR Read (4DTRD QPI = 4-4-4)	6	52MHz	8	53MHz

Notes:

1. *In the x-y-z notation used in this applications note, x specifies the number of channels for the command, y specifies the number of channels for the address, and z is the number of channels for data.*
2. *Higher clock rates can be achieved with increased number of dummy cycles (see datasheet).*

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Comparing Micron MT25QL01GB with Macronix MX66L1G45G

3. Package and Pinout

Both devices are available in a 24-BGA package with similar footprints. Pinout definitions are identical with the two exceptions shown in Table 3-2.

Where Macronix has a NC/SIO3 pin on D4, Micron has either a HOLD#/DQ3 or a RESET#/DQ3 pin. If the Micron device has a HOLD# pin, but the HOLD# function is not used, then the devices are pin compatible.

Similarly, Micron Ball A4 can be a No Connect or a Reset# pin. If the Reset# pin is available, the two device pins are identical, and if the Micron part is a NC, the devices are still compatible as the Macronix Ball A4 Reset# has an internal pull up.

Figure 3-1: 24-BGA (6x8mm with 5x5 Ball Array)

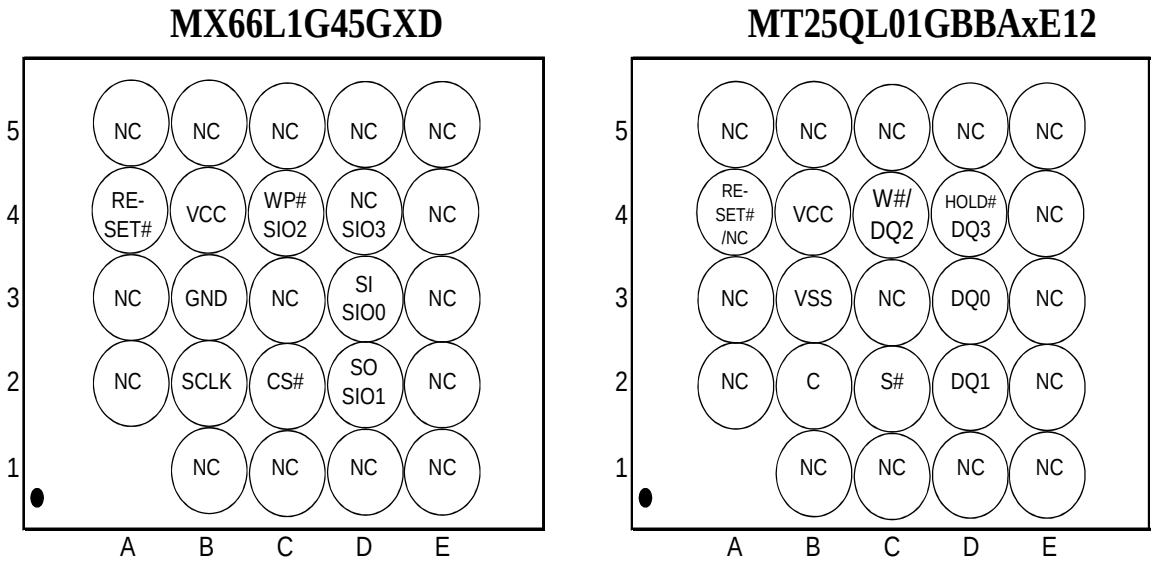


Table 3-1: 24-BGA Pin Definition Comparison

Package Ball	Macronix MX66L1G45G	Micron MT25QL01GB	Comments
Ball D4	NC/SIO3	HOLD#/DQ3	HOLD# not supported by Macronix. Dedicated Micron part numbers offer RESET# instead of HOLD#. NC means “No Connect”
Ball A4	RESET#	RESET#/NC	Dedicated Micron part numbers offer RESET# instead of NC. NC means “No Connect” Macronix RESET# pin has internal pull up.

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4. Key Feature and Operational Differences

4-1 Status Register and Configuration Register Differences

Both devices use status and configuration registers to control device behavior and report status. The registers and bits used are similar but not identical. Micron also has Non-Volatile registers not shown. Both the Micron and Macronix devices use BP[3:0] bits to select the same memory areas for protection.

The MT25QL01GB Block Protection bits BP[3:0] are located in Status Register (bits 6 and [4:2]). The Top/Bottom bit is located in Status Register bit 5 and selects whether block protection starts at the top or bottom of memory. The BP[3:0] and Top/Bottom bits are nonvolatile and reprogrammable.

The MX66L1G45G Block Protection bits BP[3:0] are located in Status Register bits [5:2]. The top/bottom starting point is controlled by the TB bit, which is located in Configuration Register bit 3. The default setting of the TB bit starts block protection at the top of memory. If the 'bottom' starting point is selected, it can never be returned to the 'top' starting point. The BP[3:0] bits are all nonvolatile and reprogrammable. The TB bit is nonvolatile and one-time-programmable.

Table 4-1: Status Register Bits

Register Bit	Macronix MX66L1G45G	Micron MT25QL01GB
Bit0	WIP; 1=write operation	WIP; 1=write operation
Bit1	WEL; 1=write enable	WEL; 1=write enable
Bit2	BP0; BP protection	BP0; BP protection
Bit3	BP1; BP protection	BP1; BP protection
Bit4	BP2; BP protection	BP2; BP protection
Bit5	BP3; BP protection	**T/B; Top/Bottom Protect**
Bit6	QE; 1=Quad mode enable	BP3; BP protection
Bit7	SRWD; 1=SR write disable	SRWD; 1=SR write disable

Table 4-2: Configuration Register/ Enhanced Volatile Configuration Register

Register Bit	Macronix MX66L1G45G	Micron MT25QL01GB
Bit0	ODS0 (Output Driver Strength)	ODS0 (Output Driver Strength)
Bit1	ODS1 (Output Driver Strength)	ODS1 (Output Driver Strength)
Bit2	ODS2 (Output Driver Strength)	ODS2 (Output Driver Strength)
Bit3	**T/B; Top/Bottom Protect**	Reserved
Bit4	PBE; 1=Enable Preamble bit	Reset/Hold; 1=Enable
Bit5	**4-BYTE; 1=4Byte address**	DTR Protocol
Bit6	DC0 (Dummy Cycle 0)	DPI protocol; 1=disable
Bit7	DC1 (Dummy Cycle 1)	QPI protocol; 1=disable

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Comparing Micron MT25QL01GB with Macronix MX66L1G45G

Table 4-3: Macronix Security Register vs. Micron Flag Status Register

Register Bit	Macronix MX66L1G45G	Micron MT25QL01GB
Bit0	Secured OTP Indicator; 1=factory lock	**Address; 1=4-Byte address**
Bit1	LDSO; 1=OTP lock down	Protection
Bit2	PSB (Program/Suspend bit)	PSB (Program/Suspend bit)
Bit3	**ESB (Erase/Suspend bit)**	Reserved
Bit4	Reserved	P_FAIL; 1=Program fail
Bit5	P_FAIL; 1=Program fail	E_FAIL; 1=Erase fail
Bit6	E_FAIL; 1=Erase fail	**Erase Suspend; 1=suspend**
Bit7	WPSEL; 1=Individual WP	PGM/ERS controller;1=ready

4-2 QPI Differences

Micron's Quad I/O mode is entered by setting a bit in the Nonvolatile Configuration Register, which remembers this mode after power cycles, or by setting a bit in the Enhanced Volatile Configuration Register and is reset after a power cycle.
The MX66L1G45G requires an EQIO (35h) command to enter the equivalent QPI mode. This mode can be terminated by a RSTQIO (F5h) command or by a power cycle or software reset.

4-3 XIP Differences

The XIP (eXecute In Place) feature (Macronix refers to this as Performance Enhance Mode) is only used during Fast Read operations and eliminates the need to input read commands prior to entering an address and reading data. This is an overhead reduction feature that increases data throughput. Both devices offer this feature, but entry and exit methods are different. The MX66L1G45G enters XIP mode whenever all four bits of the first and second dummy cycles of a FREAD instruction are not equal and will exit XIP mode if any of the bits of the first and second dummy cycles are equal. Macronix only supports XIP in Quad I/O (1-4-4) and QPI (4-4-4) modes. Micron supports XIP in all Fast Read I/O modes.

4-4 Individual Sector/Block Protection Differences

Both devices have the ability to protect individual 64KB sectors/blocks of memory. The methods used are independent of the nonvolatile BP bit configuration in the Status Register. With the Micron flash, it is possible to use both methods of write protection (BP bits and Individual Sector Protection) simultaneously, and the protected area is the combination of the two. When using the Macronix flash, either BP bit Protection or Individual Block Protection can be selected exclusively, with the default being the use of the BP bits.

The MT25QL01GB has one Lock Register for each 64KB sector to control the sector's program/erase protection status. The protection can be turned on or off at any time unless the sector's Lock Register has been locked by the application. Once locked, its associated sector will remain in the protected or unprotected state until the next power cycle or reset. All sectors not protected by the Status Register BP configuration will be unprotected after power up and all Lock Registers will be unlocked.
The MX66L1G45G has one volatile protection register for each of the top sixteen 4KB sectors, bottom sixteen 4KB sectors, and 2046 middle 64KB blocks of memory. These protection registers can only be used after permanently disabling the Status Register BP protection bits. This is done by executing the WPSEL instruction once. Please note that this irreversible and the individual sector/block protection method will be permanently selected.

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Comparing Micron MT25QL01GB with Macronix MX66L1G45G

After permanently selecting the individual sector/block protection method for the MX66L1G45G, all sectors and blocks will be locked by default on power up. Sectors/blocks must be unlocked before they can be programmed or erased. Unlocking sectors/blocks can be done on an individual basis with the SBULK (Single Block Unlock) command or on all sectors/blocks with the GBULK (Global Block Unlock) command. Sectors and blocks can be relocked as necessary with the SBLK (Single Block Lock) command or GBLK (Global Block Lock) command.

Since the smallest individual sector protection size in the MT25QL01GB is 64KB, if an application is currently locking/unlocking the top and/or bottom 64KB sector(s), it will need to lock/unlock each of the 16 top and/or bottom 4KB sectors in the MX66L1G45G for equivalent results.

4-5. Chip Erase Differences

The Micron MT25QL01GB supports the Bulk Erase function= 512Mb, which means users have to execute two Bulk Erase Commands (once in each die) to finish a chip erase operation. In the meantime, The Macronix MX66L1G45G device looks and works like a monolithic 1Gb die and only needs one CE command with no address required.

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Comparing Micron MT25QL01GB with Macronix MX66L1G45G

5. Performance

Tables 5-1 and 5-2 show that the two devices have similar AC and DC performance.

Table 5-1: AC Parameter Comparison

Parameter	Symbol		Condition	Macronix MX66L1G45G	Micron MT25QL01GB
	Macronix	Micron			
Clock High Time	tCH	tCH	min	45% fTSCLK	3.375ns
Clock Low Time	tCL	tCL	min	45% fTSCLK	3.375ns
Clock Low to Output Valid (STR mode)	tCLQV	Tclqv	max	6ns (15pF)	5ns (10pF)
				8ns (30pF)	6ns (30pF)
Output Hold Time	tCLQX	tCLQX	min	1ns	1ns
Data In Setup Time	tDVCH	tDVCH	min	2ns	1.75ns
Data In Hold Time	tCHDX	tCHDX	min	4ns	2.5ns
VCC(min) to CS# low	tVSL	tVSL	min	1500us	-
			max	-	300us
Page Program Time (256 Bytes)	tPP	tPP	typ	0.6ms	0.2ms
			max	3ms	2.8ms
Erase 4KB Subsector/Sector	tSE	tSE	typ	85ms	50ms
			max	400ms	400ms
Erase 32KB Sector	tBE32	-	typ	380ms	100ms
			max	2s	1s
Erase 64KB Sector/Block	tBE	tSE	typ	680ms	150ms
			max	4s	1s
Bulk Erase / Chip Erase	tCE	tBE	typ	480s	306s(1)
			max	1200s	920s(1)

Notes:
1. Calculated with Single Die Erase cycle time (512Mb) x2.

Table 5-2: DC Parameter Comparison

Parameter	Symbol		Condition	Macronix MX66L1G45G	Micron MT25QL01GB
	Macronix	Micron			
Leakage Current	ILI/ILO	ILI/ILO	max	+/- 4uA	+/- 2uA
Standby Current	ISB1	ICC1	typ	60uA	60uA
			max	200uA	200uA
VCC Read Current (Fast Read)	ICC1	ICC3	max @ 133MHz (Quad I/O)	-	22mA
			max @ 104MHz (Quad I/O)	40mA	-
			max @ 84MHz	30mA	-
			max @ 54MHz	-	6mA
VCC Program Current	ICC2	ICC4	max	25mA	60mA
VCC Write Status Register Current	ICC3	ICC5	max	40mA	60mA
VCC Erase Current	ICC4	ICC6	max	25mA	50mA

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6. Command Code

Both devices use the same basic command set, but there are a few minor differences highlighted in Table 6-1.

Table 6-1: Command Code Comparison

Instruction Type	Instruction	Description	Macronix MX66L1G45G	Micron MT25QL01GB
Read ID	RDID	Read Identification	9Fh	9Eh/9Fh
Read (STR)	RDSFDP	Read Serial Flash Discoverable P. Table	5Ah	5Ah
	READ	Read Data Bytes (3B/4B)	03h / 13h	03h / 13h
	FAST_READ	Read Data Bytes at Higher Speed (3B/4B)	0Bh / 0Ch	0Bh / 0Ch
	DOFR	Dual Output Fast Read (3B/4B)	3Bh / 3Ch	3Bh / 3Ch
	DIOFR	Dual Input/Output Fast Read (3B/4B)	BBh / BCh	BBh / BCh
	QOFR	Quad Output Fast Read (3B/4B)	6Bh / 6Ch	6Bh / 6Ch
	QIOFR	Quad Input/Output Fast Read (3B/4B)	EBh /ECh	EBh /ECh
Read (DTR)	FAST_READ	Read Data Bytes at Higher Speed	0Dh / 0Eh	0Dh / 0Eh
	DOFR	Dual Output Fast Read	-	3Dh
	DIOFR	Dual Input/Output Fast Read (3B/4B)	BDh / BEh	BDh / BEh
	QOFR	Quad Output Fast Read	-	6Dh
	QIOFR	Quad Input/Output Fast Read (3B/4B)	EDh / EEh	EDh / EEh
Write	WREN	Write Enable	06h	06h
	WRDI	Write Disable	04h	04h
	PP	Page Program (3B/4B)	02h / 12h	02h / 12h
	-	Dual Input Fast Program (1-1-2)	-	A2h
	-	Dual I/O Fast Program (1-2-2)	-	D2h
	4PP	Quad Page Program (1-4-4) (3B/4B)	38h / 3Eh	38h / 3Eh
	SE	Sector Erase 4KB (3B/4B)	20h /21h	20h /21h
	BE 32K	Block Erase 32KB (3B/4B)	52h / 5Ch	52h
	SE 64K	Block Erase 64KB (3B/4B)	D8h / DCh	D8h / DCh
	-	Single Die Erase (64MB)	-	C4h
	CE	Chip Erase (1Gb)	60 or C7h	-
Register	RDSR	Read Status Register	05h	05h
	RDEAR	Read Extended Address Register	C8h	C8h
	WREAR	Write Extended Address Register	C5h	C5h
	WRSR	Write Status Register	01h	01h
	RFSR	Read Flag Status Register	-	70h
	CLFSR	Clear Flag Status Register	-	50h
	RDCR	Read Non-volatile Configuration Register	-	B5h
	-	Write Non-volatile Configuration Register	-	B1h
	-	Read Volatile Configuration Register	15h	85h
	-	Write Volatile Configuration Register	-	81h
	-	Read Enhance Volatile Configuration Register	-	65h
	-	Write Enhance Volatile Configuration Register	-	61h

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Comparing Micron MT25QL01GB with Macronix MX66L1G45G

Table 6-1: Command Code Comparison - Continued

Instruction Type	Instruction	Description	Macronix MX66L1G45G	Micron MT25QL01GB
QPI	EQIO	Enable QPI	35h	35h
	RSTQIO	Reset (Exit) QPI	F5h	F5h
	QPIID	QPI ID Read	AFh	AFh
OTP	ENSO	Enter Secured OTP	B1h	-
	EXSO	Exit Secured OTP	C1h	-
	ROTP	Read OTP Area	-	4Bh
	POTP	Program OTP Area	-	42h
Security	RDSCUR	Read Security Register	2Bh	-
	WRSCUR	Write Security Register	2Fh	-
	RDLR	Read Lock Register	2Dh	2Dh
	WRLR	Write to Lock Register	2Ch	2Ch
	RDPASS	Read Password Register	27h	27h
	WRPASS	Write Password Register	28h	28h
	PASSULK	Password Unlock	29h	29h
	RDSPB	Read SPB	E2h	E2h
	WRSPB	Write SPB	E3h	E3h
	ESSPB	Erase All SPB	E4h	E4h
	SPBLK	Set SPB Lock Bit	A6h	A6h
	RDSPBLK	Read SPB Lock Register	A7h	A7h
	RDDPB	Read DPB Register	E0h	E0h
	WRDPB	Write DPB Register	E1h	E1h
Others	PGM/ERS Suspend	Program or Erase Suspend	B0h	75h
	PGM/ERS Resume	Program or Erase Resume	30h	7Ah
	RSTEN	Reset Enable	66h	66h
	RST	Reset Memory	99h	99h
	EN4B	Enter 4-Byte Mode	B7h	B7h
	EX4B	Exit 4-Byte Mode	E9h	E9h
	DP	Deep Power Down	B9h	B9h
	RDP	Release from Deep Power Down	ABh	ABh
	CRC	Cyclic Redundancy Check	-	9Bh/27h
	SBL	Set Burst Length	C0h	*Note 1*

Note 1: Micron uses their Volatile Configuration Register to control this function.

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7. Manufacturer and Device ID

Table 7-1: Manufacturer and Device ID Comparison

Command Type		Macronix MX66L1G45G	Micron MT25QL01GB
Manufacture ID		C2h	20h
Device ID	Memory Type	20h	BBh
	Memory Capacity	1Bh	21h
Unique ID		N/A	17 Bytes

8. Summary

The Macronix MX66L1G45G and Micron MT25QL01GB have similar commands, functions, and features. The devices are command compatible for basic read, program, and erase operations. The devices are essentially pin compatible if the HOLD# function is not used. A more detailed analysis should be done if "special" functions such as XIP or Individual Sector Write Protection are used. If common features are used in standard traditional modes, they may need only minimal software modification primarily due to differences in register bit settings.

9. References

Table 9-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed Macronix specification, please refer to the Macronix Website at http://www.macronix.com/.

Table 9-1: Datasheet Version

Datasheet	Location	Date Issued	Version
MX66L1G45G, 3V, 1Gb, v0.0.pdf	Macronix Website	Dec. 2013	0.0
n25q_1gb_3V_65nm.pdf	Micron Website	Dec. 2013	A

10. Appendix

Table 10-1 shows the basic part number and package information cross reference between Macronix MX66L1G45G and Micron N25Q128 parts.

Table 10-1: Part Number Cross Reference

Macronix Part No.	Micron Part No.	Package	Dimension	Note
MX66L1G45GXDI-10G	MT25QL01GBBA1E120SIT	24-BGA	8x6mm pkg. 5X5ball array	Hold# pin
MX66L1G45GXDI-10G	MT25QL01GBBA3E120SIT	24-BGA	8x6mm pkg. 5X5ball array	Reset# pin
MX66L1G45GXDI-10G	MT25QL01GBBA8E120SIT	24-BGA	8x6mm pkg. 5X5ball array	Reset# and Hold# pin

11. Revision History

Revision	Description	Date
1.0	Initial Release	January 20, 2014

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Comparing Micron MT25QL01GB with Macronix MX66L1G45G

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