1.8V, 1G/2G-bit Serial NAND Flash Memory

MX35UFxGE4AC

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1. FEATURES

- **1Gb/2Gb Serial Flash**
  - Bus: x4
  - Page size: (2048+64) byte,
  - Block size: (128K+4K) byte
- **Fast Read Access**
  - Supports Random data read out by x1 x2 & x4 modes, (1-1-1,1-1-2, 1-1-4, 1-2-2, 1-4-4)[Note 1]
  - Latency of array to register: 80us
  - Frequency: 104MHz
  - Continuous read supported
- **Page Program Operation**
  - Page program time: 360us(typ.)
- **Block Erase Operation**
  - Block erase time: 1ms (typ.)
- **Single Voltage Operation:**
  - VCC: 1.7 to 1.95V
- **BP bits for block group protection**
- **Unique ID Read**
- **Low Power Dissipation**
  - Max 40mA
  Active current (Read/Program/Erase)
- **Standby Mode**
  - 110uA (Max) standby current
- **High Reliability**
  - Program / Erase Endurance: Typical 100K cycles with 4-bit ECC per (512+16) Byte
  - Flexible ECC Bit Flip Threshold Setting by user
  - Data Retention: 10 years
- **BBM Table (Bad Block Table) supported**
- **Wide Temperature Operating Range**
  -40˚C to 85˚C
- **Package:**
  1) 8-WSON (8mm x 6mm)
  2) 24-Ball BGA (6x8mm, 5x5 ball array)
  All packaged devices are RoHS Compliant and Halogen-free.

***Note 1**. Which indicates the number of I/O for command, address and data.*

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2. GENERAL DESCRIPTIONS

The MX35UFxGE4AC is a 1.8V 1Gb/2Gb SLC NAND Flash memory device with Serial interface; also with some particular features, such as: Continuous read, Bad Block Management table support, Flexible ECC Bit Flip Threshold Setting by user, Read ECC warning page address support (for Continuous Read mode).

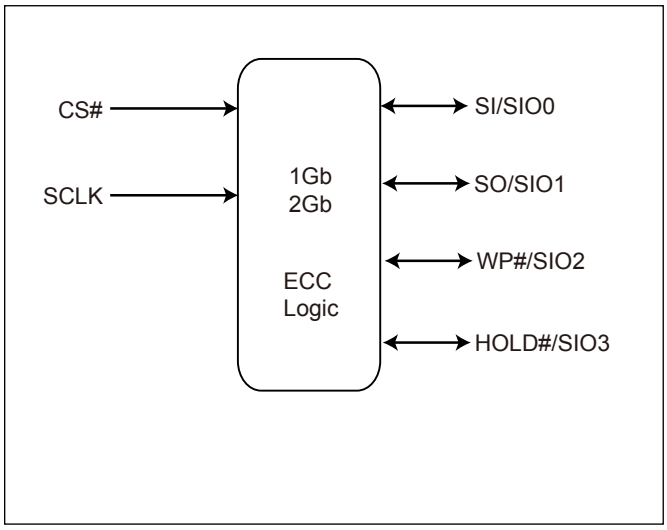
The memory array of this device adopted the same cell architecture as the parallel NAND, however implementing the industry standard serial interface.

An internal 4-bit ECC logic is implemented in the chip, which is enabled by default. The internal ECC can be disabled or enabled again by command. When the internal 4-bit ECC logic is disabled, the host side needs to handle the 4-bit ECC by host micro controller.

The device supports conventional read mode and continuous read modes. If the configuration register bit "CONT" = 0, the device is in conventional read mode which user cannot read across a page without page read command. If the configuration register bit "CONT" = 1, the device is in continuous read mode which user can read consecutive page across page boundary without next page read command.

Considering user effort reduction, the device provides 40 links of BBM(Bad Block Management), which can provide the continuous good blocks to save software effort and increase read throughput. Moreover, user may enhance the P/E endurance cycle of single block by using more than one BBM links for block replacement to same single block. For example, using two BBM links for same single block replacement which may double the P/E cycle of the same single block, using three BBM links may get triple P/E cycle and so on.

Figure 1. Logic Diagram

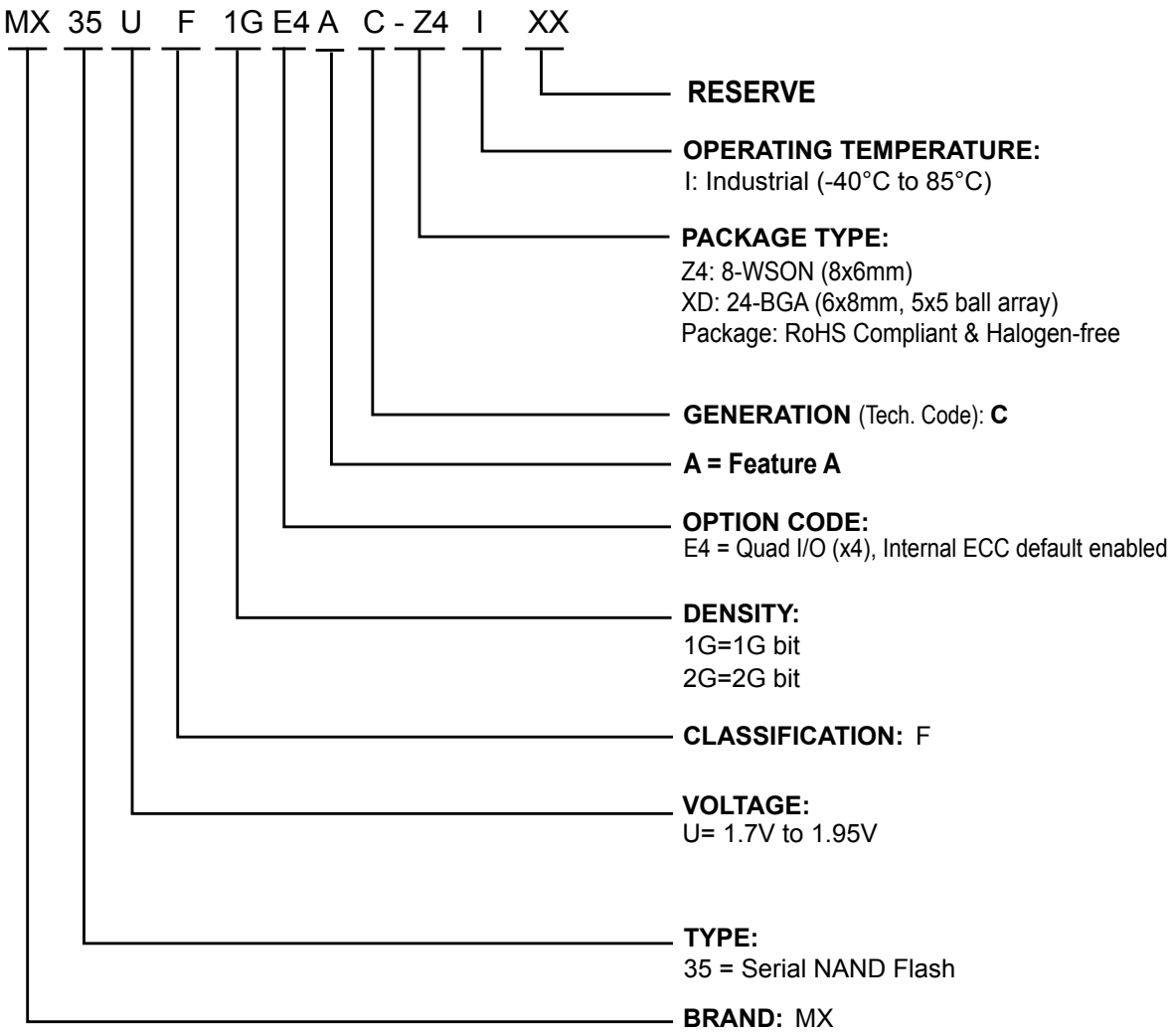


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3. ORDERING INFORMATION

Part Name Description

Macronix's NAND flash are available in different configurations and densities. Verify valid part numbers by using Macronix's product search at http://www.Macronix.com. Contact Macronix sales for devices not found.



Please contact our regional sales for the latest product selection and available form factors.

Part Number	Density	Organization	VCC Range	Package	Temperature Grade
MX35UF1GE4AC-Z4I	1Gb	x4	1.8V	8-WSON	Industrial
MX35UF1GE4AC-XDI*	1Gb	x4	1.8V	24-BGA	Industrial
MX35UF2GE4AC-Z4I	2Gb	x4	1.8V	8-WSON	Industrial
MX35UF2GE4AC-XDI*	2Gb	x4	1.8V	24-BGA	Industrial

** Advanced information*

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4. BALL ASSIGNMENT AND DESCRIPTIONS

Figure 2. 8-WSON (8x6mm)

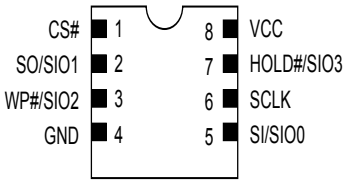
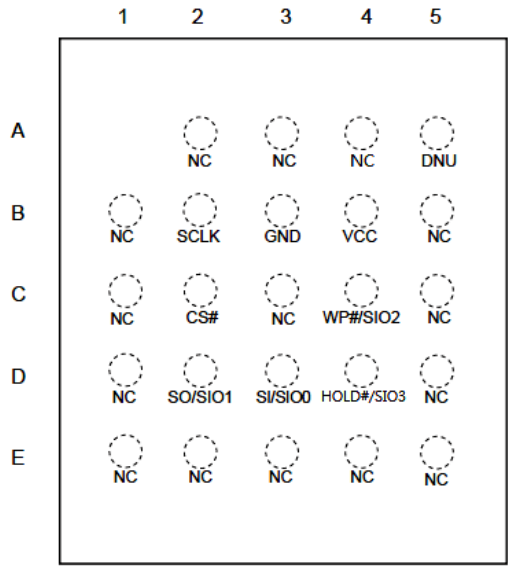


Figure 3. 24-Ball BGA (5x5 Ball Array)



5. PIN DESCRIPTIONS

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (For 1-1-2,1-1-4, 1-2-2, or 1-4-4 note1 mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (For 1-1-2,1-1-4, 1-2-2, or 1-4-4 note1 mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (For 1-1-4 or 1-4-4note1 mode)
HOLD#/ SIO3	Hold or Serial Data Input & Output (For 1-1-4 or 1-4-4note1 mode)
VCC	1.8V Power Supply
GND	Ground
DNU	Do Not Use
NC	Not Connected Internally

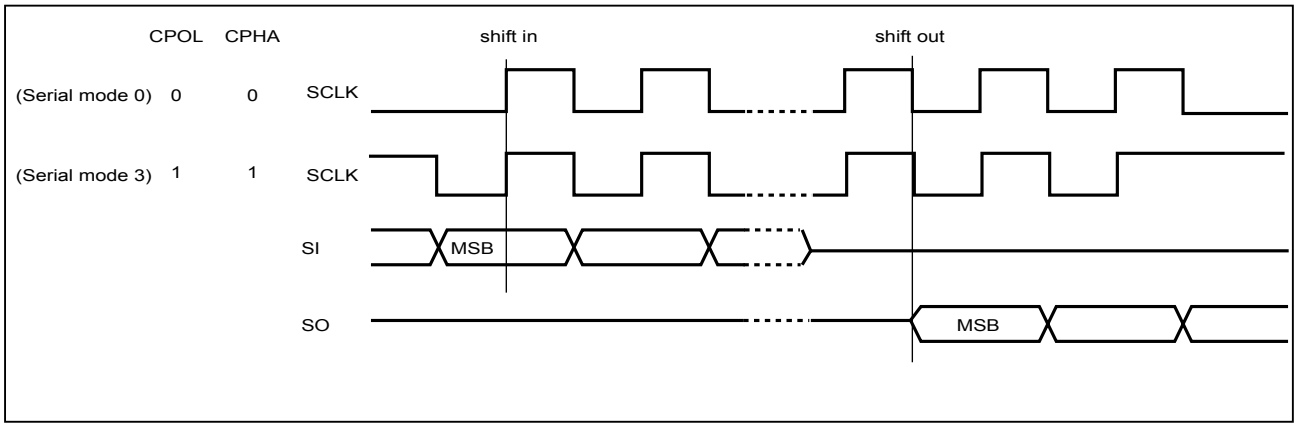
***Note 1**. Which indicates the number of I/O for command, address, and data.*

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6. DEVICE OPERATION

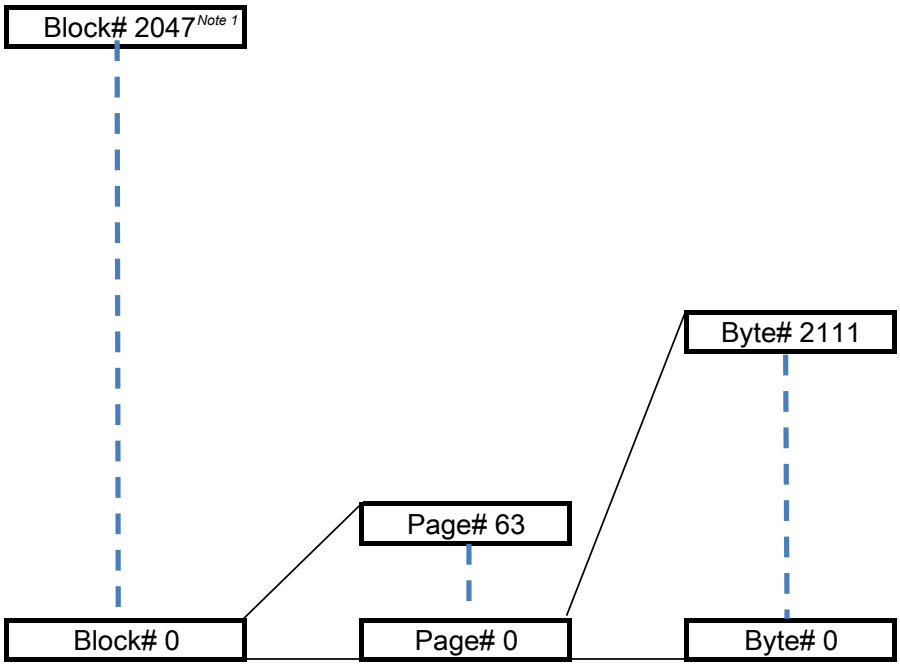
1. Before a command is issued, status register should be checked via get features operations to ensure device is ready for the intended operation.
2. When an incorrect command is written to this device, it enters standby mode and stays in standby mode until the next CS# falling edge. In standby mode, This device's SO pin should be High-Z.
3. When a correct command is written to this device, it enters active mode and stays in active mode until the next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as **"Figure 4. Serial Mode Supported"**.
5. While a Write Status Register, Program, or Erase operation is in progress, access to the memory array is ignored and will not affect the current operation of Write Status Register, Program, or Erase.

Figure 4. Serial Mode Supported



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7. ADDRESS MAPPING



Block address	Page address	Byte address
2Gb: RA[16:6] 1Gb: RA[15:6]	RA [5:0]	CA [11:0]

Note 1: *2047 for 2Gb, 1023 for 1Gb*

Table 1. RADD Definition

RADD	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RADD2	L	L	L	L	L	L	L	RA[16]Note1
RADD1	RA[15]	RA[14]	RA[13]	RA[12]	RA[11]	RA[10]	RA[9]	RA[8]
RADD0	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]

Note 1: *RA[16] is for 2Gb*

L: Low

Table 2. CADD Definition (Read From Cache Related Command)

CADD	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CADD1	L	L	L	L	CA[11]	CA[10]	CA[9]	CA[8]
CADD0	CA[7]	CA[6]	CA[5]	CA[4]	CA[3]	CA[2]	CA[1]	CA[0]

L: Low

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8. COMMAND DESCRIPTION

Table 3. Command Set - Standard Operation

(SPI_NOR_EN = 0, CONT = 0)[Note1]

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	7th Byte	8th Byte
Get Feature	0Fh	ADD	Data					
Read Status	05h	Data						
Set Feature	1Fh	ADD	Data					
Page Read	13h	RADD2	RADD1	RADD0				
Page Read Cache Random	30h	RADD2	RADD1	RADD0				
Page Read Cache Sequential	31h							
Page Read Cache End	3Fh							
Read From Cache x1	03h	CADD1	CADD0	DUMMY	DATA~			
Read From Cache x1 (Alternative)	0Bh	CADD1	CADD0	DUMMY	DATA~			
Read From Cache x2[Note4]	3Bh	CADD1	CADD0	DUMMY	DATA~[*2]			
Read From Cache x4[Note4]	6Bh	CADD1	CADD0	DUMMY	DATA~[*4]			
Read From Cache Dual IO 1-2-2[Note4]	BBh	CADD1[*2]	CADD0[*2]	DUMMY[*2]	DATA~[*2]			
Read From Cache Quad IO 1-4-4[Note4]	EBh	CADD1[*4]	CADD0[*4]	DUMMY[*4]	DUMMY[*4]	DATA~[*4]		
Read ID	9Fh	DUMMY	MID	DID1	DID2			
Block Erase	D8h	RADD2	RADD1	RADD0				
Program Execute	10h	RADD2	RADD1	RADD0				
Program Load x1	02h	CADD1	CADD0	DATA~				
Program Load Random Data x1	84h	CADD1	CADD0	DATA~				
Program Load x4[Note4]	32h	CADD1	CADD0	DATA~[*4]				
Program Load Random Data x4[Note4]	34h	CADD1	CADD0	DATA~[*4]				
Write Enable	06h							
Write Disable	04h							
Reset	FFh							
Read ECCSR	7Ch	DUMMY	SR_ECC					
Write BBM	A1h	LBA	LBA	PBA	PBA			
Read BBM[Note2]	A5h	DUMMY	LBA0	LBA0	PBA0	PBA0	LBA1	LBA1~
ECC Warning Page Address[Note3]	A9h	DUMMY	RADD2_L	RADD1_L	RADD0_L	RADD2_F	RADD1_F	RADD0_F

Notes:

1. The device supports different feature configurations by configuration register bits. This command table is for standard operation (SPI_NOR_EN = 0, CONT = 0); for details of SPI_NOR_EN, CONT bits, please refer to the relative sections.

2. A5h command may read the 40 links of BBM_table (LBAx/PBAx)

3. RADDx_L: Last Warning Page Address, RADDx_F: First Warning Page Address

*4. *2 stands for the dual I/O phase and *4 for quad I/O mode*

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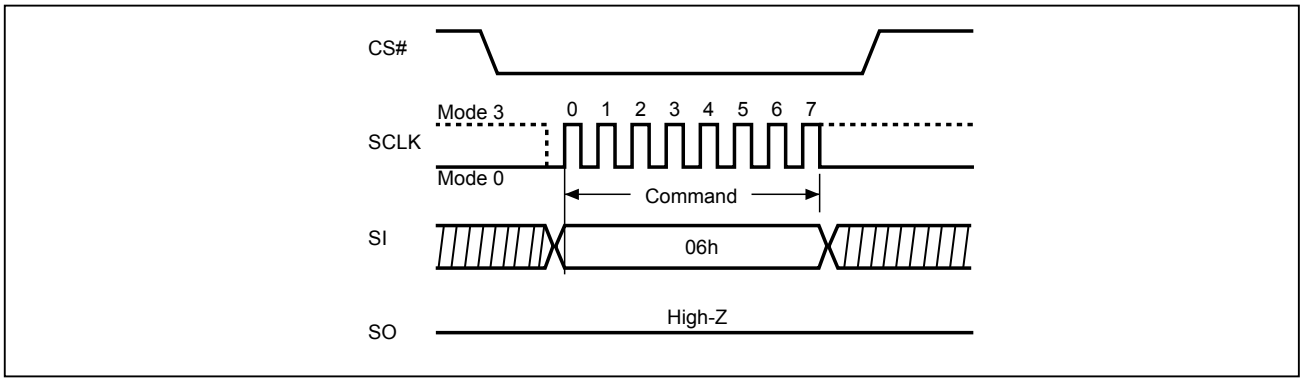
8-1. WRITE Operations

8-1-1. Write Enable

The Write Enable (WREN, 06h) instruction sets the Write Enable Latch (WEL) bit. Instructions like Page Program, Secure OTP program, Block Erase, and Write BBM that are intended to change the device content, should be preceded by the WREN instruction.

The sequence of issuing WREN instruction is: CS# goes low→send WREN instruction code→ CS# goes high.

Figure 5. Write Enable (WREN) Sequence



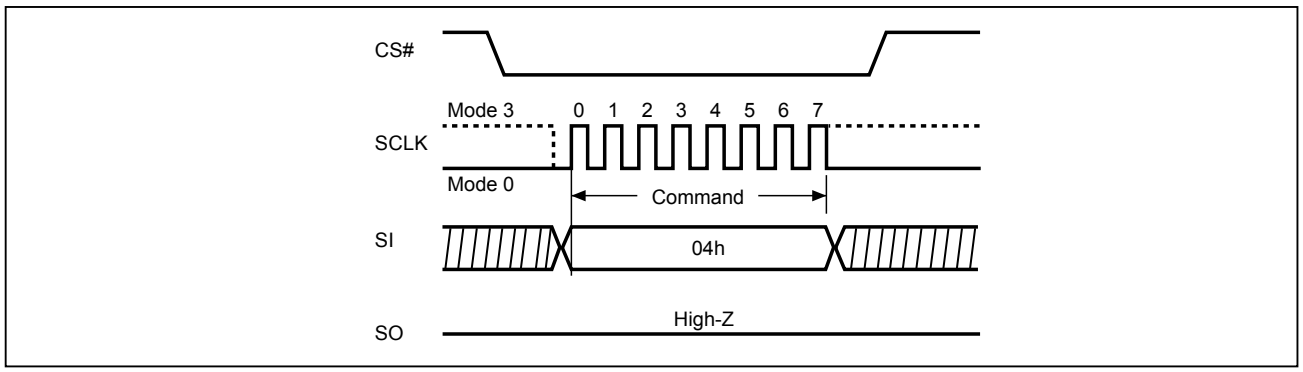
8-1-2. Write Disable (04h)

The Write Disable (WRDI) instruction resets the Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→send WRDI instruction code→CS# goes high. It disables the following operations:

- Block Erase
- Secure OTP program
- Page program
- Write BBM

Figure 6. Write Disable (WRDI) Sequence



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8-2. Feature Operations

8-2-1. GET Feature (0Fh) and SET Feature (1Fh)

By issuing a one byte address into the feature address, the device may then decide if it's a feature read or feature modification. (0Fh) is for the "GET FEATURE"; (1Fh) is for the "SET FEATURE".

The RESET command (FFh) will clear the status register, the other feature registers remain until the power is being cycled or modified by the settings in the table below. After a RESET command (FFh) is issued, the Status register OIP bit0 or CRBSY will go high. These bits can be polled to determine when the Reset operation is complete, as it will return to the default value (0) after the reset operation is finished. Issuing the RESET command (FFh) has no effect on the Block Protection and Configuration registers.

The Block Protection and Configuration registers will return to their default state after a power cycle, and can also be changed using the Set Feature command. Issuing the Get Feature command to read the selected register value will not affect register content.

Table 4. Configuration Registers

ADD	Register		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
10h	Configuration	bit name	BFT3	BFT2	BFT1	BFT0				ENPGM	F0h
		type	V2	V2	V2	V2				V	
60h	Configuration	bit name							SPI_NOR_EN	OTPRWSP	00h
		type							OTP	OTP	
A0h	Block Protection	bit name	BPRWD[note1]		BP2	BP1	BP0	Invert	Comp.	SP[note2]	38h
		type	V		V	V	V	V	V	V	
B0h	Configuration	bit name	OTP_PROT	OTPEN		ECC_EN		CONT		QE	10h
		type	V	V		V		V2		V	
C0h	Status	bit name	CRBSY	BBMT_F	ECC_S1	ECC_S0	P-FAIL	E-FAIL	WEL	OIP	00h
		type	V	V	V	V	V	V	V	V	
E0h	Configuration	bit name	DS_IO[1]	DS_IO[0]							00h
		type	V2	V2							

V: Volatile

V2: Volatile, The default value of these volatile feature bits can be changed once by special OTP Configuration Register program operation

OTP: One time setting

Notes:

1. *If BPRWD is enabled and WP# is LOW, then the block protection register can not be changed.*
2. *SP bit is for Solid-protection. Once the SP bit sets as 1, the rest of protection bits (BPx bits, invert bits, complementary bits)cannot be changed during the current power cycle.*
3. *This is the shipment power on default value, user can change the default value of registers of OTP/V2 type by Special OTP Configuration Register Program Operation.*
4. *All the reserved bits must keep low including the undefined register.*

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Table 5. Register status of Reset (FFh) command operation

Registers	Status	
	'CONT'=1	'CONT'=0
ECC_S[1:0]	***Kept***	Clear
P-FAIL	Clear	Clear
E-FAIL	Clear	Clear
WEL	Clear	Clear
OIP	Ready/busy status	Ready/busy status
CRBSY	Ready/busy status	Ready/busy status
Other V type	***Kept***	***Kept***
Other V2 type	***Kept***	***Kept***
OTP types	***Kept***	***Kept***

Notes: *"Clear" means to return to power-on value, and "Kept" means to keep the status before the Reset.*

Table 6. I/O Strength Feature Table

DS_IO[1]	DS_IO[0]	Drive Strength
0	0	normal (Default, 25 ohm typical)
0	1	underdrive 1 (35 ohm typical)
1	X	underdrive 2 (85 ohm typical)

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Figure 7. GET FEATURE (0Fh) Timing

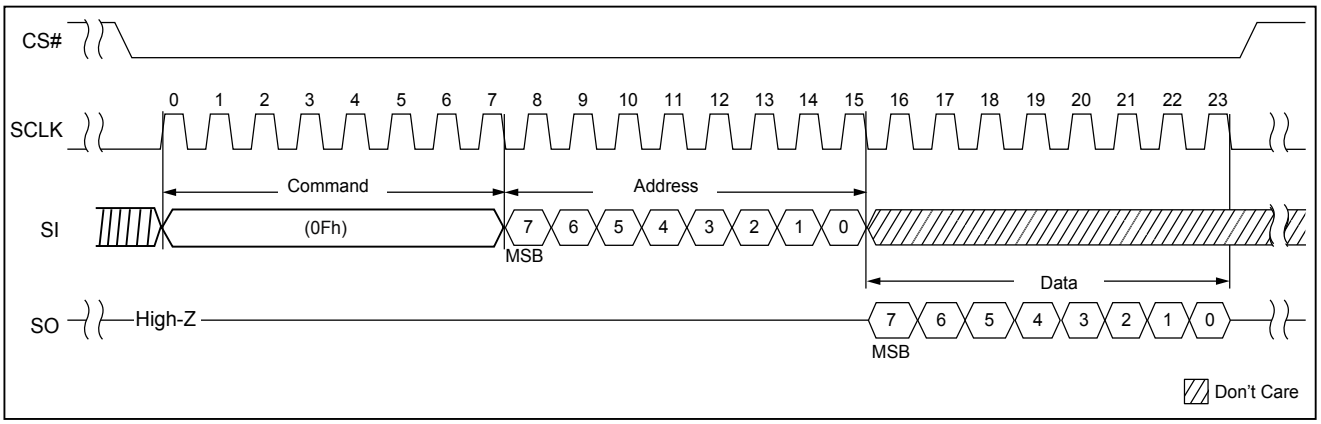
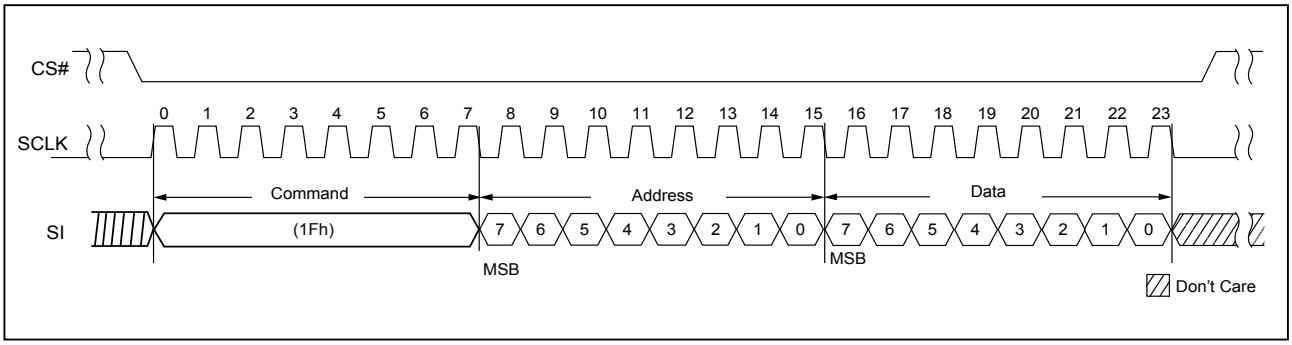


Figure 8. SET FEATURE (1Fh) Timing



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8-3. READ Operations

The device supports "Power-on Read" function, after power up, host may issue the Read From Cache command, and the device will automatically load the data of the 1st page of 1st block from array to cache. The host micro-controller may directly read the data from the cache buffer.

The device supports conventional read mode and continuous read modes. If the configuration register bit “CONT” = 0, the device is in conventional read mode. The page read operation and page read cache Random/ sequential operation is supported in the conventional read mode. If the configuration register bit “CONT” = 1, the device is in continuous read mode and only continuous read operation is supported. During the continuous read mode, the page read cache related commands are not supported. (page cache sequential (31h), page read cache random (30h) and page read cache end (3Fh)).

Table 7. Supported Read Command Table for Different Modes

Read command	Command Code	Read Mode	
		Conventional Read Mode	Continuous Read Mode
Page Read	13h	V	V
Page Read Cache Random	30h	V	
Page Read Cache Sequential	31h	V	
Page Read Cache End	3Fh	V	

Table 8. Data Output Range Per Page

Configuration Register Bit "CONT"	Read Mode	Data Length per Page
CONT=0	Conventional Read mode	2048+64
CONT=1	Continuous Read mode	2048

8-3-1. PAGE READ (13h)

The page read operation transfers data from array to cache by issuing the page read (13h)command followed by the 24-bit address (including the dummy/block/page address).

The device will have a period of time (tRD) being busy after the CS# goes high. The 0Fh (GET FEATURE) may be used to poll the operation status.

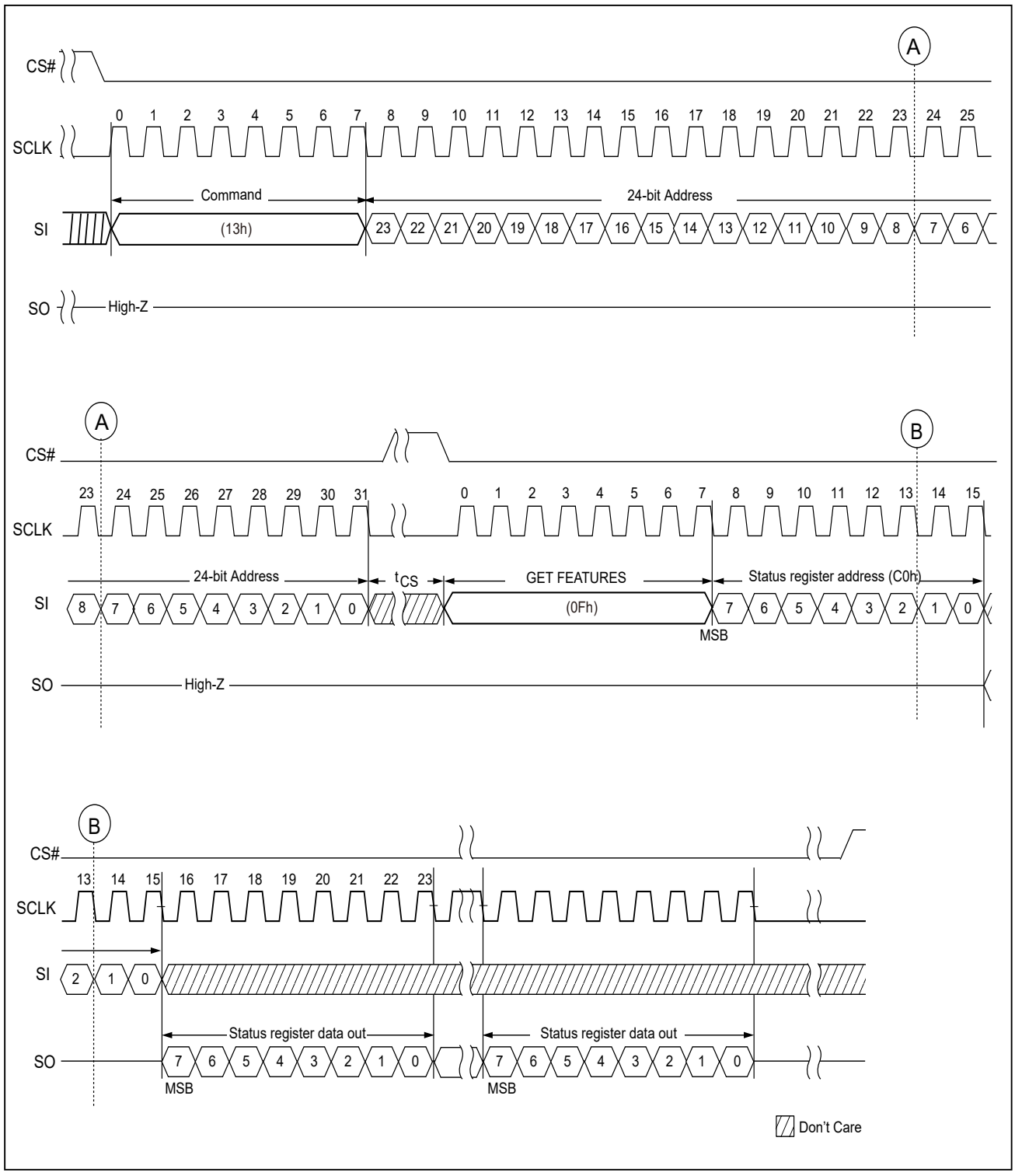
After read operation is completed, the RANDOM DATA READ (03H or 0Bh), Read from cache (x2) (3Bh), Read from cache (x4) (6Bh), read from cache dual IO (1-2-2) (BBh) and Read from cache Qual IO (1-4-4) (EBh) may be issued to fetch the data.

8-3-2. QE bit

The Quad Enable (QE) bit, volatile bit, while it is "0" (factory default), it performs non-Quad and WP#, HOLD# are enabled. While QE is "1", it performs Quad I/O mode and WP#, HOLD# are disabled. In another word, if the system goes into four I/O mode (QE=1), the feature of Hardware Protection Mode(HPM) and HOLD# will be disabled. Upon power cycle, the QE bit will go into the factory default setting "0".

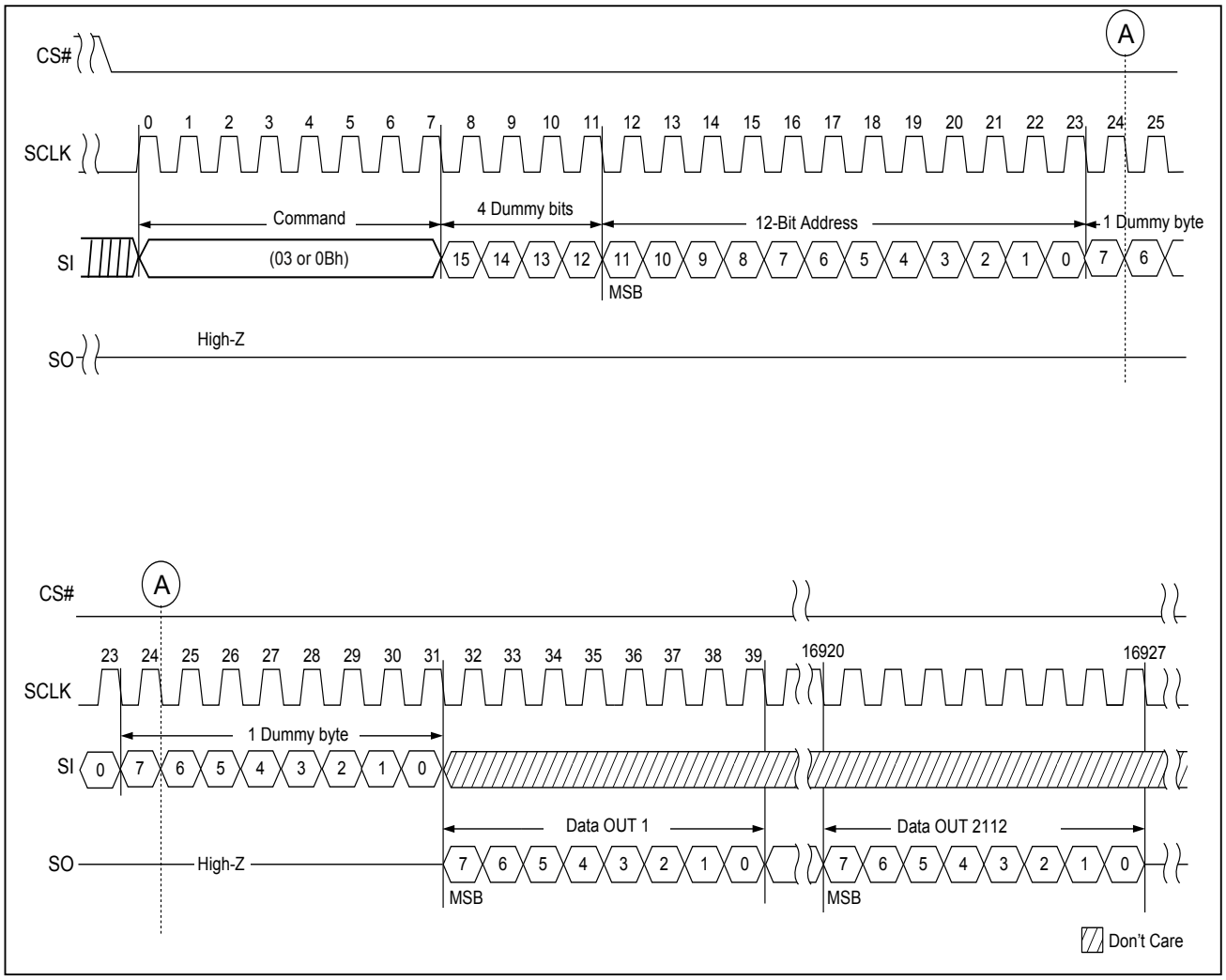
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Figure 9. PAGE READ (13h) Timing x1



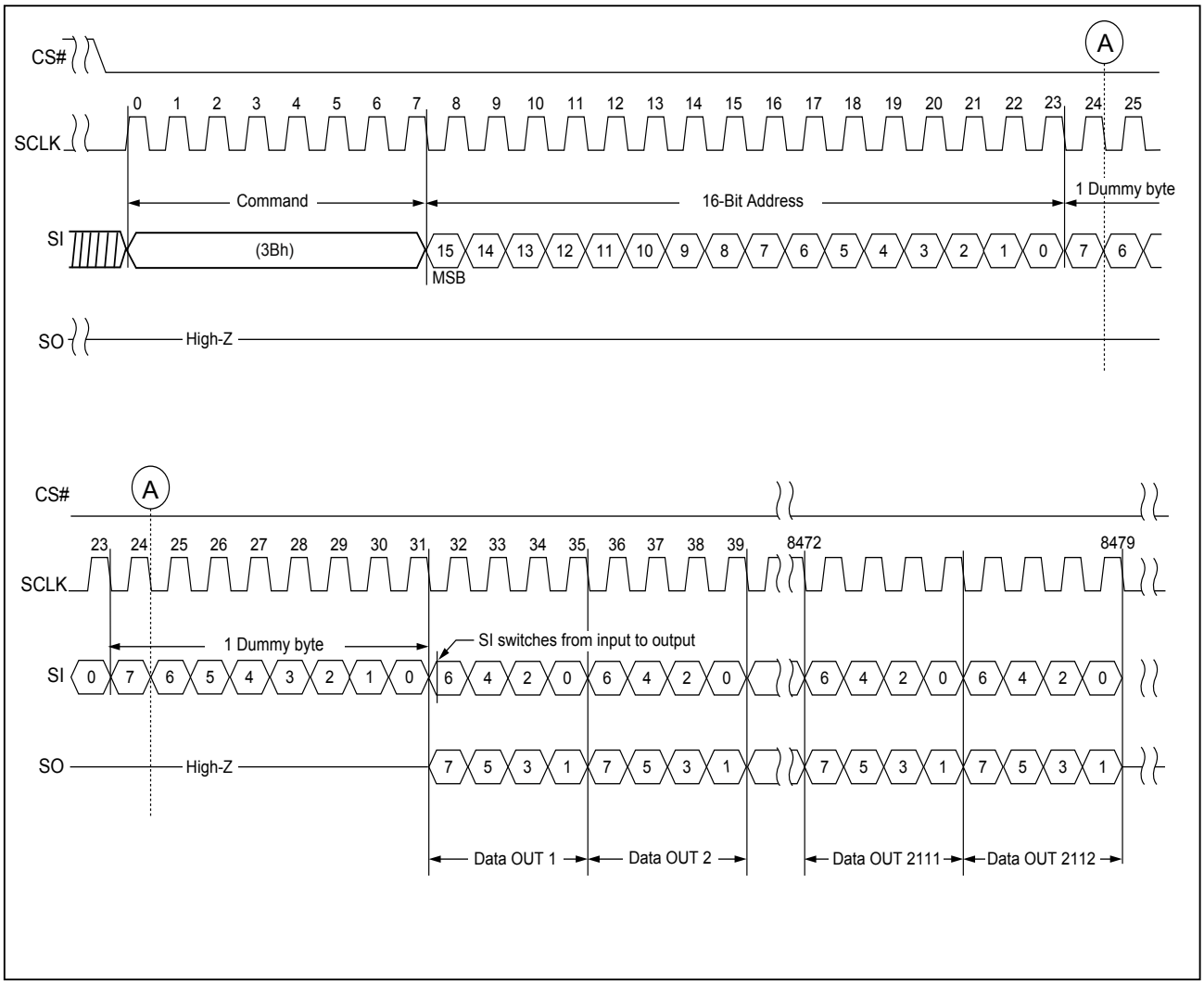
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Figure 10. READ FROM CACHE (03h or 0Bh) Timing



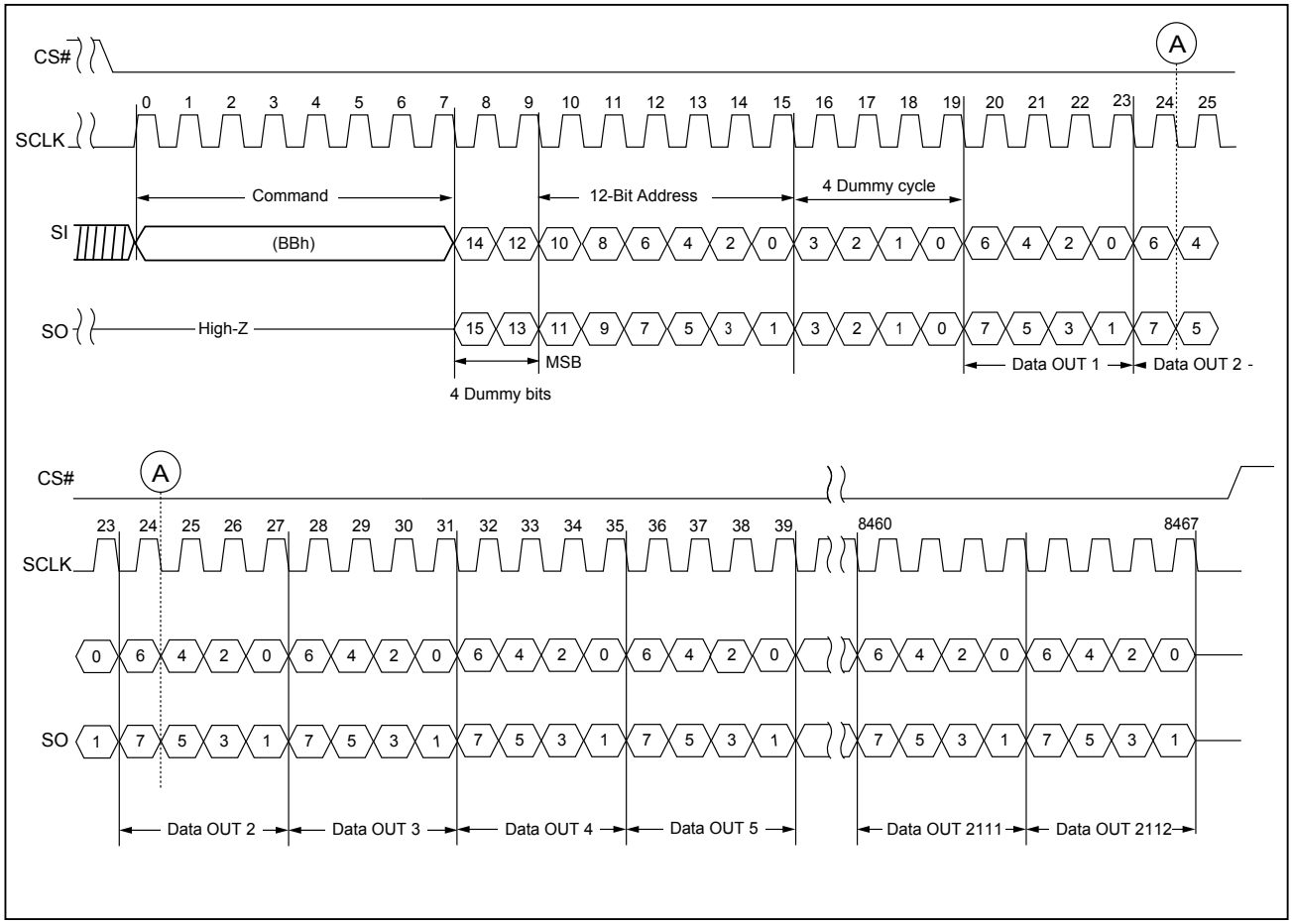
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Figure 11. READ FROM CACHE x 2



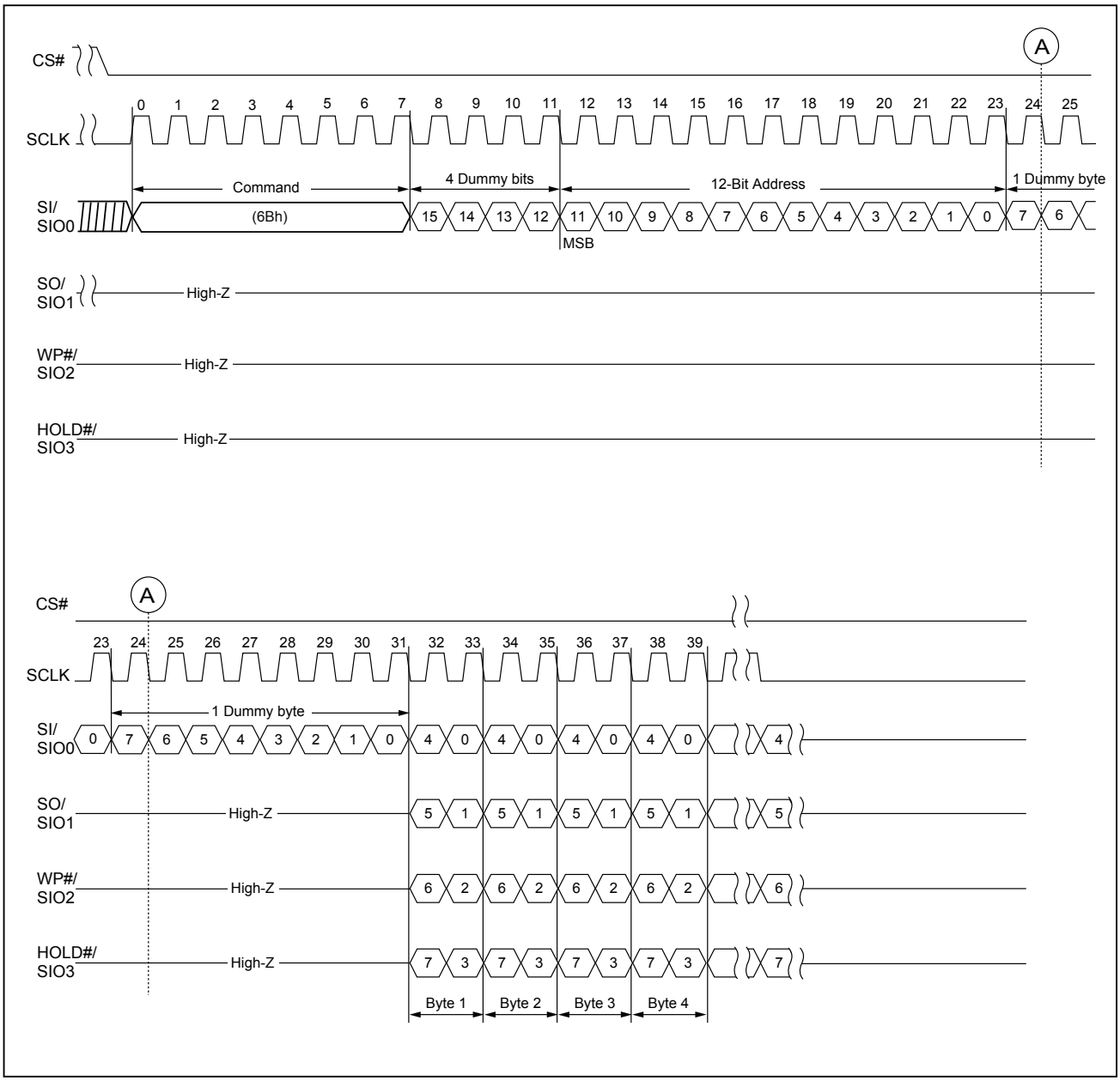
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Figure 12. Read From Cache Dual IO 1-2-2



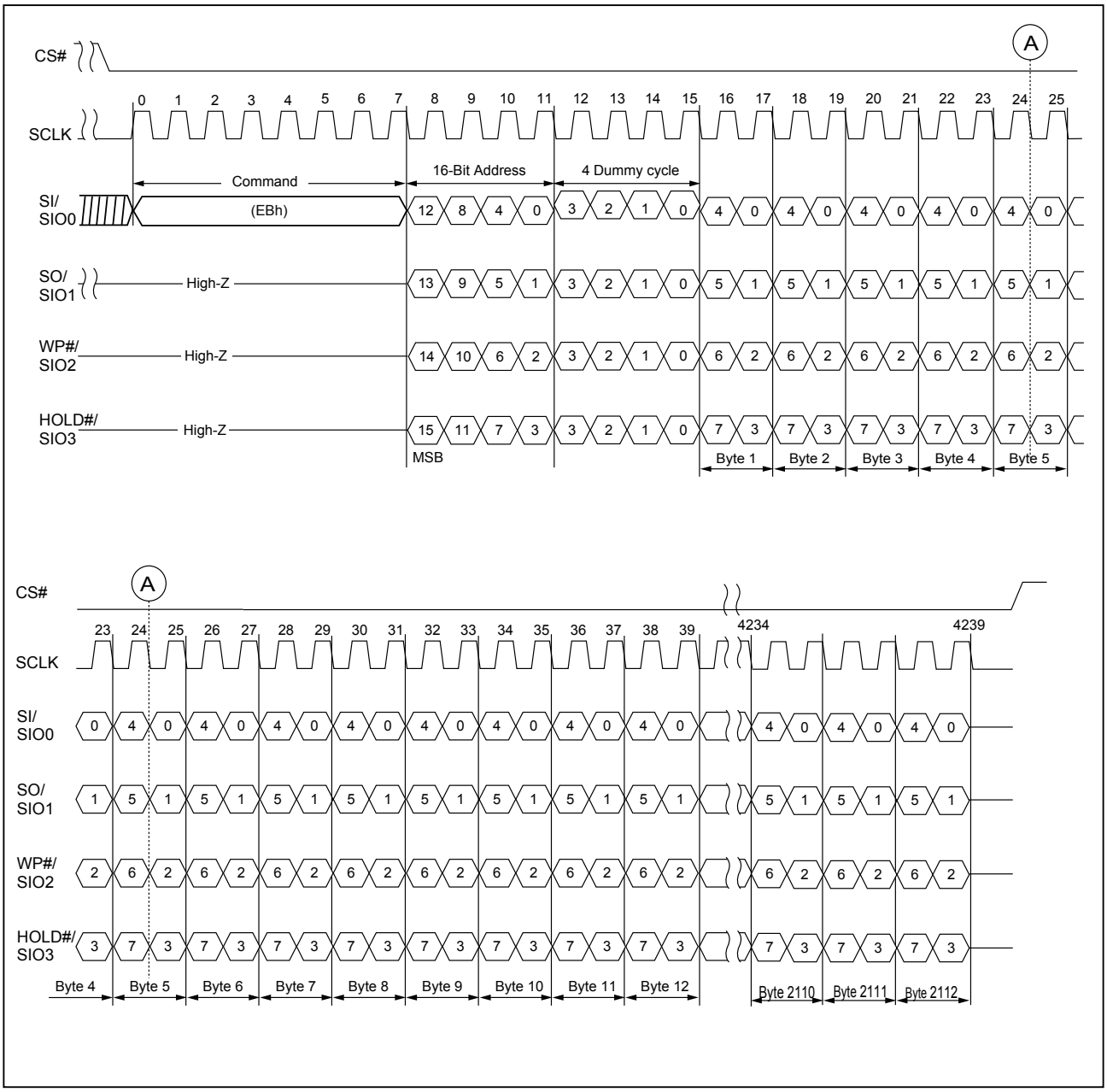
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Figure 13. READ FROM CACHE x 4



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Figure 14. Read From Cache Quad IO 1-4-4



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8-3-3. Page Read Cache Random (30h)/Page Read Cache Sequential (31h)/Page Read Cache End (3Fh)

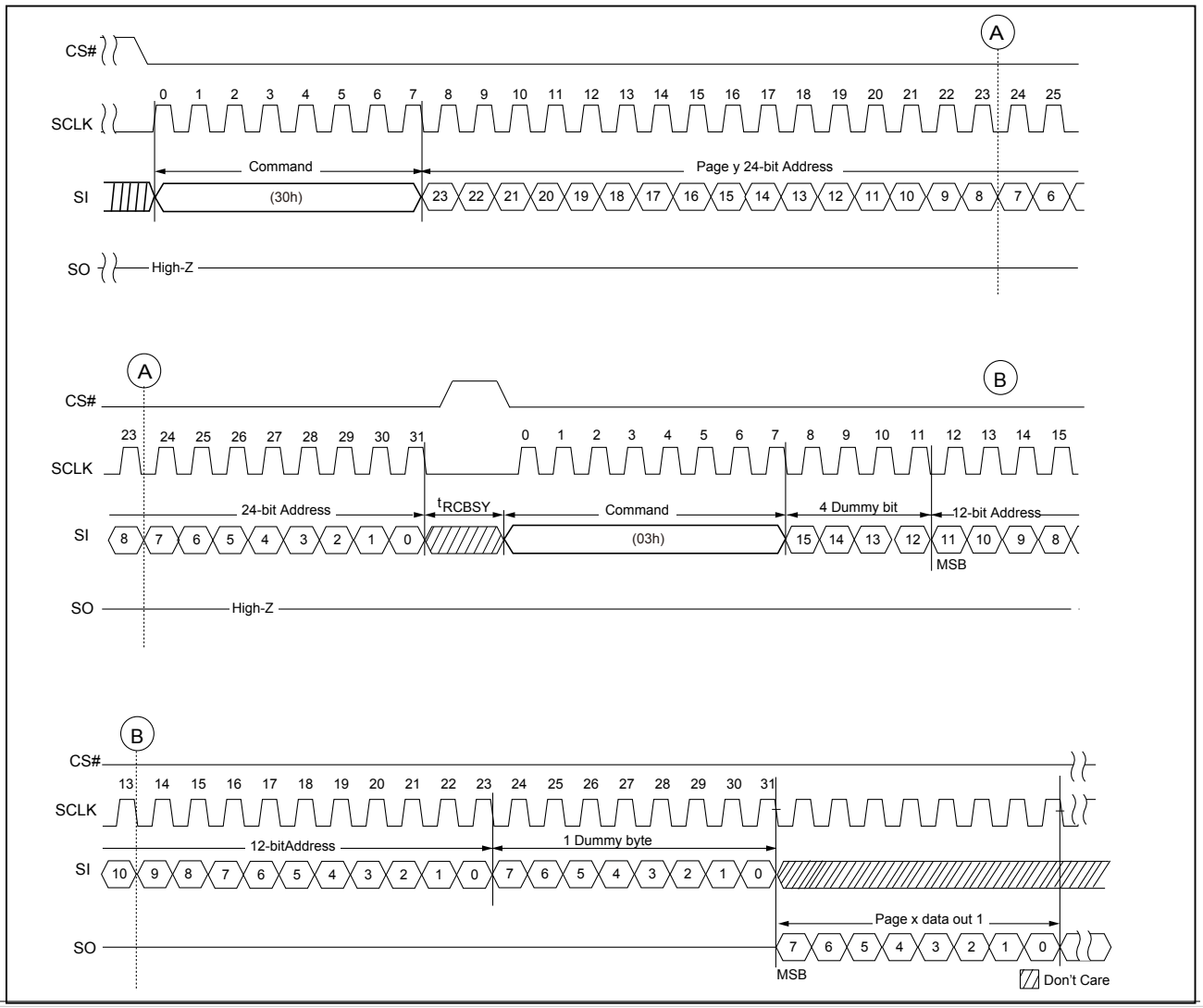
The page read cache sequential operation is for throughput enhancement by using the internal cache buffer. It allows the consecutive pages to be read-out without giving next page address, which reduces the latency time from tRD to tRCBSY between pages or blocks. While the data is read out on one page, the data of next page can be read into the cache buffer.

After writing the 13h command and giving the 24-bit address, the device will have a period of time (tRD) being busy after the CS# goes high. The 0Fh (GET FEATURE) or 05h (RDSR) may be used to poll the operation status. After the status of successfully completed, following the page read cache sequential (31h) or the page read cache random (30h) command being sent to Serial Flash device; the Serial Flash device will be at a busy time of tRCBSY for the next page data transferring to cache. And then following the cache read command (03h/0Bh/3Bh/6Bh/BBh/EBh) may get the prior page data output from cache at the same time.

To confirm the last page to be read-out during the cache read sequential operation, a 3Fh command is needed to replace the 31h or 30h command prior to the last data-out.

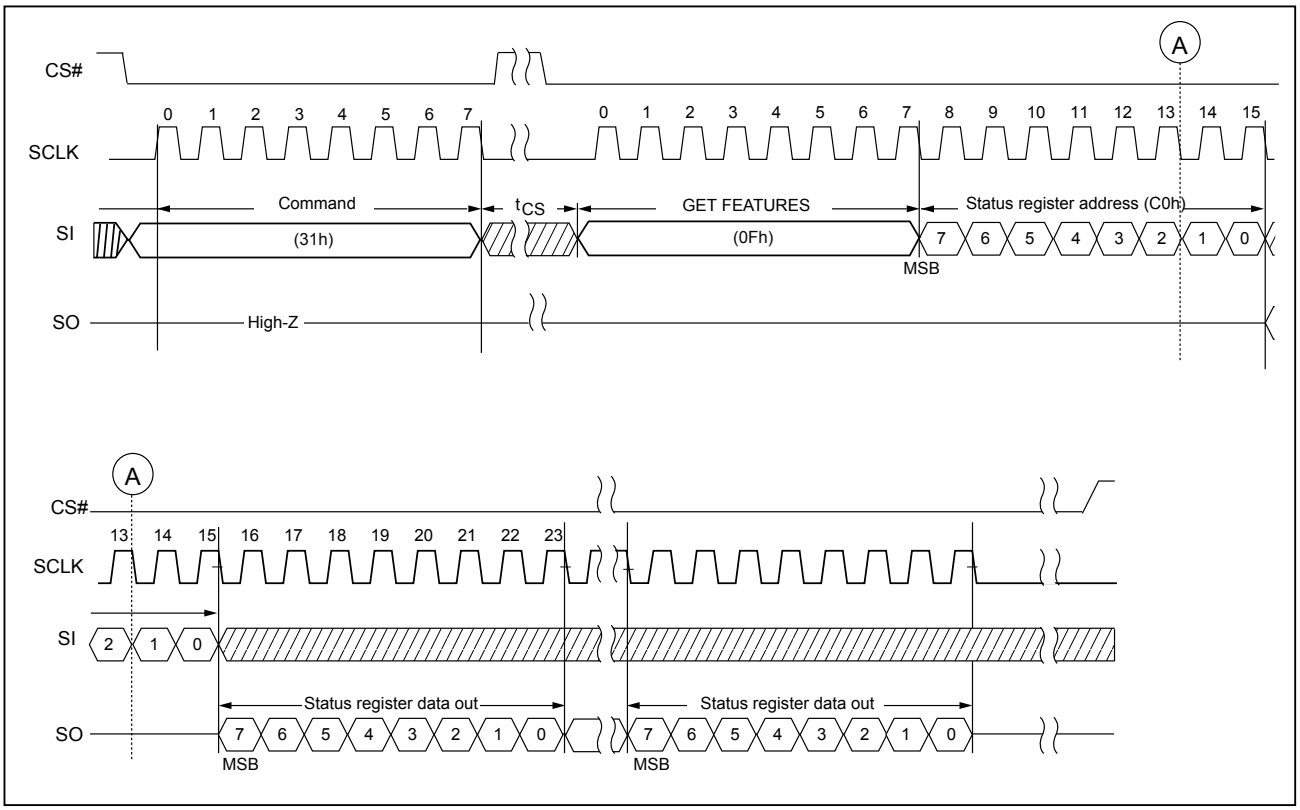
The PAGE READ CACHE SEQUENTIAL command is also valid for the consecutive page cross block.

Figure 15. Page Read Cache Random (30h)



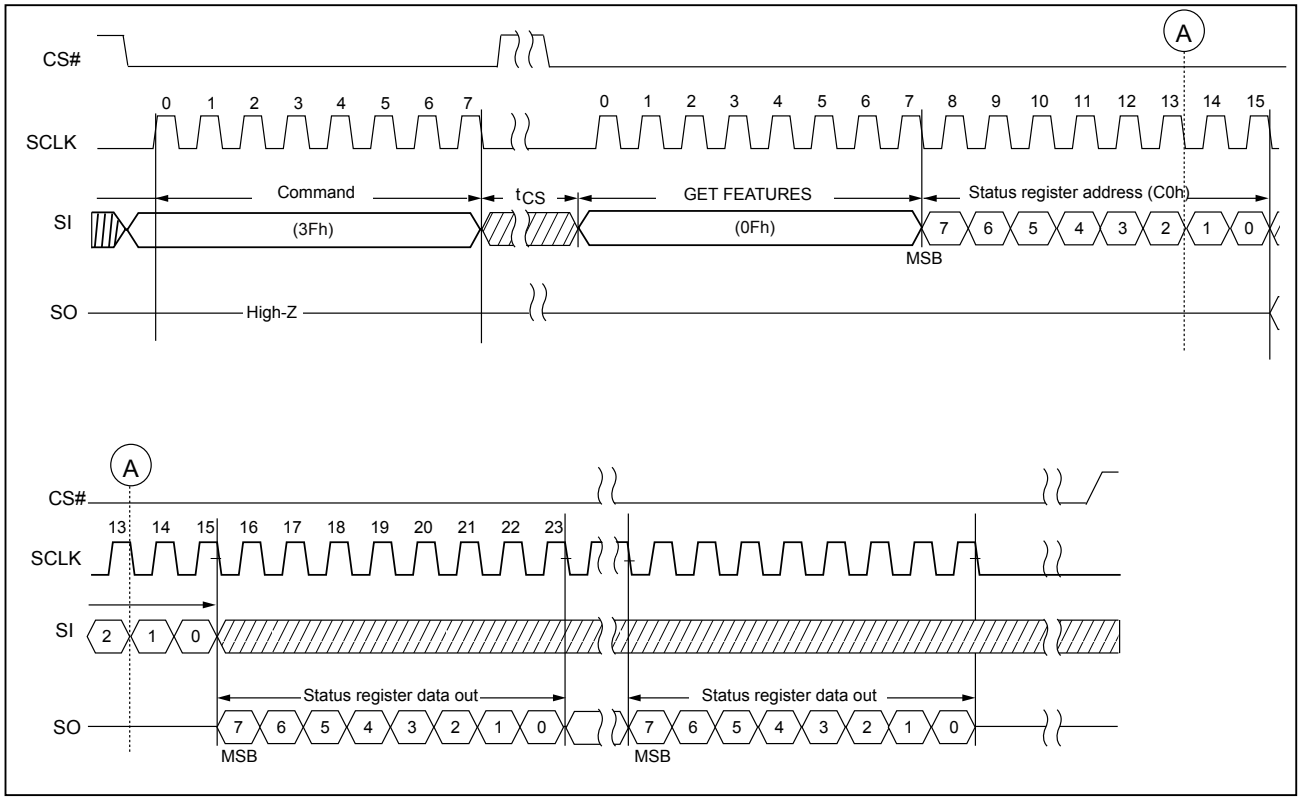
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Figure 16. Page Read Cache Sequential (31h)



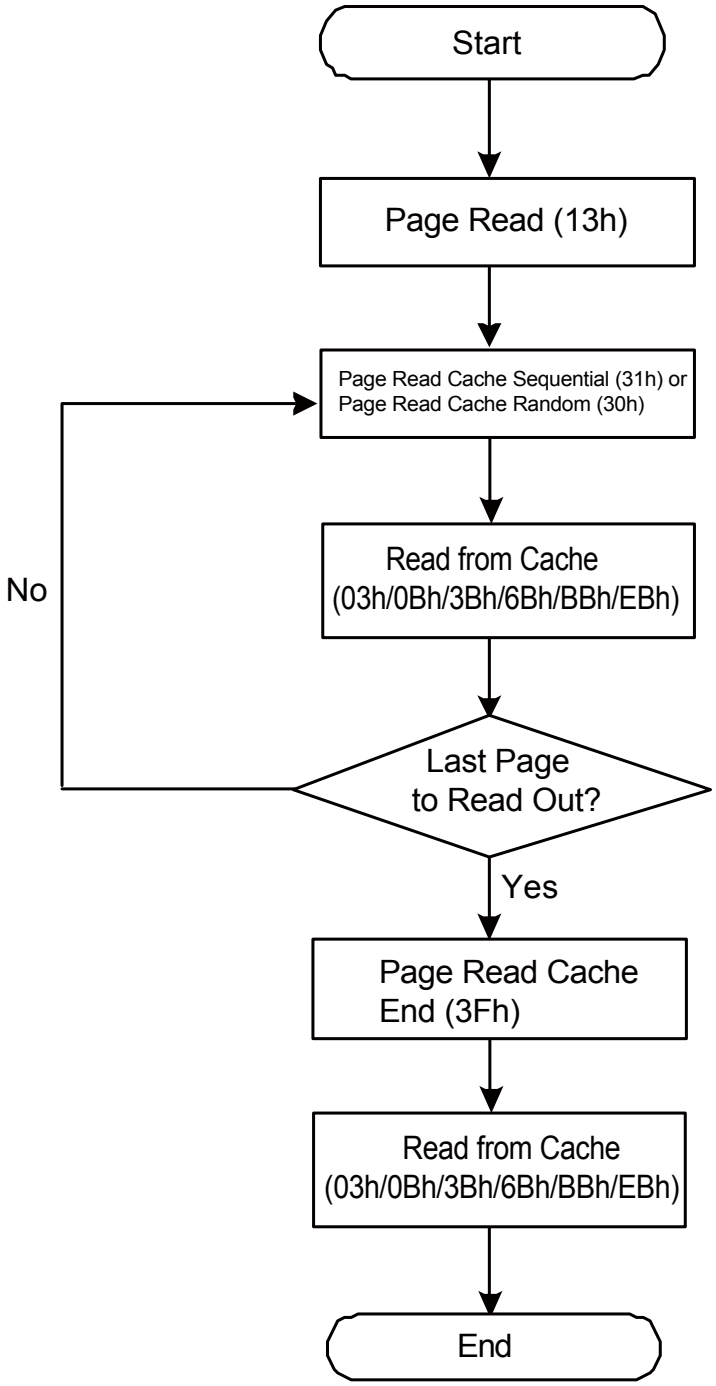
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Figure 17. Page Read Cache End (3Fh)



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Figure 18. Page Read Cache Flow



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8-3-4. Continuous Read Operation

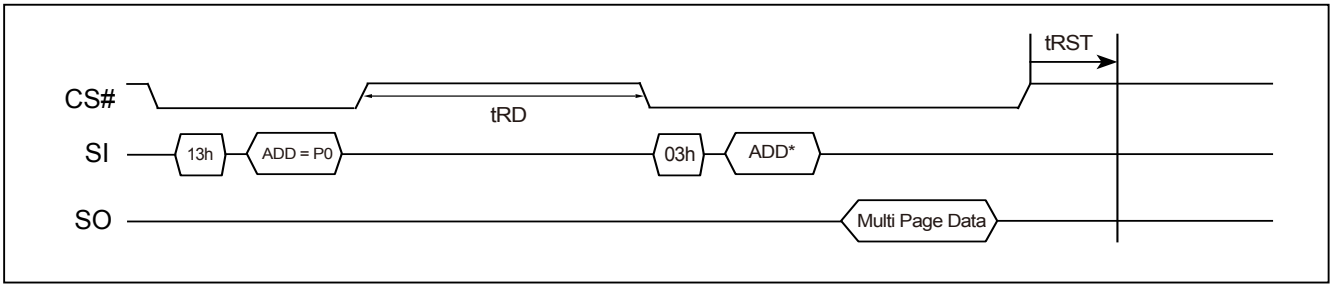
This device also supports the continuous read operation which allows the host to read out the data continuously from page to page with just first read latency.

The continuous read operation including: firstly, starting with the page read command and the 1st page data will be read into the cache after the read latency tRD. Secondly, Issuing the Read From Cache commands (03h/0Bh/3Bh/6Bh/BBh/EBh) to read out the data from cache continuously.

After all the data is read out, the host should pull CS# high to terminate this continuous read operation and wait a 6us of tRST for the NAND device resets read operation.

The data output for each page will always start from byte 0 and a full page data should be read out for each page.

Figure 19. Continuous Read Waveform



: address is Don't care.

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Read from Cache Command Definition

1. The input address is “column address” for Conventional Read mode
2. The input address is "don't care" (dummy) for Continuous Read mode

Table 9. Command Set - Continuous Read Operation Enabled

SPI_NOR_EN = 0, **CONT = 1**

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	7th Byte	8th Byte
Get Feature	0Fh	ADD	Data					
Read Status	05h	Data						
Set Feature	1Fh	ADD	Data					
Page Read	13h	RADD2	RADD1	RADD0				
Read From Cache x1	03h	DUMMY	DUMMY	DUMMY	DATA~			
Read From Cache x1 (Alternative)	0Bh	DUMMY	DUMMY	DUMMY	DATA~			
Read From Cache x2 Note 3	3Bh	DUMMY	DUMMY	DUMMY	DATA~*2			
Read From Cache x4 Note 3	6Bh	DUMMY	DUMMY	DUMMY	DATA~*4			
Read From Cache Dual IO 1-2-2 Note 3	BBh	DUMMY	DUMMY	DUMMY	DATA~*2			
Read From Cache Quad IO 1-4-4 Note 3	EBh	DUMMY	DUMMY	DUMMY	DUMMY*4	DATA~*4		
Read ID	9Fh	DUMMY	MID	DID1	DID2			
Block Erase	D8h	RADD2	RADD1	RADD0				
Program Execute	10h	RADD2	RADD1	RADD0				
Program Load x1	02h	CADD1	CADD0	DATA~				
Program Load random Data x1	84h	CADD1	CADD0	DATA~				
Program Load x4 Note 3	32h	CADD1	CADD0	DATA~*4				
Program Load Random Data x4 Note 3	34h	CADD1	CADD0	DATA~*4				
Write Enable	06h							
Write Disable	04h							
Reset	FFh							
Read ECCSR	7Ch	DUMMY	SR_ECC					
Write BBM	A1h	LBA	LBA	PBA	PBA			
Read BBM Note 1	A5h	DUMMY	LBA0	LBA0	PBA0	PBA0	LBA1	LBA1~
ECC Warning Page Address Note 2	A9h	DUMMY	RADD2_L	RADD1_L	RADD0_L	RADD2_F	RADD1_F	RADD0_F

Notes:

1. A5h command may read the 40 links of BBM_table (LBAx/PBAx)

2. RADDx_L: Last Warning Page Address, RADDx_F: First Warning Page Address

*3. *2 stands for the dual I/O phase and *4 for quad I/O mode*

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9. SPI NOR Compatible Command

Considering some SoC(or MCU) of host system must adopt the read protocol of SPI NOR like, this device provide the SPI_NOR_EN of configuration register bit to enable the read protocol of SPI NOR like for Read From Cache commands. The SPI_NOR_EN bit is OTP type once it is enable and cannot disable.

It is recommended to set the SPI_NOR_EN bit by programmer machine in advance before power on while attempts to adopt the read protocol of SPI NOR like.

Please refer to the **"Figure 34. Special OTP Configuration Register Program Operation (for V2/OTP Type of Configuration Register Bits)"**.

Table 10. Command Set - SPI NOR Like Protocol Enabled

(SPI_NOR_EN = 1, CONT=0)

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	7th Byte	8th Byte
Get Feature	0Fh	ADD	**Data**					
Read Status	05h	Data						
Set Feature	1Fh	ADD	Data					
Page Read	13h	RADD2	RADD1	RADD0				
Page Read Cache Random	30h	RADD2	RADD1	RADD0				
Page Read Cache Sequential	31h							
Page Read Cache End	3Fh							
Read From Cache x1	03h	DUMMY	CADD1	CADD0	DATA~			
Read From Cache x1 (Alternative)	0Bh	DUMMY	CADD1	CADD0	DUMMY	DATA~		
Read From Cache x2[Note3]	3Bh	CADD1	CADD0	DUMMY	DATA~*2			
Read From Cache x4[Note3]	6Bh	CADD1	CADD0	DUMMY	DATA~*4			
Read From Cache Dual IO 1-2-2[Note3]	BBh	CADD1*2	CADD0*2	DUMMY*2	DATA~*2			
Read From Cache Quad IO 1-4-4[Note3]	EBh	CADD1*4	CADD0*4	DUMMY*4	DUMMY*4	DATA~*4		
Read ID	9Fh	DUMMY	MID	DID1	DID2			
Block Erase	D8h	RADD2	RADD1	RADD0				
Program Execute	10h	RADD2	RADD1	RADD0				
Program Load x1	02h	CADD1	CADD0	DATA~				
Program Load Random Data x1	84h	CADD1	CADD0	DATA~				
Program Load x4[Note3]	32h	CADD1	CADD0	DATA~*4				
Program Load Random Data x4[Note3]	34h	CADD1	CADD0	DATA~*4				
Write Enable	06h							
Write Disable	04h							
Reset	FFh							
Read ECCSR	7Ch	DUMMY	SR_ECC					
Write BBM	A1h	LBA	LBA	PBA	PBA			
Read BBM[Note1]	A5h	DUMMY	LBA0	LBA0	PBA0	PBA0	LBA1	LBA1~
ECC Warning Page Address[Note2]	A9h	DUMMY	RADD2_L	RADD1_L	RADD0_L	RADD2_F	RADD1_F	RADD0_F

Notes: *1. A5h command may read the 40 links of BBM_table (LBAx/PBAx)*

2. RADDx_L: Last Warning Page Address, RADDx_F: First Warning Page Address

*3. *2 stands for the dual I/O phase and *4 for quad I/O mode*

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Table 11. Command Set - SPI NOR Like Protocol Enabled & Continuous Read Operation

(SPI_NOR_EN = 1, CONT=1)

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	7th Byte	8th Byte
Get Feature	0Fh	ADD	Data					
Read Status	05h	Data						
Set Feature	1Fh	ADD	Data					
Page Read	13h	RADD2	RADD1	RADD0				
Read From Cache x1	03h	DUMMY	DUMMY	DUMMY	DATA~			
Read From Cache x1 (Alternative)	0Bh	DUMMY	DUMMY	DUMMY	DUMMY	DATA~		
Read From Cache x2[Note3]	3Bh	DUMMY	DUMMY	DUMMY	DATA~[*2]			
Read From Cache x4[Note3]	6Bh	DUMMY	DUMMY	DUMMY	DATA~[*4]			
Read From Cache Dual IO 1-2-2[Note3]	BBh	DUMMY	DUMMY	DUMMY	DATA~[*2]			
Read From Cache Quad IO 1-4-4[Note3]	EBh	DUMMY	DUMMY	DUMMY	DUMMY[*4]	DATA~[*4]		
Read ID	9Fh	DUMMY	MID	DID1	DID2			
Block Erase	D8h	RADD2	RADD1	RADD0				
Program Execute	10h	RADD2	RADD1	RADD0				
Program Load x1	02h	CADD1	CADD0	DATA~				
Program Load Random Data x1	84h	CADD1	CADD0	DATA~				
Program Load x4[Note3]	32h	CADD1	CADD0	DATA~[*4]				
Program Load Random Data x4[Note3]	34h	CADD1	CADD0	DATA~[*4]				
Write Enable	06h							
Write Disable	04h							
Reset	FFh							
Read ECCSR	7Ch	DUMMY	SR_ECC					
Write BBM	A1h	LBA	LBA	PBA	PBA			
Read BBM[Note1]	A5h	DUMMY	LBA0	LBA0	PBA0	PBA0	LBA1	LBA1~
ECC Warning Page Address[Note2]	A9h	DUMMY	RADD2_L	RADD1_L	RADD0_L	RADD2_F	RADD1_F	RADD0_F

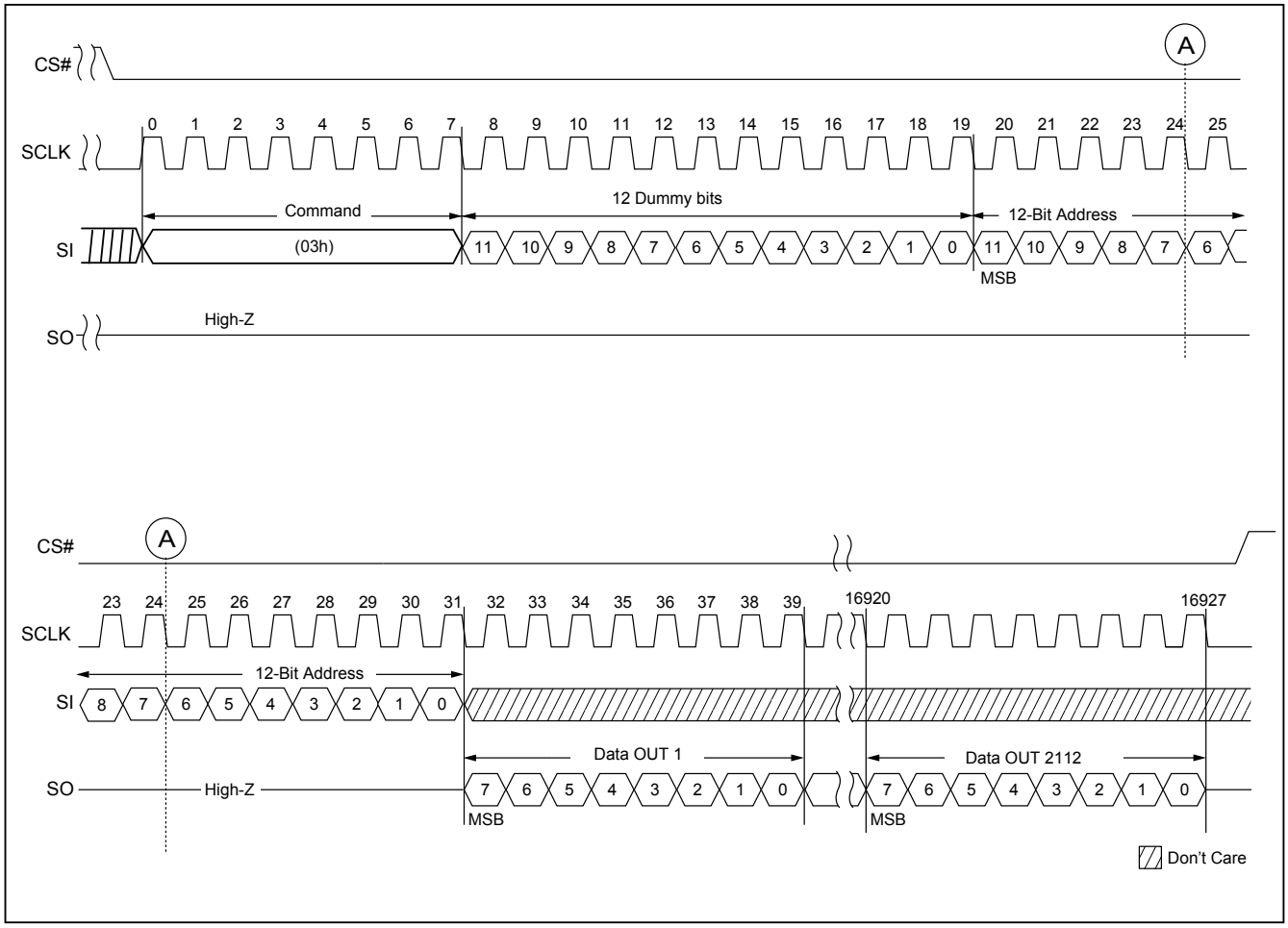
Notes: *1. A5h command may read the 40 links of BBM_table (LBAx/PBAx)*

2. RADDx_L: Last Warning Page Address, RADDx_F: First Warning Page Address

*3. *2 stands for the dual I/O phase and *4 for quad I/O mode*

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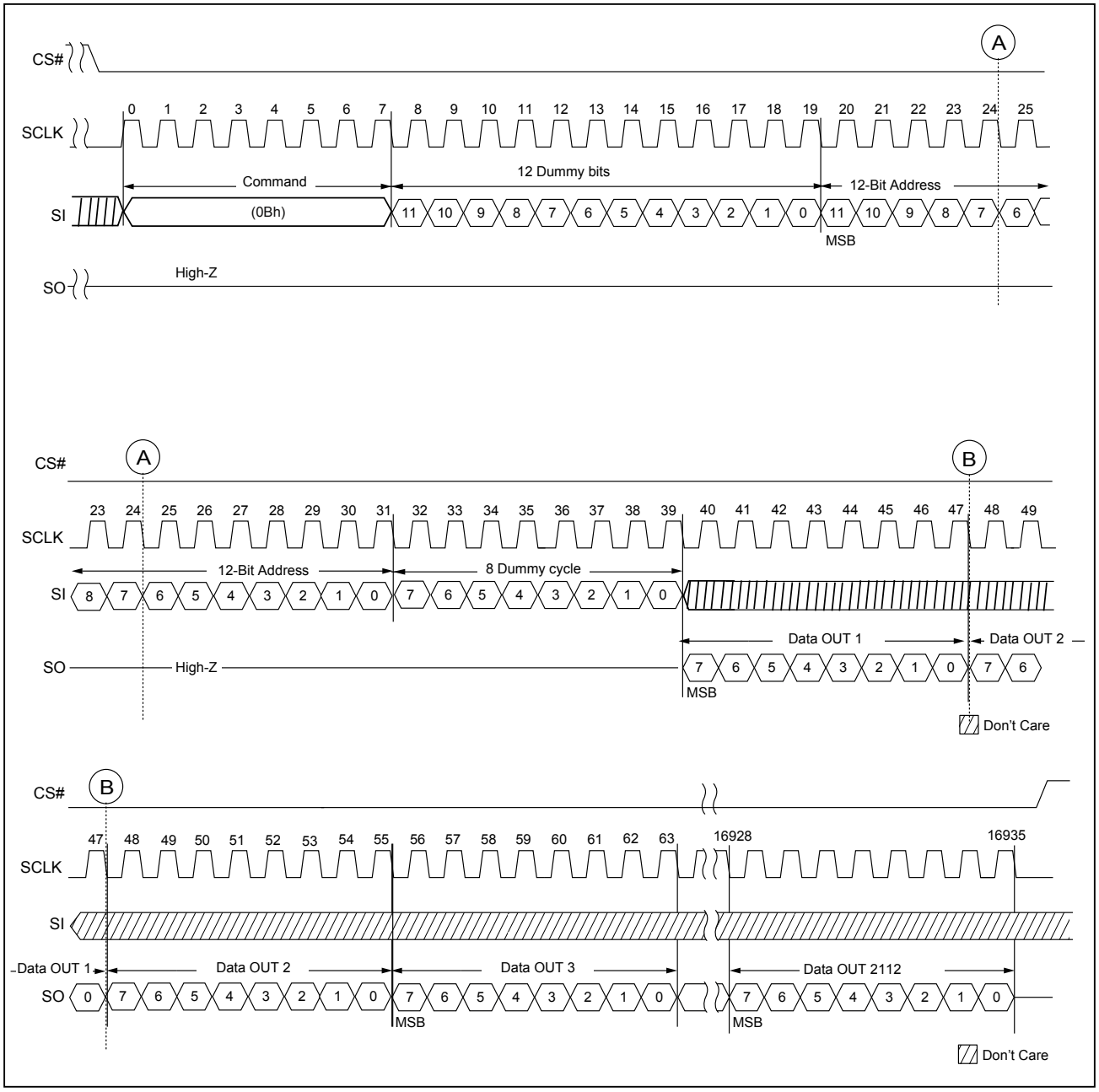
Figure 20. Read From Cache x1 (NOR like)



***Note**: For SPI NOR Like Protocol command, the Read From Cache command (03h) can run up to 20MHz only.*

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Figure 21. Read From Cache x1 (Alternative, NOR like)



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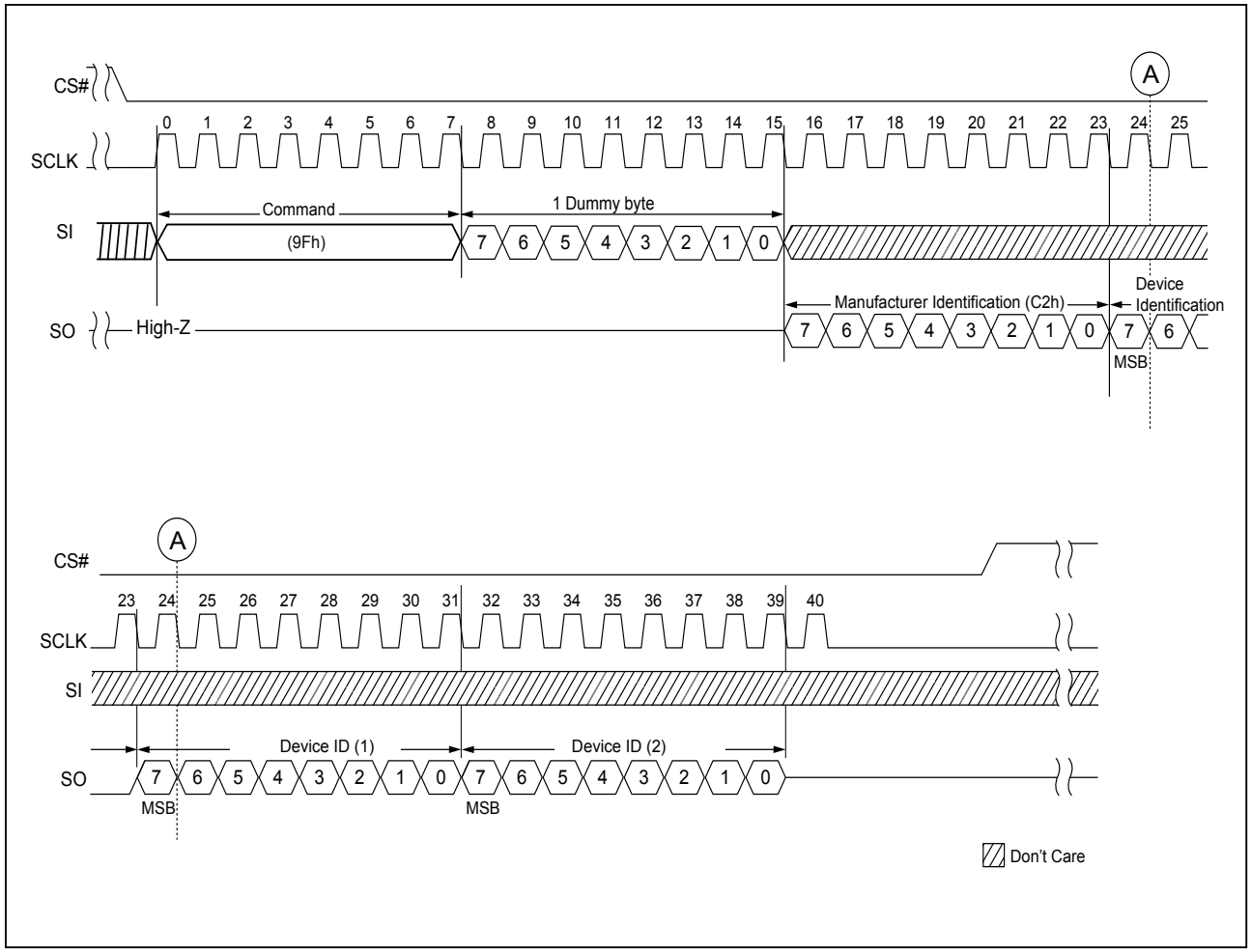
10. READ ID (9Fh)

The READ ID command is shown as the table below.

Table 12. READ ID Table

Byte	Description		I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value
Byte 0	Manufacturer ID (Macronix)		1	1	0	0	0	0	1	0	C2h
Byte 1	Device ID 1	1.8V 1Gb	1	0	0	1	0	0	1	0	92h
		1.8V 2Gb	1	0	1	0	0	0	1	0	A2h
Byte 2	Device ID 2		0	0	0	0	0	0	0	1	01h

Figure 22. READ ID (9Fh) Timing



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11. Parameter Page

The parameter page is accessed by the following command flows:

Issue 1Fh (SET FEATURE) command with Secure OTP enable (B0h for address & 40h for data) → Issue 13h (PAGE READ) with 01h address, issue 0Fh (GET FEATURE) with C0h feature address or RDSR (05h) to poll the status of read completion. → Issue 03h (READ FROM CACHE) with address A[11:0]=000h and read data → Issue 1Fh (SET FEATURE) with feature address B0h to disable Secure OTP feature (data byte = 00h) [exit parameter page read].

Table 13. Parameter Page - MX35UF1GE4AC

	Revision Information and Features Block		
Byte#	**Description**		**Data**
0-3	Parameter Page Signature		4Fh, 4Eh, 46h, 49h
4-5	Revision Number		00h, 00h
6-7	Features Supported (N/A)		00h, 00h
8-9	Optional Commands Supported		06h, 00h
10-31	Reserved		00h
	Manufacturer Information Block		
Byte#	**Description**		**Data**
32-43	Device Manufacturer (12 ASCII characters)		4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	Device Model (20 ASCII Characters)	MX35UF1GE4AC	4Dh, 58h, 33h, 35h, 55h, 46h, 31h, 47h, 45h, 34h, 41h, 43h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		C2h
65-66	Date Code		00h, 00h
67-79	Reserved		00h

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Memory Organization Block			
Byte#	**Description**		**Data**
80-83	Number of Data Bytes per Page	2048-byte	00h, 08h, 00h, 00h
84-85	Number of Spare Bytes per Page	64-byte	40h, 00h
86-89	Number of Data Bytes per Partial Page	512-byte	00h, 02h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page	16-byte	10h, 00h
92-95	Number of Pages per Block		40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		00h, 04h, 00h, 00h
100	Number of Logical Units		01h
101	Number of Address Cycles (N/A)		00h
102	Number of Bits per Cell		01h
103-104	Bad Blocks Maximum per unit		14h, 00h
105-106	Block endurance		01h, 05h
107	Guarantee Valid Blocks at Beginning of Target		01h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of Programs per Page		04h
111	Partial Programming Attributes		00h
112	Number of ECC bits		00h
113	Number of Interleaved Address Bits (N/A)		00h
114	Interleaved Operation Attributes (N/A)		00h
115-127	Reserved		00h

Electrical Parameters Block			
Byte#	**Description**		**Data**
128	I/O Pin Capacitance		0Ah
129-130	Timing Mode Support (N/A)		00h, 00h
131-132	Program Cache Timing (N/A)		00h, 00h
133-134	tPROG Maximum Page Program Time (uS)	660us	94h, 02h
135-136	BE Maximum Block Erase time (uS)	3500us	ACh, 0Dh
137-138	tRD_ECC Maximum Page Read time (uS)	80us	50h, 00h
139-140	tCCS Minimum (N/A)	0ns	00h, 00h
141-163	Reserved		00h

Vendor Blocks		
Byte#	**Description**	**Data**
164-165	Vendor Specific Revision Number	00h, 00h
166-167	Reserved	00h, 00h
168	NOR like features support 2-7: Reserved(0) 1 :1= Continuous Read support, 0= Not support 0 :1= BBM_table support, 0= Not support	03h
169	Reserved	00h
170-253	Vendor Specific	00h
254-255	Integrity CRC	Set at Test ***(Note)***

Redundant Parameter Pages		
Byte#	**Description**	**Data**
256-511	Value of Bytes 0-255	Same as 0~255 Byte
512-767	Value of Bytes 0-255	Same as 0~255 Byte
768+	Additional Redundant Parameter Pages	

Note:
The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.

The CRC shall be calculated using the following 16-bit generator polynomial:
$G(X) = X_{16} + X_{15} + X_2 + 1$

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Table 14. Parameter Page - MX35UF2GE4AC

	Revision Information and Features Block		
Byte#	**Description**		**Data**
0-3	Parameter Page Signature		4Fh, 4Eh, 46h, 49h
4-5	Revision Number		00h, 00h
6-7	Features Supported (N/A)		00h, 00h
8-9	Optional Commands Supported		06h, 00h
10-31	Reserved		00h
	Manufacturer Information Block		
Byte#	**Description**		**Data**
32-43	Device Manufacturer (12 ASCII characters)		4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	Device Model (20 ASCII Characters)	MX35UF2GE4AC	4Dh, 58h, 33h, 35h, 55h, 46h, 32h, 47h, 45h, 34h, 41h, 43h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		C2h
65-66	Date Code		00h, 00h
67-79	Reserved		00h

Memory Organization Block			
Byte#	**Description**		**Data**
80-83	Number of Data Bytes per Page	2048-byte	00h, 08h, 00h, 00h
84-85	Number of Spare Bytes per Page	64-byte	40h, 00h
86-89	Number of Data Bytes per Partial Page	512-byte	00h, 02h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page	16-byte	10h, 00h
92-95	Number of Pages per Block		40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		00h, 08h, 00h, 00h
100	Number of Logical Units		01h
101	Number of Address Cycles (N/A)		00h
102	Number of Bits per Cell		01h
103-104	Bad Blocks Maximum per unit		28h, 00h
105-106	Block endurance		01h, 05h
107	Guarantee Valid Blocks at Beginning of Target		01h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of Programs per Page		04h
111	Partial Programming Attributes		00h
112	Number of ECC bits		00h
113	Number of Interleaved Address Bits (N/A)		00h
114	Interleaved Operation Attributes (N/A)		00h
115-127	Reserved		00h

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Electrical Parameters Block			
Byte#	**Description**		**Data**
128	I/O Pin Capacitance		0Ah
129-130	Timing Mode Support (N/A)		00h, 00h
131-132	Program Cache Timing (N/A)		00h, 00h
133-134	tPROG Maximum Page Program Time (uS)	660us	94h, 02h
135-136	BE Maximum Block Erase time (uS)	3500us	ACh, 0Dh
137-138	tRD_ECC Maximum Page Read time (uS)	80us	50h, 00h
139-140	tCCS Minimum (N/A)	0ns	00h, 00h
141-163	Reserved		00h
Vendor Blocks			
Byte#	**Description**		**Data**
164-165	Vendor Specific Revision Number		00h, 00h
166-167	Reserved		00h, 00h
168	NOR like features support 2-7: Reserved(0) 1 :1= Continuous Read support, 0= Not support 0 :1= BBM_table support, 0= Not support		03h
169	Reserved		00h
170-253	Vendor Specific		00h
254-255	Integrity CRC		Set at Test ***(Note)***
Redundant Parameter Pages			
Byte#	**Description**		**Data**
256-511	Value of Bytes 0-255		Same as 0~255 Byte
512-767	Value of Bytes 0-255		Same as 0~255 Byte
768+	Additional Redundant Parameter Pages		

Note:
The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.

The CRC shall be calculated using the following 16-bit generator polynomial:
$G(X) = X_{16} + X_{15} + X_2 + 1$

12. Unique ID Page

The Unique ID page is accessed by the following command flows:

Issue 1Fh (SET FEATURE) command with Secure OTP enable bit 6 (B0h for address & 1b for bit 6 data) → Issue 13h (PAGE READ) with 00h address, issue 0Fh (GET FEATURE) with C0h feature address or RDSR (05h) to poll the status of read completion → Issue 03h (READ FROM CACHE) with address A[11:0]=000h and read data → Issue 1Fh (SET FEATURE) with feature address B0h to disable Secure OTP function (bit 6 data =0b) [exit unique ID read]

Unique ID data: 16x32byte of Unique ID data. On each 32byte, the first 16byte and following 16byte should be XOR to be FFh.

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13. Internal ECC Status

13-1. Internal ECC Enabled/Disabled

The internal ECC logic may detect 5-bit error and correct 4-bit error. The default state of the internal ECC is enabled. To enable/disable the internal ECC, it is operated by the Set Feature operation to enable internal ECC or disable the internal ECC, and then check the internal ECC state by Get Feature operation.

The internal ECC is enabled by using Set Feature command (1Fh) and followed by feature address (B0h) and then set Bit4(ECC enabled) as "1". To disable the internal ECC can be done by using the Set Feature command (1Fh) and followed by the feature address (B0h) and then set Bit4 (ECC enabled) as "0".

When the internal ECC is enabled, after the data transfer time (tRD) is completed, a Status Read operation is required to check any uncorrectable read error happened. Please refer to **"Table 18. Status Register Bit Descriptions"**.

The constraint of the internal ECC enabled operation:

- The ECC protection coverage: please refer to **"Table 15. The Distribution of ECC Segment and Spare Area"**. Only the grey areas are under internal ECC protection when the internal ECC is enabled.
- The number of partial-page program is not 4 in an ECC segment, the user need to program the main area (512B)+Spare(M1: 4B) at one program time, so the ECC parity code can be calculated properly and stored in the last 8B of the Spare Area and the additional hidden spare area.

Table 15. The Distribution of ECC Segment and Spare Area

Area	Main Area (0)	Main Area (1)	Main Area (2)	Main Area (3)	Spare(0)			Spare(1)			Spare(2)			Spare(3)		
					M2	M1	R	M2	M1	R	M2	M1	R	M2	M1	R
Addr. (Start)	000h	200h	400h	600h	800h	804h	808h	810h	814h	818h	820h	824h	828h	830h	834h	838h
Addr. (End)	1FFh	3FFh	5FFh	7FFh	803h	807h	80Fh	813h	817h	81Fh	823h	827h	82Fh	833h	837h	83Fh
Size	512(B)	512(B)	512(B)	512(B)	4(B)	4(B)	8(B)	4(B)	4(B)	8(B)	4(B)	4(B)	8(B)	4(B)	4(B)	8(B)
Data Type	User	User	User	User	User	User	R	User	User	R	User	User	R	User	User	R

Notes:

M2: Metadata 2 (for bad block mark and metadata)

M1: Metadata 1

R: Reserved for ECC parity code

Grey area: Under ECC protection

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13-2. Read ECCSR (7Ch) Command for ECC Status Read

Besides the Get Feature(with feature address of C0h) may collect the internal ECC status; the 7Ch command may read out the error bits number for the worst segment of the page(s). This command reports two kinds of ECC status. The first kind is the ECC status for the current page, the second kind is the ECC status for the accumulated pages.

Figure 23. Read ECCSR (7Ch Command)

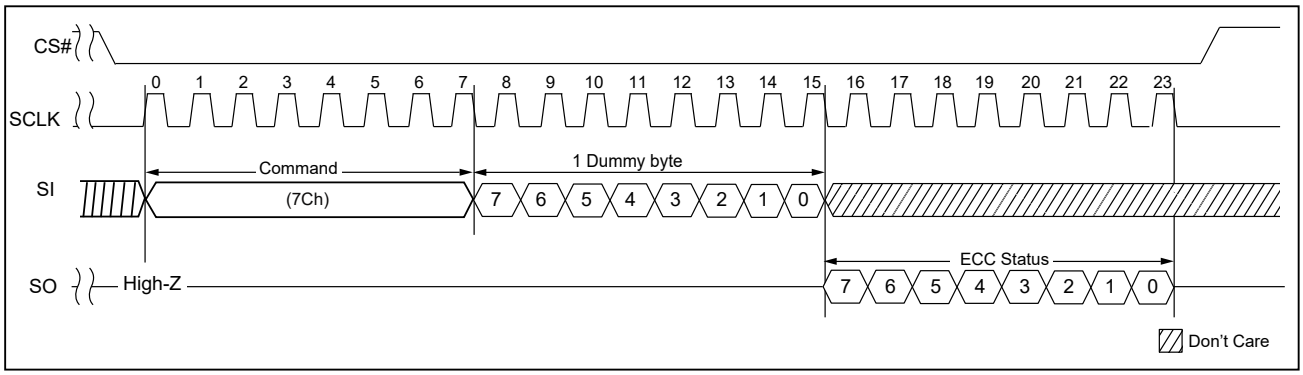


Table 16. ECC Status Read

Error #	ECCSR[3:0]
0	0000
1	0001
2	0010
3	0011
4	0100
>4	1111

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ECC Status for the Accumulated pages				ECC Status for the Current page			
ECCSR[3]	ECCSR[2]	ECCSR[1]	ECCSR[0]	ECCSR[3]	ECCSR[2]	ECCSR[1]	ECCSR[0]

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13-3. Flexible ECC Bit Flip Threshold Setting & Read ECC Warning Page Address

Flexible ECC Bit Flip Threshold Setting: Host can set the ECC warning criterion by themselves. This Serial Flash offers “BFT[3:0]” for the user to set their own ECC warning criterion. The Chip will report the warning status when on the status feature bits ECC_S[1:0] error bit number is larger or equal to the BFT.

Table 17. Flexible ECC Bit Flip Threshold Setting & Read ECC Warning Page Address

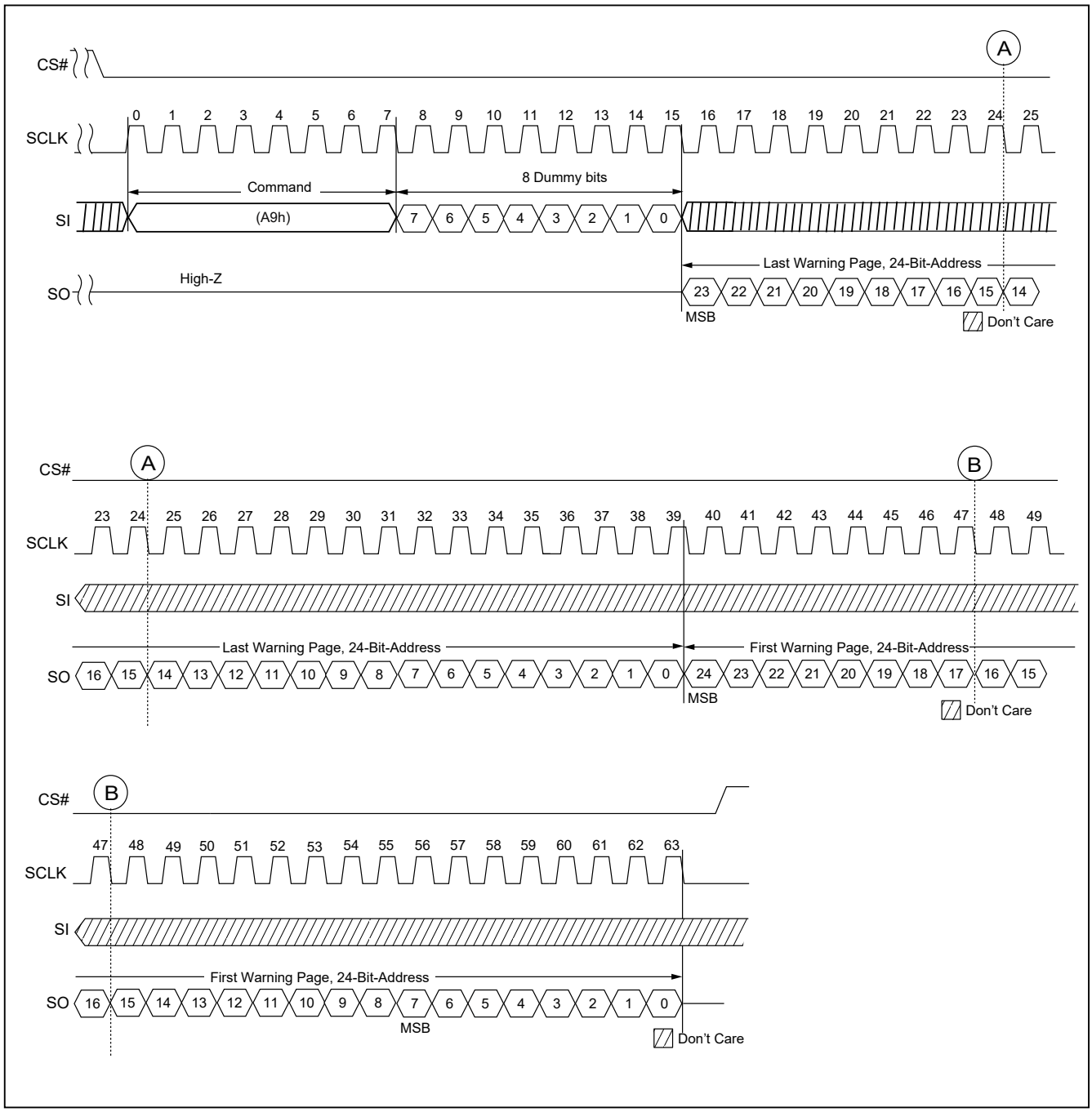
ADD	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
10h	Configuration	BFT3	BFT2	BFT1	BFT0				ENPGM	F0h

BFT[3:0]	Flexible ECC Bit Flip Threshold Setting
0000	Detect uncorrected error
0001	Detect ≥1 bit error & corrected
0010	Detect ≥2 bit error & corrected
0011	Detect ≥3 bit error & corrected
0100	Detect ≥4 bit error & corrected
0101	Detect uncorrected error
0110	Detect uncorrected error
0111	Detect uncorrected error
1000	Detect uncorrected error
1001	Detect uncorrected error
1010	Detect uncorrected error
1011	Detect uncorrected error
1100	Detect uncorrected error
1101	Detect uncorrected error
1110	Detect uncorrected error
1111	Detect uncorrected error (default)

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Read ECC warning page address: Host can get the 1st and last page addresses which reaches the ECC warning criterion. During continuous read operation, the chip will record the 1st and last page address with error bit number is larger or equal to BFT[3:0]. Host can issue the “Read ECC warning Page address” command to read out these two page addresses.

Figure 24. ECC Warning Timing



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14. Program Operations

14-1. PAGE PROGRAM

With following operation sequences, the PAGE PROGRAM operation programs the page from byte 1 to byte 2112.

WRITE ENABLE (06h) → PROGRAM LOAD (02h) → PROGRAM LOAD RANDOM DATA (84h) if needed → PROGRAM EXECUTE (10h) → GET FEATUR from command to read status (0Fh) or RDSR (05h) to get status.

WEL bit is set with the WRITE ENABLE (06h) issued. The program operation will be ignored if 06h command not issued. In a single page, four partial page programs are allowed. Exceeded bytes (Page address is larger than 2112 for "PROGRAM LOAD" or "PROGRAM LOAD RANDOM DATA", the exceeding bytes will be ignored. When CS goes high, the "PROGRAM LOAD" or "PROGRAM LOAD RANDOM DATA" operation" terminates. Please note the figure below for PROGRAM LOAD.

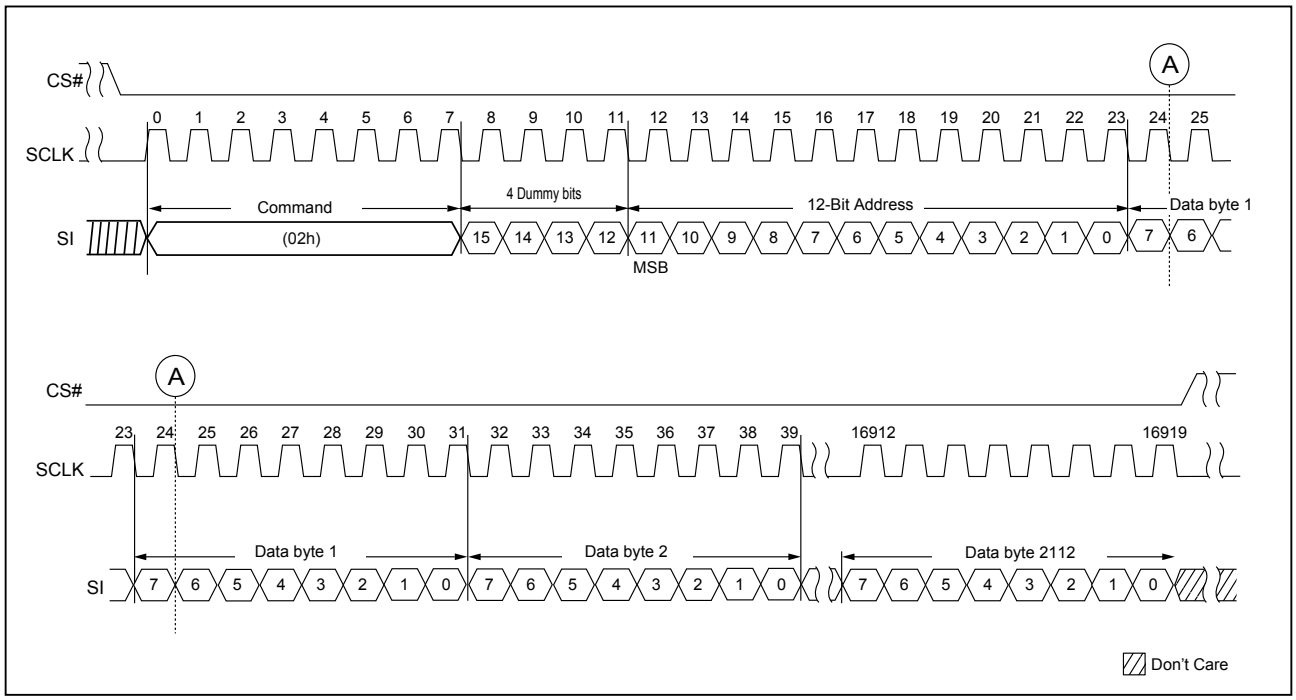
After PROGRAM LOAD is done, the programming of data should be as following steps: issue 10h (PROGRAM EXECUTE) with 1byte command code, 24 bits address → code programming to memory and busy for tPROG → Program complete.

The page program operation in a block should start from the low address to high address.

During programming, status to be polled by the status register.

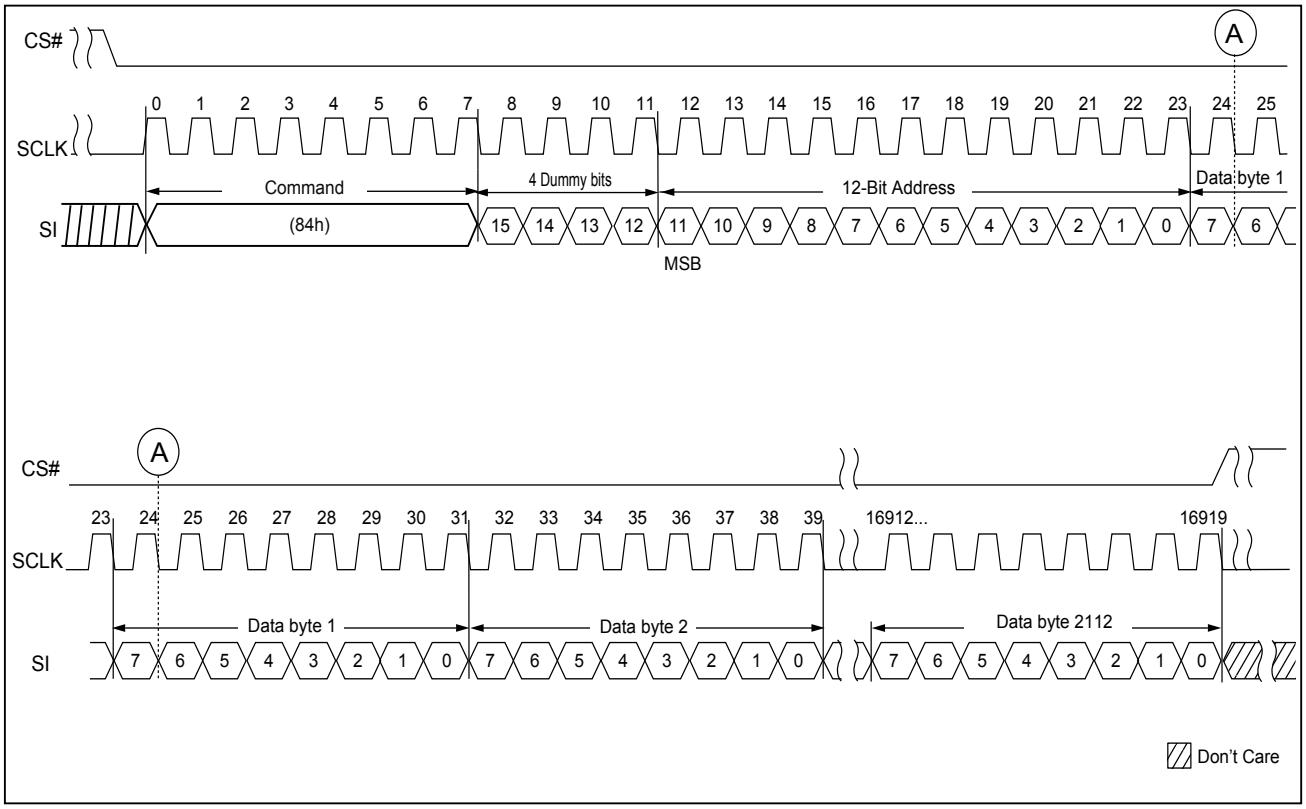
Operation shows in the Figure below.

Figure 25. PROGRAM LOAD (02h) Timing



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Figure 26. PROGRAM LOAD RANDOM DATA (84h) Timing

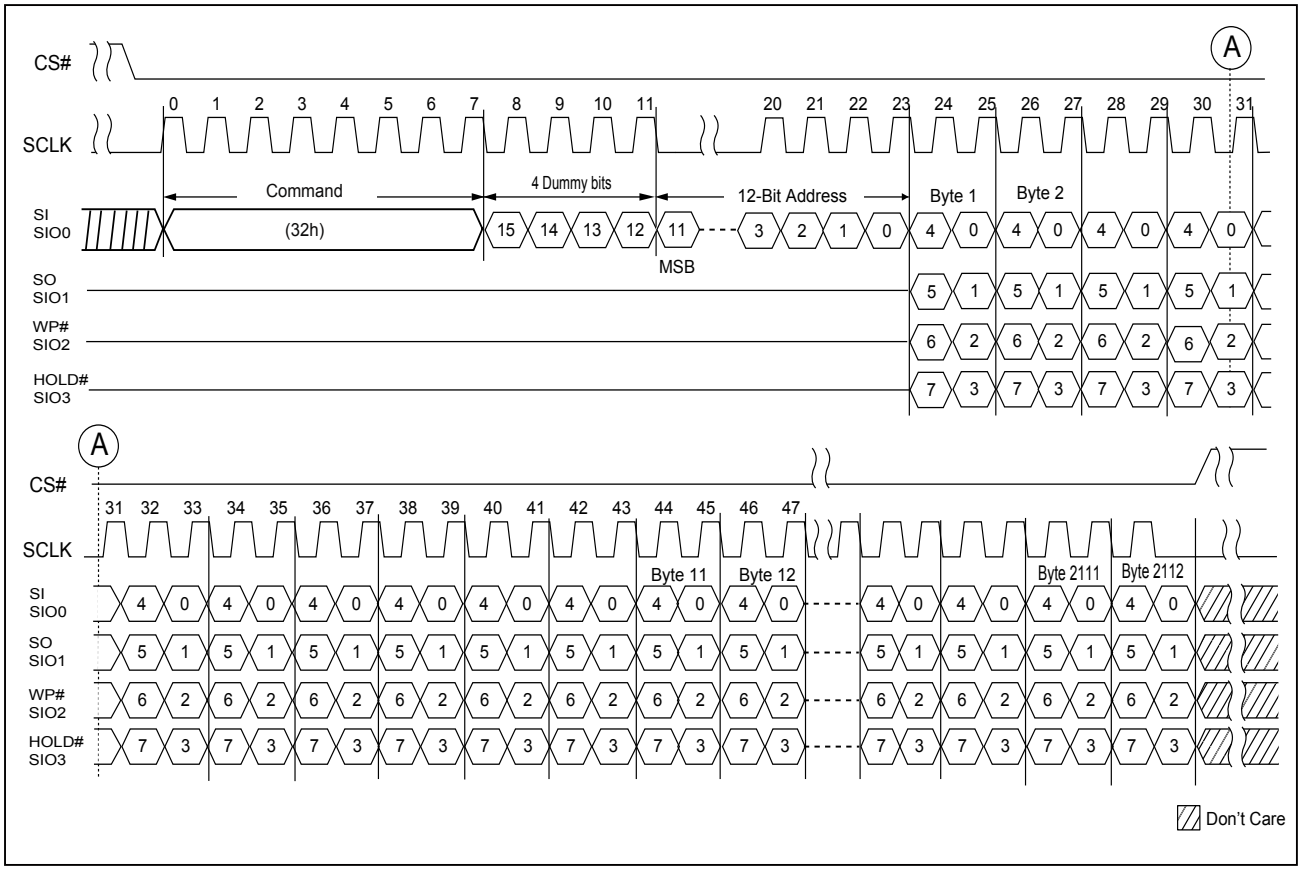


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14-2. QUAD IO PAGE PROGRAM

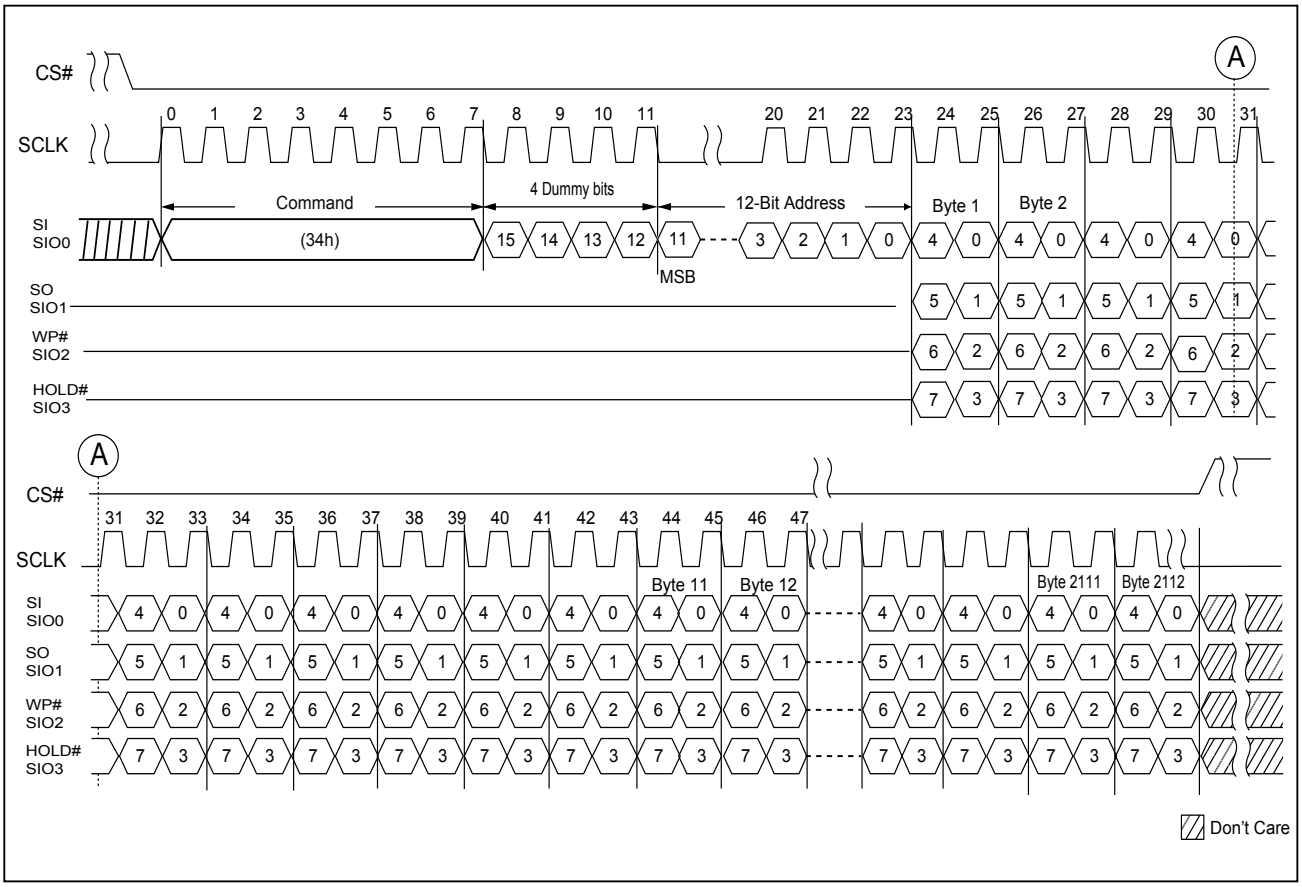
QUAD IO PAGE PROGRAM conducts the 2KB program with 4 I/O mode. The steps are: WRITE ENABLE (06h) → PROGRAM LOAD X4 (32h) → PROGRAM LOAD RANDOM DATA (34h) if needed → PROGRAM EXECUTE (10h) → Poll status by issuing GET FEATURE (0Fh) or RDSR (05h).

Figure 27. PROGRAM LOAD X4 (32h) Timing



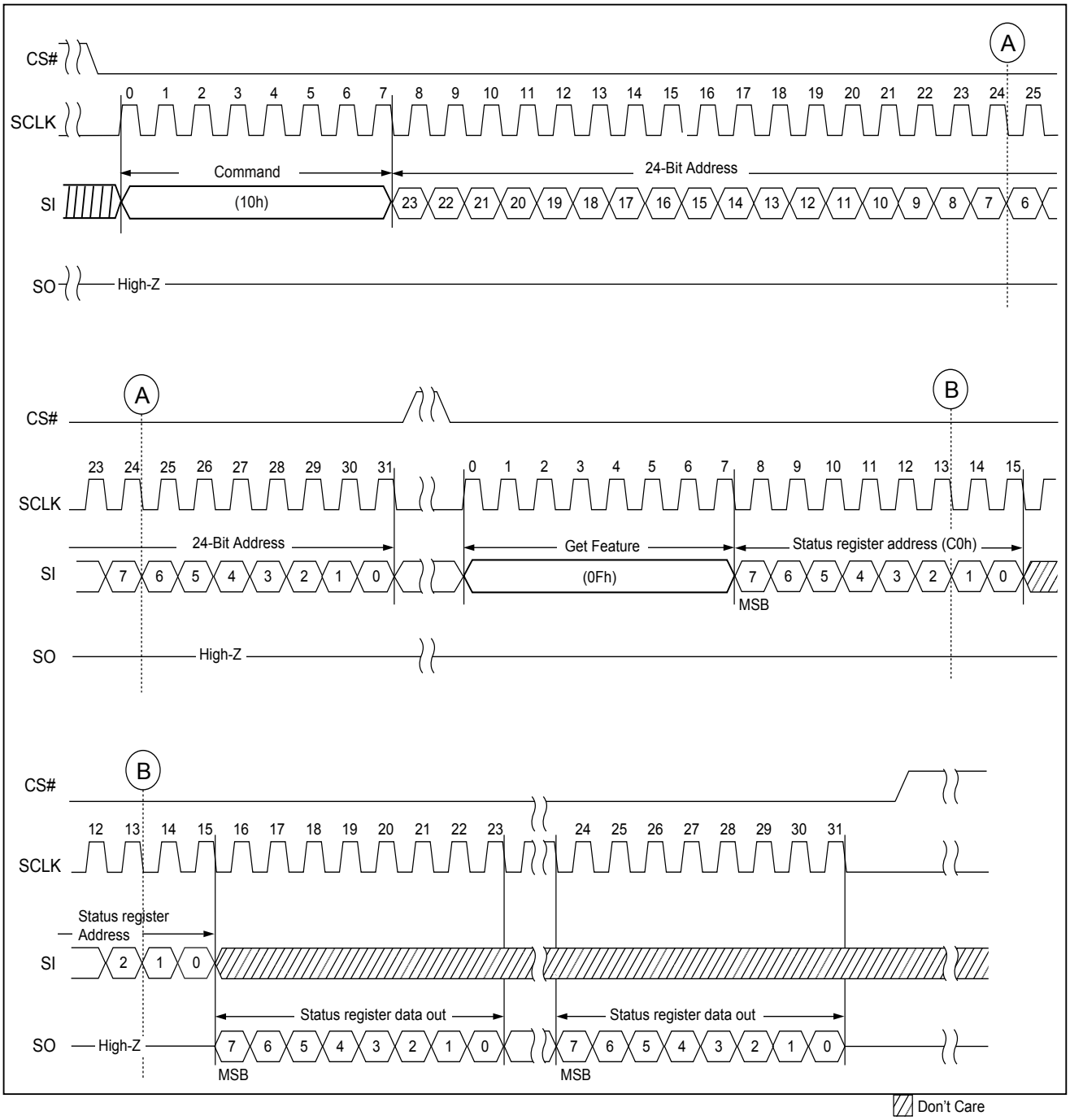
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Figure 28. QUAD IO PROGRAM RANDOM INPUT (34h) Timing



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Figure 29. PROGRAM EXECUTE (10h) Timing



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14-3. BLOCK OPERATIONS

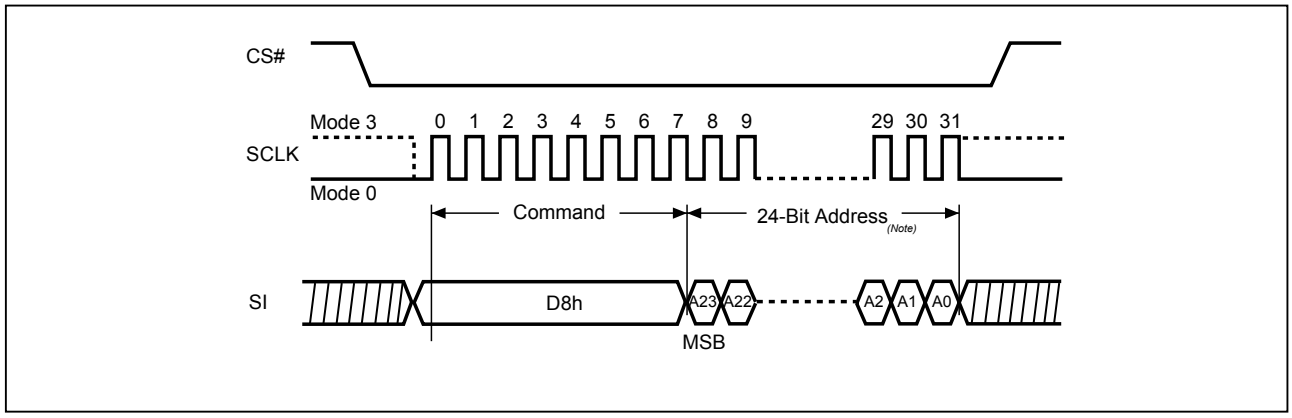
Block Erase (D8h)

The Block Erase (D8h) instruction is for erasing the data of the chosen block to be "1". The instruction is used for a block of 128KB erase operation. A Write Enable (WREN) instruction be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (D8h). Any address of the block is a valid address for Block Erase (D8h) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed. Finally, a Get Feature(0Fh) or RDSR (05h) instruction to check the status is necessary.

The sequence of issuing Block Erase instruction is: CS# goes low→ send Block Erase instruction code→ 24-bit address on SI→CS# goes high.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Get Feature (0Fh) instruction with Address (C0h) or RDSR (05h) may check the status of the operation during the Block Erase cycle is in progress (please refer to the waveform **"Figure 7. GET FEATURE (0Fh) Timing"** and **"Table 4. Configuration Registers"**). The OIP bit is "1" during the tBE timing, and is cleared to "0" when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

Figure 30. Block Erase (BE) Sequence



Note: *The 24-bit Address includes: 17-bit row address and 7-bit dummy (for 2Gb), or 16-bit row address and 8-bit dummy (for 1Gb).*

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15. Configuration Registers and Status Registers

The device provides several registers which includes Block Protection registers and configuration registers to set the feature configurations as well as the status register to output the device status.

Table 18. Status Register Bit Descriptions

Register	Feature bits	Type	Description
Status	CRBSY	V	Chip busy status for Cache Read operation 0b: Chip is ready and can accepted new command for cache operation 1b: Chip is busy and cannot accept new command for cache read operation
	BBMT_F	V	BBM table is full or not 0b: BBM table is not full and new L2P link can be added 1b: BBM table is full and new L2P link cannot be added
	ECC_S[1:0]	V	The bit shows the status of ECC as below: 00b = 0 bit error 01b = bit error are detected and been corrected, bit error count is less than the bit flip threshold 10b = bit error and can not be corrected. 11b = bit error are detected and been corrected, bit error count is equal or more than the bit flip threshold. If CONT=0, the value of ECC_Sx(S1:S0) bits will be cleared as “00b” by reset command. After the page read or page read cache operation is completed, the bits will be updated to reflect the ECC status of the current output page. The ECC_Sx(S1:S0) value reflects the ECC status of the content of the POR page (the default POR page is the page 0 of the block 0) after a power-on reset. If CONT=1, the value of ECC_Sx(S1:S0) bits will not be cleared by the reset command. After the continuous read operation is completed, the bits will be updated to reflect the ECC status of the accumulated pages in the current continuous read operation. The ECC_Sx(S1:S0) value reflects the ECC status of the content of the accumulated pages which starts from the POR page after a power-on reset. If the internal ECC is disabled by the Set feature command, the ECC_ Sx(S1:S0) are invalid.
	P_FAIL	V	The bit value shows the status of program failure or if host program any invalid address or protected area (including protected blocks or protected Secure OTP area). 0: Passed 1: Failed The bit value will be cleared (as "0") by RESET command or during the program execute command operation.
	E_FAIL	V	The bit value shows the status of erase failure or if host erase any invalid address or protected area (including protected blocks or protected Secure OTP area). 0: Passed 1: Failed The bit value will be cleared (as "0") by RESET command or at the beginning of the block erase command operation.
	WEL	V	Status bit for write enable successful or not. The bit value will be cleared (as "0") by issuing Write Disable command(04h) or after the program/erase operation completion. 0b: the chip is write protected and cannot accept any program/erase command 1b: the chip is not write protected and can accept the program/erase command
	OIP	V	Chip busy Status bit 0b: Chip is ready 1b: Chip is busy

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Table 19. Configuration and Block Protection Register Bit Descriptions

Register	Feature bits	Type	Description
Configuration	ENPGM	V	Enable the special OTP configuration register program operation 0b: Disabled 1b: Enabled
	BFT[3:0]	V2	ECC bit flip threshold
	OTPRWSP	OTP	V2/OTP feature register write solid protection 0b: V2/OTP type feature register are not solid protected 1b: V2/OTP type feature register are solid protected (after OTPRWSP bit is programmed)
	SPI_NOR_EN	OTP	Enable SPI NOR Interface 1b: SPI NOR Interface is selected 0b: SPI NOR Interface is NOT selected
	CONT	V2	Enable Continuous read operation mode 0b: Not enabled 1b: Enabled
	QE	V	Quad enable 0b: Not enabled 1b: Enabled
	OTP_PROT	V	Secure OTP protection 0b: Not enabled 1b: Enabled
	OTPEN	V	Secure OTP enable 0b: Not enabled 1b: Enabled
	ECC_EN	V	Internal ECC enabled 0b: Not enabled 1b: Enabled (default)
	DS_IO[1:0]	V2	I/O Strength Feature, refer to **"Table 6. I/O Strength Feature Table"**.
Block Protection	BPRWD	V	Block protection on register write protect 0b: Block protection register is not protected 1b & WP# = HI: Block protection register is not protected 1b & WP# = Low: Block protection register is protected
	BP[2:0], Invert, Complementary	V	Block protection registers
	SP	V	Enabled the block protection register write solid protection function 0b: Block protection register is not solid protected 1b: Block protection register is solid protected

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15-1. Block Protection Feature

The Block Protection feature includes three block protection bits (BPx), Block Protection Register Write Disable (BPRWD). Inverse bit (INVERT), complement bit (COMPLEMENTARY) and Solid Protection Bit (SP).

Soft Protection Mode (SPM)

The SPM uses the BPx bits, INVERT, and COMPLEMENTARY bits to allow part of memory to be protected as read only. The protected area definition is shown as **"Table 20. Definition of Protection Bits"**. The protected areas are more flexible which may protect various area by setting value of BP0-BP2 and Invert bit, and Complementary bit. These are volatile bits and can be modified by set feature command.

After power-up, the chip is in protection state, that is, the feature bits BPx is 1, all other bits (BPRWD, INVERT, COMPLEMENTARY and SP) are 0. The Set feature instruction (1Fh) with feature address (A0h) may change the value of the block protection bits and un-protect whole chip or a certain area for further program/erase operation. For example, after the power-on, the whole chip is protected from program/erase operation, the top 1/64 area may be un-protected by using the Set feature instruction (1Fh) with the feature address (A0h) to change the values of BP2 and BP1 from "1" to "0" as **"Table 20. Definition of Protection Bits"**.

Hardware Protection Mode (HPM) & Solid Protection Mode (SDPM)

Under the Hardware Protection mode and Solid Protection Mode, the (BPx, INVERT, COMPLEMENTART) bits can not be changed.

Hardware Protection Mode: The device enters HPM if BPRWD bits is set to 1 and WP#/SIO2 is driven to 0.

Note 1: *HPM also requires SP bit to be 0 state .*

Note 2: *The Quad mode is not supported in HPM.*

Solid Protection Mode: If SP bit is set to 1, the device enters SDPM. After that, the selected block is solid protected and can not be un-protected until next power cycle.

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Table 20. Definition of Protection Bits

BP2	BP1	BP0	Invert	Complementary	Protection Area
0	0	0	x	x	all unlocked
0	0	1	0	0	upper 1/64 locked
0	1	0	0	0	upper 1/32 locked
0	1	1	0	0	upper 1/16 locked
1	0	0	0	0	upper 1/8 locked
1	0	1	0	0	upper 1/4 locked
1	1	0	0	0	upper 1/2 locked
1	1	1	x	x	all locked (default)
0	0	1	1	0	lower 1/64 locked
0	1	0	1	0	lower 1/32 locked
0	1	1	1	0	lower 1/16 locked
1	0	0	1	0	lower 1/8 locked
1	0	1	1	0	lower 1/4 locked
1	1	0	1	0	lower 1/2 locked
0	0	1	0	1	lower 63/64 locked
0	1	0	0	1	lower 31/32 locked
0	1	1	0	1	lower 15/16 locked
1	0	0	0	1	lower 7/8 locked
1	0	1	0	1	lower 3/4 locked
1	1	0	0	1	block 0
0	0	1	1	1	upper 63/64 locked
0	1	0	1	1	upper 31/32 locked
0	1	1	1	1	upper 15/16 locked
1	0	0	1	1	upper 7/8 locked
1	0	1	1	1	upper 3/4 locked
1	1	0	1	1	block0

Note: *Block #0 is at lower portion.*

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15-2. Secure OTP (One-Time-Programmable) Feature

There is an Secure OTP area which has 30 full pages (x 2112B) from page 02h to page 1Fh guarantee to be good for system device serial number storage or other fixed code storage. The Secure OTP area is a non-erasable and one-time-programmable area, which is default to “1” and allows partial page program to be “0”, once the Secure OTP protection mode is set, the Secure OTP area becomes read-only and cannot be programmed again.

The Secure OTP operation is operated by the Set Feature instruction with feature address (B0h) to access the Secure OTP operation mode and Secure OTP protection mode.

To check the Serial Flash device is ready or busy in the Secure OTP operation mode, the status register bit 0 (OIP bit) may report the status by Get Feature command operation.

To exit the Secure OTP operation or protect mode, it can be done by writing "0" to both Bit7 (Secure OTP protect bit) and bit6 (Secure OTP enable bit) for returning to the normal operation.

Secure OTP Read

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set the "Secure OTP Enabled Bit" as "1".
3. Issuing normal Page Read command (13h)

Secure OTP Program (if the "Secure OTP Protection Bit" is "0") for

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set the "Secure OTP Enabled Bit" as "1".
3. Issuing WRITE ENABLE command (06h)
4. Issuing Page Program command (02h)
5. Issuing program execute command (10h)

Secure OTP Protection

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set both the "Secure OTP Protection Bit" (OTP_PROT) and "Secure OTP Enabled Bit" OTPEN as "1".
3. Issuing program execute command (10h)

Table 21. Secure OTP States

Secure OTP Protection Bit[Note1]	Secure OTP Enabled Bit	State
0	0	Normal operation
0	1	Access the Secure OTP for reading or programming
1	0	Not applicable
1	1	Secure OTP Protection by using the Program Execution command (10h)[Note2]

Note 1. *OTP protection bit is non-volatile.*

Note 2. *Once the "Secure OTP Protection Bit" and "Secure OTP Enabled Bit" are set as "1" and completion of the secure OTP protection operation, the secure OTP becomes read only, even though after that the value of OTP_PROT to be cleared as "0".*

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15-3. Status Register

15-3-1. Get Feature command (0Fh)

The MX35UFxGE4AC provides a status register that outputs the device status by writing a Get Feature command (0Fh) with the feature address (C0h), and then the IO pins output the status. Refer to **"Figure 7. GET FEATURE (0Fh) Timing"**.

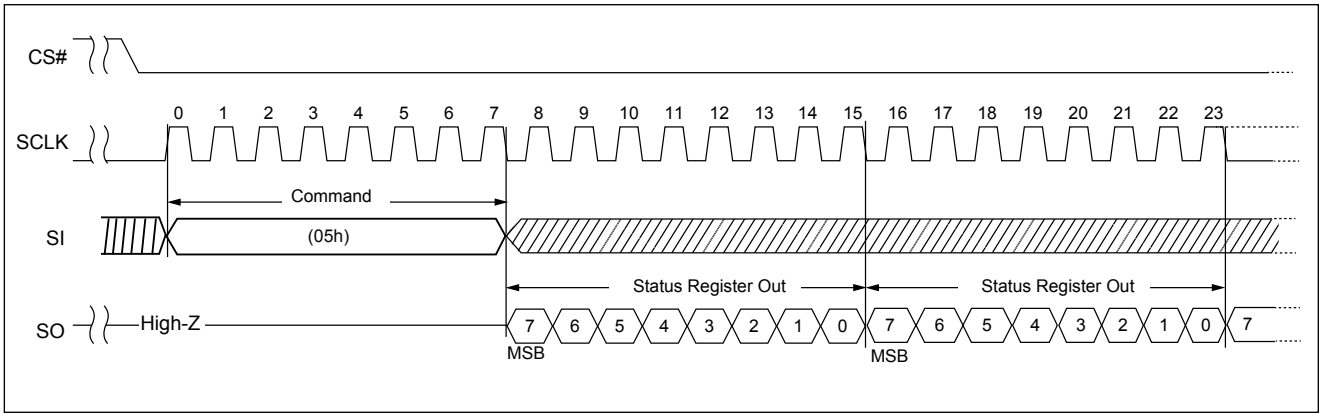
The Get Feature (0Fh) command with the feature address(C0h) will keep the device at the status read mode unless next valid command is issued. The resulting information is outlined as **"Table 18. Status Register Bit Descriptions"**.

15-3-2. Read Status command (RDSR)

In additional to read the chip status by Get Feature command, this device also supports the SPI NOR Read Status command (05h). The Read Status command can be issued any time (even during read/program/erase operation), it is recommended to check the Operation in Program (OIP) bit or Cache Read Busy (CRBSY) before sending a new instruction when a read, program or erase operation is in progress.

The sequence of issuing RDSR instruction is CS# goes low→ send RDSR instruction code →Status register data out on SO.

Figure 31. Read Status Register (RDSR)



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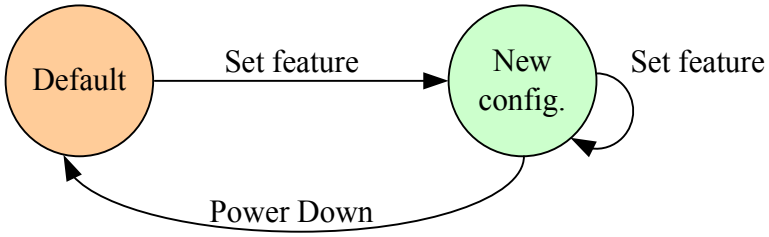
15-4. Configuration Feature Operation

15-4-1. Type: Volatile Register [Symbol: V]

Default value: can not be changed.

Set feature command to change configuration register.

Figure 32. Setting of Volatile Configuration Register

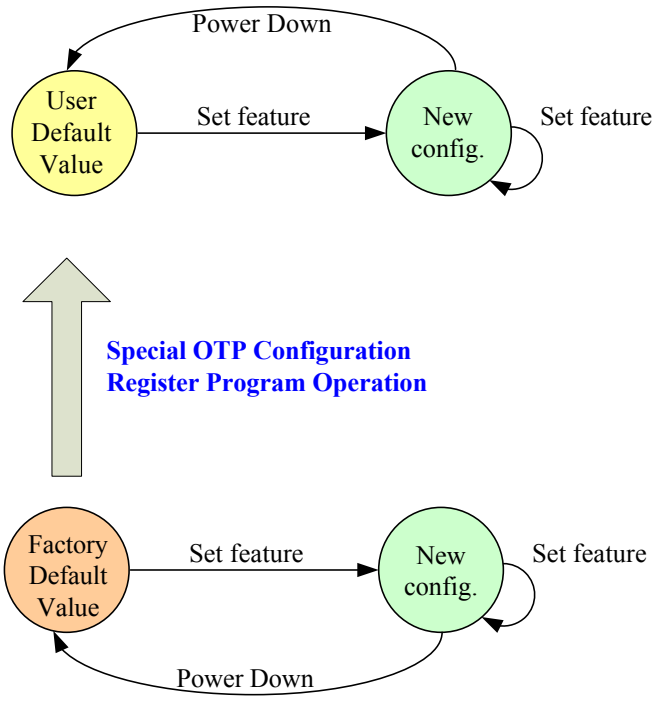


15-4-2. Type: Volatile Register with OTP Fuse Default Value [Symbol: V2]

Default value: can be changed by special OTP Configuration Register program operation.

Set feature command to change value of configuration register. Those configuration register bits of type V2 are: BFT[3:0], CONT, DS_IO[1:0].

Figure 33. Setting of Volatile Configuration Register (Type: V2)



15-4-3. Type: One-time Setting Register [Symbol: OTP]

- SPI_NOR_EN, OTPRWSP bit

The OTP Configuration Register bits can be only changed from 0 to 1 through Special OTP Configuration Register Program Operation.

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15-5. OTP "Configuration" Register Solid Protection (for V2/OTP type configuration register)

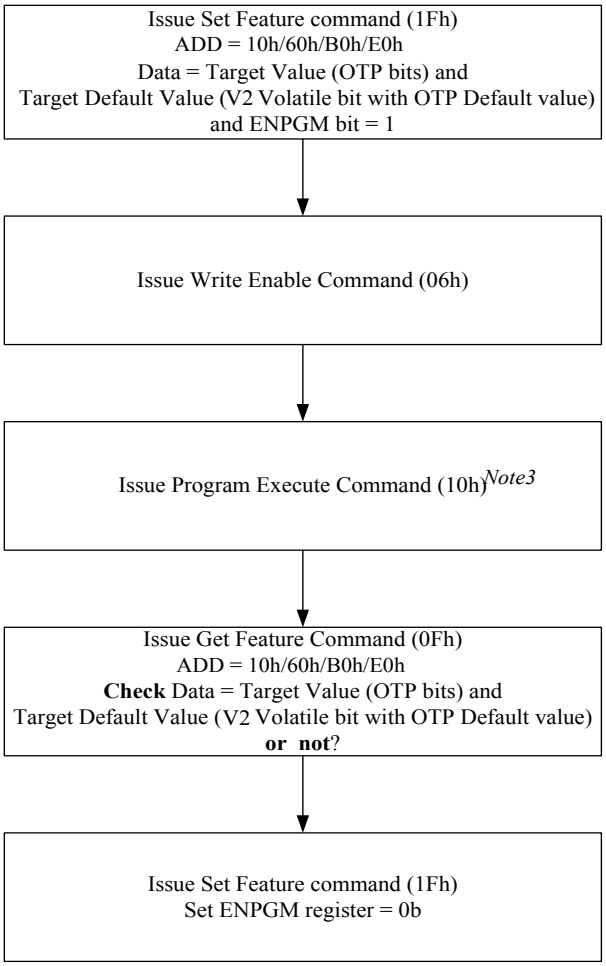
To avoid the OTP register bits and OTP Fuse value of V2 type Register bits to be programmed accidentally, this chip provide OTPRWSP (OTP register write solid protection) register to prevent it.

If OTPRWSP register bit is not programmed, the V2 type register (e.g.BFT[3:0], DS_IO[1:0]) and OTP type registers(e.g. SPI_NOR_EN) can be programmed; after the OTPRWSP register is programmed, the V2/OTP type registers can not be programmed anymore.

User should program OTPRWSP register even though they do not want to change the V2/OTP type register. This can avoid the accidental programming of the V2/OTP type register during later usage.

For those "V" type registers in the ADD=10h/60h/B0h/E0h, please must keep as "0" value while use the 'Special OTP configuration register program operation'.

Figure 34. Special OTP Configuration Register Program Operation (for V2/OTP Type of Configuration Register Bits)



Notes:

1. OTP Configuration Registers can be programmed together or individually by this programming flow.

2. It is recommended to program OTPRWSP register for V2 default value & OTP type Configuration Register solid protection. The related V2 default value & OTP type Configuration Registers can't be changed anymore, while OTPRWSP=1b.

3: Users need to check `OIP' bit to get device ready before get the new register data.

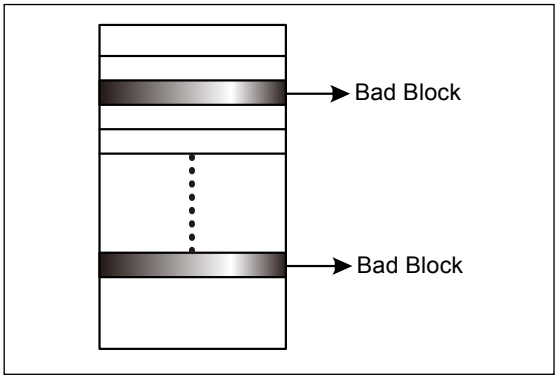
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16. SOFTWARE ALGORITHM

16-1. Invalid Blocks (Bad Blocks)

The bad blocks are included in the device while it gets shipped. During the time of using the device, the additional bad blocks might be increasing; therefore, it is necessary to check the bad block marks and avoid using the bad blocks. Furthermore, please read out the bad block information before any erase operation since the bad block marks may be cleared by any erase operation.

Figure 35. Bad Blocks



While the device is shipped, the value of all data bytes of the good blocks are FFh. The 1st byte of the 1st and 2nd page in the spare area for bad block will be 00h. The erase operation at the bad blocks is not recommended.

After the device is installed in the system, the bad block checking is recommended. **"Figure 36. Bad Block Test Flow"** shows the brief test flow by the system software managing the bad blocks while the bad blocks were found. When a block gets damaged, it should not be used any more.

Due to the blocks are isolated from bit-line by the selected gate, the performance of good blocks will not be impacted by bad ones.

Table 22. Valid Blocks

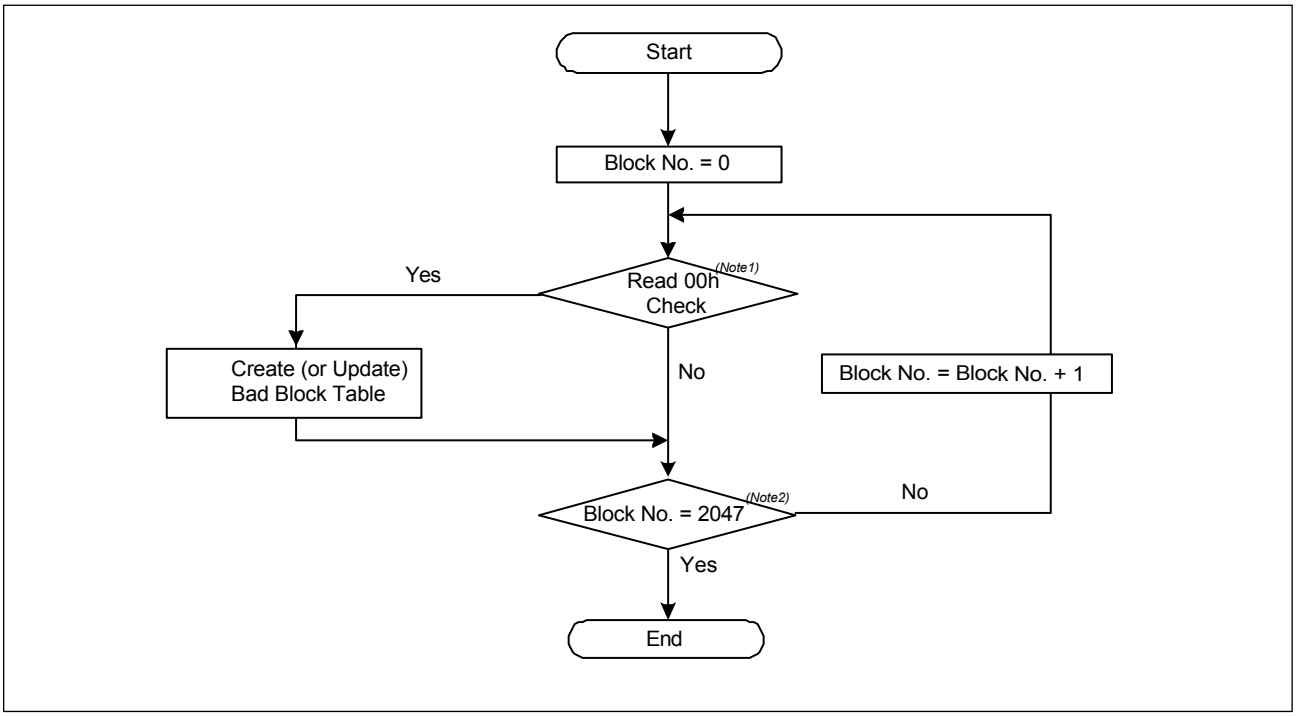
	Density	Min.	Typ.	Max.	Unit	Remark
Valid (Good) Block Number	1Gb	1004		1024	Block	Block 0 is guaranteed to be good (with internal ECC)
	2Gb	2008		2048	Block	Block 0 is guaranteed to be good (with internal ECC)

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16-2. Bad Block Test Flow

Although the initial bad blocks are marked by the flash vendor, they could be inadvertently erased and destroyed by a user that does not pay attention to them. To prevent this from occurring, it is necessary to always know where any bad blocks are located. Continually checking for bad block markers during normal use would be very time consuming, so it is highly recommended to initially locate all bad blocks and build a bad block table and reference it during normal Serial flash use. This will prevent having the initial bad block markers erased by an unexpected program or erase operation. Failure to keep track of bad blocks can be fatal for the application. For example, if boot code is programmed into a bad block, a boot up failure may occur. **"Figure 36. Bad Block Test Flow"** shows the recommended flow for creating a bad block table. There is a simple way to build the bad block table, by utilizing the internal "Bad Block management" table in the device and maintain the link of logical to physical block address.

Figure 36. Bad Block Test Flow



Note 1: *Read 00h check is at the 1st byte of the 1st and 2nd pages of the block spare area.*

Note 2: *Block No.=1023 for 1Gb*

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Bad Block Management Function

The BBM table supports 40 links.

The BBM table is an OTP Non-volatile memory

1. The BBM table is written by “Write BBM” command (A1h) and input the address of LBA & PBA, and then wait a tPROG time.
2. The user can read the BBM by “read BBM” command (A5h)

Figure 37. BBM Table

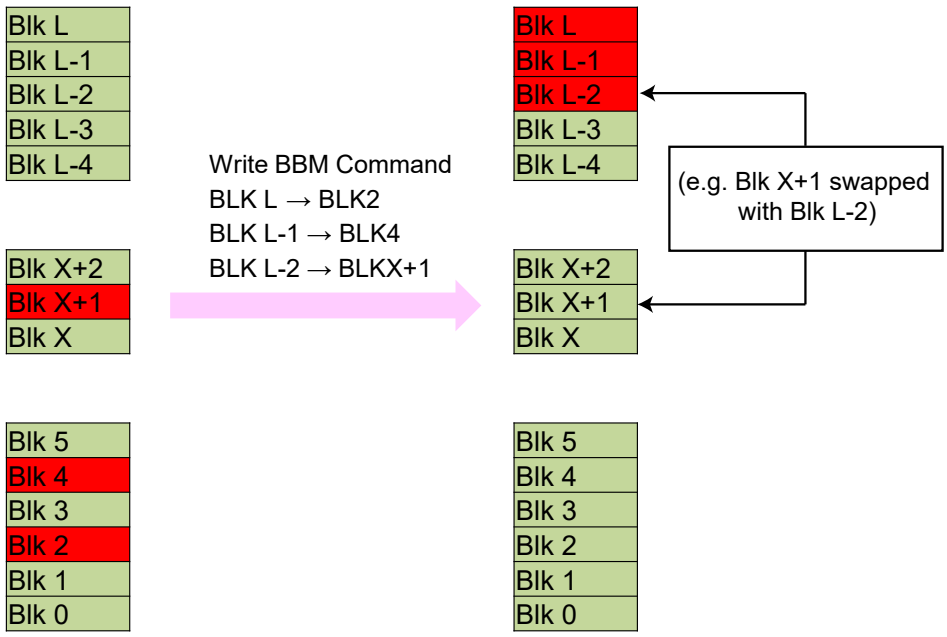
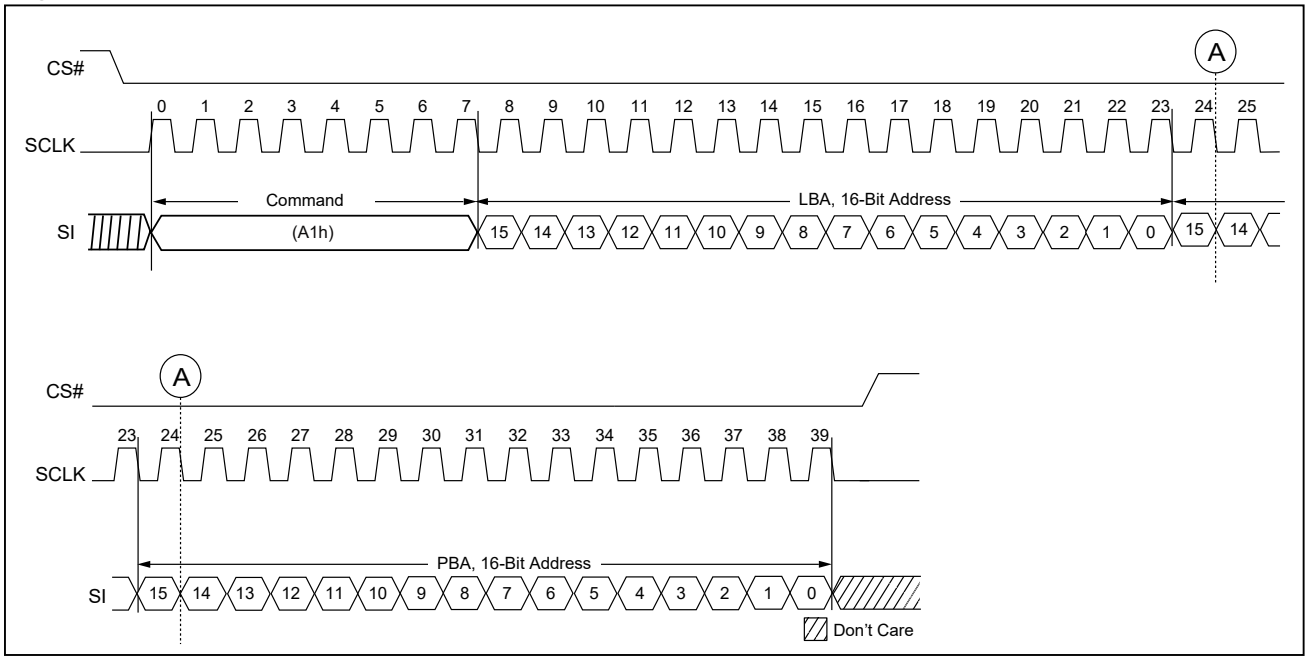
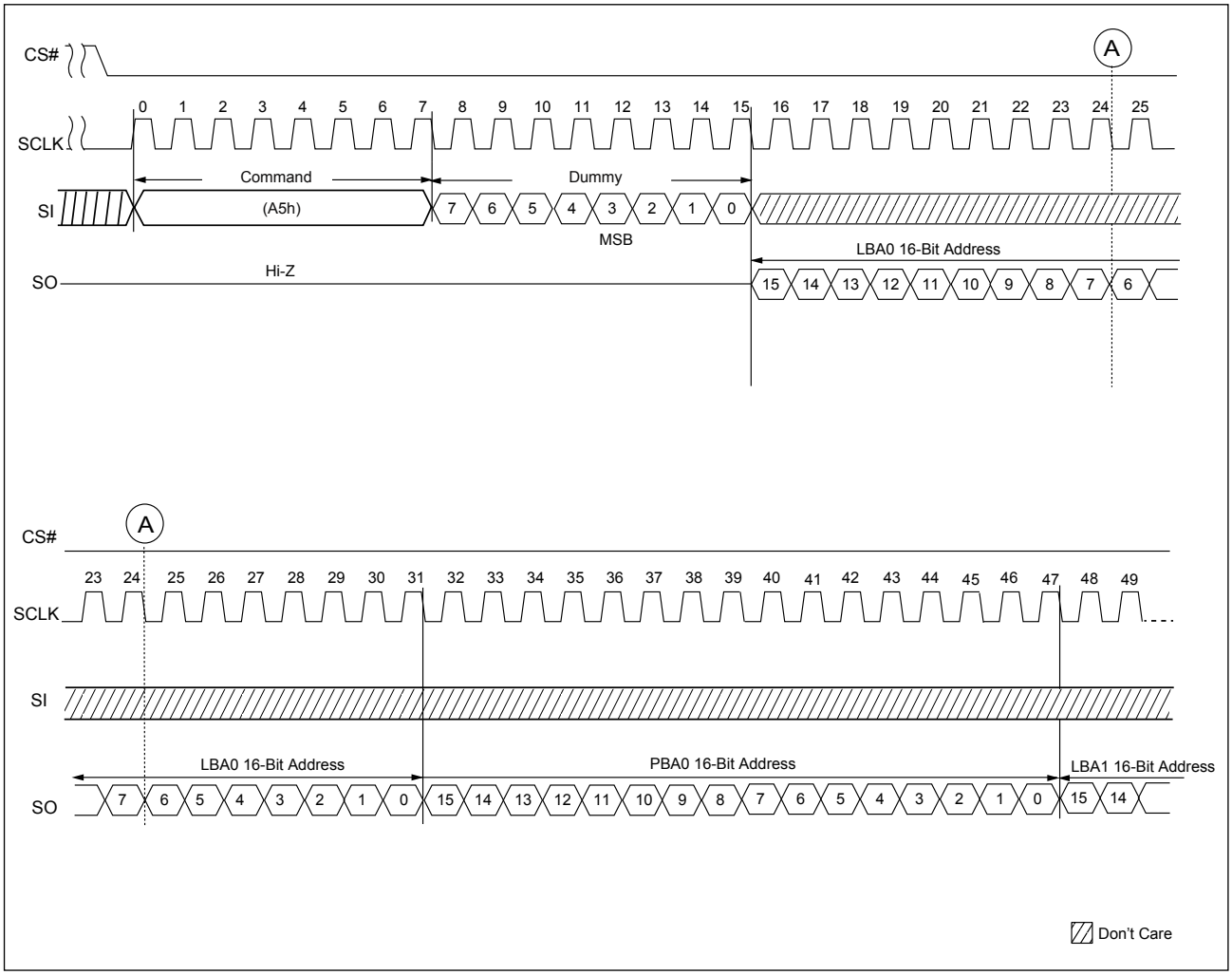


Figure 38. Write BBM Command (A1h)



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Figure 39. Read BBM Command (A5h)



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Figure 40. Bad Block Management

The user can read the BBM table full or not by “get feature” command for BBMT_F status bit.

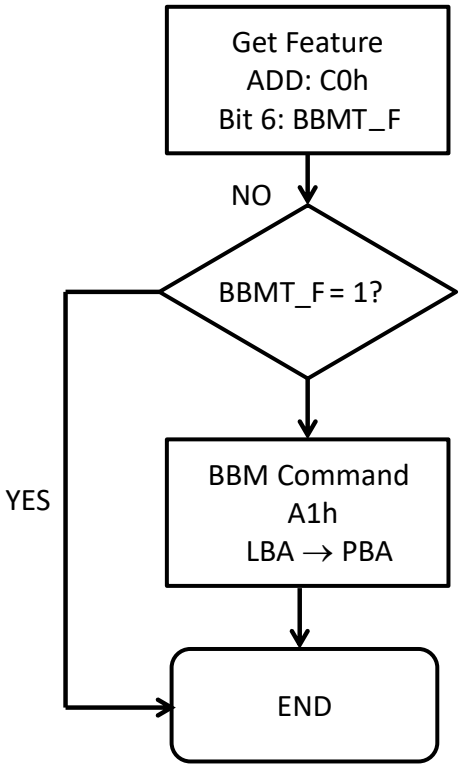


Table 23. BBM Address Definition

When user read out the BBM table, the LBA[15:14] has special meaning which indicates this link is enable and valid status.

ADD	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LBA[15:8]	ENABLE	INVALID	0	0	0	LRA[16]Note	LRA[15]	LRA[14]
LBA[7:0]	LRA[13]	LRA[12]	LRA[11]	LRA[10]	LRA[9]	LRA[8]	LRA[7]	LRA[6]
PBA[15:8]	0	0	0	0	0	PRA[16]Note	PRA[15]	PRA[14]
PBA[7:0]	PRA[13]	PRA[12]	PRA[11]	PRA[10]	PRA[9]	PRA[8]	PRA[7]	PRA[6]

Note: *LRA[16]/PRA[16] is not applicable for 1Gb.*

ENABLE	INVALID	Description
0	0	This link is not used
1	0	This link is enabled and valid
1	1	This link is enabled but invalid
0	1	This case does not exist

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16-3. Failure Phenomena for Read/Program/Erase Operations

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system:

Table 24. Failure Modes

Failure Mode	Detection and Countermeasure	Sequence
Erase Failure	**Status Read after Erase**	Block Replacement
Programming Failure	**Status Read after Program**	Block Replacement
Read Failure	**Read Failure**	Internal ECC. Host may move data to good block while internal ECC reaches the ECC threshold

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17. DEVICE POWER-UP

17-1. Power-up

After the Chip reaches the power on level, the internal power on reset sequence will be triggered. During the internal power on reset period, no any external command is accepted. The device can be fully accessible when VCC reaches the power-on level and wait 2ms.

During power-up, it is recommended that CS# should follow the voltage applied on VCC, and SCLK/SI/WP#/HOLD# should either keep low or follow the voltage applied on VCC.

Figure 41. Power Up/Down and Voltage Drop

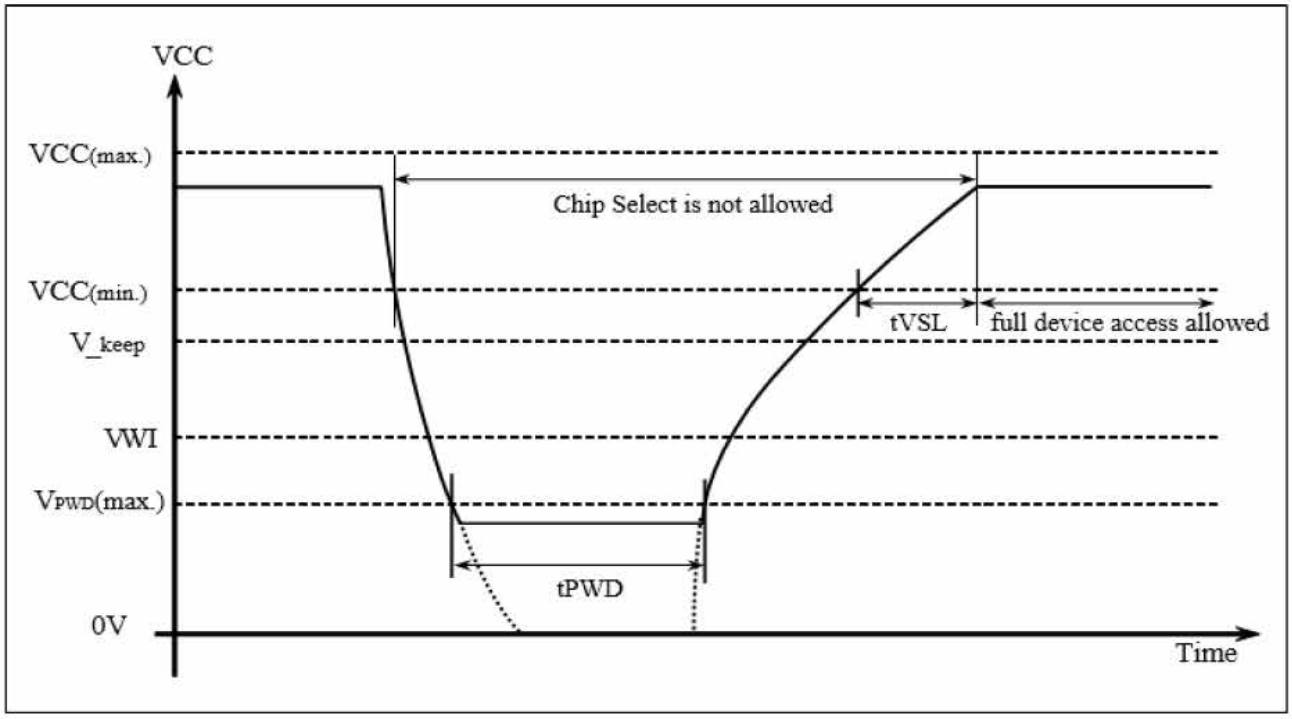


Table 25. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
V_{PWD}	VCC voltage needs to be below V_{PWD} for proper initialization to occur		0.9	V
$V_{_keep}$	Voltage threshold where re-initialization is necessary if VDD drop below to $V_{_KEEP}$	1.5		V
tPWD	The minimum duration to ensure initialization occurs	300		us
tVSL	VCC(min.) to device operation	2000		us
VCC	VCC Power Supply	1.7	1.95	V
VWI	Write Inhibit Voltage	1.0	1.5	V

Note: *These parameters are characterized only.*

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18. PARAMETERS

18-1. ABSOLUTE MAXIMUM RATINGS

Temperature under Bias	-50°C to +125°C
Storage temperature	-65°C to +150°C
All input voltages with respect to ground (Note 2)	-0.6V to 2.4V
VCC supply voltage with respect to ground (Note 2)	-0.6V to 2.4V
ESD protection	>2000V

Notes:

1. The reliability of device may be impaired by exposing to extreme maximum rating conditions for long range of time.

2. Permanent damage may be caused by the stresses higher than the "Absolute Maximum Ratings" listed.

3. During voltage transitions, all pins may overshoot Vss to -1.0V and VCC to +1.0V for periods up to 20n, please refer to **"Figure 42. Maximum Negative Operation"** *and* **"Figure 43. Maximum Positive Operation"**.

Figure 42. Maximum Negative Operation

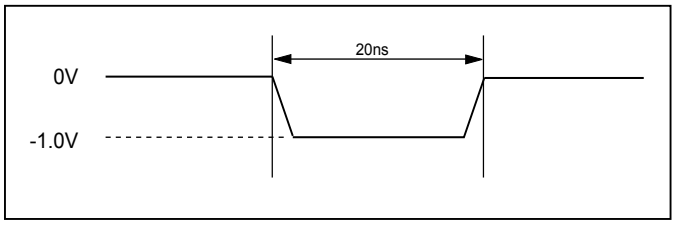
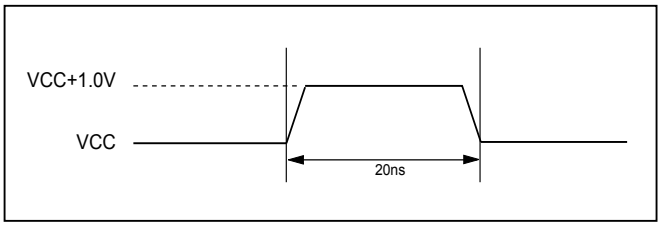


Figure 43. Maximum Positive Operation



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Table 26. AC Testing Conditions

Testing Conditions	Min.	Max.	Unit
Input Pulse Level	0	VCC	V
Output Load Capacitance (CL)	30		pF
Input Rising & Falling Time	-	2.5	ns
Input Timing Measurement Reference Levels	0.3VCC	0.7VCC	V
Output Timing Measurement Reference Levels	VCC/2		V

Figure 44. AC Measurement I/O Waveform

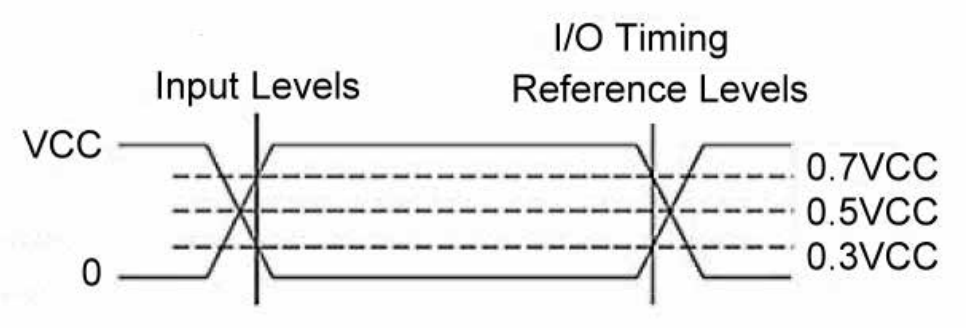


Table 27. Capacitance

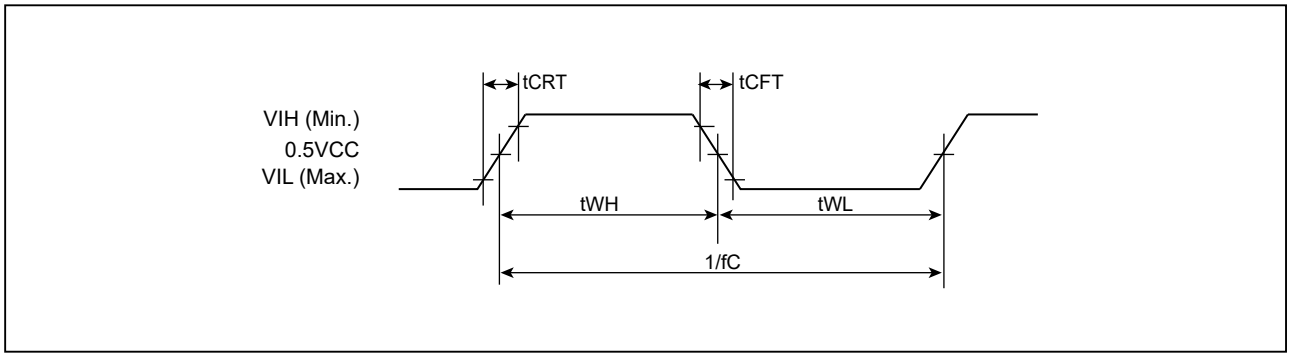
TA = +25°C, F = 1 MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
CIN	Input capacitance			10	pF	VIN = 0V
COUT	Output capacitance			10	pF	VOUT = 0V

Table 28. Operating Range

Temperature	VCC	Tolerance
-40°C to +85°C	+1.8V	1.7- 1.95V

Figure 45. SCLK TIMING DEFINITION



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Table 29. DC Characteristics

Symbol	Parameter	Min.	Typical	Max.	Unit	Test Conditions
ILI	Input leakage current			± 10	uA	VIN= 0 to VCC MAX
ILO	Output leakage current			± 10	uA	VOUT= 0 to VCC MAX
ISB1	VCC standby current (CMOS)			110	uA	VIN=VCC or GND, CS#=VCC
ICC1	VCC active current (Read for non-continuous read operation)			40	mA	f=104MHz, Iout = 0mA
				30	mA	f=80MHz, Iout = 0mA
ICC2	VCC active current (Read for continuous read operation)			40	mA	f=80MHz, Iout = 0mA
ICC3	VCC active current (Program)			40	mA	
ICC4	VCC active current (Erase)			30	mA	
VIL	Input low level	-0.3		0.2VCC	V	
VIH	Input high level	0.8VCC		VCC + 0.3	V	
VOL	Output low voltage			0.2	V	IOL= 1mA
VOH	Output high voltage	VCC-0.2			V	IOH= -20uA

Table 30. General Timing Characteristics

Symbol	Parameter	Note	Min.	Max.	Unit
fC	Serial Clock Frequency for all command	1, 2	D.C.	104	MHz
tCHHH	HOLD# Hold Time (relative to SCLK)		5	-	ns
tCHHL	HOLD Hold Time (relative to SCLK)		5	-	ns
tCS	CS# Diselect Time		30	-	ns
tCHSH	CS# Active Hold Time (relative to SCLK)		4	-	ns
tSLCH	CS# Active Setup Time (relative to SCLK)		4	-	ns
tSHCH	CS# Not Active Setup Time (relative to SCLK)		4	-	ns
tCHSL	CS# Not Active Hold Time (relative to SCLK)		4	-	ns
tDIS	Output Disable Time		-	20	ns
tHC	HOLD Setup Time (relative to SCLK)		5	-	ns
tHD	HOLD# Setup Time (relative to SCLK)		5	-	ns
tHDDAT	Data Input Hold Time		2	-	ns
tHO	Output Hold Time		1	-	ns
tHZ	HOLD# to Output High-Z		-	15	ns
tLZ	HOLD# to Output Low-Z		-	15	ns
tSUDAT	Data In Setup Time		2	-	ns
tV	Serial Clock Low to Output Valid (30pF)		-	8	ns
tWH	Serial Clock High Time		4	-	ns
tWL	Serial Clock Low Time		4	-	ns
tCRT	Clock Rise Time (peak to peak)		0.5		V/ns
tCFT	Clock Fall Time (peak to peak)		0.5		V/ns
tWPH	Write protect Hold Time		100	-	ns
tWPS	Write protect Setup Time		20	-	ns
tVSL	VCC(min.) to device operation		2		ms
tRST	Device Reset time (Idle/Read/Program/Erase)	-	-	6/6/10/500	us

Notes:

1. fC(max) is 20MHz for read from cache x1 (03h) if SPI NOR interface is enabled.

2. fC(max) is 80MHz for the continuous read operation.

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Table 31. Program/Read/Erase Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRD	Data transfer time from Serial Flash array to data register	-	-	80	us
tRD_OTP	Data transfer time from Serial Flash array to data register in secure OTP mode (internal ECC enabled)			85	us
tRCBSY	Dummy busy time for cache read	-	60	80	us
tPROG	Page Programming time	-	360	660	us
tERS	Block Erase Time	-	1	3.5	ms
NOP	Number of partial-page programming operation supported			4	Cycle

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Figure 46. WP# Setup Timing and Hold Timing during SET FEATURE when BPRWD=1

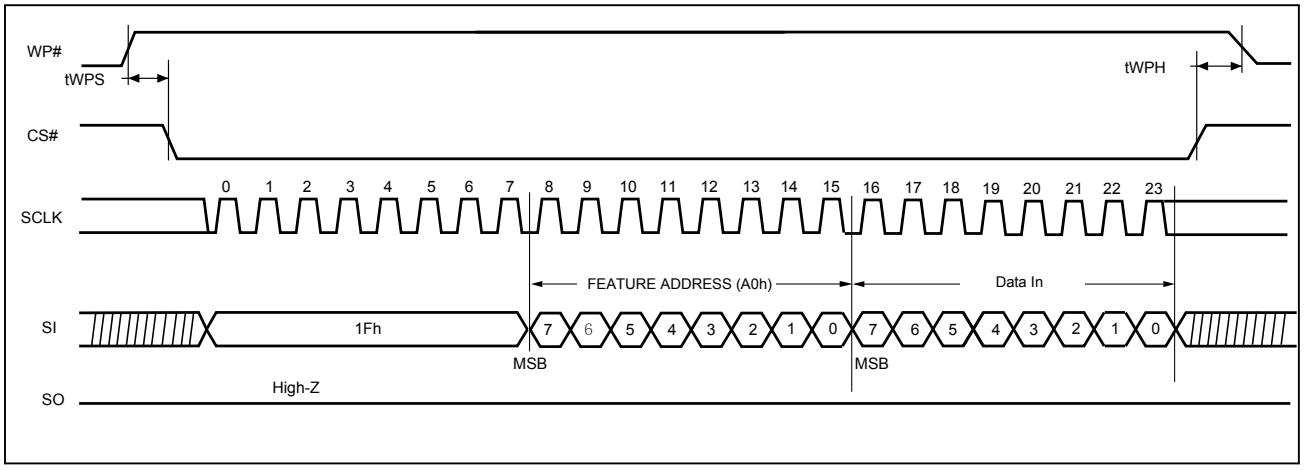


Figure 47. Serial Input Timing

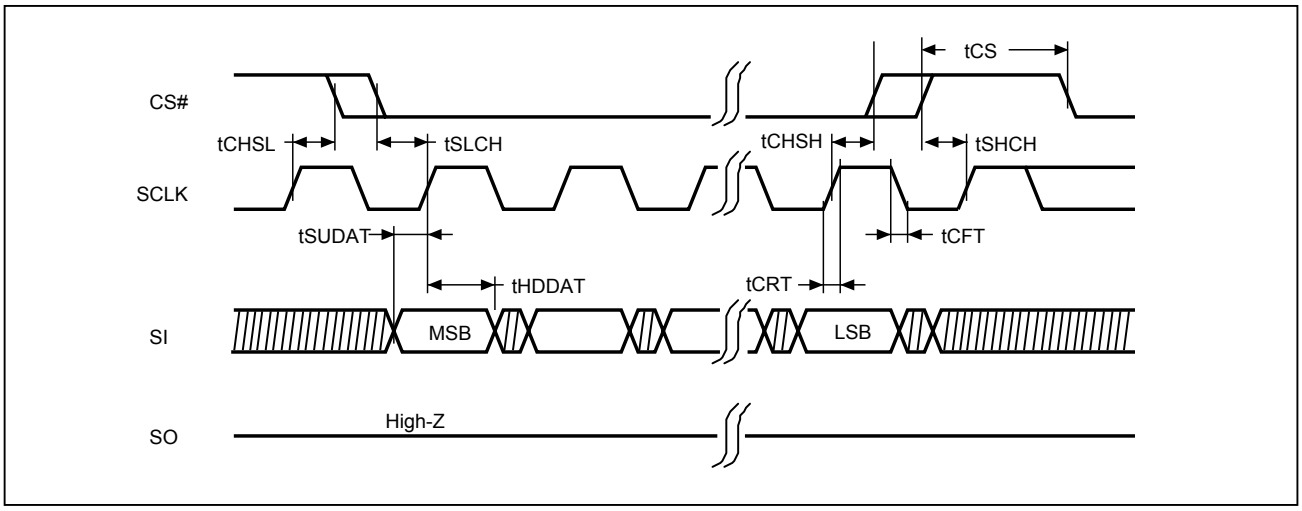
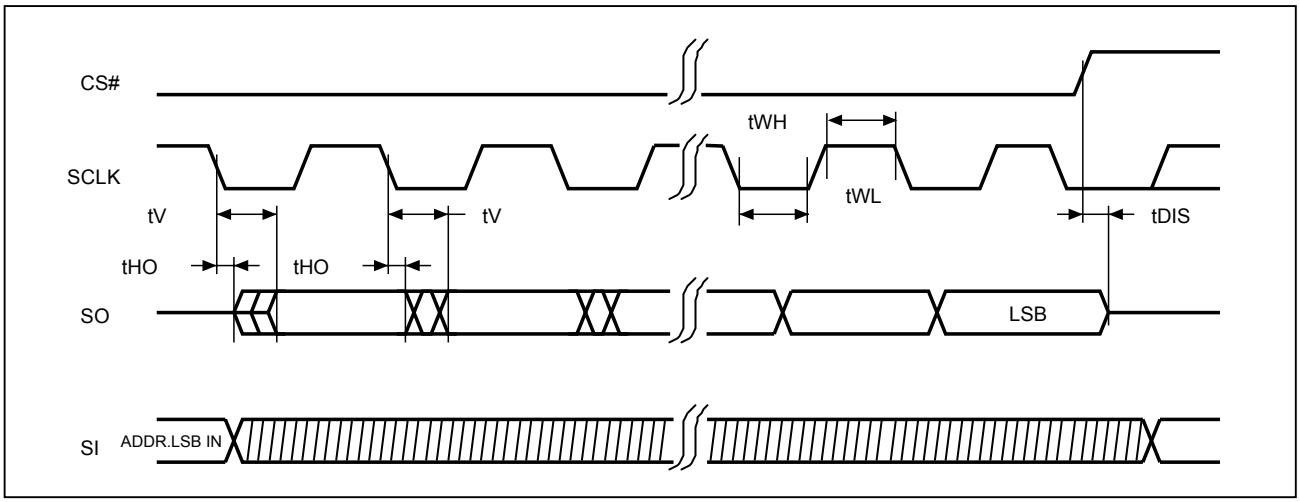
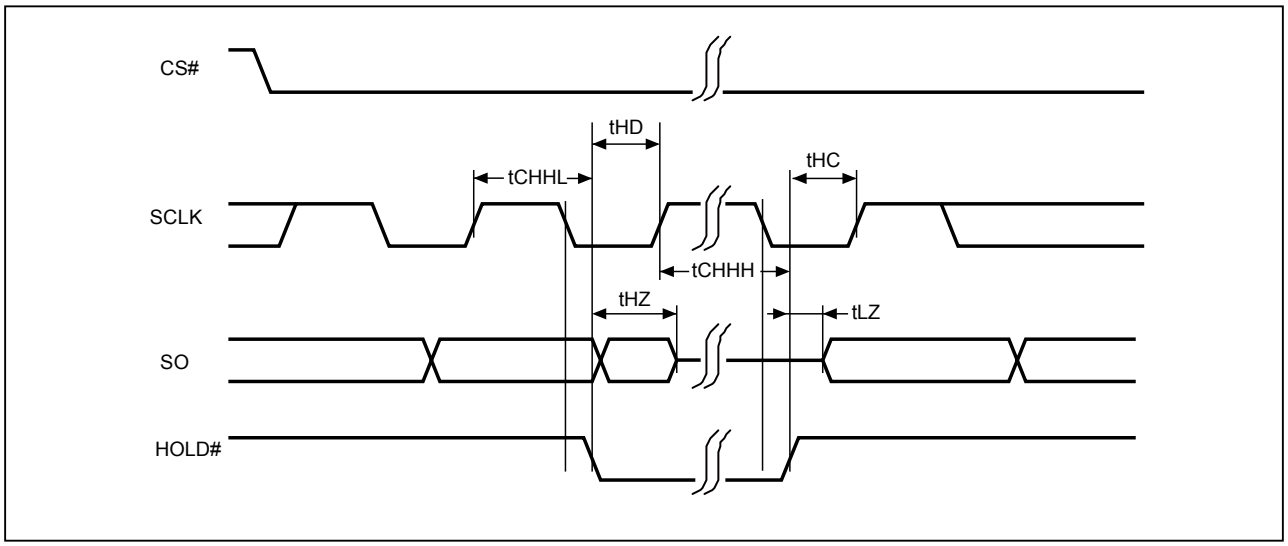


Figure 48. Serial Output Timing



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Figure 49. Hold Timing



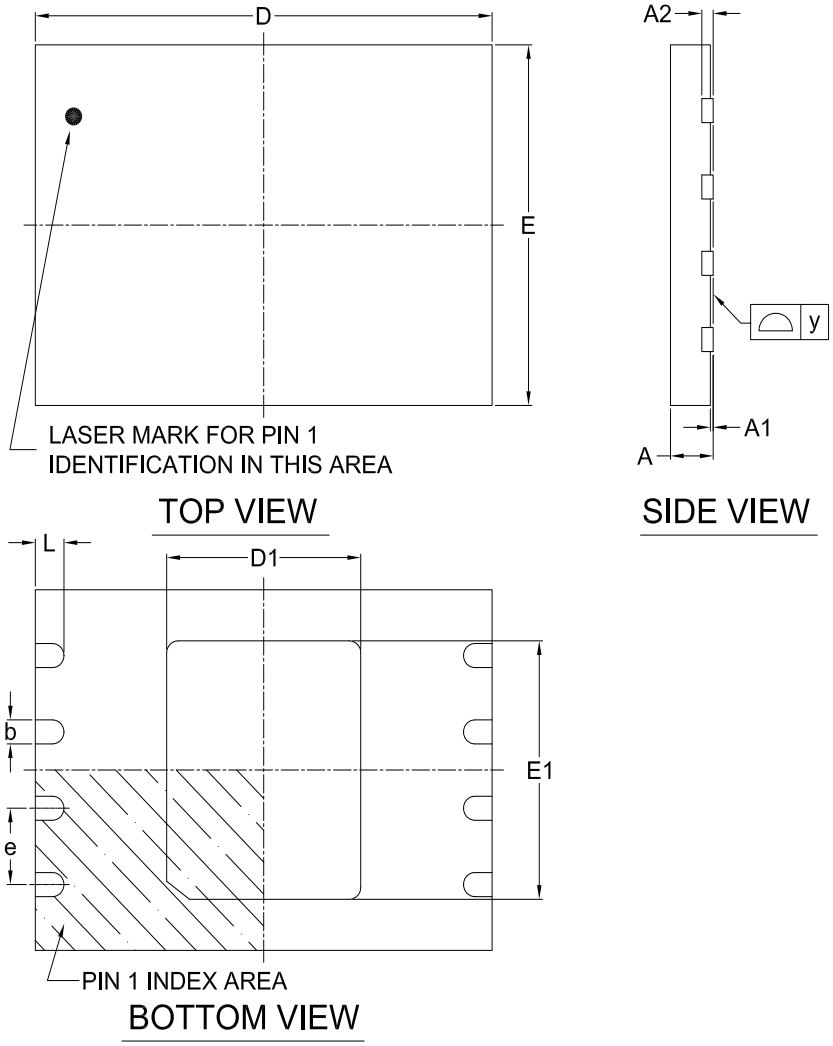
Note: *SI is "don't care" during HOLD operation.*

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19. PACKAGE INFORMATION

19-1. 8-WSON (8x6x0.8mm)

Doc. Title: Package Outline for WSON 8L (8x6x0.8MM, LEAD PITCH 1.27MM, E.P. 3.4x4.3MM)



Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

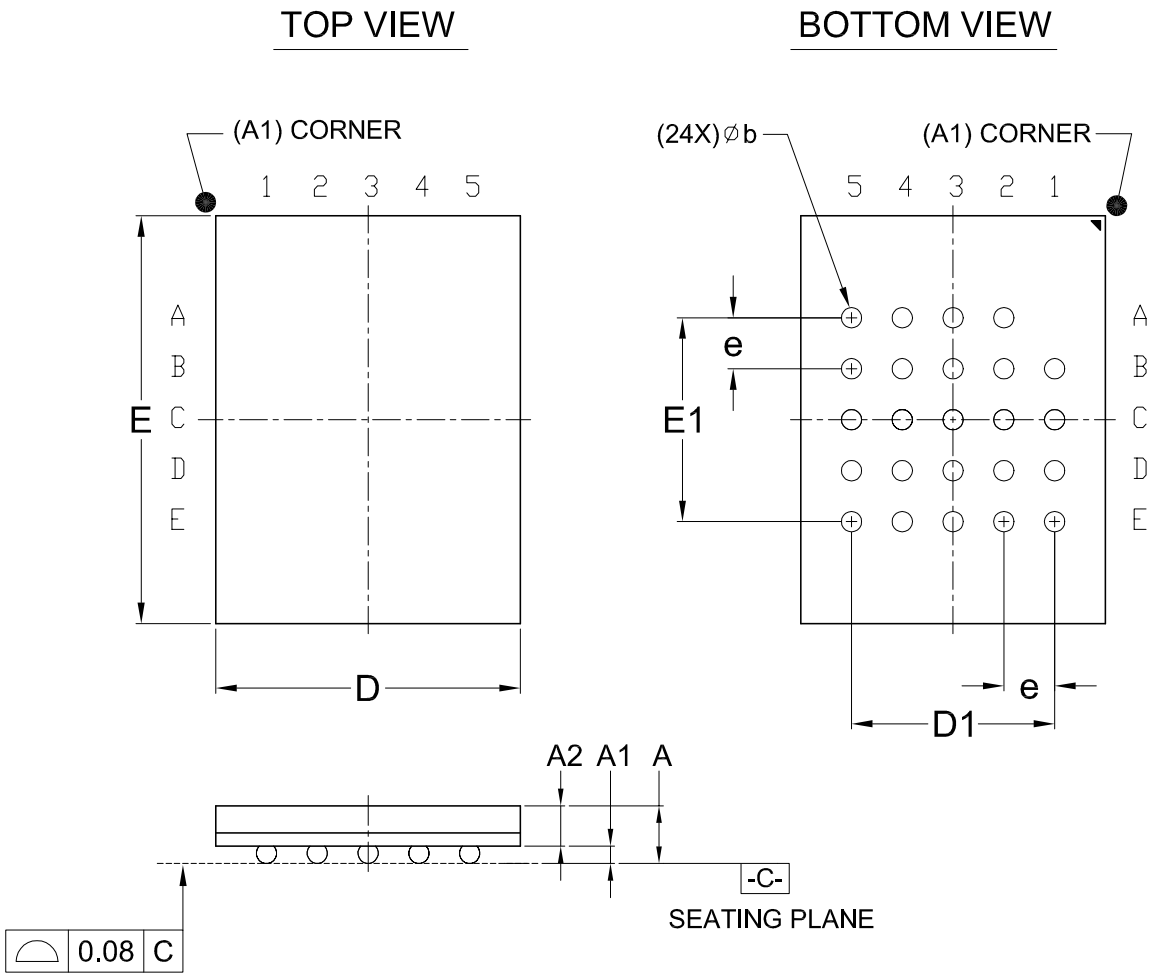
Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	7.90	3.35	5.90	4.25	0.45	---	0.00
	Nom.	---	---	0.20	0.40	8.00	3.40	6.00	4.30	0.50	1.27	---
	Max.	0.80	0.05	---	0.48	8.10	3.45	6.10	4.35	0.55	---	0.05
Inch	Min.	0.028	---	---	0.014	0.311	0.132	0.232	0.167	0.018	---	0.00
	Nom.	---	---	0.008	0.016	0.315	0.134	0.236	0.169	0.020	0.05	---
	Max.	0.032	0.002	---	0.019	0.319	0.136	0.240	0.171	0.022	---	0.002

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19-2. 24-BGA (6x8x1.2mm)

Doc. Title: Package Outline for CSP 24BALL (6x8x1.2MM, BALL PITCH 1.0MM, BALL DIAMETER 0.4MM, 5x5 BALL ARRAY)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90	---	7.90	---	---
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	4.00	1.00
	Max.	1.20	0.35	---	0.45	6.10	---	8.10	---	---
Inch	Min.	---	0.010	0.026	0.014	0.232	---	0.311	---	---
	Nom.	---	0.012	---	0.016	0.236	0.157	0.315	0.157	0.039
	Max.	0.047	0.014	---	0.018	0.240	---	0.319	---	---

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20. REVISION HISTORY

Revision	Descriptions	Page
September 18, 2019		
0.00	Initial Release	ALL
June 05, 2020		
0.01	1. Title changed as “Preliminary”	ALL
	2. Revised package type of 2Gb from 8-WLGA to 8-WSON	P8, 9, 71
	3. Added RDSR command (05h), SPI_NOR_EN, NOR4BADD, OTPRWSP functions	P12, 14, 16, 23, 27, 30-38, 40, 43, 47, 49, 52, 54, 59-60
	4. Correction on oversights	P13, 16, 40-43, 52, 58, 60, 65, 67
	5. Supplement of WEL bit in Table 13, the bit value will be cleared (as "0") by issuing Write Disable command(04h) or after the program/ erase operation completion	P53
	6. Added Figure of SCLK Timing Definition	P66
	7. Improved ICC3 from 40mA to 30mA, adjusted condition of VOL/VOH	P67
	8. Added tCRT/tCFT in Table of General Timing Characteristics	P67
	9. Improved tRD from 85us to 80us and tRCBSY from 65(typ)/85(max.) to 60(typ)/80(max)	P68
September 21, 2020		
0.02	1. Added Continuous read and BBM link function	P6-7, 12-14, 16, 27, 34-37, 48-49, 54, 58-60, 65
	2. Added "Read ECC Warning Page Address" function	P41
	3. Terminology alignment	P14, 54
	4. Removal of "NOR4BADD" function	P30-38, 54-55
	5. Corrected Table of BFT[3:0]	P40
	6. Supplement "P_FAIL" & "E_FAIL" description	P48
	7. Added Figure and Table for power-Up/Down and Voltage drop	P62
February 18, 2021		
1.0	1. Removed "Preliminary" document title	ALL
	2. Added Note 4 of Table 2 and Note of Table 20	P14, 60
	3. Corrected the definition of Table11	P40
	4. Supplement of V2 in the Figure 34	P55
	5. Re-organized the ICC parameters to add VCC active current (Read for continuous read operation)	P65

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Revision	Descriptions	Page
January 24, 2022		
1.1	1. Corrected the misprints of Figure 1	P7
	2. Added note of 'Advanced information on XDI part name	P8
	3. Added **"Table 5. Register status of Reset (FFh) command operation"**	P15
	4. Re-phrase on ECC segment description and re-organized **"Table 15. The Distribution of ECC Segment and Spare Area"**	P39
	5. Supplement of 'special OTP configuration register program operation' and added Note 3	P56
	6. Removal statement of WP# keeps low at power-on/off on 'DEVICE POWER-UP' section and supplement on the state of CS#/SCLK/SI/WP#/HOLD# during power-up	P63
July 28, 2022		
1.2	1. Supplement tables for the definition of RADD/CADD for address mapping	P11
	2. Correction of the missing footnotes of **"Table 9. Command Set - Continuous Read Operation Enabled"**	P29
	3. Supplement the page program in a block should start from low address to high address	P43

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