3V, 1G-bit/2G-bit/4G-bit Serial NAND Flash Memory

MX35LFxG24AD

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Contents

1. FEATURES 5

2. GENERAL DESCRIPTIONS 6

Figure 1. Logic Diagram 6

3. ORDERING INFORMATION 7

4. BALL ASSIGNMENT AND DESCRIPTIONS 8

Figure 2. 8-WSON (8x6mm) 8

5. PIN DESCRIPTIONS 8

6. DEVICE OPERATION 9

Figure 3. Serial Mode Supported 9

7. ADDRESS MAPPING 10

8. COMMAND DESCRIPTION 11

Table 1. Command Set 11

8-1. WRITE Operations 12

8-1-1. Write Enable 12

Figure 4. Write Enable (WREN) Sequence 12

8-1-2. Write Disable (04h) 12

Figure 5. Write Disable (WRDI) Sequence 12

8-2. Feature Operations 13

8-2-1. GET Feature (0Fh) and SET Feature (1Fh) 13

Table 2-1. Configuration Registers 13

Table 2-2. I/O Strength Feature Table 13

Figure 6. GET FEATURE (0Fh) Timing 14

Figure 7. SET FEATURE (1Fh) Timing 14

8-3. READ Operations 15

8-3-1. PAGE READ (13h) 15

8-3-2. QE Bit 15

Figure 8. PAGE READ (13h) Timing x1 16

Figure 9. READ FROM CACHE (03h or 0Bh) Timing 17

Figure 10. READ FROM CACHE x 2 18

Figure 11. Read From Cache Dual IO 1-2-2 19

Figure 12. READ FROM CACHE x 4 20

Figure 13. Read From Cache Quad IO 1-4-4 21

8-3-3. Page Read Cache Random (30h)/Page Read Cache Sequential (31h)/Page Read Cache End (3Fh) 22

Figure 14. Page Read Cache Random (30h) 22

Figure 15. Page Read Cache Sequential (31h) 23

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Figure 16. Page Read Cache End (3Fh) 24
Figure 17. Page Read Cache Flow 25
8-3-4. Special Read for Data Recovery 26
Figure 18. Procedure of Entering/Exiting the Special Read for Data Recovery operation 26
Table 3. Feature Settings 27
8-3-5. Randomizer Operation 27
Table 4. The definition of RANDOPT bit for the randomized area per page 27
Figure 19. Flowchart of RANDEN and RANDOPT Bits Program Operation 28

9. SPI NOR Compatible Command (Only for 1Gb/2Gb) 29
Table 5. Command Set - SPI NOR Like Protocol Enabled 29
Figure 20. Read From Cache x1 (NOR like) 30
Figure 21. Read From Cache x1 (Alternative, NOR like) 31
9-3-1. READ ID (9Fh) 32
Table 6. READ ID Table 32
Figure 22. READ ID (9Fh) Timing 32
9-1. Parameter Page 33
Table 7-1. Parameter Page Data Structure (MX35LF1G24AD) 33
Table 7-2. Parameter Page Data Structure (MX35LF2G24AD) 35
Table 7-3. Parameter Page Data Structure (MX35LF4G24AD) 37
9-2. UniqueID Page with PUF Type Code Structure 39
9-3. Program Operations 40
9-3-1. PAGE PROGRAM 40
Figure 23. PROGRAM LOAD (02h) Timing 40
Figure 24. PROGRAM LOAD RANDOM DATA (84h) Timing 41
9-3-2. QUAD IO PAGE PROGRAM 42
Figure 25. PROGRAM LOAD X4 (32h) Timing 42
Figure 26. PROGRAM EXECUTE (10h) Timing 43
Figure 27. QUAD IO PROGRAM RANDOM INPUT (34h) Timing 44

10. BLOCK OPERATIONS 45
10-1. Block Erase (D8h) 45
Figure 28. Block Erase (BE) Sequence 45

11. Feature Register 46
11-1. Configuration Feature Operation 46
11-1-1. Type: Volatile Register [Symbol: V] 46
11-1-2. Type: Volatile Register with OTP Fuse Default Value [Symbol: V2] 46
11-1-3. Type: One-time Setting Register [Symbol: OTP] 46
Figure 29. Setting of Volatile Configuration Register 46
Figure 30. Setting of Volatile Configuration Register (Type: V2) 46

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11-2. OTP "Configuration" Register Solid Protection (for 1Gb/2Gb) 47
11-3. Block Protection Feature 48
Table 8. Definition of Protection Bits 49
11-4. Secure OTP (One-Time-Programmable) Feature 50
Table 9. Secure OTP States 50
11-5. Status Register 51
Table 10. Status Register Bit Descriptions 51
12. SOFTWARE ALGORITHM 52
12-1. Invalid Blocks (Bad Blocks) 52
Figure 31. Bad Blocks 52
Table 11. Valid Blocks 52
12-2. Bad Block Test Flow 53
Figure 32. Bad Block Test Flow 53
12-3. Failure Phenomena for Read/Program/Erase Operations 53
Table 12. Failure Modes 53
13. DEVICE POWER-UP 54
13-1. Power-up 54
Figure 33. Power On Sequence 54
14. PARAMETERS 55
14-1. ABSOLUTE MAXIMUM RATINGS 55
Figure 34. Maximum Negative Overshoot Waveform 55
Figure 35. Maximum Positive Overshoot Waveform 55
Table 13. AC Testing Conditions 56
Table 14. Capacitance 56
Table 15. Operating Range 56
Figure 36. SCLK TIMING DEFINITION 56
Table 16. DC Characteristics 57
Table 17. General Timing Characteristics 57
Table 18. Program/ Read/ Erase Characteristics 58
Figure 37. WP# Setup Timing and Hold Timing during SET FEATURE when BPRWD=1 59
Figure 38. Serial Input Timing 59
Figure 39. Serial Output Timing 59
Figure 40. Hold Timing 60
15. PACKAGE INFORMATION 61
15-1. 8-WSON (8x6x0.8mm) 61
16. REVISION HISTORY 62

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1. FEATURES

- **1Gb/2Gb/4Gb SLC NAND Flash**
  - Bus: x4
  - 1Gb/2Gb:
    Page size: (2048+128) byte,
    Block size: (128K+8K) byte
  - 4Gb: Page size: (4096+256) byte,
    Block size: (256K+16K) byte
- **8-bit ECC/ 544B is required**
- **Fast Read Access**
  - Supports data read by x1 x2 & x4 modes, (1-1-1,1-1-2, 1-1-4, 1-2-2, 1-4-4)[Note 1]
  - Latency of array to register: 25us
  - Frequency: 120MHz
- **Page Program Operation**
  - Page program time: 320us(typ.)
- **Block Erase Operation**
  - Block erase time: 4ms(typ.)
- **Single Voltage Operation:**
  - VCC: 2.7 to 3.6V
- **BP bits for Block group protection**
- **Unique ID Read with PUF type code structure**
- **Low Power Dissipation**
  - Max. 30mA
    Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max.) standby current
- **High Reliability**
  - Randomizer (default disable): enabled by Set Feature
  - Special Read for data recovery : enabled by Set Feature
  - Program / Erase Endurance: Typical 60K cycles (with 8-bit ECC per 512+32) Byte
  - Data Retention: 10 years[Note2]
- **Wide Temperature Operating Range**
  -40°C to +85°C
- **Package:**
  8-WSON (8x6mm)
  All packaged devices are RoHS Compliant and Halogen-free.

Notes:

1. Which indicates the number of I/O for command, address and data.

2. Please contact Macronix for Reliability report on the detailed condition of retention test.

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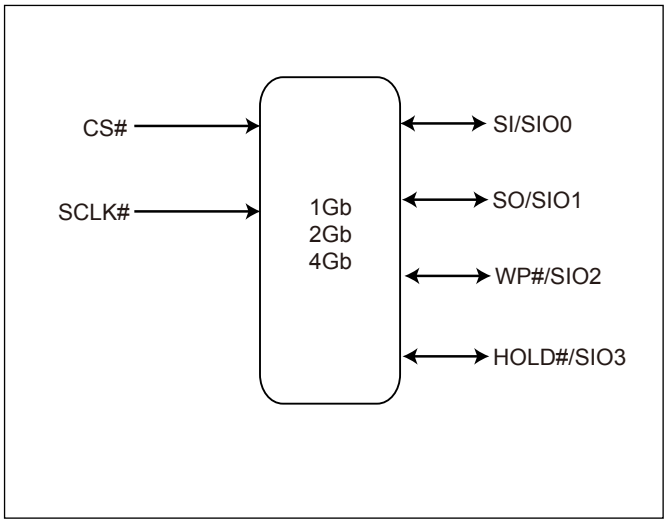
2. GENERAL DESCRIPTIONS

The MX35LFxG24AD is a 1Gb/2Gb/4Gb SLC NAND Flash memory device with Serial interface.

The memory array of this device adopted the same cell architecture as the parallel NAND, however implementing the industry standard serial interface.

The device needs the micro controller of host side to support 8-bit ECC/544-byte operation.

Figure 1. Logic Diagram

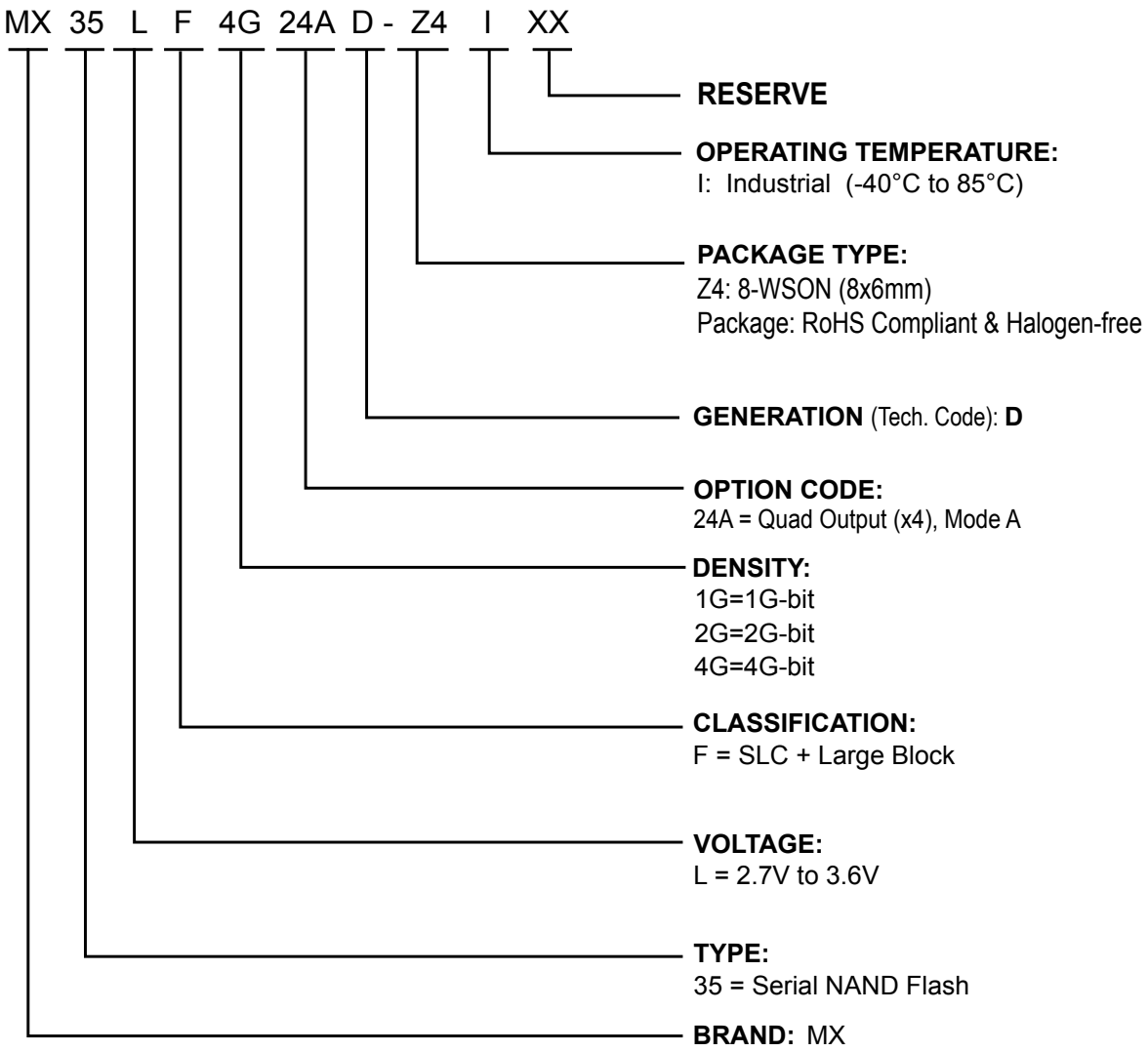


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3. ORDERING INFORMATION

Part Name Description

Macronix NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Macronix's product search at http://www.Macronix.com. Contact Macronix sales for devices not found.



Please contact Macronix regional sales for the latest product selection and available form factors.

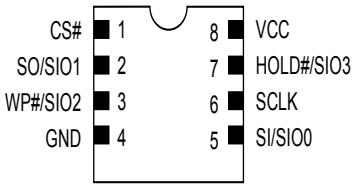
Part Number	Density	Organization	VCC Range	Package	Temperature Grade
MX35LF4G24AD-Z4I	4Gb	x4	3V	8-WSON	Industrial
MX35LF2G24AD-Z4I*	2Gb	x4	3V	8-WSON	Industrial
MX35LF1G24AD-Z4I*	1Gb	x4	3V	8-WSON	Industrial

* : Preliminary stage.

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4. BALL ASSIGNMENT AND DESCRIPTIONS

Figure 2. 8-WSON (8x6mm)



5. PIN DESCRIPTIONS

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (For 1-1-2,1-1-4, 1-2-2, or 1-4-4 note1 mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (For 1-1-2,1-1-4, 1-2-2, or 1-4-4 note1 mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (For 1-1-4 or 1-4-4note1 mode)
HOLD#/SIO3	Hold or Serial Data Input & Output (For 1-1-4 or 1-4-4note1 mode)
VCC	+ 3V Power Supply
GND	Ground

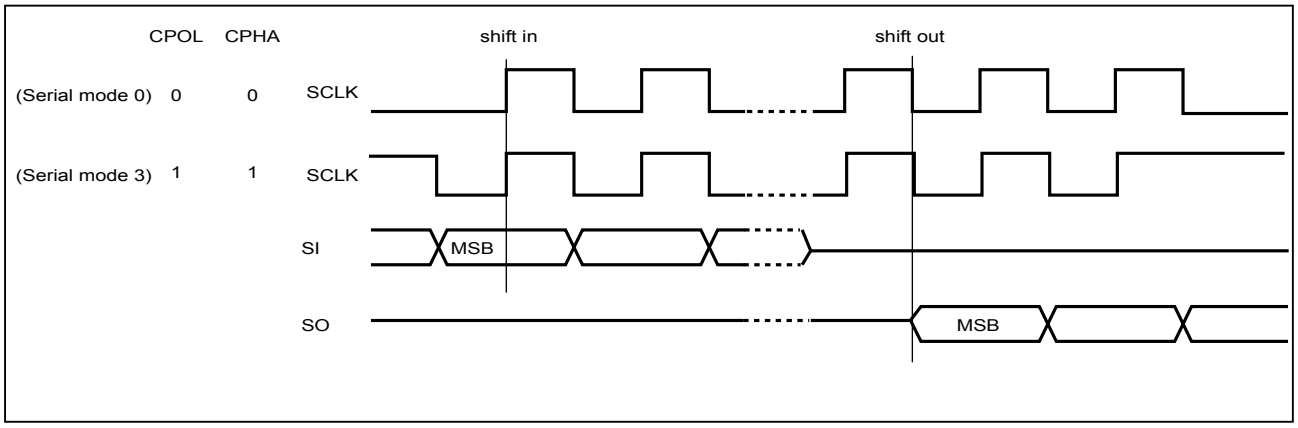
***Note 1**. Which indicates the number of I/O for command, address, and data.*

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6. DEVICE OPERATION

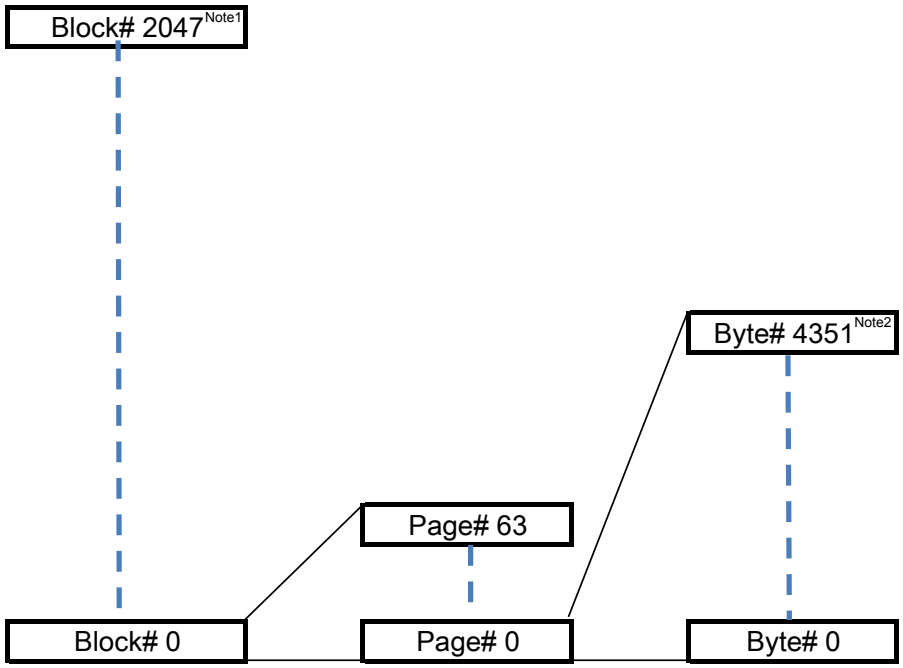
1. Before a command is issued, status register should be checked via get features operations to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as **"Figure 3. Serial Mode Supported"**.
5. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 3. Serial Mode Supported



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7. ADDRESS MAPPING



Block address	Page address	Byte address
RA [16:6]	RA [5:0]	CA [12:0]Note3

Note1: *1023 for 1Gb*

Note2: *Byte#=2175 for 1Gb/2Gb*

Note3: *CA[11] for 1Gb/2Gb*

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8. COMMAND DESCRIPTION

Table 1. Command Set

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	7th Byte	8th Byte	9th Byte
Get Feature	0Fh	ADD	Data						
Set Feature	1Fh	ADD	Data						
Page Read	13h	RADD2	RADD1	RADD0					
Page Read cache random	30h	RADD2	RADD1	RADD0					
Page Read cache sequential	31h								
Page Read cache last	3Fh								
Read From Cache x1	03h	CADD1	CADD0	DUMMY	DATA~				
Read From Cache x1 (alternative)	0Bh	CADD1	CADD0	DUMMY	DATA~				
Read From Cache x2Note	3Bh	CADD1	CADD0	DUMMY	DATA~(2)				
Read From Cache x4Note	6Bh	CADD1	CADD0	DUMMY	DATA~(4)				
Read From Cache Dual IO 1-2-2Note	BBh	CADD1(2)	CADD0(2)	DUMMY(2)	DATA~(2)				
Read From Cache Quad IO 1-4-4Note	EBh	CADD1(4)	CADD0(4)	DUMMY(4)	DUMMY(4)	DATA~(4)			
Read ID	9Fh	DUMMY	MID	DID1	DID2				
Block Erase	D8h	RADD2	RADD1	RADD0					
Program execute	10h	RADD2	RADD1	RADD0					
Program Load x1	02h	CADD1	CADD0	DATA~					
Program Load random data x1	84h	CADD1	CADD0	DATA~					
Program Load x4Note	32h	CADD1	CADD0	DATA~(4)					
Program Load random data x4Note	34h	CADD1	CADD0	DATA~(4)					
Write enable	06h								
Write disable	04h								
Reset	FFh								

Note: (2) stands for the dual I/O mode and (4) for quad I/O mode

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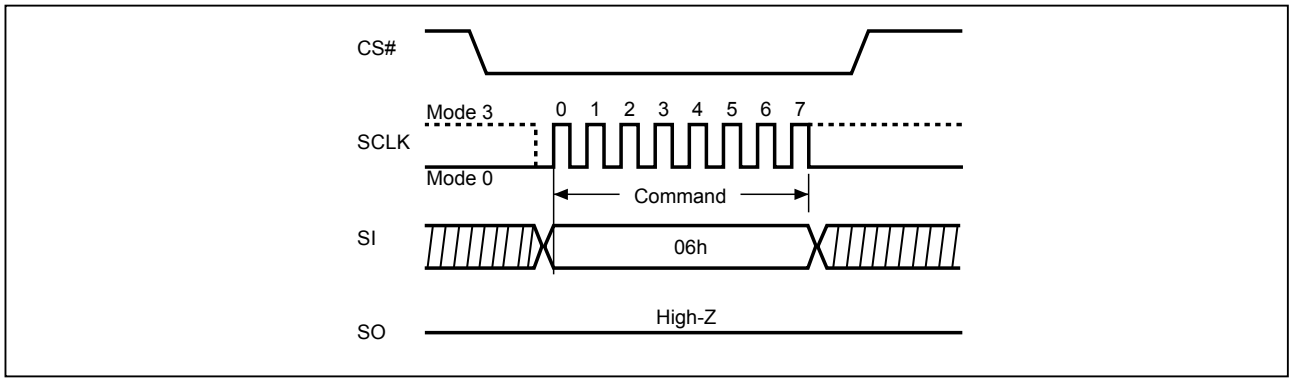
8-1. WRITE Operations

8-1-1. Write Enable

The Write Enable (WREN, 06h) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like Page Program, Secure OTP program, Block Erase, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Figure 4. Write Enable (WREN) Sequence



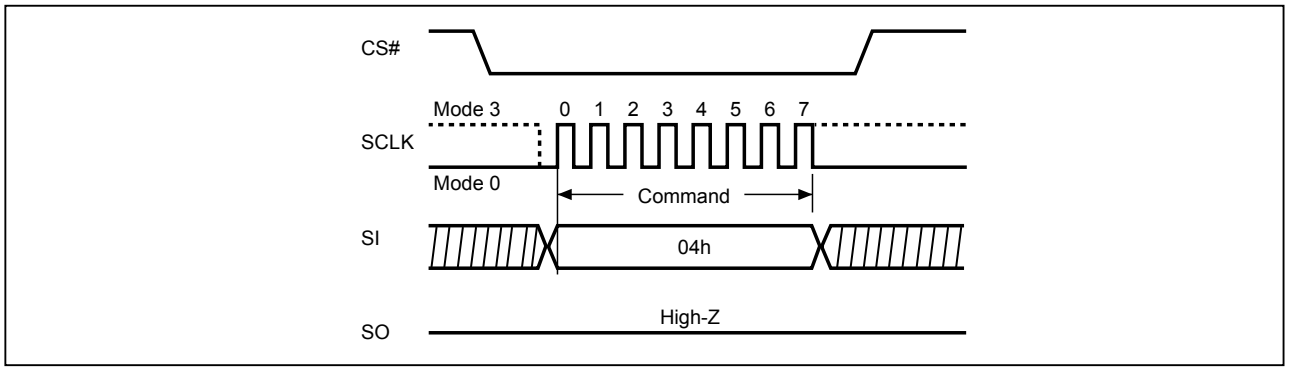
8-1-2. Write Disable (04h)

The Write Disable (WRDI, 04h) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high. It disables the following operations:

- Block Erase
- Secure OTP program
- Page program

Figure 5. Write Disable (WRDI) Sequence



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8-2. Feature Operations

8-2-1. GET Feature (0Fh) and SET Feature (1Fh)

By issuing a one byte address into the feature address, the device may then decide if it's a feature read or feature modification. (0Fh) is for the "GET FEATURE"; (1Fh) is for the "SET FEATURE".

The RESET command (FFh) will clear the status and special read for data recovery registers, the other feature registers remain until the power is being cycled or modified by the settings in the table below. After a RESET command (FFh) is issued, the Status register OIP bit0 or CRBSY will go high. These bits can be polled to determine when the Reset operation is complete, as it will return to the default value (0) after the reset operation is finished. Issuing the RESET command (FFh) has no effect on the Block Protection and Configuration registers.

The Block Protection and Configuration registers will return to their default state after a power cycle, and can also be changed using the Set Feature command. Issuing the Get Feature command to read the selected register value will not affect register content.

Table 2-1. Configuration Registers

ADD	Register		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
10h	Configuration	bit name						RANDOPT	RANDEN	ENPGM	00h
		Type						V2	V2	V	
60h	Configuration	bit name							SPI_NOR_EN[3]	OTPRWSP[3]	00h
		Type							OTP	OTP	
70h	Special Read for Data Recovery	bit name						SPEC_RD2	SPEC_RD1	SPEC_RD0	00h
		Type						V	V	V	
A0h	Block Protection	bit name	BPRWD[1]		BP2	BP1	BP0	Invert	Comp.	SP[2]	38h
		Type	V		V	V	V	V	V	V	
B0h	Configuration	bit name	OTP_PROT	OTPEN						QE	00h
		Type	V	V						V	
C0h	Status	bit name	CRBSY				PGM-FAIL	ERS_FAIL	WEL	OIP	00h
		Type	V				V	V	V	V	
E0h	Configuration	bit name	DS_IO[1]	DS_IO[0]							00h
		Type	V2	V2							

V: Volatile

V2: Volatile, the default value of these volatile feature bits can be changed once by special OTP feature bits program operation

OTP: One time setting

Note 1: *If BPRWD is enabled and WP# is LOW, then the block protection register cannot be changed.*

Note 2: *SP bit is for Solid-protection. Once the SP bit sets as 1, the rest of the protection bits (BPx bits, Invert bits, complementary bits) cannot be changed during the current power cycle.*

Note 3: *SPI_NOR_EN bit and OTPRWSP bit are only for 1Gb/2Gb.*

Table 2-2. I/O Strength Feature Table

DS_IO[1]	DS_IO[0]	Drive Strength
0	0	normal (defaul, 25 ohm typical)
0	1	underdrive 1 (35 ohm typical)
1	X	underdrive 2 (85 ohm typical)

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Figure 6. GET FEATURE (0Fh) Timing

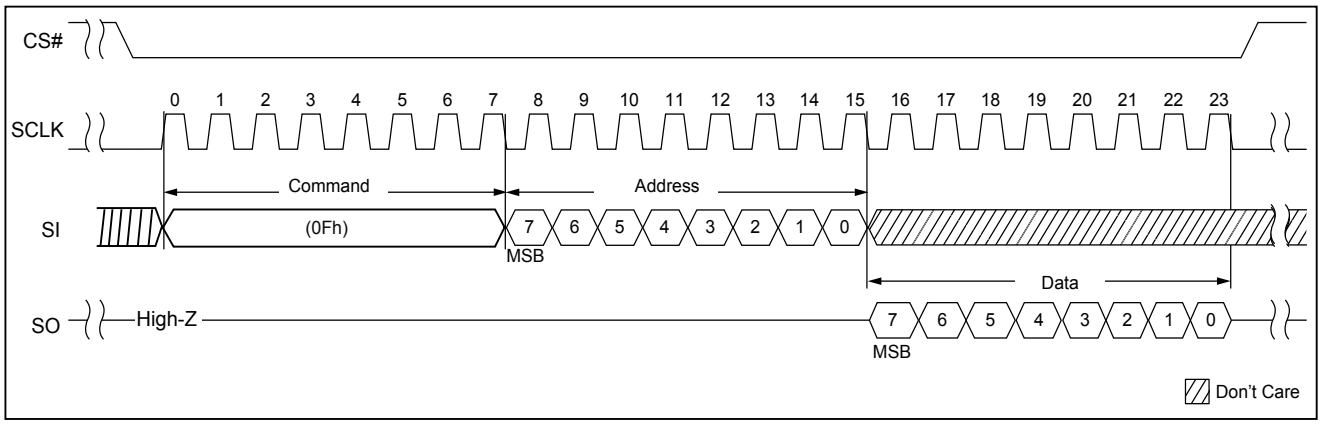
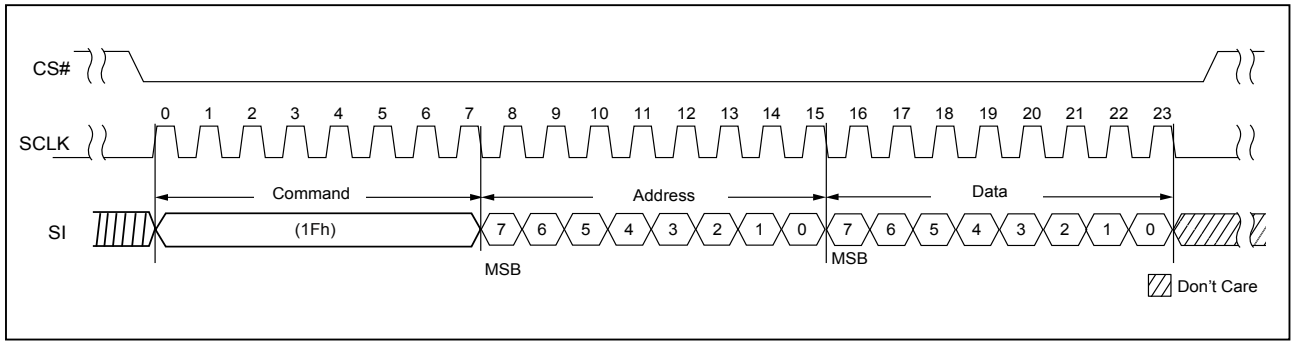


Figure 7. SET FEATURE (1Fh) Timing



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8-3. READ Operations

The device supports "Power-on Read" function, after power up, host may issue the Read From Cache command, and the device will automatically load the data of the 1st page of 1st block from array to cache. The host micro-controller may directly read the 1st page of 1st block data from the cache buffer.

The device supports the page read operation and page read cache Random/sequential operation.

8-3-1. PAGE READ (13h)

The page read operation transfers data from array to cache by issuing the page read (13h)command followed by the 24-bit address (including the dummy/block/page address).

The device will have a period of time (tRD) being busy after the CS# goes high. The 0Fh (GET FEATURE) may be used to poll the operation status.

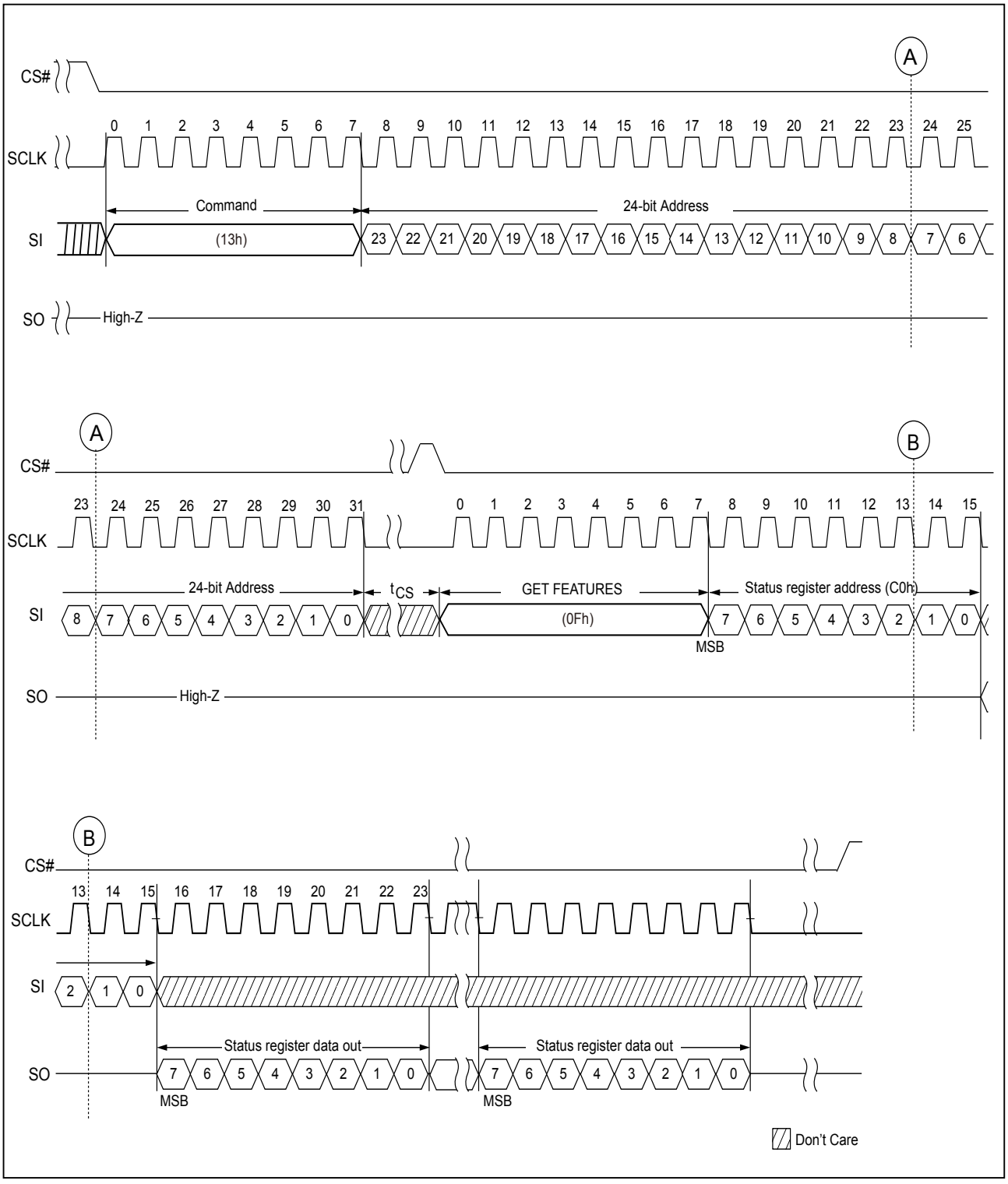
After read operation is completed, the Read from cache (03H or 0Bh), Read from cache (x2) (3Bh), Read from cache (x4) (6Bh), read from cache dual IO (1-2-2) (BBh) and Read from cache Qual IO (1-4-4) (EBh) may be issued to fetch the data.

8-3-2. QE Bit

The Quad Enable (QE) bit, volatile bit, while it is "0" (factory default), it performs non-Quad and WP#, HOLD# are enabled. While QE is "1", it performs Quad I/O mode and WP#, HOLD# are disabled. In another word, if the system goes into four I/O mode (QE=1), the feature of Hardware Protection Mode(HPM) and HOLD will be disabled. Upon power cycle, the QE bit will go into the factory default setting "0".

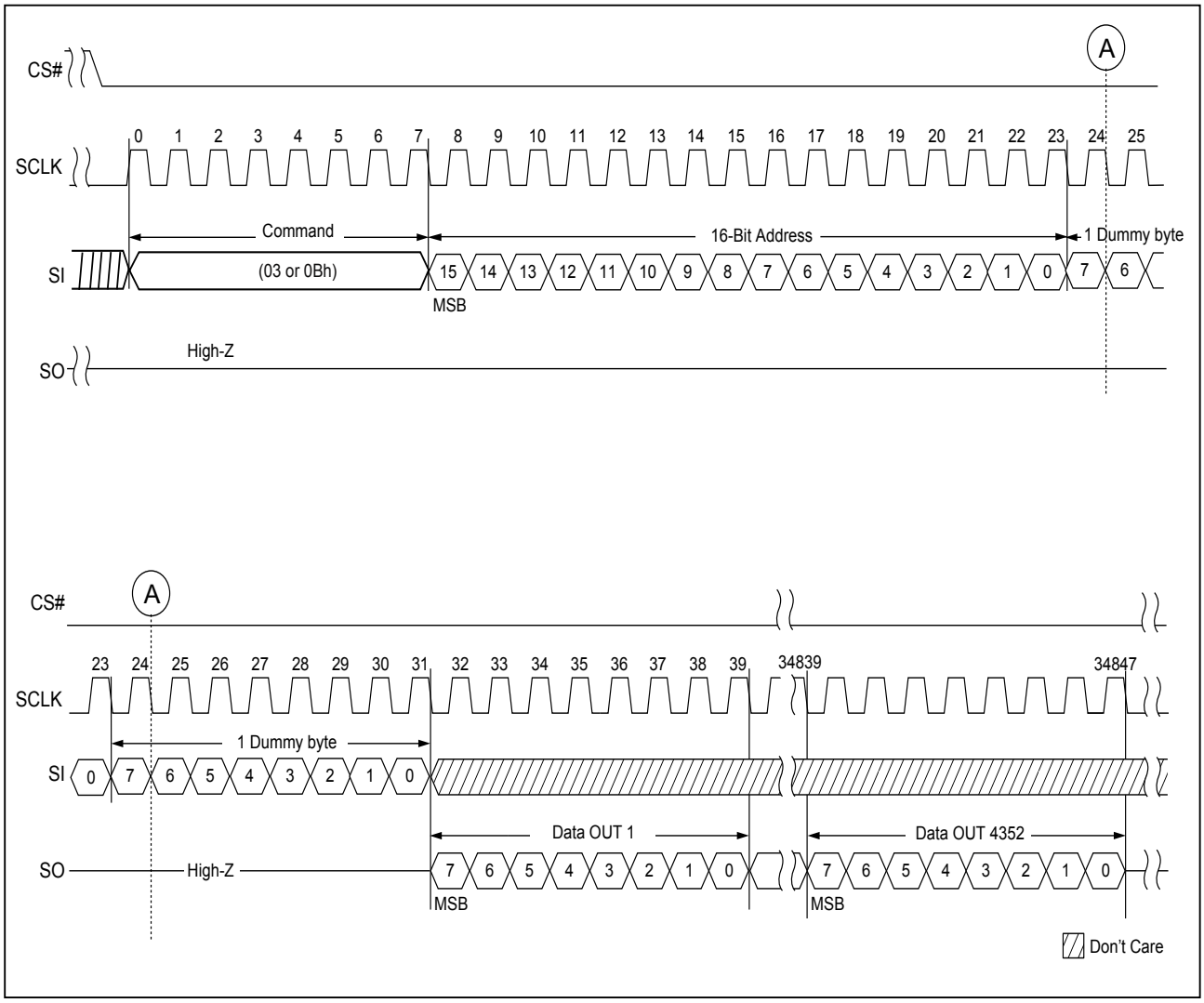
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Figure 8. PAGE READ (13h) Timing x1



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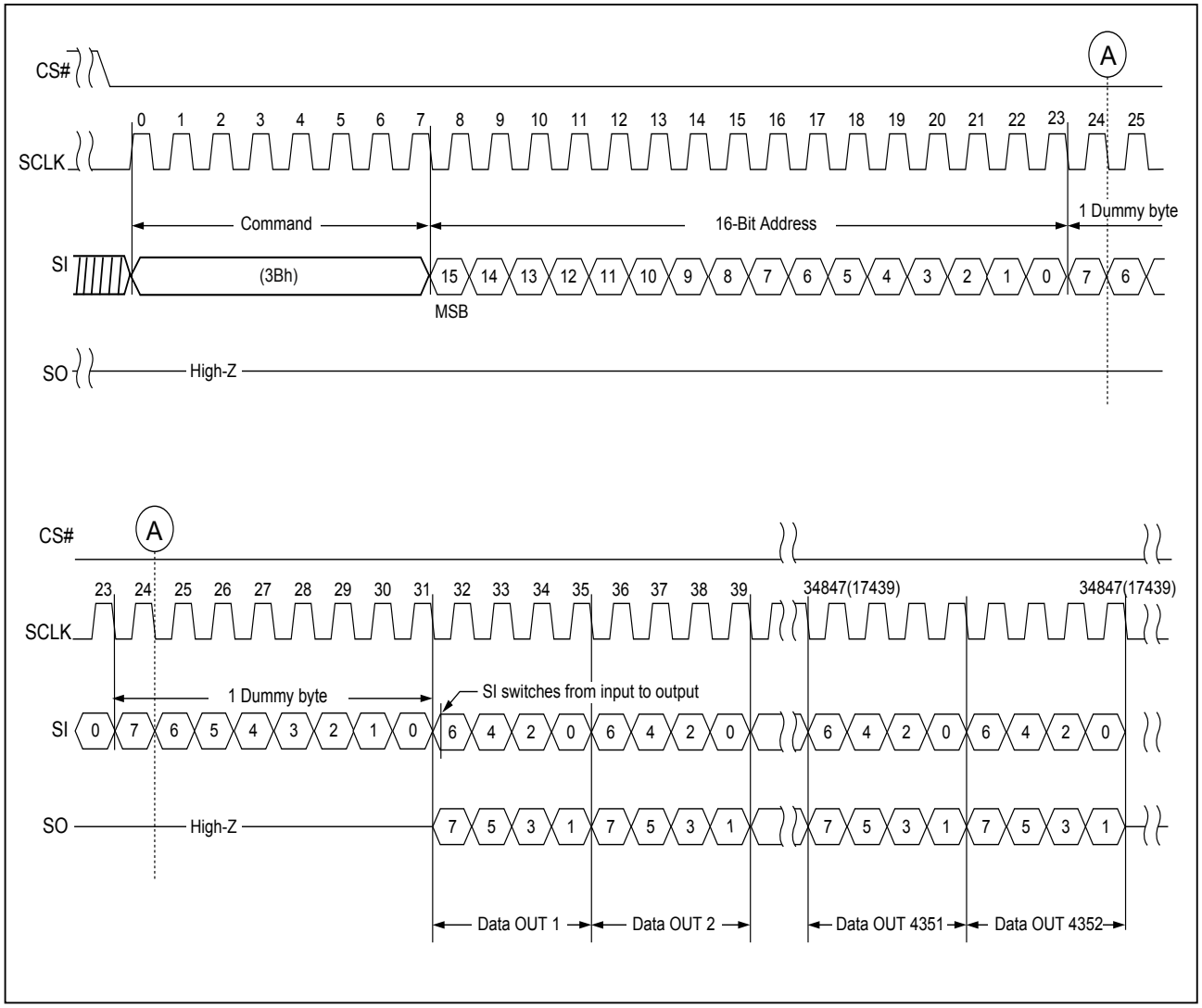
Figure 9. READ FROM CACHE (03h or 0Bh) Timing



***Note**: Data byte is 2176 for 1Gb/2Gb*

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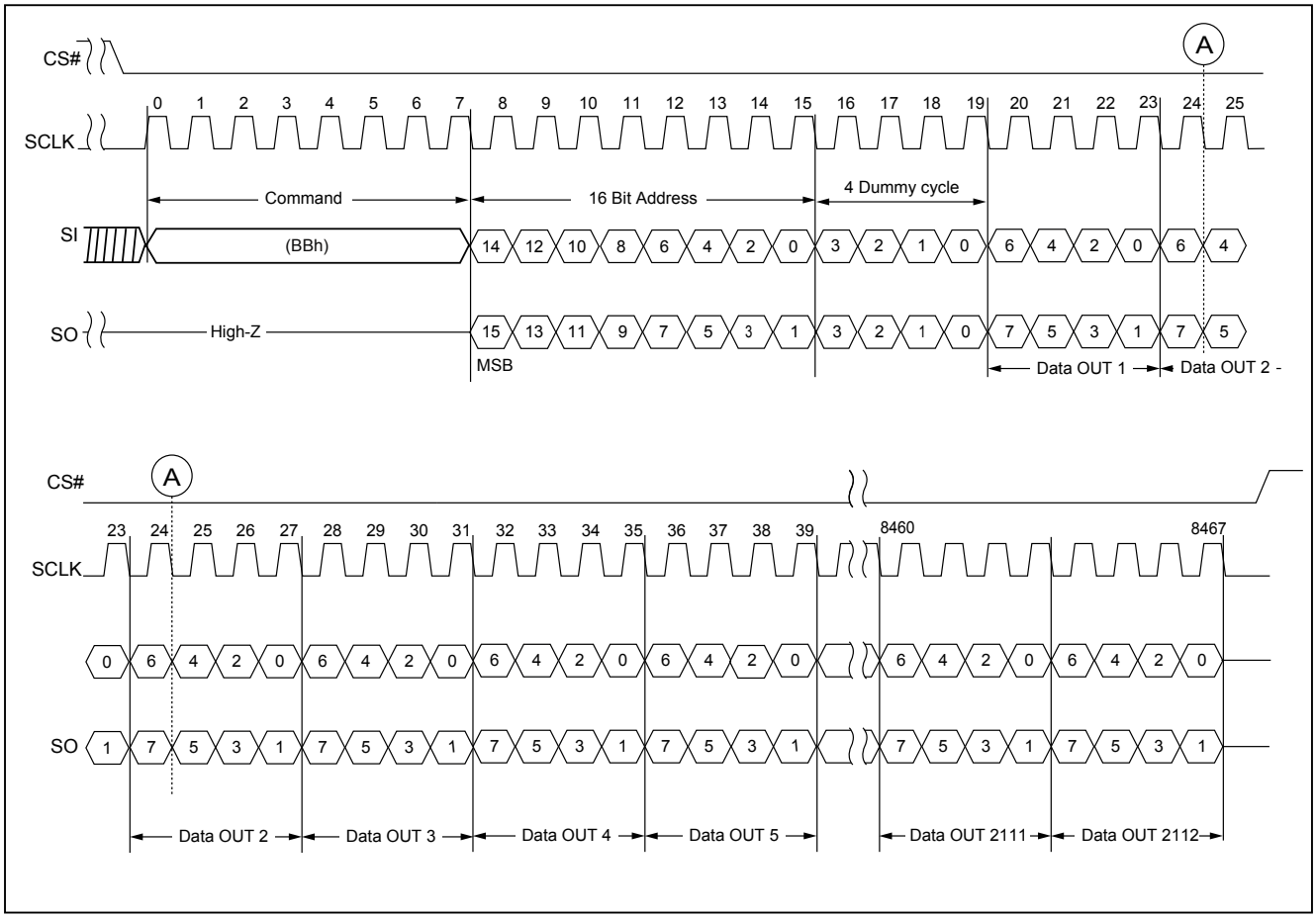
Figure 10. READ FROM CACHE x 2



***Note**: Data byte is 2176 for 1Gb/2Gb*

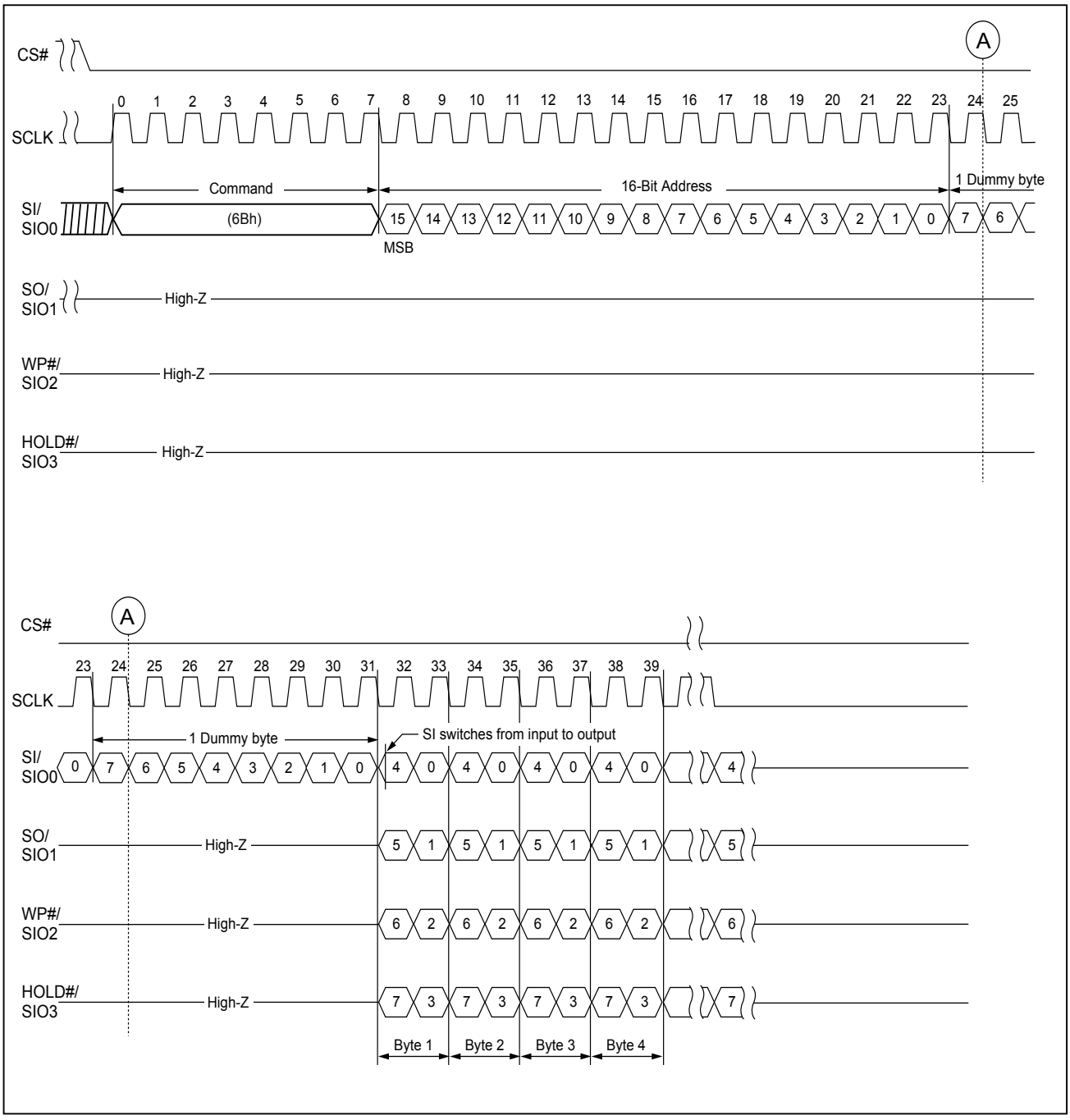
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Figure 11. Read From Cache Dual IO 1-2-2



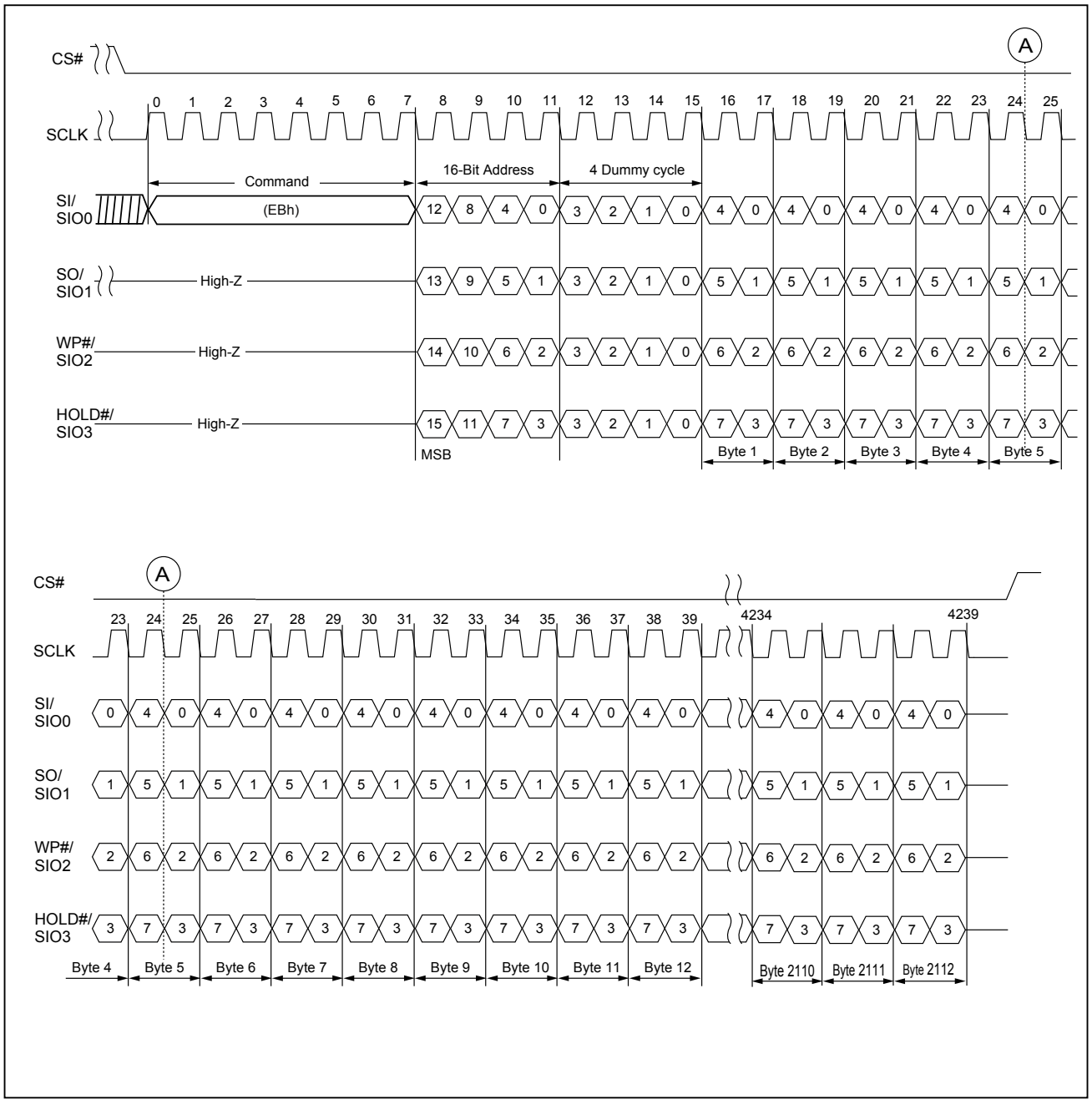
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Figure 12. READ FROM CACHE x 4



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Figure 13. Read From Cache Quad IO 1-4-4



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8-3-3. Page Read Cache Random (30h)/Page Read Cache Sequential (31h)/Page Read Cache End (3Fh)

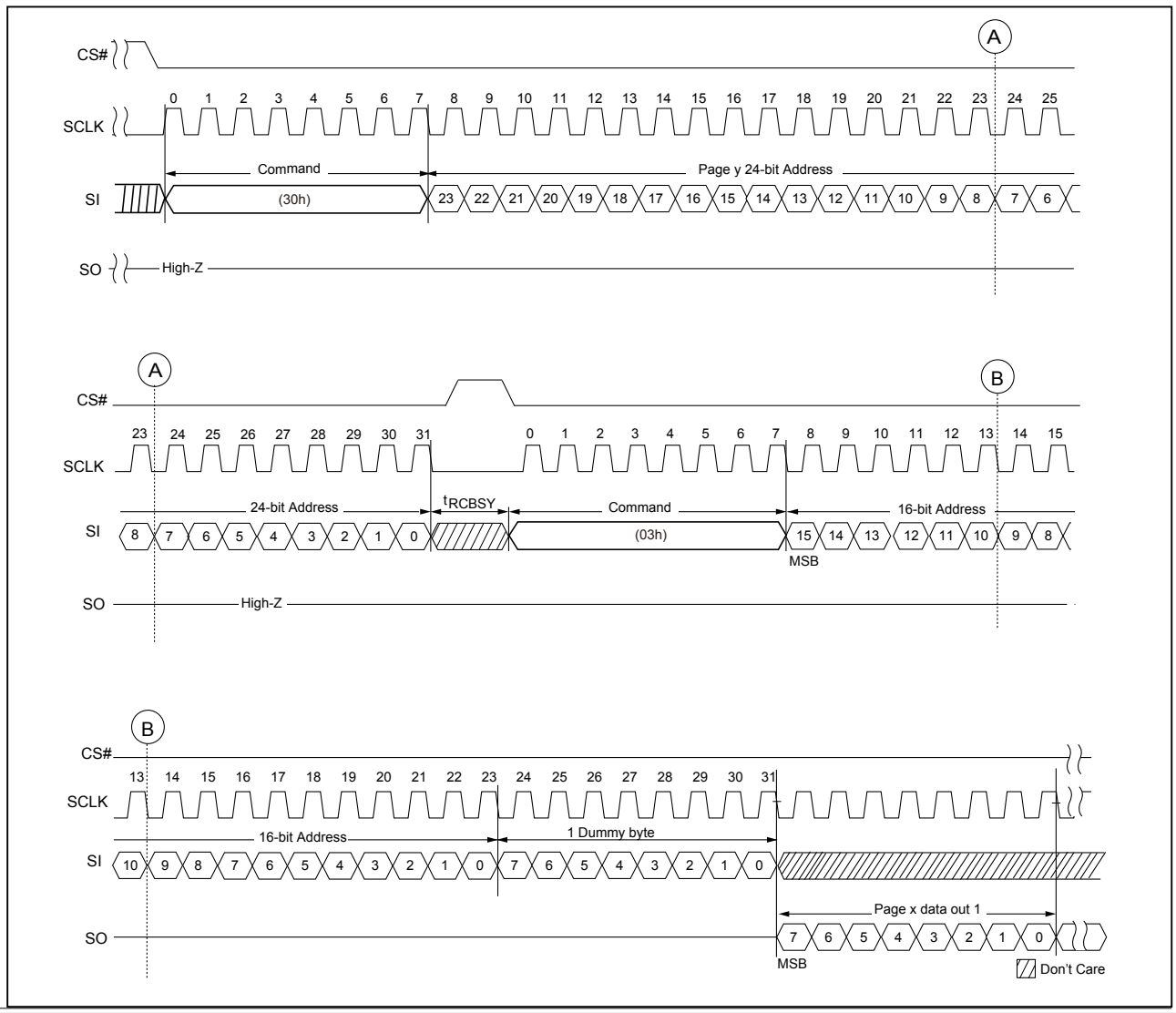
The page read cache sequential operation is for throughput enhancement by using the internal cache buffer. It allows the consecutive pages to be read-out without giving next page address, which reduces the latency time from tRD to tRCBSY between pages or blocks. While the data is read out on one page, the data of next page can be read into the cache buffer.

After writing the 13h command and giving the 24-bit address, the device will have a period of time (tRD) being busy after the CS# goes high. The 0Fh (GET FEATURE) may be used to poll the operation status. After the status of successfully completed, following the page read cache sequential (31h) or the page read cache random (30h) command being sent to NAND device; the NAND device will be at a busy time of tRCBSY for the next page data transferring to cache. And then following the cache read command (03h/0Bh/3Bh/6Bh/BBh/EBh) may get the prior page data output from cache at the same time.

To confirm the last page to be read-out during the cache read sequential operation, a 3Fh command is needed to replace the 31h or 30h command prior to the last data-out.

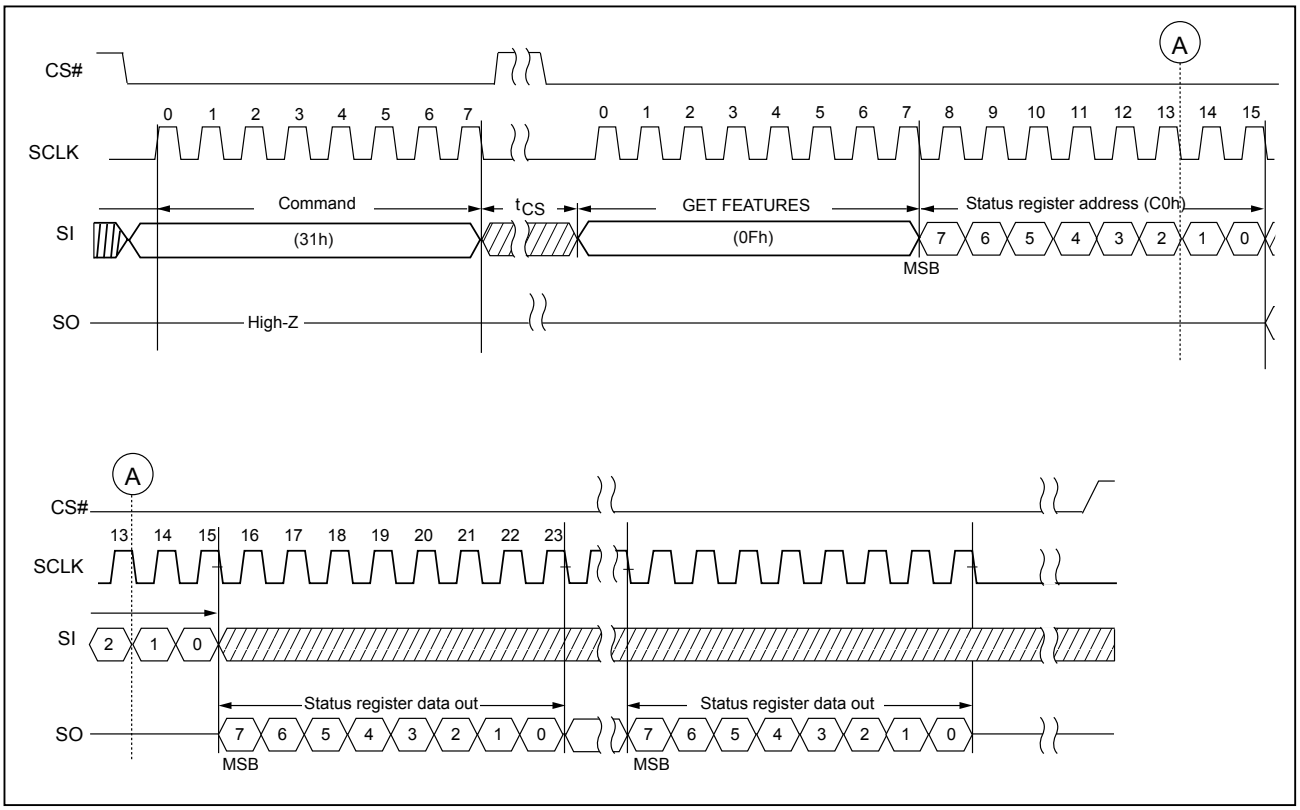
The PAGE READ CACHE SEQUENTIAL command is also valid for the consecutive page cross block.

Figure 14. Page Read Cache Random (30h)



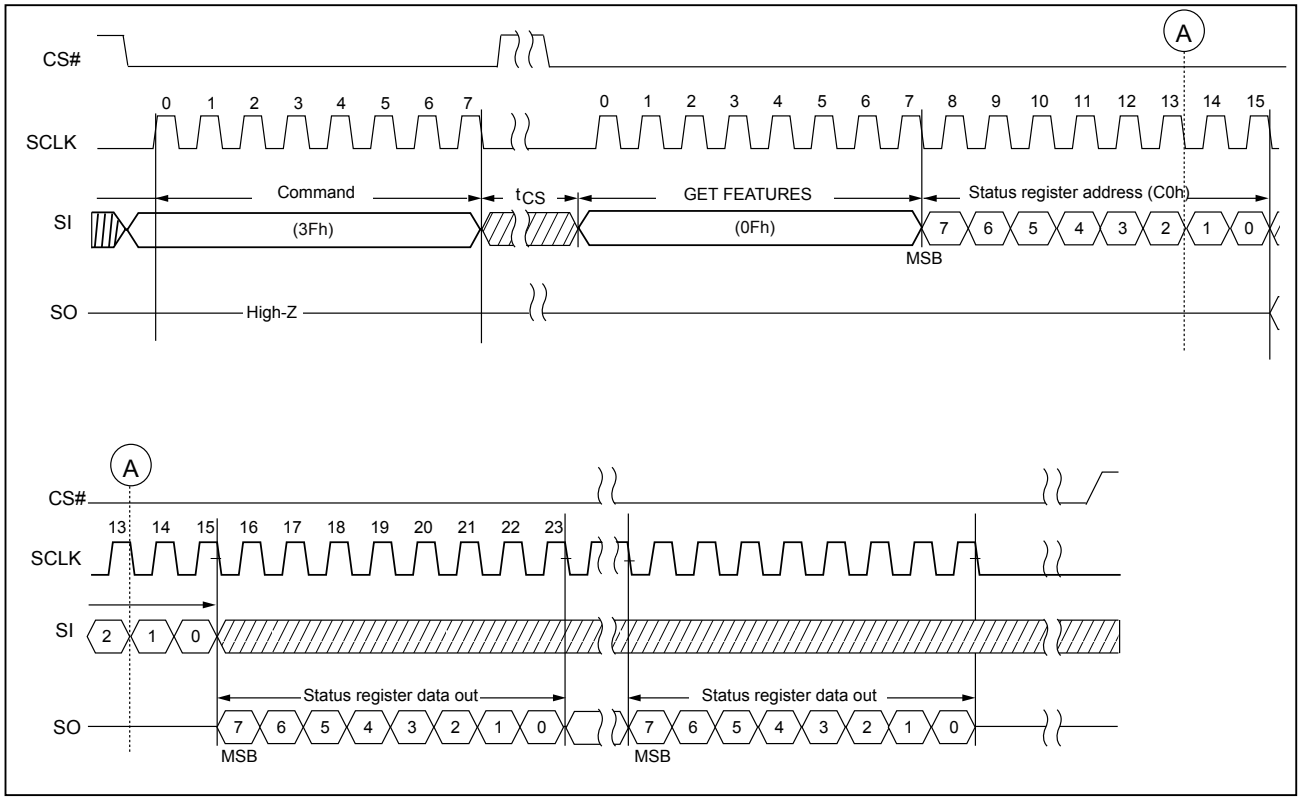
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Figure 15. Page Read Cache Sequential (31h)



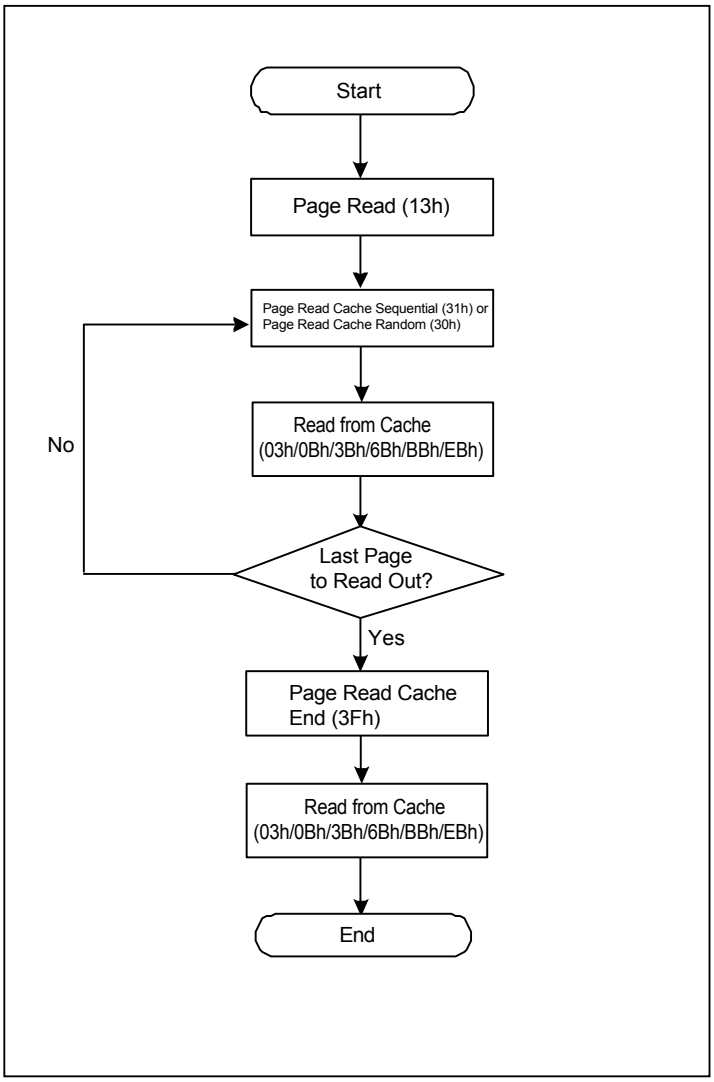
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Figure 16. Page Read Cache End (3Fh)



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Figure 17. Page Read Cache Flow



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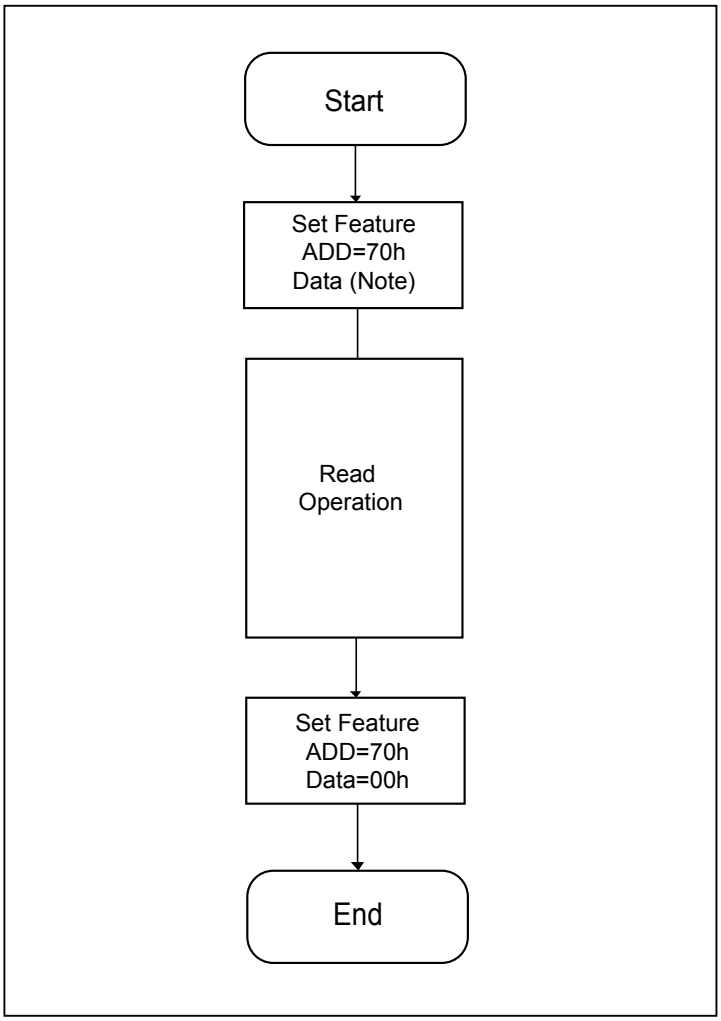
8-3-4. Special Read for Data Recovery

When the host ECC fails to correct the data error of NAND device, there's a special read for data recovery method which host executes the Special Read for Data Recovery operation and may recover the lost data by host ECC again. After that, it is needed to move the data to another good block.

The Special Read for Data Recovery operation is enabled by Set Feature function (**"Table 3. Feature Settings"**).

There are 5 modes for the user to recover the lost data. The procedure of entering and exiting the operation is shown as Figure below.

Figure 18. Procedure of Entering/Exiting the Special Read for Data Recovery operation



Note: Please refer to **"Table 3. Feature Settings"**

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Table 3. Feature Settings

Definition		SPEC_RD2	SPEC_RD1	SPEC_RD0	Value
Special Read for Data Recovey	Disable (Default)	0	0	0	00h
	Mode 1	0	0	1	01h
	Mode 2	0	1	0	02h
	Mode 3	0	1	1	03h
	Mode 4	1	0	0	04h
	Mode 5	1	0	1	05h

8-3-5. Randomizer Operation

The randomizer function is enabled on the NAND device, the user data and OTP area are scrambled in random pattern before written to the NAND device. When attempting to use the randomizer function, it is necessary to enable the randomizer function prior to program data in main array and OTP area. The randomizer function is enabled through “set feature” operation (as **"Table 2-1. Configuration Registers"**). The following feature bits RANDEN and RANDOPT is related with randomizer function (as **"Table 2-1. Configuration Registers"**)

To enable the randomizer function, RANDEN bit must be set to “1”, RANDOPT can be set to “0” or “1” depending on the user choice (as **"Table 4. The definition of RANDOPT bit for the randomized area per page"** (as grey color).

Both RANDEN and RANDOPT feature bits are OTP bits and can be programmed once. After programming, the RANDEN and RANDOPT bits are fixed and can not be changed by set feature command or power cycle anymore. The RANDEN and RANDOPT bits program flowchart is shown on the **"Figure 19. Flowchart of RANDEN and RANDOPT Bits Program Operation"**.

To enable the program sequence, ENPGM feature bit must be set to “1”. After the program is finished, ENPGM feature bit must be set to “0” as shown in the flow.

After the RANDEN and RANDOPT feature bits are programmed, the user can issue get feature command to check the RANDEN and RANDOPT feature bits are programmed successfully or not.

Note: *Please do not program the configuration feature bits more than once.*

RANDOPT bit: considering the needs of different applications; there are two options of randomizer coverage providing (as **"Table 4. The definition of RANDOPT bit for the randomized area per page"** (as grey color" shown. The grey data area is covered by the randomizer function for each option; whereas the white area is not.

Note: *the NOP=1 for the randomizer covered data area.*

Table 4. The definition of RANDOPT bit for the randomized area per page

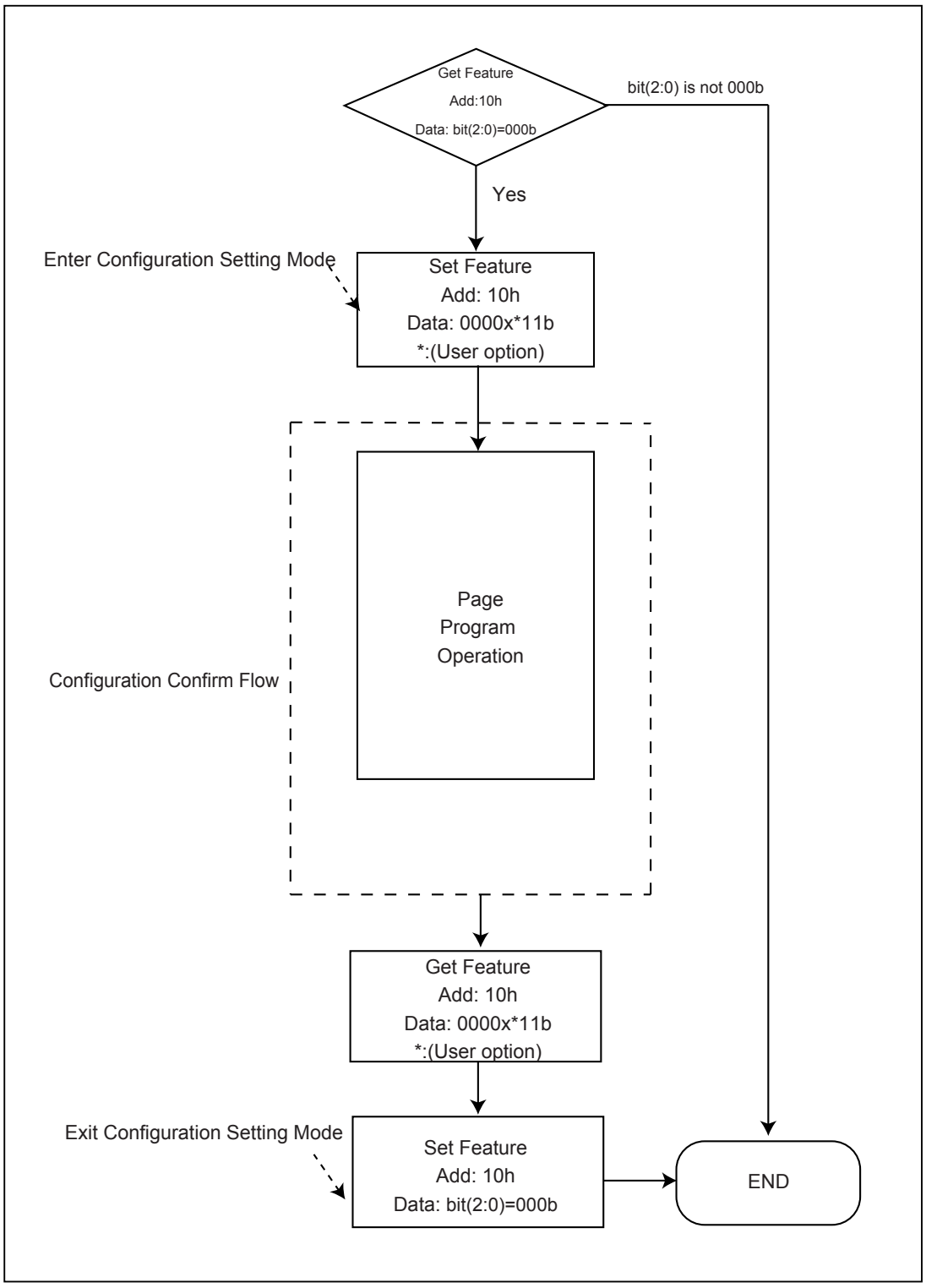
(As grey color)

Density	RANDOPT	Main	Spare 0	Spare 1	Remark
1G/2G	0	0000h~07FFh	0800h~081Fh	0820h~087Fh	NOP=1 for Main/Spare 0/Spare 1
	1	0000h~07FFh	0800h~081Fh	0820h~087Fh	NOP=1 for Main/Spare 1

Density	RANDOPT	Main	Spare 0	Spare 1	Remark
4G	0	0000h~0FFFh	1000h~101Fh	1020h~10FFh	NOP=1 for Main/Spare 0/Spare 1
	1	0000h~0FFFh	1000h~101Fh	1020h~10FFh	NOP=1 for Main/Spare 1

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Figure 19. Flowchart of RANDEN and RANDOPT Bits Program Operation



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9. SPI NOR Compatible Command (Only for 1Gb/2Gb)

Considering some SoC(or MCU) of host system must adopt the read protocol of SPI NOR like, this device provide the SPI_NOR_EN of configuration register bit to enable the read protocol of SPI NOR like for Read From Cache commands. The SPI_NOR_EN bit is OTP type once it is enable and cannot disable.

It is recommended to set the SPI_NOR_EN bit by programmer machine in advance before power on while attempts to adopt the read protocol of SPI NOR like.

Please refer to the **"Figure 46-3. Special OTP Configuration Register Program Operation (for V2/OTP Type of Configuration Register Bits)"**.

Table 5. Command Set - SPI NOR Like Protocol Enabled

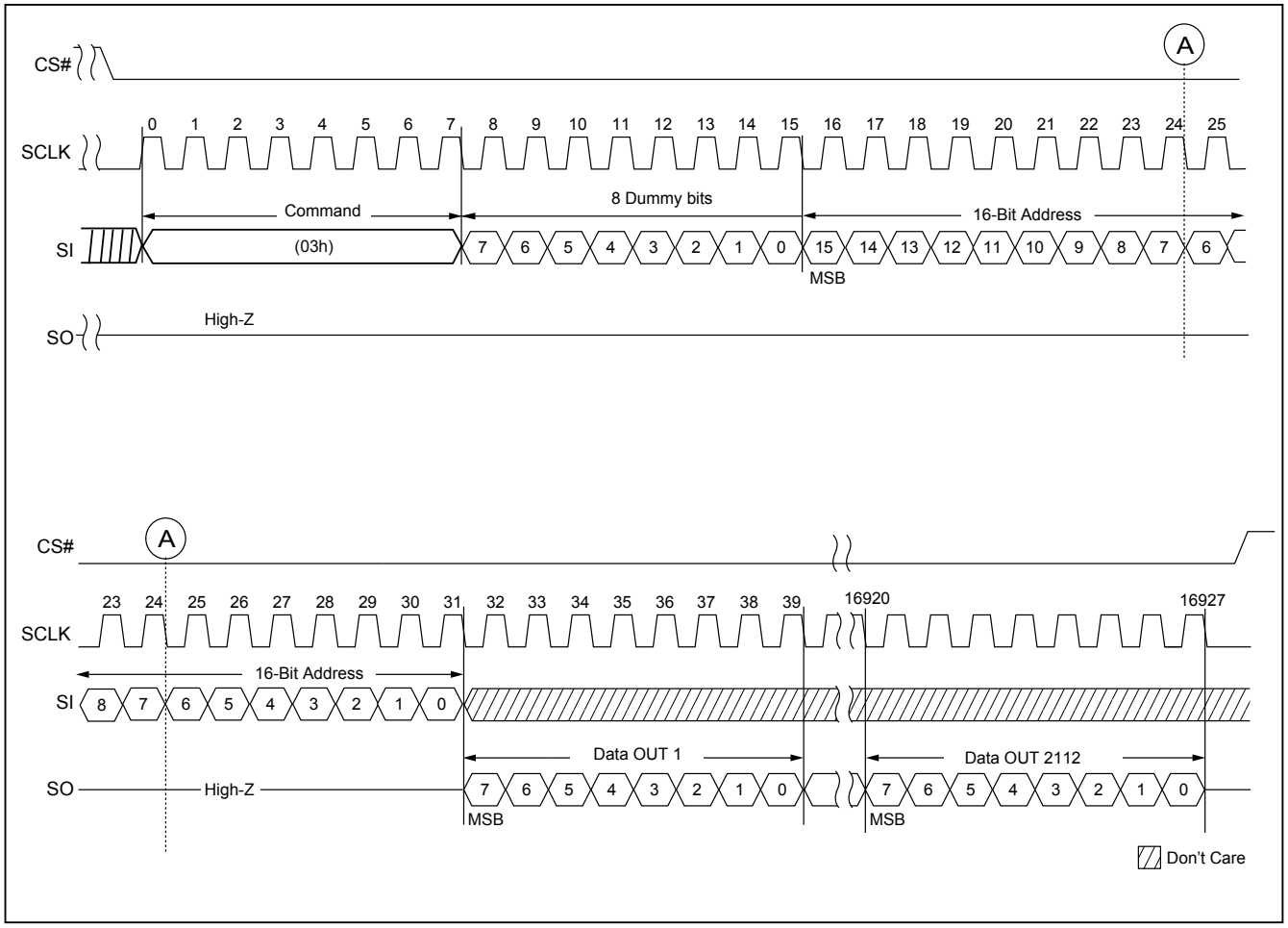
(**SPI_NOR_EN = 1**)

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	7th Byte	8th Byte
Get Feature	0Fh	ADD	**Data**					
Set Feature	1Fh	ADD	Data					
Page Read	13h	RADD2	RADD1	RADD0				
Page Read Cache Random	30h	RADD2	RADD1	RADD0				
Page Read Cache Sequential	31h							
Page Read Cache Last	3Fh							
Read From Cache x1	03h	DUMMY	CADD1	CADD0	DATA~			
Read From Cache x1 (Alternative)	0Bh	DUMMY	CADD1	CADD0	DUMMY	DATA~		
Read From Cache x2 Note	3Bh	CADD1	CADD0	DUMMY	DATA~*2			
Read From Cache x4 Note	6Bh	CADD1	CADD0	DUMMY	DATA~*4			
Read From Cache Dual IO 1-2-2 Note	BBh	CADD1*2	CADD0*2	DUMMY*2	DATA~*2			
Read From Cache Quad IO 1-4-4 Note	EBh	CADD1*4	CADD0*4	DUMMY*4	DUMMY*4	DATA~*4		
Read ID	9Fh	DUMMY	MID	DID1	DID2			
Block Erase	D8h	RADD2	RADD1	RADD0				
Program Execute	10h	RADD2	RADD1	RADD0				
Program Load x1	02h	CADD1	CADD0	DATA~				
Program Load Random Data x1	84h	CADD1	CADD0	DATA~				
Program Load x4 Note	32h	CADD1	CADD0	DATA~*4				
Program Load Random Data x4 Note	34h	CADD1	CADD0	DATA~*4				
Write Enable	06h							
Write Disable	04h							
Reset	FFh							

Note: **2 stands for the dual I/O phase and *4 for quad I/O mode*

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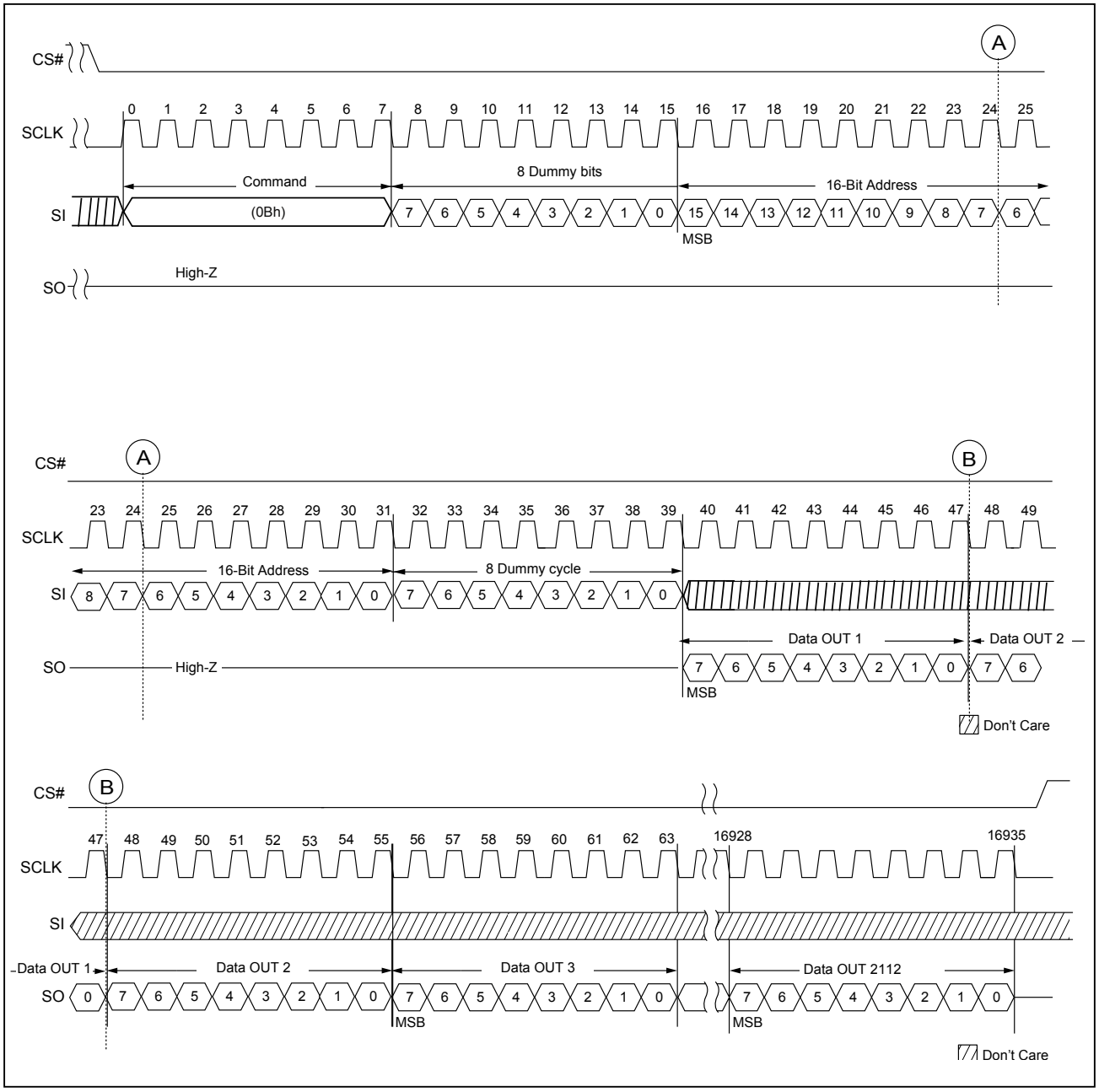
Figure 20. Read From Cache x1 (NOR like)



***Note 1**: For SPI NOR Like Protocol command, the Read From Cache command (03h) can run up to 20MHz only.*

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Figure 21. Read From Cache x1 (Alternative, NOR like)



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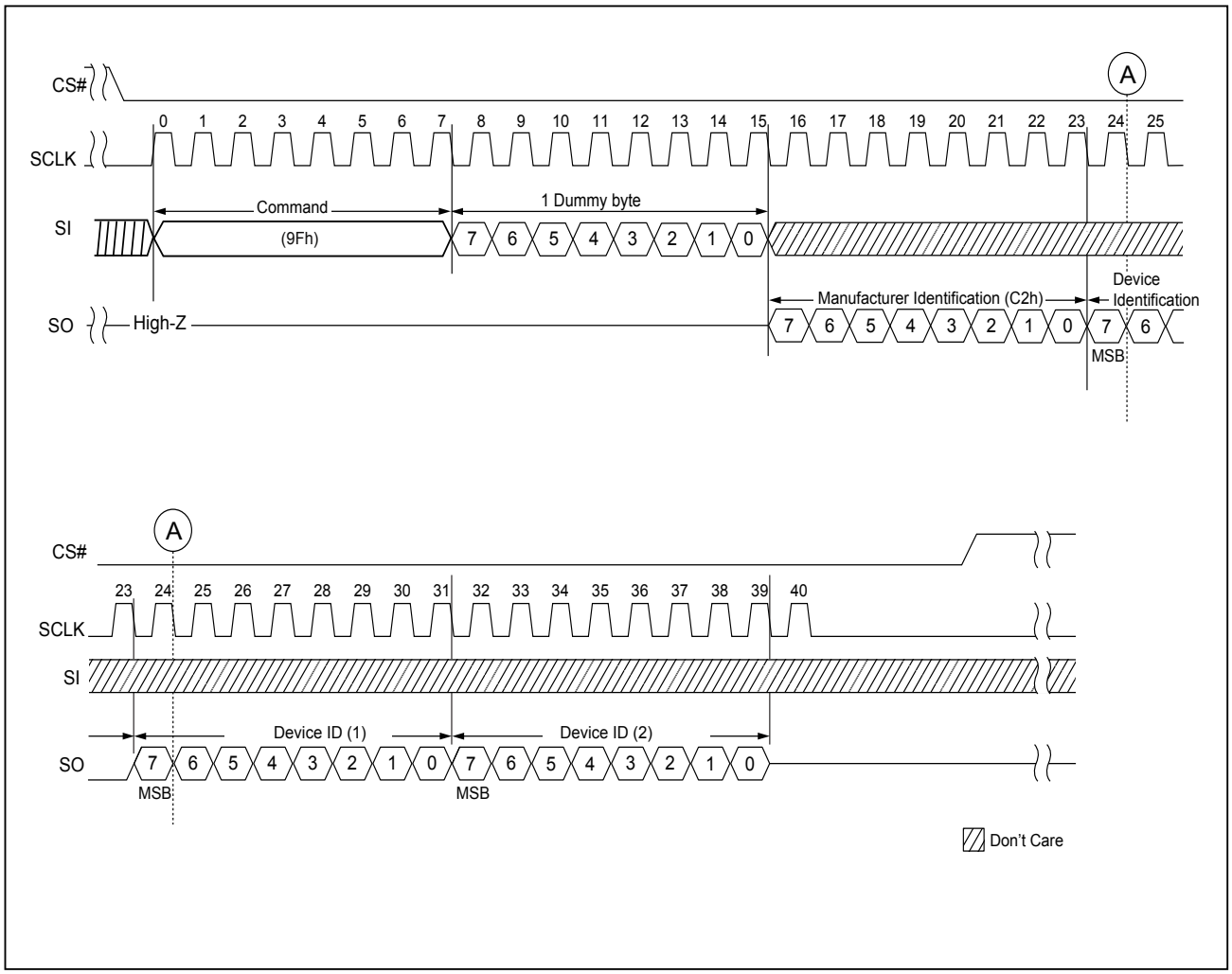
9-3-1. READ ID (9Fh)

The READ ID command is shown as the table below.

Table 6. READ ID Table

Byte	Description		I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value
Byte 0	Manufacturer ID (Macronix)		1	1	0	0	0	0	1	0	C2h
Byte 1	Device ID 1	1Gb	0	0	0	1	0	1	0	0	14h
		2Gb	0	0	1	0	0	1	0	0	24h
		4Gb	0	0	1	1	0	1	0	1	35h
Byte 2	Device ID 2		0	0	0	0	0	0	1	1	03h

Figure 22. READ ID (9Fh) Timing



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9-1. Parameter Page

The parameter page is accessed by the following command flows:

Issue 1Fh (SET FEATURE) command with Secure OTP enable (B0h for address & 40h for data) → Issue 13h (PAGE READ) with 01h address, issue 0Fh (GET FEATURE) with C0h feature address to poll the status of read completion. → Issue 03h (READ FROM CACHE) with address A[11:0]=000h and read data → Issue 1Fh (SET FEATURE) with feature address B0h to disable Secure OTP feature (data byte = 00h) [exit parameter page read].

Table 7-1. Parameter Page Data Structure (MX35LF1G24AD)

	Revision Information and Features Block		
Byte#	**Description**		**Data**
0-3	Parameter Page Signature		4Fh, 4Eh, 46h, 49h
4-5	Revision Number		00h, 00h
6-7	Features Supported (N/A)		00h, 00h
8-9	Optional Commands Supported		06h, 00h
10-31	Reserved		00h
	Manufacturer Information Block		
Byte#	**Description**		**Data**
32-43	Device Manufacturer (12 ASCII characters)		4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	Device Model (20 ASCII Characters)	MX35LF1G24AD	4Dh, 58h, 33h, 35h, 4Ch, 46h, 31h, 47h, 32h, 34h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		C2h
65-66	Date Code		00h, 00h
67-79	Reserved		00h

Memory Organization Block			
Byte#	**Description**		**Data**
80-83	Number of Data Bytes per Page	2048-byte	00h, 08h, 00h, 00h
84-85	Number of Spare Bytes per Page	128-byte	80h, 00h
86-89	Number of Data Bytes per Partial Page	512-byte	00h, 02h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page	32-byte	20h, 00h
92-95	Number of Pages per Block		40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		00h, 04h, 00h, 00h
100	Number of Logical Units		01h
101	Number of Address Cycles (N/A)		00h
102	Number of Bits per Cell		01h
103-104	Bad Blocks Maximum per unit		14h, 00h
105-106	Block endurance		06h, 04h
107	Guarantee Valid Blocks at Beginning of Target		08h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of Programs per Page		04h
111	Partial Programming Attributes		00h
112	Number of ECC bits		08h
113	Number of Interleaved Address Bits		00h
114	Interleaved Operation Attributes (N/A)		00h
115-127	Reserved		00h

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Electrical Parameters Block			
Byte#	**Description**		**Data**
128	I/O Pin Capacitance		0Ah
129-130	Timing Mode Support (N/A)		00h, 00h
131-132	Program Cache Timing (N/A)		00h, 00h
133-134	tPROG Maximum Page Program Time (uS)	700us	BCh, 02h
135-136	BE Maximum Block Erase time (uS)	6000us	70h, 17h
137-138	tRD Maximum Page Read time (uS)	25us	19h, 00h
139-140	tCCS Minimum (N/A)	0ns	00h, 00h
141-163	Reserved		00h
Vendor Blocks			
Byte#	**Description**		**Data**
164-165	Vendor Specific Revision Number		00h, 00h
166	Reserved		00h
167	Reliability enhancement function 2-7 Reserved(0) 1 1= Randomizer support, 0= Not support 0 1= Special read for data recovery support, 0= Not support		03h
168	Reserved		00h
169	Number of special read for data recovery (N)		05h
170-253	Vendor Specific		00h
254-255	Integrity CRC		Set at Test ***(Note)***
Redundant Parameter Pages			
Byte#	**Description**		**Data**
256-2047	Value of Bytes 0-255, total 7 copies		Same as 0-255 Byte

Note:
The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.

The CRC shall be calculated using the following 16-bit generator polynomial:
$G(X) = X_{16} + X_{15} + X_2 + 1$

There are at least eight copies of 256-byte data and additional redundant parameter pages.

The host needs to find the parameter page of next copy if the CRC is not correct at current copy of parameter page. This procedure should be continue until the host get the correct CRC of the parameter page. The host may use bit-wise majority way to recover the content of parameter page from the copy of parameter page.

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Table 7-2. Parameter Page Data Structure (MX35LF2G24AD)

	Revision Information and Features Block		
Byte#	**Description**		**Data**
0-3	Parameter Page Signature		4Fh, 4Eh, 46h, 49h
4-5	Revision Number		00h, 00h
6-7	Features Supported (N/A)		00h, 00h
8-9	Optional Commands Supported		06h, 00h
10-31	Reserved		00h
	Manufacturer Information Block		
Byte#	**Description**		**Data**
32-43	Device Manufacturer (12 ASCII characters)		4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	Device Model (20 ASCII Characters)	MX35LF2G24AD	4Dh, 58h, 33h, 35h, 4Ch, 46h, 32h, 47h, 32h, 34h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		C2h
65-66	Date Code		00h, 00h
67-79	Reserved		00h

Memory Organization Block			
Byte#	**Description**		**Data**
80-83	Number of Data Bytes per Page	2048-byte	00h, 08h, 00h, 00h
84-85	Number of Spare Bytes per Page	128-byte	80h, 00h
86-89	Number of Data Bytes per Partial Page	512-byte	00h, 02h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page	32-byte	20h, 00h
92-95	Number of Pages per Block		40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		00h, 08h, 00h, 00h
100	Number of Logical Units		01h
101	Number of Address Cycles (N/A)		00h
102	Number of Bits per Cell		01h
103-104	Bad Blocks Maximum per unit		28h, 00h
105-106	Block endurance		06h, 04h
107	Guarantee Valid Blocks at Beginning of Target		08h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of Programs per Page		04h
111	Partial Programming Attributes		00h
112	Number of ECC bits		08h
113	Number of Interleaved Address Bits		01h
114	Interleaved Operation Attributes (N/A)		00h
115-127	Reserved		00h

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Electrical Parameters Block			
Byte#	**Description**		**Data**
128	I/O Pin Capacitance		0Ah
129-130	Timing Mode Support (N/A)		00h, 00h
131-132	Program Cache Timing (N/A)		00h, 00h
133-134	tPROG Maximum Page Program Time (uS)	700us	BCh, 02h
135-136	BE Maximum Block Erase time (uS)	6000us	70h, 17h
137-138	tRD Maximum Page Read time (uS)	25us	19h, 00h
139-140	tCCS Minimum (N/A)	0ns	00h, 00h
141-163	Reserved		00h
Vendor Blocks			
Byte#	**Description**		**Data**
164-165	Vendor Specific Revision Number		00h, 00h
166	Reserved		00h
167	Reliability enhancement function 2-7 Reserved(0) 1 1= Randomizer support, 0= Not support 0 1= Special read for data recovery support, 0= Not support		03h
168	Reserved		00h
169	Number of Special Read for Data Recovery (N)		05h
170-253	Vendor Specific		00h
254-255	Integrity CRC		Set at Test ***(Note)***
Redundant Parameter Pages			
Byte#	**Description**		**Data**
256-2047	Value of Bytes 0-255, total 7 copies		Same as 0-255 Byte
2048+	Additional Redundant Parameter Pages		

Note:
The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.

The CRC shall be calculated using the following 16-bit generator polynomial:
$G(X) = X_{16} + X_{15} + X_2 + 1$

There are at least eight copies of 256-byte data and additional redundant parameter pages.

The host needs to find the parameter page of next copy if the CRC is not correct at current copy of parameter page. This procedure should be continue until the host get the correct CRC of the parameter page. The host may use bit-wise majority way to recover the content of parameter page from the copy of parameter page.

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Table 7-3. Parameter Page Data Structure (MX35LF4G24AD)

	Revision Information and Features Block		
Byte#	**Description**		**Data**
0-3	Parameter Page Signature		4Fh, 4Eh, 46h, 49h
4-5	Revision Number		00h, 00h
6-7	Features Supported (N/A)		00h, 00h
8-9	Optional Commands Supported		06h, 00h
10-31	Reserved		00h
	Manufacturer Information Block		
Byte#	**Description**		**Data**
32-43	Device Manufacturer (12 ASCII characters)		4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	Device Model (20 ASCII Characters)	MX35LF4G24AD	4Dh, 58h, 33h, 35h, 4Ch, 46h, 34h, 47h, 32h, 34h, 41h, 44h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		C2h
65-66	Date Code		00h, 00h
67-79	Reserved		00h

Memory Organization Block			
Byte#	**Description**		**Data**
80-83	Number of Data Bytes per Page	4096-byte	00h, 10h, 00h, 00h
84-85	Number of Spare Bytes per Page	256-byte	00h, 01h
86-89	Number of Data Bytes per Partial Page	1024-byte	00h, 04h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page	64-byte	40h, 00h
92-95	Number of Pages per Block		40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		00h, 08h, 00h, 00h
100	Number of Logical Units		01h
101	Number of Address Cycles (N/A)		00h
102	Number of Bits per Cell		01h
103-104	Bad Blocks Maximum per unit		28h, 00h
105-106	Block endurance		06h, 04h
107	Guarantee Valid Blocks at Beginning of Target		08h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of Programs per Page		04h
111	Partial Programming Attributes		00h
112	Number of ECC bits		08h
113	Number of Interleaved Address Bits		01h
114	Interleaved Operation Attributes (N/A)		00h
115-127	Reserved		00h

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Electrical Parameters Block			
Byte#	**Description**		**Data**
128	I/O Pin Capacitance		0Ah
129-130	Timing Mode Support (N/A)		00h, 00h
131-132	Program Cache Timing (N/A)		00h, 00h
133-134	tPROG Maximum Page Program Time (uS)	700us	BCh, 02h
135-136	BE Maximum Block Erase time (uS)	6000us	70h, 17h
137-138	tRD Maximum Page Read time (uS)	25us	19h, 00h
139-140	tCCS Minimum (N/A)	0ns	00h, 00h
141-163	Reserved		00h
Vendor Blocks			
Byte#	**Description**		**Data**
164-165	Vendor Specific Revision Number		00h, 00h
166	Reserved		00h
167	Reliability enhancement function 2-7 Reserved(0) 1 1= Randomizer support, 0= Not support 0 1= Special read for data recovery support, 0= Not support		03h
168	Reserved		00h
169	Number of Special Read for Data Recovery (N)		05h
170-253	Vendor Specific		00h
254-255	Integrity CRC		Set at Test ***(Note)***
Redundant Parameter Pages			
Byte#	**Description**		**Data**
256-2047	Value of Bytes 0-255, total 7 copies		Same as 0-255 Byte
2048+	Additional Redundant Parameter Pages		

Note:
The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host.

The CRC shall be calculated using the following 16-bit generator polynomial:
$G(X) = X_{16} + X_{15} + X_2 + 1$

There are at least eight copies of 256-byte data and additional redundant parameter pages.

The host needs to find the parameter page of next copy if the CRC is not correct at current copy of parameter page. This procedure should be continue until the host get the correct CRC of the parameter page. The host may use bit-wise majority way to recover the content of parameter page from the copy of parameter page.

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9-2. UniqueID Page with PUF Type Code Structure

The UniqueID page is accessed by the following command flows:

Issue 1Fh (SET FEATURE) command with Secure OTP enable (B0h for address & 40h for data) → Issue 13h (PAGE READ) with 00h address, issue 0Fh (GET FEATURE) with C0h feature address to poll the status of read completion → Issue 03h (READ FROM CACHE) with address A[11:0]=000h and read data → Issue 1Fh (SET FEATURE) with feature address B0h to disable Secure OTP function (data byte = 00h) [exit unique ID read].

The MX30LF4G24AD unique ID adopts Macronix PUF-like code structure, which is truly random and the numbers of "0" bit almost equal to numbers of "1" bit. The unique ID is 32-byte and with 16 copies for back-up purpose. The host need to XOR the 1st 16-byte unique data and the 2nd 16-byte complement data to get the result, if the result is FFh, the unique ID data is correct; otherwise, host need to repeat the XOR with the next copy of Unique ID data.

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9-3. Program Operations

9-3-1. PAGE PROGRAM

With following operation sequences, the PAGE PROGRAM operation programs the page from byte 1 to byte 2176(for 1Gb/2Gb) or 4352(for 4Gb).

WRITE ENABLE (06h) → PROGRAM LOAD (02h) → PROGRAM LOAD RANDOM DATA (84h) if needed → PROGRAM EXECUTE (10h) → GET FEATUR from command to read status (0Fh).

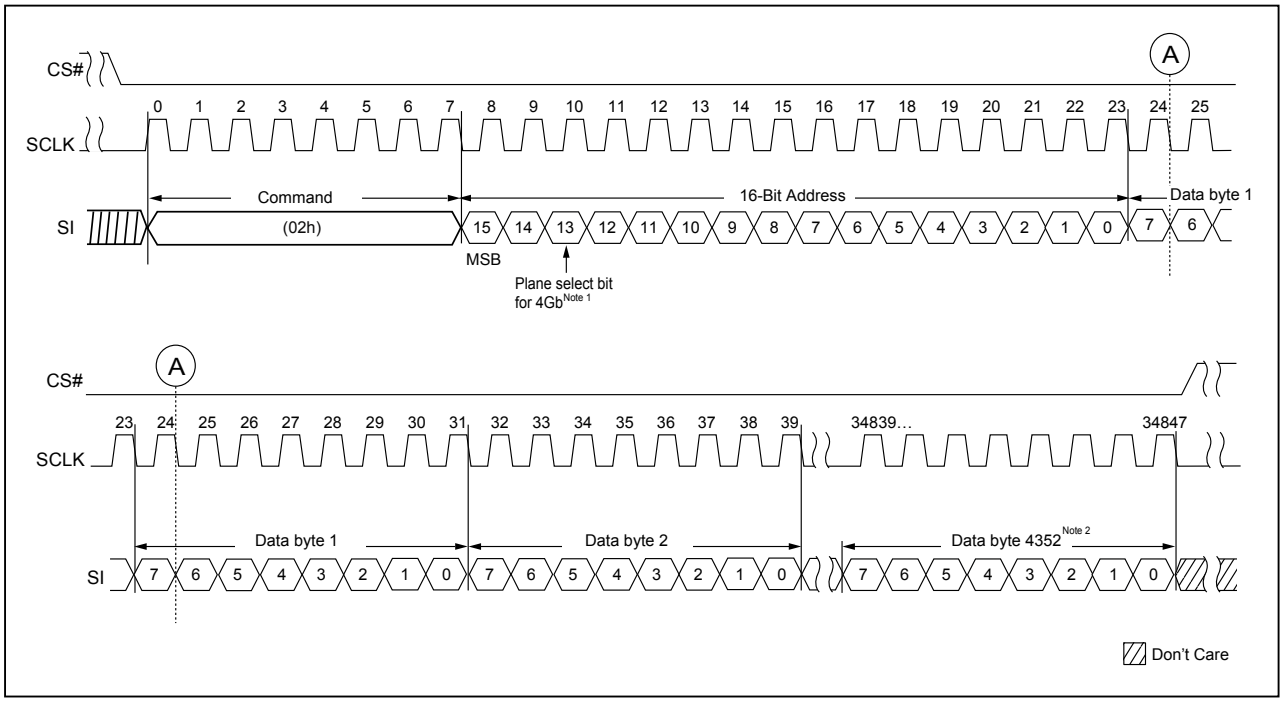
WEL bit is set with the WRITE ENABLE (06h) issued. The program operation will be ignored if 06h command not issued. In a single page, four partial page programs are allowed. Exceeded bytes (Page address is larger than 2176 (for 1G/2G) or 4352 (for 4G) for "PROGRAM LOAD" or "PROGRAM LOAD RANDOM DATA", the exceeding bytes will be ignored. When CS goes high, the "PROGRAM LOAD" or "PROGRAM LOAD RANDOM DATA" operation" terminates. Please note the figure below for PROGRAM LOAD.

After PROGRAM LOAD is done, the programming of data should be as following steps: issue 10h (PROGRAM EXECUTE) with 1byte command code, 24 bits address → code programming to memory and busy for tPROG → Program complete.

During programming, status to be polled by the status register.

Operation shows in the Figure below.

Figure 23. PROGRAM LOAD (02h) Timing

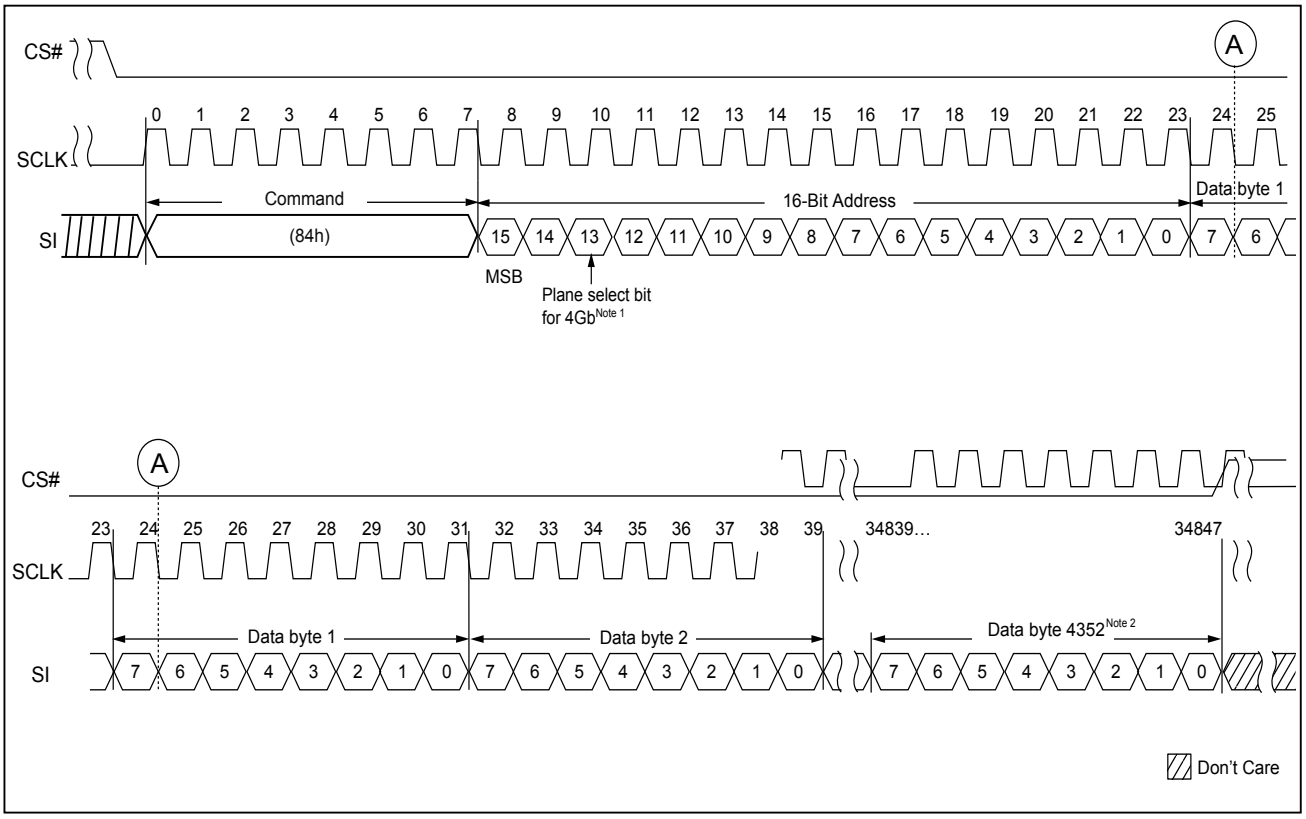


***Note** 1. Bit12 is plane select bit for 2Gb*

***Note** 2. Data byte is 2176 for 1Gb/2Gb*

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Figure 24. PROGRAM LOAD RANDOM DATA (84h) Timing



***Note** 1. Bit12 is plane select bit for 2Gb*

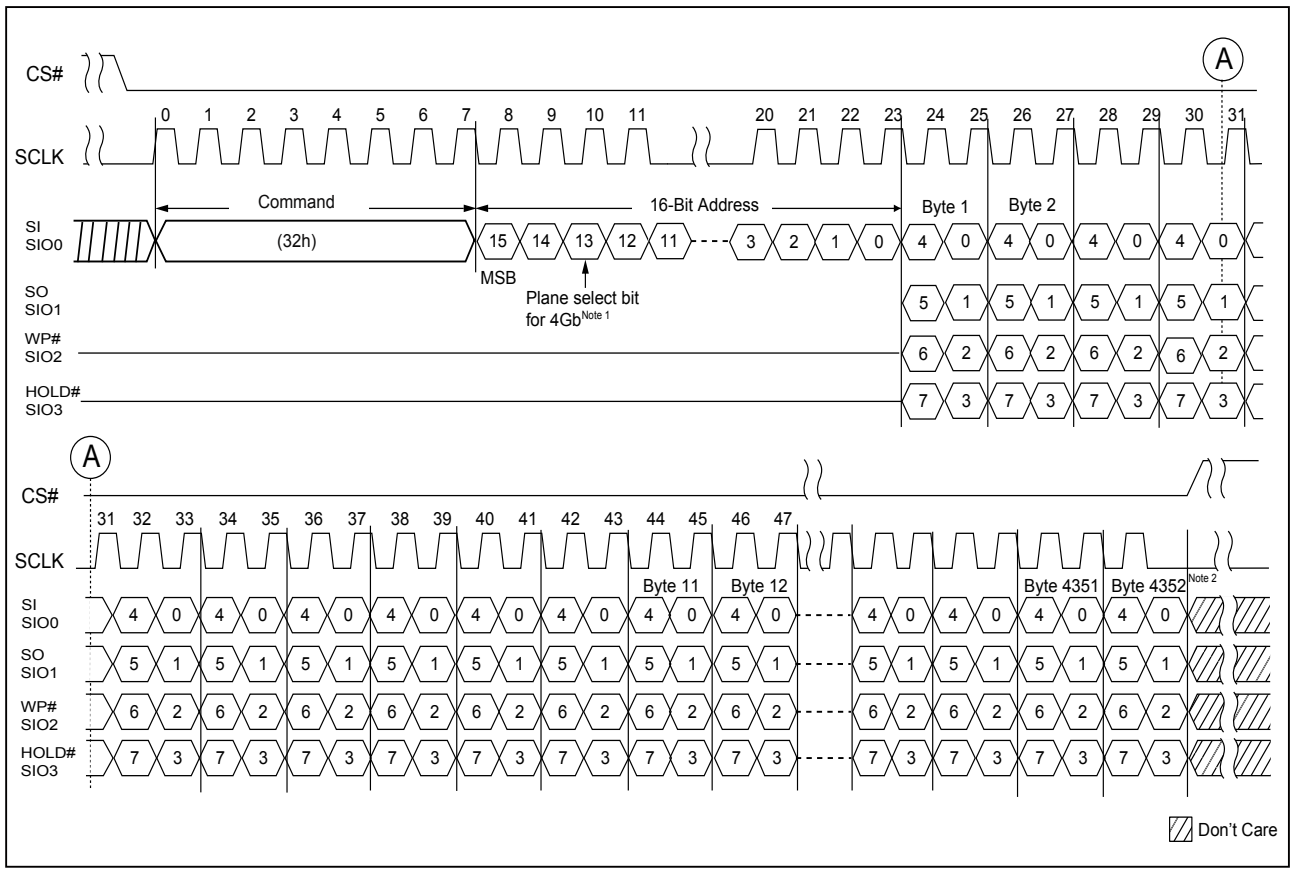
***Note** 2. Data byte is 2176 for 1Gb/2Gb*

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9-3-2. QUAD IO PAGE PROGRAM

QUAD IO PAGE PROGRAM conducts the 2Kbyte program with 4 I/O mode. The steps are: WRITE ENABLE (06h) → PROGRAM LOAD X4 (32h) → PROGRAM LOAD RANDOM DATA (34h) if needed → PROGRAM EXECUTE (10h) → Poll status by issuing GET FEATURE (0Fh).

Figure 25. PROGRAM LOAD X4 (32h) Timing

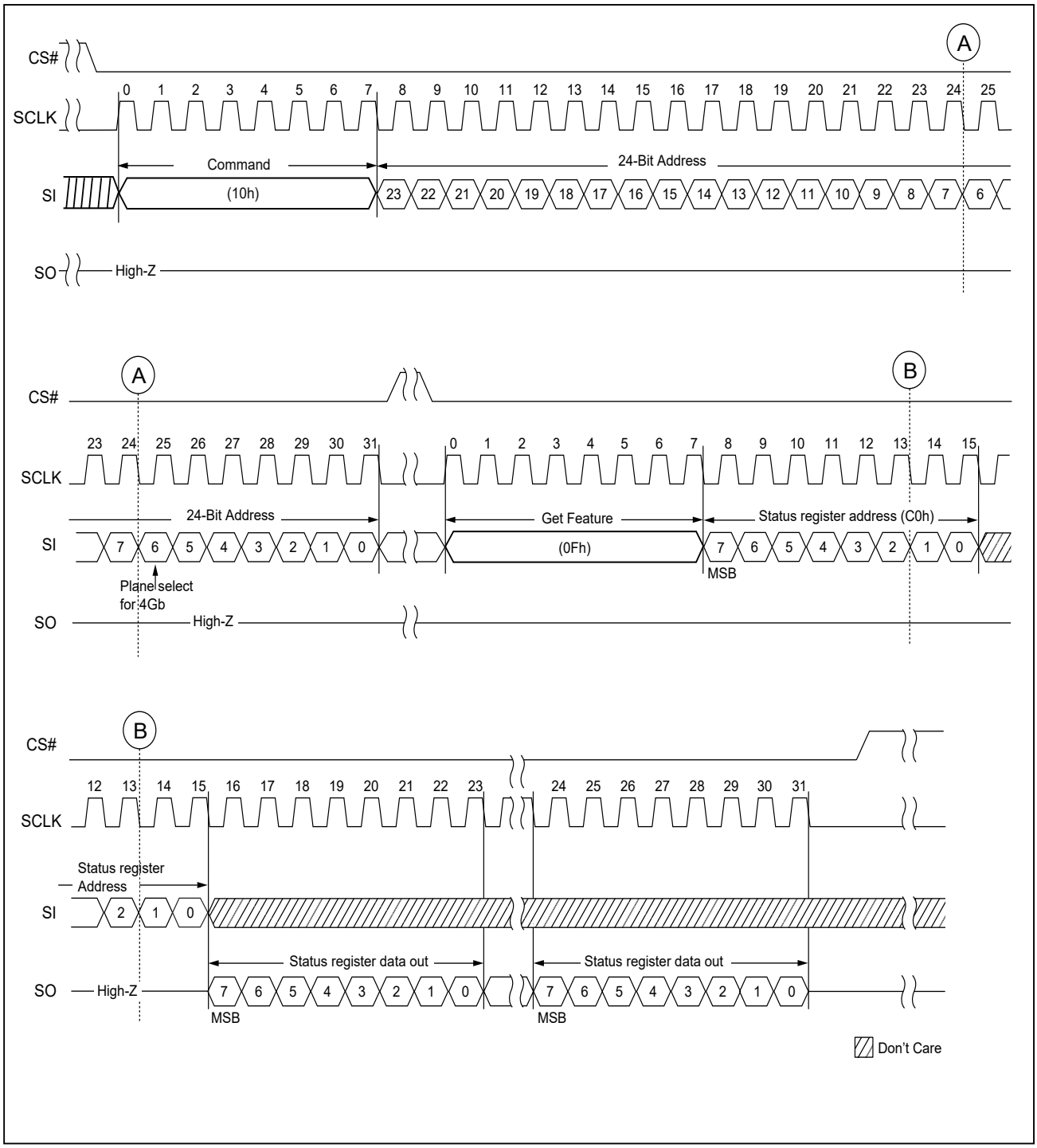


***Note** 1. Bit12 is plane select bit for 2Gb*

***Note** 2. Data byte is 2176 for 1Gb/2Gb*

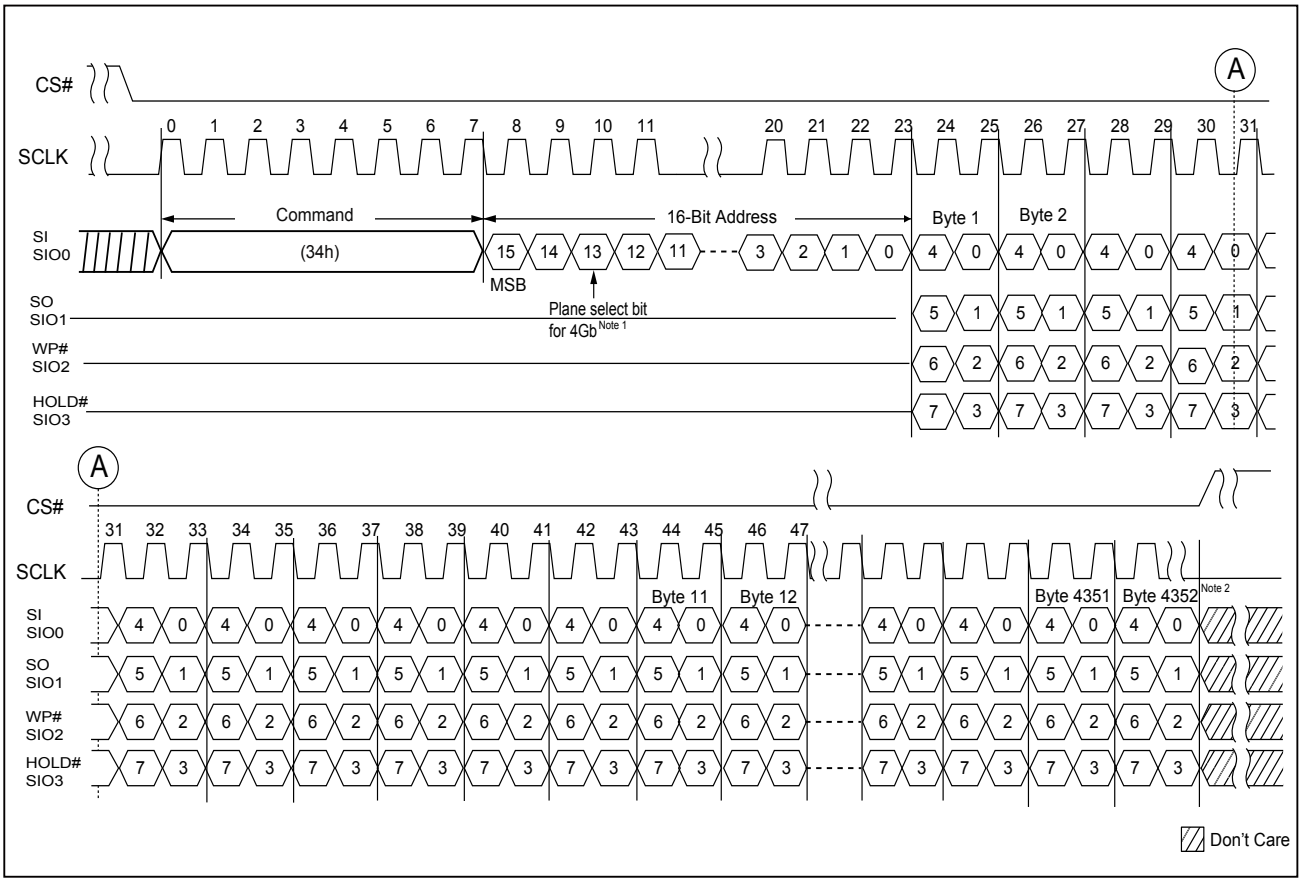
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Figure 26. PROGRAM EXECUTE (10h) Timing



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Figure 27. QUAD IO PROGRAM RANDOM INPUT (34h) Timing



***Note** 1. Bit12 is plane select bit for 2Gb*

***Note** 2. Data byte is 2176 for 1Gb/2Gb*

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10. BLOCK OPERATIONS

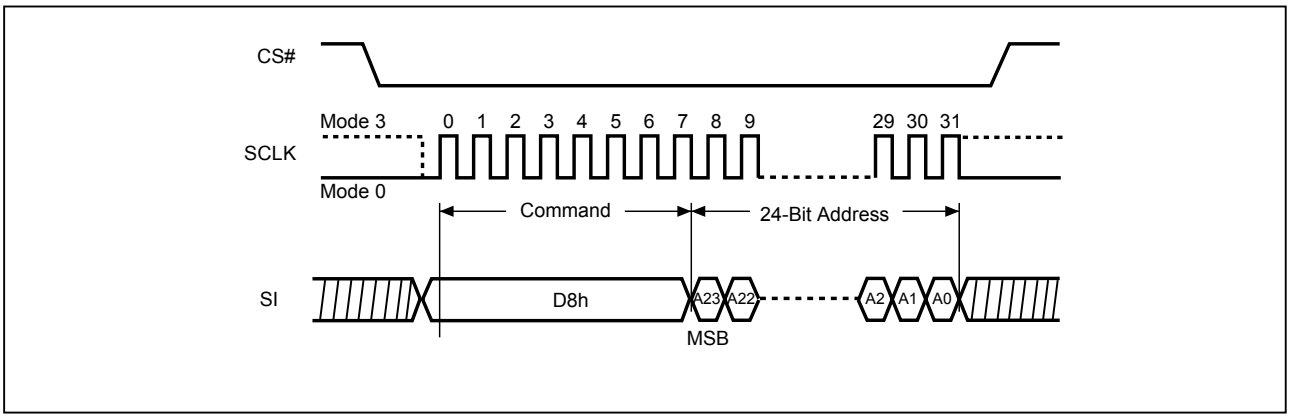
10-1. Block Erase (D8h)

The Block Erase (D8h) instruction is for erasing the data of the chosen block to be "1". The instruction is used for a block of 256K-byte erase operation. A Write Enable (WREN) instruction be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (D8h). Any address of the block is a valid address for Block Erase (D8h) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed. Finally, a Get Feature(0Fh) instruction to check the status is necessary.

The sequence of issuing Block Erase instruction is: CS# goes low→ sending Block Erase instruction code→ 24-bit address on SI→CS# goes high.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Get Feature (0Fh) instruction with Address (C0h) may check the status of the operation during the Block Erase cycle is in progress (please refer to **"Figure 6. GET FEATURE (0Fh) Timing"** and **"Table 3. Feature Settings"**). The OIP bit is "1" during the tBE timing, and is cleared to "0" when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

Figure 28. Block Erase (BE) Sequence



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11. Feature Register

Feature register defines various register's definitions (Block Protection, Secure OTP, Status register). The definition of each register is defined in **"Table 8. Definition of Protection Bits"**.

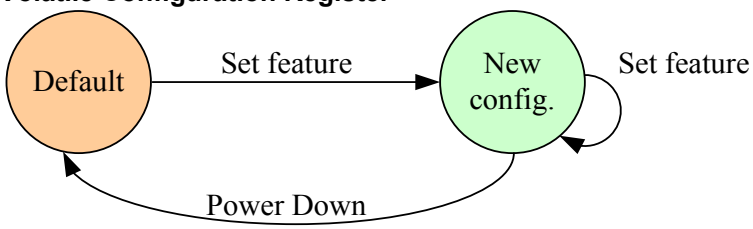
11-1. Configuration Feature Operation

11-1-1. Type: Volatile Register [Symbol: V]

Default value: can not be changed.

Set feature command to change configuration register.

Figure 29. Setting of Volatile Configuration Register

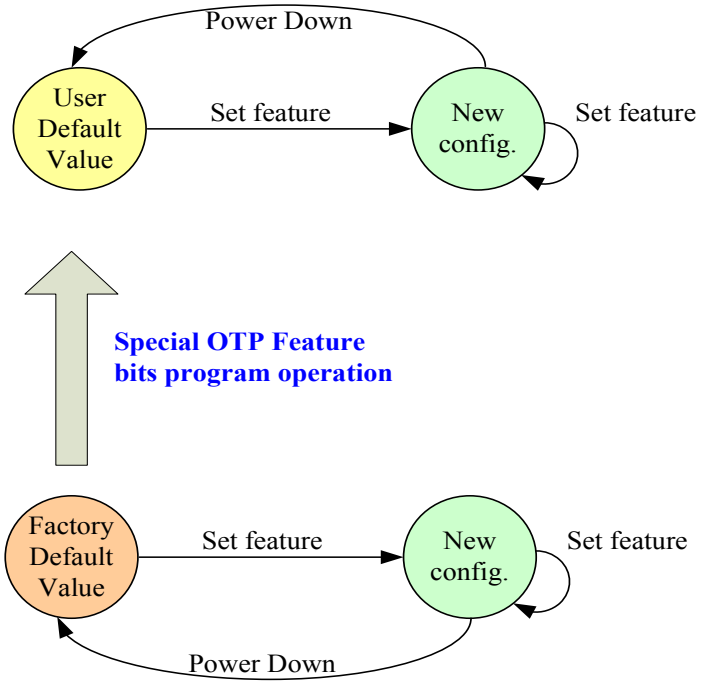


11-1-2. Type: Volatile Register with OTP Fuse Default Value [Symbol: V2]

Default value: can be changed by special OTP Configuration Register program operation.

Set feature command to change value of configuration register. Those configuration register bits of type V2 are: RANDOPT, RANDEN, DS_IO[1:0].

Figure 30. Setting of Volatile Configuration Register (Type: V2)



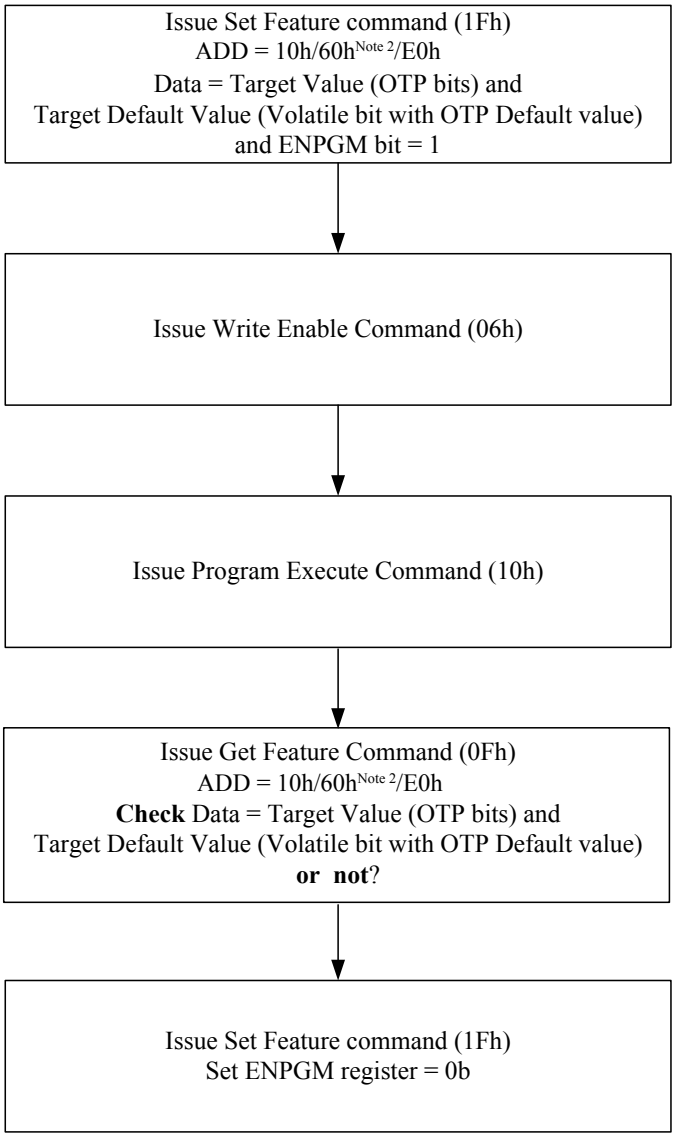
11-1-3. Type: One-time Setting Register [Symbol: OTP]

Configuration register bits of OTP type: SPI_NOR_EN, OTPRWSP bit (only for 1Gb/2Gb).

The OTP Configuration Register bits can be only changed from 0 to 1 through Special OTP Configuration Register Program Operation.

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Figure 46-3. Special OTP Configuration Register Program Operation (for V2/OTP Type of Configuration Register Bits)



Notes:

1. OTP Configuration Registers can be programmed together or individually by this programming flow.

2. ADD(60h) is only for 1Gb/2Gb. It is recommended to program OTPRWSP register for V2/OTP type Configuration Register solid protection. The related V2/OTP type Configuration Registers can't be changed anymore, while OTPRWSP=1b.

11-2. OTP "Configuration" Register Solid Protection (for 1Gb/2Gb)

To avoid the OTP register bits and OTP Fuse value of V2 type Register bits to be programmed accidentally, this chip provide OTPRWSP (OTP register write solid protection) register to prevent it.

If OTPRWSP register bit is not programmed, the V2/OTP type registers (e.g. RANDOPT, RANDEN, DS_ IO[1:0], SPI_NOR_EN) can be programmed; after the OTPRWSP register is programmed, the V2/OTP type registers can not be programmed anymore.

User should program OTPRWSP register even though they do not want to change the V2/OTP register. This can avoid the accidental programming of the V2/OTP register during later usage.

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11-3. Block Protection Feature

The Block Protection feature includes three block protection bits (BPx), Block Protection Register Write Disable (BPRWD). Inverse bit (INVERT), complement bit (COMPLEMENTARY) and Solid Protection Bit (SP).

Soft Protection Mode (SPM)

The SPM uses the BPx bits, INVERT, and COMPLEMENTARY bits to allow part of memory to be protected as read only. The protected area definition is shown as **"Table 8. Definition of Protection Bits"**. The protected areas are more flexible which may protect various area by setting value of BP0-BP2 and Invert bit, and Complementary bit. These are volatile bits and can be modified by set feature command.

After power-up, the chip is in protection state, that is, the feature bits BPx is 1, all other bits (BPRWD, INVERT, COMPLEMENTARY and SP) are 0. The Set feature instruction (1Fh) with feature address (A0h) may change the value of the block protection bits and un-protect whole chip or a certain area for further program/erase operation. For example, after the power-on, the whole chip is protected from program/erase operation, the top 1/64 area may be un-protected by using the Set feature instruction (1Fh) with the feature address (A0h) to change the values of BP2 and BP1 from "1" to "0" as **"Table 8. Definition of Protection Bits"** below.

Hardware Protection Mode (HPM) & Solid Protection Mode (SDPM)

Under the Hardware Protection mode and Solid Protection Mode, the (BPx, INVERT, COMPLEMENTART) bits can not be changed.

Hardware Protection Mode: The device enters HPM if BPRWD bits is set to 1 and WP#/SIO2 is driven to 0.

Note 1: *HPM also requires SP bit to be 0 state .*

Note 2: *The Quad mode is not supported in HPM.*

Solid Protection Mode: If SP bit is set to 1, the device enters SDPM. After that, the selected block is solid protected and can not be un-protected until next power cycle.

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Table 8. Definition of Protection Bits

BP2	BP1	BP0	Invert	Complementary	Protection Area
0	0	0	x	x	all unlocked
0	0	1	0	0	upper 1/64 locked
0	1	0	0	0	upper 1/32 locked
0	1	1	0	0	upper 1/16 locked
1	0	0	0	0	upper 1/8 locked
1	0	1	0	0	upper 1/4 locked
1	1	0	0	0	upper 1/2 locked
1	1	1	x	x	all locked (default)
0	0	1	1	0	lower 1/64 locked
0	1	0	1	0	lower 1/32 locked
0	1	1	1	0	lower 1/16 locked
1	0	0	1	0	lower 1/8 locked
1	0	1	1	0	lower 1/4 locked
1	1	0	1	0	lower 1/2 locked
0	0	1	0	1	lower 63/64 locked
0	1	0	0	1	lower 31/32 locked
0	1	1	0	1	lower 15/16 locked
1	0	0	0	1	lower 7/8 locked
1	0	1	0	1	lower 3/4 locked
1	1	0	0	1	block 0
0	0	1	1	1	upper 63/64 locked
0	1	0	1	1	upper 31/32 locked
0	1	1	1	1	upper 15/16 locked
1	0	0	1	1	upper 7/8 locked
1	0	1	1	1	upper 3/4 locked
1	1	0	1	1	block0

Note: *Block #0 is at lower portion.*

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11-4. Secure OTP (One-Time-Programmable) Feature

There is an Secure OTP area which has 30 full pages (30 x 2176-byte for 1Gb/2Gb or 30 x 4352-byte for 4Gb) from page 02h to page 1Fh guarantee to be good for system device serial number storage or other fixed code storage. The Secure OTP area is a non-erasable and one-time-programmable area, which is default to “1” and allows partial page program to be “0”, once the Secure OTP protection mode is set, the Secure OTP area becomes read-only and cannot be programmed again. The OTP area is scrambled if randomizer function is enabled.

The Secure OTP operation is operated by the Set Feature instruction with feature address (B0h) to access the Secure OTP operation mode and Secure OTP protection mode.

To check the NAND device is ready or busy in the Secure OTP operation mode, the status register bit 0 (OIP bit) may report the status by Get Feature command operation.

To exit the Secure OTP operation or protect mode, it can be done by writing "0" to both Bit7 (Secure OTP protect bit) and bit6 (Secure OTP enable bit) for returning to the normal operation.

Secure OTP Read

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set the "Secure OTP Enabled Bit" as "1".
3. Issuing normal Page Read command (13h)

Secure OTP Program (if the "Secure OTP Protection Bit" is "0") for

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set the "Secure OTP Enabled Bit" as "1".
3. Issuing Page Program command (02h)
4. Issuing program execute command (10h)

Secure OTP Protection

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set both the "Secure OTP Protection Bit" and "Secure OTP Enabled Bit" as "1".
3. Issuing program execute command (10h)

Table 9. Secure OTP States

Secure OTP Protection Bit[Note1]	Secure OTP Enabled Bit	State
0	0	Normal operation
0	1	Access the Secure OTP for reading or programming
1	0	Not applicable
1	1	Secure OTP Protection by using the Program Execution command (10h)[Note2]

Note 1. *OTP protection bit is volatile.*

Note 2. *Once the "Secure OTP Protection Bit" and "Secure OTP Enabled Bit" are set as "1", the secure OTP becomes read only.*

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11-5. Status Register

The MX35LFxG24AD provides a status register that outputs the device status by writing a Get Feature command (0Fh) with the feature address (C0h), and then the IO pins output the status.

The Get Feature (0Fh) command with the feature address(C0h) will keep the device at the status read mode unless next valid command is issued. The resulting information is outlined in the table below.

Table 10. Status Register Bit Descriptions

SR Bit	Bit Name	Description
SR[0] (OIP)	Operation in progress	The bit value indicates whether the device is busy in operations of read/ program execute/ erase/ reset command. 1: Busy, 0: Ready
SR[1] (WEL)	Write enable latch	The bit value indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, and then the device can accept program/ erase/write status register instruction. 1: write enable, 0: not write enable. The bit value will be cleared (as "0") by issuing Write Disable command(04h) or after the program/erase operation completion.
SR[2] (ERS_Fail)	Erase fail	The bit value shows the status of erase failure or if host erase any invalid address. 0: Passed, 1: Failed. The bit value will be cleared (as "0") by RESET command or at the beginning of the block erase command operation.
SR[3] (PGM_Fail)	Program fail	The bit value shows the status of program failure or if host program any invalid address. 0: Passed, 1: Failed. The bit value will be cleared (as "0") by RESET command or during the program execute command operation.
SR[6:4]	Reserved	
SR[7] (CRBSY)	Cache Status Bit	The bit value indicates whether the internal cache is busy in Page Read Cache Operations. 1: Busy- internal cache is busy on data transfer 0: Ready- device is ready for cache data out

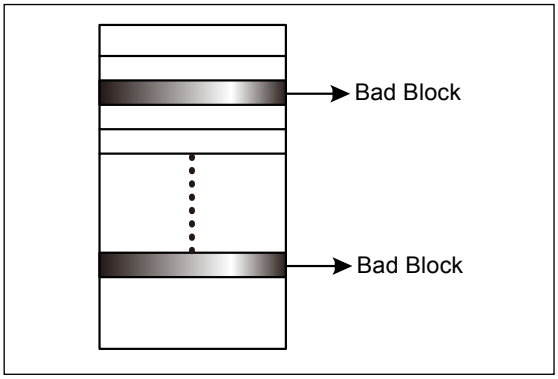
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12. SOFTWARE ALGORITHM

12-1. Invalid Blocks (Bad Blocks)

The bad blocks are included in the device while it gets shipped. During the time of using the device, the additional bad blocks might be increasing; therefore, it is necessary to check the bad block marks and avoid using the bad blocks. Furthermore, please read out the bad block information before any erase operation since the bad block marks may be cleared by any erase operation.

Figure 31. Bad Blocks



While the device is shipped, the value of all data bytes of the good blocks are FFh. The 1st byte of the 1st and 2nd page in the spare area for bad block will be 00h. The erase operation at the bad blocks is not recommended.

After the device is installed in the system, the bad block checking is recommended. **"Figure 32. Bad Block Test Flow"** shows the brief test flow by the system software managing the bad blocks while the bad blocks were found. When a block gets damaged, it should not be used any more.

Due to the blocks are isolated from bit-line by the selected gate, the performance of good blocks will not be impacted by bad ones.

Table 11. Valid Blocks

	Density	Min.	Typ.	Max.	Unit	Remark
Valid (Good) Block Number	1Gb	1004		1024	Block	Block 0-7 is guaranteed to be good at the time of shipment (with ECC implementation by host)
	2Gb	2008		2048	Block	Block#0-7 are guaranteed to be good at the time of shipment (with ECC implementation by host)
	4Gb	2008		2048	Block	Block#0-7 are guaranteed to be good at the time of shipment (with ECC implementation by host)

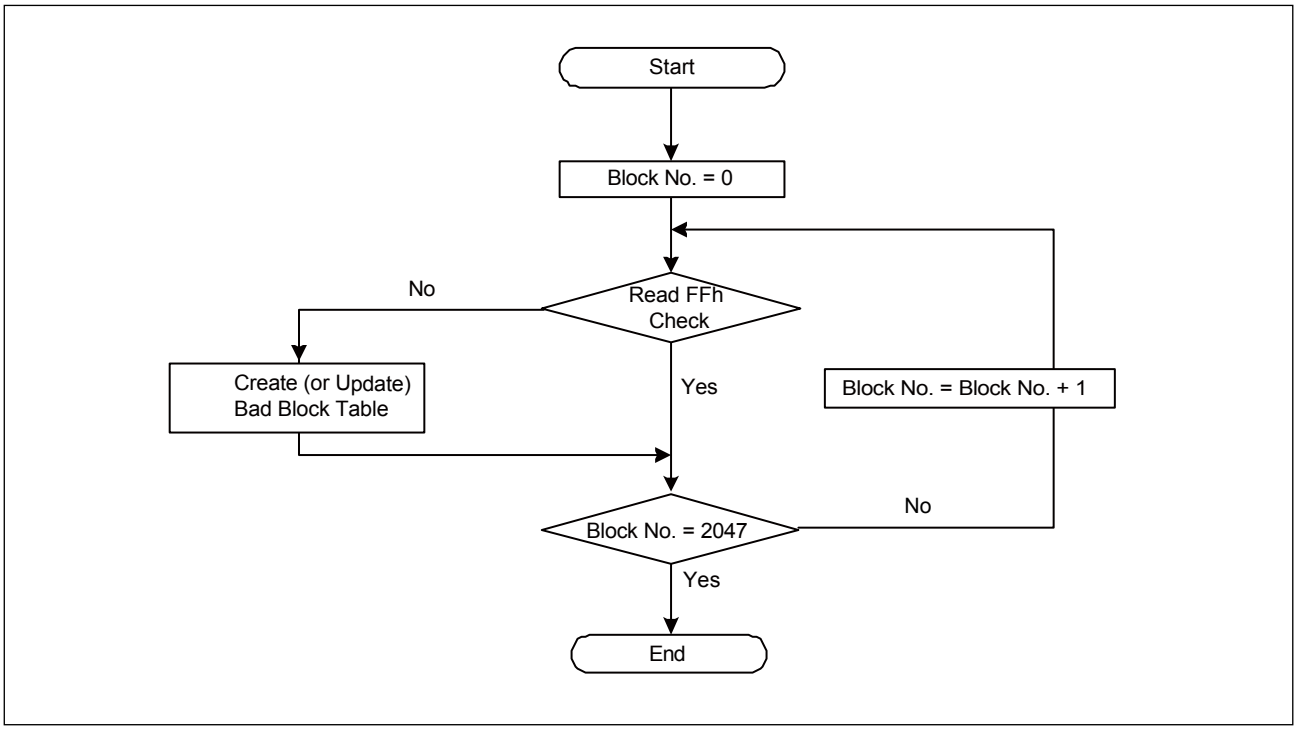
Note: *The total good block numbers will not be less than minimum good block numbers during the NAND device lifetime.*

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12-2. Bad Block Test Flow

Although the initial bad blocks are marked by the flash vendor, they could be inadvertently erased and destroyed by a user that does not pay attention to them. To prevent this from occurring, it is necessary to always know where any bad blocks are located. Continually checking for bad block markers during normal use would be very time consuming, so it is highly recommended to initially locate all bad blocks and build a bad block table and reference it during normal NAND flash use. This will prevent having the initial bad block markers erased by an unexpected program or erase operation. Failure to keep track of bad blocks can be fatal for the application. For example, if boot code is programmed into a bad block, a boot up failure may occur. **"Figure 32. Bad Block Test Flow"** shows the recommended flow for creating a bad block table.

Figure 32. Bad Block Test Flow



12-3. Failure Phenomena for Read/Program/Erase Operations

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system:

Table 12. Failure Modes

Failure Mode	Detection and Countermeasure	Sequence
Erase Failure	Status Read after Erase	Block Replacement
Programming Failure	Status Read after Program	Block Replacement
Read Failure	Read Failure	ECC

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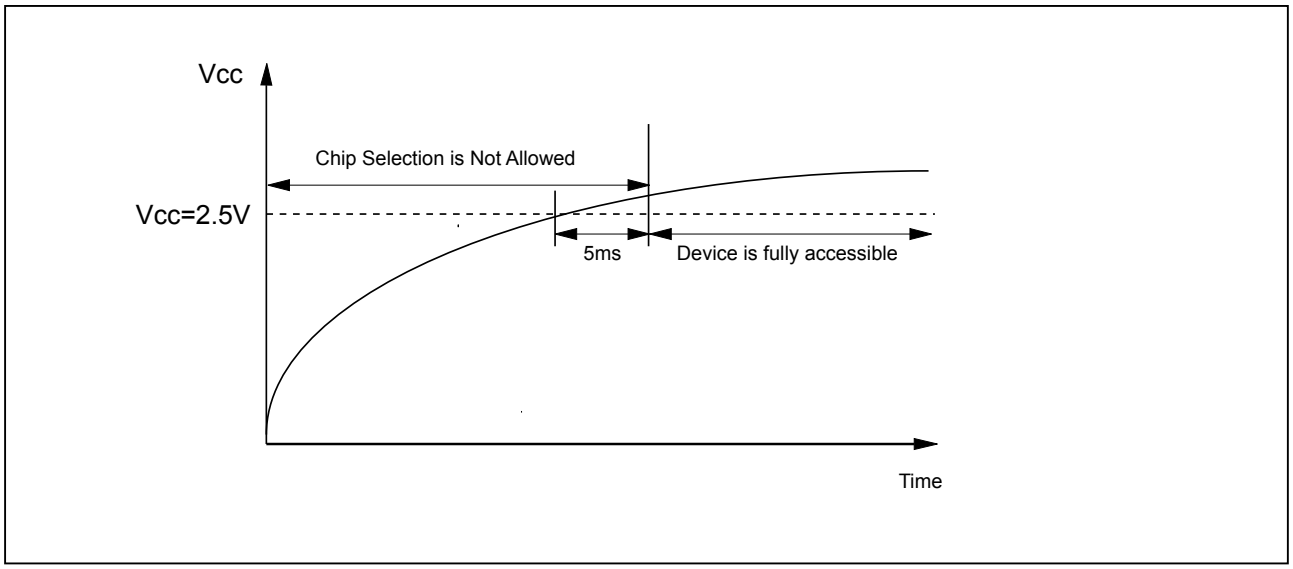
13. DEVICE POWER-UP

13-1. Power-up

After the Chip reaches the power on level, the internal power on reset sequence will be triggered. During the internal power on reset period, no any external command is accepted. The device can be fully accessible when VCC reaches the power-on level and wait 5ms.

During the power on and power off sequence, it is necessary to keep the WP# = Low for internal data protection.

Figure 33. Power On Sequence



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14. PARAMETERS

14-1. ABSOLUTE MAXIMUM RATINGS

Temperature under Bias	-50°C to +125°C
Storage temperature	-65°C to +150°C
All input voltages with respect to ground (Note 2)	-0.6V to 4.6V
VCC supply voltage with respect to ground (Note 2)	-0.6V to 4.6V
ESD protection	>2000V

Notes:

1. The reliability of device may be impaired by exposing to extreme maximum rating conditions for long range of time.

2. Permanent damage may be caused by the stresses higher than the "Absolute Maximum Ratings" listed.

*3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, please refer to **"Figure 34. Maximum Negative Overshoot Waveform"** and **"Figure 35. Maximum Positive Overshoot Waveform"**.*

Figure 34. Maximum Negative Overshoot Waveform

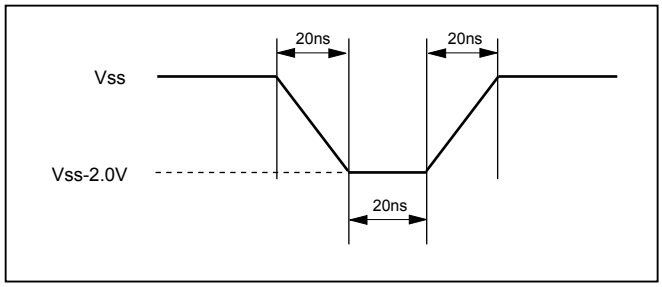
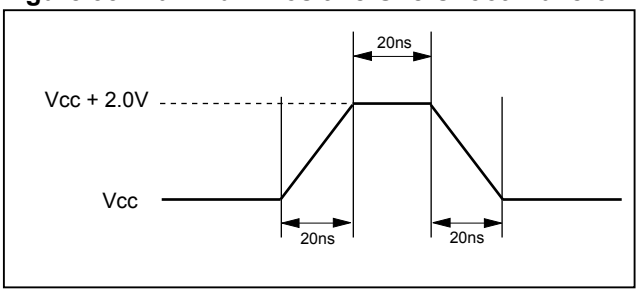


Figure 35. Maximum Positive Overshoot Waveform



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Table 13. AC Testing Conditions

Testing Conditions	Value	Unit
Input pulse level	0 to VCC	V
Output load capacitance	1TTL+CL(30)	pF
Input rising & falling time	5	ns
Input timing measurement reference levels	VCC/2	V
Output timing measurement reference levels	VCC/2	V

Table 14. Capacitance

TA = +25°C, F = 1 MHz

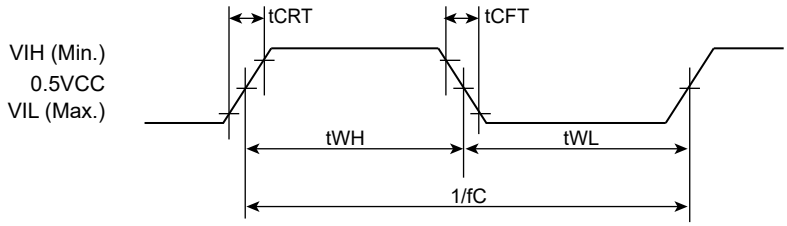
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
CIN	Input capacitance			6	pF	VIN = 0V
COUT	Output capacitance			8	pF	VOUT = 0V

Note: *CIN/COUT=10pF/10pF for 4Gb*

Table 15. Operating Range

Temperature	VCC	Tolerance
-40°C to + 85°C	+3.3V	2.7 - 3.6V

Figure 36. SCLK TIMING DEFINITION



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Table 16. DC Characteristics

Symbol	Parameter	Min.	Typical	Max.	Unit	Test Conditions
ILI	Input leakage current			+/- 10	uA	VIN= 0 to VCC Max.
ILO	Output leakage current			+/- 10	uA	VOUT= 0 to VCC Max.
ISB1	VCC standby current (CMOS)		15	50	uA	VIN=VCC or GND, CS#=VCC
ICC1	VCC active current (Sequential Read)		20	30	mA	f=120MHz, Iout = 0mA
ICC2	VCC active current (Program)		20	30	mA	
ICC3	VCC active current (Erase)		15	30	mA	
VIL	Input low level	-0.3		0.2VCC	V	
VIH	Input high level	0.8VCC		VCC + 0.3	V	
VOL	Outout low voltage			0.2	V	IOL= -1mA
VOH	Outout high voltage	VCC-0.2			V	IOH= -20uA

Table 17. General Timing Characteristics

Symbol	Parameter	Note	Min.	Max.	Unit
fC	Serial Clock Frequency for all command	1	D.C.	120	MHz
tCHHH	HOLD# Hold Time (relative to SCLK)		3.75	-	ns
tCHHL	HOLD Hold Time (relative to SCLK)		3.75	-	ns
tCS	CS# Diselect Time		30	-	ns
tCHSH	CS# Active Hold Time (relative to SCLK)		4	-	ns
tSLCH	CS# Active Setup Time (relative to SCLK)		4	-	ns
tSHCH	CS# Not Active Setup Time (relative to SCLK)		4	-	ns
tCHSL	CS# Not Active Hold Time (relative to SCLK)		4	-	ns
tDIS	Output Disable Time		-	7	ns
tHC	HOLD Setup Time (relative to SCLK)		3.75	-	ns
tHD	HOLD# Setup Time (relative to SCLK)		3.75	-	ns
tHDDAT	Data Input Hold Time		2	-	ns
tHO	Output Hold Time		1	-	ns
tHZ	HOLD# to Output High-Z		-	15	ns
tLZ	HOLD# to Output Low-Z		-	15	ns
tSUDAT	Data In Setup Time		2	-	ns
tV	Serial Clock Low to Output Valid (30pF)		-	7	ns
	Serial Clock Low to Output Valid (15pF)		-	6	ns
tWH	Serial Clock High Time		3.75	-	ns
tWL	Serial Clock Low Time		3.75	-	ns
tCRT	Clock Rise Time (peak to peak)		1.3	-	V/ns
tCFT	Clock Fall Time (peak to peak)		1.3	-	V/ns
tWPH	Write protect Hold Time		100	-	ns
tWPS	Write protect Setup Time		20	-	ns
tVSL	VCC(min.) to device operation		5	-	ms
tRST	Device reset time (Idle/ Read/ Program/ Erase)	2		5/5/10/500	us

Notes:

1*: Max. clock rate=108MHz for BBh/EBh command, and 20MHz for 03h command.*

2: *the tRST is 5ms for the first RESET command after Power-on.*

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Table 18. Program/ Read/ Erase Characteristics

Symbol	Parameter	Note	Typical	Max.	Unit
tRD	The data transfering from array to buffer			25	us
tPROG	Page programming time (Randomizer disabled)		320	700	us
tPROG_RAND	Page programming time (Randomizer enabled)		360	740	us
tRCBSY (Read)	Dummy busy time for cache read		4.5	25	us
tERASE	Block Erase Time		4	6	ms
NOP	Number of partial program cycles in same page			4	times

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Figure 37. WP# Setup Timing and Hold Timing during SET FEATURE when BPRWD=1

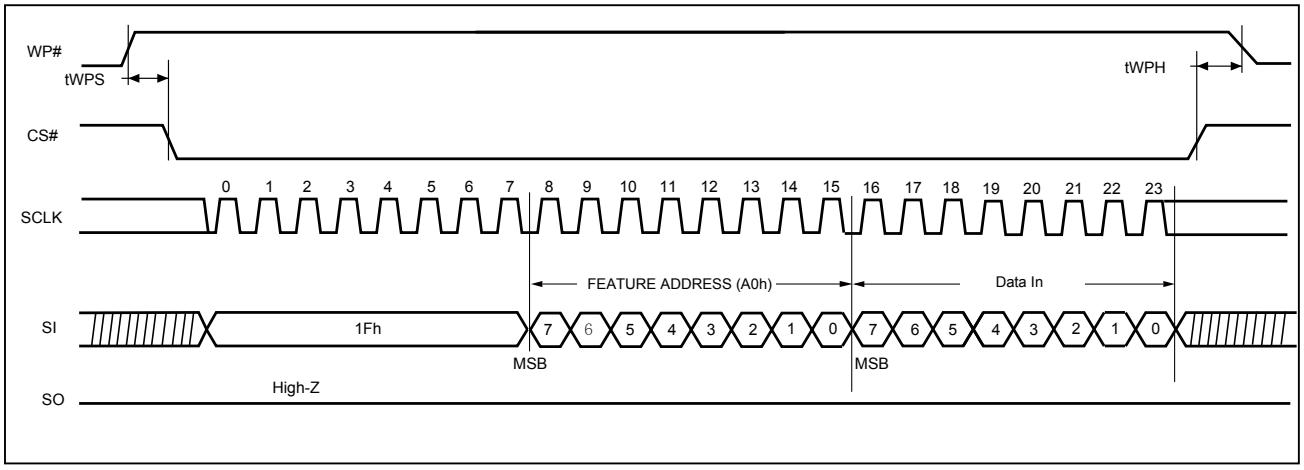


Figure 38. Serial Input Timing

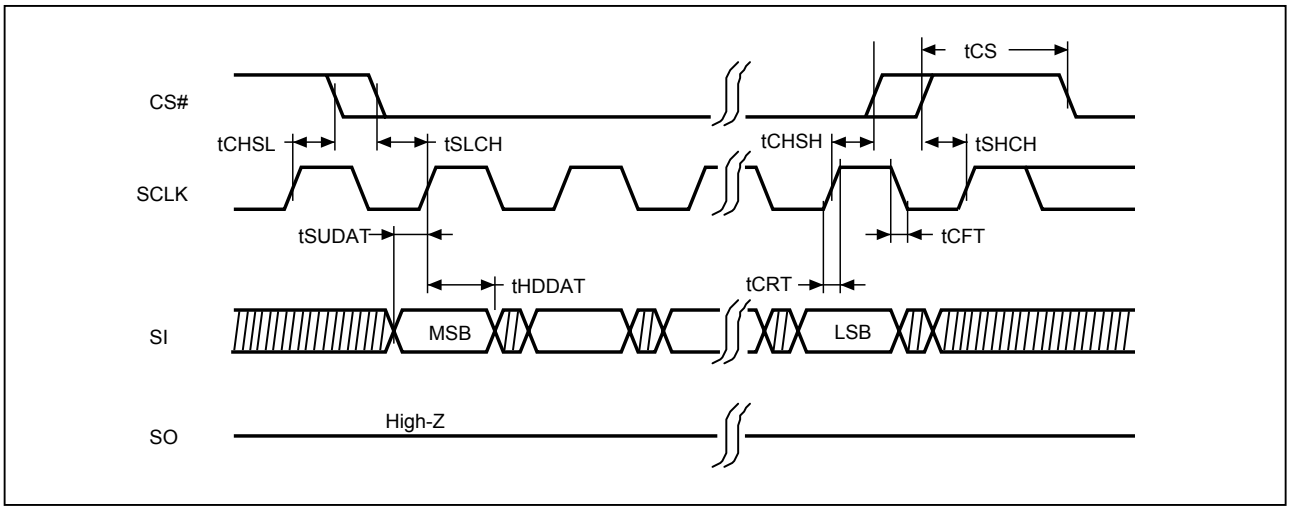
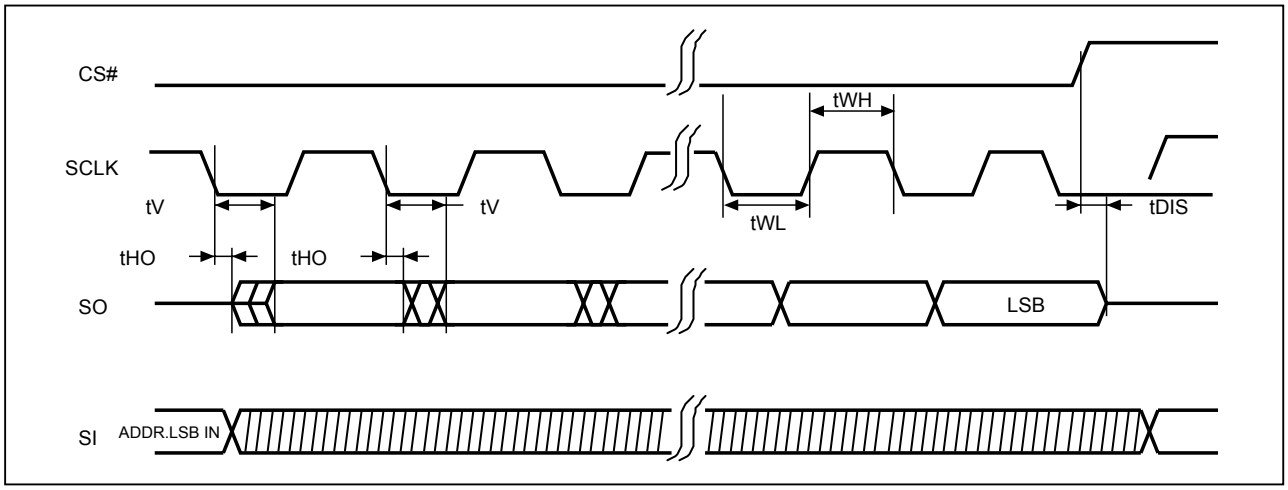
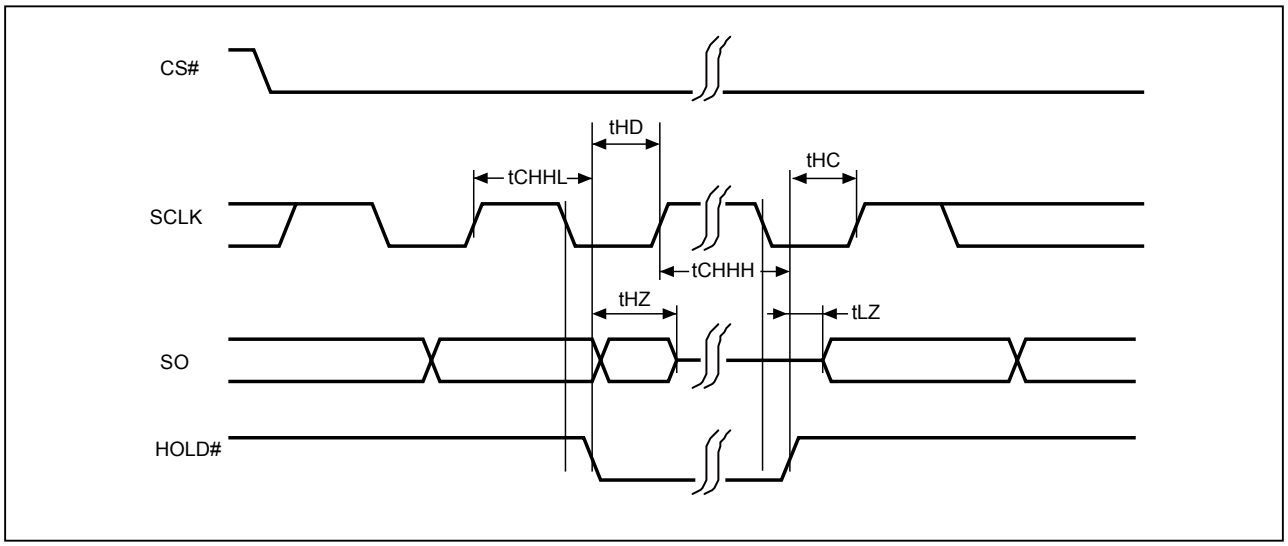


Figure 39. Serial Output Timing



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Figure 40. Hold Timing



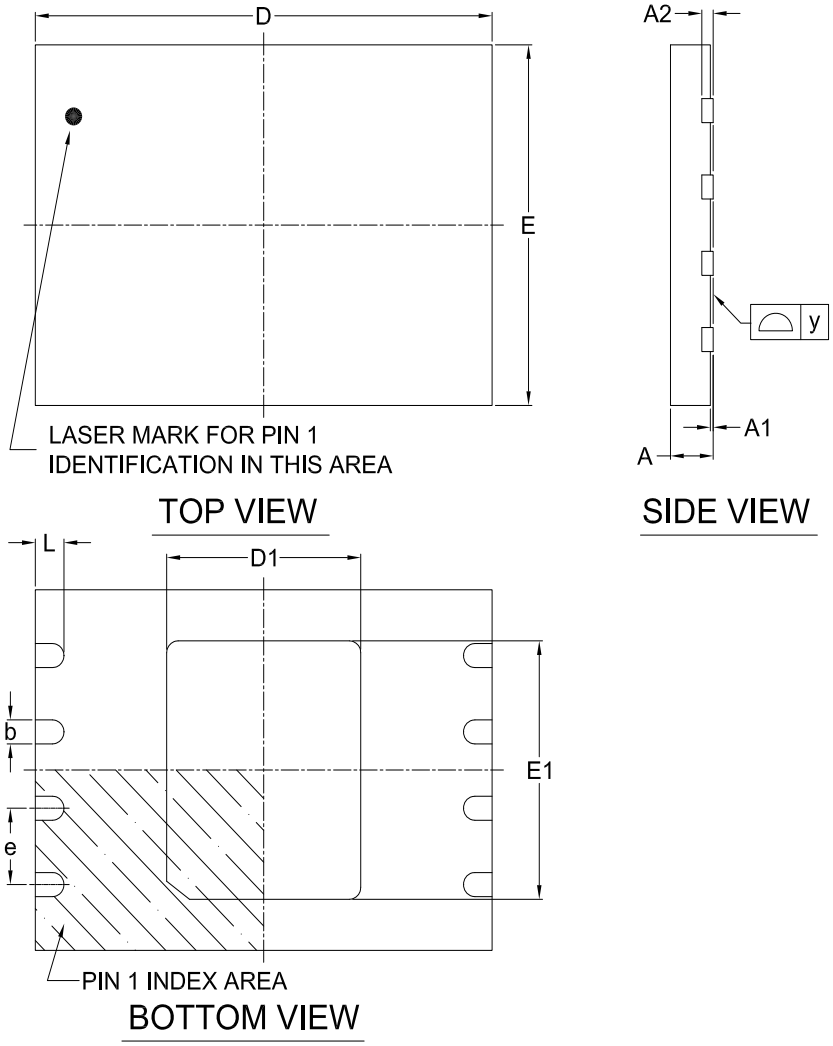
Note: *SI is "don't care" during HOLD operation.*

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15. PACKAGE INFORMATION

15-1. 8-WSON (8x6x0.8mm)

Doc. Title: Package Outline for WSON 8L (8x6x0.8MM, LEAD PITCH 1.27MM, E.P. 3.4x4.3MM)



Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	7.90	3.35	5.90	4.25	0.45	---	0.00
	Nom.	---	---	0.20	0.40	8.00	3.40	6.00	4.30	0.50	1.27	---
	Max.	0.80	0.05	---	0.48	8.10	3.45	6.10	4.35	0.55	---	0.05
Inch	Min.	0.028	---	---	0.014	0.311	0.132	0.232	0.167	0.018	---	0.00
	Nom.	---	---	0.008	0.016	0.315	0.134	0.236	0.169	0.020	0.05	---
	Max.	0.032	0.002	---	0.019	0.319	0.136	0.240	0.171	0.022	---	0.002

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16. REVISION HISTORY

Revision	Descriptions	Page
August 28, 2018		
0.00	Initial Release	ALL
September 03, 2019		
0.01	1. New adding the 2Gb spec	ALL
	2. Revised timing spec as tPROG(typ): 320us, tPROG_RAND(typ): 360us, tERASE(typ.): 3.2ms, tERASE(max.) 6ms	P5, 54
	3. Adding notes of for the Command Set table to specify the dual I/O mode and quad I/O mode	P11
	4. Reorganized the configuration register table and remove the PBLEN bit	P13
	5. Unified the command name of (03h, 0Bh) as “Read from cache” command	P15, 17
	6. Remove SPI NOR compatible command function	P13, 15
	7. Added byte#169 for ONFI Table	P31, 34
	8. Modified description of CRBSY from “Cache sequential” to “Cache operations	P48
	9. Revised for the block#0-7 good at shipping	P49
	10. Modified the Bad Block Test flow	P50
January 21, 2020		
0.02	1. Added a note about Reliability report.	P5
	2. Modified ICC1/ICC2/tERASE/tRCBSY(Read) typical spec and tSUDAT minimum spec	P5, 56
	3. Changed title as "Preliminary" and add 1Gb	ALL
	4. Removed Deep power-down mode	P5, 11, 56
	5.Added ADD=60h in the Configuration Register, which support SPI_NOR_EN and OTPRWSP function.	P13,29, P30-31,47
	6. Waveforms modification for address definition alignment	P17-21, P37-39, 45
	7. Supplement table 10 on the WEL is clear after program/erase completion	P51
	8. Added note of Table 11.	P52
	9. Modified the tWH/tWL waveform of Fig.36	P58
	10. Added tCRT and tCFT values.	P56
	11. Modified descriptions.	P27, 29, 48

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Revision	Descriptions	Page
May 21, 2020		
1.0	1. Removal of "Preliminary" title and added note of "preliminary stage" on 1G/2G.	ALL
	2. Revised the note descriptions of Parameter Page Data Structure Tables.	P34, 36, 38
	3. Added Section 11-2 for OTPRWSP (for 1Gb/2Gb).	P47
	4. Added the figure of SCLK timing.	P56
	5. Corrected name of symbol from SCK to SCLK.	P57
	6. Moved tRST parameter from Table 18 to Table 17.	P57-58
	7. Removed the SPI_NOR_EN and OTPRWSP specs from 4Gb.	P13, 29, 46-47
	8. Format adjustment.	P46-47
	9. SR[3:2] is not available for protected area (including protected blocks or protected Secure OTP area).	P51

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