*3V, 1G-bit NAND Flash Memory*

# MX30LF1G18AC

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# 1. FEATURES

- 1G-bit SLC NAND Flash
  - Bus: x8
  - Page size: (2048+64) byte,
  - Block size: (128K+4K) byte,
- **ONFI 1.0 compliant**
- **Multiplexed Command/Address/Data**
- **User Redundancy**
  - 64-byte attached to each page
- **Fast Read Access**
  - Latency of array to register: 25us
  - Sequential read: 20ns
- **Cache Read Support**
- **Page Program Operation**
  - Page program time: 300us( typ.)
- **Cache Program Support**
- **Block Erase Operation**
  - Block erase time: 1ms (typ.)
- **Single Voltage Operation:**
  - VCC: 2.7 - 3.6V
- **Low Power Dissipation**
  - Max. 30mA
    Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max) standby current
- **Hardware Data Protection:** WP# pin
- **Block Protection**

  - PT (Protection) pin: active high at power-on, which protects the entire chip. The pin has an internal weak pull down.

  - Temporary protection/un-protection function (enabling by PT pin)

  - Solid protection
  (enabling by PT pin)
- **Device Status Indicators**
  - Ready/Busy (R/B#) pin
  - Status Register
- **Chip Enable Don't Care**
  - Simplify System Interface
- **Unique ID Read support (ONFI)**
- **Secure OTP support**
- **High Reliability**
  - Endurance: typical 100K cycles (with 4-bit ECC per (512+16) Byte)
  - Data Retention: 10 years
- **Wide Temperature Operating Range**
  -40°C to +85°C
- Package:

  1) 48-TSOP(I) (12mm x 20mm)

  2) 63-ball 9mmx11mm VFBGA

  All packaged devices are RoHS Compliant and Halogen-free.


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# 2. GENERAL DESCRIPTIONS

The MX30LF1G18AC is a 1Gb SLC NAND Flash memory device. Its standard NAND Flash features and reliable quality of typical P/E cycles 100K (with ECC), which makes it most suitable for embedded system code and data storage.

The product family requires 4-bit ECC per (512+16)B.

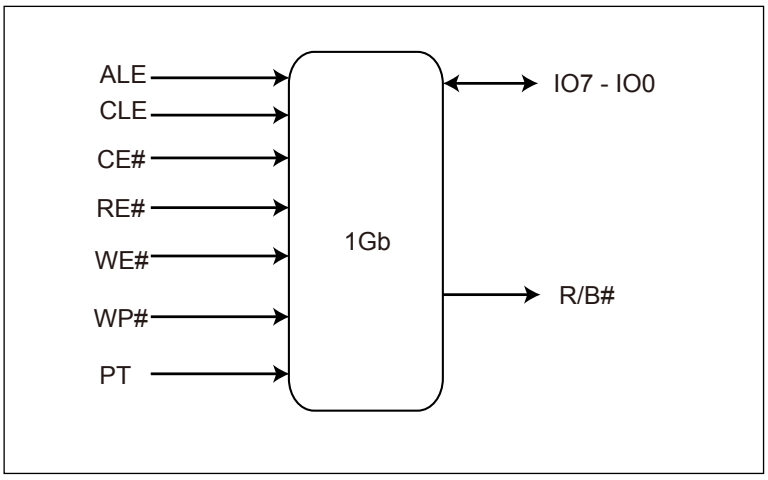
The MX30LF1G18AC is typically accessed in pages of 2,112 bytes for read and program operations.

The MX30LF1G18AC array is organized as thousands of blocks, which is composed by 64 pages of (2,048+64) byte in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 64 bytes for ECC and other purposes. The device has an on-chip buffer of 2,112 bytes for data load and access.

The Cache Read Operation of the MX30LF1G18AC enables first-byte read-access latency of 25us and sequential read of 20ns and the latency time of next sequential page will be shorten from tR to tRCBSY.

The MX30LF1G18AC power consumption is 30mA during all modes of operations (Read/Program/Erase), and 50uA in standby mode.

**Figure 1. Logic Diagram**

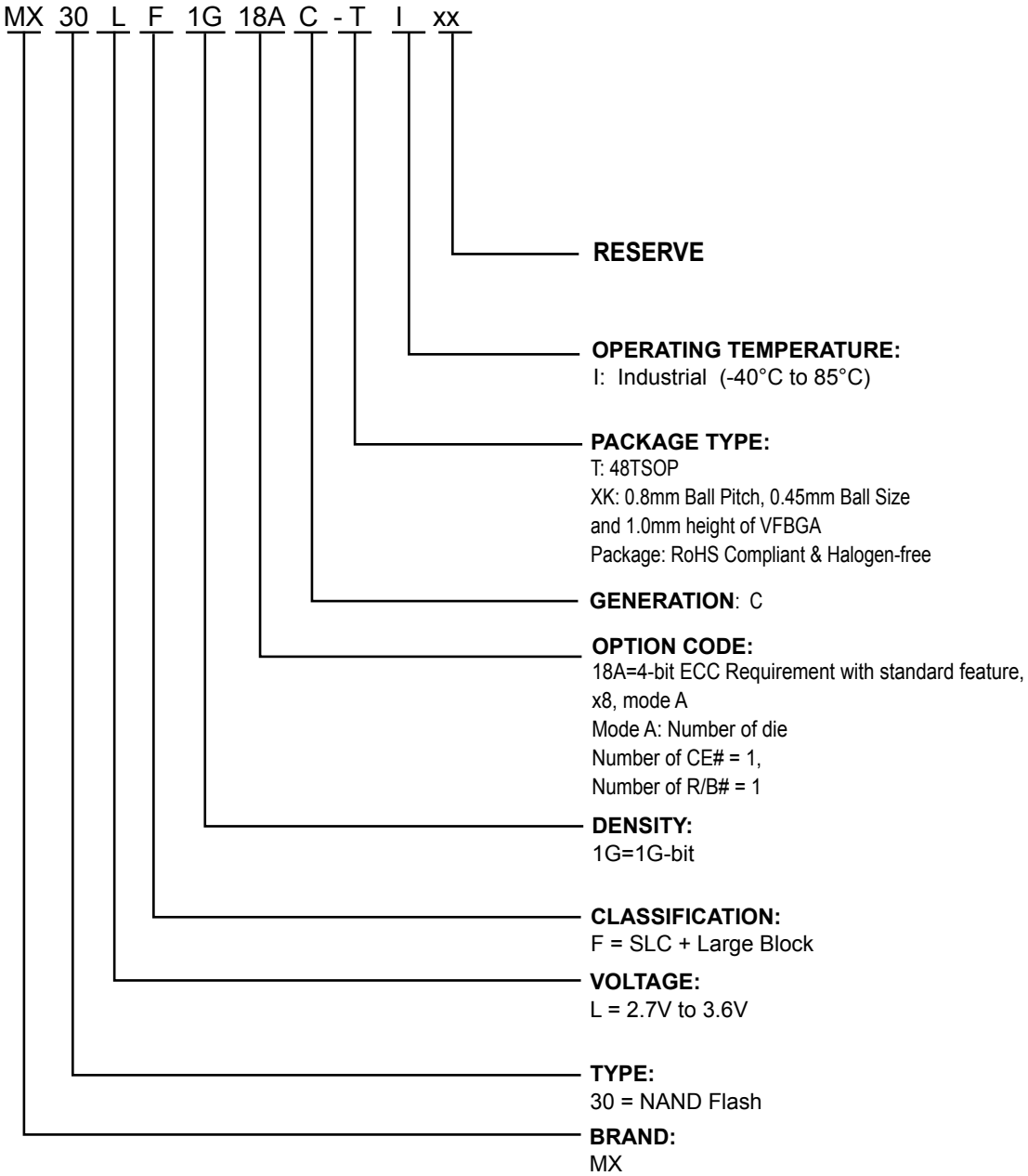




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## 2-1. ORDERING INFORMATION

### Part Name Description

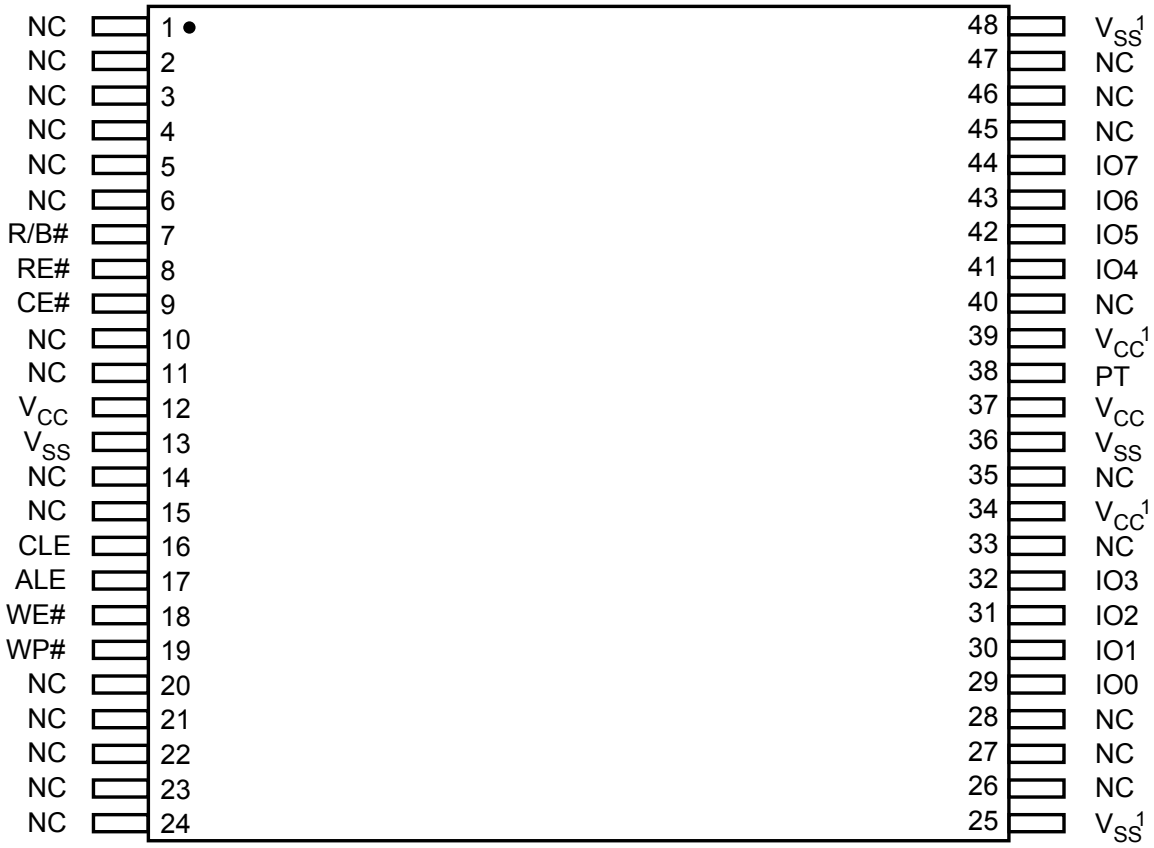



| Part Number | Density | Organization | VCC Range | Package | Temperature Grade |
|---|---|---|---|---|---|
| MX30LF1G18AC-TI | 1Gb | x8 | 3V | 48-TSOP | Industrial |
| MX30LF1G18AC-XKI | 1Gb | x8 | 3V | 63-VFBGA | Industrial |


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# 3. PIN CONFIGURATIONS

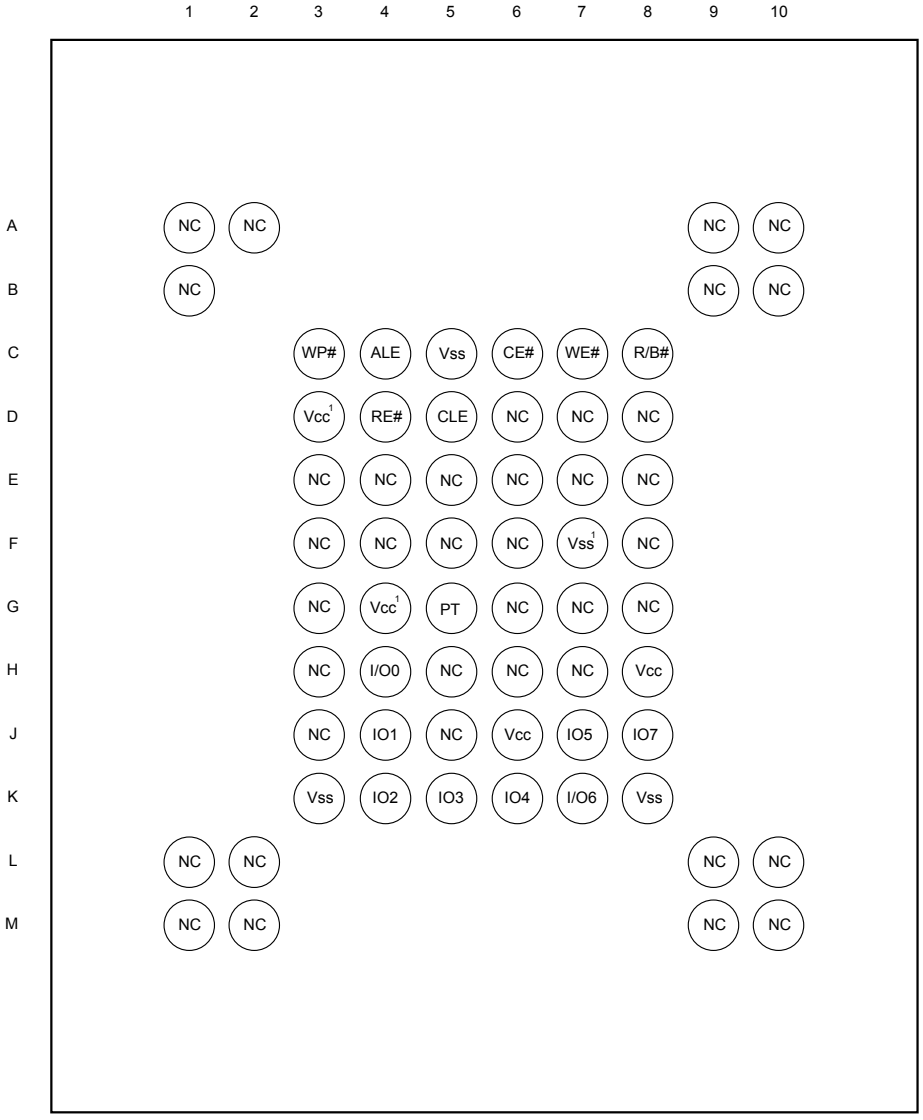
## 48-TSOP




***Note 1.*** *These pins might not be connected internally. However, it is recommended to connect these pins to power(or ground) as designated for ONFI compatibility.*


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## 63-ball 9mmx11mm VFBGA




***Note 1.*** *These pins might not be connected internally; however, it is recommended to connect these pins to power (or ground) as designated for ONFI compatibility.*


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## 3-1. PIN DESCRIPTIONS

| SYMBOL | PIN NAME |
|---|---|
| **IO7 - IO0** | Data I/O port |
| **CE#** | Chip Enable (Active Low) |
| **RE#** | Read Enable (Active Low) |
| **WE#** | Write Enable (Active Low) |
| **CLE** | Command Latch Enable |
| **ALE** | Address Latch Enable |
| **WP#** | Write Protect (Active Low) |
| **PT** | PT (Protection) pin connecting to high for entire chip protected and enabling the Block Protection. A weak pull-down internally. |
| **R/B#** | Ready/Busy (Open Drain) |
| **VSS** | Ground |
| **VCC** | Power Supply for Device Operation |
| **NC** | Not Connected Internally |


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## PIN FUNCTIONS

The MX30LF1G18AC device is a sequential access memory that utilizes multiplexing input of Command/Address/Data.

### I/O PORT: IO7 - IO0

The IO7 to IO0 pins are for address/command input and data output to/from the device.

### CHIP ENABLE: CE#

The device goes into low-power Standby Mode when CE# goes high during a read operation and not at busy stage.

The CE# goes low to enable the device to be ready for standard operation. When the CE# goes high, the device is deselected. However, when the device is at busy stage, the device will not go to standby mode when CE# pin goes high.

### READ ENABLE: RE#

The RE# (Read Enable) allows the data to be output by a tREA time after the falling edge of RE#. The internal address counter is automatically increased by one at the falling edge of RE#.

### WRITE ENABLE: WE#

When the WE# goes low, the address/data/command are latched at the rising edge of WE#.

### COMMAND LATCH ENABLE: CLE

The CLE controls the command input. When the CLE goes high, the command data is latched at the rising edge of the WE#.

### ADDRESS LATCH ENABLE: ALE

The ALE controls the address input. When the ALE goes high, the address is latched at the rising edge of WE#.

### WRITE PROTECT: WP#

The WP# signal keeps low and then the memory will not accept the program/erase operation. It is recommended to keep WP# pin low during power on/off sequence. Please refer to **Figure 37. Power On/Off Sequence**.

### READY/Busy: R/B#

The R/B# is an open-drain output pin. The R/B# outputs the ready/busy status of read/program/erase operation of the device. When the R/B# is at low, the device is busy for read or program or erase operation. When the R/B# is at high, the read/program/erase operation is finished.

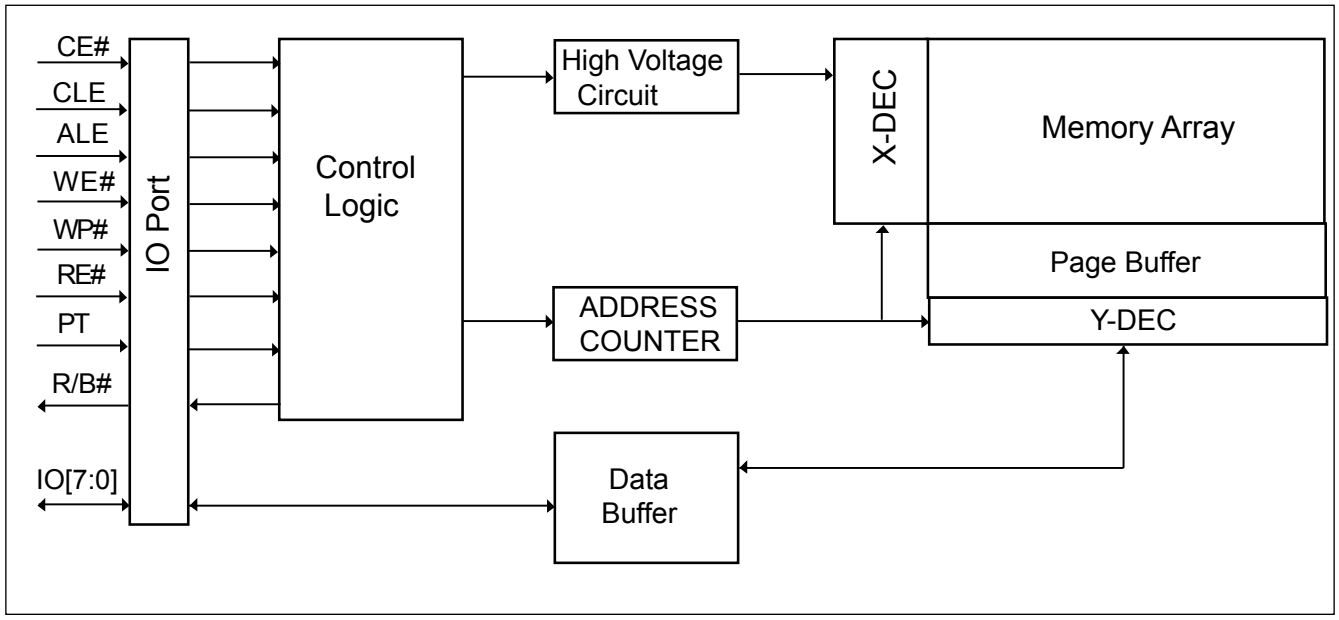
Please refer to **8-1. R/B#: Termination for The Ready/Busy# Pin (R/B#)** for details.

### PT: Protection

When the PT pin is high at power on, the whole chip is protected even the WP# is at high; the unprotection procedure (through BP bits setting) is necessary before any program/erase operation. When the PT pin is connected to low or floating, the function of block protection is disabled.


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# 4. BLOCK DIAGRAM





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# 5. SCHEMATIC CELL LAYOUT AND ADDRESS ASSIGNMENT

MX30LF1G18AC is composed by 64 pages of (2,048+64)-byte in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 64 bytes for ECC and other purposes. The device has an on-chip buffer of 2,112 bytes for data load and access. Each 2K-Byte page has the two area, one is the main area which is 2048-bytes and the other is spare area which is 64-byte.

There are four address cycles for the address allocation, please refer to the table below.

**Table 1. Address Allocation**

| Addresses | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |
|---|---|---|---|---|---|---|---|---|
| **Column address - 1st cycle** | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| **Column address - 2nd cycle** | L | L | L | L | A11 | A10 | A9 | A8 |
| **Row address - 3rd cycle** | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 |
| **Row address - 4th cycle** | A27 | A26 | A25 | A24 | A23 | A22 | A21 | A20 |


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# 6. DEVICE OPERATIONS

## 6-1. Address Input/Command Input/Data Input

Address input bus operation is for address input to select the memory address. The command input bus operation is for giving command to the memory. The data input bus is for data input to the memory device.

**Figure 2. AC Waveforms for Command / Address / Data Latch Timing**

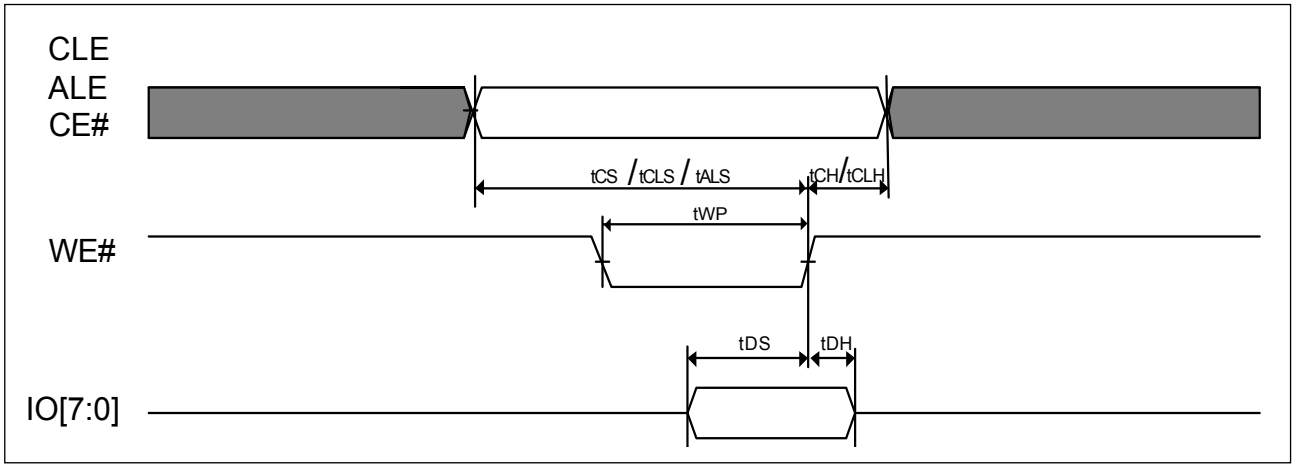
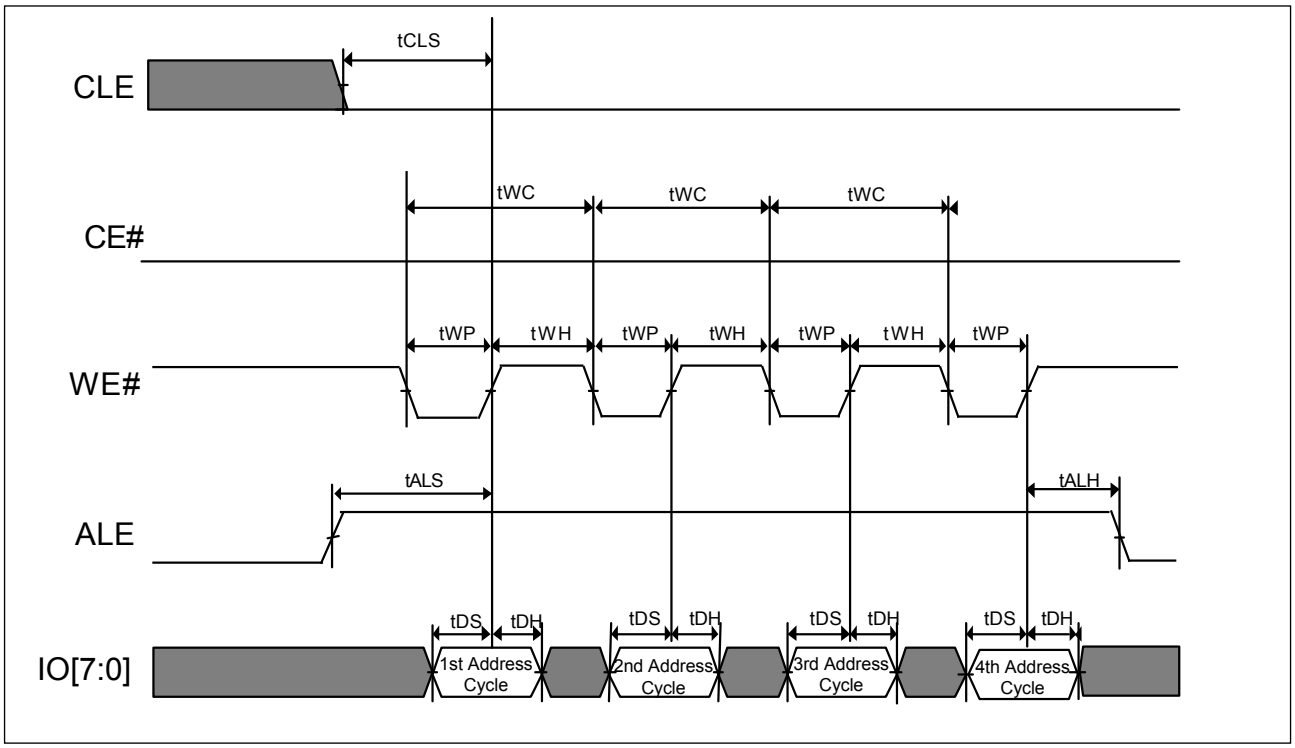



**Figure 3. AC Waveforms for Address Input Cycle**





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**Figure 4. AC Waveforms for Command Input Cycle**

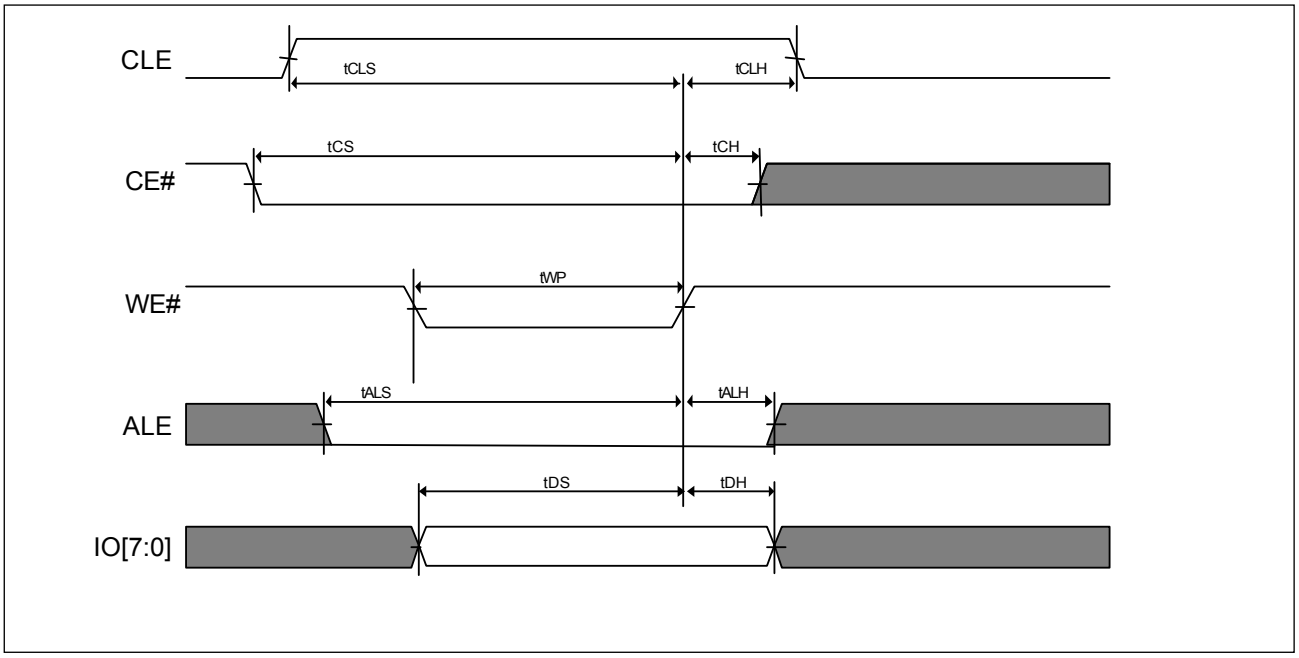
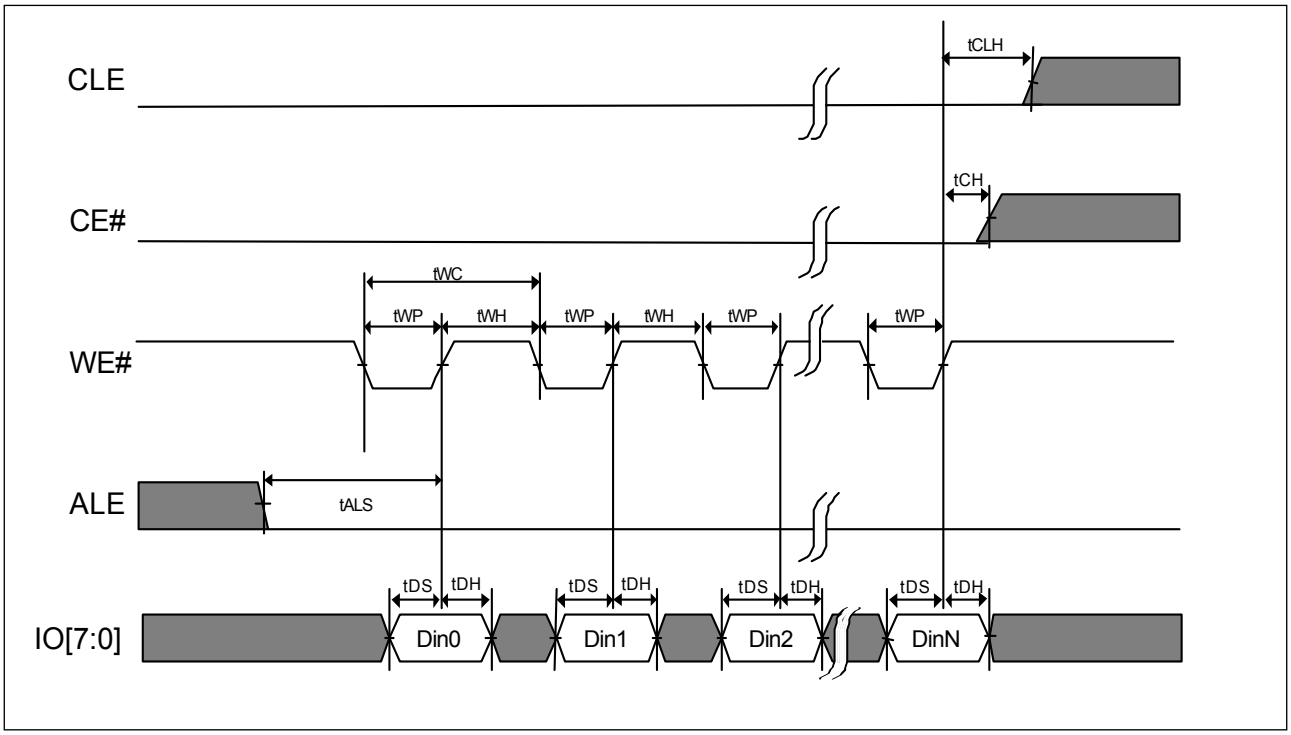



**Figure 5. AC Waveforms for Data Input Cycle**





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## 6-2. Page Read

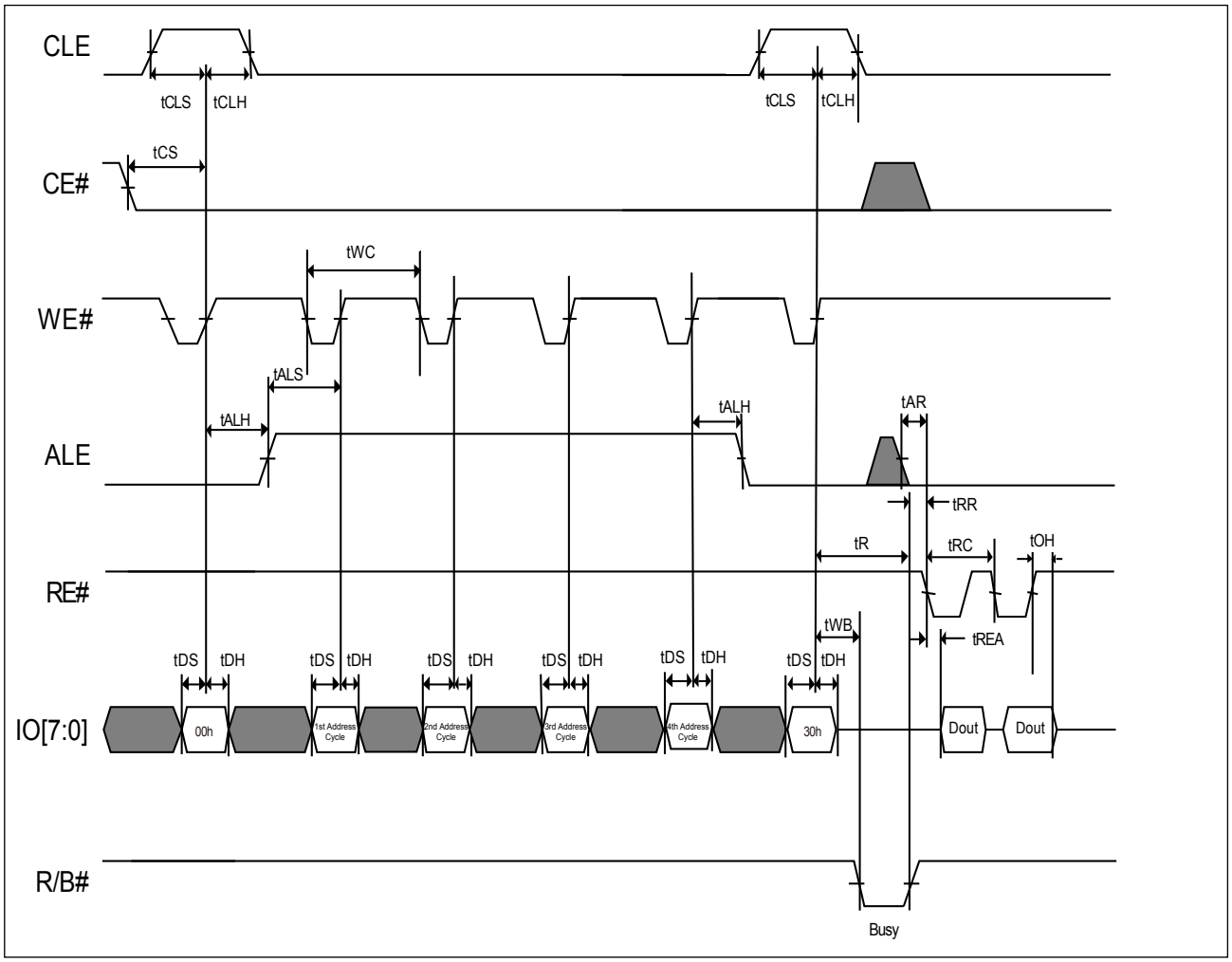
The MX30LF1G18AC array is accessed in Page of 2,112 bytes. External reads begins after the R/B# pin goes to READY.

The Read operation may also be initiated by writing the 00h command and giving the address (column and row address) and being confirmed by the 30h command, the MX30LF1G18AC begins the internal read operation and the chip enters busy state. The data can be read out in sequence after the chip is ready. Refer to **Figure 6. AC Waveforms for Read Cycle**.

If the host side uses a sequential access time (tRC) of less than 30ns, the data can be latched on the next falling edge of RE# as the waveform of EDO mode (**Figure 9-2. AC Waveforms for Sequential Data Out Cycle (After Read) - EDO Mode**).

To access the data in the same page randomly, a command of 05h may be written and only column address following and then confirmed by E0h command.

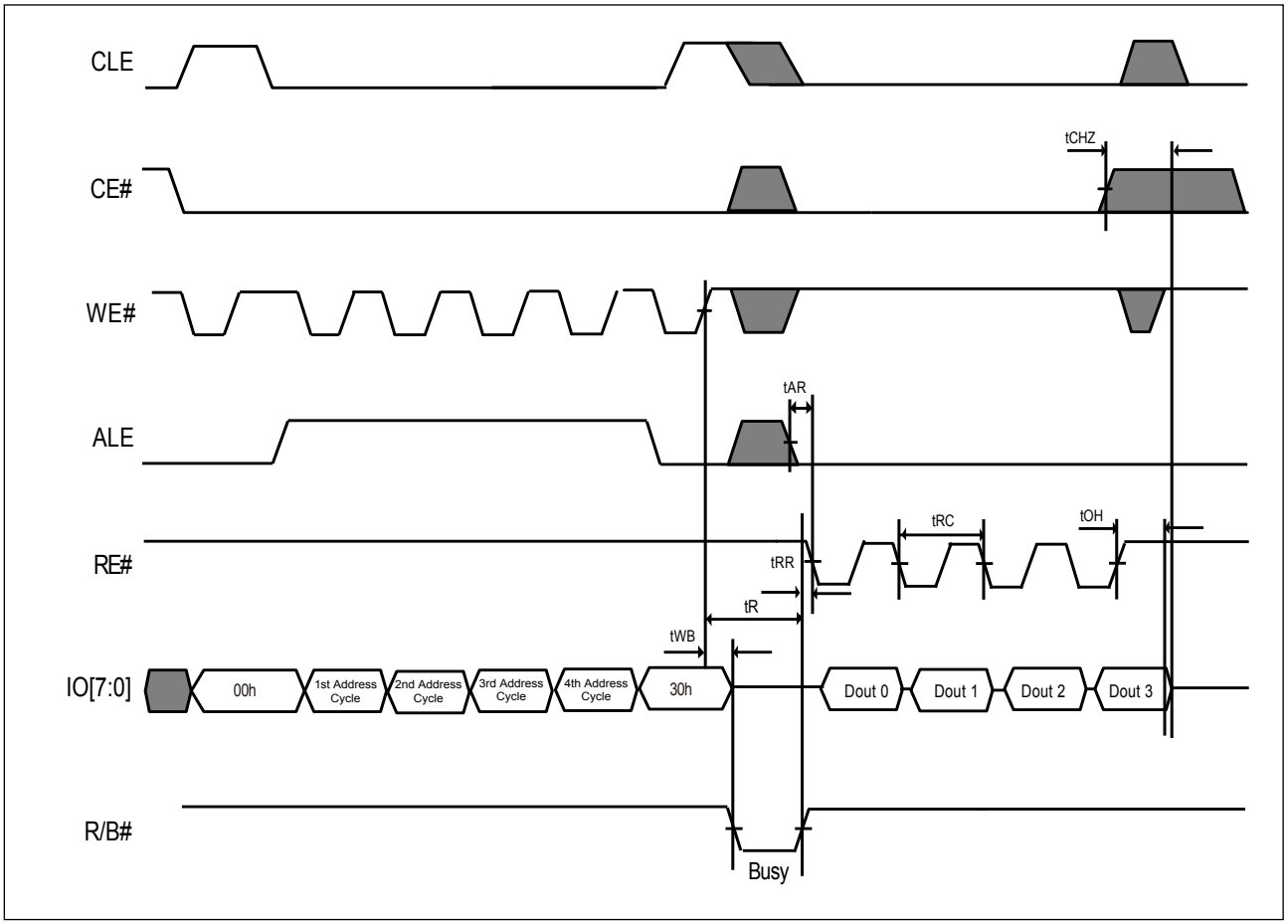
**Figure 6. AC Waveforms for Read Cycle**





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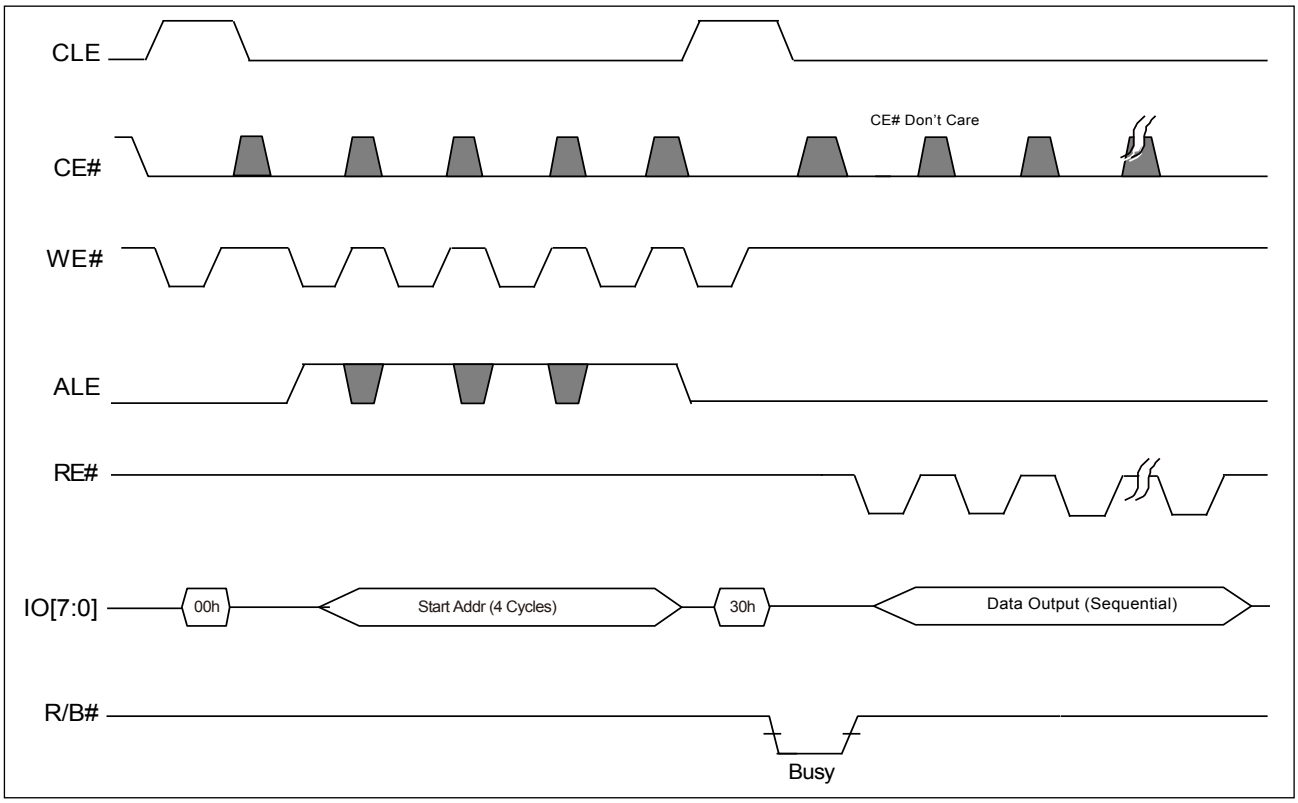
**Figure 7. AC Waveforms for Read Operation (Intercepted by CE#)**





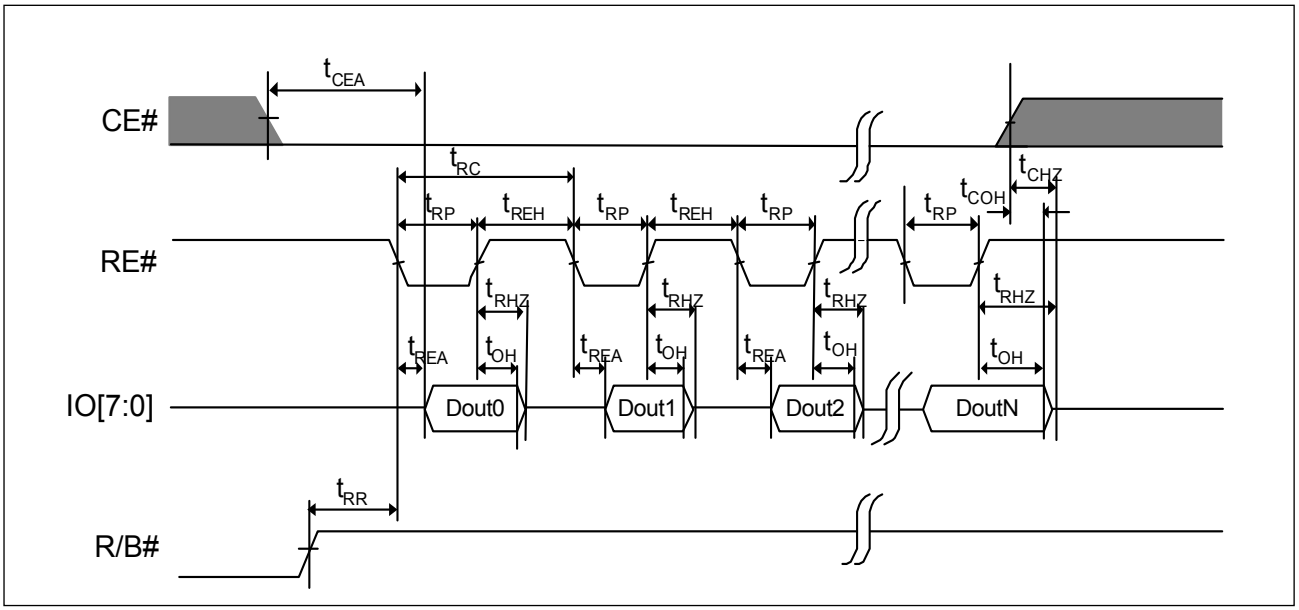
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**Figure 8. AC Waveforms for Read Operation (with CE# Don't Care)**




***Note:*** *The CE# "Don't Care" feature may simplify the system interface, which allows controller to directly download the code from flash device, and the CE# transitions will not stop the read operation during the latency time.*

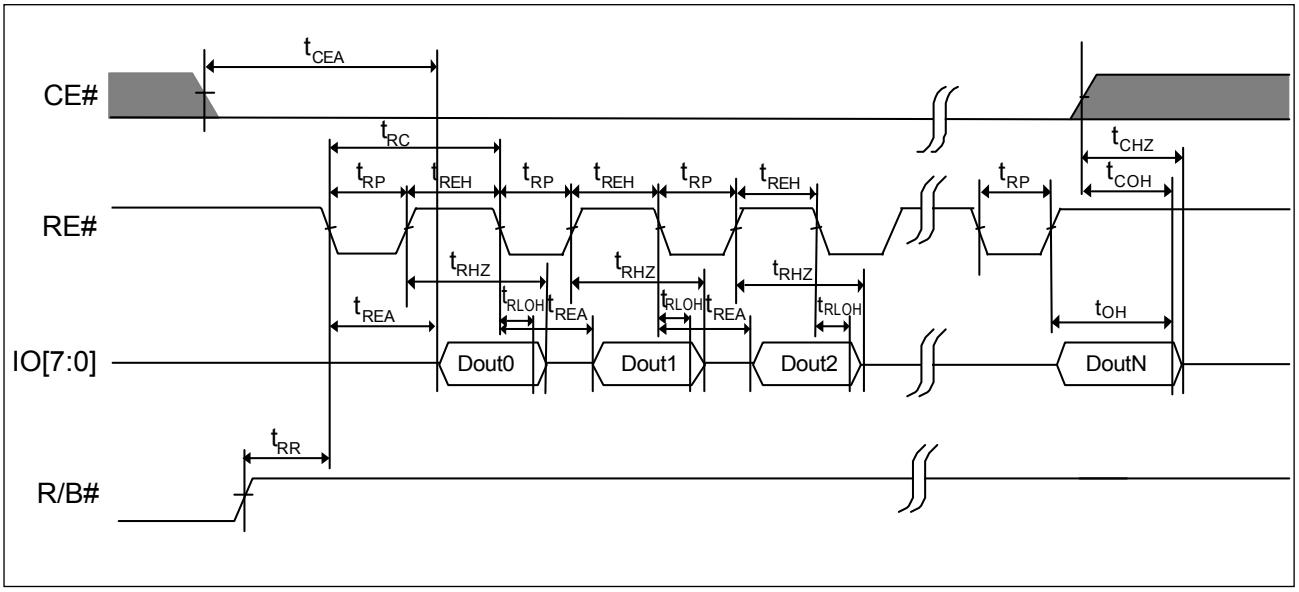
**Figure 9-1. AC Waveforms for Sequential Data Out Cycle (After Read)**





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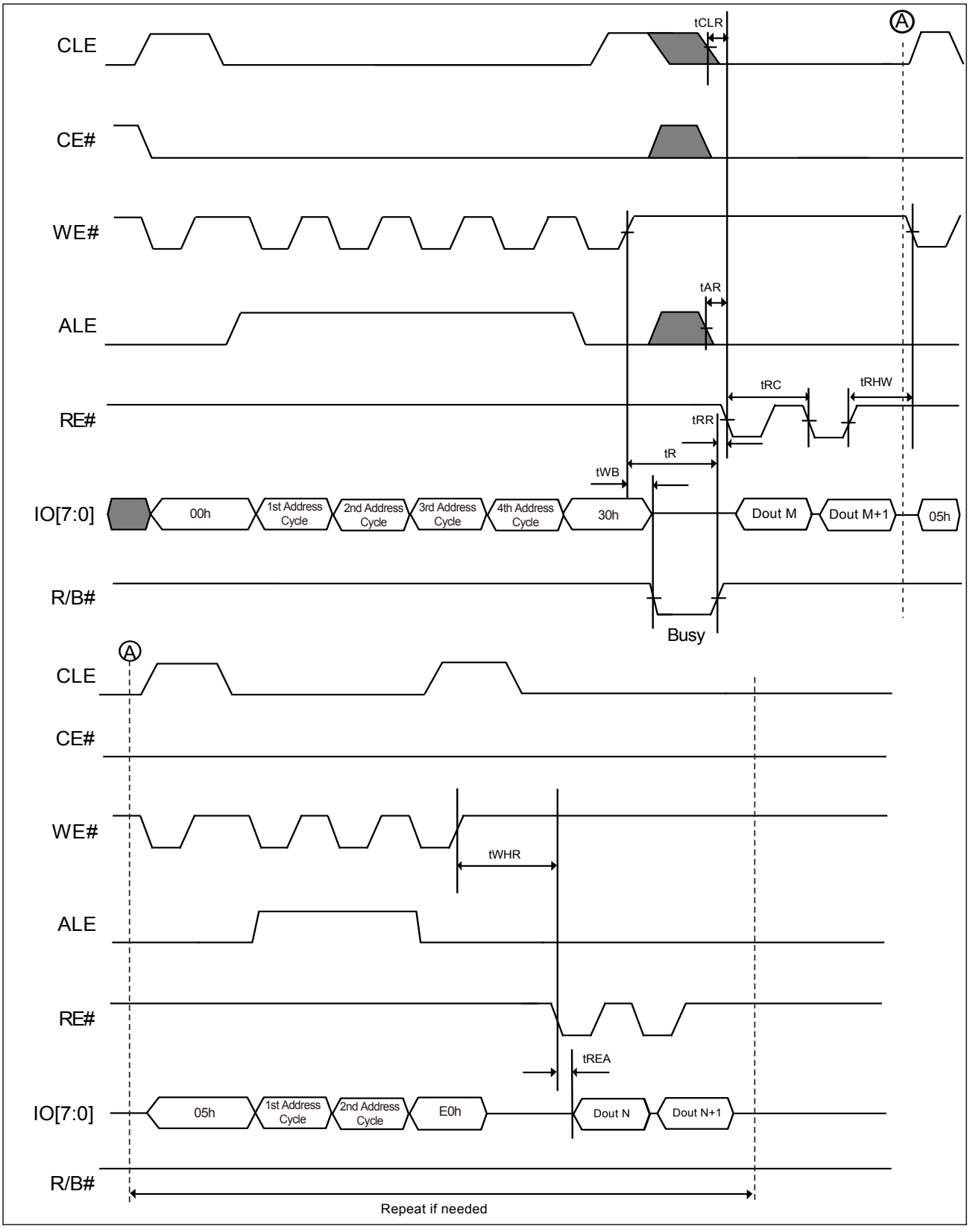
**Figure 9-2. AC Waveforms for Sequential Data Out Cycle (After Read) - EDO Mode**





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**Figure 10. AC Waveforms for Random Data Output**





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## 6-3. Cache Read Sequential

The cache read sequential operation is for throughput enhancement by using the internal cache buffer. It allows the consecutive pages to be read-out without giving next page address, which reduces the latency time from tR to tRCBSY between pages or blocks. While the data is read out on one page, the data of next page can be read into the cache buffer.

After writing the 00h command, the column and row address should be given for the start page selection, and followed by the 30h command for address confirmation. After that, the CACHE READ operation starts after a latency time tR and following a 31h command with the latency time of tRCBSY, the data can be read-out sequentially from 1$^{st}$ column address (A[11:0]=000h) without giving next page address input. The 31h command is necessary to confirm the next cache read sequential operation and followed by a tRCBSY latency time before next page data is necessary. The CACHE READ SEQUENTIAL command is also valid for the consecutive page cross block.

The random data out (05h-E0h) command set is available to change the column address of the current page data in the cache register.

The user can check the chip status by the following method:

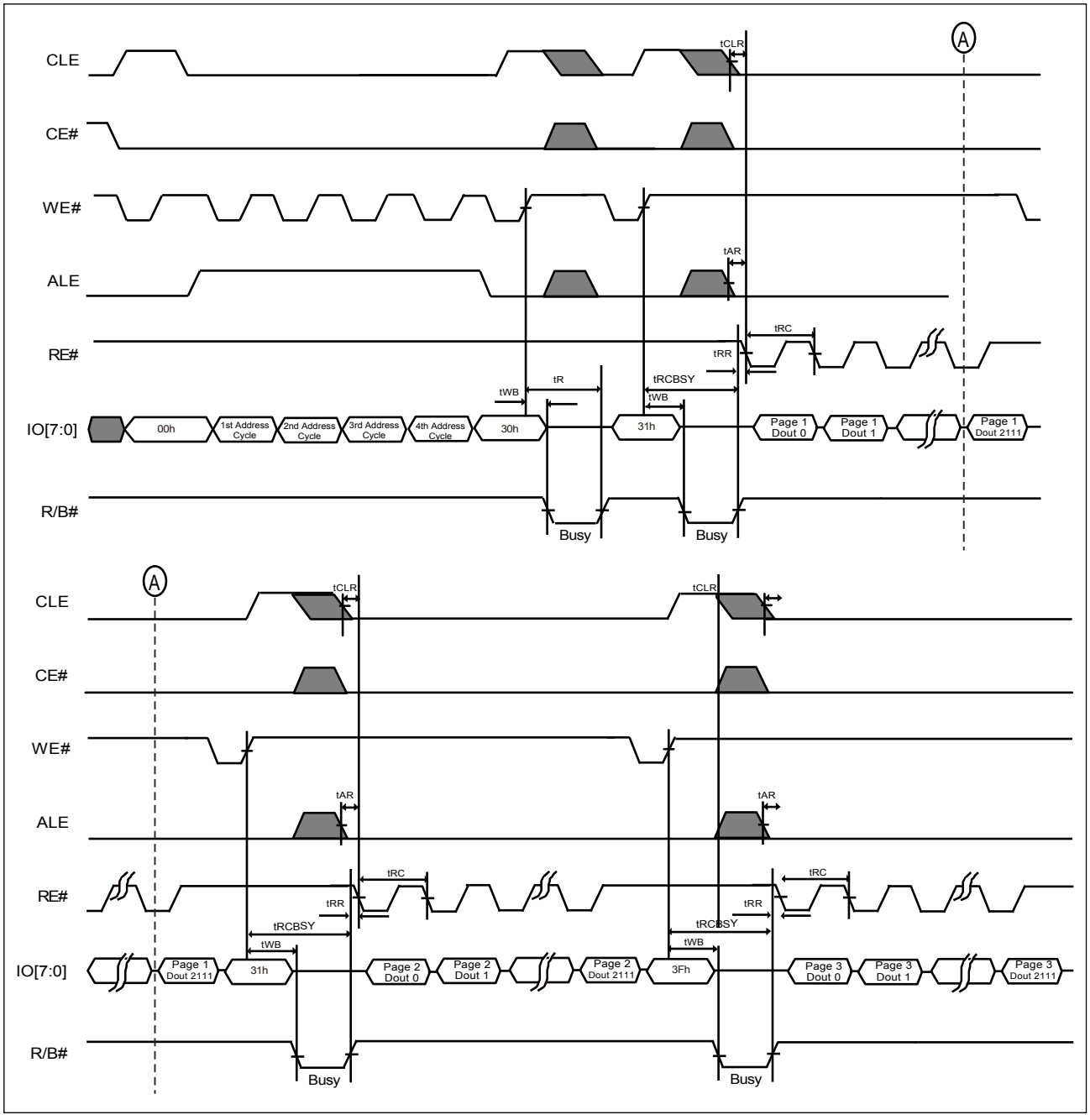
- R/B# pin ("0" means the data is not ready, "1" means the user can read the data)

- Status Register (SR[6] functions the same as R/B# pin, SR[5] indicates the internal chip operation, "0" means the chip is in internal operation and "1" means the chip is idle.) Status Register can be checked after the Read Status command (70h) is issued. Command 00h should be given to return to the cache read sequential operation.

To confirm the last page to be read-out during the cache read sequential operation, a 3Fh command is needed to replace the 31h command prior to the last data-out.


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**Figure 11-1. AC Waveforms for Cache Read Sequential**





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## 6-4. Cache Read Random

The main difference from the Cache Read Sequential operation is the Cache Read Random operation may allow the random page to be read-out with cache operation not just for the consecutive page only.

After writing the 00h command, the column and row address should be given for the start page selection, and followed by the 30h command for address confirmation. The column address is ignored in the cache read random operation. And then, the CACHE READ RANDOM operation starts after a latency time tR and following a 00h command with the selected page address and following a 31h command, the data can be read-out sequentially from the 1st column address (A[11:0] =000h) after the latency time of tRCBSY. After the previous selected page data out, a new selected page address can be given by writing the 00h-31h command set again. The CACHE READ RANDOM command is also valid for the consecutive page cross block.

The random data out (05h-E0h) command set is available to change the column address of the current page data in the cache register.

The user can check the chip status by the following method:

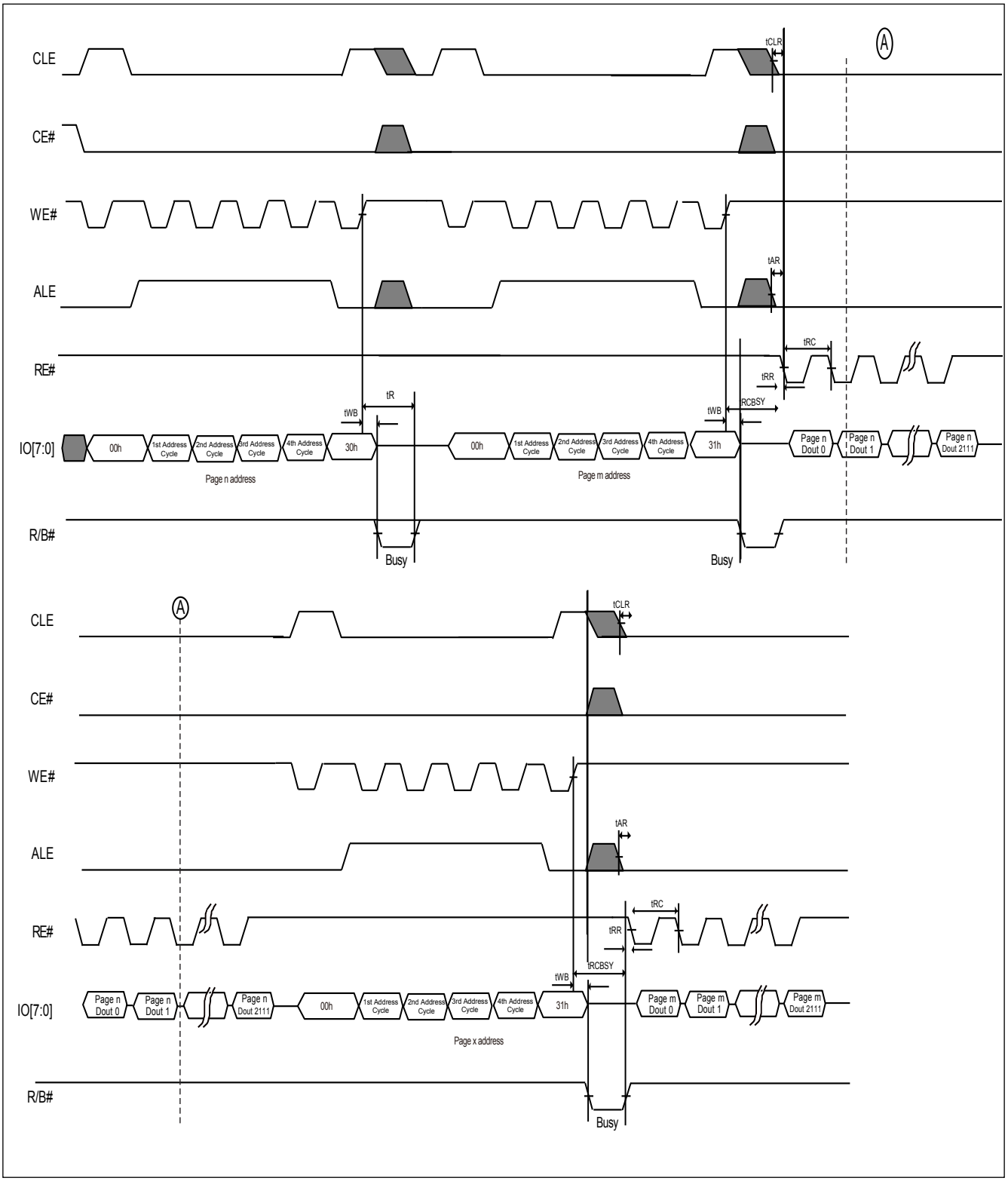
- R/B# pin ("0" means the data is not ready, "1" means the user can read the data)

- Status Register can be checked after the Read Status command (70h) is issued. (SR[6] behaves the same as R/B# pin, SR[5] indicates the internal chip operation, "0" means the chip is in internal operation and "1" means the chip is idle.) Command 00h should be given to return to the cache read operation.

To confirm the last page to be read-out during the cache read operation, a 3Fh command is needed to replace the 31h command prior to the last data-out.


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**Figure 11-2. AC Waveforms for Cache Read Random**





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## 6-5. Page Program

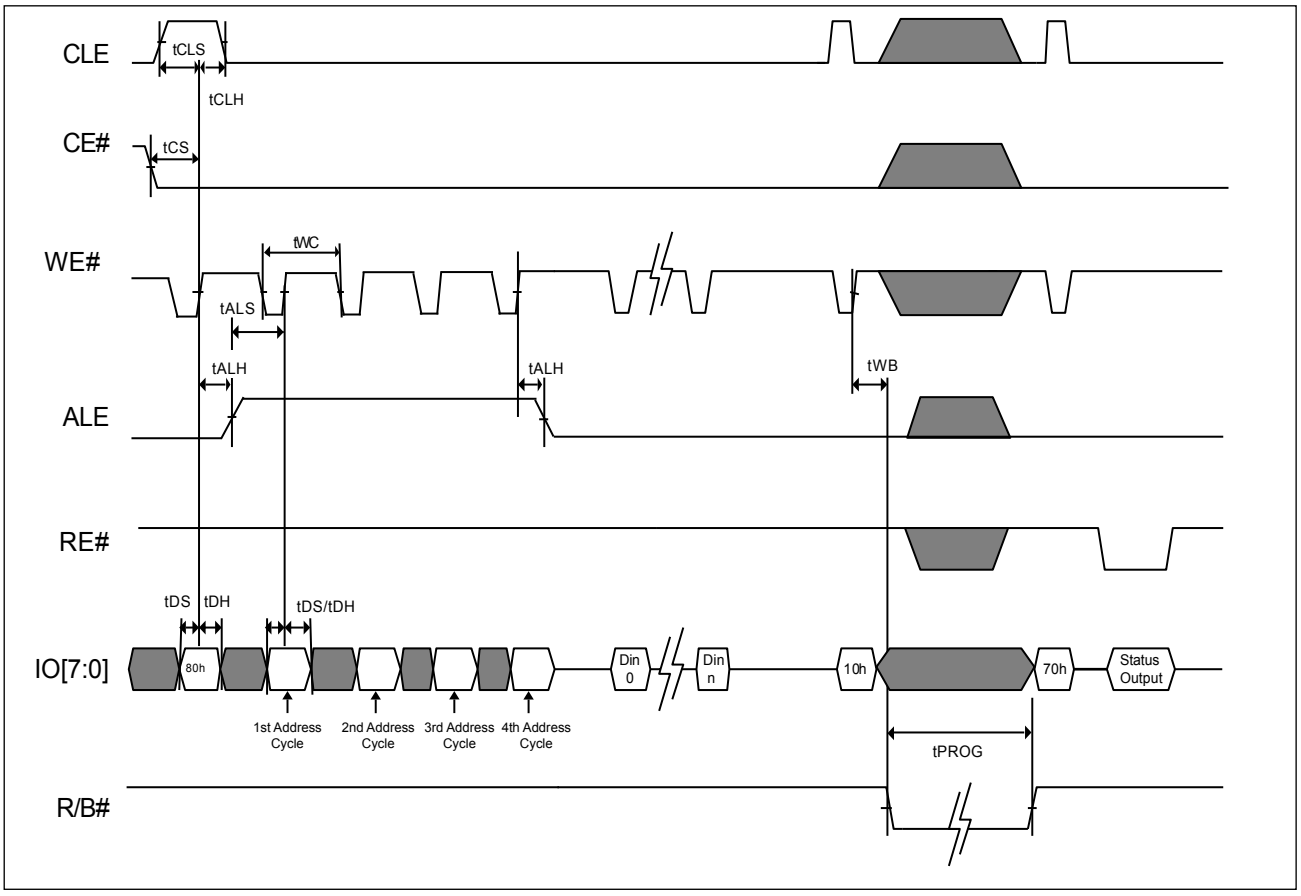
The memory is programmed by page, which is 2,112 bytes. After Program load command (80h) is issued and the row and column address is given, the data will be loaded into the chip sequentially. Random Data Input command (85h) allows multi-data load in non-sequential address. After data load is complete, program confirm command (10h) is issued to start the page program operation. The page program operation in a block should start from the low address to high address. Partial program in a page is allowed up to 4 times. However, the random data input mode for programming a page is allowed and number of times is not limited.

The status of the program completion can be detected by R/B# pin or Status register bit SR[6].

The program result is shown in the chip status bit (SR[0]). SR[0] = 1 indicates the Page Program is not successful and SR[0] = 0 means the program operation is successful.

During the Page Program progressing, only the read status register command and reset command are accepted, others are ignored.

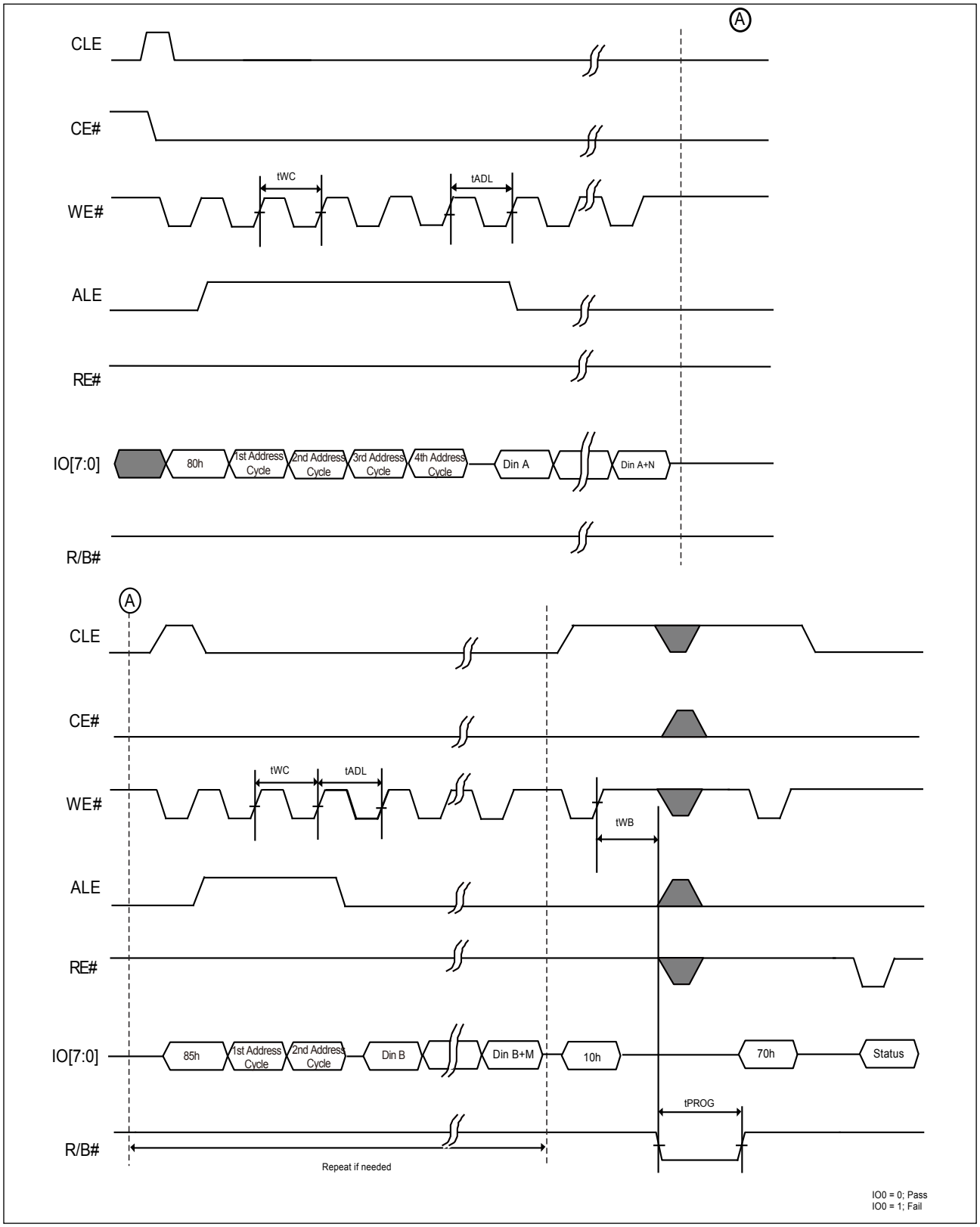
**Figure 12. AC Waveforms for Program Operation after Command 80H**





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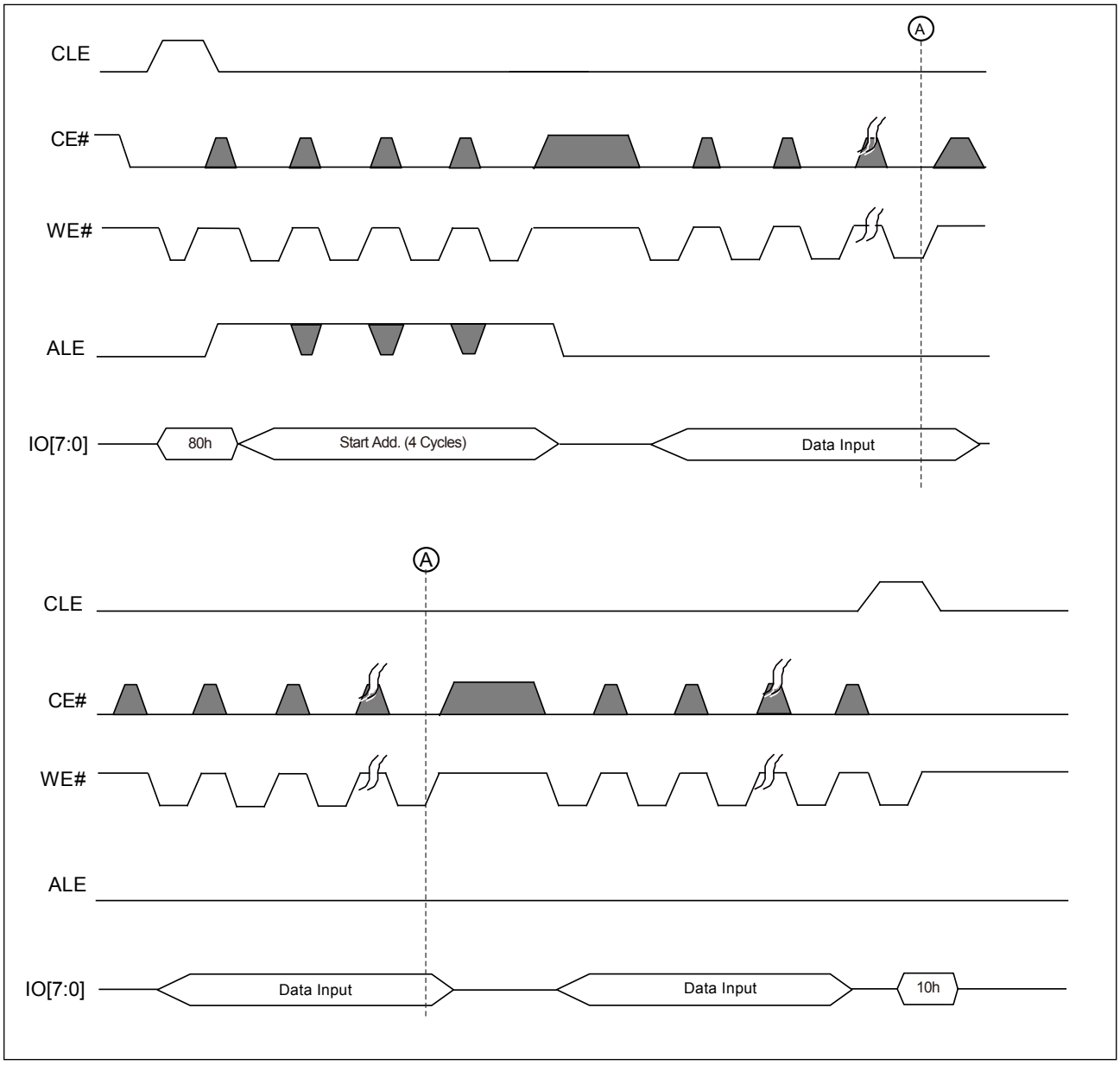
**Figure 13. AC Waveforms for Random Data In (For Page Program)**




***Note:*** *Random Data In is also supported in cache program.*


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**Figure 14. AC Waveforms for Program Operation with CE# Don't Care**




***Note:*** *The CE# "Don't Care" feature may simplify the system interface, which allows the controller to directly write data into flash device, and the CE# transitions will not stop the program operation during the latency time.*


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## 6-6. Cache Program

The cache program feature enhances the program performance by using the cache buffer of 2,112-byte. The serial data can be input to the cache buffer while the previous data stored in the buffer are programming into the memory cell. Cache Program command sequence is almost the same as page program command sequence. Only the Program Confirm command (10h) is replaced by cache Program command (15h).

After the Cache Program command (15h) is issued. The user can check the status by the following methods.

- R/B# pin

- Cache Status Bit (SR[6] = 0 indicates the cache is busy; SR[6] = 1 means the cache is ready).

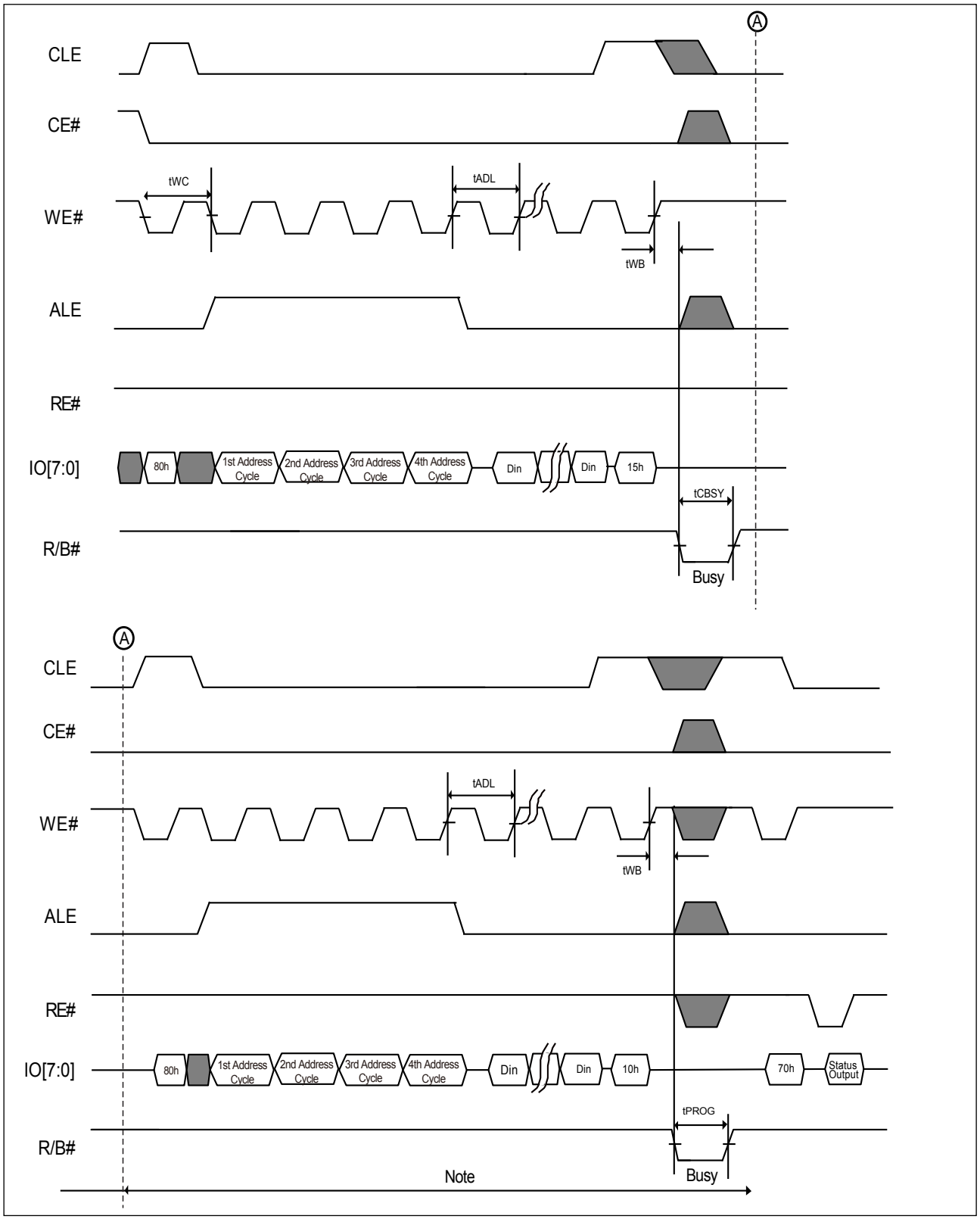
The user can issue another Cache Program Command Sequence after the Cache is ready. The user can always monitor the chip state by Ready/Busy Status Bit (SR[5]). The user can issues either program confirm command (10h) or cache program command (15h) for the last page if the user monitor the chip status by issuing Read Status Command (70h).

However, if the user only monitors the R/B# pin, the user needs to issue the program confirm command (10h) for the last page.

The user can check the Pass/Fail Status through P/F Status Bit (SR[0]) and Cache P/F Status Bit (SR[1]). SR[1] represents Pass/Fail Status of the previous page. SR[1] is updated when SR[6] change from 0 to 1 or Chip is ready. SR[0] shows the Pass/Fail status of the current page. It is updated when SR[5] change from "0" to "1" or the end of the internal programming.  For more details, please refer to the related waveforms.


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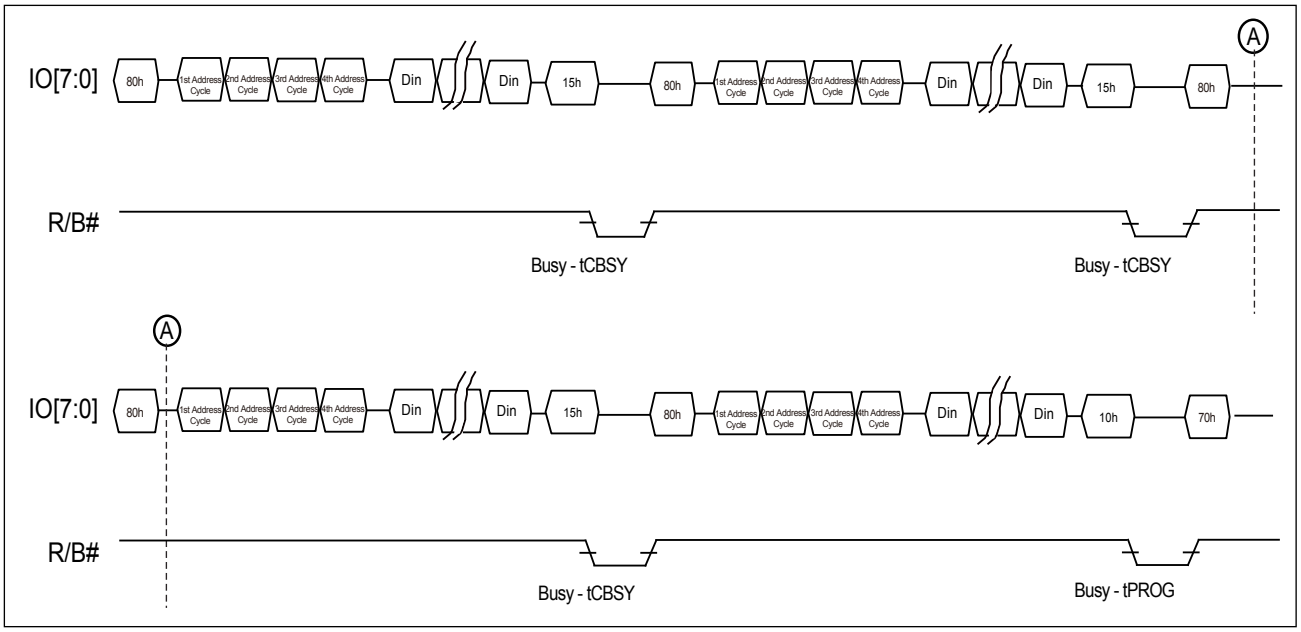
**Figure 15-1. AC Waveforms for Cache Program**




***Note:*** *It indicates the last page Input & Program.*


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**Figure 15-2. AC Waveforms for Sequence of Cache Program**




***Note:*** *tPROG = Page$_{(Last)}$ programming time + Page $_{(Last-1)}$ programming time - Input cycle time of command & address - Data loading time of page $_{(Last)}$.*


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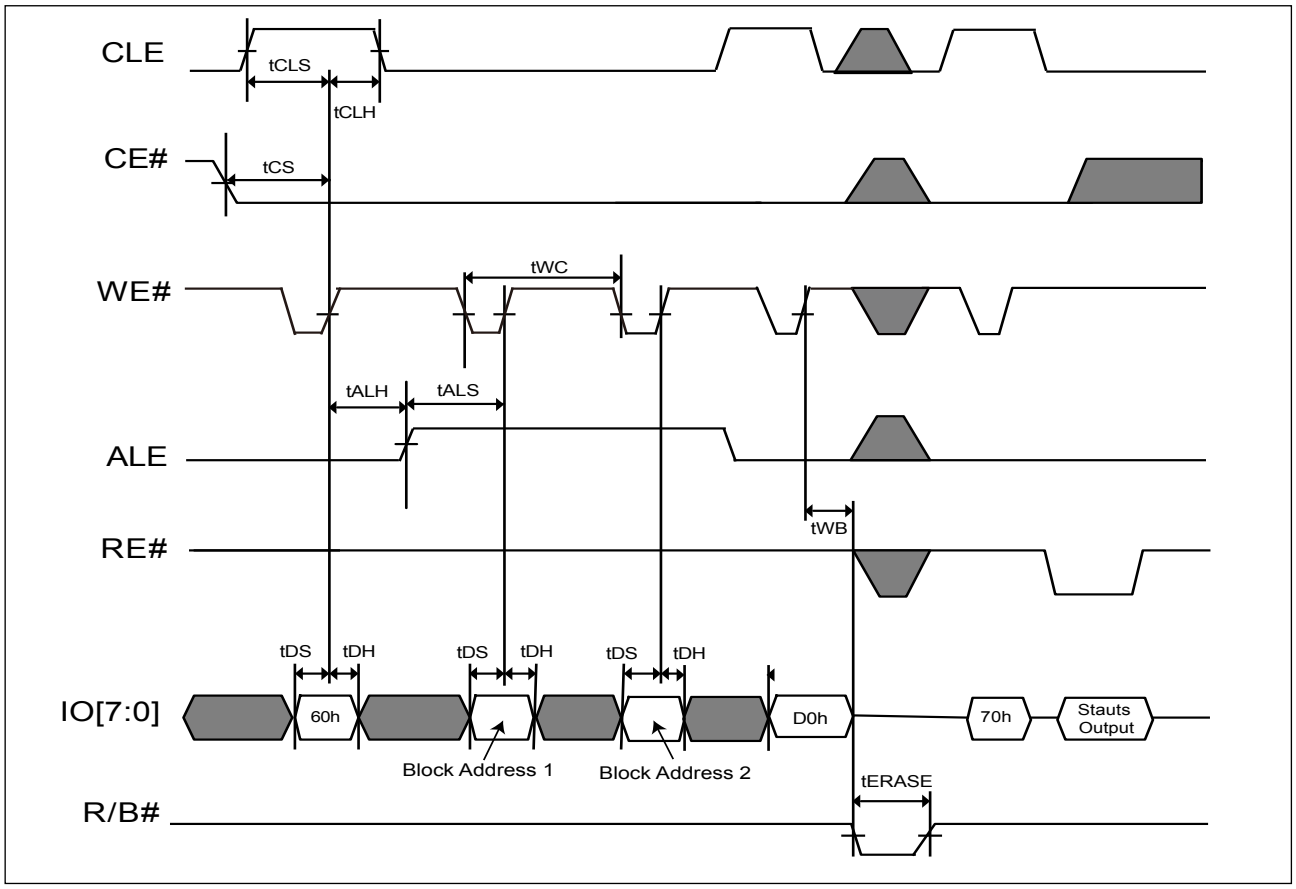
## 6-7. Block Erase

The MX30LF1G18AC supports a block erase command. This command will erase a block of 64 pages associated with the most significant address bits.

The completion of the erase operation can be detected by R/B# pin or Status register bit (IO6). Recommend to check the status register bit IO0 after the erase operation completes.

During the erasing process, only the read status register command and reset command can be accepted, others are ignored.

**Figure 16. AC Waveforms for Erase Operation**





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## 6-8. ID Read

The device contains ID codes that identify the device type and the manufacturer. The ID READ command sequence includes one command Byte (90h), one address byte (00h). The Read ID command 90h may provide the manufacturer ID (C2h) of one-byte and device ID (F1h) of one-byte, also Byte2, Byte3, and Byte4 ID code are followed.

The device support ONFI Parameter Page Read, by sending the ID Read (90h) command and following one byte address (20h), the four-byte data returns the value of 4Fh-4Eh-46h-49h for the ASCII code of "O"-"N"-"F"-"I" to identify the ONFI parameter page.

**Table 2. ID Codes Read Out by ID Read Command 90H**

| ID Codes | 1Gb, x8, 3V |
|---|---|
| **Byte0-Manufacturer** | C2h |
| **Byte1: Device ID** | F1h |
| **Byte2** | 80h |
| **Byte3** | 95h |
| **Byte4** | 02h |

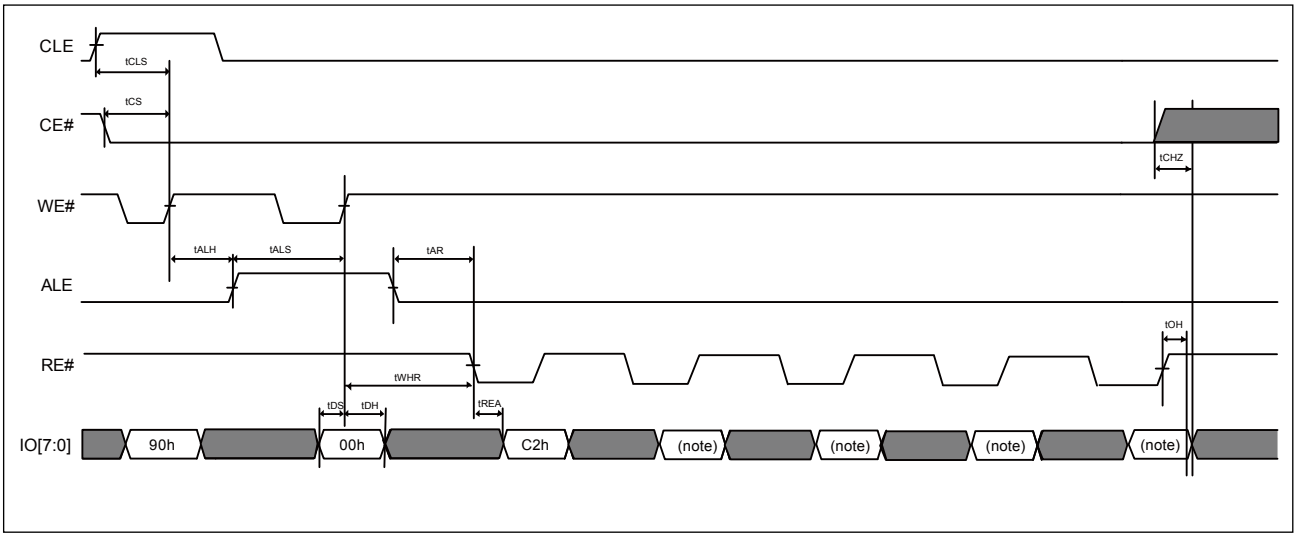

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**Table 3. The Definition of Byte2-Byte4 of ID Table**

| Terms | Description | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |
|---|---|---|---|---|---|---|---|---|---|
| **Byte 2** | | | | | | | | | |
| **Die Number** | 1 | | | | | | | 0 | 0 |
| | 2 | | | | | | | 0 | 1 |
| **Cell Structure** | SLC | | | | | 0 | 0 | | |
| **# of Concurrently Programmed page** | 1 | | | 0 | 0 | | | | |
| | 2 | | | 0 | 1 | | | | |
| **Interleaved operations between Multiple die** | Not supported | | 0 | | | | | | |
| **Cache Program** | Supported | 1 | | | | | | | |
| **Byte 3** | | | | | | | | | |
| **Page size (Exclude spare)** | 2KB | | | | | | | 0 | 1 |
| **Spare area size (Per 512B)** | 16B | | | | | | 1 | | |
| **Block size (Exclude spare)** | 128KB | | | 0 | 1 | | | | |
| **Organization** | x8 | | 0 | | | | | | |
| **Sequential Read Cycle Time** | 25ns | 0 | | | | 0 | | | |
| | 20ns | 1 | | | | 0 | | | |
| **Byte 4** | | | | | | | | | |
| **ECC level requirement** | 4-bit ECC/528B | | | | | | | 1 | 0 |
| **#Plane per CE** | 1 | | | | | 0 | 0 | | |
| | 2 | | | | | 0 | 1 | | |
| | 4 | | | | | 1 | 0 | | |
| **Plane size** | 1Gb | | 0 | 0 | 0 | | | | |
| | 2Gb | | 1 | 0 | 1 | | | | |
| **Reserved** | | 0 | | | | | | | |

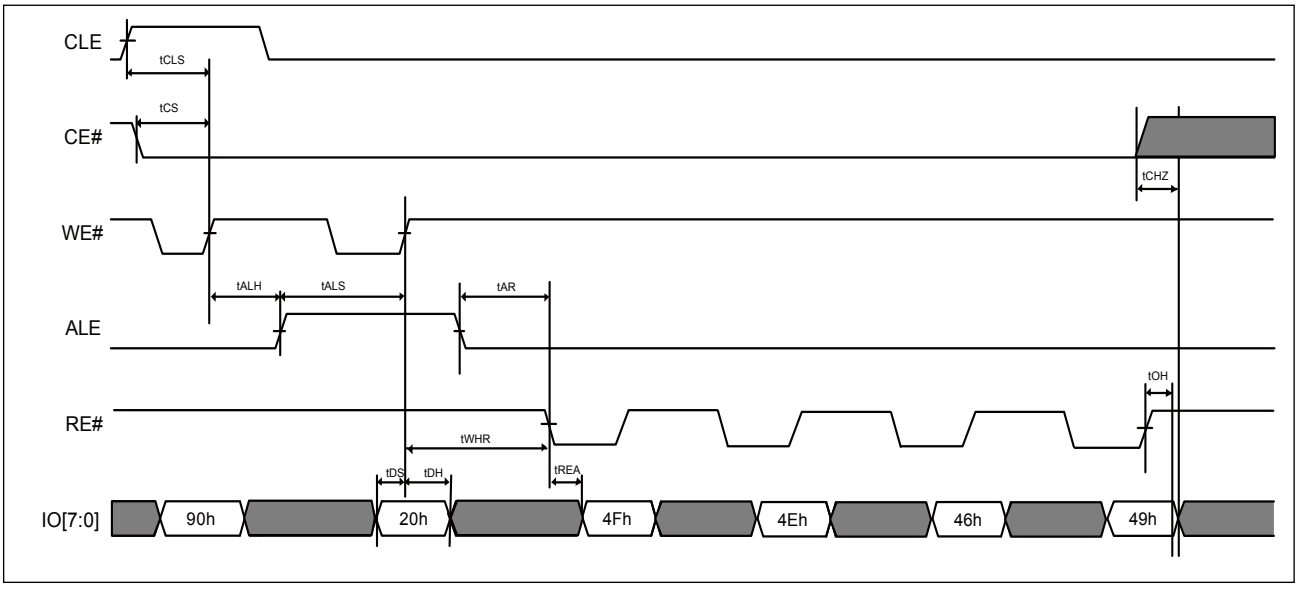

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**Figure 17-1. AC Waveforms for ID Read Operation**




***Note***: *See also* ***Table 2. ID Codes Read Out by ID Read Command 90H***.

**Figure 17-2. AC Waveforms for ID Read (ONFI Identifier) Operation**





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## 6-9. Status Read

The MX30LF1G18AC provides a status register that outputs the device status by writing a command code 70h, and then the IO pins output the status at the falling edge of CE# or RE# which occurs last. Even though when multiple flash devices are connecting in system and the R/B#pins are common-wired, the two lines of CE# and RE# may be checked for individual devices status separately.

The status read command 70h will keep the device at the status read mode unless next valid command is issued. The resulting information is outlined in **Table 4** as below.

**Table 4. Status Output**

| Pin | Status | Related Mode | Value | |
|---|---|---|---|---|
| **SR[0]** | Chip Status | Page Program, Cache Program (Page N), Block Erase | 0: Passed | 1: Failed |
| **SR[1]** | Cache Program Result | Cache Program (Page N-1) | 0: Passed | 1: Failed |
| **SR[2-4]** | Not Used | | | |
| **SR[5]** | Ready / Busy (For P/E/R Controller) | Cache Program/Cache Read operation, other Page Program/Block Erase/Read are same as IO6 **(Note 1)** | 0: Busy | 1: Ready |
| **SR[6]** | Ready / Busy | Page Program, Block Erase, Cache Program, Read, Cache Read **(Note 2)** | 0: Busy | 1: Ready |
| **SR[7]** | Write Protect | Page Program, Block Erase, Cache Program, Read | 0: Protected | 1: Unprotected |

***Notes:***

1. *During the actual programming operation, the SR[5] is "0" value; however, when the internal operation is completed during the cache mode, the SR[5] returns to "1".*
2. *The SR[6] returns to "1" when the internal cache is available to receive new data. The SR[6] value is consistent with the R/B#.*


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The following is an example of a HEX data bit assignment:

**Figure 18. Bit Assignment (HEX Data)**

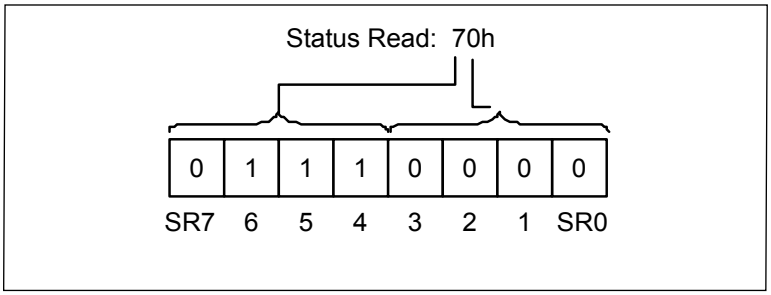
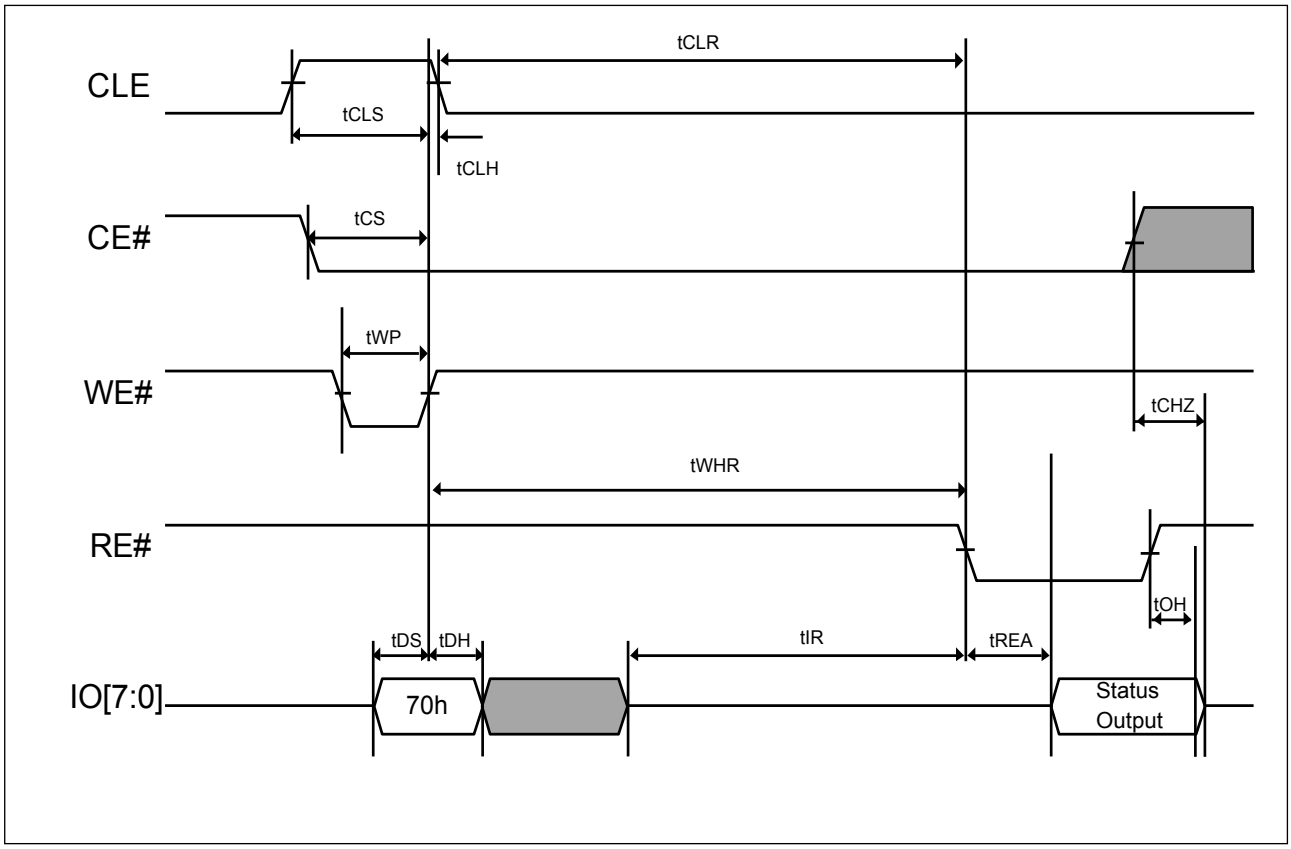



**Figure 19. AC Waveforms for Status Read Operation**





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## 6-10. Block Protection Status Read

The Block Protection Status Read command (7Ah) may check the protect/un-protect status of blocks. The status output is shown in **Table 5. Block Protection Status Output** and the address cycle is referred to **Table 6. Address Cycle Definition of Block**.

### Table 5. Block-Protection Status Output

| Block-Protection Status | IO[7:3] | IO2(PT#) | IO1(SP#) | IO0(SP) |
|---|---|---|---|---|
| Block is protected, and device is solid-protected | x | 0 | 0 | 1 |
| Block is protected, and device is not solid-protected | x | 0 | 1 | 0 |
| Block is un-protected, and device is solid-protected | x | 1 | 0 | 1 |
| Block is un-protected, and device is not solid-protected | x | 1 | 1 | 0 |

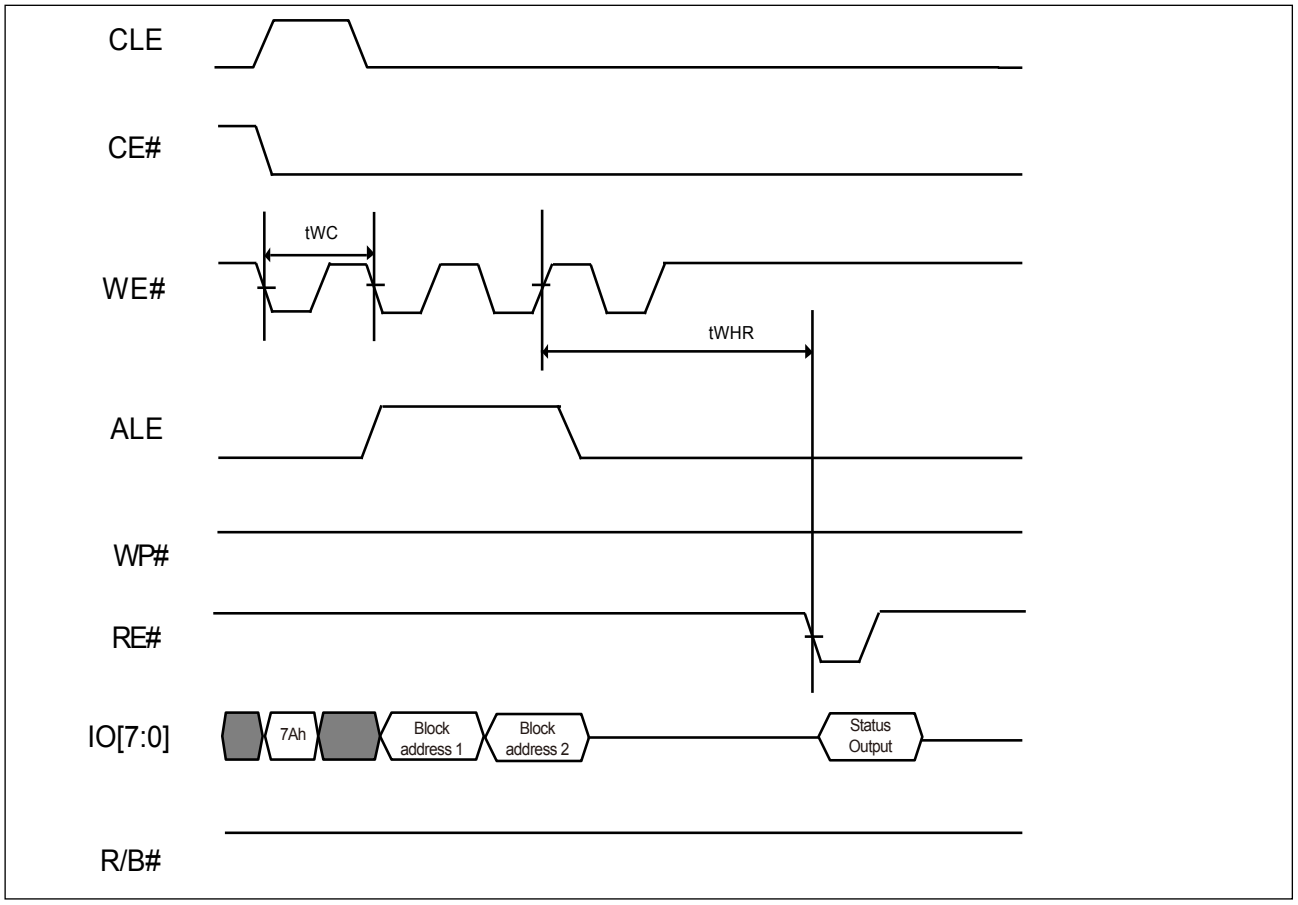
***Note:*** *SP stands for Solid-protected. Once the SP bit sets as 1, the rest of the protection bits (BPx bits, Invert bit, Complementary bit) cannot be changed during the current power cycle.*

### Table 6. Address Cycle Definition of Block

| Address Cycle | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |
|---|---|---|---|---|---|---|---|---|
| **Block Address 1** | A19 | A18 | L | L | L | L | L | L |
| **Block Address 2** | A27 | A26 | A25 | A24 | A23 | A22 | A21 | A20 |


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**Figure 20. AC Waveforms for Block Protection Status Read**





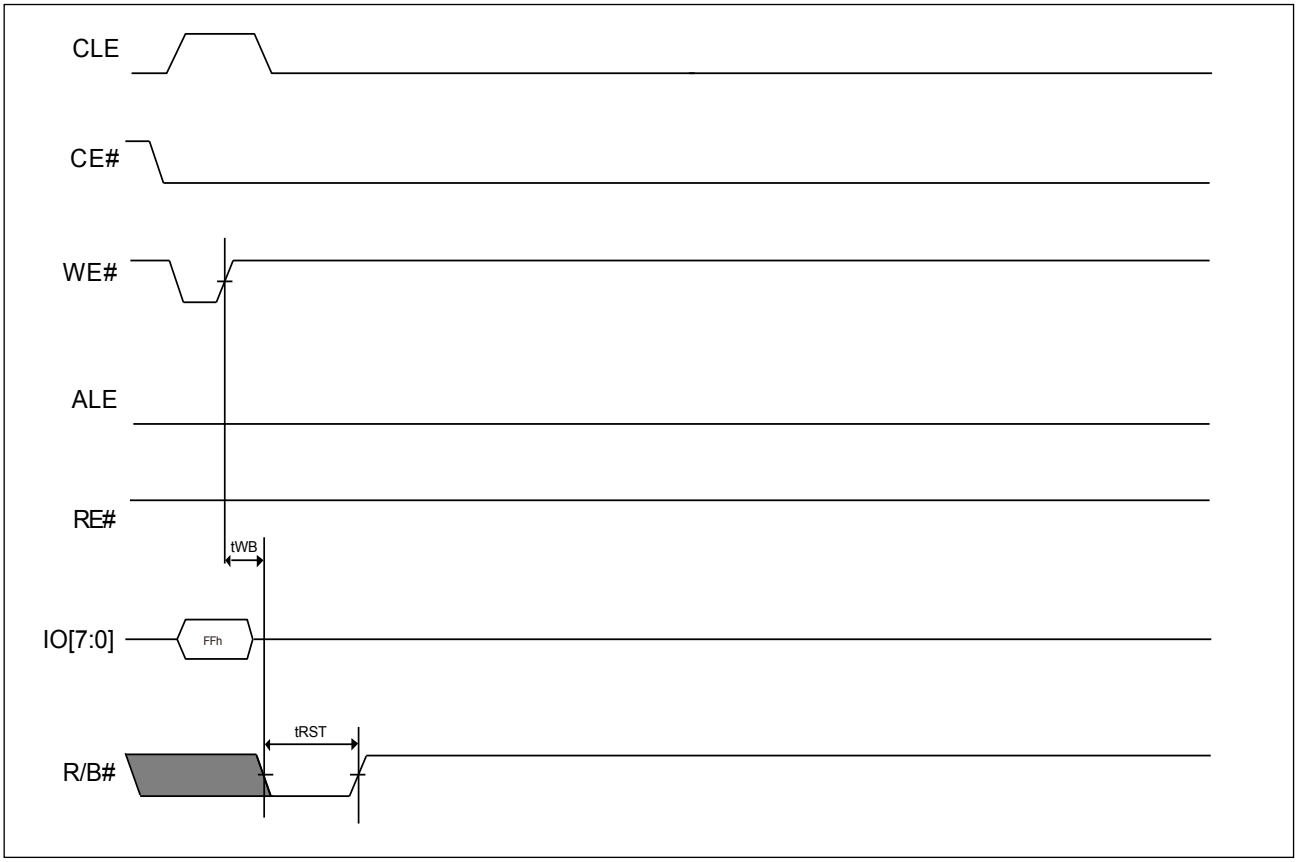
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## 6-11. Reset

The reset command FFh resets the read/program/erase operation and clear the status register to be E0h (when WP# is high). The reset command during the program/erase operation will result in the content of the selected locations(perform programming/erasing) might be partially programmed/erased.

If the Flash memory has already been set to reset stage with reset command, the additional new reset command is invalid.

**Figure 21. AC waveforms for Reset Operation**





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## 6-12. Parameter Page Read (ONFI)

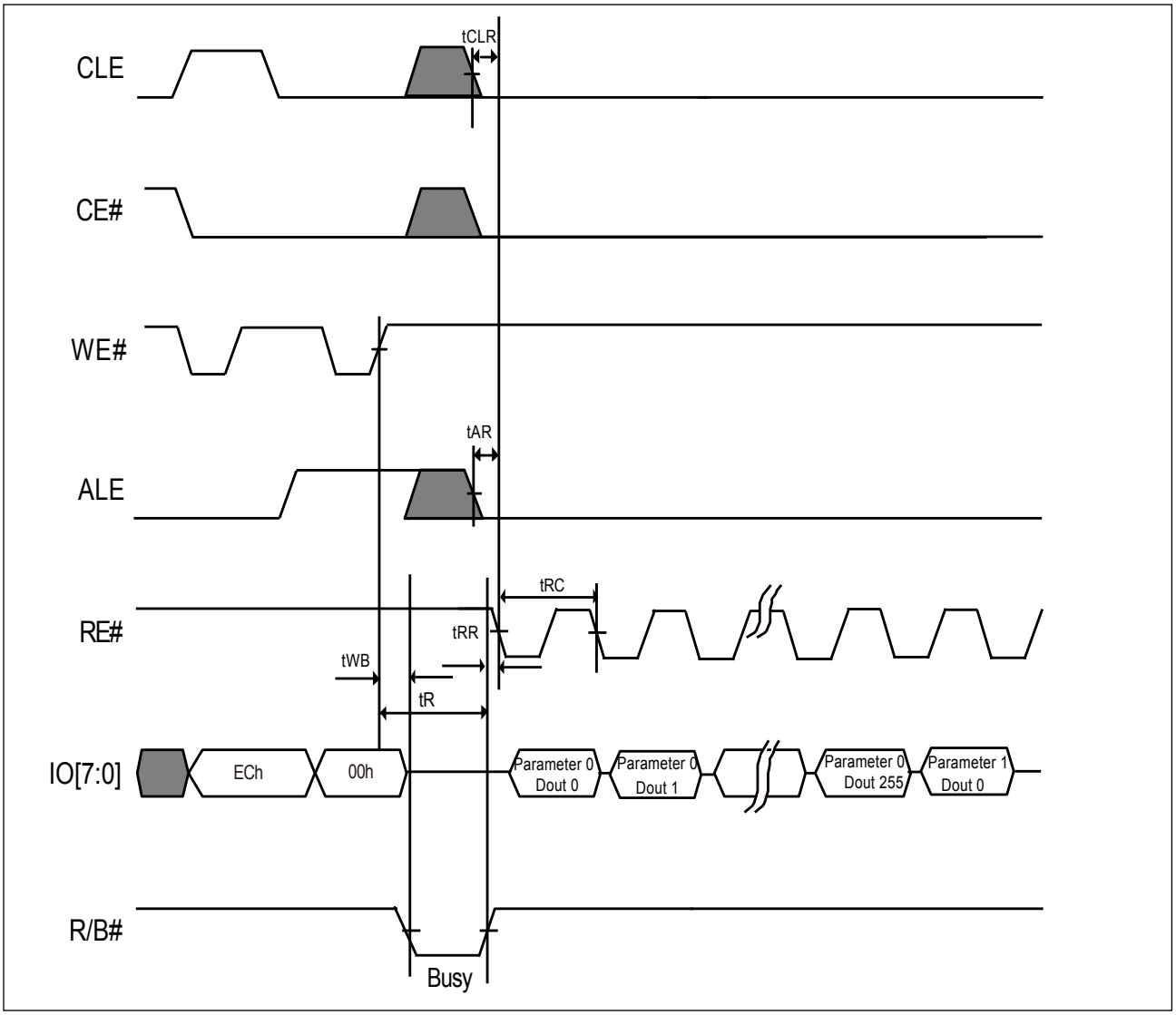
The NAND Flash device support ONFI Parameter Page Read and the parameter can be read out by sending the command of ECh and giving the address 00h. The NAND device information may refer to the table of parameter page(ONFI), there are three copies of 256-byte data and additional redundant parameter pages.

Once sending the ECh command, the NAND device will remain in the Parameter Page Read mode until next valid command is sent.

The Random Data Out command set (05h-E0h) can be used to change the parameter location for the specific parameter data random read out.

The Status Read command (70h) can be used to check the completion with a following read command (00h) to enable the data out.

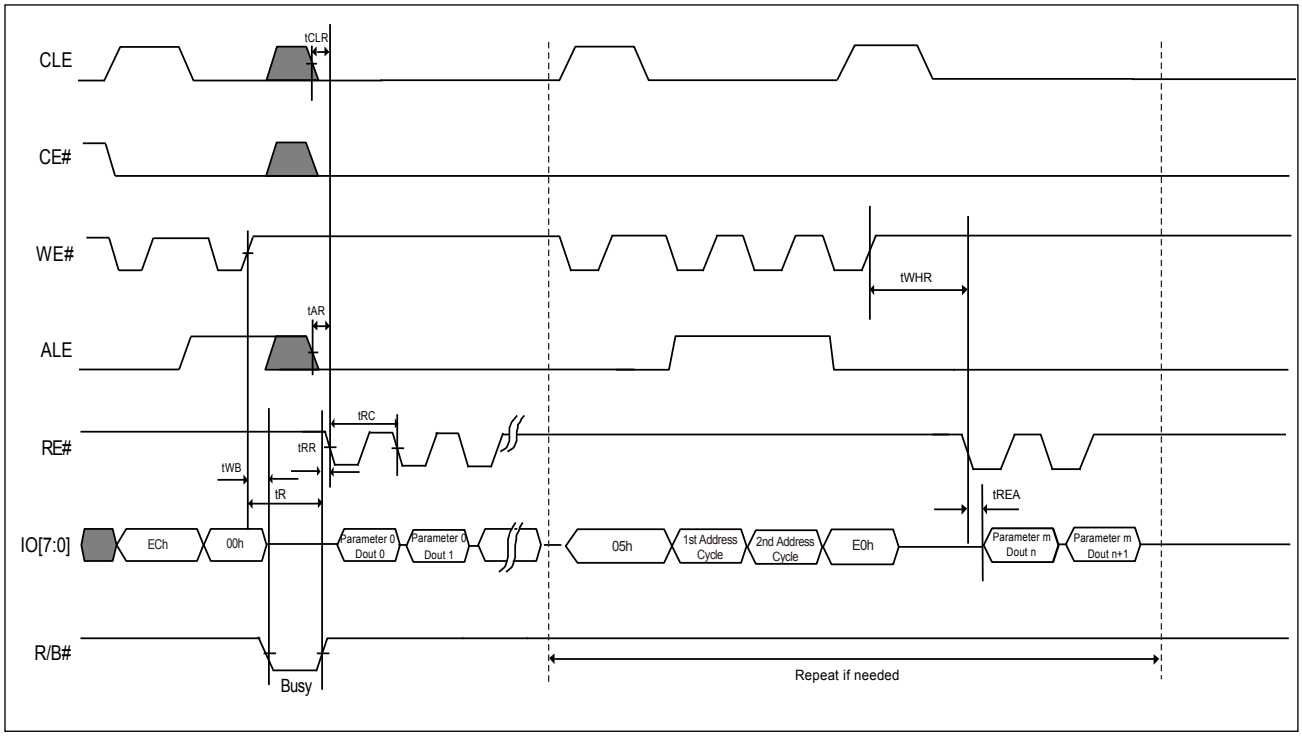
**Figure 22. AC waveforms for Parameter Page Read (ONFI) Operation**





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**Figure 23. AC Waveforms for Parameter Page Read (ONFI) Random Operation (For 05h-E0h)**





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**Table 7. Parameter Page (ONFI)**

| | Revision Information and Features Block | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **0-3** | **Parameter Page Signature** | | 4Fh, 4Eh, 46h, 49h |
| **4-5** | **Revision Number** | | 02h, 00h |
| **6-7** | **Features Supported** | | 10h, 00h |
| **8-9** | **Optional Commands Supported** | | 37h, 00h |
| **10-31** | **Reserved** | | 00h |
| | **Manufacturer Information Block** | | |
| **Byte#** | **Description** | | **Data** |
| **32-43** | **Device Manufacturer (12 ASCII characters)** | | 4Dh,41h,43h,52h,4Fh,4Eh,49h,58h, 20h,20h,20h,20h |
| **44-63** | **Device Model (20 ASCII Characters)** | MX30LF1G18AC | 4Dh,58h,33h,30h,4Ch,46h,31h,47h, 31h,38h,41h,43h,20h,20h,20h,20h, 20h,20h,20h,20h, |
| **64** | **JEDEC Manufacturer ID** | | C2h |
| **65-66** | **Date Code** | | 00h, 00h |
| **67-79** | **Reserved** | | 00h |

| Memory Organization Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **80-83** | Number of Data Bytes per Page | 2048-byte | 00h,08h,00h,00h |
| **84-85** | Number of Spare Bytes per Page | 64-byte | 40h,00h |
| **86-89** | Number of Data Bytes per Partial Page | 512-byte | 00h,02h,00h,00h |
| **90-91** | Number of Spare Bytes per Partial Page | 16-byte | 10h,00h |
| **92-95** | Number of Pages per Block | | 40h,00h,00h,00h |
| **96-99** | Number of Blocks per Logical Unit | | 00h,04h,00h,00h |
| **100** | Number of Logical Units (LUNs) | | 01h |
| **101** | Number of Address Cycles | | 22h |
| **102** | Number of Bits per Cell | | 01h |
| **103-104** | Bad Blocks Maximum per LUN | | 14h,00h |
| **105-106** | Block endurance | | 01h, 05h |
| **107** | Guarantee Valid Blocks at Beginning of Target | | 01h |
| **108-109** | Block endurance for guaranteed valid blocks | | 01h, 03h |
| **110** | Number of Programs per Page | | 04h |
| **111** | Partrial Programming Attributes | | 00h |
| **112** | Number of Bits ECC Correctability | | 04h |
| **113** | Number of Interleaved Address Bits | | 00h |
| **114** | Interleaved Operation Attributes | | 00h |
| **115-127** | Reserved | | 00h |


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| Electrical Parameters Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **128** | I/O Pin Capacitance | | 0Ah |
| **129-130** | Timing Mode Support | | 3Fh,00h |
| **131-132** | Program Cache Timing Mode Support | | 3Fh,00h |
| **133-134** | tPROG Maximum Page Program Time (uS) | 600us | 58h,02h |
| **135-136** | tBERS(tERASE) Maximum Block Erase Time (uS) | 3,500us | ACh,0Dh |
| **137-138** | tR Maximum Page Read Time (uS) | 25us | 19h,00h |
| **139-140** | tCCS Minimum Change Column Setup Time (ns) | 60ns | 3Ch,00h |
| **141-163** | Reserved | | 00h |
| **Vendor Blocks** | | | |
| **Byte#** | **Description** | | **Data** |
| **164-165** | Vendor Specific Revision Number | | 00h |
| **166-253** | Vendor Specific | | 00h |
| **254-255** | Integrity CRC | | Set at Test ***(Note)*** |
| **Redundant Parameter Pages** | | | |
| **Byte#** | **Description** | | **Data** |
| **256-511** | Value of Bytes 0-255 | | |
| **512-767** | Value of Bytes 0-255 | | |
| **768+** | Additional Redundant Parameter Pages | | |

***Note:*** *The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details.*

*The CRC shall be calculated using the following 16-bit generator polynomial:*

$G(X) = X_{16} + X_{15} + X_2 + 1$


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## 6-13. Unique ID Read (ONFI)

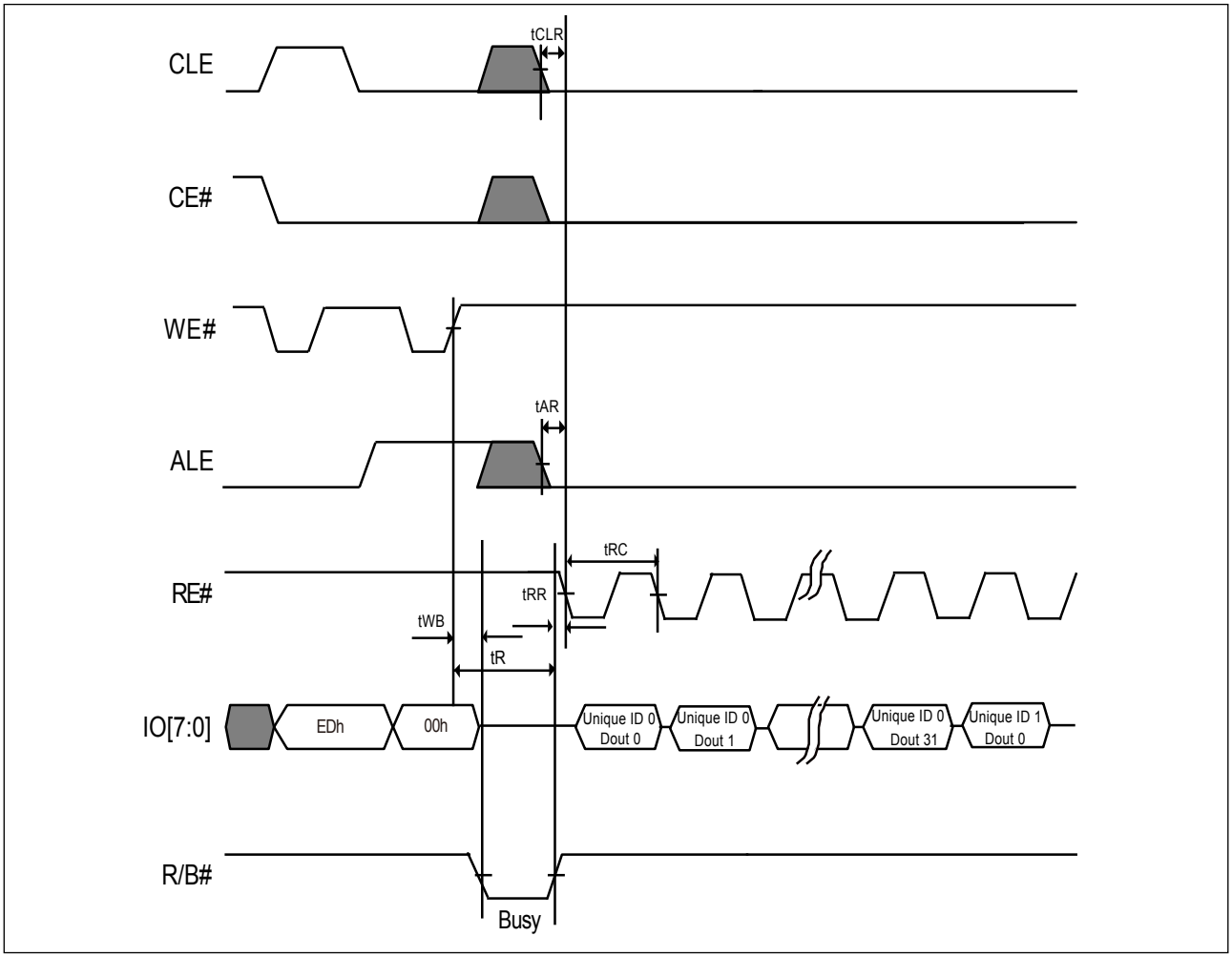
The unique ID is 32-byte and with 16 copies for back-up purpose. After writing the Unique ID read command (EDh) and following the one address byte (00h), the host may read out the unique ID data. The host need to XOR the 1st 16-byte unique data and the 2nd 16-byte complement data to get the result, if the result is FFh, the unique ID data is correct; otherwise, host need to repeat the XOR with the next copy of Unique ID data.

Once sending the EDh command, the NAND device will remain in the Unique ID read mode until next valid command is sent.

To change the data output location, it is recommended to use the Random Data Out command set (05h-E0h).

The Status Read command (70h) can be used to check the completion. To continue the read operation, a following read command (00h) to re-enable the data out is necessary.

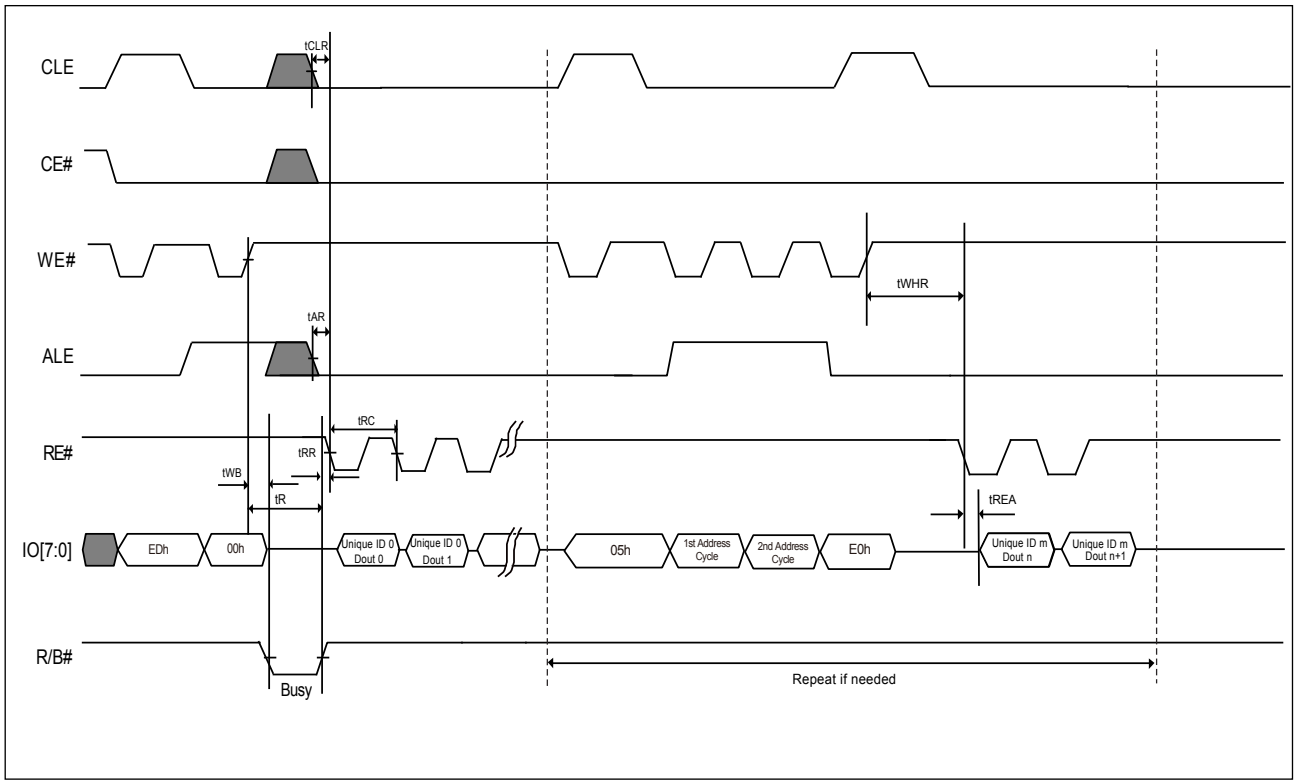
**Figure 24. AC waveforms for Unique ID Read Operation**





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**Figure 25. AC waveforms for Unique ID Read Operation (For 05h-E0h)**





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## 6-14. Feature Set Operation (ONFI)

The Feature Set operation is to change the default power-on feature sets by using the Set Feature and Get Feature command and writing the specific parameter data (P1-P4) on the specific feature addresses. The NAND device may remain the current feature set until next power cycle since the feature set data is volatile. However, the reset command (FFh) can not reset the current feature set.

**Table 8-1. Definition of Feature Address**

| Feature Address | Description |
|---|---|
| 00h-8Fh, 91h-FFh, | Reserved |
| 90h | Array Operation Mode |
| A0h | Block Protection Operation |

**Table 8-2. Sub-Feature Parameter Table of Feature Address - 90h (Array Operation Mode)**

| Sub Feature Parameter | Definition | | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | Values | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P1 | Array Operation Mode | Normal | Reserved (0) | | | | | | 0 | 0 | 0000 0000b | 1 |
| | | OTP Operation | Reserved (0) | | | | | 0 | 0 | 1 | 0000 0001b | |
| | | OTP Protection | Reserved (0) | | | | | 0 | 1 | 1 | 0000 0011b | |
| P2 | | | Reserved (0) | | | | | | | | 0000 0000b | |
| P3 | | | Reserved (0) | | | | | | | | 0000 0000b | |
| P4 | | | Reserved (0) | | | | | | | | 0000 0000b | |

***Note 1.*** *The value is clear to 00h at power cycle.*

**Table 8-3. Sub-Feature Parameter Table of Feature Address - A0h (Block Protection Operation) (note 1)**

| Sub Feature Parameter | Definition | | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | Values | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P1 | Block Protection Operation | Default mode | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38h | note 2 |
| | | Protection Bit Setting | 0 | 0 | BP2 | BP1 | BP0 | Invert | Complementary | SP | note 3 | note 4 |
| P2 | | | Reserved (0) | | | | | | | | | |
| P3 | | | Reserved (0) | | | | | | | | | |
| P4 | | | Reserved (0) | | | | | | | | | |

***Notes:***

1. *If the PT pin is not connected to high, this sub-feature address A0h command is not valid.*
2. *The value is returned to 38h at power cycle.*
3. *The value is defined in the Table 9. Definition of Protection Bits.*
4. *The SP stands for Solid-Protection. Once the SP bit sets as 1, the rest of protection bits cannot be changed during the current power cycle.*

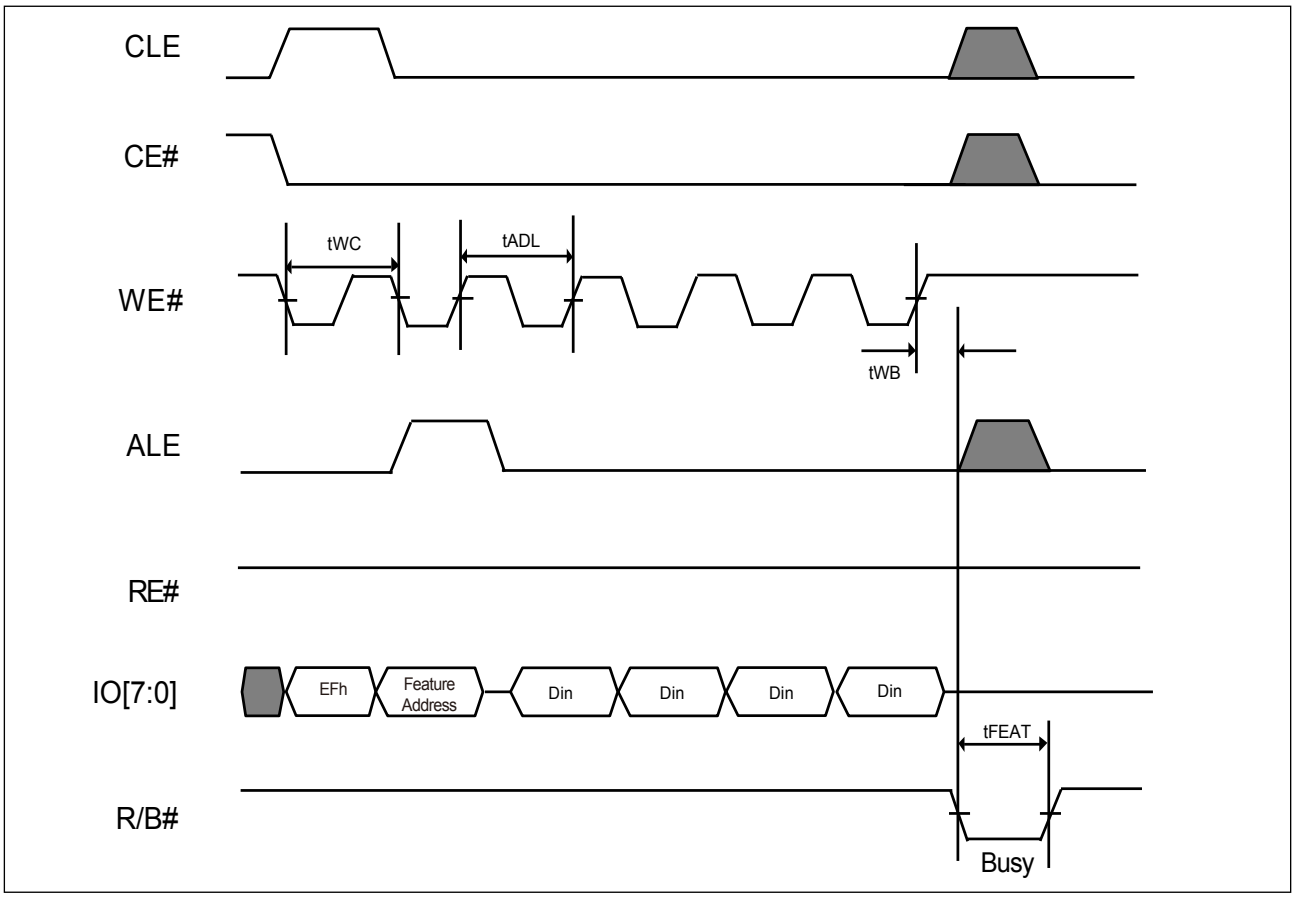

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### 6-14-1. Set Feature (ONFI)

The Set Feature command is to change the power-on default feature set. After sending the Set Feature command (EFh) and following specific feature and then input the P1-P4 parameter data to change the default power-on feature set. Once sending the EFh command, the NAND device will remain in the Set Feature mode until next valid command is sent.

The Status Read command (70h) may check the completion of the Set Feature.

**Figure 26. AC Waveforms for Set Feature (ONFI) Operation**





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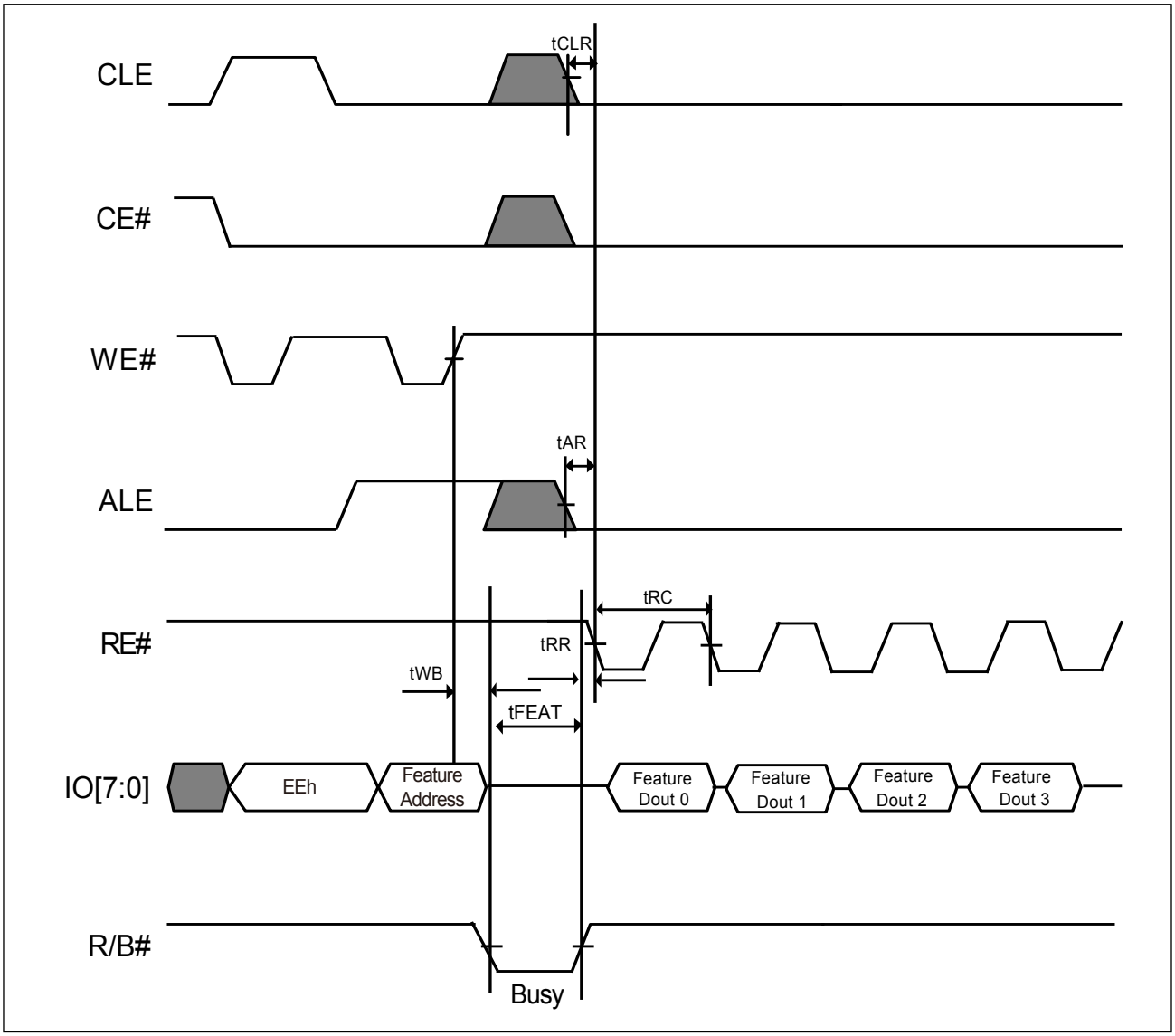
## 6-14-2. Get Feature (ONFI)

The Get Feature command is to read sub-feature parameter. After sending the Get Feature command (EEh) and following specific feature, the host may read out the P1-P4 sub- feature parameter data. Once sending the EEh command, the NAND device will remain in the Get Feature mode until next valid command is sent.

The Status Read command (70h) can be used to check the completion. To continue the read operation, a following read command (00h) to re-enable the data out is necessary.

Please refer to the following waveform of **Get Feature Operation** for details.

**Figure 27. AC Waveforms for Get Feature (ONFI) Operation**





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## 6-14-3. Secure OTP (One-Time-Programmable) Feature

There is an OTP area which has thirty full pages (30 x 2,112-byte) guarantee to be good for system device serial number storage or other fixed code storage. The OTP area is a non-erasable and one-time-programmable area, which is default to “1” and allows whole page or partial page program to be “0”, once the OTP protection mode is set, the OTP area becomes read-only and cannot be programmed again.

The OTP operation is operated by the Set Feature/ Get Feature operation to access the OTP operation mode and OTP protection mode.

To check the NAND device is ready or busy in the OTP operation mode, either checking the R/B# or writing the Status Read command (70h) may collect the status.

To exit the OTP operation or protect mode, it can be done by writing 00h to P1 at feature address 90h.

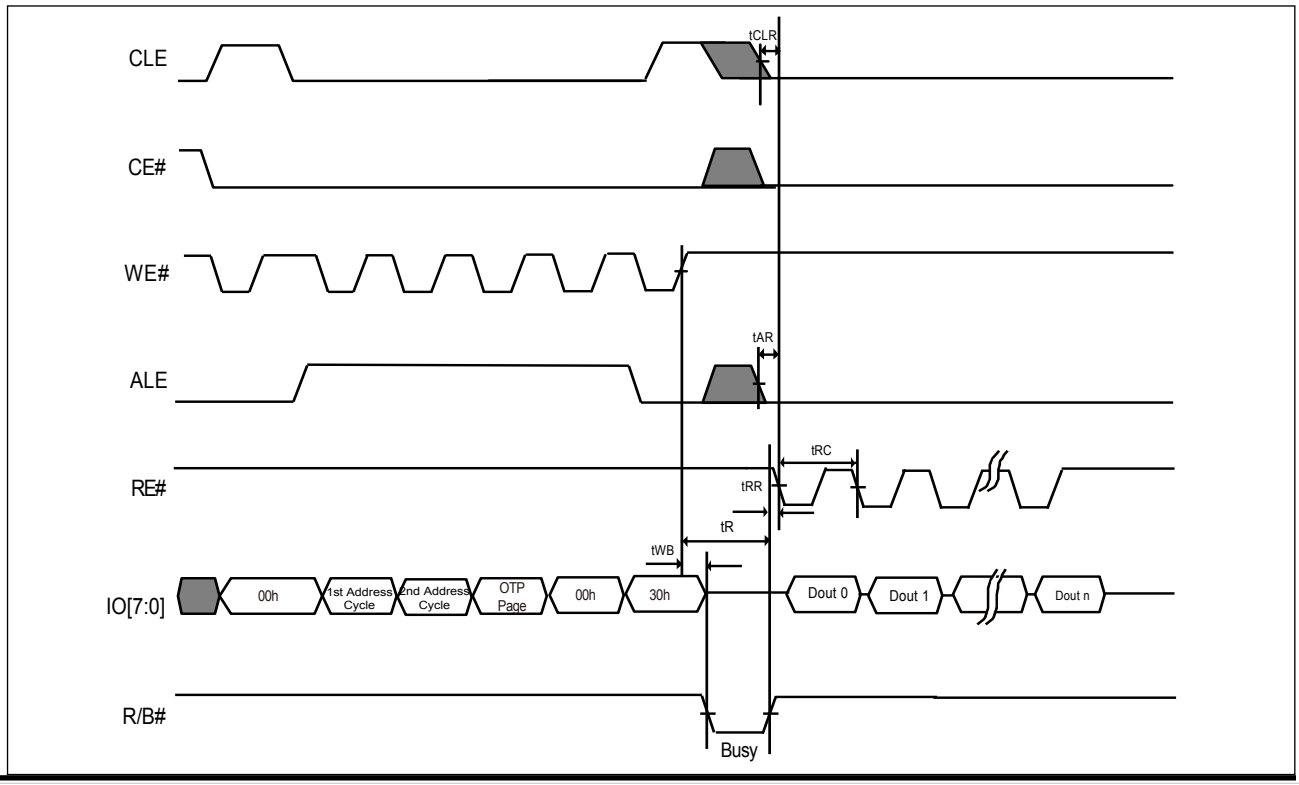
### OTP Read/Program Operation

To enter the OTP operation mode, it is by using the Set Feature command (EFh) and followed by the feature address (90h) and then input the 01h to P1 and 00h to P2-P4 of sub-Feature Parameter data( please refer to **Table 8-2. Sub-Feature Parameter Table of Feature Address - 90h (Array Operation Mode)** and **Table 8-3. Sub-Feature Parameter Table of Feature Address - A0h (Block Protection Operation) (note 1)**). After enter the OTP operation mode, the normal Read command (00h-30h) or Page program( 80h-10h) command can be used to read the OTP area or program it. The address of OTP is located on the 02h-1Fh of page address.

Besides the normal Read command, the Random Data Output command (05h-E0h) can be used for read OTP data. However, the Cache Read command is not supported in the OTP area.

Besides the normal page program command, the Random Data Input command (85h) allows multi-data load in non-sequential address. After data load is completed, a program confirm command (10h) is issued to start the page program operation. The number of partial-page OTP program is 8 per each OTP page.

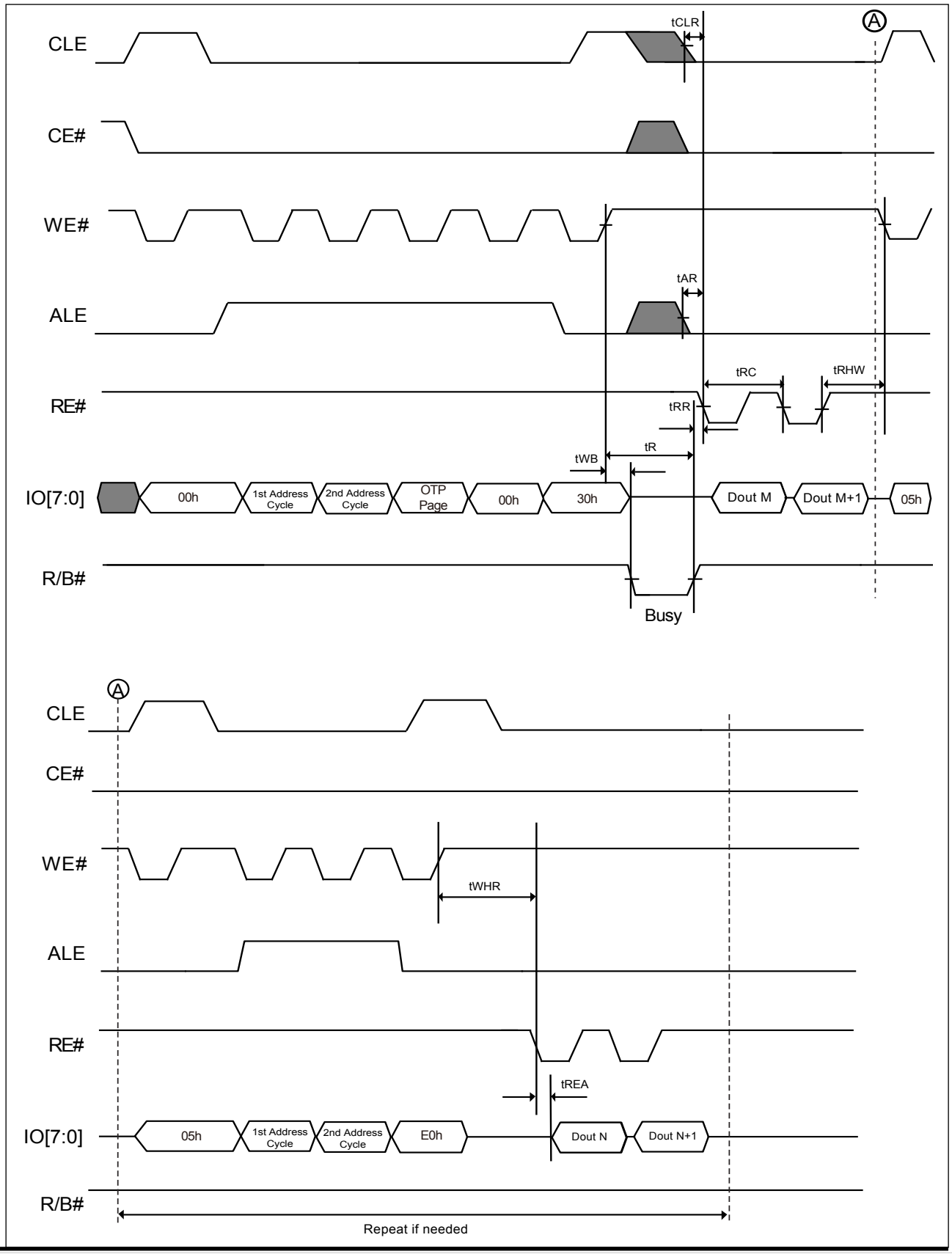
**Figure 28. AC Waveforms for OTP Data Read**





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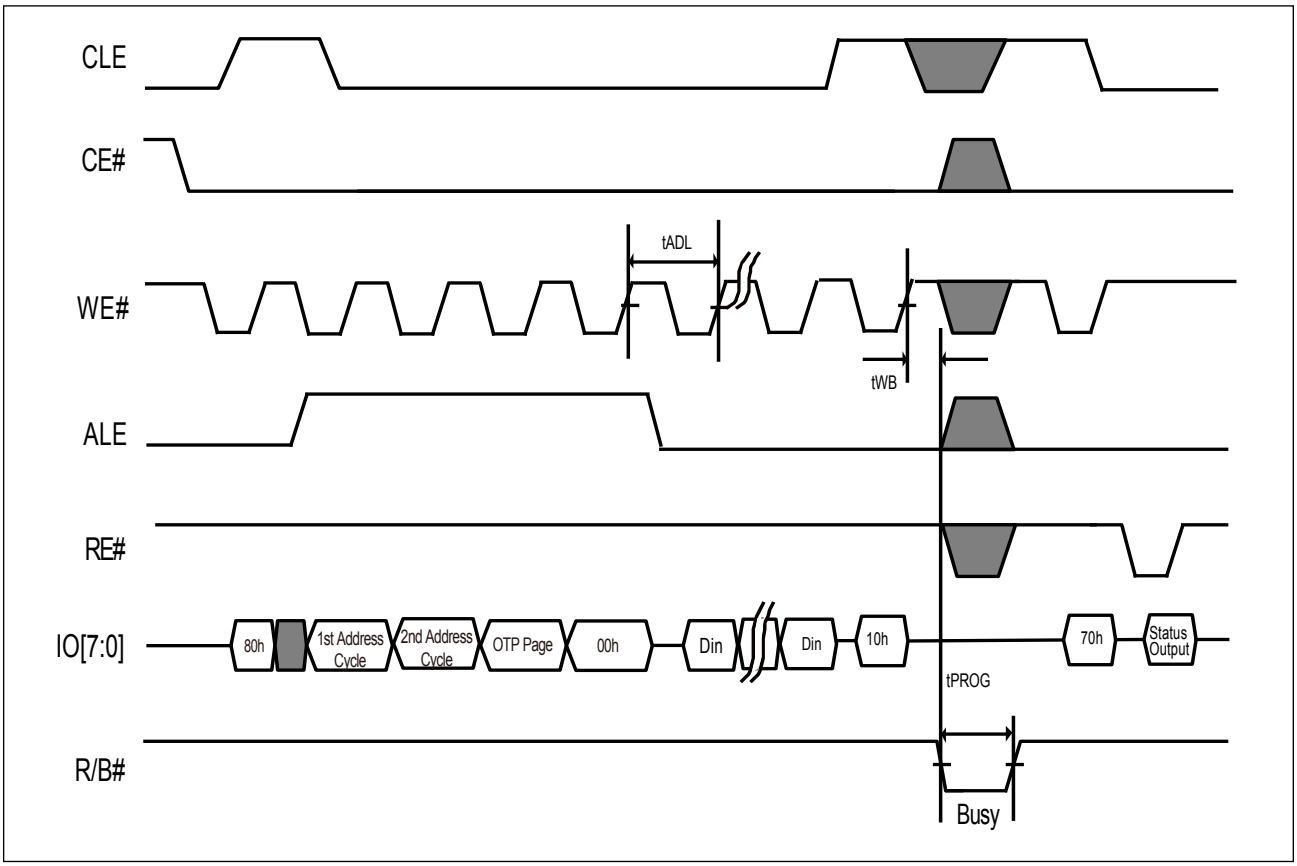
**Figure 29. AC Waveforms for OTP Data Read with Random Data Output**





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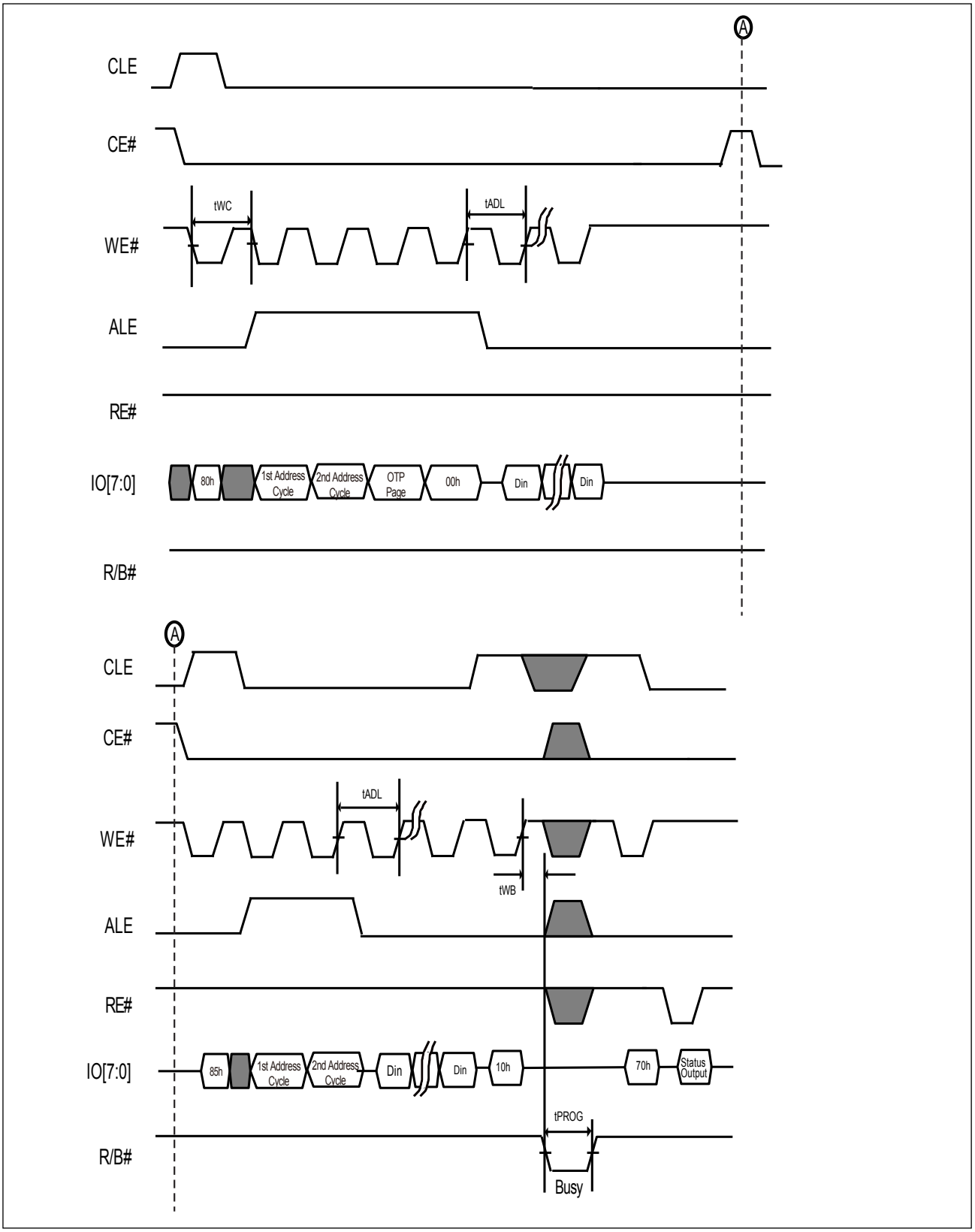
**Figure 30. AC Waveforms for OTP Data Program**





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**Figure 31. AC Waveforms for OTP Data Program with Random Data Input**





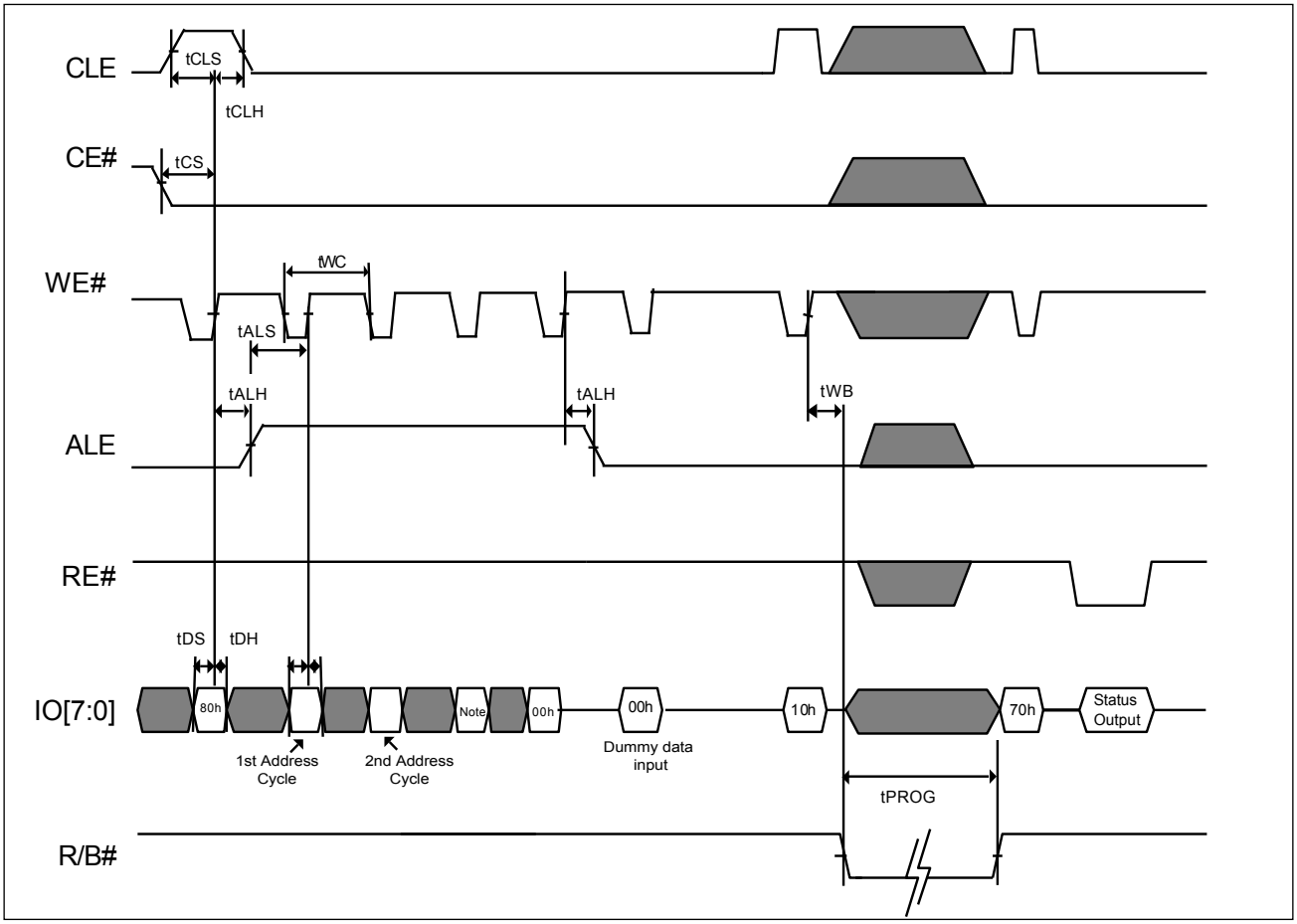
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## OTP Protection Operation

To prevent the further OTP data to be changed, the OTP protection mode operation is necessary. To enter the OTP protection mode, it can be done by using the Set Feature command (EFh) and followed by the feature address (90h) and then input the 03h to P1 and 00h to P2-P4 of sub-Feature Parameter data (please refer to the **Table 8-2. Sub-Feature Parameter Table of Feature Address - 90h (Array Operation Mode)** and **Table 8-3. Sub-Feature Parameter Table of Feature Address - A0h (Block Protection Operation) (note 1)**). And then the normal page program command (80h-10h) with the address 00h before the 10h command is required.

The OTP Protection mode is operated by the whole OTP area instead of individual OTP page. Once the OTP protection mode is set, the OTP area cannot be programmed or unprotected again.

**Figure 32. AC Waveforms for OTP Protection Operation**




***Note:*** *This address cycle can be any value since the OTP protection protects the entire OTP area instead of individual OTP page.*


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## 6-14-4. Block Protection

The block protect operation can protect the whole chip or selected blocks from erasing or programming. Through the PT pin at power-on stage, it decides the block protection operation is enabled or disabled. At power-on, if the PT pin is connected to high, the block protection operation is enabled, all the blocks are default to be protected from programming/erasing even the WP# is disabled. If the PT pin is low, block protection operation is disabled. Please refer to the **Figure 33. PT Pin and Block Protection Mode Operation.**

When program or erase attempt at a protected block is happened, the R/B# keeps low for the time of tPBSY, and the Status Read command (70h) may get the 60h result.

There are Temporary Protection/un-Protection and Solid Protection features as below description.

**Temporary Protection/un-Protection**

At power-on, if the PT pin is connected to high, all the blocks are default to be protected for the BPx protection bits are all "1". The Set feature command with feature address A0h followed by the destined protection bits data is necessary to un-protect those selected blocks before those selected blocks to be updated. The WP# pin needs to connect to high before writing the Set Feature command for the block protection operation. After the selected blocks are un-protected, those un-protected blocks can be protected again by Block Protection procedure if required.

**Solid Protection**

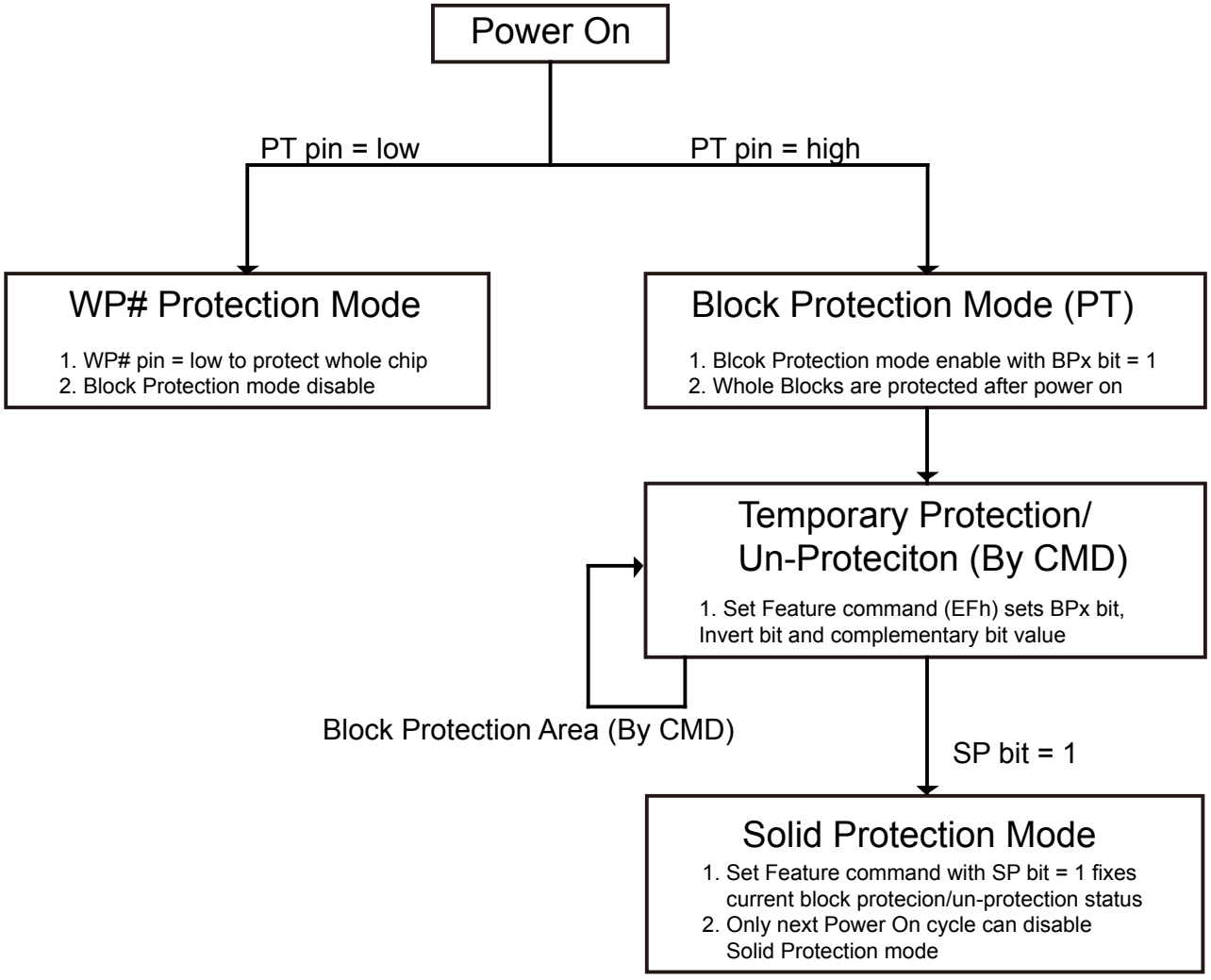
The "solid-protection" feature can be set by writing the Set Feature command with address A0h and the "SP" solid-protection bit as "1", after that, the selected block is solid-protected and cannot be up-protected until next power cycle.

### Table 9. Definition of Protection Bits

| BP2 | BP1 | BP0 | Invert | Complementary | Protection Area |
|---|---|---|---|---|---|
| 0 | 0 | 0 | x | x | all unlocked |
| 0 | 0 | 1 | 0 | 0 | upper 1/64 locked |
| 0 | 1 | 0 | 0 | 0 | upper 1/32 locked |
| 0 | 1 | 1 | 0 | 0 | upper 1/16 locked |
| 1 | 0 | 0 | 0 | 0 | upper 1/8 locked |
| 1 | 0 | 1 | 0 | 0 | upper 1/4 locked |
| 1 | 1 | 0 | 0 | 0 | upper 1/2 locked |
| 1 | 1 | 1 | x | x | all locked (default) |
| 0 | 0 | 1 | 1 | 0 | lower 1/64 locked |
| 0 | 1 | 0 | 1 | 0 | lower 1/32 locked |
| 0 | 1 | 1 | 1 | 0 | lower 1/16 locked |
| 1 | 0 | 0 | 1 | 0 | lower 1/8 locked |
| 1 | 0 | 1 | 1 | 0 | lower 1/4 locked |
| 1 | 1 | 0 | 1 | 0 | lower 1/2 locked |
| 0 | 0 | 1 | 0 | 1 | lower 63/64 locked |
| 0 | 1 | 0 | 0 | 1 | lower 31/32 locked |
| 0 | 1 | 1 | 0 | 1 | lower 15/16 locked |
| 1 | 0 | 0 | 0 | 1 | lower 7/8 locked |
| 1 | 0 | 1 | 0 | 1 | lower 3/4 locked |
| 1 | 1 | 0 | 0 | 1 | block 0 |
| 0 | 0 | 1 | 1 | 1 | upper 63/64 locked |
| 0 | 1 | 0 | 1 | 1 | upper 31/32 locked |
| 0 | 1 | 1 | 1 | 1 | upper 15/16 locked |
| 1 | 0 | 0 | 1 | 1 | upper 7/8 locked |
| 1 | 0 | 1 | 1 | 1 | upper 3/4 locked |
| 1 | 1 | 0 | 1 | 1 | block0 |


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**Figure 33. PT Pin and Block Protection Mode Operation**





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# 7. PARAMETERS

## 7-1. ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| **Temperature under Bias** | -50°C to +125°C |
| **Storage temperature** | -65°C to +150°C |
| **All input voltages with respect to ground (Note 2)** | -0.6V to 4.6V |
| **VCC supply voltage with respect to ground (Note 2)** | -0.6V to 4.6V |
| **ESD protection** | >2000V |

***Notes:***

*1. The reliability of device may be impaired by exposing to extreme maximum rating conditions for long range of time.*

*2. Permanent damage may be caused by the stresses higher than the "Absolute Maximum Ratings" listed.*

*3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, as shown in **Figure 34. Maximum Negative Overshoot Waveform** and **Figure 35. Maximum Positive Overshoot Waveform**.*

**Figure 34. Maximum Negative Overshoot Waveform**

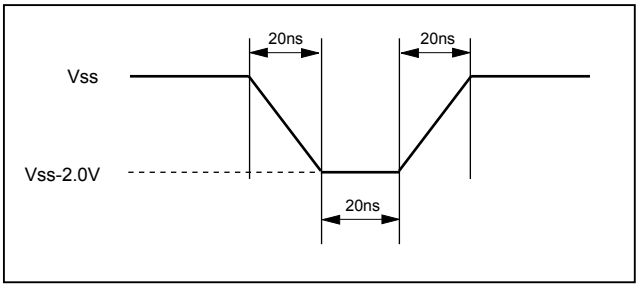
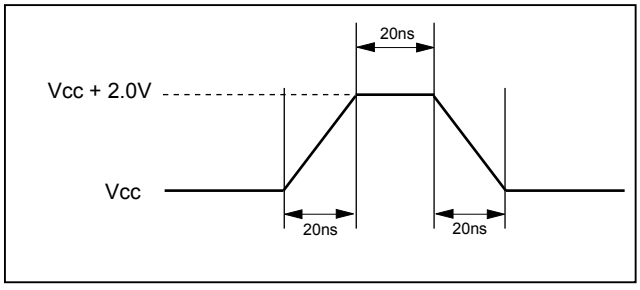



**Figure 35. Maximum Positive Overshoot Waveform**





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**Table 10. Operating Range**

| Temperature | VCC | Tolerance |
|---|---|---|
| -40°C to +85°C | +3.3V | 2.7 - 3.6V |

**Table 11. DC Characteristics**

| Symbol | Parameter | Test Conditions | Min. | Typical | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| VIL | Input low level | | -0.3 | | 0.2VCC | V | |
| VIH | Input high level | | 0.8VCC | | VCC + 0.3 | V | |
| VOL | Output low voltage | IOL= 2.1mA, VCC= VCC Min. | | | 0.2 | V | |
| VOH | Output high voltage | IOH= -400uA, VCC= VCC Min. | VCC-0.2 | | | V | |
| ISB1 | VCC standby current (CMOS) | CE# = VCC -0.2V, WP# = 0/VCC | | 10 | 50 | uA | |
| ISB2 | VCC standby current (TTL) | CE# = VIH Min., WP# = 0/VCC | | | 1 | mA | |
| ICC0 | Power on current (Including POR current) | | | | 50 | mA | |
| ICC1 | VCC active current (Sequential Read) | tRC Min., CE# = VIL, IOUT= 0mA | | 15 | 30 | mA | |
| ICC2 | VCC active current (Program) | | | 15 | 30 | mA | |
| ICC3 | VCC active current (Erase) | | | 15 | 30 | mA | |
| ILI | Input leakage current | VIN= 0 to VCC Max. | | | +/- 10 | uA | |
| ILO | Output leakage current | VOUT= 0 to VCC Max. | | | +/- 10 | uA | |
| ILO (R/B#) | Output current of R/B# pin | VOL=0.4V | 8 | 10 | | mA | |


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**Table 12. Capacitance**

TA = +25°C, F = 1 MHz

| Symbol | Parameter | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| CIN | Input capacitance | | 10 | pF | VIN = 0 V |
| COUT | Output capacitance | | 10 | pF | VOUT = 0 V |

**Table 13. AC Testing Conditions**

| Testing Conditions | Value | Unit |
|---|---|---|
| **Input pulse level** | 0 to VCC | V |
| **Output load capacitance** | 1TTL+CL(50) | pF |
| **Input rise and fall time** | 5 | ns |
| **Input timing measurement reference levels** | VCC/2 | V |
| **Output timing measurement reference levels** | VCC/2 | V |

**Table 14. Program and Erase Characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| **tPROG** | Page programming time | | 300 | 600 | us | |
| **tCBSY (Program)** | Dummy busy time for cache program | | 5 | 600 | us | |
| **tRCBSY (Read)** | Dummy busy time for cache read | | 3.5 | 25 | us | |
| **tDBSY** | The busy time for two-plane program/erase operation | | 0.5 | 1 | us | |
| **tFEAT** | The busy time for Set Feature/ Get Feature | | | 1 | us | |
| **tOBSY** | The busy time for OTP program at OTP protection mode | | | 30 | us | |
| **tPBSY** | The busy time for program/erase at protected blocks | | | 3 | us | |
| **NOP** | Number of partial program cycles in same page | | | 4 | cycles | |
| **tERASE (Block)** | Block erase time | | 1 | 3.5 | ms | |


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**Table 15. AC Characteristics**

| Symbol | Parameter | Min. | Typical | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| **tCLS** | CLE setup time | 10 | | | ns | 1 |
| **tCLH** | CLE hold time | 5 | | | ns | 1 |
| **tCS** | CE# setup time | 15 | | | ns | 1 |
| **tCH** | CE# hold time | 5 | | | ns | 1 |
| **tWP** | Write pulse width | 10 | | | ns | 1 |
| **tALS** | ALE setup time | 10 | | | ns | 1 |
| **tALH** | ALE hold time | 5 | | | ns | 1 |
| **tDS** | Data setup time | 7 | | | ns | 1 |
| **tDH** | Data hold time | 5 | | | ns | 1 |
| **tWC** | Write cycle time | 20 | | | ns | 1, 2 |
| **tWH** | WE# high hold time | 7 | | | ns | 1 |
| **tADL** | Last address latched to data loading time during program operations | 70 | | | ns | 1 |
| **tWW** | WP# transition to WE# high | 100 | | | ns | 1 |
| **tRR** | Ready to RE# falling edge | 20 | | | ns | 1 |
| **tRP** | Read pulse width | 10 | | | ns | 1 |
| **tRC** | Read cycle time | 20 | | | ns | 1 |
| **tREA** | RE# access time (serial data access) | | | 16 | ns | 1 |
| **tCEA** | CE# access time | | | 25 | ns | 1 |
| **tRLOH** | RE#-low to data hold time (EDO) | 5 | | | ns | |
| **tOH** | Data output hold time | 15 | | | ns | 1 |
| **tRHZ** | RE#-high to output-high impedance | | | 60 | ns | 1 |
| **tCHZ** | CE#-high to output-high impedance | | | 50 | ns | 1 |
| **tCOH** | CE# high to output hold time | 15 | | | ns | |
| **tREH** | RE# high hold time | 7 | | | ns | 1 |
| **tIR** | Output high impedance to RE# falling edge | 0 | | | ns | 1 |
| **tRHW** | RE# high to WE# low | 60 | | | ns | 1 |
| **tWHR** | WE# high to RE# low | 60 | | | ns | 1 |
| **tR** | The data transfering from array to buffer | | | 25 | us | 1 |
| **tWB** | WE# high to busy | | | 100 | ns | 1 |
| **tCLR** | CLE low to RE# low | 10 | | | ns | 1 |
| **tAR** | ALE low to RE# low | 10 | | | ns | 1 |
| **tRST** | Device reset time (Idle/ Read/ Program/ Erase) | | | 5/5/10/500 | us | 1 |

***Note 1**. ONFI Mode 5 compliant*


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# 8. OPERATION MODES: LOGIC AND COMMAND TABLES

Address input, command input and data input/output are managed by the CLE, ALE, CE#, WE#, RE# and WP# signals, as shown in **Table 16. Logic Table** below.

Program, Erase, Read and Reset are four major operations modes controlled by command sets, please refer to **Table 17. HEX Command Table**.

**Table 16. Logic Table**

| Mode | CE# | RE# | WE# | CLE | ALE | WP# |
|---|---|---|---|---|---|---|
| Address Input (Read Mode) | L | H | ↑ | L | H | X |
| Address Input (Write Mode) | L | H | ↑ | L | H | H |
| Command Input (Read Mode) | L | H | ↑ | H | L | X |
| Command Input (Write Mode) | L | H | ↑ | H | L | H |
| Data Input | L | H | ↑ | L | L | H |
| Data Output | L | ↓ | H | L | L | X |
| During Read (Busy) | X | H | H | L | L | X |
| During Programming (Busy) | X | X | X | X | X | H |
| During Erasing (Busy) | X | X | X | X | X | H |
| Program/Erase Inhibit | X | X | X | X | X | L |
| Stand-by | H | X | X | X | X | 0V/VCC |

***Notes:***

1. *H = VIH;  L = VIL;  X = VIH or VIL*
2. *WP# should be biased to CMOS high or CMOS low for stand-by.*


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**Table 17. HEX Command Table**

| | First Cycle | Second Cycle | Acceptable While Busy |
|---|---|---|---|
| **Read Mode** | 00H | 30H | |
| **Random Data Input** | 85H | - | |
| **Random Data Output** | 05H | E0H | |
| **Cache Read Random** | 00H | 31H | |
| **Cache Read Sequential** | 31H | - | |
| **Cache Read End** | 3FH | - | |
| **ID Read** | 90H | - | |
| **Parameter Page Read (ONFI)** | ECH | - | |
| **Unique ID Read (ONFI)** | EDH | - | |
| **Set Feature (ONFI)** | EFH | - | |
| **Get Feature (ONFI)** | EEH | - | |
| **Reset** | FFH | - | V |
| **Page Program** | 80H | 10H | |
| **Cache Program** | 80H | 15H | |
| **Block Erase** | 60H | D0H | |
| **Status Read** | 70H | - | V |
| **Block Protection Status Read** | 7AH | - | |

***Caution:*** *None of the undefined command inputs can be accepted except for the command set in the above table.*


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## 8-1. R/B#: Termination for The Ready/Busy# Pin (R/B#)

The R/B# is an open-drain output pin and a pull-up resistor is necessary to add on the R/B# pin. The R/B# outputs the ready/busy status of read/program/ erase operation of the device. When the R/B# is at low, the device is busy for read or program or erase operation. When the R/B# is at high, the read/program/erase operation is finished.

### Rp Value Guidence

The rise time of the R/B# signal depends on the combination of Rp and capacitive loading of the R/B# circuit. It is approximately two times constants (Tc) between the 10% and 90% points on the R/B# waveform.

$$T_C = R \times C$$

Where R = $R_p$ (Resistance of pull-up resistor), and C = $C_L$ (Total capacitive load)

The fall time of the R/B# signal majorly depends on the output impedance of the R/B# signal and the total load capacitance.

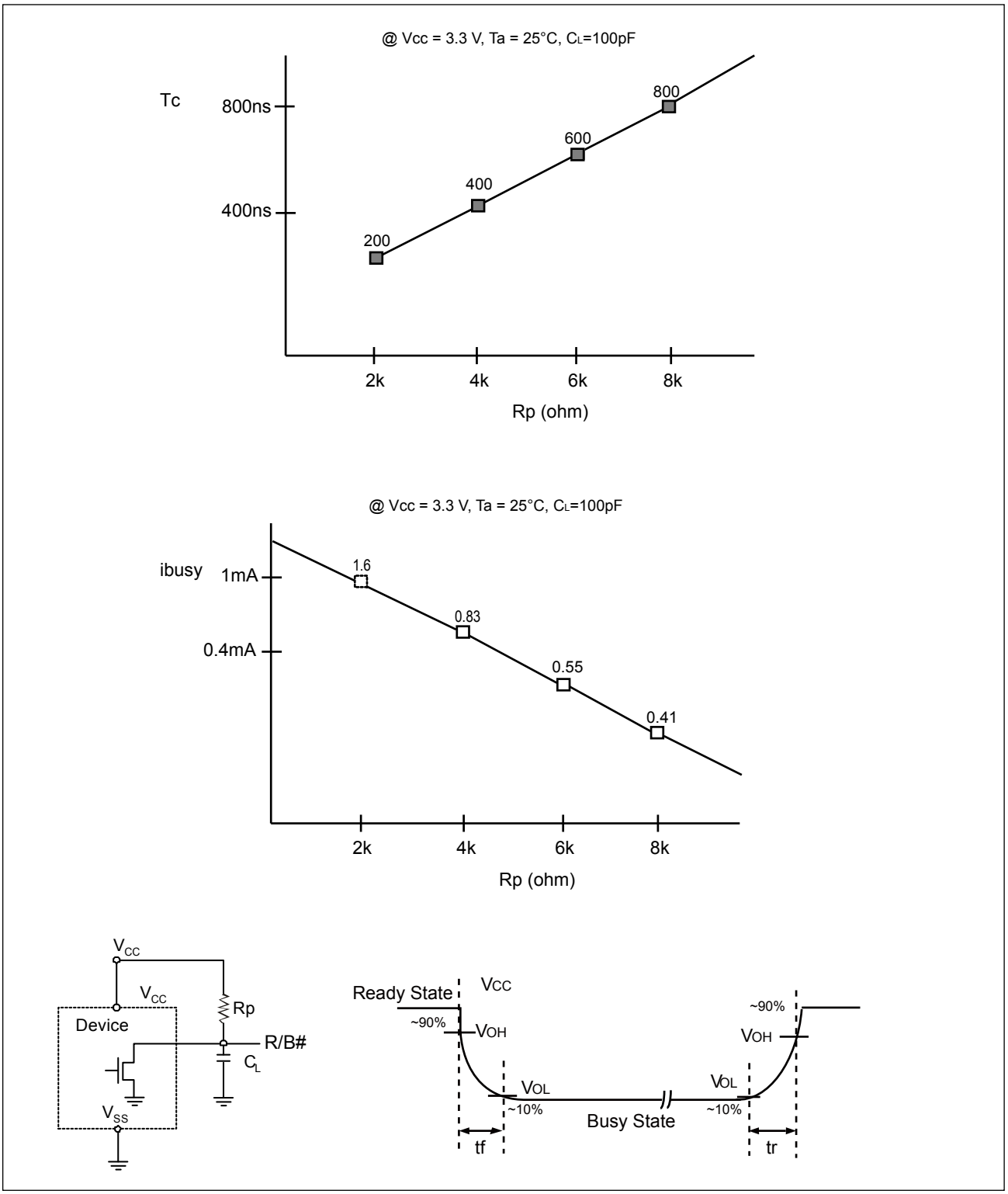
$$Rp\ (Min.) = \frac{Vcc\ (Max.) - VOL\ (Max.)}{I_{OL} + \Sigma I_L}$$

***Notes:***

1. *Considering of the variation of device-by-device, the above data is for reference to decide the resistor value.*
2. *Rp maximum value depends on the maximum permissible limit of tr.*
3. *IL is the total sum of the input currents of all devices tied to the R/B pin.*


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**Figure 36. R/B# Pin Timing Information**





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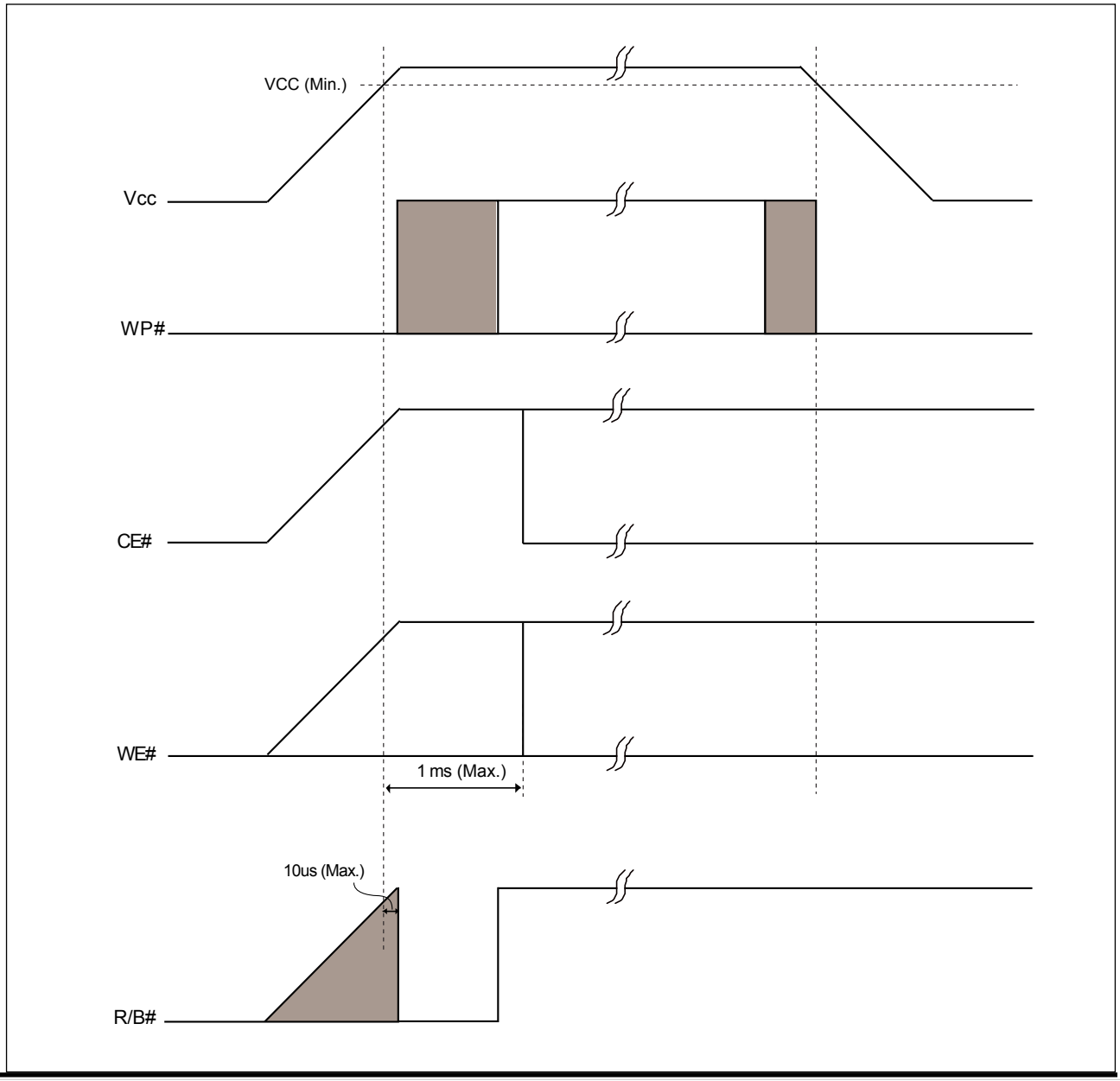
## 8-2. Power On/Off Sequence

After the Chip reaches the power on level (Vth = Vcc min.), the internal power on reset sequence will be triggered. During the internal power on reset period, no any external command is accepted. There are two ways to identify the termination of the internal power on reset sequence. Please refer to **Figure 37. Power On/Off Sequence**.

- R/B# pin
- Wait 1 ms

During the power on and power off sequence, it is recommended to keep the WP# = Low for internal data protection.

**Figure 37. Power On/Off Sequence**





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### 8-2-1. WP# Signal

WP# going Low can cause program and erase operations automatically reset.

The enabling & disabling of the both operations are as below:

**Figure 38-1. Enable Programming of WP# Signal**

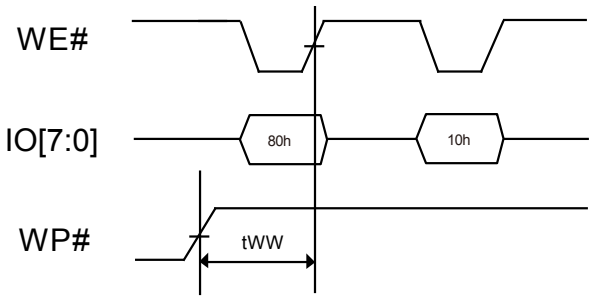



**Figure 38-2. Disable Programming of WP# Signal**

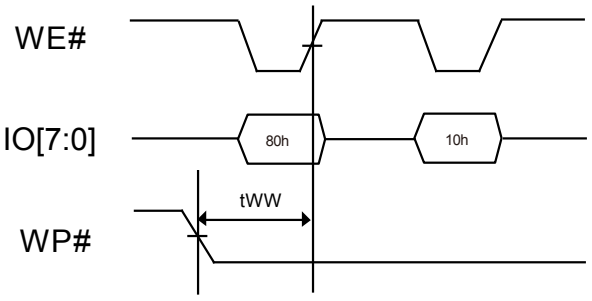



**Figure 38-3. Enable Erasing of WP# Signal**

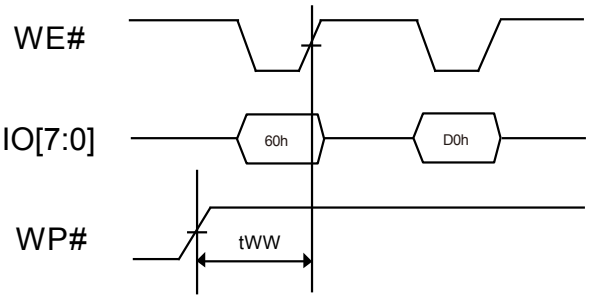
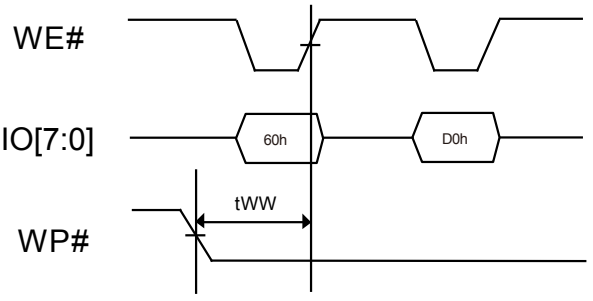



**Figure 38-4. Disable Erasing of WP# Signal**





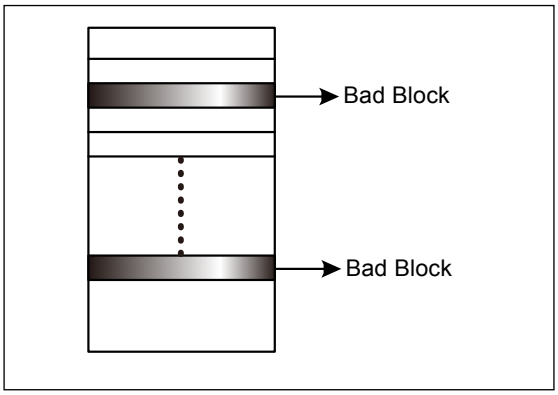
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# 9. SOFTWARE ALGORITHM

## 9-1. Invalid Blocks (Bad Blocks)

The bad blocks are included in the device while it gets shipped. During the time of using the device, the additional bad blocks might be increasing; therefore, it is recommended to check the bad block marks and avoid using the bad blocks. Furthermore, please read out the bad block information before any erase operation since it may be cleared by any erase operation.

**Figure 39. Bad Blocks**




While the device is shipped, the value of all data bytes of the good blocks are FFh. The 1st bytes of the 1st and 2nd page in the spare area for bad block will be 00h. The erase operation at the bad blocks is not recommended.

After the device is installed in the system, the bad block checking is recommended. **Figure 40. Bad Block Test Flow** shows the brief test flow by the system software managing the bad blocks while the bad blocks were found. When a block gets damaged, it should not be used any more.

Due to the blocks are isolated from bit-line by the selected gate, the performance of good blocks will not be impacted by bad ones.

**Table 18. Valid Blocks**

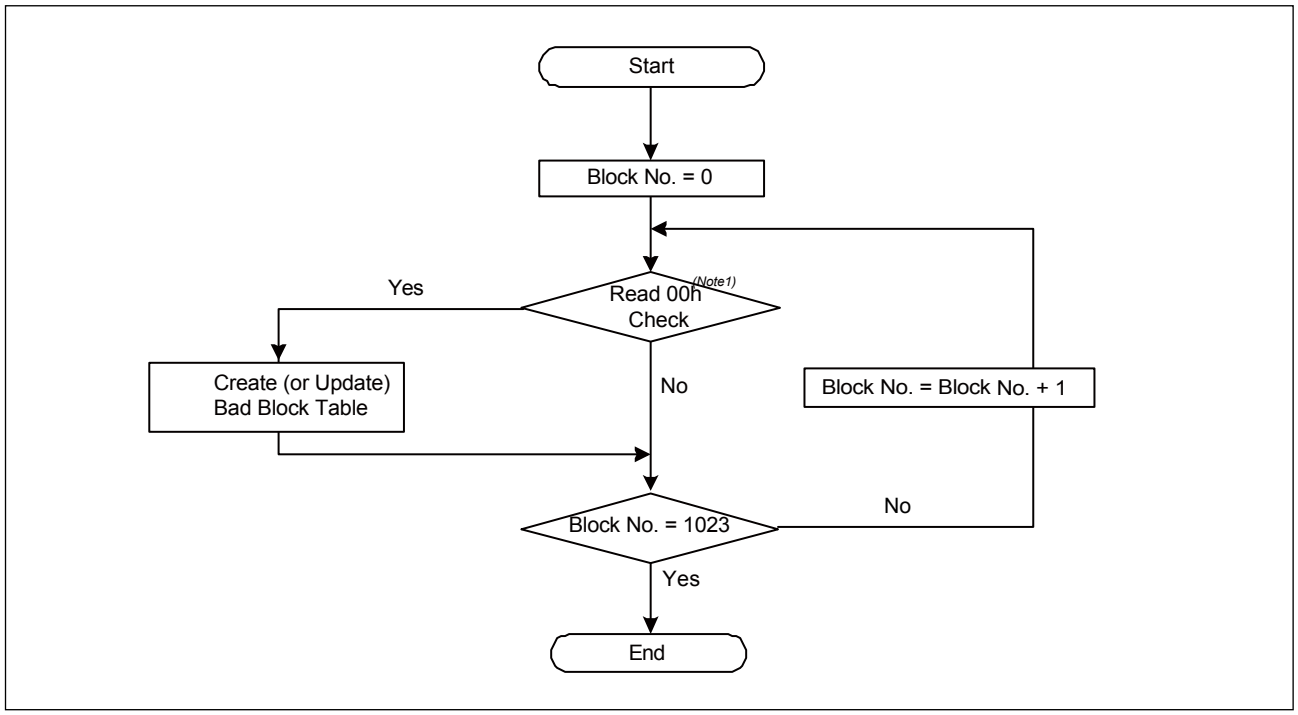
| | Density | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Valid (Good) Block Number | 1Gb | 1004 | | 1024 | Block | Block 0 is guaranteed to be good at least 1K P/E cycle (with ECC). |


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## 9-2. Bad Block Test Flow

Although the initial bad blocks are marked by the flash vendor, they could be inadvertently erased and destroyed by a user that does not pay attention to them. To prevent this from occurring, it is necessary to always know where any bad blocks are located. Continually checking for bad block markers during normal use would be very time consuming, so it is highly recommended to initially locate all bad blocks and build a bad block table and reference it during normal NAND flash use. This will prevent having the initial bad block markers erased by an unexpected program or erase operation. Failure to keep track of bad blocks can be fatal for the application. For example, if boot code is programmed into a bad block, a boot up failure may occur. **Figure 40. Bad Block Test Flow** shows the recommended flow for creating a bad block table.

**Figure 40. Bad Block Test Flow**




***Note 1:*** *Read 00h check is at the 1st byte of the 1st and 2nd pages of the block spare area.*

## 9-3. Failure Phenomena for Read/Program/Erase Operations

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system:

**Table 19. Failure Modes**

| Failure Mode | Detection and Countermeasure | Sequence |
|---|---|---|
| **Erase Failure** | Status Read after Erase | Block Replacement |
| **Programming Failure** | Status Read after Program | Block Replacement |
| **Read Failure** | Read Failure | ECC |


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## 9-4. Program

It is feasible to reprogram the data into another page (Page B) when an error occurred in Page A by loading from an external buffer. Then create a bad block table or by using another appropriate scheme to prevent further system accesses to Page A.

**Figure 41. Failure Modes**

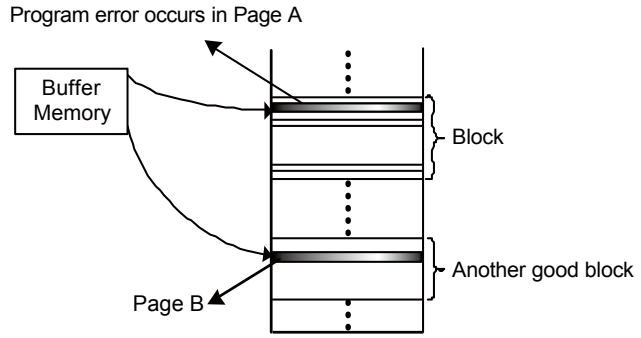
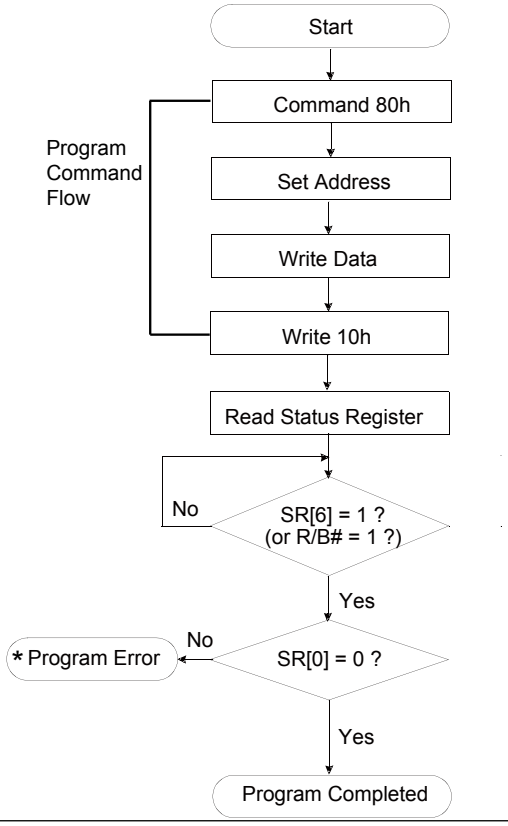



**Figure 42. Program Flow Chart**




## 9-5. Erase

To prevent future accesses to this bad block, it is feasible to create a table within the system or by using another appropriate scheme when an error occurs in an Erase operation.


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**Figure 43. Erase Flow Chart**

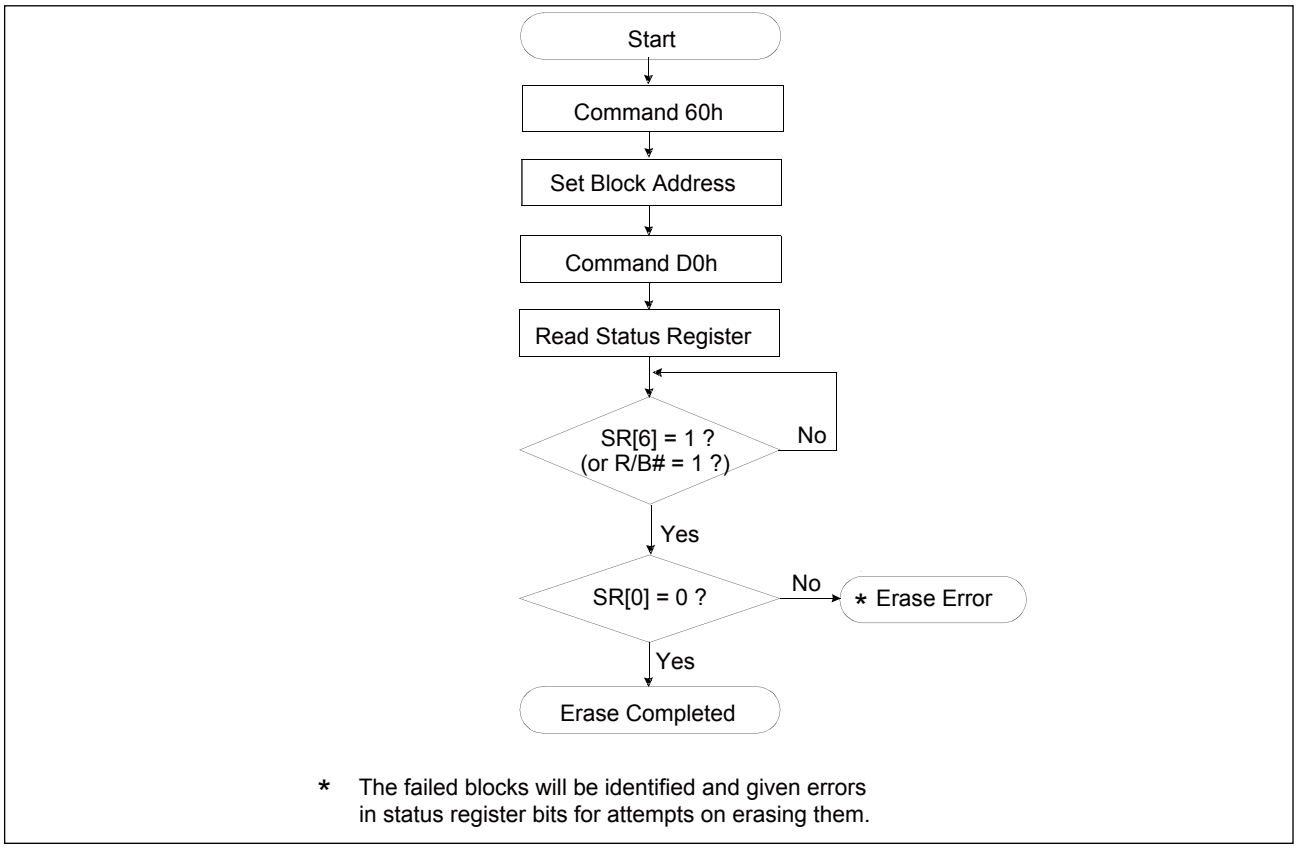
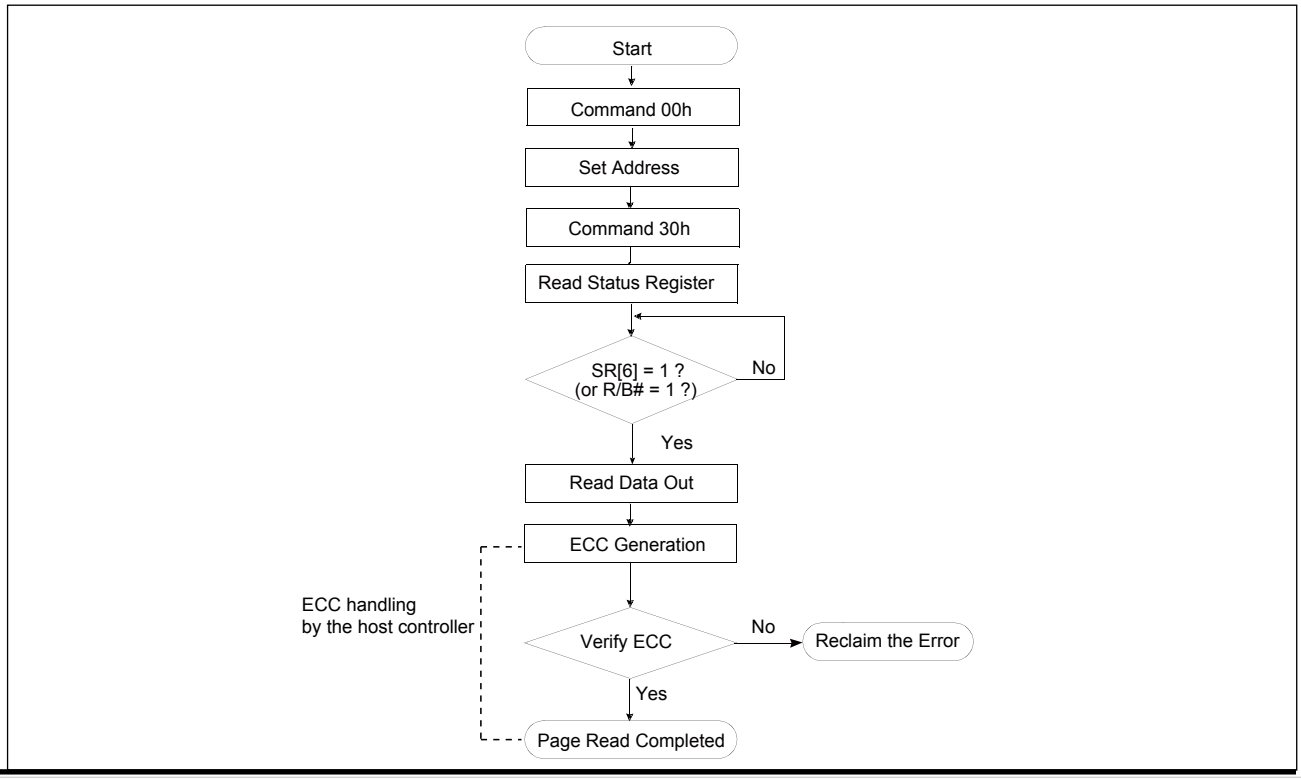



**Figure 44. Read Flow Chart**

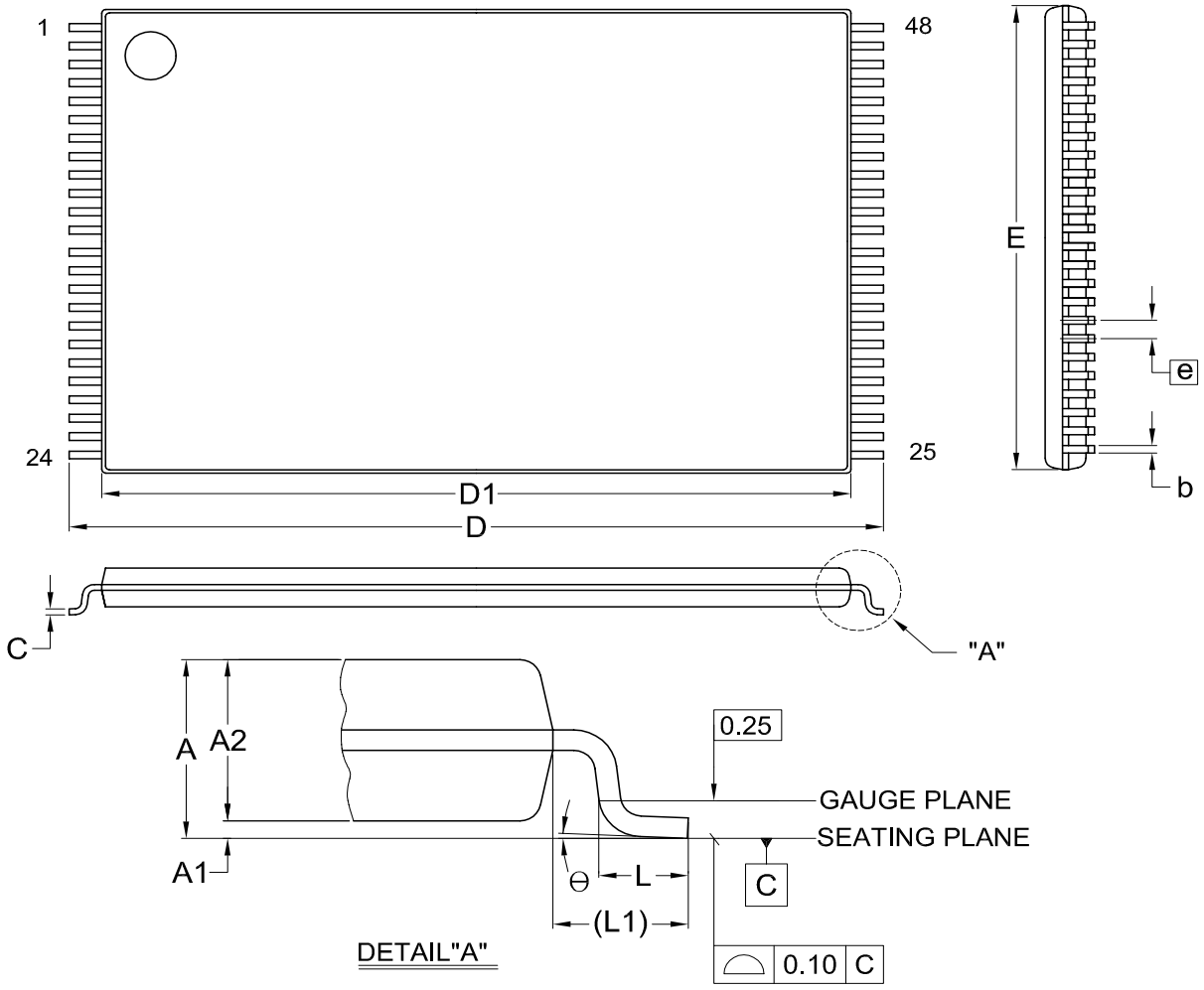




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# 10. PACKAGE INFORMATION

**Title:** Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM



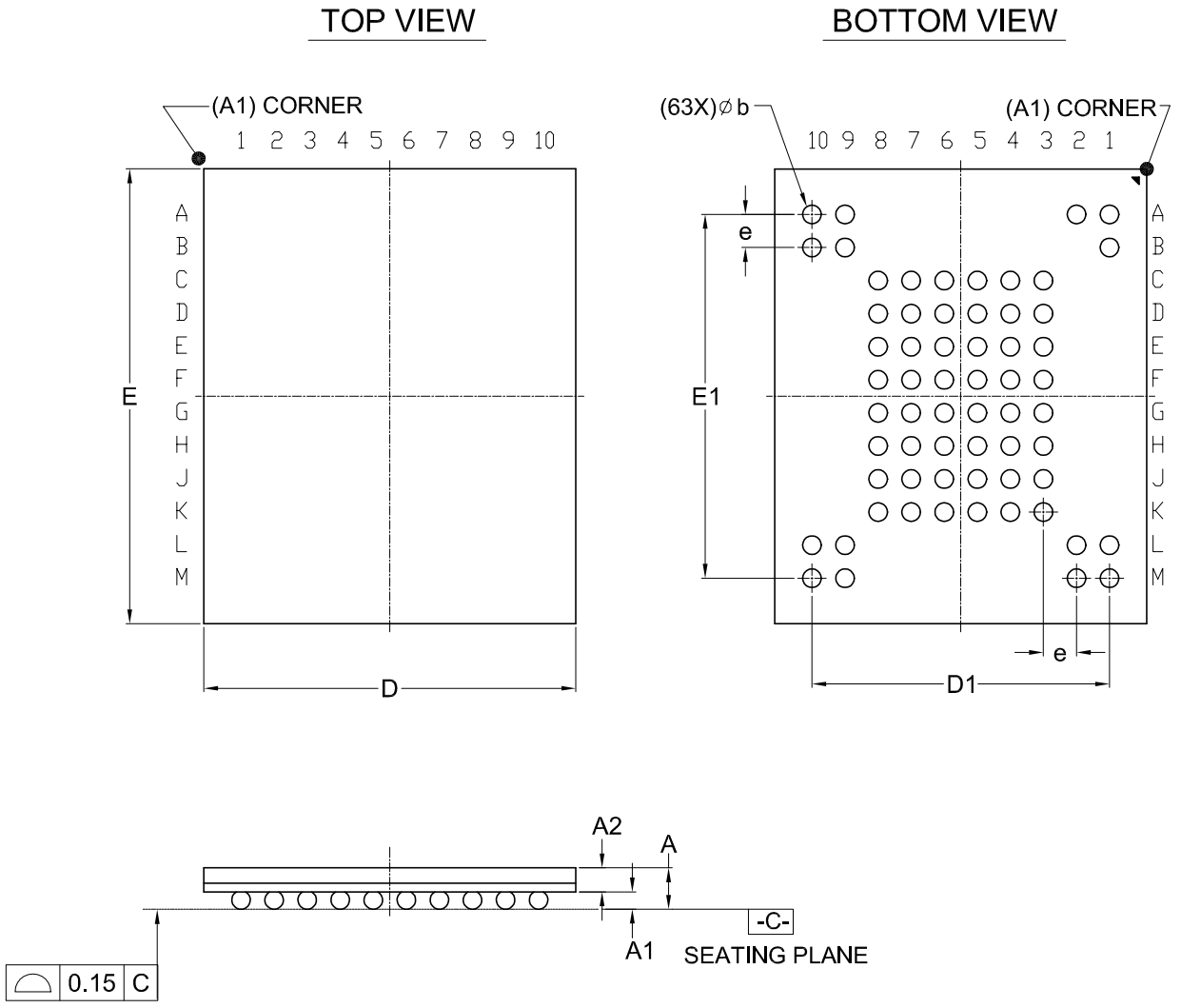

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | D1 | E | e | L | L1 | Θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | — | 0.05 | 0.95 | 0.17 | 0.10 | 19.80 | 18.30 | 11.90 | — | 0.50 | 0.70 | 0 |
| | Nom. | --- | 0.10 | 1.00 | 0.20 | 0.13 | 20.00 | 18.40 | 12.00 | 0.50 | 0.60 | 0.80 | 5 |
| | Max. | 1.20 | 0.15 | 1.05 | 0.27 | 0.21 | 20.20 | 18.50 | 12.10 | — | 0.70 | 0.90 | 8 |
| Inch | Min. | --- | 0.002 | 0.037 | 0.007 | 0.004 | 0.780 | 0.720 | 0.469 | — | 0.020 | 0.028 | 0 |
| | Nom. | --- | 0.004 | 0.039 | 0.008 | 0.005 | 0.787 | 0.724 | 0.472 | 0.020 | 0.024 | 0.031 | 5 |
| | Max. | 0.047 | 0.006 | 0.041 | 0.011 | 0.008 | 0.795 | 0.728 | 0.476 | — | 0.028 | 0.035 | 8 |

| DWG.NO. | REVISION | REFERENCE | | | ISSUE DATE |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-1607 | 8 | MO-142 | | | 2007/08/03 |


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**Title:** Package Outline for 63-VFBGA (9x11x1.0mm, Ball-pitch: 0.8mm, Ball-diameter: 0.45mm)




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.25 | 0.55 | 0.40 | 8.90 | --- | 10.90 | — | — |
| | Nom. | --- | 0.30 | — | 0.45 | 9.00 | 7.20 | 11.00 | 8.80 | 0.80 |
| | Max. | 1.00 | 0.40 | — | 0.50 | 9.10 | --- | 11.10 | — | — |
| Inch | Min. | --- | 0.010 | 0.022 | 0.016 | 0.350 | --- | 0.429 | — | — |
| | Nom. | --- | 0.012 | — | 0.018 | 0.354 | 0.283 | 0.433 | 0.346 | 0.031 |
| | Max. | 0.039 | 0.016 | — | 0.020 | 0.358 | --- | 0.437 | — | — |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-4267 | 0 | | | | |


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# 11. REVISION HISTORY

| Rev. No. | Descriptions | Page | Date |
|---|---|---|---|
| 0.01 | 1. Corrected the value of byte#6-9 of ONFI parameter page | P42 | SEP/04/2014 |
| | 2. Revised the IO3 of feature address 90h from "x" to "reserved (0)" | P46 | |
| | 3. Revised the typical spec of tCBSY from 3us to 5us and tRCBSY from 2us to 3.5us | P57 | |
| 0.02 | 1. Revised title of "Advanced Information" to "Preliminary" | ALL | DEC/30/2014 |
| | 2. Corrected tALS timing waveform as ALE high till WE# high | P25,53 | |
| | 3. Added Figure 33 PT Pin and Block Protection Mode Operation | P55 | |
| | 4. ICC1/ICC2 (typical) are improved from 20mA to 15mA | P57 | |
| | 5. Revised the bad block mark from non-FFh to 00h, also revised the page of bad block mark from 1st or 2nd page to 1st and 2nd page | P66,67 | |
| 1.0 | 1. Removed "Preliminary" title | ALL | FEB/02/2015 |
| 1.1 | 1. Added negative overshoot/positive overshoot waveforms | P56 | JUN/30/2015 |
| 1.2 | 1. Added the tRST=5us for the device reset time from idle | P59 | MAY/27/2016 |
| | 2. Modification of the power-on/off sequence: supplement the CE# signal, supplement the WE# single waveform with WE#=0 without toggle during the power-on period. | P64 | |
| | 3. Modified wording of "at least 1K P/E(with ECC) "on block#0 | P66 | |


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