# MX29LV160D T/B

# DATASHEET

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## 16M-BIT [2M x 8 / 1M x 16] 3V SUPPLY FLASH MEMORY

## FEATURES

### GENERAL FEATURES

- Byte/Word mode switchable
  - 2,097,152 x8 / 1,048,576 x16
- Sector Structure
  - 16K-Byte x 1, 8K-Byte x 2, 32K-Byte x 1, 64K-Byte x 31
  - Provides sector protect function to prevent program or erase operation in the protected sector
  - Provides chip unprotect function to allow code changing
  - Provides temporary sector unprotect function for code changing in previously protected sector
- Power Supply Operation
  - Vcc 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to 1.5 x Vcc
- Low Vcc write inhibit : Vcc ≤ Vlko
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- **Functional compatible with MX29LV160C device**

### PERFORMANCE

- High Performance
  - Fast access time: 70ns
  - Word program time: 11us/word (typical)
  - Fast erase time: 0.7s/sector, 15s/chip (typical)
- Low Power Consumption
  - Low active read current: 5mA (typical) at 5MHz
  - Low standby current: 5uA (typical)
- Typical 100,000 erase/program cycle
- 20 years data retention

### SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

### HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC
  - Provide accelerated program capability

### PACKAGE

- 48-Pin TSOP
- 48-Ball CSP (TFBGA)
- 48-Ball WFBGA/XFLGA
- **All devices are RoHS Compliant**



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## GENERAL DESCRIPTION

MX29LV160DT/B is a 16Mbit flash memory that can be organized as 2Mbytes of 8 bits each or as 1Mwords of 16 bits each. These devices operate over a voltage range of 2.7V to 3.6V typically using a 3V power supply input. The memory array is divided into 32 equal 64 Kilo byte blocks. However, depending on the device being used as a Top-Boot or Bottom-Boot device. The outermost one sector at the top or at the bottom are respectively the boot blocks for this device.

The MX29LV160DT/B is offered in a 48-pin TSOP, 48-ball XFLGA/WFBGA and a 48-ball CSP(TFBGA) JEDEC standard package. These packages are offered in leaded, as well as lead-free versions that are compliant to the RoHS specifications. The software algorithm used for this device also adheres to the JEDEC standard for single power supply devices. These flash parts can be programmed in system or on commercially available EPROM/ Flash programmers.

Separate OE# and CE# (Output Enable and Chip Enable) signals are provided to simplify system design. When used with high speed processors, the 70ns read access time of this flash memory permits operation with minimal time lost due to system timing delays.

The automatic write algorithm provided on Macronix flash memories perform an automatic erase prior to write. The user only needs to provide a write command to the command register. The on-chip state machine automatically controls the program and erase functions including all necessary internal timings. Since erase and write operations take much longer time than read operations, erase/write can be interrupted to perform read operations in other sectors of the device. For this, Erase Suspend operation along with Erase Resume operation are provided. Data# polling or Toggle bits are used to indicate the end of the erase/write operation.

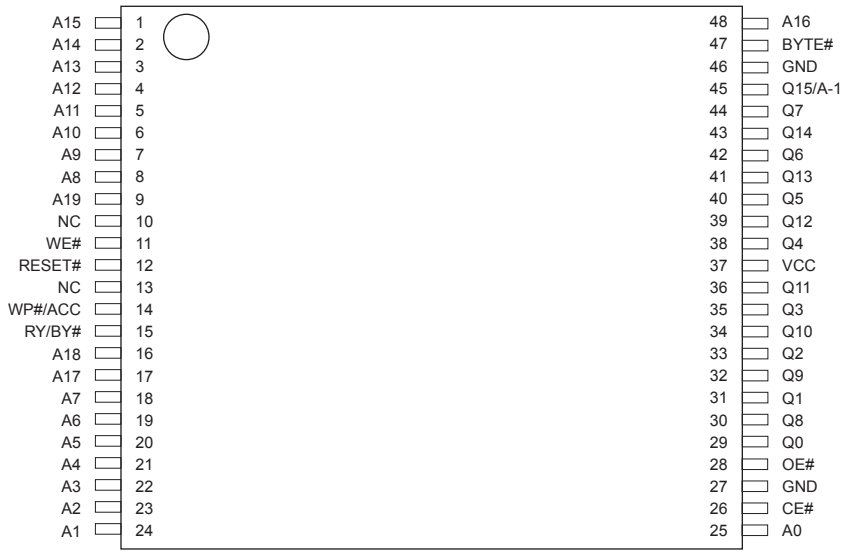
These devices are manufactured at the Macronix fabrication facility using the time tested and proven Macronix's advance technology. This proprietary non-epi process provides a very high degree of latch-up protection for stresses up to 100 milliamperes on address and data pins from -1V to 1.5xVCC.

With low power consumption and enhanced hardware and software features, this flash memory retains data reliably for at least twenty years. Erase and programming functions have been tested to meet a typical specification of 100,000 cycles of operation.

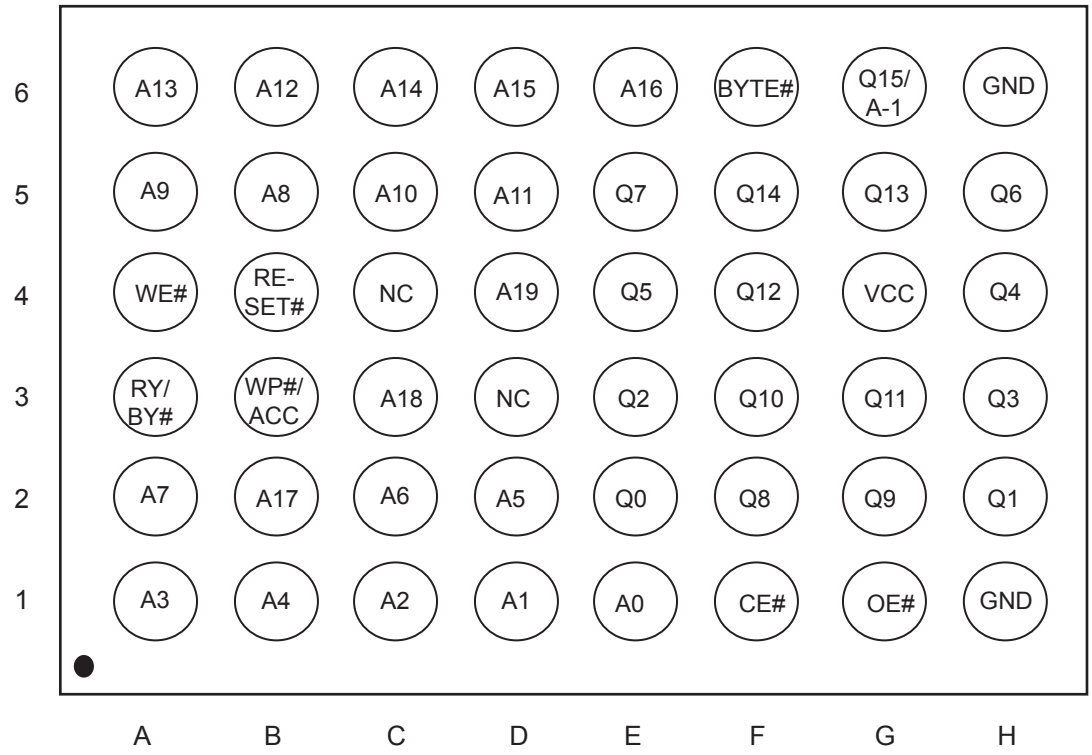

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## PIN CONFIGURATIONS

### 48 TSOP (Standard Type) (12mm x 20mm)



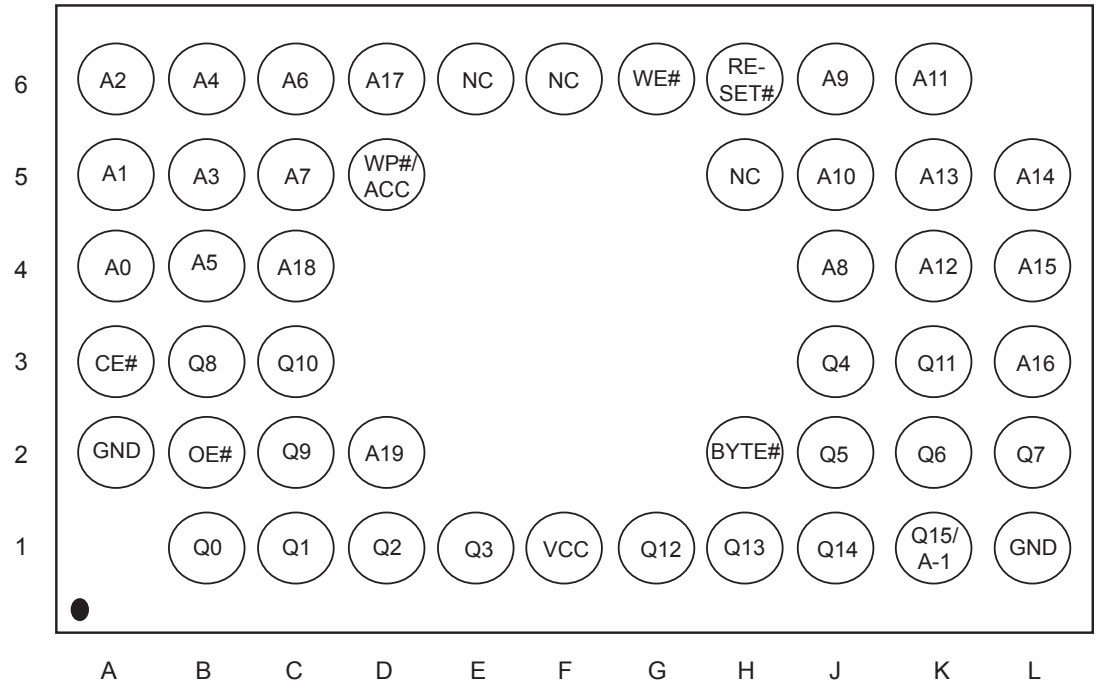

### 48-Ball CSP(TFBGA/LFBGA) (Ball Pitch = 0.8 mm, Top View, Balls Facing Down, 6 x 8 mm)



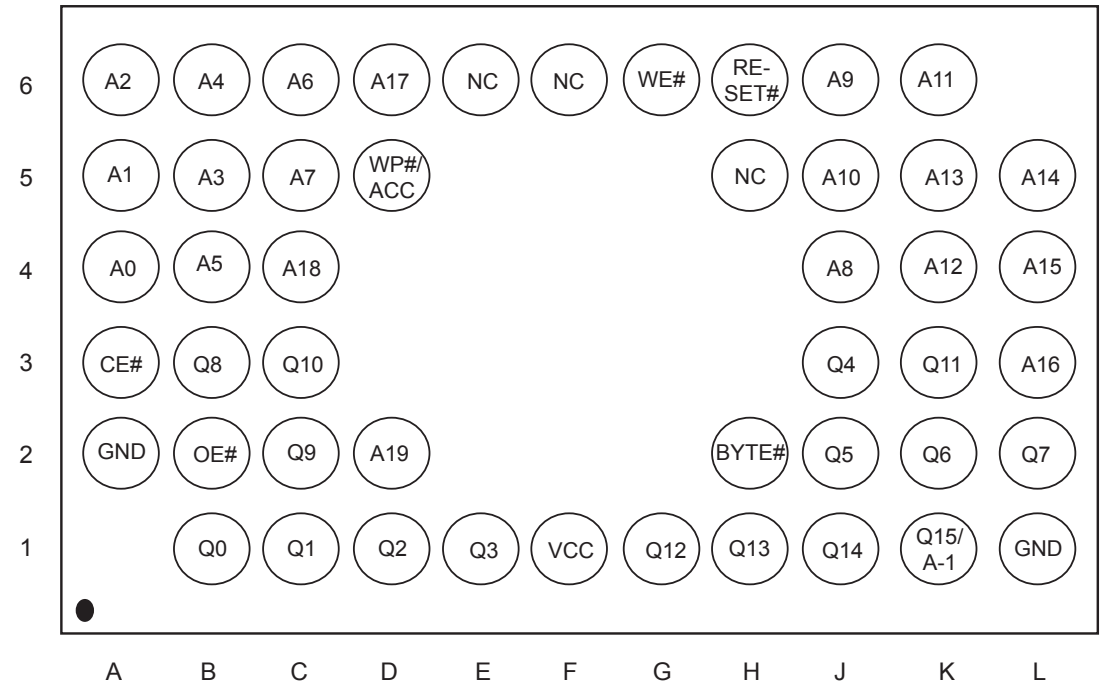


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**48-Ball WFBGA (Balls Facing Down, 4 x 6 x 0.75 mm)**




**48-Ball XFLGA (Balls Facing Down, 4 x 6 x 0.5 mm)**





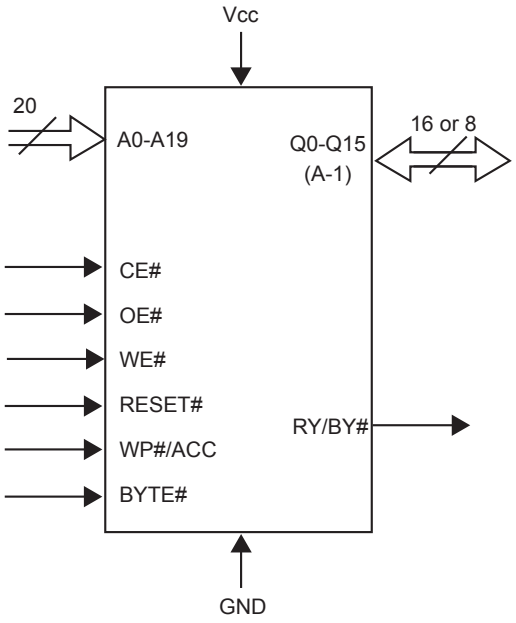
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## PIN DESCRIPTION

| SYMBOL | PIN NAME |
|---|---|
| A0~A19 | Address Input |
| Q0~Q14 | Data Input/Output |
| Q15/A-1 | Q15(Word mode)/LSB addr(Byte mode) |
| CE# | Chip Enable Input |
| WE# | Write Enable Input |
| BYTE# | Word/Byte Selection input |
| RESET# | Hardware Reset Pin/Sector Protect Unlock |
| OE# | Output Enable Input |
| RY/BY# | Ready/Busy Output |
| VCC | Power Supply Pin (2.7V~3.6V) |
| GND | Ground Pin |
| WP#/ACC | Hardware write Protect/Acceleration Pin |
| NC | Pin Not Connected Internally |

Note: If customer does not need WP#/ACC feature please connect WP#/ACC pin to VCC or let it floating. The WP#/ACC has an internal pull-up when unconnected WP#/ACC is at Vih.

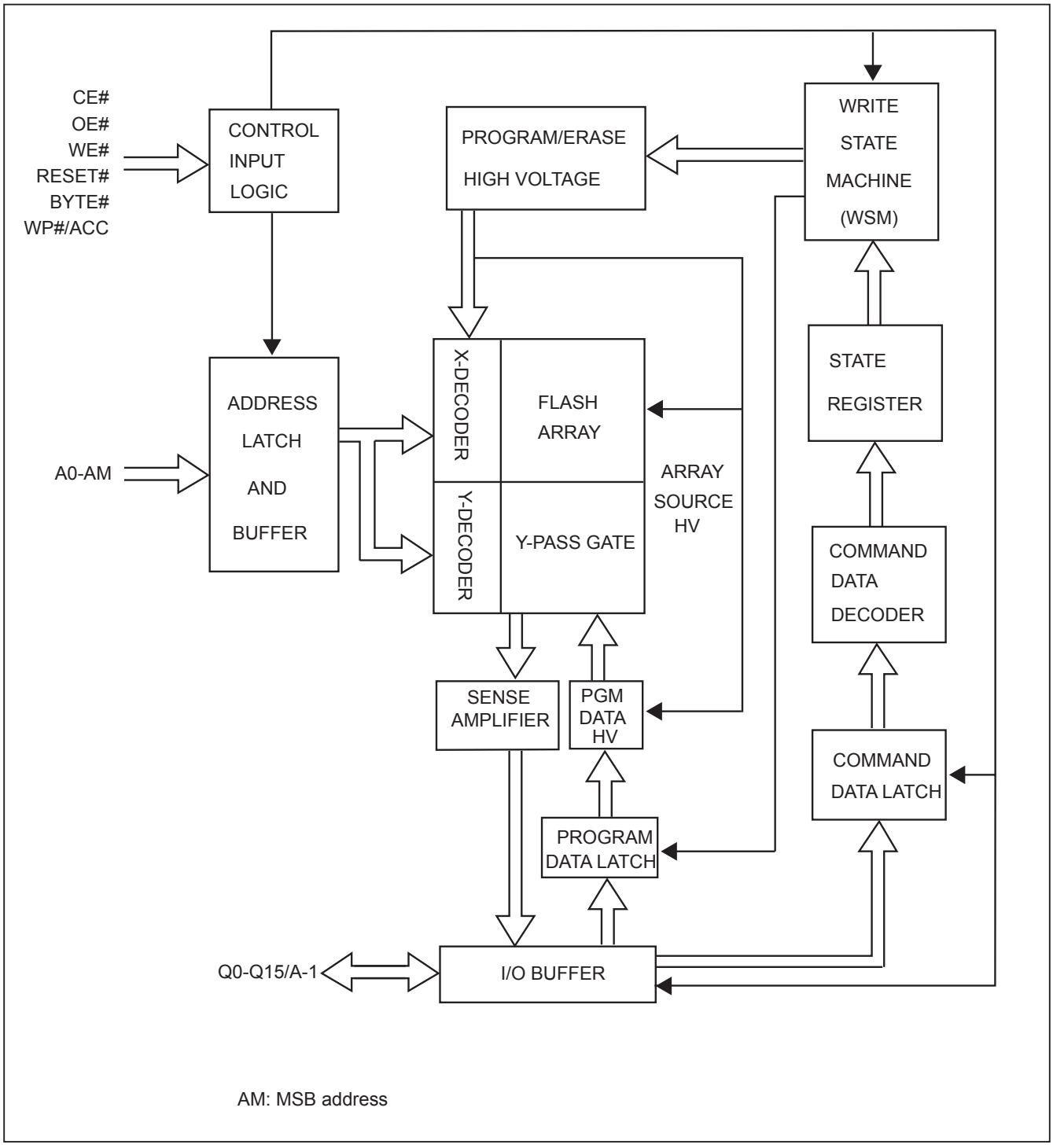
## LOGIC SYMBOL





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## BLOCK DIAGRAM





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## BLOCK DIAGRAM DESCRIPTION

The block diagram on Page 10 illustrates a simplified architecture of MX29LV160D T/B. Each block in the block diagram represents one or more circuit modules in the real chip used to access, erase, program, and read the memory array..

The "CONTROL INPUT LOGIC" block receives input pins CE#, OE#, WE#, RESET#, BYTE# and WP#/ACC. It creates internal timing control signals according to the input pins and outputs to the "ADDRESS LATCH AND BUFFER" to latch the external address pins A0-AM(A19). The internal addresses are output from this block to the main array and decoders composed of "X-DECODER", "Y-DECODER", "Y-PASS GATE", and "FLASH ARRAY". The X-DECODER decodes the word-lines of the flash array, while the Y-DECODER decodes the bit-lines of the flash array. The bit lines are electrically connected to the "SENSE AMPLIFIER" and "PGM DATA HV" selectively through the y-pass gates. Sense amplifiers are used to read out the contents of the flash memory, while the "PGM DATA HV" block is used to selectively deliver high power to bit-lines during programming. The "I/O BUFFER" controls the input and output on the Q0-Q15/A-1 pads. During read operation, the I/O buffer receives data from sense amplifiers and drives the output pads accordingly. In the last cycle of program command, the I/O buffer transmits the data on Q0-Q15/A-1 to "PROGRAM DATA LATCH", which controls the high power drivers in "PGM DATA HV" to selectively program the bits in a word or byte according to the user input pattern.

The "PROGRAM/ERASE HIGH VOLTAGE" block comprises the circuits to generate and deliver the necessary high voltage to the X-DECODER flash array, and "PGM DATA HV" block. The logic control module comprises of the "WRITE STATE MACHINE(WSM)", "STATE REGISTER", "COMMAND DATA DECODER", and "COMMAND DATA LATCH". When the user issues a command by toggling WE#, the command on Q0-A15/A-1 is latched in the command data latch and is decoded by the command data decoder. The state register receives the command and records the current state of the device. The WSM implements the internal algorithms for program or erase according to the current command state by controlling each block in the block diagram.


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## BLOCK STRUCTURE

The main flash memory array can be organized as 2M Bytes x 8 or as 1M Words x 16. The details of the address ranges and the corresponding sector addresses are shown in Table 1. Table 1.a shows the sector architecture for the Top Boot part, whereas Table 1.b shows the sector architecture for the Bottom Boot part. The specific security sector addresses are shown at the bottom off each of these tables.

**Table 1-1. MX29LV160DT SECTOR ARCHITECTURE**

| Sector Size | | Sector | Sector Address A19-A12 | Address Range | |
|---|---|---|---|---|---|
| Byte Mode (Kbytes) | Word Mode (Kwords) | | | Byte Mode (x8) | Word Mode (x16) |
| 64 | 32 | SA0 | 00000xxx | 000000h-00FFFFh | 000000h-07FFFh |
| 64 | 32 | SA1 | 00001xxx | 010000h-01FFFFh | 008000h-0FFFFh |
| 64 | 32 | SA2 | 00010xxx | 020000h-02FFFFh | 010000h-17FFFh |
| 64 | 32 | SA3 | 00011xxx | 030000h-03FFFFh | 018000h-01FFFFh |
| 64 | 32 | SA4 | 00100xxx | 040000h-04FFFFh | 020000h-027FFFh |
| 64 | 32 | SA5 | 00101xxx | 050000h-05FFFFh | 028000h-02FFFFh |
| 64 | 32 | SA6 | 00110xxx | 060000h-06FFFFh | 030000h-037FFFh |
| 64 | 32 | SA7 | 00111xxx | 070000h-07FFFFh | 038000h-03FFFFh |
| 64 | 32 | SA8 | 01000xxx | 080000h-08FFFFh | 040000h-047FFFh |
| 64 | 32 | SA9 | 01001xxx | 090000h-09FFFFh | 048000h-04FFFFh |
| 64 | 32 | SA10 | 01010xxx | 0A0000h-0AFFFFh | 050000h-057FFFh |
| 64 | 32 | SA11 | 01011xxx | 0B0000h-0BFFFFh | 058000h-05FFFFh |
| 64 | 32 | SA12 | 01100xxx | 0C0000h-0CFFFFh | 060000h-067FFFh |
| 64 | 32 | SA13 | 01101xxx | 0D0000h-0DFFFFh | 068000h-06FFFFh |
| 64 | 32 | SA14 | 01110xxx | 0E0000h-0EFFFFh | 070000h-077FFFh |
| 64 | 32 | SA15 | 01111xxx | 0F0000h-0FFFFFh | 078000h-07FFFFh |
| 64 | 32 | SA16 | 10000xxx | 100000h-10FFFFh | 080000h-087FFFh |
| 64 | 32 | SA17 | 10001xxx | 110000h-11FFFFh | 088000h-08FFFFh |
| 64 | 32 | SA18 | 10010xxx | 120000h-12FFFFh | 090000h-097FFFh |
| 64 | 32 | SA19 | 10011xxx | 130000h-13FFFFh | 098000h-09FFFFh |
| 64 | 32 | SA20 | 10100xxx | 140000h-14FFFFh | 0A0000h-0A7FFFh |
| 64 | 32 | SA21 | 10101xxx | 150000h-15FFFFh | 0A8000h-0AFFFFh |
| 64 | 32 | SA22 | 10110xxx | 160000h-16FFFFh | 0B0000h-0B7FFFh |
| 64 | 32 | SA23 | 10111xxx | 170000h-17FFFFh | 0B8000h-0BFFFFh |
| 64 | 32 | SA24 | 11000xxx | 180000h-18FFFFh | 0C0000h-0C7FFFh |
| 64 | 32 | SA25 | 11001xxx | 190000h-19FFFFh | 0C8000h-0CFFFFh |
| 64 | 32 | SA26 | 11010xxx | 1A0000h-1AFFFFh | 0D0000h-0D7FFFh |
| 64 | 32 | SA27 | 11011xxx | 1B0000h-1BFFFFh | 0D8000h-0DFFFFh |
| 64 | 32 | SA28 | 11100xxx | 1C0000h-1CFFFFh | 0E0000h-0E7FFFh |
| 64 | 32 | SA29 | 11101xxx | 1D0000h-1DFFFFh | 0E8000h-0EFFFFh |
| 64 | 32 | SA30 | 11110xxx | 1E0000h-1EFFFFh | 0F0000h-0F7FFFh |
| 32 | 16 | SA31 | 111110xx | 1F0000h-1F7FFFh | 0F8000h-0FBFFFh |
| 8 | 4 | SA32 | 11111100 | 1F8000h-1F9FFFh | 0FC000h-0FCFFFh |
| 8 | 4 | SA33 | 11111101 | 1FA000h-1FBFFFh | 0FD000h-0FDFFFh |
| 16 | 8 | SA34 | 1111111x | 1FC000h-1FFFFFh | 0FE000h-0FFFFFh |


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**Table 1-2. MX29LV160DB SECTOR ARCHITECTURE**

| Sector Size | | Sector | Sector Address A19-A12 | Address Range | |
|---|---|---|---|---|---|
| Byte Mode (Kbytes) | Word Mode (Kwords) | | | Byte Mode (x8) | Word Mode (x16) |
| 16 | 8 | SA0 | 0000000x | 000000h-003FFFh | 000000h-001FFFh |
| 8 | 4 | SA1 | 00000010 | 004000h-005FFFh | 002000h-002FFFh |
| 8 | 4 | SA2 | 00000011 | 006000h-007FFFh | 003000h-003FFFh |
| 32 | 16 | SA3 | 000001xx | 008000h-00FFFFh | 004000h-007FFFh |
| 64 | 32 | SA4 | 00001xxx | 010000h-01FFFFh | 008000h-00FFFFh |
| 64 | 32 | SA5 | 00010xxx | 020000h-02FFFFh | 010000h-017FFFh |
| 64 | 32 | SA6 | 00011xxx | 030000h-03FFFFh | 018000h-01FFFFh |
| 64 | 32 | SA7 | 00100xxx | 040000h-04FFFFh | 020000h-027FFFh |
| 64 | 32 | SA8 | 00101xxx | 050000h-05FFFFh | 028000h-02FFFFh |
| 64 | 32 | SA9 | 00110xxx | 060000h-06FFFFh | 030000h-037FFFh |
| 64 | 32 | SA10 | 00111xxx | 070000h-07FFFFh | 038000h-03FFFFh |
| 64 | 32 | SA11 | 01000xxx | 080000h-08FFFFh | 040000h-047FFFh |
| 64 | 32 | SA12 | 01001xxx | 090000h-09FFFFh | 048000h-04FFFFh |
| 64 | 32 | SA13 | 01010xxx | 0A0000h-0AFFFFh | 050000h-057FFFh |
| 64 | 32 | SA14 | 01011xxx | 0B0000h-0BFFFFh | 058000h-05FFFFh |
| 64 | 32 | SA15 | 01100xxx | 0C0000h-0CFFFFh | 060000h-067FFFh |
| 64 | 32 | SA16 | 01101xxx | 0D0000h-0DFFFFh | 068000h-06FFFFh |
| 64 | 32 | SA17 | 01110xxx | 0E0000h-0EFFFFh | 070000h-077FFFh |
| 64 | 32 | SA18 | 01111xxx | 0F0000h-0FFFFFh | 078000h-07FFFFh |
| 64 | 32 | SA19 | 10000xxx | 100000h-10FFFFh | 080000h-087FFFh |
| 64 | 32 | SA20 | 10001xxx | 110000h-11FFFFh | 088000h-08FFFFh |
| 64 | 32 | SA21 | 10010xxx | 120000h-12FFFFh | 090000h-097FFFh |
| 64 | 32 | SA22 | 10011xxx | 130000h-13FFFFh | 098000h-09FFFFh |
| 64 | 32 | SA23 | 10100xxx | 140000h-14FFFFh | 0A0000h-0A7FFFh |
| 64 | 32 | SA24 | 10101xxx | 150000h-15FFFFh | 0A8000h-0AFFFFh |
| 64 | 32 | SA25 | 10110xxx | 160000h-16FFFFh | 0B0000h-0B7FFFh |
| 64 | 32 | SA26 | 10111xxx | 170000h-17FFFFh | 0B8000h-0BFFFFh |
| 64 | 32 | SA27 | 11000xxx | 180000h-18FFFFh | 0C0000h-0C7FFFh |
| 64 | 32 | SA28 | 11001xxx | 190000h-19FFFFh | 0C8000h-0CFFFFh |
| 64 | 32 | SA29 | 11010xxx | 1A0000h-1AFFFFh | 0D0000h-0D7FFFh |
| 64 | 32 | SA30 | 11011xxx | 1B0000h-1BFFFFh | 0D8000h-0DFFFFh |
| 64 | 32 | SA31 | 11100xxx | 1C0000h-1CFFFFh | 0E0000h-0E7FFFh |
| 64 | 32 | SA32 | 11101xxx | 1D0000h-1DFFFFh | 0E8000h-0EFFFFh |
| 64 | 32 | SA33 | 11110xxx | 1E0000h-1EFFFFh | 0F0000h-0F7FFFh |
| 64 | 32 | SA34 | 11111xxx | 1F0000h-1FFFFFh | 0F8000h-0FFFFFh |


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## BUS OPERATION

### Table 2-1. BUS OPERATION

| Mode Select | RE-SET# | CE# | WE# | OE# | Address | Data I/O Q7~Q0 | Byte# Vil Data (I/O) Q15~Q8 | Byte# Vih Data (I/O) Q15~Q8 | WP#/ ACC |
|---|---|---|---|---|---|---|---|---|---|
| Device Reset | L | X | X | X | X | HighZ | HighZ | HighZ | L/H |
| Standby Mode | Vcc ± 0.3V | Vcc± 0.3V | X | X | X | HighZ | HighZ | HighZ | H |
| Output Disable | H | L | H | H | X | HighZ | HighZ | HighZ | L/H |
| Read Mode | H | L | H | L | AIN | DOUT | Q8-Q14= HighZ, Q15=A-1 | DOUT | L/H |
| Write | H | L | L | H | AIN | DIN | | DIN | Note3 |
| Accelerate Program | H | L | L | H | AIN | DIN | | DIN | Vhv |
| Temporary Sector Unprotect | Vhv | X | X | X | AIN | DIN | HighZ | DIN | Note3 |
| Sector Protect (Note2) | Vhv | L | L | H | Sector Address, A6=L, A1=H, A0=L | DIN, DOUT | X | X | L/H |
| Chip Unprotect (Note2) | Vhv | L | L | H | Sector Address, A6=H, A1=H, A0=L | DIN, DOUT | X | X | Note3 |

Notes:
1. All sectors will be unprotected if WP#/ACC=Vhv.
2. The one outmost boot sector is protected if WP#/ACC=Vil.
3. When WP#/ACC = Vih, the protection conditions of the one outmost boot sector depend on previous protection conditions."Sector/Sector Block Protection and Unprotection" describes the protect and unprotect method.
4. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
5. In Word Mode (Byte#=Vih), the addresses are AM to A0.
   In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15).
6. AM: MSB of address.


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**Table 2-2. BUS OPERATION**

| Item | Control Input | | | AM to A12 | A11 to A10 | A9 | A8 to A7 | A6 | A5 to A2 | A1 | A0 | Q7 ~ Q0 | Q15 ~ Q8 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CE# | WE# | OE# | | | | | | | | | | |
| Sector Lock Status Verification | L | H | L | SA | x | $V_{hv}$ | x | L | x | H | L | 01h or 00h (Note 1) | x |
| Read Silicon ID Manufacturer Code | L | H | L | x | x | $V_{hv}$ | x | L | x | L | L | C2h | x |
| Read Silicon ID MX29LV160DT | L | H | L | x | x | $V_{hv}$ | x | L | x | L | H | C4h | 22h(Word) |
| | | | | | | | | | | | | | x (Byte) |
| Read Silicon ID MX29LV160DB | L | H | L | x | x | $V_{hv}$ | x | L | x | L | H | 49h | 22h(Word) |
| | | | | | | | | | | | | | x (Byte) |

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. AM: MSB of address.


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## FUNCTIONAL OPERATION DESCRIPTION

### WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CE# and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

### REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped temporarily after a period of time no more than Tready1 and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.

2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.


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## RESET# OPERATION

Driving RESET# pin low for a period more than Trp will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of Tready1 for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at GND±0.3V, the device consumes standby current(Isb).However, device draws larger current if RESET# pin is held at Vil but not within GND±0.3V.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read boot code from flash memory.

## SECTOR PROTECT OPERATION

When a sector is protected, program or erase operation will be disabled on that protected sector. MX29LV160D T/B provides two methods for sector protection.

Once the sector is protected, the sector remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at Vhv. Refer to temporary sector unprotect operation for further details.

The first method is by applying Vhv on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for the algorithm for this method.

The other method is asserting Vhv on A9 and OE# pins, with A6 and CE# at Vil. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

## CHIP UNPROTECT OPERATION

MX29LV160D T/B provides two methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sectors are unprotected when shipped from the factory.

The first method is by applying Vhv on RESET# pin. Refer to Figure 12 for timing diagram and Figure 14 for algorithm of the operation.

The other method is asserting Vhv on A9 and OE# pins, with A6 at Vih and CE# at Vil. The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

## HARDWARE WRITE PROTECT

By driving the WP#/ACC pin LOW, the outermost one boot sector is protected from all erase/program operations. If WP#/ACC is held HIGH (Vih to VCC), the one outermost sector revert to its previously protected/unprotected status.

## ACCELERATED PROGRAMMING OPERATION

By applying high voltage (Vhv) to the WP#/ACC pin, the device will enter the Accelerated Programming mode. This mode permits the system to skip the normal command unlock sequences and program byte/word locations directly. During accelerated programming, the current drawn from the WP#/ACC pin is no more than ICP1.


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## TEMPORARY SECTOR UNPROTECT OPERATION

System can apply RESET# pin at Vhv to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The devices returns to normal operation once Vhv is removed from RESET# pin and previously protected sectors are again protected.

## AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE#, A6 and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

## VERIFY SECTOR PROTECT STATUS OPERATION

MX29LV160D T/B provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires Vhv on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A12 to Am pins. If the read out data is 01h, the designated sector is protected. Oppositely, if the read out data is 00h, the designated sector is not protected.

## DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

## LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than Vlko. This prevents data from spuriously altered. The device automatically resets itself when Vcc is lower than Vlko and write cycles are ignored until Vcc is greater than Vlko. System must provide proper signals on control pins after Vcc is larger than Vlko to avoid unintentional program or erase operation

## WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.


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## LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

## POWER-UP SEQUENCE

Upon power up, MX29LV160D T/B is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

## POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

## POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.


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## COMMAND OPERATIONS

### TABLE 3. MX29LV160D T/B COMMAND DEFINITIONS

| Command | | Read Mode | Reset Mode | Automatic Select | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Manifacture ID | | Device ID | | Sector Protect Verify | |
| | | | | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | Addr | XXX | 555 | AAA | 555 | AAA | 555 | AAA |
| | Data | Data | F0 | AA | AA | AA | AA | AA | AA |
| 2nd Bus Cycle | Addr | | | 2AA | 555 | 2AA | 555 | 2AA | 555 |
| | Data | | | 55 | 55 | 55 | 55 | 55 | 55 |
| 3rd Bus Cycle | Addr | | | 555 | AAA | 555 | AAA | 555 | AAA |
| | Data | | | 90 | 90 | 90 | 90 | 90 | 90 |
| 4th Bus Cycle | Addr | | | X00 | X00 | X01 | X02 | (Sector)X02 | (Sector)X04 |
| | Data | | | C2h | C2h | ID | ID | 00/01 | 00/01 |
| 5th Bus Cycle | Addr | | | | | | | | |
| | Data | | | | | | | | |
| 6th Bus Cycle | Addr | | | | | | | | |
| | Data | | | | | | | | |

| Command | | Program | | Chip Erase | | Sector Erase | | CFI Read | | Erase Suspend | Erase Resume |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Byte/ Word | Byte/ Word |
| 1st Bus Cycle | Addr | 555 | AAA | 555 | AAA | 555 | AAA | 55 | AA | XXX | XXX |
| | Data | AA | AA | AA | AA | AA | AA | 98 | 98 | B0 | 30 |
| 2nd Bus Cycle | Addr | 2AA | 555 | 2AA | 555 | 2AA | 555 | | | | |
| | Data | 55 | 55 | 55 | 55 | 55 | 55 | | | | |
| 3rd Bus Cycle | Addr | 555 | AAA | 555 | AAA | 555 | AAA | | | | |
| | Data | A0 | A0 | 80 | 80 | 80 | 80 | | | | |
| 4th Bus Cycle | Addr | Addr | Addr | 555 | AAA | 555 | AAA | | | | |
| | Data | Data | Data | AA | AA | AA | AA | | | | |
| 5th Bus Cycle | Addr | | | 2AA | 555 | 2AA | 555 | | | | |
| | Data | | | 55 | 55 | 55 | 55 | | | | |
| 6th Bus Cycle | Addr | | | 555 | AAA | Sector | Sector | | | | |
| | Data | | | 10 | 10 | 30 | 30 | | | | |

Notes:
1. Device ID : MX29LV160DT: 22C4; MX29LV160DB: 2249.
2. For sector protect verify result, XX00h/00h means sector is not protected, XX01h/01h means sector has been protected.
3. Sector Protect command is valid during Vhv at RESET# pin, Vih at A1 pin and Vil at A0, A6 pins. The last Bus cyc is for protect verify.
4. It is not allowed to adopt any other code which is not in the above command definition table.


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## COMMAND OPERATIONS (cont'd)

### AUTOMATIC PROGRAMMING OF THE MEMORY ARRAY

The MX29LV160D T/B provides the user the ability to program the memory array in Byte mode or Word mode. As long as the users enters the correct cycle defined in the Table 3 (including 2 unlock cycles and the A0h program command), any byte or word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, the user only needs to enter the program command and data once.

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done by an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready1. When the embedded program algorithm is complete or the program operation is terminated by a hardware reset, the device will return to Read mode.

After the embedded program operation has begun, the user can check for completion by reading the following bits in the status register:

| Status | Q7 | Q6 | Q5 | RY/BY# *2 |
|---|---|---|---|---|
| In progress *3 | Q7# | Toggling | 0 | 0 |
| Finished | Q7 | Stop toggling | 0 | 1 |
| Exceed time limit | Q7# | Toggling | 1 | 0 |

*1: When an attempt is made to program a protected sector, the program operation will abort thus preventing any data changes in the protected sector. Q7 will output complement data and Q6 will toggle briefly (1us or less) before aborting and returning the device to Read mode.

*2: RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

*3: The status "in progress" means both program and erase-suspended program mode.

### ERASING THE MEMORY ARRAY

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. In the Sector Erase operation, one or more selected sectors may be erased simultaneously. In the Chip Erase operation, the complete memory array is erased except for any protected sectors.


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## COMMAND OPERATIONS (cont'd)

### SECTOR ERASE

The sector erase operation is used to clear data within a sector by returning all of its memory locations to the "1" state. It requires six command cycles to initiate the erase operation. The first two cycles are "unlock cycles", the third is a configuration cycle, the fourth and fifth are also "unlock cycles", and the sixth cycle is the Sector Erase command. After the sector erase command sequence has been issued, an internal 50us time-out counter is started. Until this counter reaches zero, additional sector addresses and Sector Erase commands may be issued thus allowing multiple sectors to be selected and erased simultaneously. After the 50us time-out counter has expired, no new commands will be accepted and the embedded sector erase operation will begin. Note that the 50us timer-out counter is restarted after every erase command sequence. If the user enters any command other than Sector Erase or Erase Suspend during the time-out period, the erase operation will abort and the device will return to Read mode.

After the embedded sector erase operation begins, all commands except Erase Suspend will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode.

The system can determine the status of the embedded sector erase operation by the following methods:

| Status | Q7 | Q6 | Q5 | Q3 (*1) | Q2 | RY/BY#(*2) |
|---|---|---|---|---|---|---|
| Time-out period | 0 | Toggling | 0 | 0 | Toggling | 0 |
| In progress | 0 | Toggling | 0 | 1 | Toggling | 0 |
| Finished | 1 | Stop toggling | 0 | 1 | 1 | 1 |
| Exceeded time limit | 0 | Toggling | 1 | 1 | Toggling | 0 |

Note :

*1.The Q3 status bit is the time-out indicator. When Q3=0, the time-out counter has not yet reached zero and a new Sector Erase command may be issued to specify the address of another sector to be erased. When Q3=1, the time-out counter has expired and the Sector Erase operation has already begun. Erase Suspend is the only valid command that may be issued once the embedded erase operation is underway.

*2. RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

*3. When an attempt is made to erase only protected sector(s), the program operation will abort thus preventing any data changes in the protected sector(s). Q7 will output its complement data and Q6 will toggle briefly (100us or less) before aborting and returning the device to Read mode. If unprotected sectors are also specified, however, they will be erased normally and the protected sector(s) will remain unchanged.

*4. Q2 is a localized indicator showing a specified sector is undergoing erase operation or not. Q2 toggles when user reads at addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode). When a sector has been completely erased, Q2 stops toggling at the sector even when the device is still in erase operation for remaining selected sectors. At that circumstance, Q2 will still toggle when device is read at any other sector that remains to be erased.


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## COMMAND OPERATIONS (cont'd)

### CHIP ERASE

The Chip Erase operation is used erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 6 write cycles to initiate the action. The first two cycles are "unlock" cycles, the third is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle initiates the chip erase operation.

During the chip erase operation, no other software commands will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase, the chip will automatically return to Read mode.

The system can determine the status of the embedded chip erase operation by the following methods:

| Status | Q7 | Q6 | Q5 | Q2 | RY/BY#*1 |
|---|---|---|---|---|---|
| In progress | 0 | Toggling | 0 | Toggling | 0 |
| Finished | 1 | Stop toggling | 0 | 1 | 1 |
| Exceed time limit | 0 | Toggling | 1 | Toggling | 0 |

*1: RY/BY# is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

### SECTOR ERASE SUSPEND

After beginning a sector erase operation, Erase Suspend is the only valid command that may be issued. If system issues an Erase Suspend command during the 50us time-out period following a Sector Erase command, the time-out period will terminate immediately and the device will enter Erase-Suspended Read mode. If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended Read mode until Tready1 time has elapsed. The system can determine if the device has entered the Erase-Suspended Read mode through Q6, Q7, and RY/BY#.

After the device has entered Erase-Suspended Read mode, the system can read or program any sector(s) except those being erased by the suspended erase operation. Reading any sector being erased or programmed will return the contents of the status register. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another erase command. The system can use the status register bits shown in the following table to determine the current state of the device:

| Status | Q7 | Q6 | Q5 | Q3 | Q2 | RY/BY# |
|---|---|---|---|---|---|---|
| Erase suspend read in erase suspended sector | 1 | No toggle | 0 | N/A | Toggle | 1 |
| Erase suspend read in non-erase suspended sector | Data | Data | Data | Data | Data | 1 |
| Erase suspend program in non-erase suspended sector | Q7# | Toggle | 0 | N/A | N/A | 0 |

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.


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## COMMAND OPERATIONS (cont'd)

### SECTOR ERASE RESUME

The sector Erase Resume command is valid only when the device is in Erase-Suspended Read mode. After erase resumes, the user can issue another Ease Suspend command, but there should be a 4ms interval between Ease Resume and the next Erase Suspend command. If the user enters an infinite suspend-resume loop, or suspend-resume exceeds 1024 times, erase times will increase dramatically.

### AUTOMATIC SELECT OPERATIONS

When the device is in Read mode, Erase-Suspended Read mode, or CFI mode, the user can issue the Automatic Select command shown in Table 3 (two unlock cycles followed by the Automatic Select command 90h) to enter Automatic Select mode. After entering Automatic Select mode, the user can query the Manufacturer ID, Device ID, Security Sector locked status, or Sector-Group protected status multiple times without issuing a new Automatic Select command.

While In Automatic Select mode, issuing a Reset command (F0h) will return the device to Read mode (or Ease-Suspended Read mode if Erase-Suspend was active).

Another way to enter Automatic Select mode is to use one of the bus operations shown in Table 2-2. BUS OPERATION. After the high voltage (Vhv) is removed from the A9 pin, the device will automatically return to Read mode or Erase-Suspended Read mode.

### AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

| | | Address (Hex) | Data (Hex) | Representation |
|---|---|---|---|---|
| Manufacturer ID | Word | X00 | 00C2 | |
| | Byte | X00 | C2 | |
| Device ID | Word | X01 | 22C4/2249 | Top/Bottom Boot Sector |
| | Byte | X02 | C4/49 | Top/Bottom Boot Sector |
| Sector Protect Verify | Word | (Sector address) X 02 | 0000/0001 | Unprotected/protected |
| | Byte | (Sector address) X 04 | 00/01 | Unprotected/protected |

After entering automatic select mode, no other commands are allowed except the reset command.


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## COMMAND OPERATIONS (cont'd)

### READ MANUFACTURER ID OR DEVICE ID

The Manufacturer ID (identification) is a unique hexadecimal number assigned to each manufacturer by the JEDEC committee. Each company has its own manufacturer ID, which is different from the ID of all other companies. The number assigned to Macronix is C2h.

The Device ID is a unique hexadecimal number assigned by the manufacturer for each one of the flash devices made by that manufacturer.

The above two ID types are stored in a 16-bit register on the flash device -- eight bits for each ID. This register is normally read by the user or by the programming machine to identify the manufacturer and the specific device.

After entering Automatic Select mode, performing a read operation with A1 & A0 held LOW will cause the device to output the Manufacturer ID on the Data I/O (Q7 to Q0) pins. Performing a read operation with A1 LOW and A0 HIGH will cause the device to output the Device ID.

### VERIFY SECTOR GROUP PROTECTION

After entering Automatic Select mode, performing a read operation with A1 held HIGH and A0 held LOW and the address of the sector to be checked applied to A19 to A12, data bit Q0 will indicate the protected status of the addressed sector. If Q0 is HIGH, the sector is protected. Conversely, if Q0 is LOW, the sector is unprotected.

### RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.


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## COMMON FLASH MEMORY INTERFACE (CFI) MODE

### QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV160D T/B features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h"/"AAh" (depending on Word/Byte mode), the device will enter the CFI Query Mode, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4.

Once user enters CFI query mode, user can not issue any other commands except reset command. The reset command is required to exit CFI mode and go back to the mode before entering CFI. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode.

**Table 4-1. CFI mode: Identification Data Values**
(All values in these tables are in hexadecimal)

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) |
|---|---|---|---|
| Query-unique ASCII string "QRY" | 10 | 20 | 0051 |
| | 11 | 22 | 0052 |
| | 12 | 24 | 0059 |
| Primary vendor command set and control interface ID code | 13 | 26 | 0002 |
| | 14 | 28 | 0000 |
| Address for primary algorithm extended query table | 15 | 2A | 0040 |
| | 16 | 2C | 0000 |
| Alternate vendor command set and control interface ID code | 17 | 2E | 0000 |
| | 18 | 30 | 0000 |
| Address for alternate algorithm extended query table | 19 | 32 | 0000 |
| | 1A | 34 | 0000 |

**Table 4-2. CFI Mode: System Interface Data Values**

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) |
|---|---|---|---|
| Vcc supply minimum program/erase voltage | 1B | 36 | 0027 |
| Vcc supply maximum program/erase voltage | 1C | 38 | 0036 |
| VPP supply minimum program/erase voltage | 1D | 3A | 0000 |
| VPP supply maximum program/erase voltage | 1E | 3C | 0000 |
| Typical timeout per single word/byte write, $2^n$ us | 1F | 3E | 0004 |
| Typical timeout for maximum-size buffer write, $2^n$ us | 20 | 40 | 0000 |
| Typical timeout per individual block erase, $2^n$ ms | 21 | 42 | 000A |
| Typical timeout for full chip erase, $2^n$ ms | 22 | 44 | 0000 |
| Maximum timeout for word/byte write, $2^n$ times typical | 23 | 46 | 0005 |
| Maximum timeout for buffer write, $2^n$ times typical | 24 | 48 | 0000 |
| Maximum timeout per individual block erase, $2^n$ times typical | 25 | 4A | 0004 |
| Maximum timeout for chip erase, $2^n$ times typical | 26 | 4C | 0000 |


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**Table 4-3. CFI Mode: Device Geometry Data Values**

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) |
|---|---|---|---|
| Device size = $2^n$ in number of bytes (MX29LV160D) | 27 | 4E | 0015 |
| Flash device interface description (02=asynchronous x8/x16) | 28 | 50 | 0002 |
| | 29 | 52 | 0000 |
| Maximum number of bytes in buffer write = $2^n$ (not support) | 2A | 54 | 0000 |
| | 2B | 56 | 0000 |
| Number of erase regions within device | 2C | 58 | 0004 |
| Index for Erase Bank Area 1<br>[2E,2D] = # of same-size sectors in region 1-1<br>[30, 2F] = sector size in multiples of 256-bytes | 2D | 5A | 0000 |
| | 2E | 5C | 0000 |
| | 2F | 5E | 0040 |
| | 30 | 60 | 0000 |
| Index for Erase Bank Area 2 | 31 | 62 | 0001 |
| | 32 | 64 | 0000 |
| | 33 | 66 | 0020 |
| | 34 | 68 | 0000 |
| Index for Erase Bank Area 3 | 35 | 6A | 0000 |
| | 36 | 6C | 0000 |
| | 37 | 6E | 0080 |
| | 38 | 70 | 0000 |
| Index for Erase Bank Area 4 (for MX29LV160D) | 39 | 72 | 001E |
| | 3A | 74 | 0000 |
| | 3B | 76 | 0000 |
| | 3C | 78 | 0001 |


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**Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values**

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) |
|---|---|---|---|
| Query - Primary extended table, unique ASCII string, PRI | 40 | 80 | 0050 |
| | 41 | 82 | 0052 |
| | 42 | 84 | 0049 |
| Major version number, ASCII | 43 | 86 | 0031 |
| Minor version number, ASCII | 44 | 88 | 0030 |
| Unlock recognizes address (0= recognize, 1= don't recognize) | 45 | 8A | 0000 |
| Erase suspend (2= to both read and program) | 46 | 8C | 0002 |
| Sector protect (N= # of sectors/group) | 47 | 8E | 0001 |
| Temporary sector unprotect (1=supported) | 48 | 90 | 0001 |
| Sector protect/Chip unprotect scheme | 49 | 92 | 0004 |
| Simultaneous R/W operation (0=not supported) | 4A | 94 | 0000 |
| Burst mode (0=not supported) | 4B | 96 | 0000 |
| Page mode (0=not supported) | 4C | 98 | 0000 |
| Minimum acceleration supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV | 4D | 9A | 00A5 |
| Maximum acceleration supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV | 4E | 9C | 00B5 |
| Top/Bottom boot block indicator<br>02h=bottom boot device 03h=top boot device | 4F | 9E | 0002/0003 |


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## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM STRESS RATINGS

| | | |
|---|---|---|
| Surrounding Temperature with Bias | | -65°C to +125°C |
| Storage Temperature | | -65°C to +150°C |
| Voltage Range | VCC | -0.5V to +4.0 V |
| | RESET#, A9 and OE# | -0.5V to +10.5 V |
| | The other pins | -0.5V to Vcc +0.5V |
| Output Short Circuit Current (less than one second) | | 200 mA |

Note:
1. Minimum voltage may undershoot to -2V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to Vcc+2V during transition and for less than 20ns during transitions.

### OPERATING TEMPERATURE AND VOLTAGE

| | | |
|---|---|---|
| **Commercial (C) Grade** | Surrounding Temperature ($T_A$) | 0°C to +70°C |
| **Industrial (I) Grade** | Surrounding Temperature ($T_A$) | -40°C to +85°C |
| **VCC Supply Voltages** | VCC range | +2.7 V to 3.6 V |

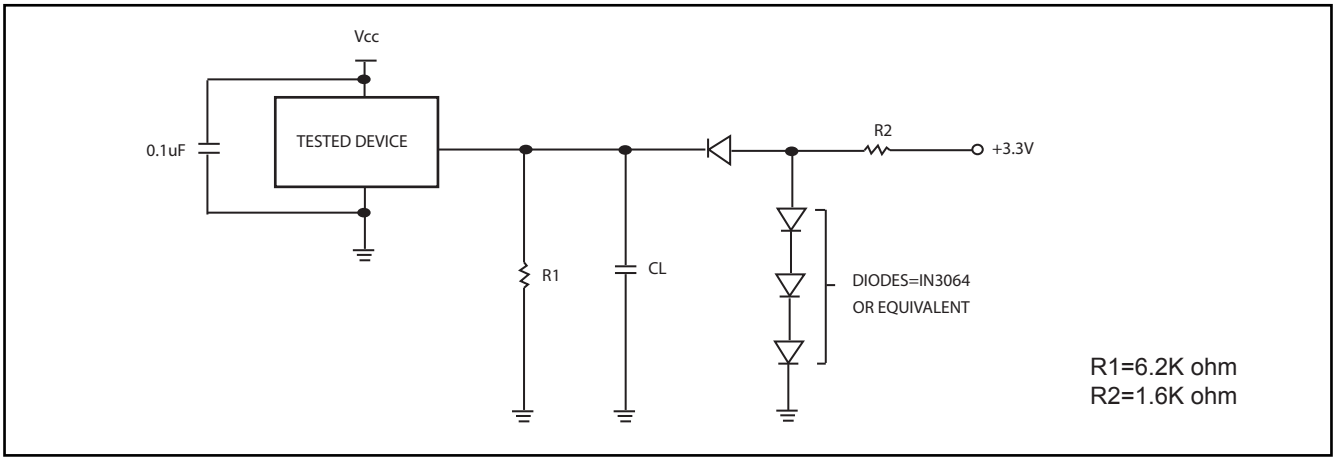

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## DC CHARACTERISTICS

| Symbol | Description | Min. | Typ. | Max. | Remark |
|---|---|---|---|---|---|
| Iilk | Input Leak | | | ± 1.0uA | |
| Iilk9 | A9 Leak | | | 35uA | A9=10.5V |
| Iolk | Output Leak | | | ± 1.0uA | |
| Icr1 | Read Current(5MHz) | | 5mA | 12mA | CE#=Vil, OE#=Vih |
| Icr2 | Read Current(1MHz) | | 2mA | 4mA | CE#=Vil, OE#=Vih |
| Icw | Write Current | | 15mA | 30mA | CE#=Vil, OE#=Vih, WE#=Vil |
| Isb | Standby Current | | 5uA | 15uA | Vcc=Vcc max, other pins disable |
| Isbr | Reset Current | | 5uA | 15uA | Vcc=Vccmax, Reset# enable, other pins disable |
| Isbs | Sleep Mode Current | | 5uA | 15uA | |
| Icp1 | Accelerated Pgm Current, WP#/Acc pin(Word/Byte) | | 5mA | 10mA | CE#=Vil, OE#=Vih |
| Icp2 | Accelerated Pgm Current, Vcc pin,(Word/Byte) | | 15mA | 30mA | CE#=Vil, OE#=Vih |
| Vil | Input Low Voltage | -0.5V | | 0.8V | |
| Vih | Input High Voltage | 0.7xVcc | | Vcc+0.3V | |
| Vhv | Very High Voltage for hardware Protect/Unprotect/Accelerated Program/Auto Select/Temporary Unprotect | 9.5V | | 10.5V | |
| Vol | Output Low Voltage | | | 0.45V | Iol=4.0mA |
| Voh1 | Ouput High Voltage | 0.85xVcc | | | Ioh1=-2mA |
| Voh2 | Ouput High Voltage | Vcc-0.4V | | | Ioh2=-100uA |
| Vlko | Low Vcc Lock-out Voltage | 2.3V | | 2.5V | |

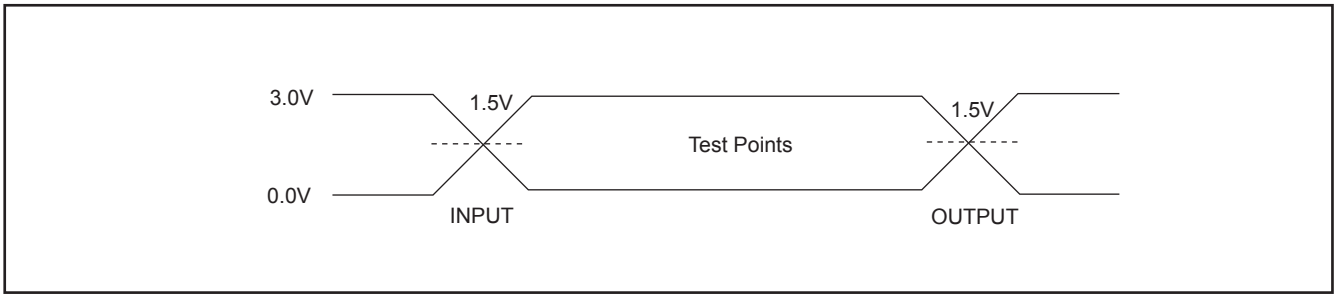

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## SWITCHING TEST CIRCUIT




Test Condition
Output Load : 1 TTL gate
Output Load Capacitance,CL : 30pF(70ns)/100pF(90ns)
Rise/Fall Times : 5ns
In/Out reference levels :1.5V

## SWITCHING TEST WAVEFORM





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## AC CHARACTERISTICS

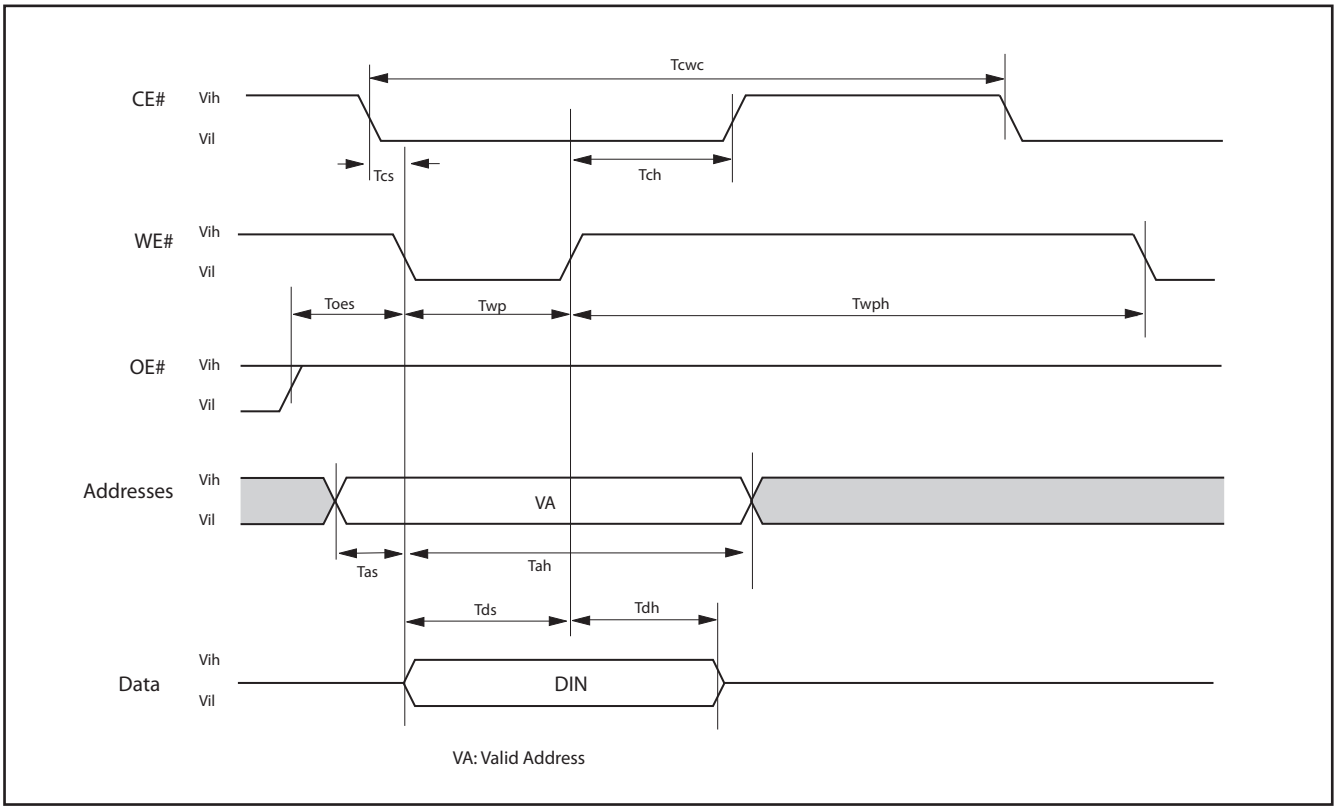
| Symbol | Description | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Taa | Valid data output after address | | | | 70 | ns |
| Tce | Valid data output after CE# low | | | | 70 | ns |
| Toe | Valid data output after OE# low | | | | 30 | ns |
| Tdf | Data output floating after OE# high or CE# high | | | | 30 | ns |
| Toh | Output hold time from the earliest rising edge of address, CE#, OE# | | 0 | | | ns |
| Trc | Read period time | | 70 | | | ns |
| Tsrw | Latency Between Read and Write Operation (*Note 1) | | 45 | | | ns |
| Twc | Write period time | | 70 | | | ns |
| Tcwc | Command write period time | | 70 | | | ns |
| Tas | Address setup time | | 0 | | | ns |
| Tah | Address hold time | | 45 | | | ns |
| Tds | Data setup time | | 35 | | | ns |
| Tdh | Data hold time | | 0 | | | ns |
| Tvcs | Vcc setup time | | 200 | | | us |
| Tcs | Chip enable Setup time | | 0 | | | ns |
| Tch | Chip enable hold time | | 0 | | | ns |
| Toes | Output enable setup time | | 0 | | | ns |
| Toeh | Output enable hold time | Read | 0 | | | ns |
| Toeh | | Toggle & Data# Polling | 10 | | | ns |
| Tws | WE# setup time | | 0 | | | ns |
| Twh | WE# hold time | | 0 | | | ns |
| Tcep | CE# pulse width | | 35 | | | ns |
| Tceph | CE# pulse width high | | 30 | | | ns |
| Twp | WE# pulse width | | 35 | | | ns |
| Twph | WE# pulse width high | | 30 | | | ns |
| Tbusy | Program/Erase active time by RY/BY# | | | | 90 | ns |
| Tghwl | Read recover time before write | | 0 | | | ns |
| Tghel | Read recover time before write | | 0 | | | ns |
| Twhwh1 | Program operation | Byte | | 9 | 300 | us |
| Twhwh1 | Program operation | Word | | 11 | 360 | us |
| Twhwh1 | Accelerated program operation | | | 7 | 210 | us |
| Twhwh2 | Sector Erase Operation | | | 0.7 | 2 | sec |
| Tbal | Sector Add hold time | | | | 50 | us |

* Note 1: Sampled only, not 100% tested.


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## WRITE COMMAND OPERATION

### Figure 1. COMMAND WRITE OPERATION

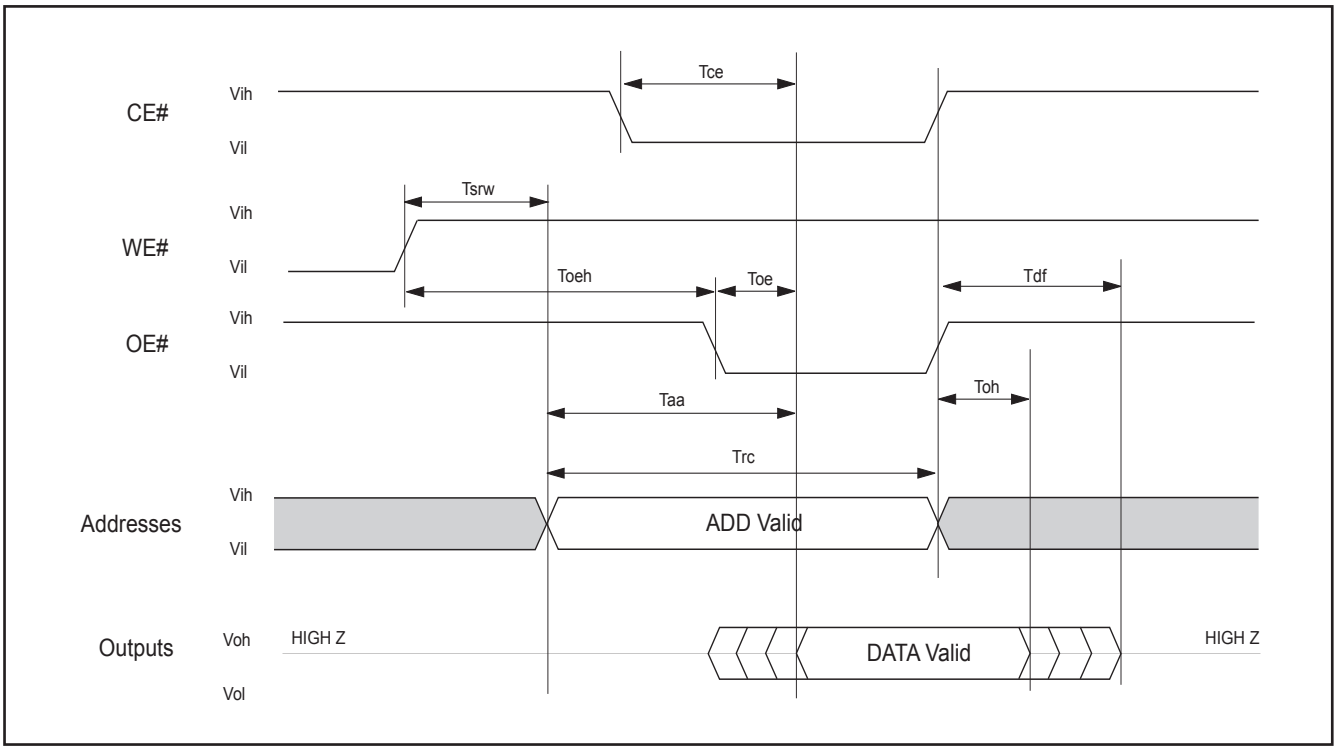




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## READ/RESET OPERATION

### Figure 2. READ TIMING WAVEFORM



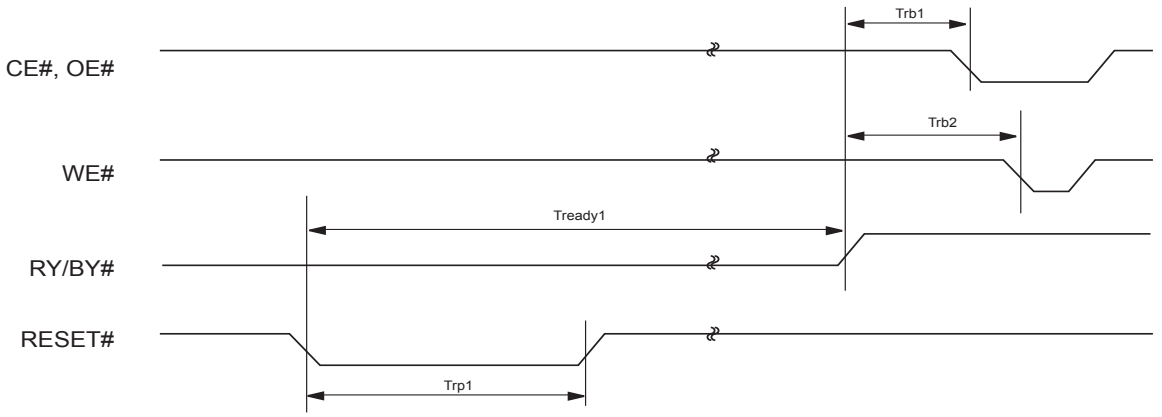


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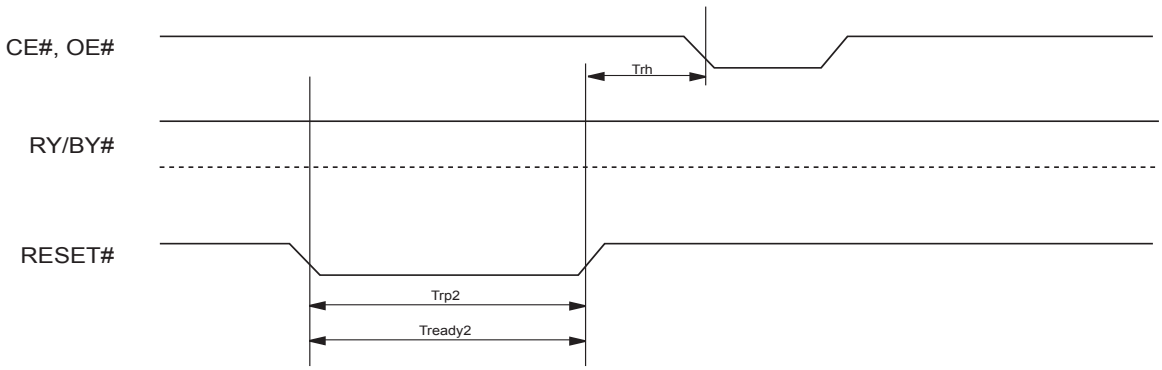
## AC CHARACTERISTICS

| Item | Description | Setup | Speed | Unit |
|---|---|---|---|---|
| Trp1 | RESET# Pulse Width (During Automatic Algorithms) | MIN | 10 | us |
| Trp2 | RESET# Pulse Width (NOT During Automatic Algorithms) | MIN | 500 | ns |
| Trh | RESET# High Time Before Read | MIN | 70 | ns |
| Trb1 | RY/BY# Recovery Time (to CE#, OE# go low) | MIN | 0 | ns |
| Trb2 | RY/BY# Recovery Time (to WE# go low) | MIN | 50 | ns |
| Tready1 | RESET# PIN Low (During Automatic Algorithms) to Read or Write | MAX | 20 | us |
| Tready2 | RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write | MAX | 500 | ns |

**Figure 3. RESET# TIMING WAVEFORM**




Reset Timing during Automatic Algorithms

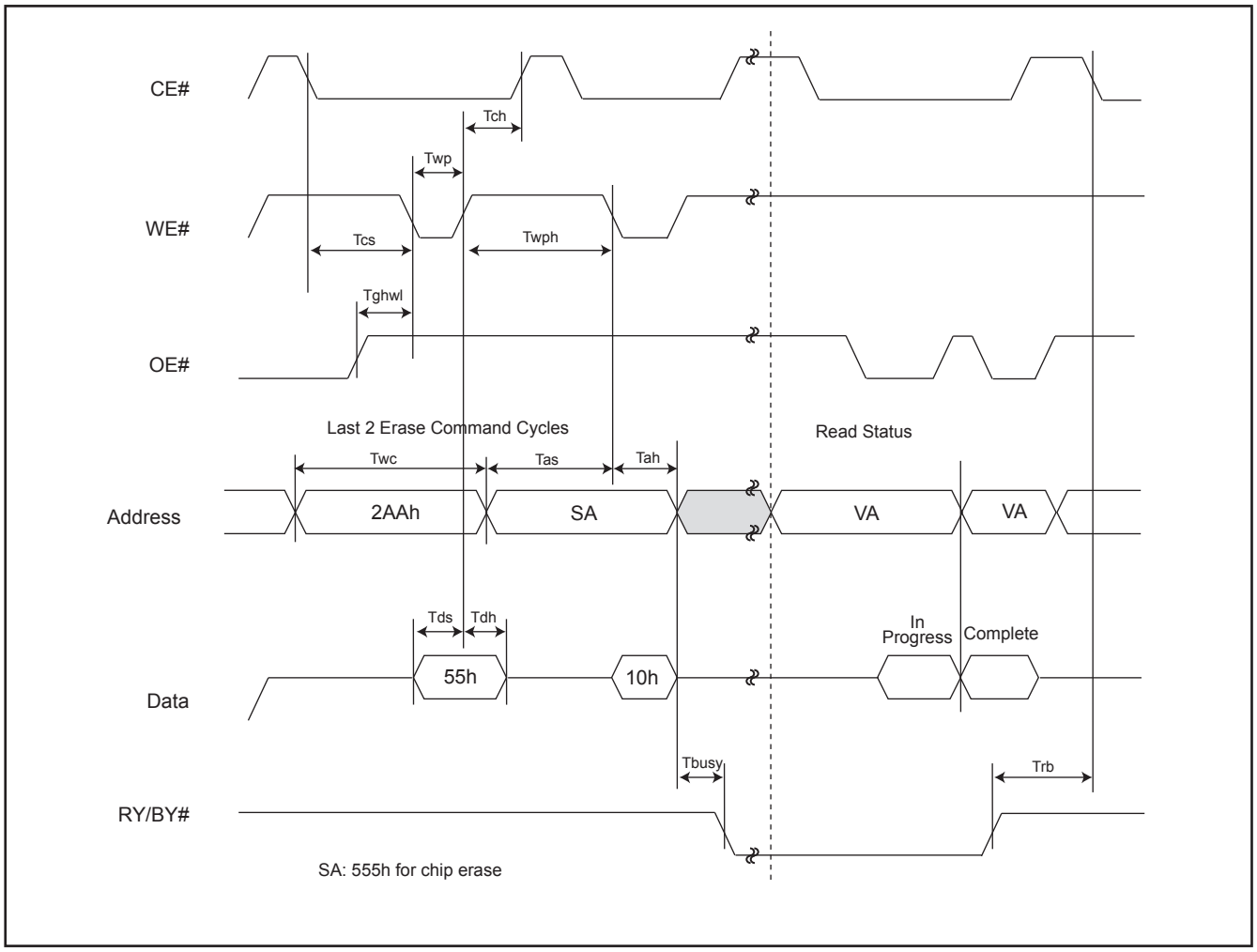



Reset Timing NOT during Automatic Algorithms


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## ERASE/PROGRAM OPERATION

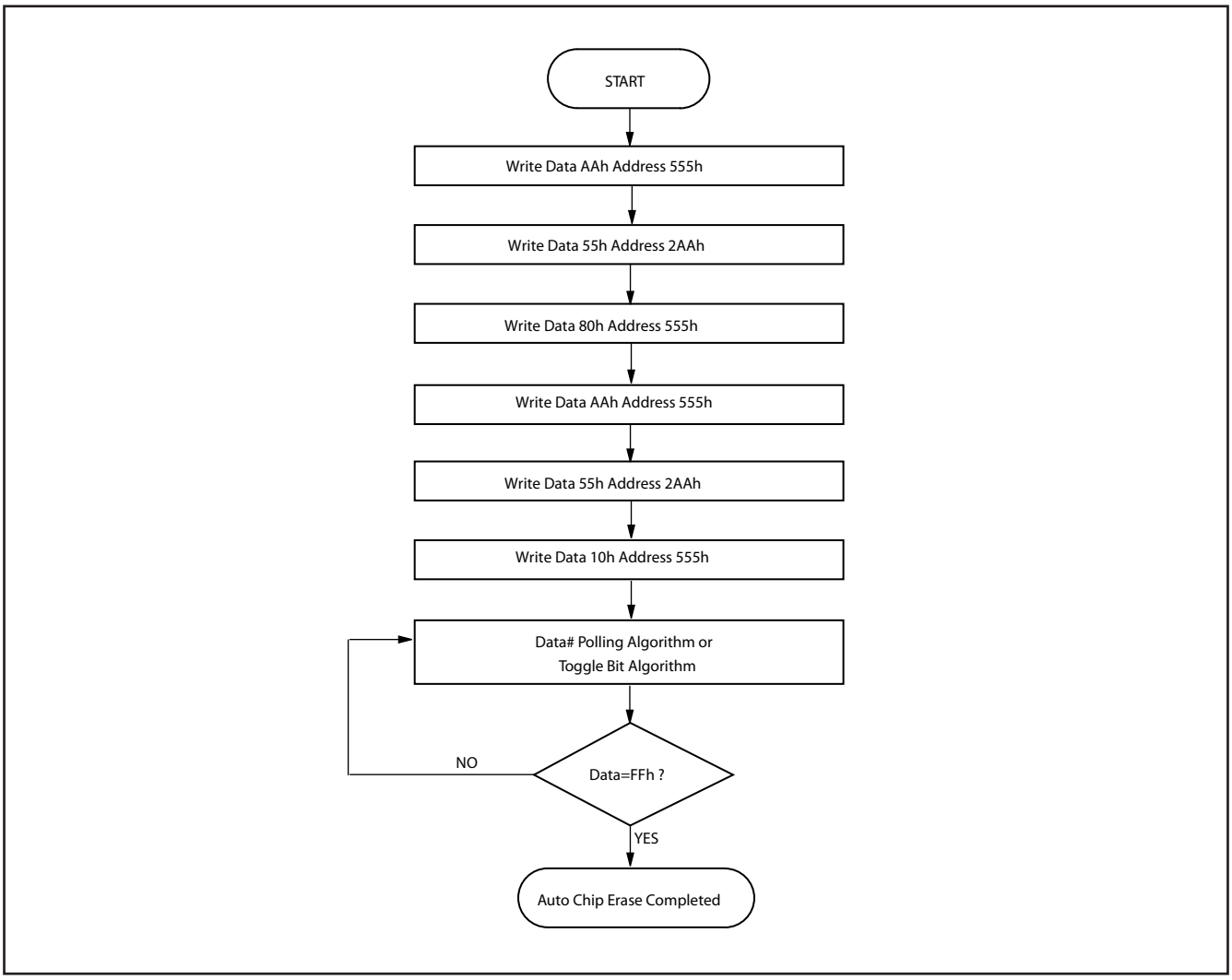
### Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM





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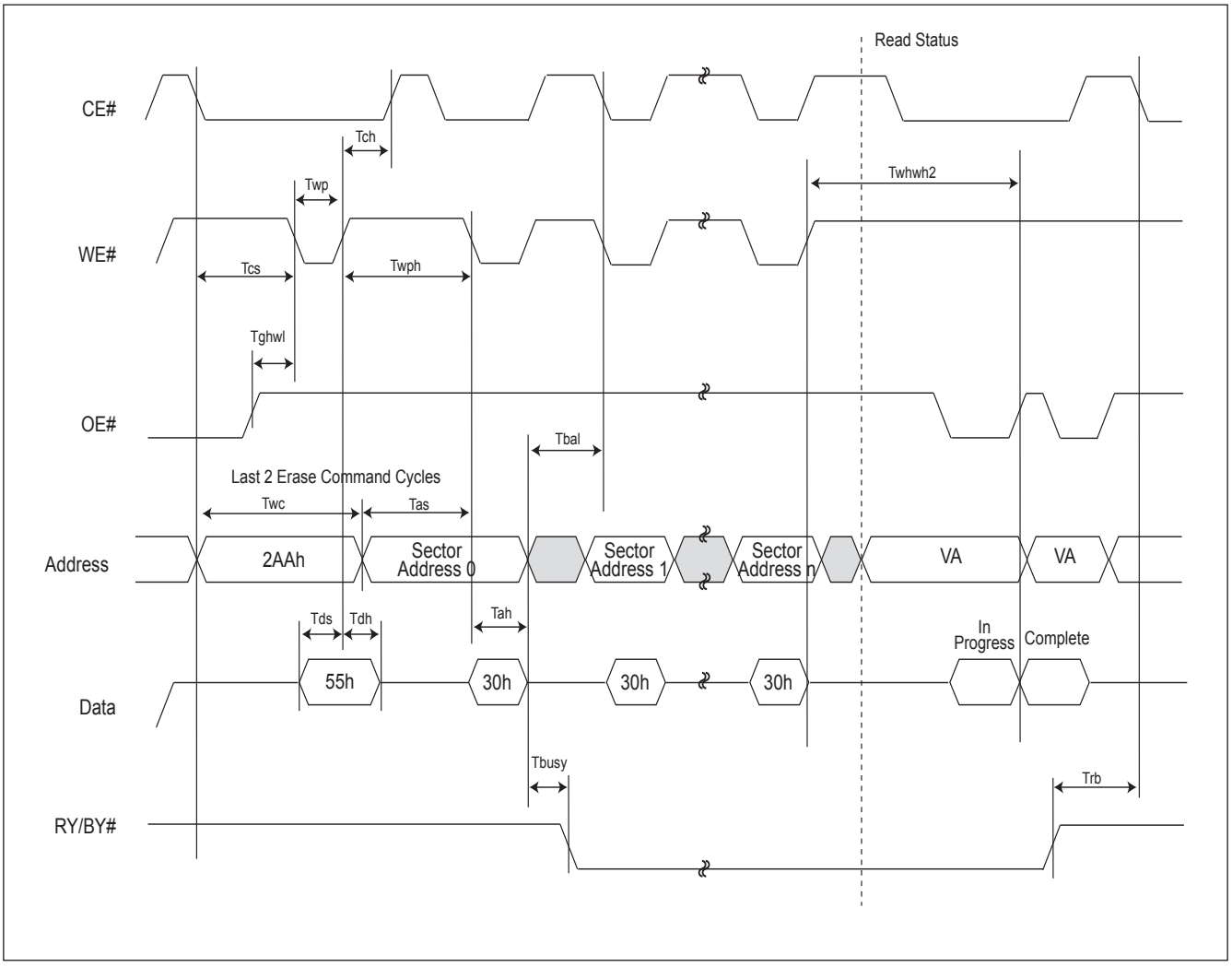
**Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART**





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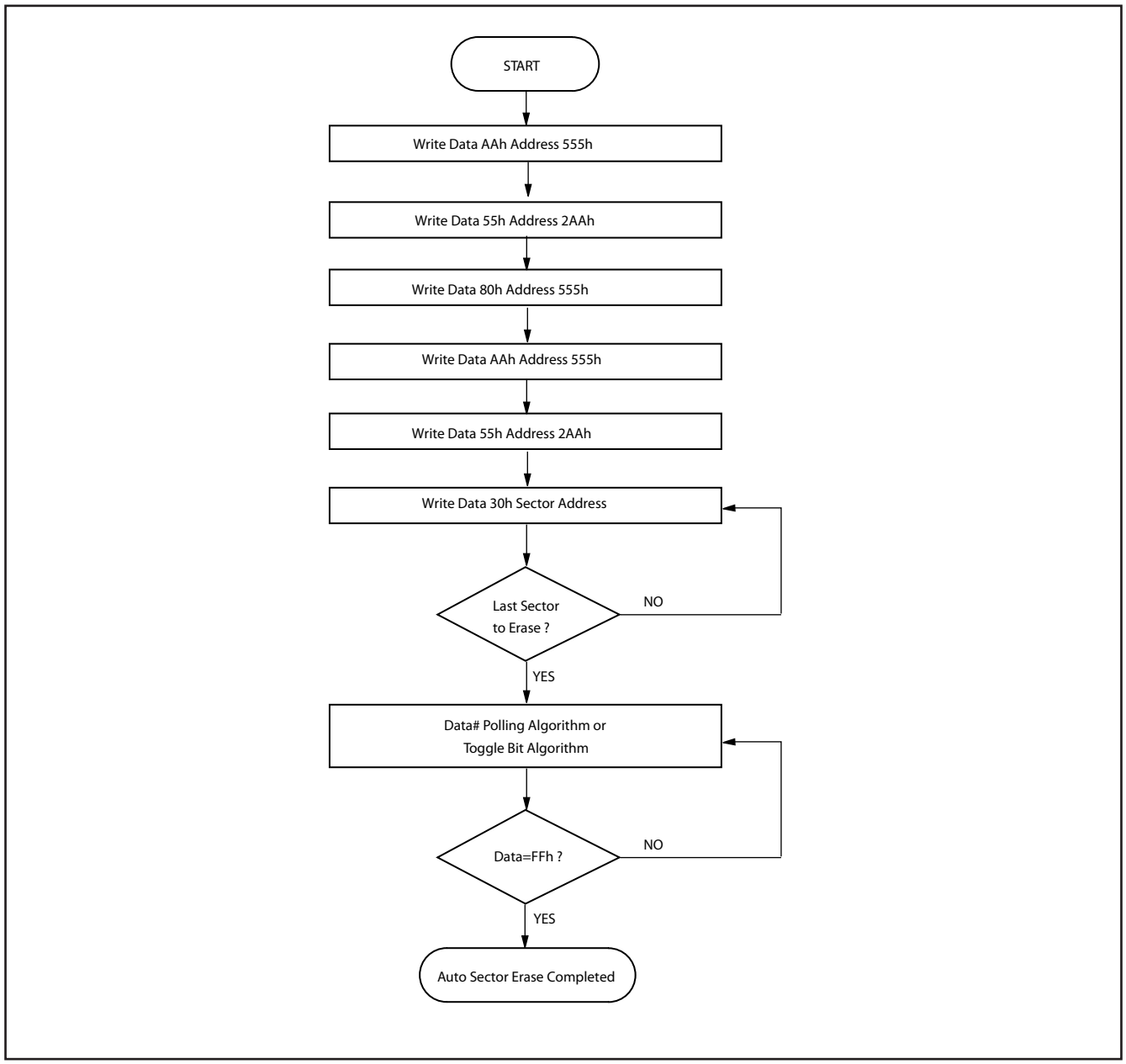
**Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM**





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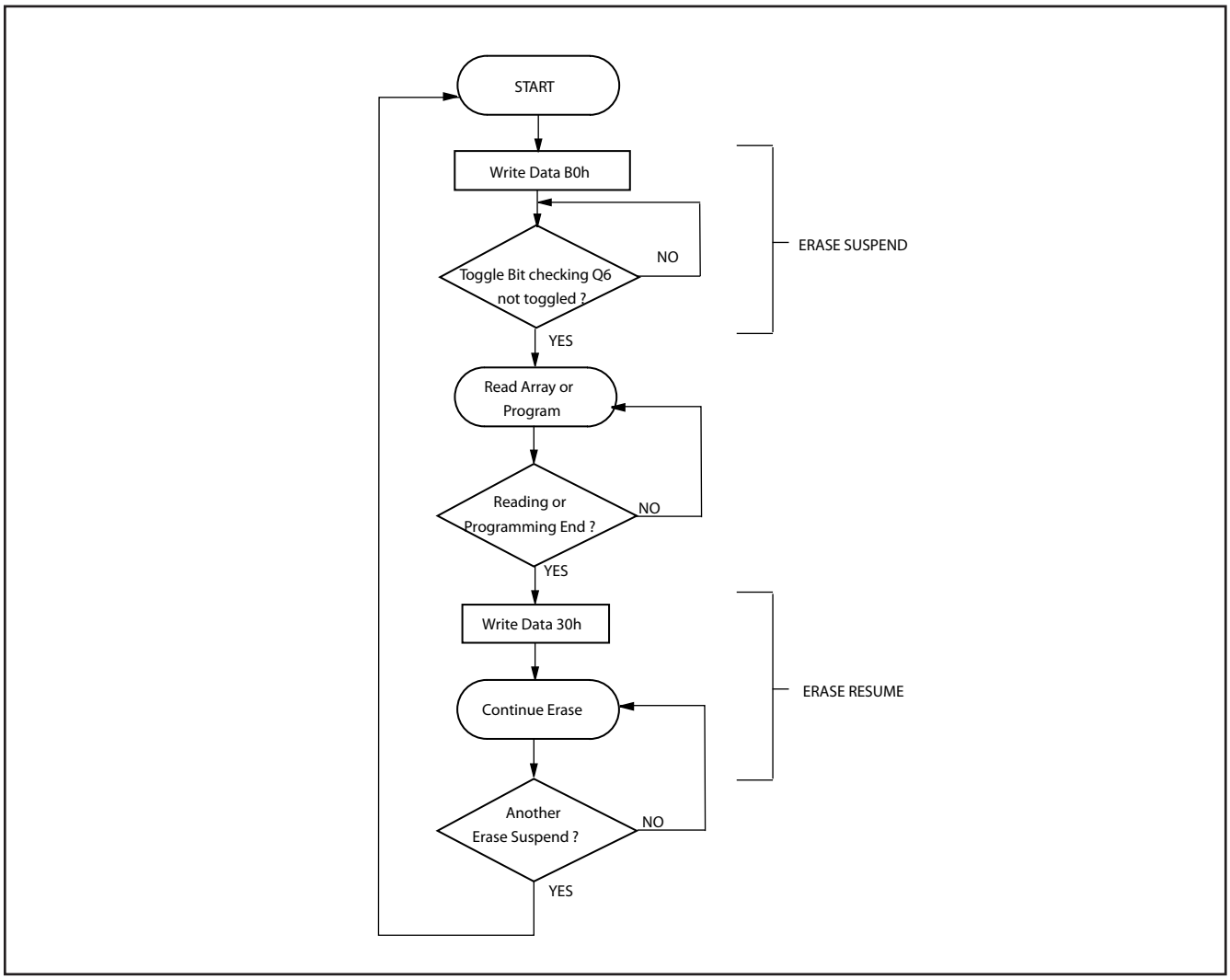
**Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART**





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**Figure 8. ERASE SUSPEND/RESUME FLOWCHART**





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**Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORM**

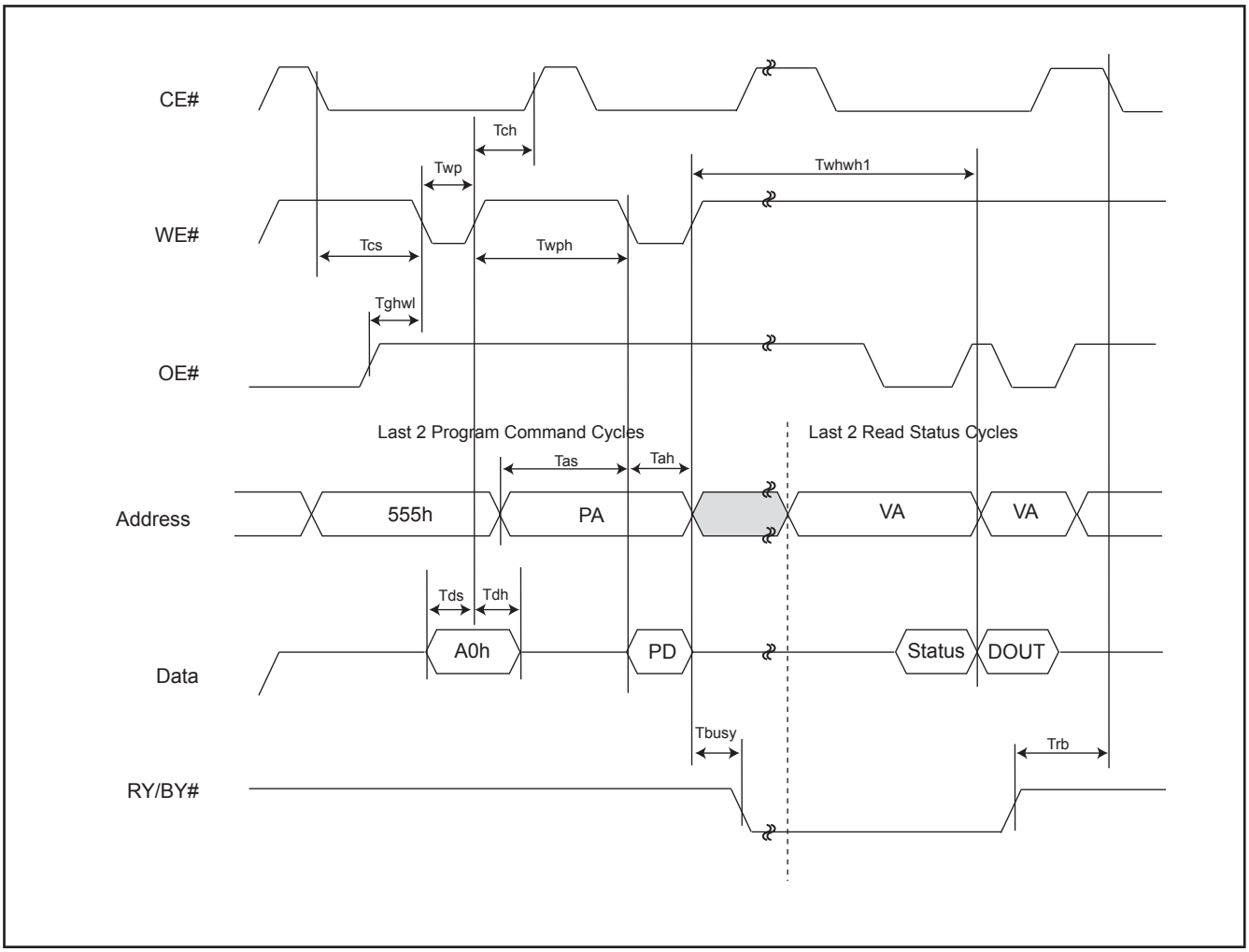
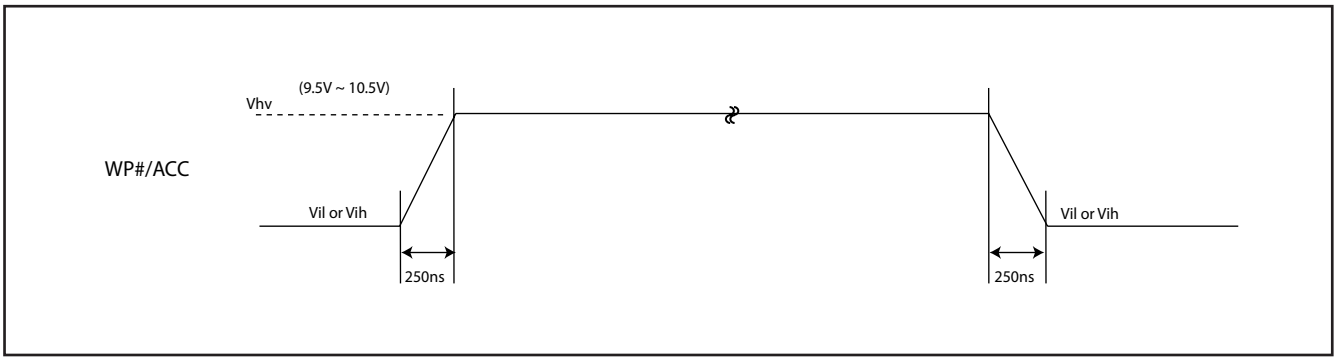


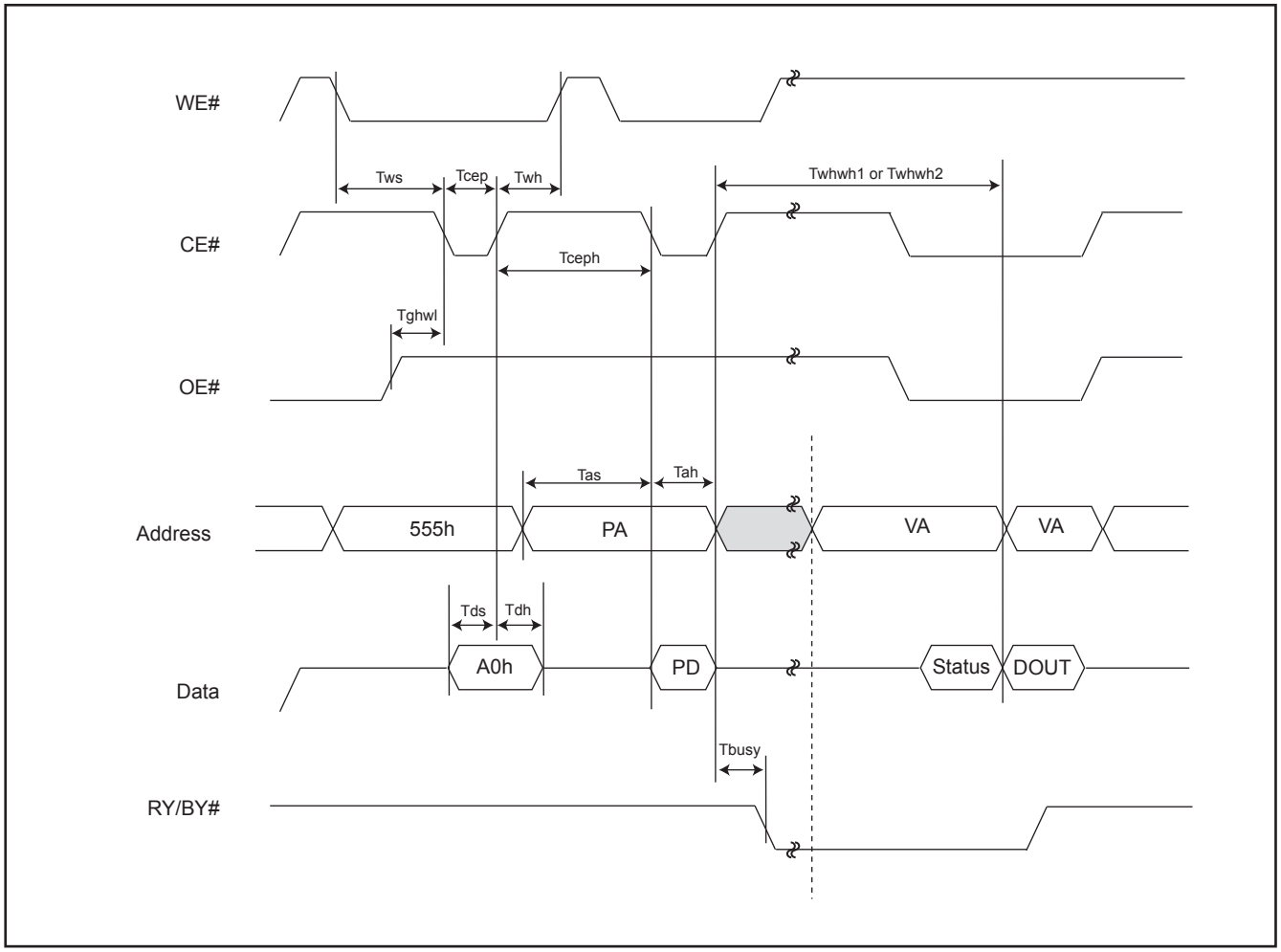

**Figure 10. ACCELERATED PROGRAM TIMING DIAGRAM**





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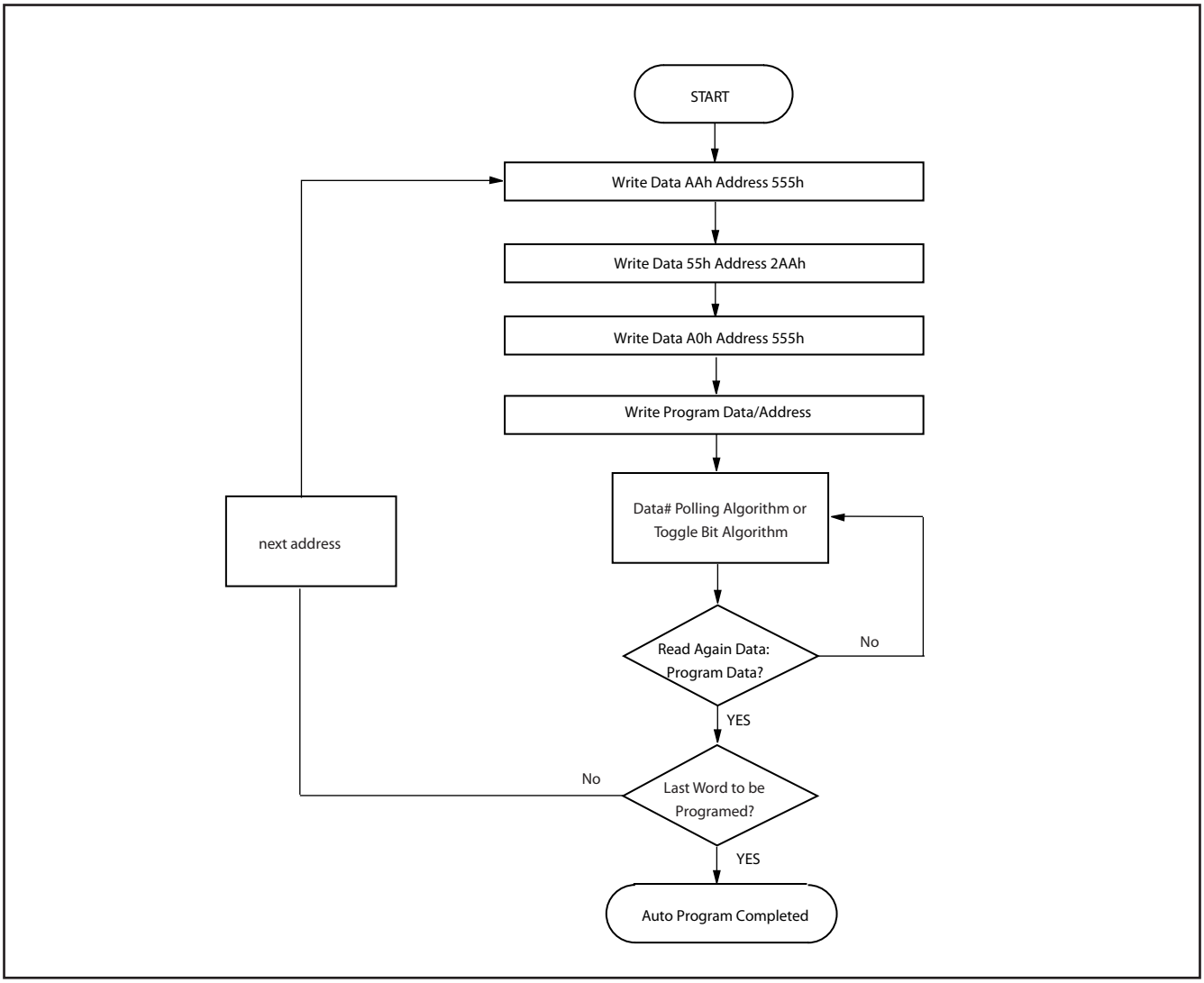
**Figure 11. CE# CONTROLLED WRITE TIMING WAVEFORM**





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**Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART**

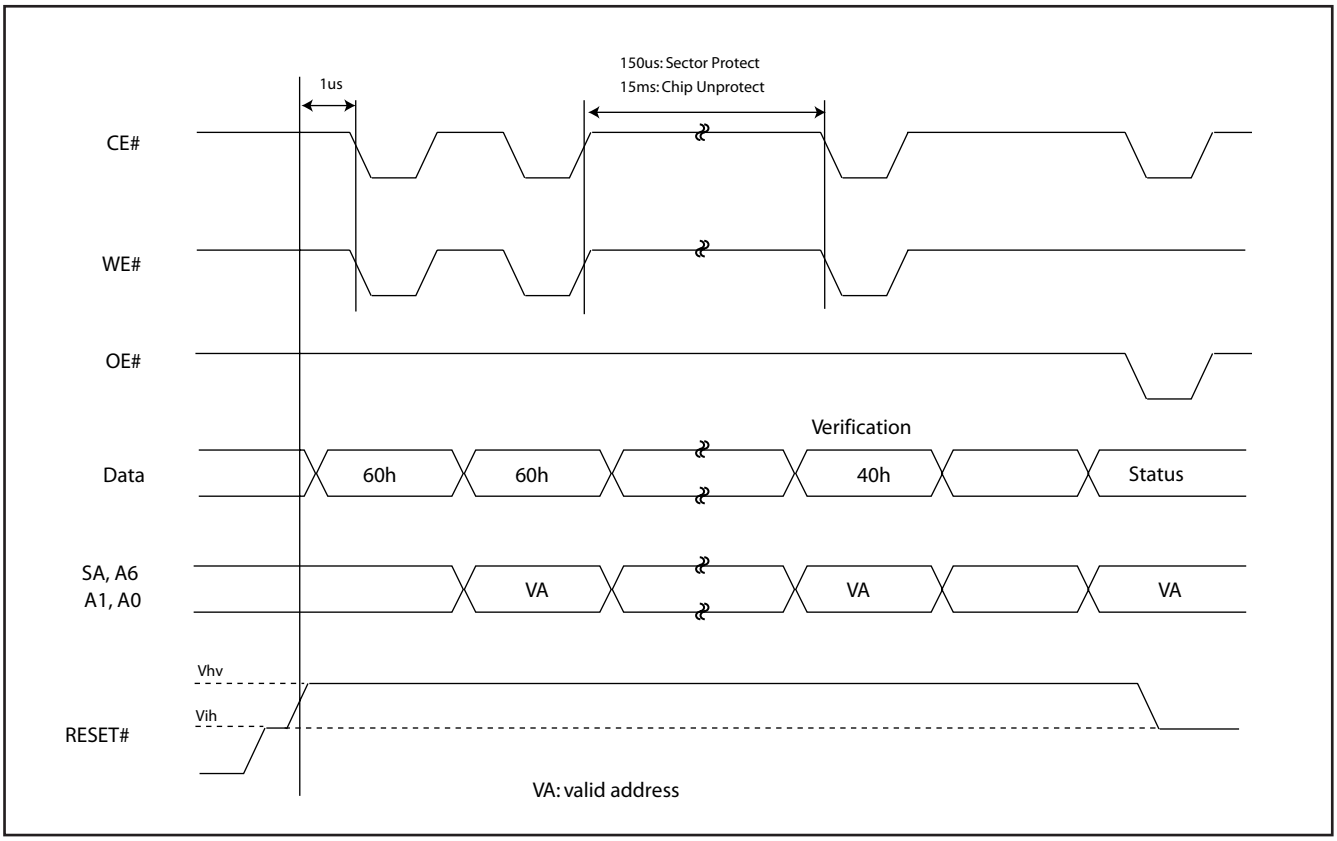




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## SECTOR PROTECT/CHIP UNPROTECT

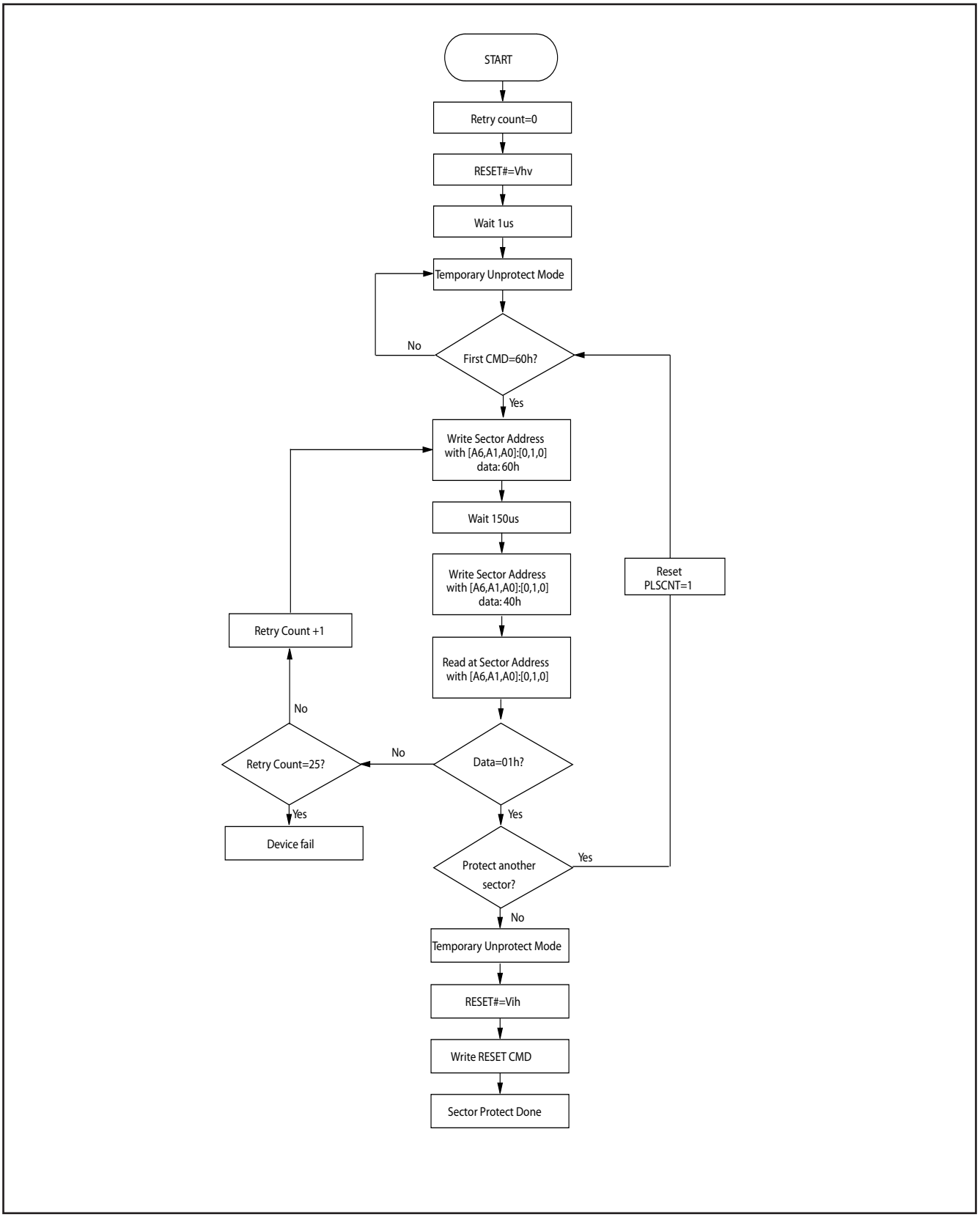
**Figure 13. SECTOR PROTECT/CHIP UNPROTECT WAVEFORM (RESET# Control)**





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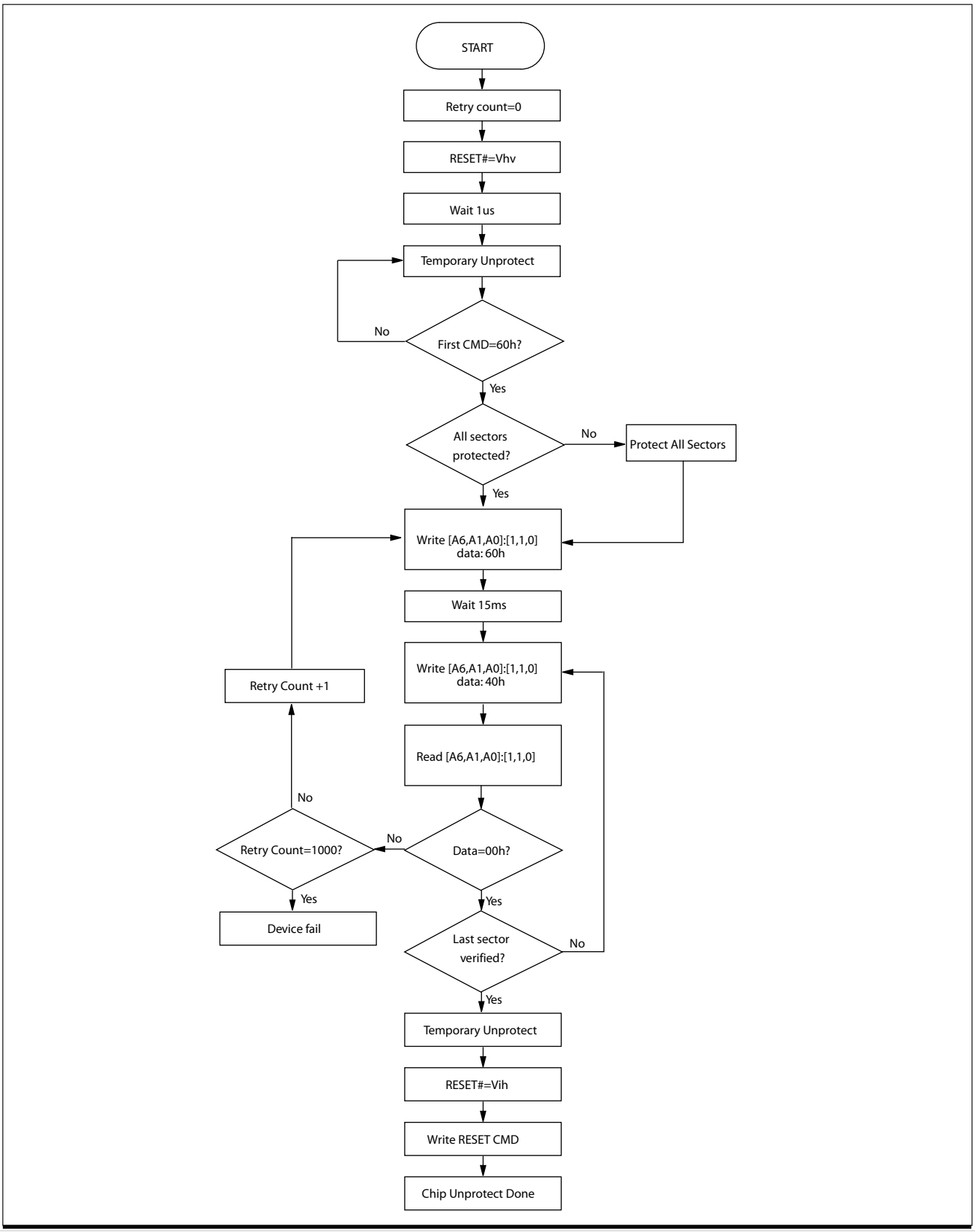
**Figure 14. IN-SYSTEM SECTOR PROTECT WITH RESET#=Vhv**





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**Figure 15. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv**



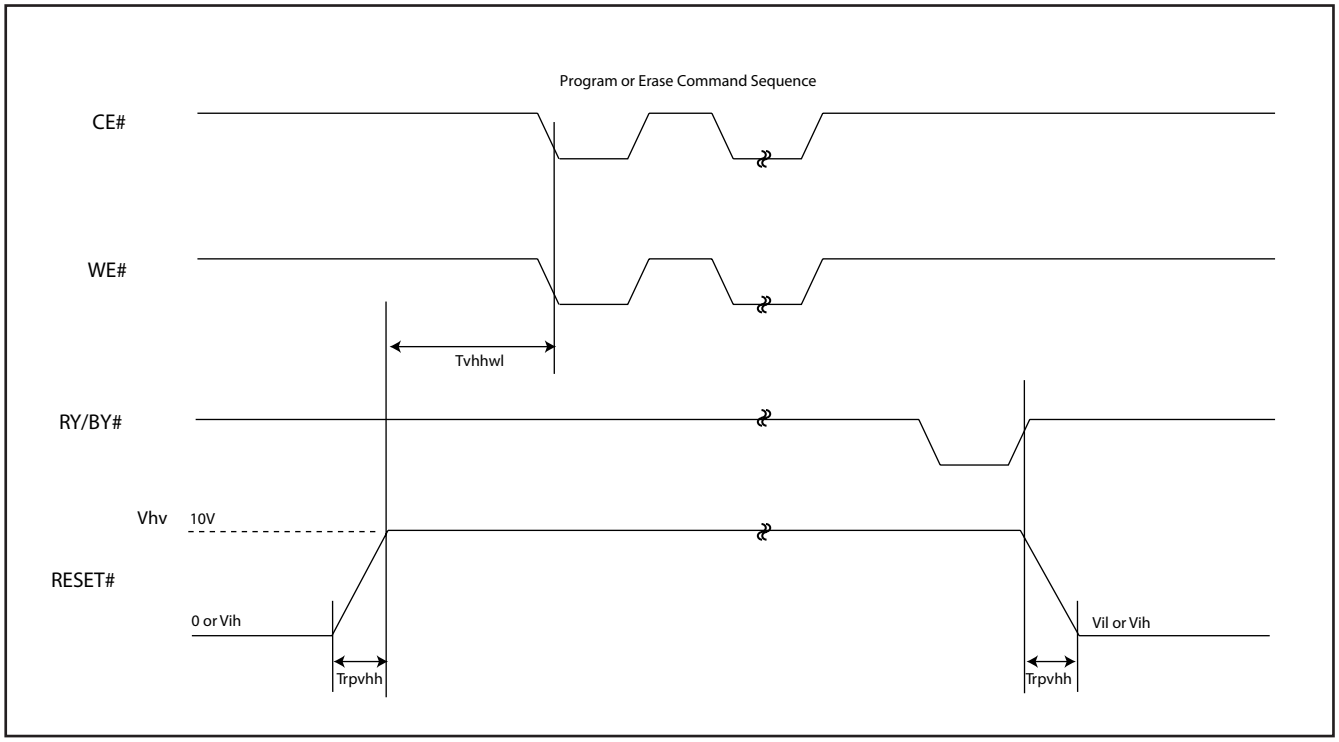


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**Table 5. TEMPORARY SECTOR UNPROTECT**

| Parameter | Alt | Description | Condition | Speed | Unit |
|---|---|---|---|---|---|
| Trpvhh | Tvidr | RESET# Rise Time to Vhv and Vhv Fall Time to RESET# | MIN | 500 | ns |
| Tvhhwl | Trsp | RESET# Vhv to WE# Low | MIN | 4 | us |

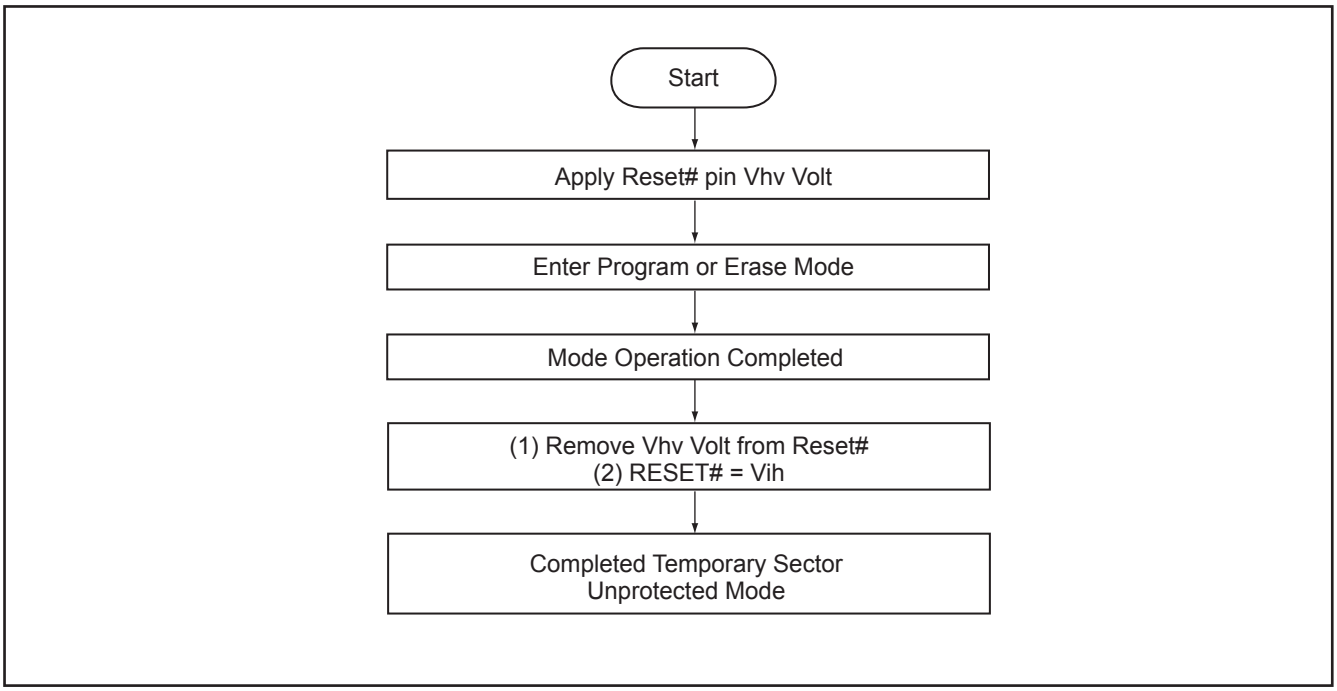
**Figure 16. TEMPORARY SECTOR UNPROTECT WAVEFORM**





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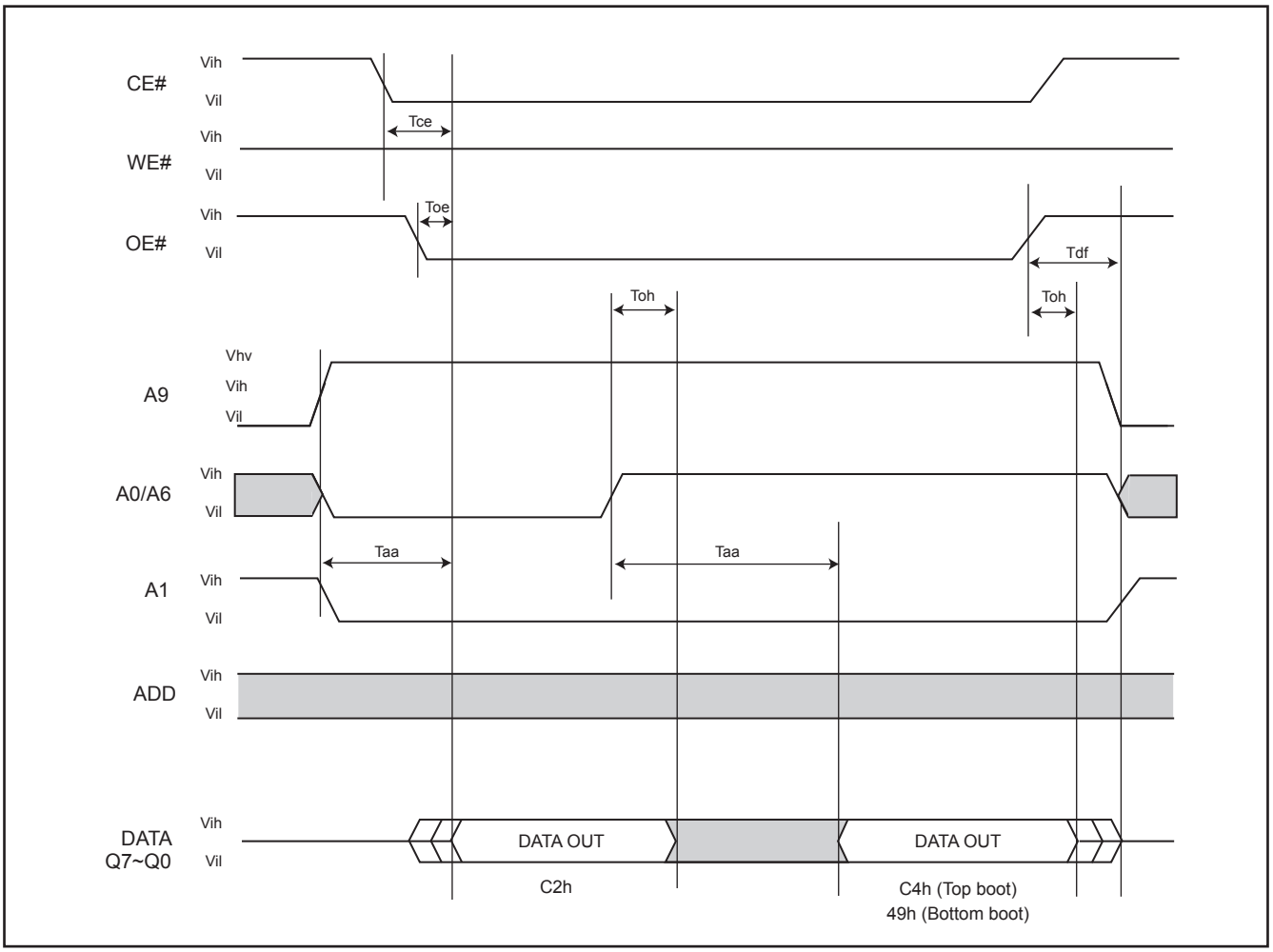
**Figure 17. TEMPORARY SECTOR UNPROTECT FLOWCHART**




Notes:
1. Temporary unprotect all protected sectors Vhv=9.5~10.5V.
2. After leaving temporary unprotect mode, the previously protected sectors are again protected.


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**Figure 18. SILICON ID READ TIMING WAVEFORM**

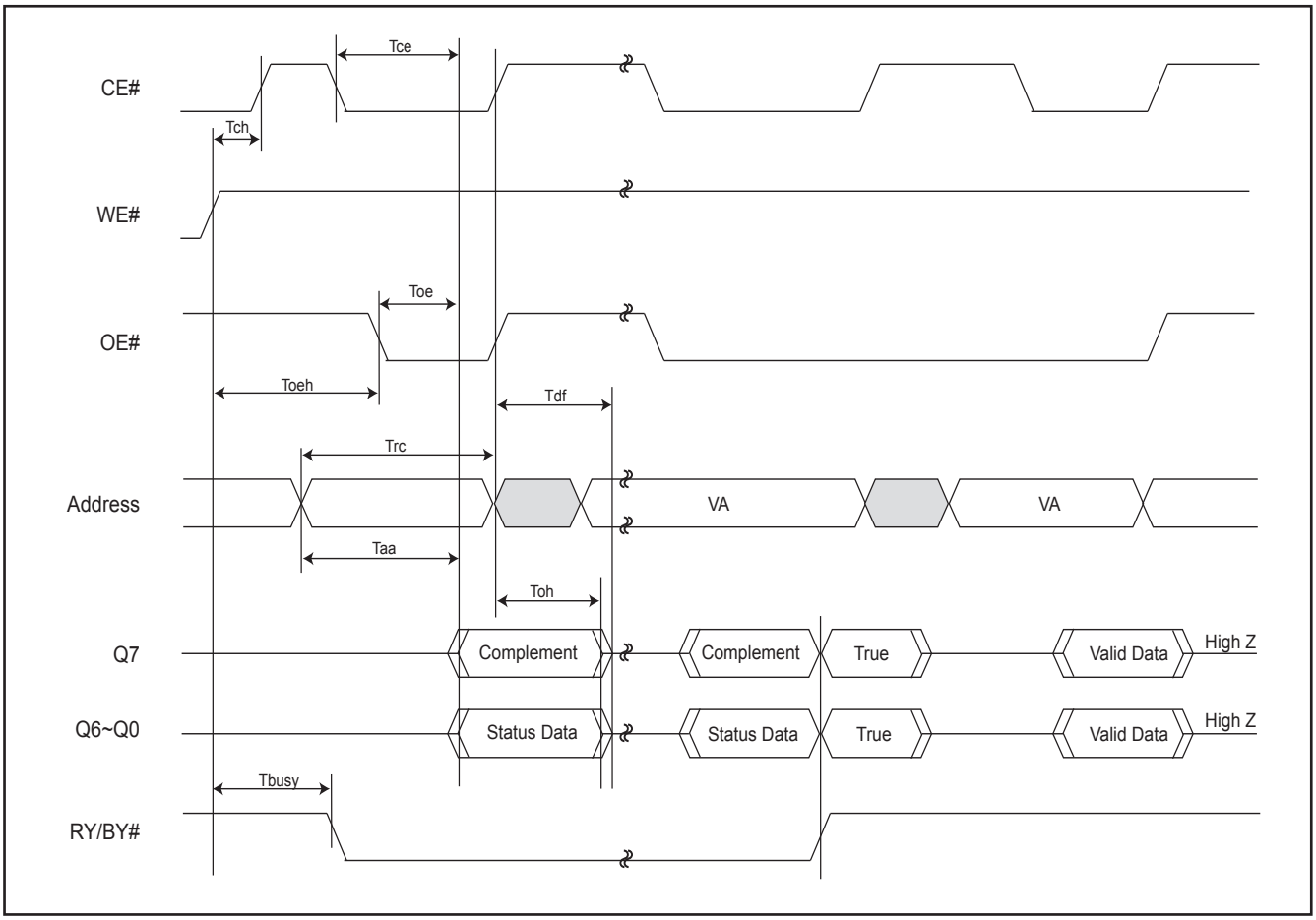




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## WRITE OPERATION STATUS

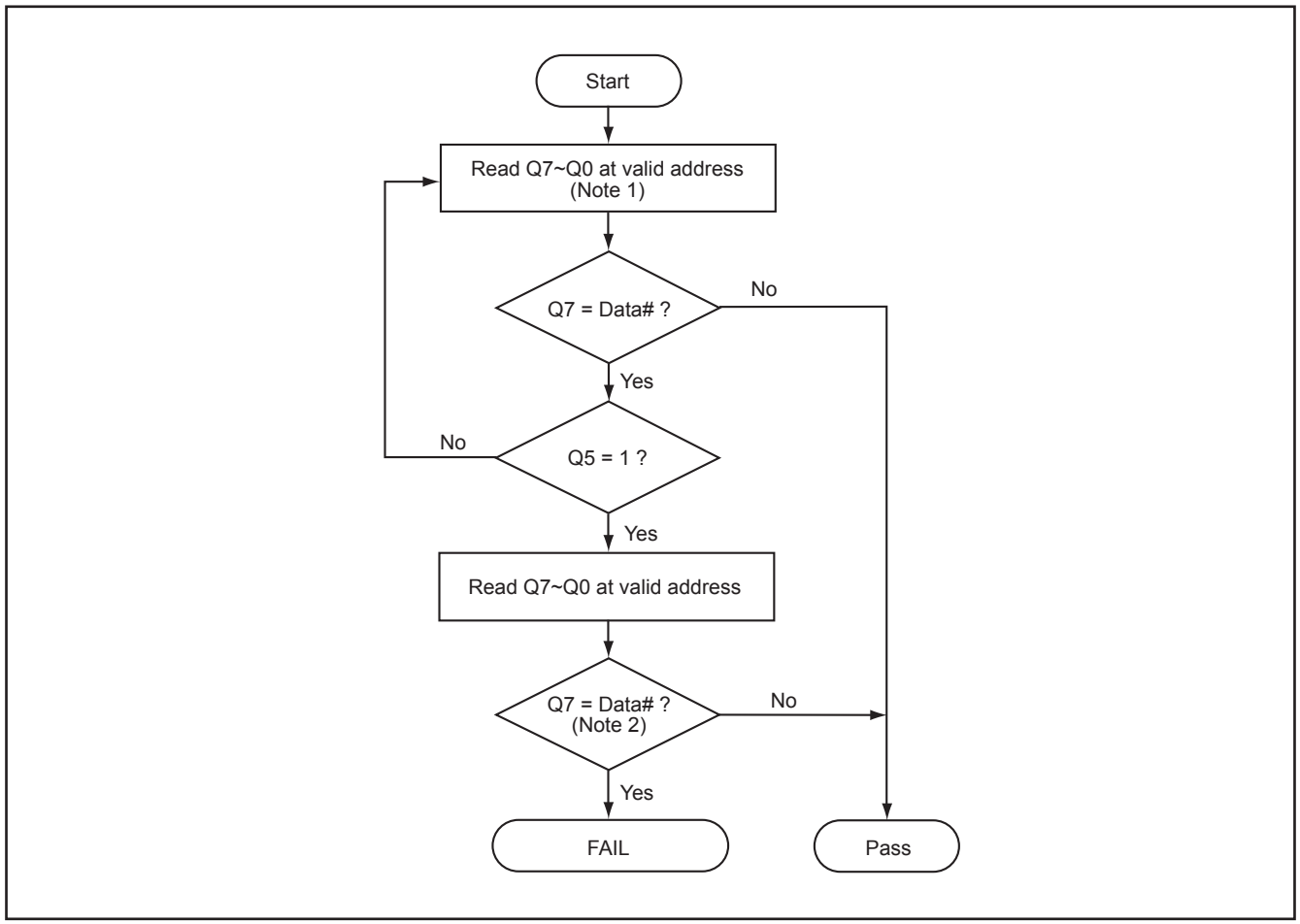
**Figure 19. DATA# POLLING TIMING WAVEFORM (DURING AUTOMATIC ALGORITHM)**





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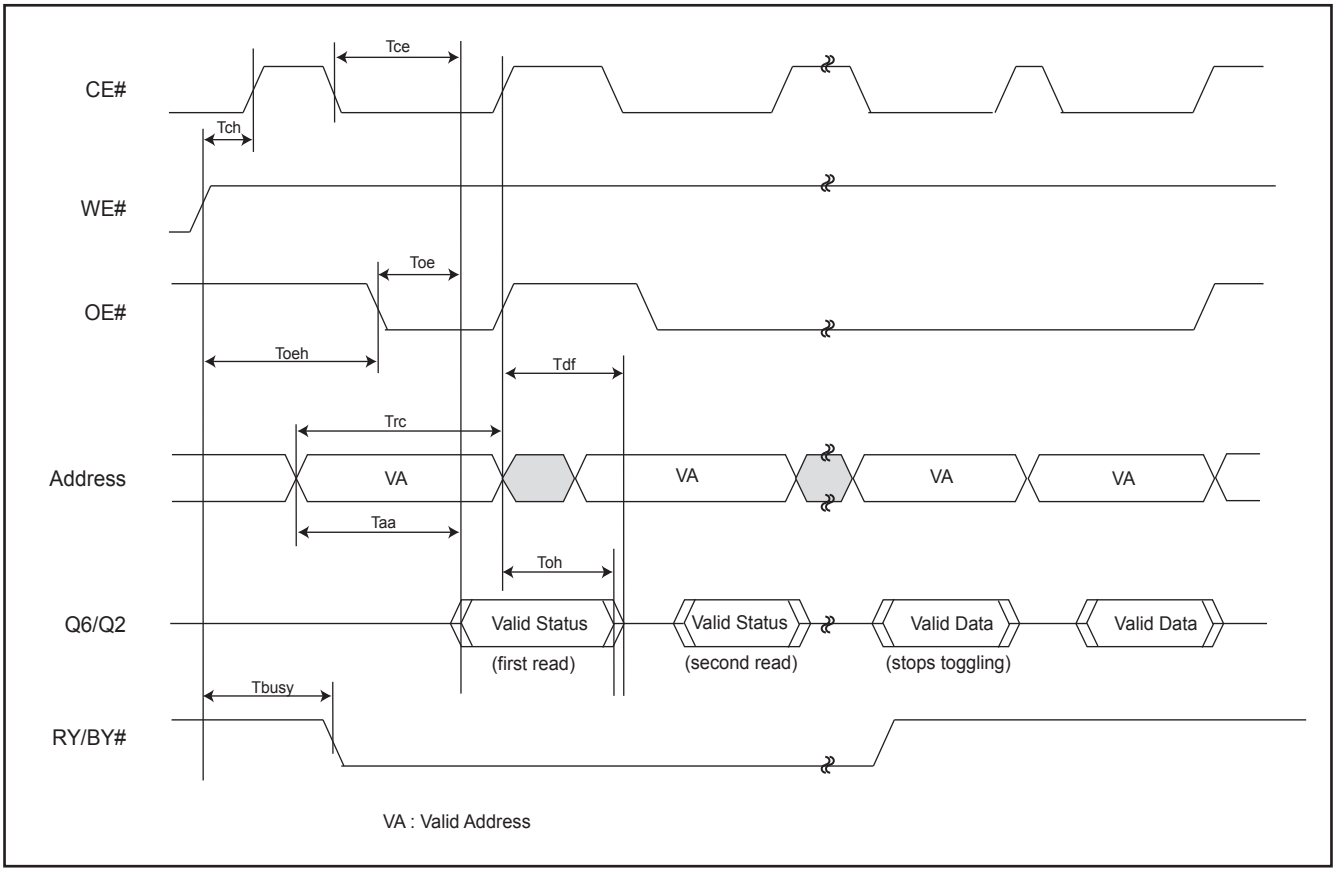
**Figure 20. DATA# POLLING ALGORITHM**




Notes:
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.


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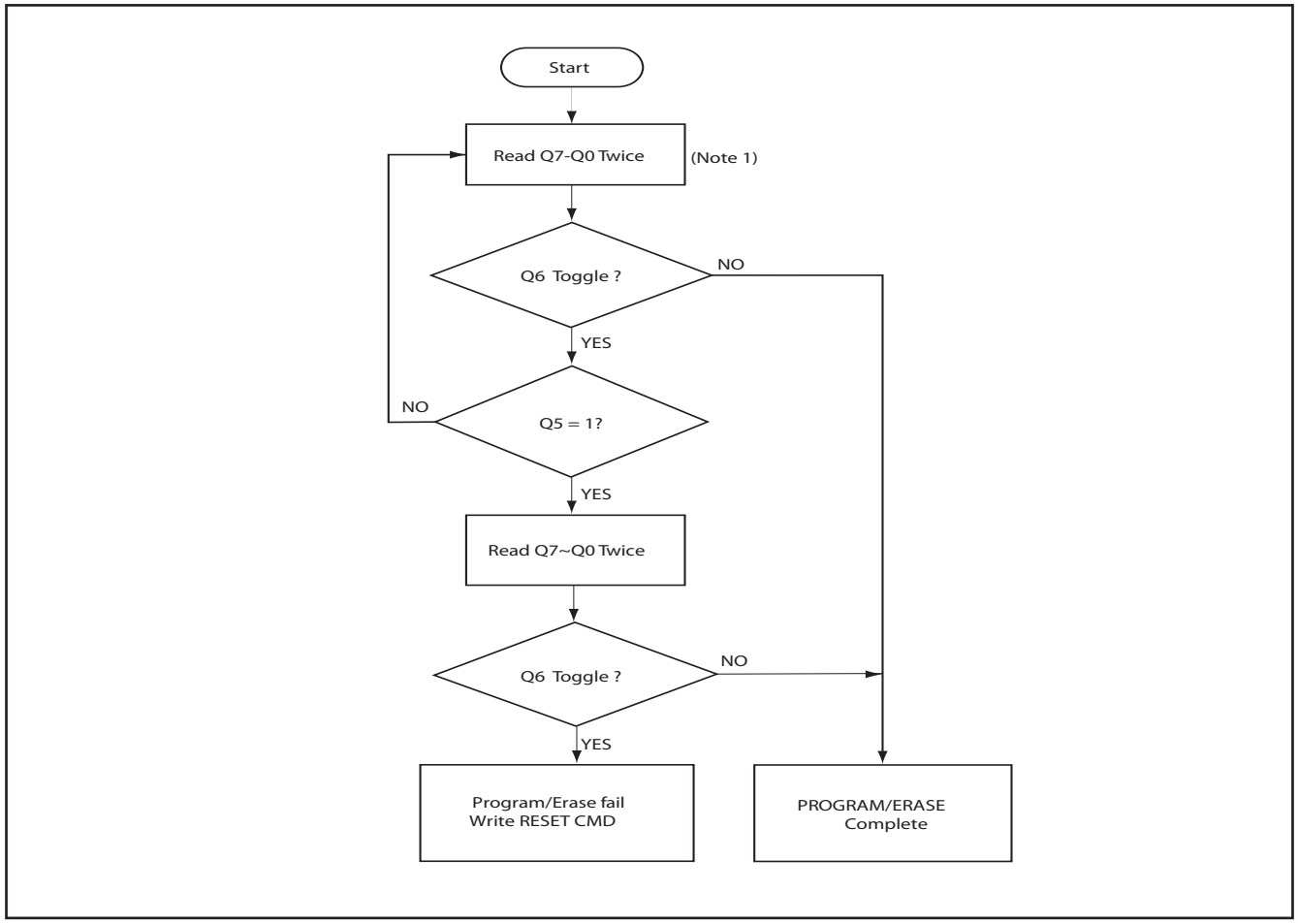
**Figure 21. TOGGLE BIT TIMING WAVEFORM (DURING AUTOMATIC ALGORITHM)**





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**Figure 22. TOGGLE BIT ALGORITHM**




Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

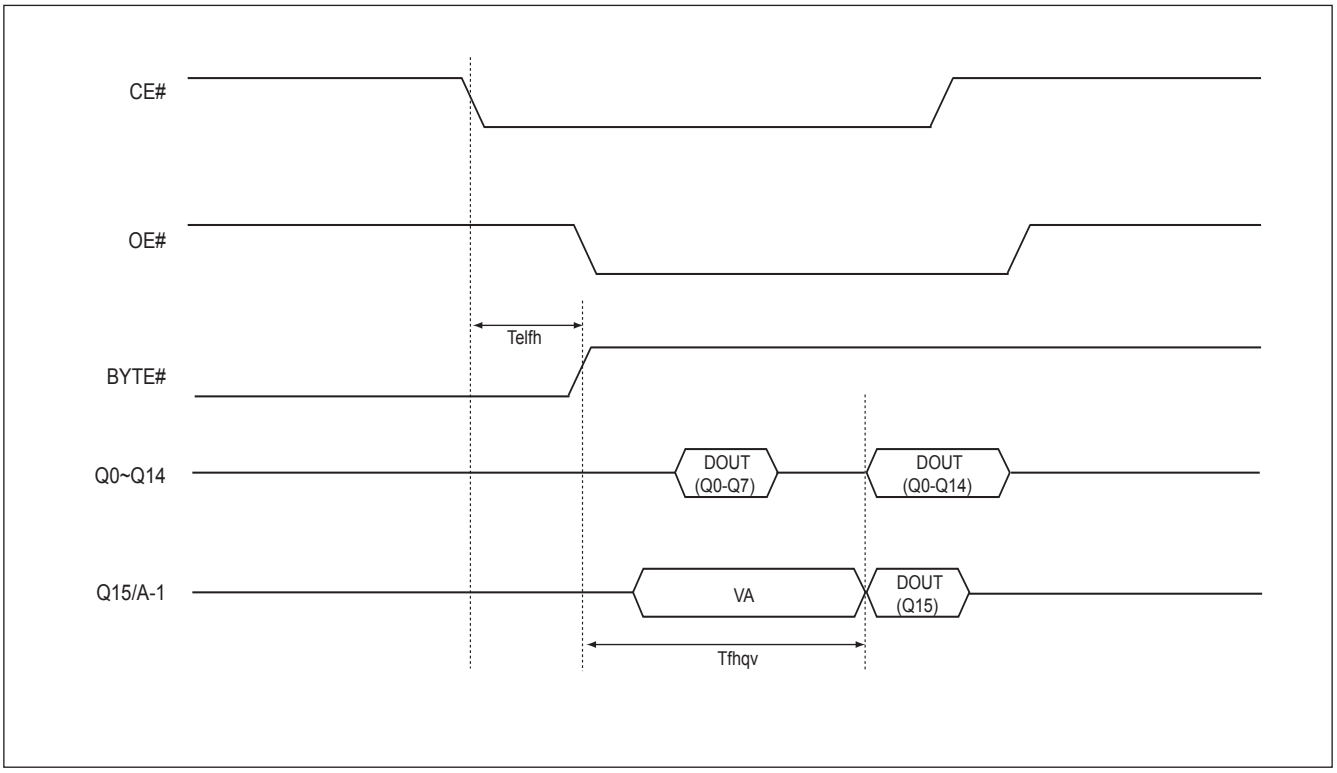

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## AC CHARACTERISTICS

### WORD/BYTE CONFIGURATION (BYTE#)

| Parameter | Description | | Speed Options | | Unit |
|---|---|---|---|---|---|
| | | | -70 | -90 | |
| Telfl/Telfh | CE# to BYTE# from L/H | MAX | 5 | 5 | ns |
| Tflqz | BYTE# from L to Output Hiz | MAX | 25 | 30 | ns |
| Tfhqv | BYTE# from H to Output Active | MIN | 70 | 90 | ns |

**Figure 23. BYTE# TIMING WAVEFORM FOR READ OPERATIONS (BYTE# switching from byte mode to word mode)**





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## RECOMMENDED OPERATING CONDITIONS

### At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

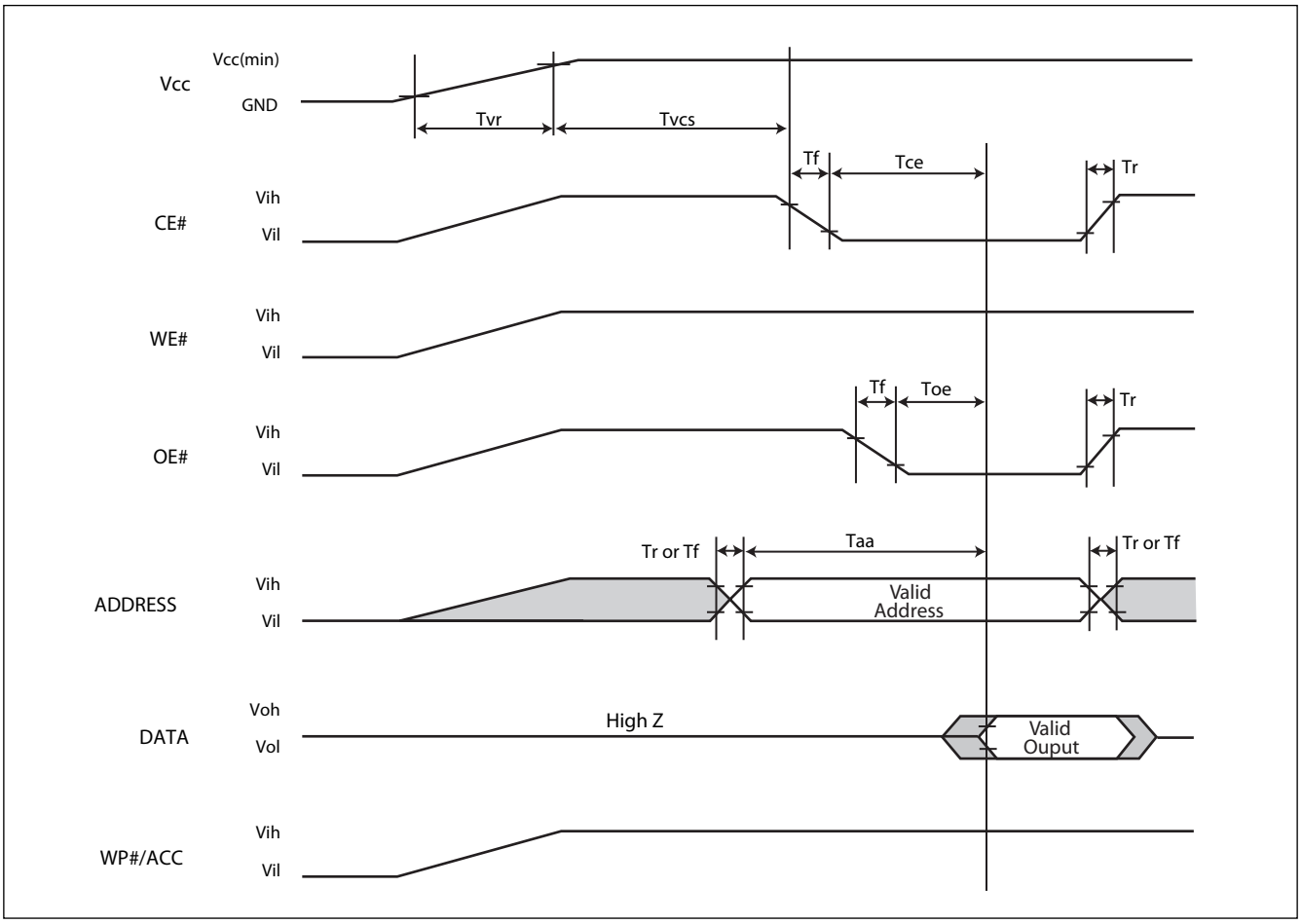



**Figure A. AC Timing at Device Power-Up**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| Tvr | Vcc Rise Time | 20 | 500000 | us/V |
| Tr | Input Signal Rise Time | | 20 | us/V |
| Tf | Input Signal Fall Time | | 20 | us/V |
| Tvcs | Vcc Setup Time | 200 | | us |


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## ERASE AND PROGRAMMING PERFORMANCE

| Parameter | | Limits | | | Units |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Chip Erase Time | | | 15 | 32 | sec |
| Sector Erase Time | | | 0.7 | 2 | sec |
| Erase/Program Cycles | | | 100,000 | | Cycles |
| Chip Programming Time | Byte Mode | | 18 | 54 | sec |
| | Word Mode | | 12 | 36 | sec |
| Word Program Time | | | 11 | 360 | us |
| Byte Programming Time | | | 9 | 300 | us |
| Accelerated Program Time | | | 7 | 210 | us |

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC. Programming specifications assume checkboard data pattern.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
4. Erase/Program cycles comply with JEDEC JESD-47 & JESD 22-A117 standard.

## DATA RETENTION

| Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|
| Data retention | 55˚C | 20 | | years |

## LATCH-UP CHARACTERISTICS

| | Min. | Max. |
|---|---|---|
| Input voltage difference with GND on all pins except I/O pins | -1.0V | 10.5V |
| Input voltage difference with GND on all I/O pins | -1.0V | 1.5 x Vcc |
| Vcc Current | -100mA | +100mA |
| All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing | | |

## PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Set | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| CIN2 | Control Pin Capacitance | VIN=0 | 7.5 | 9 | pF |
| COUT | Output Capacitance | VOUT=0 | 8.5 | 12 | pF |
| CIN | Input Capacitance | VIN=0 | 6 | 7.5 | pF |


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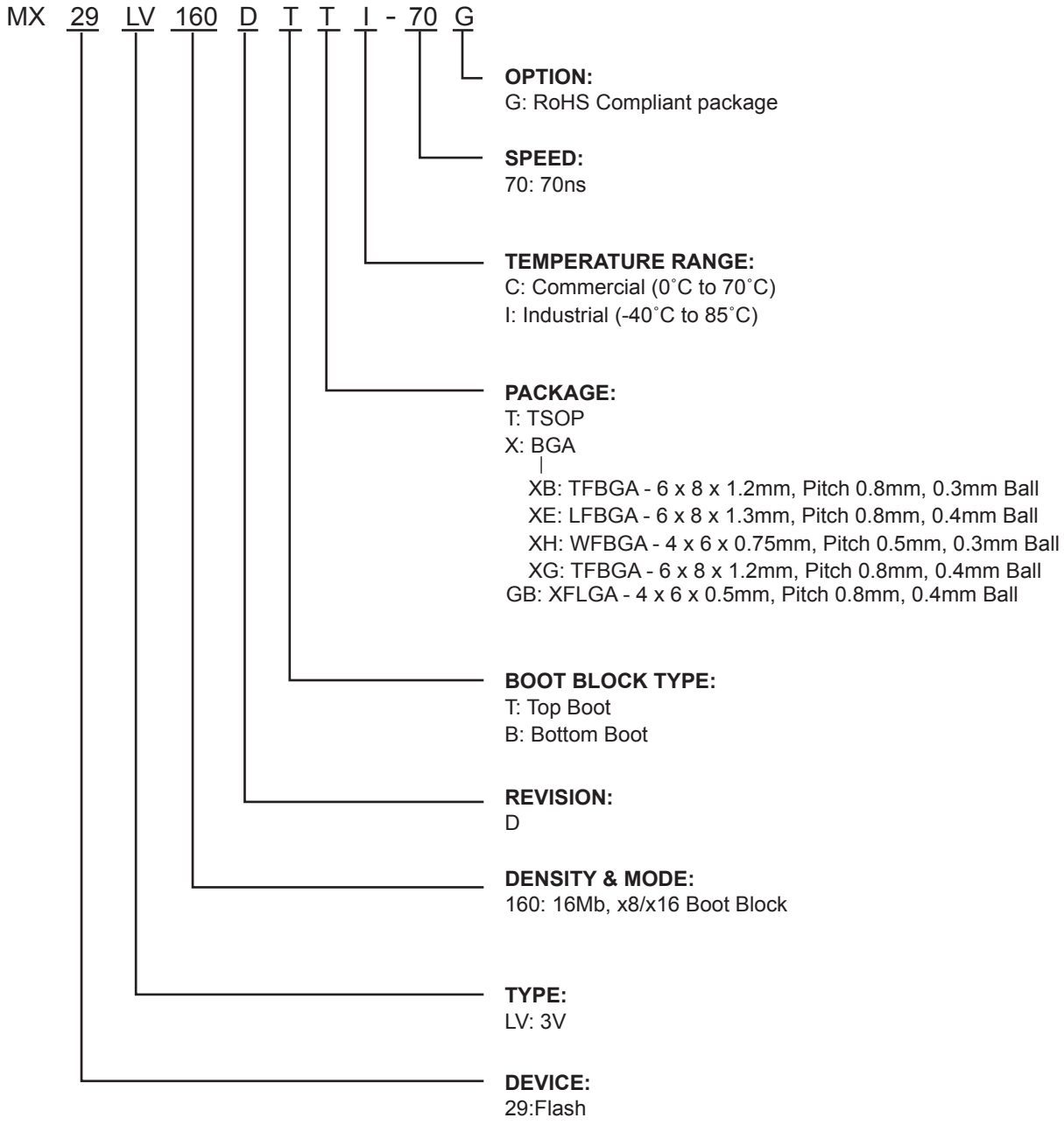
## ORDERING INFORMATION

| PART NO. | ACCESS TIME (ns) | Ball Pitch/ Ball Size | PACKAGE | Remark |
|---|---|---|---|---|
| MX29LV160DTTI-70G | 70 | | 48 Pin TSOP (Normal Type) | |
| MX29LV160DBTI-70G | 70 | | 48 Pin TSOP (Normal Type) | |
| MX29LV160DTXBI-70G | 70 | 0.8mm/0.3mm | 48 Ball CSP(TFBGA) (ball size:0.3mm) | |
| MX29LV160DBXBI-70G | 70 | 0.8mm/0.3mm | 48 Ball CSP(TFBGA) (ball size:0.3mm) | |
| MX29LV160DTGBI-70G | 70 | | 48 Ball XFLGA (4 x 6 x 0.5mm) | |
| MX29LV160DBGBI-70G | 70 | | 48 Ball XFLGA (4 x 6 x 0.5mm) | |
| MX29LV160DTXHI-70G | 70 | | 48 Ball WFBGA (4 x 6 x 0.75mm) | |
| MX29LV160DBXHI-70G | 70 | | 48 Ball WFBGA (4 x 6 x 0.75mm) | |
| MX29LV160DTXEI-70G | 70 | 0.8mm/0.4mm | 48 Ball LFBGA (ball size:0.4mm) | |
| MX29LV160DBXEI-70G | 70 | 0.8mm/0.4mm | 48 Ball LFBGA (ball size:0.4mm) | |
| MX29LV160DTXGI-70G* | 70 | 0.8mm/0.4mm | 48 Ball TFBGA (ball size: 0.4mm, height: 1.2mm) | |
| MX29LV160DBXGI-70G* | 70 | 0.8mm/0.4mm | 48 Ball TFBGA (ball size: 0.4mm, height: 1.2mm) | |

* Advanced Information


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## PART NAME DESCRIPTION

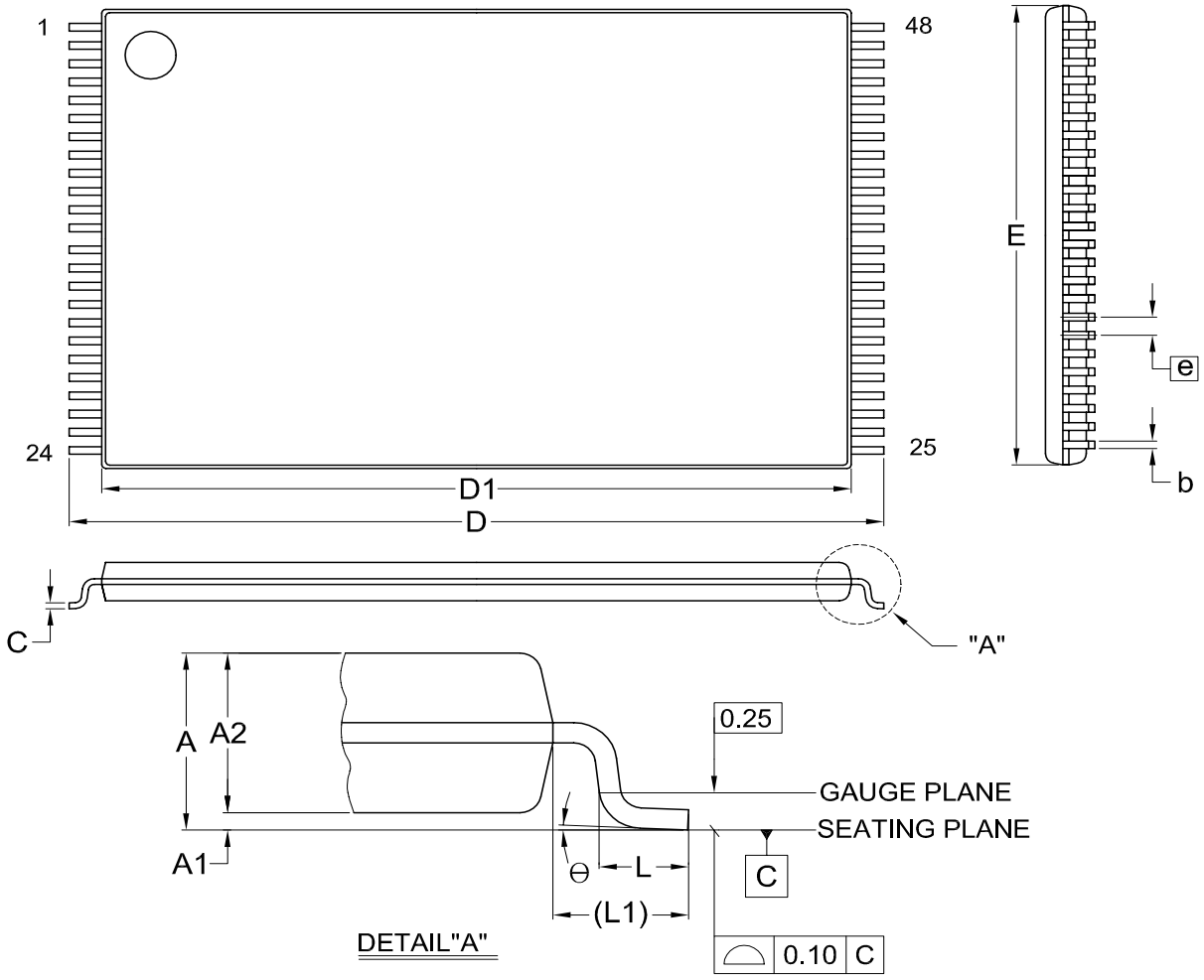




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## PACKAGE INFORMATION

Doc. Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM




Dimensions (inch dimensions are derived from the original mm dimensions)

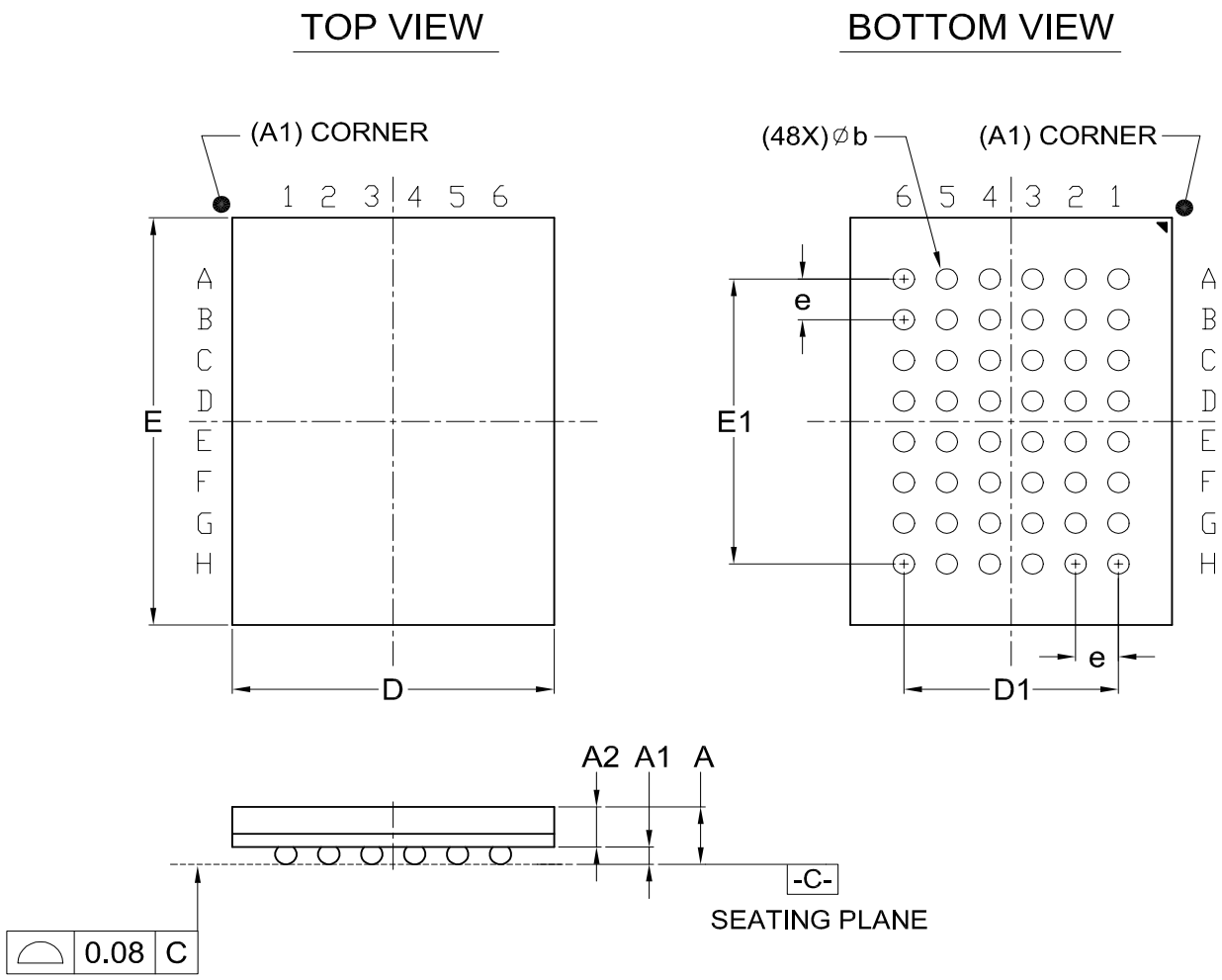
| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | D1 | E | e | L | L1 | Θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | — | 0.05 | 0.95 | 0.17 | 0.10 | 19.80 | 18.30 | 11.90 | --- | 0.50 | 0.70 | 0 |
| | Nom. | --- | 0.10 | 1.00 | 0.20 | 0.13 | 20.00 | 18.40 | 12.00 | 0.50 | 0.60 | 0.80 | 5 |
| | Max. | 1.20 | 0.15 | 1.05 | 0.27 | 0.21 | 20.20 | 18.50 | 12.10 | --- | 0.70 | 0.90 | 8 |
| Inch | Min. | --- | 0.002 | 0.037 | 0.007 | 0.004 | 0.780 | 0.720 | 0.469 | --- | 0.020 | 0.028 | 0 |
| | Nom. | --- | 0.004 | 0.039 | 0.008 | 0.005 | 0.787 | 0.724 | 0.472 | 0.020 | 0.024 | 0.031 | 5 |
| | Max. | 0.047 | 0.006 | 0.041 | 0.011 | 0.008 | 0.795 | 0.728 | 0.476 | --- | 0.028 | 0.035 | 8 |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-1607 | 9 | MO-142 | | | |


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**48-Ball TFBGA (for MX29LV160D TXBI/BXBI)**

Doc. Title: Package Outline for CSP 48BALL(6X8X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.3MM)




Dimensions (inch dimensions are derived from the original mm dimensions)

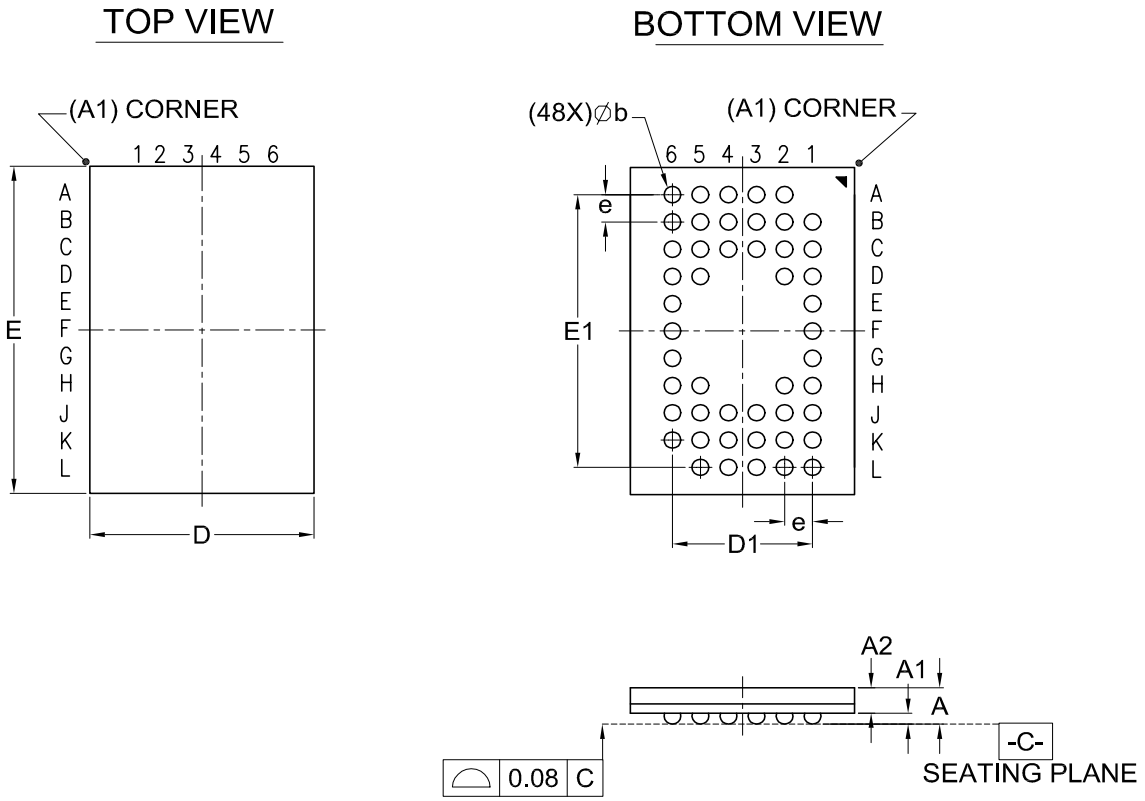
| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | — | 0.18 | 0.65 | 0.25 | 5.90 | | 7.90 | | |
| | Nom. | — | 0.23 | — | 0.30 | 6.00 | 4.00 | 8.00 | 5.60 | 0.80 |
| | Max. | 1.20 | 0.28 | — | 0.35 | 6.10 | | 8.10 | | |
| Inch | Min. | --- | 0.007 | 0.026 | 0.010 | 0.232 | | 0.311 | | |
| | Nom. | --- | 0.009 | --- | 0.012 | 0.236 | 0.157 | 0.315 | 0.220 | 0.031 |
| | Max. | 0.047 | 0.011 | --- | 0.014 | 0.240 | | 0.319 | | |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-4201 | 7 | MO-210 | | | |


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**48-Ball WFBGA (for MX29LV160D TXHI/BXHI)**

Doc. Title: Package Outline for CSP 48BALL(4X6X0.75MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)




Dimensions (inch dimensions are derived from the original mm dimensions)

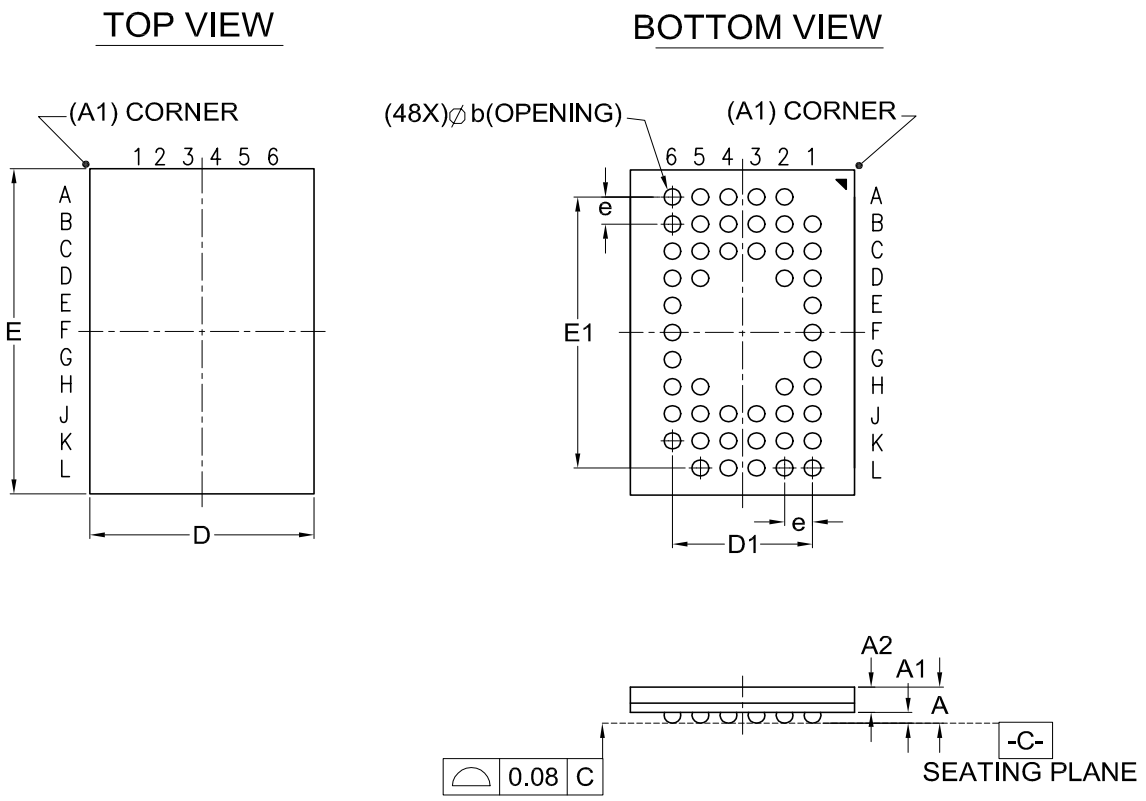
| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.16 | 0.41 | 0.25 | 3.90 | | 5.90 | | |
| | Nom. | --- | 0.21 | --- | 0.30 | 4.00 | 2.50 | 6.00 | 5.00 | 0.50 |
| | Max. | 0.75 | 0.26 | --- | 0.35 | 4.10 | | 6.10 | | |
| Inch | Min. | — | 0.006 | 0.016 | 0.010 | 0.154 | | 0.232 | | |
| | Nom. | — | 0.008 | -— | 0.012 | 0.157 | 0.098 | 0.236 | 0.197 | 0.020 |
| | Max. | 0.030 | 0.010 | -— | 0.014 | 0.161 | | 0.240 | | |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-4250 | 2 | | | | |


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**48-Ball XFLGA (for MX29LV160D TGBI/BGBI)**

Doc. Title: Package Outline for XFLGA 48L (4x6x0.5MM,LAND PITCH 0.5MM,LAND OPENING 0.25MM)




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.02 | 0.33 | 0.20 | 3.90 | — | 5.90 | — | — |
| | Nom. | --- | 0.05 | --- | 0.25 | 4.00 | 2.50 | 6.00 | 5.00 | 0.50 |
| | Max. | 0.50 | 0.08 | --- | 0.30 | 4.10 | — | 6.10 | — | — |
| Inch | Min. | — | 0.001 | 0.013 | 0.008 | 0.154 | — | 0.232 | — | — |
| | Nom. | — | 0.002 | --- | 0.010 | 0.157 | 0.098 | 0.236 | 0.197 | 0.020 |
| | Max. | 0.020 | 0.003 | --- | 0.012 | 0.161 | — | 0.240 | — | — |

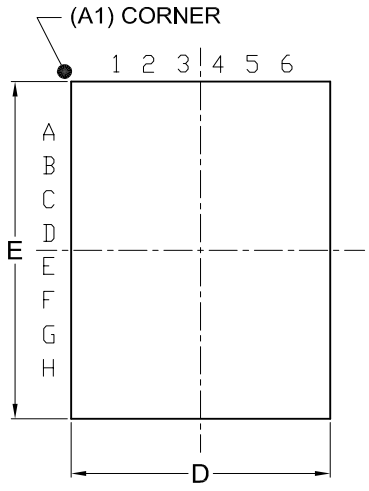
| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-3501 | 1 | MO-222 | | | |


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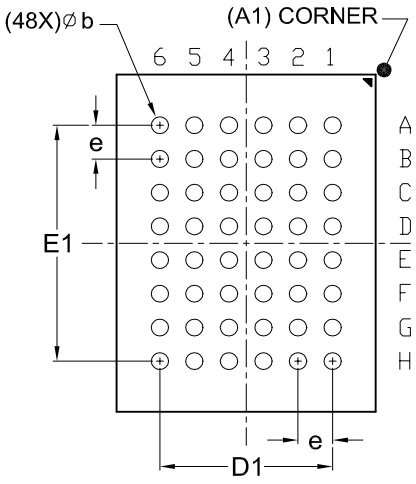
**48-Ball LFBGA (for MX29LV160D TXEI/BXEI)**

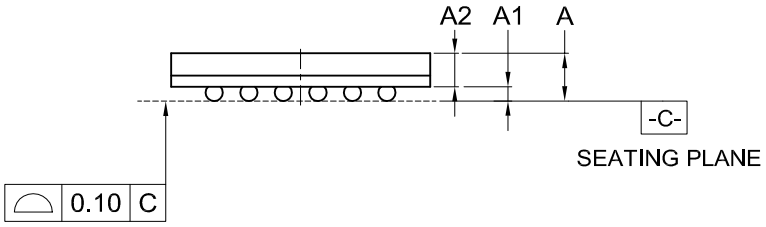
Doc. Title: Package Outline for CSP 48BALL(6X8X1.3MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)

TOP VIEW




BOTTOM VIEW




Dimensions (inch dimensions are derived from the original mm dimensions)

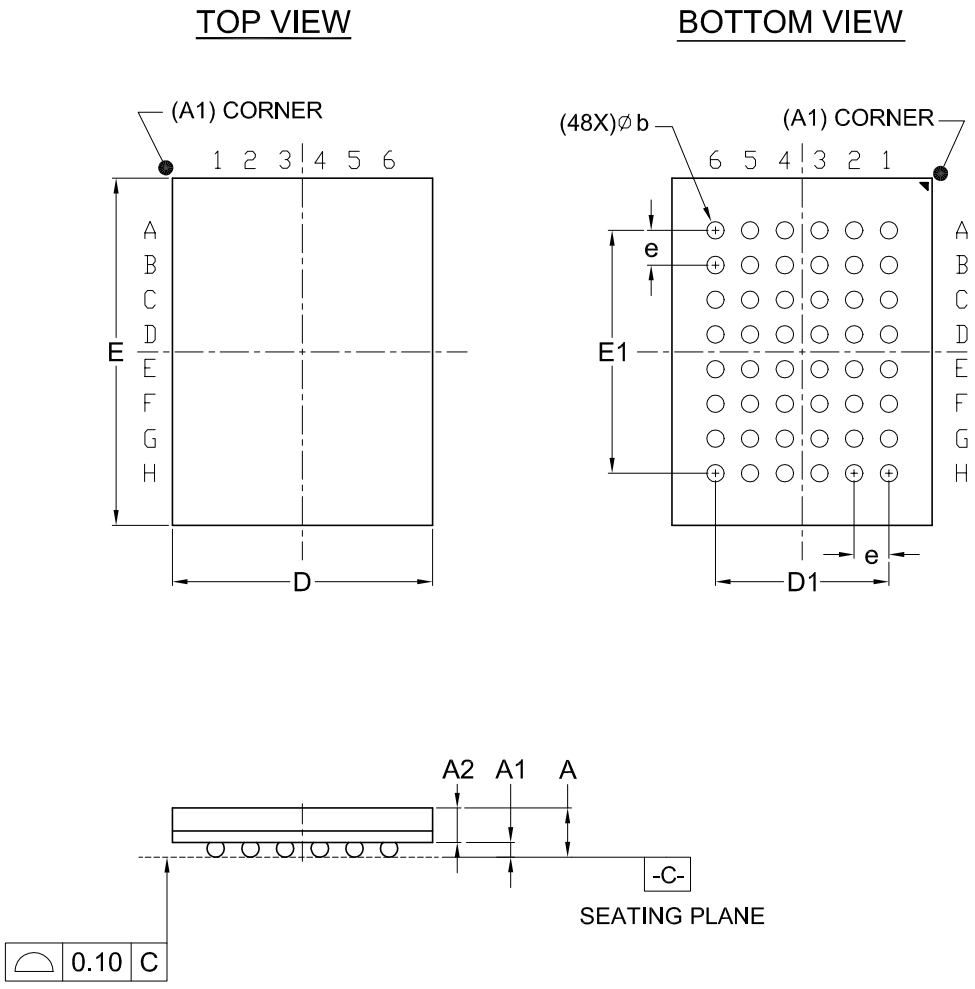
| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.25 | 0.65 | 0.35 | 5.90 | | 7.90 | | |
| | Nom. | --- | 0.30 | --- | 0.40 | 6.00 | 4.00 | 8.00 | 5.60 | 0.80 |
| | Max. | 1.30 | 0.35 | --- | 0.45 | 6.10 | | 8.10 | | |
| Inch | Min. | — | 0.010 | 0.026 | 0.014 | 0.232 | | 0.311 | | |
| | Nom. | — | 0.012 | — | 0.016 | 0.236 | 0.157 | 0.315 | 0.220 | 0.031 |
| | Max. | 0.051 | 0.014 | — | 0.018 | 0.240 | | 0.319 | | |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-4202 | 5 | MO-219 | | | |


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**48-Ball TFBGA (for MX29LV160D TXGI/BXGI)**

Doc. Title: Package Outline for CSP 48BALL (6X8X1.2MM , BALL PITCH 0.8MM , DIAMETER 0.4MM)




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | — | 0.25 | 0.65 | 0.35 | 5.90 | --- | 7.90 | — | — |
| | Nom. | — | 0.30 | — | 0.40 | 6.00 | 4.00 | 8.00 | 5.60 | 0.80 |
| | Max. | 1.20 | 0.35 | — | 0.45 | 6.10 | --- | 8.10 | — | — |
| Inch | Min. | — | 0.010 | 0.026 | 0.014 | 0.232 | --- | 0.311 | — | — |
| | Nom. | — | 0.012 | --- | 0.016 | 0.236 | 0.157 | 0.315 | 0.220 | 0.031 |
| | Max. | 0.047 | 0.014 | --- | 0.018 | 0.240 | --- | 0.319 | — | — |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-4258 | 1 | MO-219 | | | |


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## REVISION HISTORY

| Revision No. | Description | Page | Date |
|---|---|---|---|
| 1.0 | 1. Changed Icr1 from 7mA(typ.) to 5mA(typ.) | P5,30 | AUG/11/2008 |
| | 2. Removed "Advanced Information" | P5 | |
| 1.1 | 1. Revised data retention from 10 years to 20 years | P5-6,56 | MAY/18/2009 |
| | 2. Added TXGI/BXGI ordering information and part name information (TFBGA PACKAGE) | P57-58,64 | |
| | 3. Added Tsrw (AC/WAVEFORM, Min. 45ns) | P32,34 | |
| | 4. Added WP#ACC PIN note | P9 | |
| 1.2 | 1. Modified description for RoHS compliance | P5,58 | DEC/22/2011 |
| | 2. Modified Figure 11. CE# Controlled Write Timing Waveform | P42 | |


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