# MX29GL512G / MX68GL1G0G

## SINGLE VOLTAGE 3V ONLY FLASH MEMORY

### *Key Features*

- *2.7 to 3.6 volts for read, erase, and program operations*
- *64KW/128KB uniform equal sectors architecture*
- *16 word page read buffer/256 word write buffer*
- *Program/Erase Suspend & Program/Erase Resume*

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## SINGLE VOLTAGE 3V ONLY FLASH MEMORY

# 1. FEATURES

### GENERAL FEATURES

- Power Supply Operation
  - 2.7 to 3.6 volts for read, erase, and program operations
    - H/L: VI/O=VCC=2.7V to 3.6V, VI/O voltage must tight with VCC
    - U/D: VI/O=1.65V to 3.6V for Input/Output
- Byte/Word mode switchable
  - 512Mb: 67,108,864 x 8 / 33,554,432 x 16
  -1Gb: 134,217,728 x 8 / 67,108,864 x 16
- 64KW/128KB uniform equal sectors architecture
- 32 byte/16 word page read buffer
- 256 word write buffer
- Extra 512 word sector for security
  - Features factory locked and identifiable, and customer lockable
- Latch-up protected to 100mA from -1V to 1.5xVcc
- Low Vcc write inhibit : Vcc ≤ VLKO
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash

### PERFORMANCE

- High Performance
  - Fast access time:
    - H/L: 100ns
    - U/D: 110ns
  - Page access time:
    - H/L: 15ns
    - U/D: 25ns
  - Word program time: 30us
  - Write Buffer Program Through: 1.8MB/Sec, 2.6MB/Sec with Accelerated Program mode
  - Sector erase time: 0.25sec
- Low Power Consumption
  - Low active read current: 12mA (typ.) at 5MHz
  - Low standby current: 512Mb/1Gb: 20/40uA (typ.)
  -Deep power down current: 3uA(typ.)
- 100,000 erase/program cycle
- 20 years data retention

### SOFTWARE FEATURES

- Program/Erase Suspend & Program/Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
  - Suspends sector program operation to read data from another sector which is not being program
- Support Common Flash Interface (CFI)
- Advanced sector protection function (Solid and Password Protect)
- Status Register(Data Polling/Toggle), Extended Status Register(volatile bit) and Ready/Busy pin methods to determine device status
- Deep power down mode


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## HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
  - Hardware write protect pin/Provides accelerated program capability
- BYTE# input pin
  - Selects 8 bits or 16 bits mode

## PACKAGE

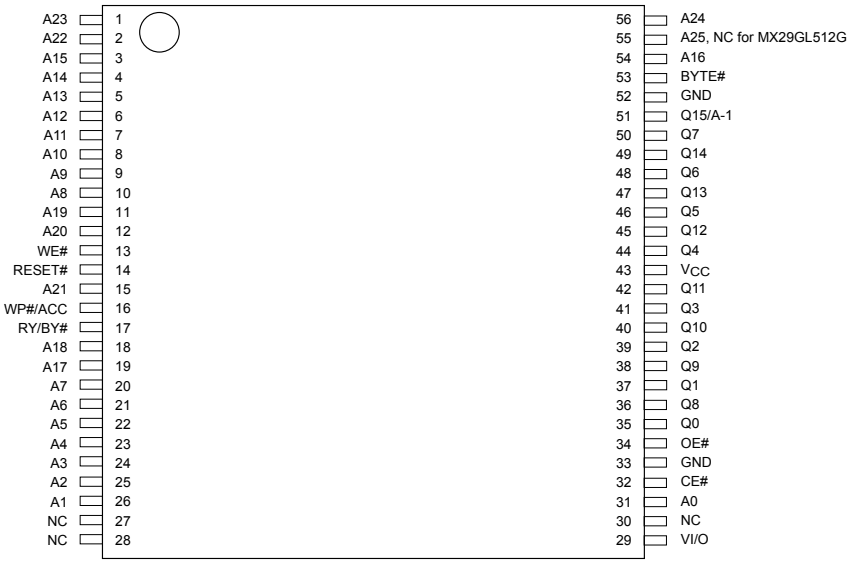
- 56-Pin TSOP
- 64-Ball LFBGA (11mm x 13mm)
- **All devices are RoHS Compliant and Halogen-free**


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## 2. PIN CONFIGURATION

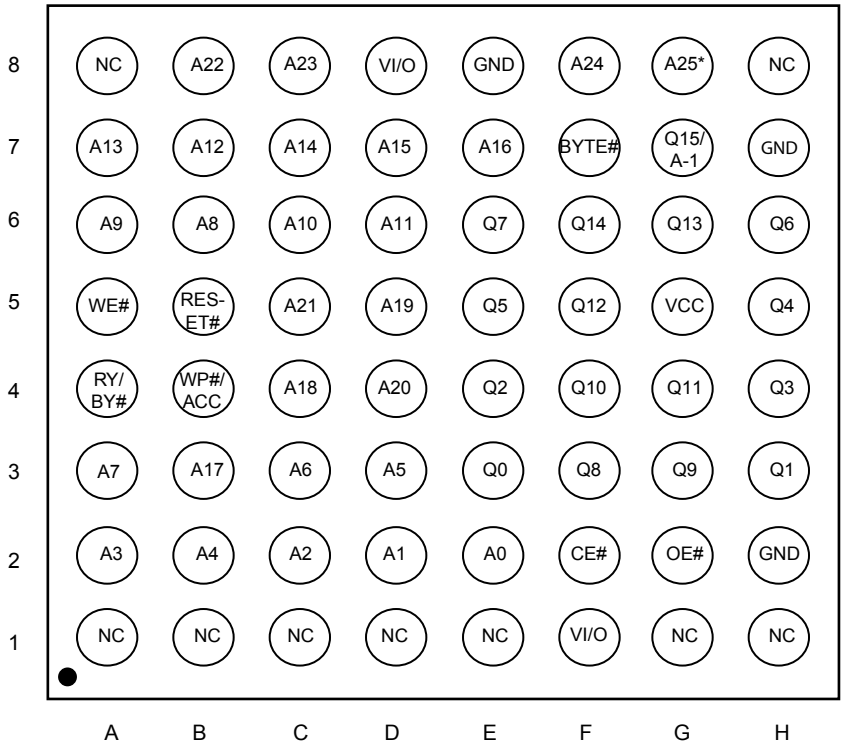
### 56 TSOP

**Top View**




### 64 LFBGA

**Top View**




Note: * G8(A25) is NC for MX29GL512G



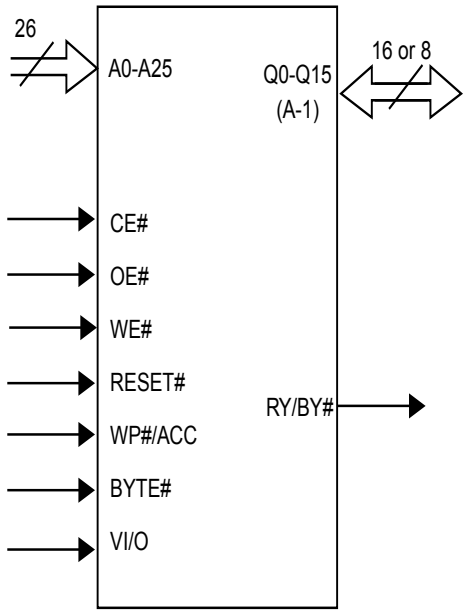
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## 3. PIN DESCRIPTION

| SYMBOL | PIN NAME |
|---|---|
| A0~A25 | Address Input<br>A0~A24 is for MX29GL512G<br>A0~A25 is for MX68GL1G0G |
| Q0~Q14 | Data Inputs/Outputs |
| Q15/A-1 | Q15(Word Mode)/LSB addr(Byte Mode) |
| CE# | Chip Enable Input |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| RESET# | Hardware Reset Pin, Active Low |
| WP#/ACC * | Hardware Write Protect/Program Acceleration input |
| RY/BY# | Ready/Busy Output |
| BYTE# * | Selects 8 bits or 16 bits mode |
| VCC | +3.0V single power supply |
| GND | Device Ground |
| NC | Pin Not Connected Internally |
| VI/O | Power Supply for Input/Output |

***Note:** WP#/ACC and BYTE# has internal pull up.

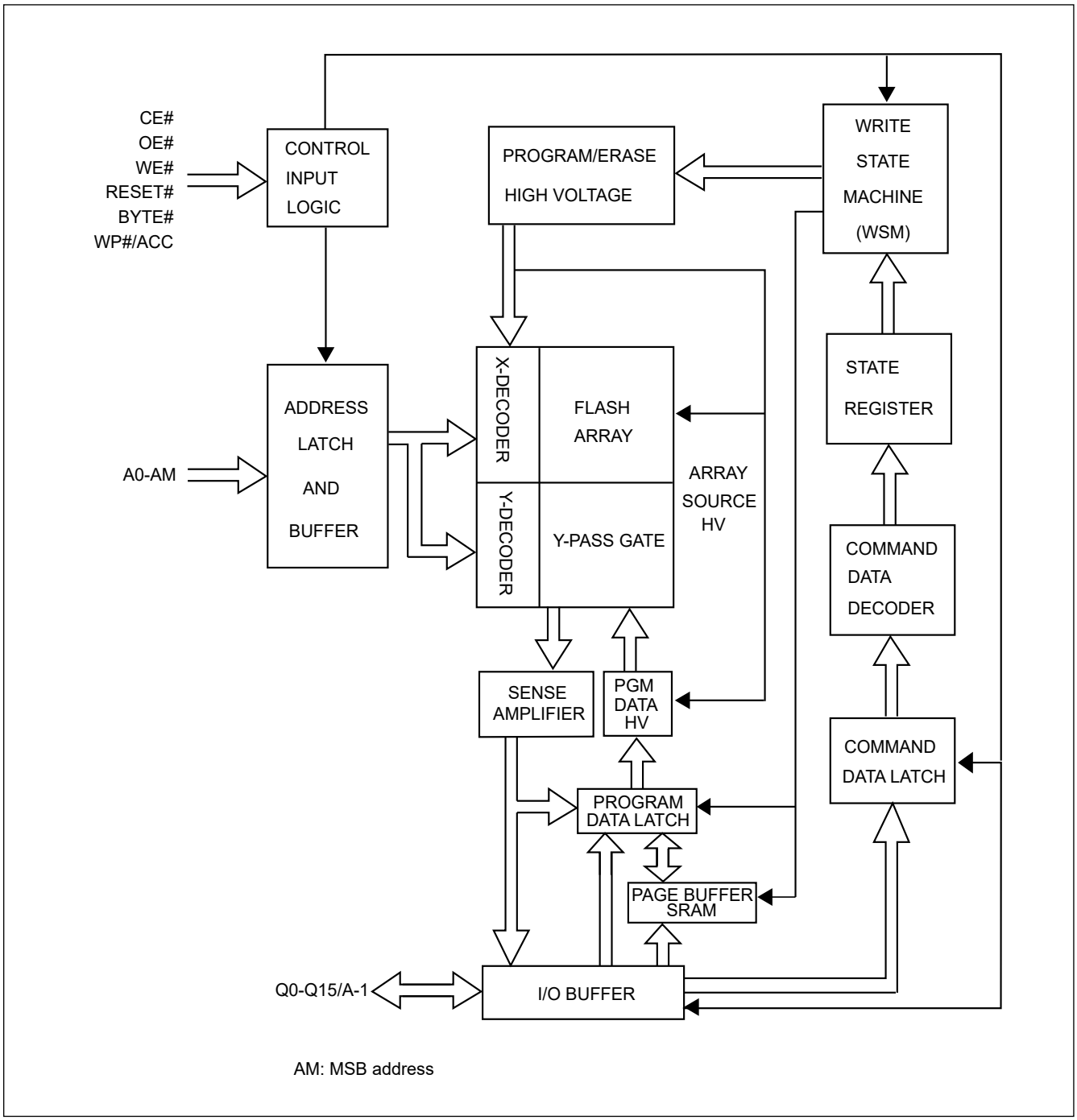
**LOGIC SYMBOL**





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## 4. BLOCK DIAGRAM



## 5. BLOCK DIAGRAM DESCRIPTION

The *"4. BLOCK DIAGRAM"* illustrates a simplified architecture of this device. Each block in the block diagram represents one or more circuit modules in the real chip used to access, erase, program, and read the memory array.

The "CONTROL INPUT LOGIC" block receives input pins CE#, OE#, WE#, RESET#, BYTE#, and WP#/ACC. It creates internal timing control signals according to the input pins and outputs to the "ADDRESS LATCH AND BUFFER" to latch the external address pins A0-AM (AM=A24 is for MX29GL512G, AM=A25 is for MX68GL1G0G). The internal addresses are output from this block to the main array and decoders composed of "X-DECODER", "Y-DECODER", "Y-PASS GATE", AND "FLASH ARRAY". The X-DECODER decodes the word-lines of the flash array, while the Y-DECODER decodes the bit-lines of the flash array. The bit lines are electrically connected to the "SENSE AMPLIFIER" and "PGM DATA HV" selectively through the Y-PASS GATES. "SENSE AMPLIFIERS" are used to read out the contents of the flash memory, while the "PGM DATA HV" block is used to selectively deliver high power to bit-lines during programming. The "I/O BUFFER" controls the input and output on the Q0-Q15/A-1 pads. During read operation, the "I/O BUFFER" receives data from SENSE AMPLIFIERS and drives the output pads accordingly. In the last cycle of program command, the "I/O BUFFER" transmits the data on Q0-Q15/A-1 to "PROGRAM DATA LATCH", which controls the high power drivers in "PGM DATA HV" to selectively program the bits in a word or byte according to the user input pattern. During write-to-buffer sequence, the "I/O BUFFER" transmits the data on Q0-Q15 to PAGE BUFFER SRAM to store user data. After user has issued the confirm command, the data in PAGE BUFFER SRAM would transmit to PROGRAM DATA LATCH sequentially and program the data to flash memory cells through PGM DATA HV.

The "PROGRAM/ERASE HIGH VOLTAGE" block comprises the circuits to generate and deliver the necessary high voltage to the X-DECODER, FLASH ARRAY, and "PGM DATA HV" blocks. The logic control module comprises of the "WRITE STATE MACHINE, WSM", "STATE REGISTER", "COMMAND DATA DECODER", and "COMMAND DATA LATCH". When the user issues a command by toggling WE#, the command on Q0-Q15/A-1 is latched in the COMMAND DATA LATCH and is decoded by the COMMAND DATA DECODER. The STATE REGISTER receives the command and records the current state of the device. The WSM implements the internal algorithms for program or erase according to the current command state by controlling each block in the block diagram.

### ARRAY ARCHITECTURE

The main flash memory array can be organized as Byte mode (x8) or Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in *"6. BLOCK STRUCTURE"*.


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## 6. BLOCK STRUCTURE

**Table 1. MX29GL512G SECTOR ARCHITECTURE**

| Sector Size | | Sector | Sector Address A24-A16 | Address Range (x16) |
|---|---|---|---|---|
| Kbytes | Kwords | | | |
| 128 | 64 | SA0 | 000000000 | 0000000h-000FFFFh |
| 128 | 64 | SA1 | 000000001 | 0010000h-001FFFFh |
| 128 | 64 | SA2 | 000000010 | 0020000h-002FFFFh |
| : | : | : | : | : |
| 128 | 64 | SA511 | 111111111 | 1FF0000h-1FFFFFFh |

**Table 2. MX68GL1G0G SECTOR ARCHITECTURE**

| Sector Size | | Sector | Sector Address A25-A16 | Address Range (x16) |
|---|---|---|---|---|
| Kbytes | Kwords | | | |
| 128 | 64 | SA0 | 0000000000 | 0000000h-000FFFFh |
| 128 | 64 | SA1 | 0000000001 | 0010000h-001FFFFh |
| 128 | 64 | SA2 | 0000000010 | 0020000h-002FFFFh |
| : | : | : | : | : |
| 128 | 64 | SA1023 | 1111111111 | 3FF0000h-3FFFFFFh |


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## 7. BUS OPERATION

**Table 3. BUS OPERATION**

| Mode Select | RE-SET# | CE# | WE# | OE# | Address (Note4) | Data I/O Q7~Q0 | Byte# Vil Data (I/O) Q15~Q8 | Byte# Vih Data (I/O) Q15~Q8 | WP#/ ACC |
|---|---|---|---|---|---|---|---|---|---|
| Device Reset | L | X | X | X | X | HighZ | HighZ | HighZ | L/H |
| Standby Mode | Vcc ± 0.3V | Vcc± 0.3V | X | X | X | HighZ | HighZ | HighZ | H |
| Output Disable | H | L | H | H | X | HighZ | HighZ | HighZ | L/H |
| Read Mode | H | L | H | L | AIN | DOUT | Q8-Q14= HighZ, Q15=A-1 | DOUT | L/H |
| Write | H | L | L | H | AIN | DIN | | DIN | *Note1*,*2* |
| Accelerate Program | H | L | L | H | AIN | DIN | | DIN | Vhv |

**Notes:**
1. The first or last sector was protected if WP#/ACC=Vil.
2. When WP#/ACC = Vih, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the advanced protect feature.
3. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
4. In Word Mode (Byte#=Vih), the addresses are AM to A0, AM: MSB of address.
   In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15), AM: MSB of address.


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# 8. FUNCTIONAL OPERATION DESCRIPTION

## 8-1. READ OPERATION

To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving CE# & OE# LOW, and WE# HIGH. After the Tce and Toe timing requirements have been met, the system can read the contents of the addressed location by reading the Data (I/O) pins. If either the CE# or OE# is held HIGH, the outputs will remain tri-stated and no data will appear on the output pins.

## 8-2. PAGE READ

This device is able to conduct Macronix compatible high performance page read. Page size is 32 bytes or 16 words. The higher address Amax ~ A4 select the certain page, while A3~A0 for word mode, A3~A-1 for byte mode select the particular word or byte in a page. The page access time is Taa or Tce, following by Tpa for the rest of the page read time. When CE# toggles, access time is Taa or Tce. Page mode can be turned on by keeping "page-read address" constant and changing the "intra-read page" addresses.

## 8-3. WRITE OPERATION

To perform a write operation, the system provides the desired address on the address pins, enables the chip by asserting CE# LOW, and disables the Data (I/O) pins by holding OE# HIGH. The system then places data to be written on the Data (I/O) pins and pulses WE# LOW. The device captures the address information on the falling edge of WE# and the data on the rising edge of WE#. To see an example, please refer to the timing diagram in *"Figure 18. COMMAND WRITE TIMING WAVEFORM (WE# CONTROLLED)".* The system is not allowed to write invalid commands (commands not defined in this datasheet) to the device. Writing an invalid command may put the device in an undefined state.

## 8-4. DEVICE RESET

Driving the RESET# pin LOW for a period of Trp or more will return the device to Read mode. If the device is in the middle of a program or erase operation, the reset operation will take at most a period of Tready1 before the device returns to Read mode. Until the device does returns to Read mode, the RY/BY# pin will remain Low (Busy Status).

When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

## 8-5. STANDBY MODE

The device enters Standby mode whenever the RESET# and CE# pins are both held High except in the embedded mode. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (Isb) current.


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## 8-6. OUTPUT DISABLE

While in active mode (RESET# HIGH and CE# LOW), the OE# pin controls the state of the output pins. If OE# is held HIGH, all Data (I/O) pins will remain tri-stated. If held LOW, the Byte or Word Data (I/O) pins will drive data.

## 8-7. BYTE/WORD SELECTION

The BYTE# input pin is used to select the organization of the array data and how the data is input/output on the Data (I/O) pins. If the BYTE# pin is held HIGH, Word mode will be selected and all 16 data lines (Q0 to Q15) will be active.

If BYTE# is forced LOW, Byte mode will be active and only data lines Q0 to Q7 will be active. Data lines Q8 to Q14 will remain in a high impedance state and Q15 becomes the A-1 address input pin.

## 8-8. HARDWARE WRITE PROTECT

By driving the WP#/ACC pin LOW. The highest or lowest was protected from all erase/program operations. If WP#/ACC is held HIGH (Vih to VCC), these sectors revert to their previously protected/unprotected status.

## 8-9. ACCELERATED PROGRAM OPERATION

By applying high voltage (Vhv) to the WP#/ACC pin, the device will enter the Accelerated Program mode. This mode permits the system to skip the normal command unlock sequences and program byte/word locations directly. During accelerated program, the current drawn from the WP#/ACC pin is no more than Icp1.

## 8-10. WRITE BUFFER PROGRAM OPERATION

Programs 256 word in word mode program and 256 byte in byte mode program operation. To trigger the Write Buffer Program, start by the first two unlock cycles, then third cycle writes the Write Buffer Load command at the destined program Sector Address. The forth cycle writes the "word locations subtract one" number.

Following above operations, system starts to write the mingling of address and data. After the programming of the first address or data, the "write-buffer-page" is selected. The following data should be within the above mentioned page.

The "write-buffer-page" is selected by choosing address Amax~A8.

"Write-Buffer-Page" address has to be the same for all address/data write into the write buffer. If not, operation will ABORT.

To program the content of the write buffer page this command must be followed by a write to buffer Program confirm command.

The operation of write-buffer can be suspended or resumed by the standard commands, once the write buffer program operation is finished, it'll return to normal READ mode.


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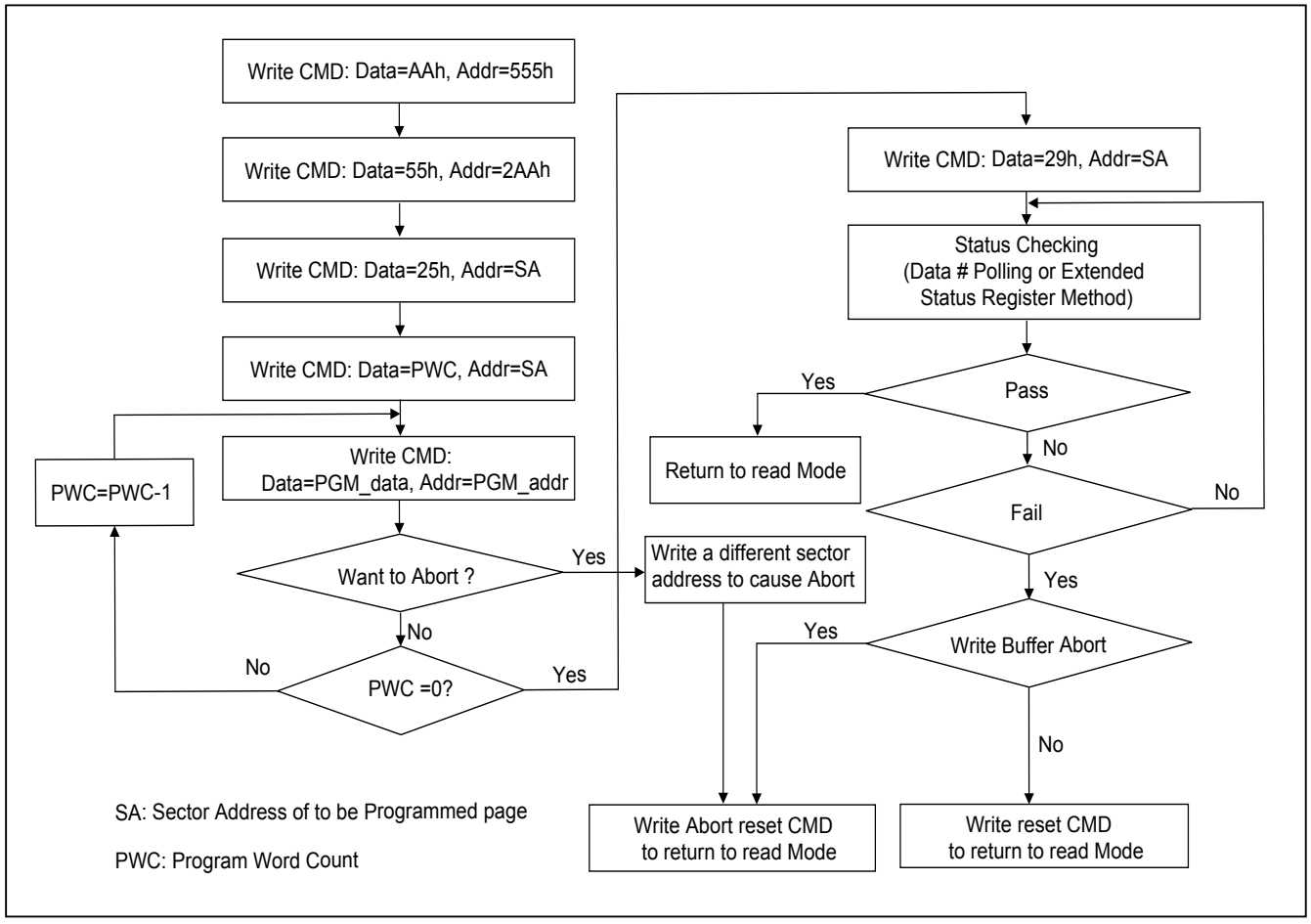
ABORT will be executed for the Write Buffer Program Sequence if following condition occurs:

- The value loaded is bigger than the page buffer size during "Number of Locations to Program"
- Address written in a sector is not the same as the one assigned during the Write-Buffer-Load command.
- Address/Data pair written to a different write-buffer-page than the one assigned by the "Starting Address" during the "write buffer data loading" operation.
- Writing not "Confirm Command" after the assigned number of "data load" cycles.

At Write Buffer Abort mode, the status register will be Q1=1, Q7=DATA# (last address written), Q6=toggle.
A Write-to-Buffer-Abort Reset command sequence has to be written to reset the device for the next operation.

Write buffer program can be conducted in any sequence. However the CFI functions, autoselect, Security sector are not functional when program operation is in progress. Multiple write buffer program operations on the same write buffer address range without intervening erases is available. Any bit in a write buffer address range can't be programmed from 0 back to 1.

**Figure 1. WRITE BUFFER PROGRAM FLOWCHART**



### 8-11. SECTOR PROTECT OPERATION

The device provides user programmable protection operations for selected sectors. Please refer to *"6. BLOCK STRUCTURE"* which show all Sector assignments.

During the protection operation, the sector address of any sector may be used to specify the sector being protected.

### 8-12. AUTOMATIC SELECT OPERATIONS

Automatic Select mode is used to access the manufacturer ID, device ID and CFI code. The automatic select mode has four command cycles. There are 2 methods to enter automatic select mode, user can issues the autoselect commands or applies the high voltage on the A9 pin. Please see AUTOMATIC SELECT OPERATIONS in the COMMAND OPERATIONS section.

### 8-13. INHERENT DATA PROTECTION

To avoid accidental erase or program of the device, the device is automatically reset to Read mode during power up. Additionally, the following design features protect the device from unintended data corruption.

### 8-14. COMMAND COMPLETION

Only after the successful completion of the specified command sets will the device begin its erase or program operation. The failure in observing valid command sets will result in the memory returning to read mode.

### 8-15. LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than VLKO and write commands are ignored until Vcc is greater than VLKO. The system must provide proper signals on control pins after Vcc rises above VLKO to avoid unintentional program or erase operations.

### 8-16. WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

### 8-17. LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# at Vih, or OE# at Vil.


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### 8-18. POWER-UP SEQUENCE

Upon power up, the device is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

### 8-19. POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

### 8-20. POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.


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# 9. COMMAND OPERATIONS

## 9-1. READING THE MEMORY ARRAY

Read mode is the default state after power up or after a reset operation. To perform a read operation, please refer to READ OPERATION in the BUS OPERATIONS section above.

If the device receives an Erase Suspend command while in the Sector Erase state, the erase operation will pause (after a time delay not exceeding Tesl period) and the device will enter Erase-Suspended Read mode. While in the Erase-Suspended Read mode, data can be programmed or read from any sector not being erased. Reading from addresses within sector(s) being erased will only return the contents of the status register, which is in fact how the current status of the device can be determined.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the device will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where is was suspended and will continue until it completes successfully or another Erase Suspend command is received.

After the memory device completes an embedded operation (automatic Chip Erase, Sector Erase, or Program) successfully, it will automatically return to Read mode and data can be read from any address in the array. If the embedded operation fails to complete, as indicated by status register bit Q5 (exceeds time limit flag) going HIGH during the operations, the system must perform a reset operation to return the device to Read mode.

There are several states that require a reset operation to return to Read mode:

1. A program or erase failure--indicated by status register bit Q5 going HIGH during the operation. Failures during either of these states will prevent the device from automatically returning to Read mode.

2. The device is in Auto Select mode or CFI mode. These two states remain active until they are terminated by a reset operation.

In the two situations above, if a reset operation (either hardware reset or software reset command) is not performed, the device will not return to Read mode and the system will not be able to read array data.

## 9-2. AUTOMATIC PROGRAM OF THE MEMORY ARRAY

The device provides the user the ability to program the memory array in Byte mode or Word mode. As long as the users enters the correct cycle defined in the *"Table 9. COMMAND DEFINITIONS"* (including 2 unlock cycles and the A0H program command), any byte or word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for program and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the program process, the user only needs to enter the program command and data once.

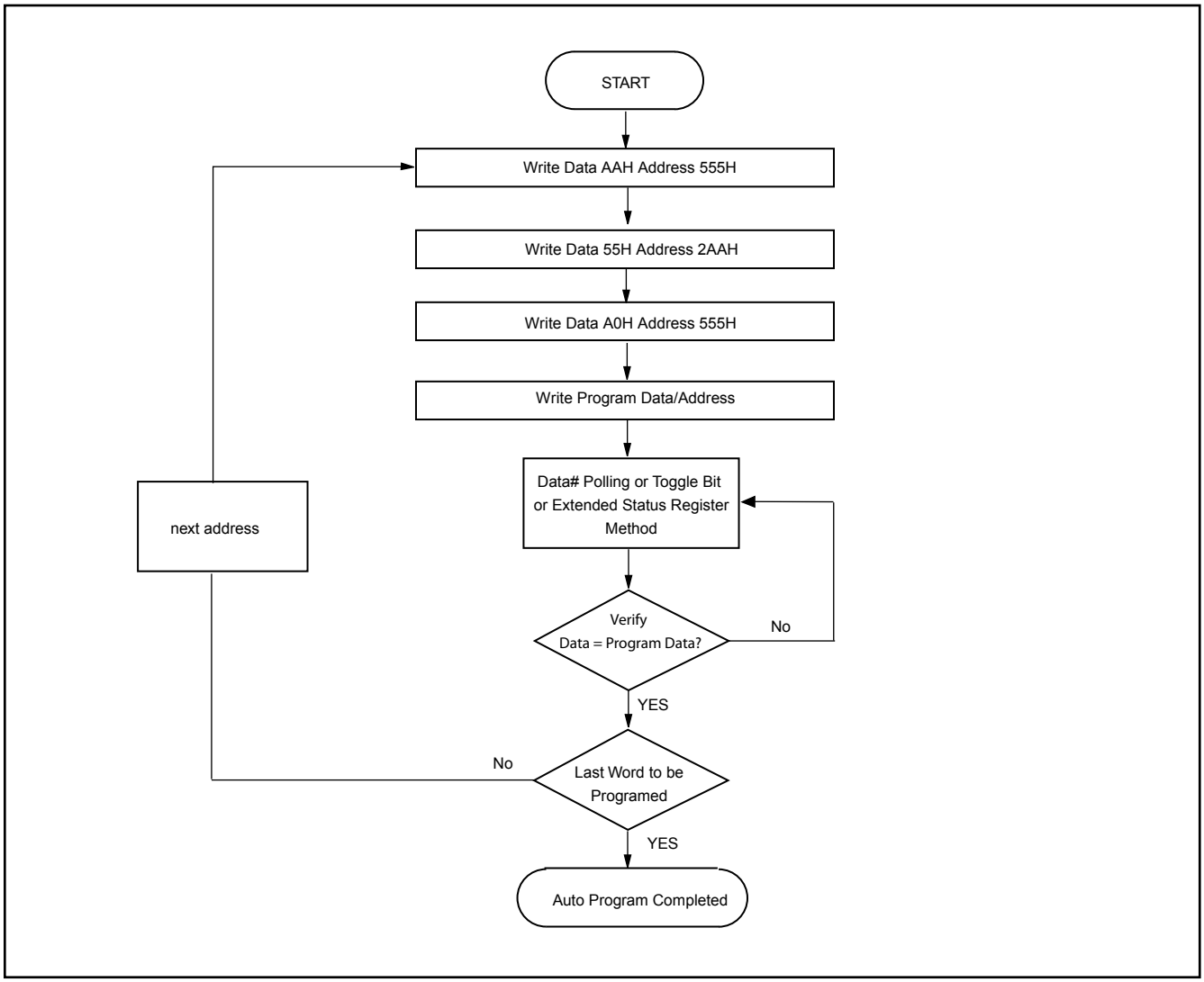

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Program will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by program. This can only be done by an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset or program suspend. Hardware reset will terminate the program operation after a period of time no more than 10us. When the embedded program algorithm is complete or the program operation is terminated by a hardware reset, the device will return to Read mode. Program suspend ready, the device will enter program suspend read mode.

Please refer to the following figure for automatic programming flowchart.

**Figure 2. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART**




After the embedded program operation has begun, the user can check for completion by reading the following bits in the status register.


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## 9-3. ERASING THE MEMORY ARRAY

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. In the Sector Erase operation, the selected sector shall be erased. In the Chip Erase operation, the complete memory array is erased except for any protected sectors. More details of the protected sectors are explained in Section *"9-17. ADVANCED SECTOR PROTECTION/UNPROTECTION"*.

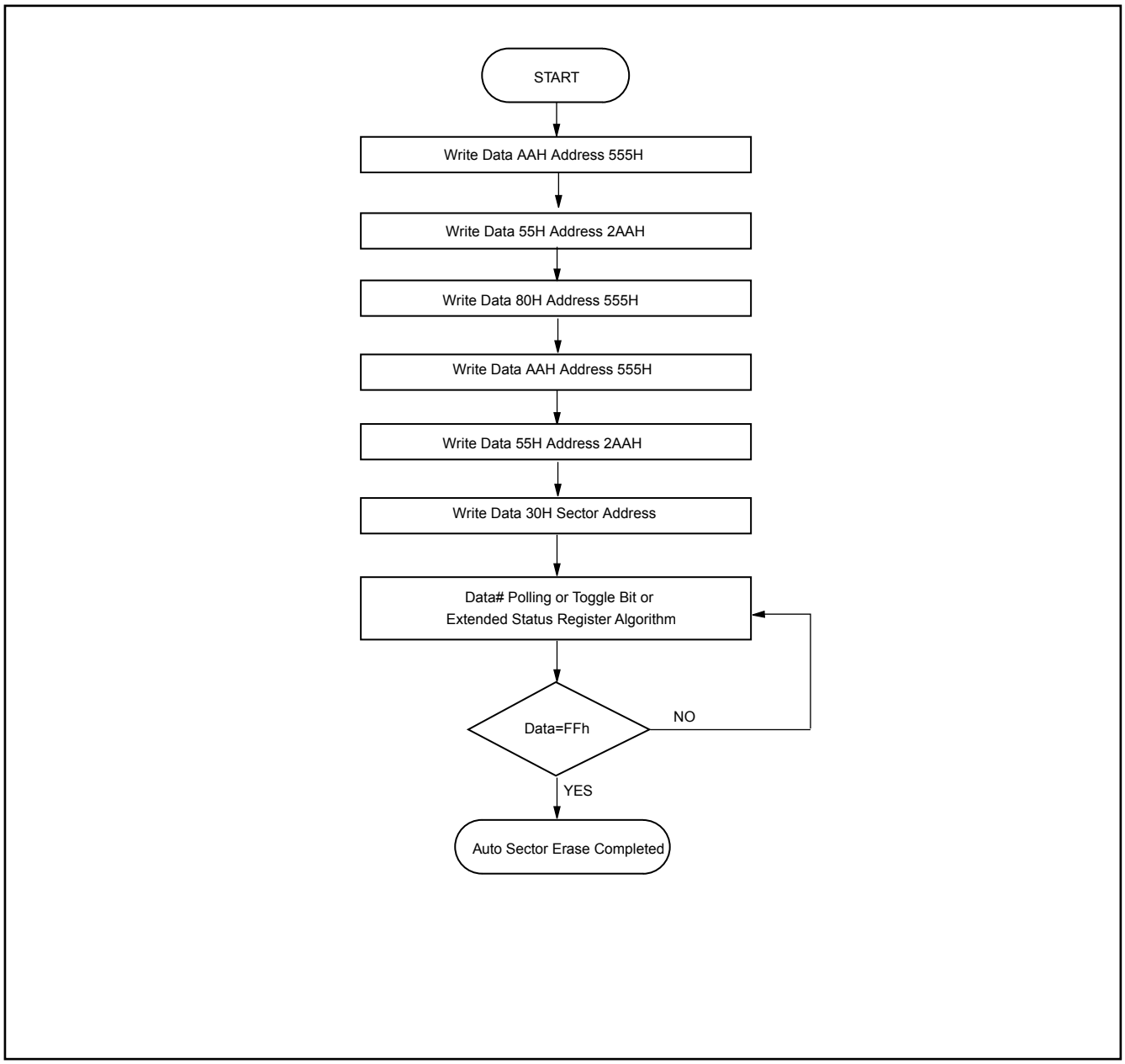
## 9-4. SECTOR ERASE

The sector erase operation is used to clear data within a sector by returning all of its memory locations to the "1" state. It requires six command cycles to initiate the erase operation. The first two cycles are "unlock cycles", the third is a configuration cycle, the fourth and fifth are also "unlock cycles", and the sixth cycle is the Sector Erase command.

After the embedded sector erase operation begins, all commands except Erase Suspend and Extended Status Register Read will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode. Please refer to the following figure for sector erase flowchart.


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**Figure 3. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART**




The system can determine the status of the automatic sector erase operation by the status register, see the STATUS REGISTER for the details.

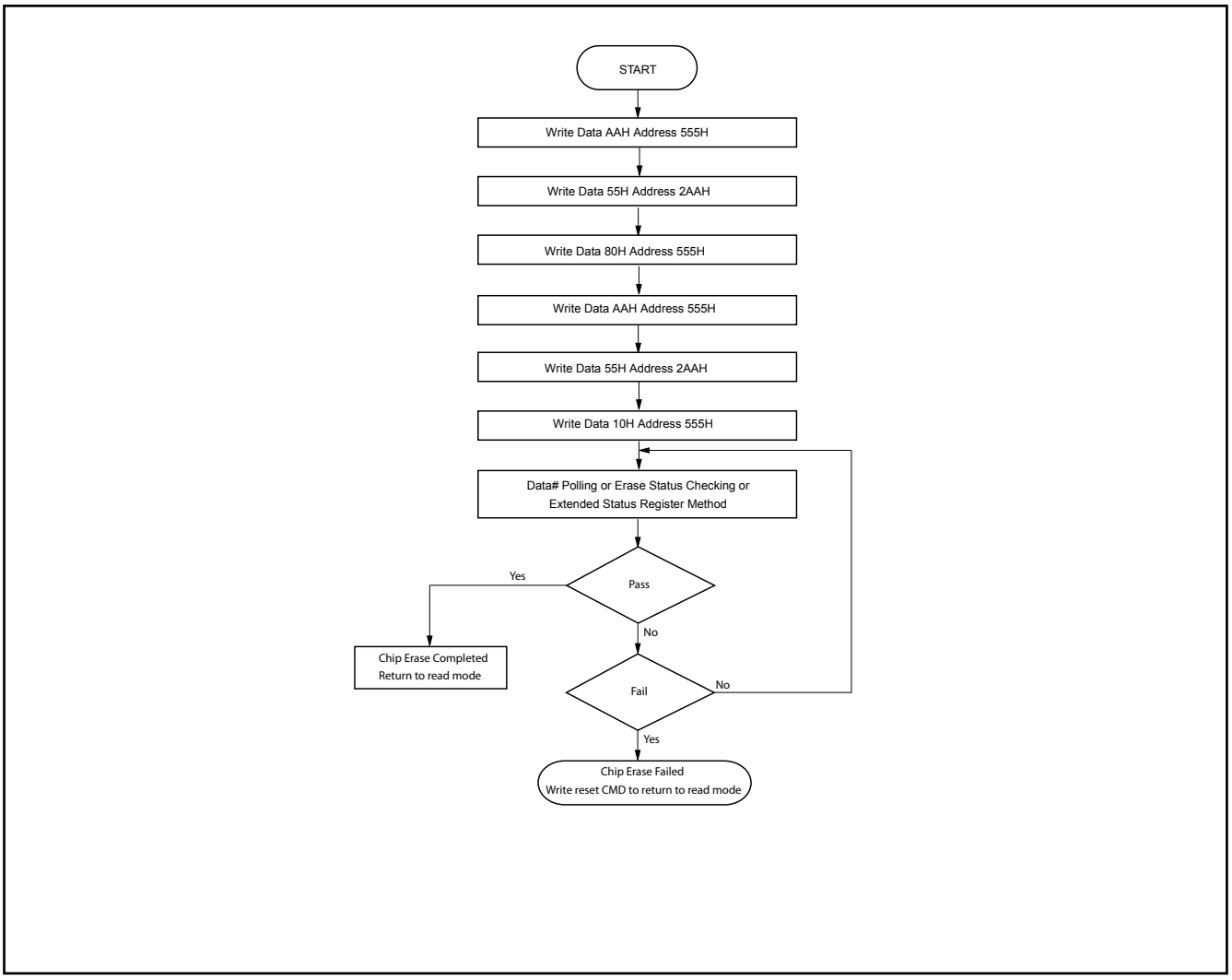

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## 9-5. CHIP ERASE

The Chip Erase operation is used erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 6 write cycles to initiate the action. The first two cycles are "unlock" cycles, the third is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle initiates the chip erase operation.

During the chip erase operation, no other software commands will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase, the chip will automatically return to Read mode. See following figure for chip erase flowchart.

**Figure 4. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART**




The system can determine the status of the embedded chip erase operation by the status register, see the STATUS REGISTER for the details.


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## 9-6. ERASE SUSPEND/RESUME

After beginning a sector erase operation, Erase Suspend and read Extended Status Register are the valid commands that may be issued. If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended Read mode until Tesl period has elapsed. The system can determine if the device has entered the Erase-Suspended Read mode through Q6, Q7, and RY/BY# of Status Register or Extended Status Register.

After the device has entered Erase-Suspended Read mode, the system can read or program any sector (s) except this suspended sector. Reading this sector being erased will return the contents of status register. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another erase command. See following figure for erase suspend/resume flowchart.

## 9-7. SECTOR ERASE RESUME

The sector Erase Resume command is valid only when the device is in Erase-Suspended Read mode. After erase resumes, the user can issue another Ease Suspend command, but there should be a Ters interval between Ease Resume and the next Erase Suspend command.

## 9-8. PROGRAM SUSPEND/RESUME

After beginning a program operation, Program Suspend and read Extended Status Register are the valid commands that may be issued. If the system issues an Program Suspend command after the program operation has already begun, the device will not enter Program-Suspended Read mode until Tpsl period has elapsed. The system can determine if the device has entered the Program-Suspended Read mode through Q6 and RY/BY# of Status Register or Extended Status Register.

After the device has entered Program-Suspended mode, the system can read any sector(s) except those being programmed by the suspended program operation. Reading the sector being program suspended is invalid. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another program command. The system can use the status register bits shown in the following table to determine the current state of the device, see the STATUS REGISTER for the details.

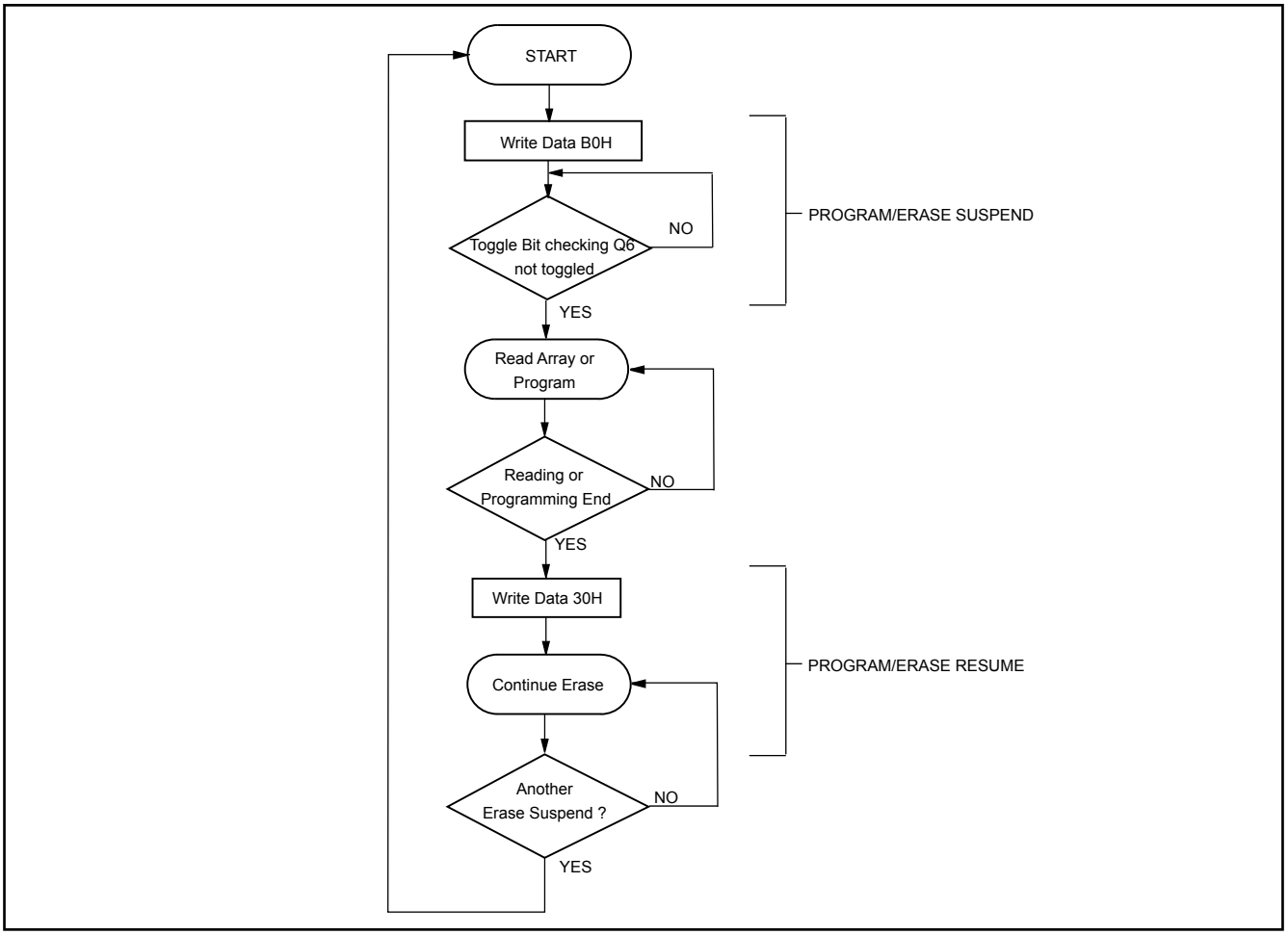
When the device has Program/Erase suspended, user can execute read array, auto-select, read CFI, read security sector.

## 9-9. PROGRAM RESUME

The Program Resume command is valid only when the device is in Program-Suspended mode. After program resumes, the user can issue another Program Suspend command, but there should be a Tprs interval between Program Resume and the next Program Suspend command.


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**Figure 5. PROGRAM/ERASE SUSPEND/RESUME ALGORITHM FLOWCHART**




The system can use the status register bits shown in the following table to determine the current state of the device, see the STATUS REGISTER for the details.

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as Automatic select, program, CFI query and erase resume.

### 9-10. BLANK CHECK

Blank Check command can check if the erase operation works correctly in the selected sector. During the Blank Check, array read operation will return the contents of status register.

Write data 33h to address 555h into the sector to start the Blank Check.

In the following operations, Blank Check may not be written successfully:

1. program
2. erase
3. suspend

Device Ready (bit 7) of Extended Status Register or Status Register can display if the Blank Check is in progress or not.
Erase status (bit 5) of the Extended Status Register or Status Register can display the blank check result.


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### 9-11. BUFFER WRITE ABORT

Status register Q1 is the indicator of Buffer Write Abort. When Q1=1, the device will abort from buffer write and go back to read, see WRITE BUFFER PROGRAMMING OPERATION for the details.

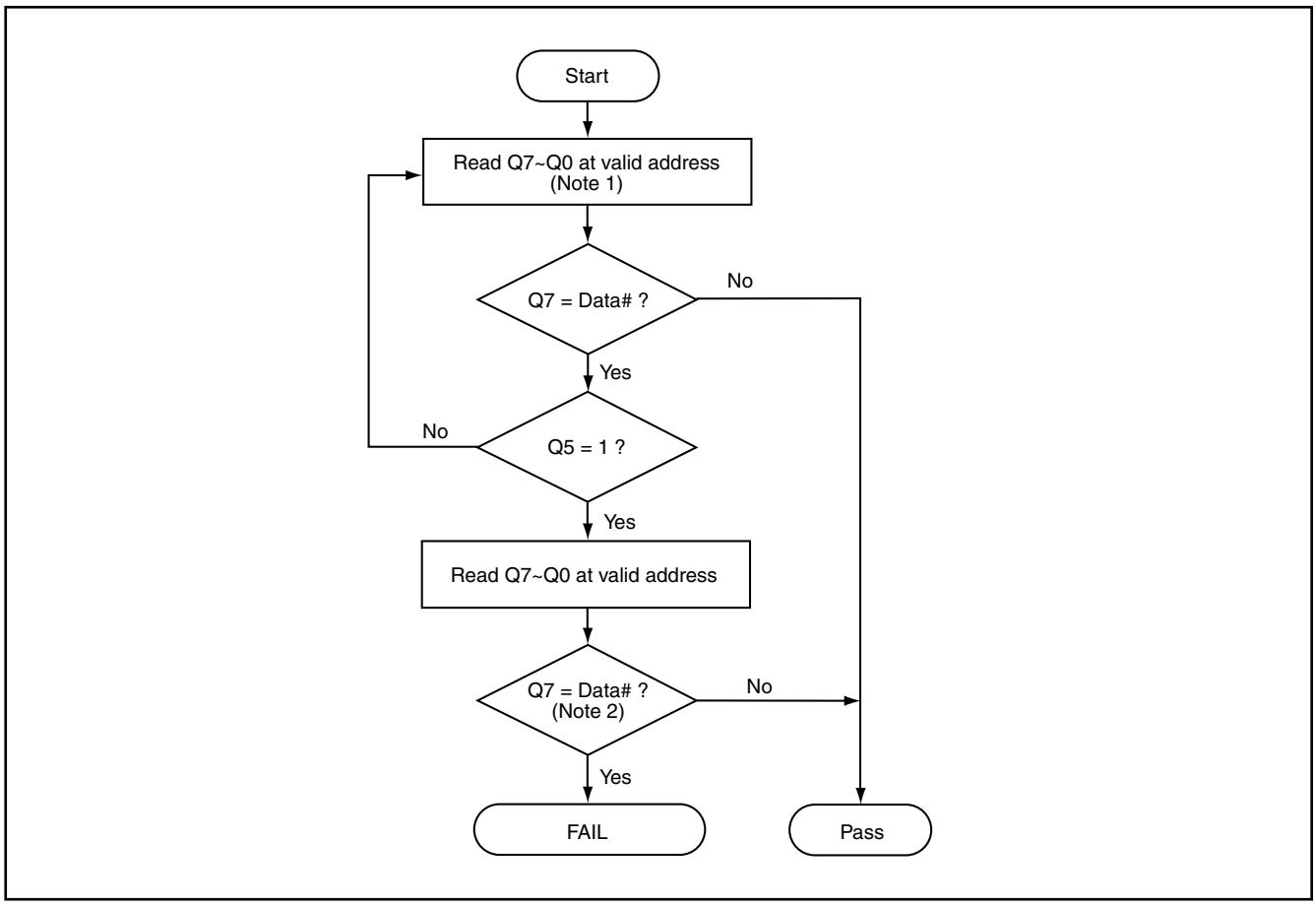
### 9-12. PROGRAM/ERASE STATUS CHECKING METHOD

When the device program/erase operation is in progress, either the "Polling Method", "Toggle Bit Method" or Extended Status Register" may be used to monitor the operation:

#### 9-12-1. Polling Method:

The polling method checks Q7 (data complement bit) and Q5 (time out bit) values during the operation. After the operation has fisnished, Q7 will output true data. See the following figures for the word program/erase and write buffer program flowchart respectively.

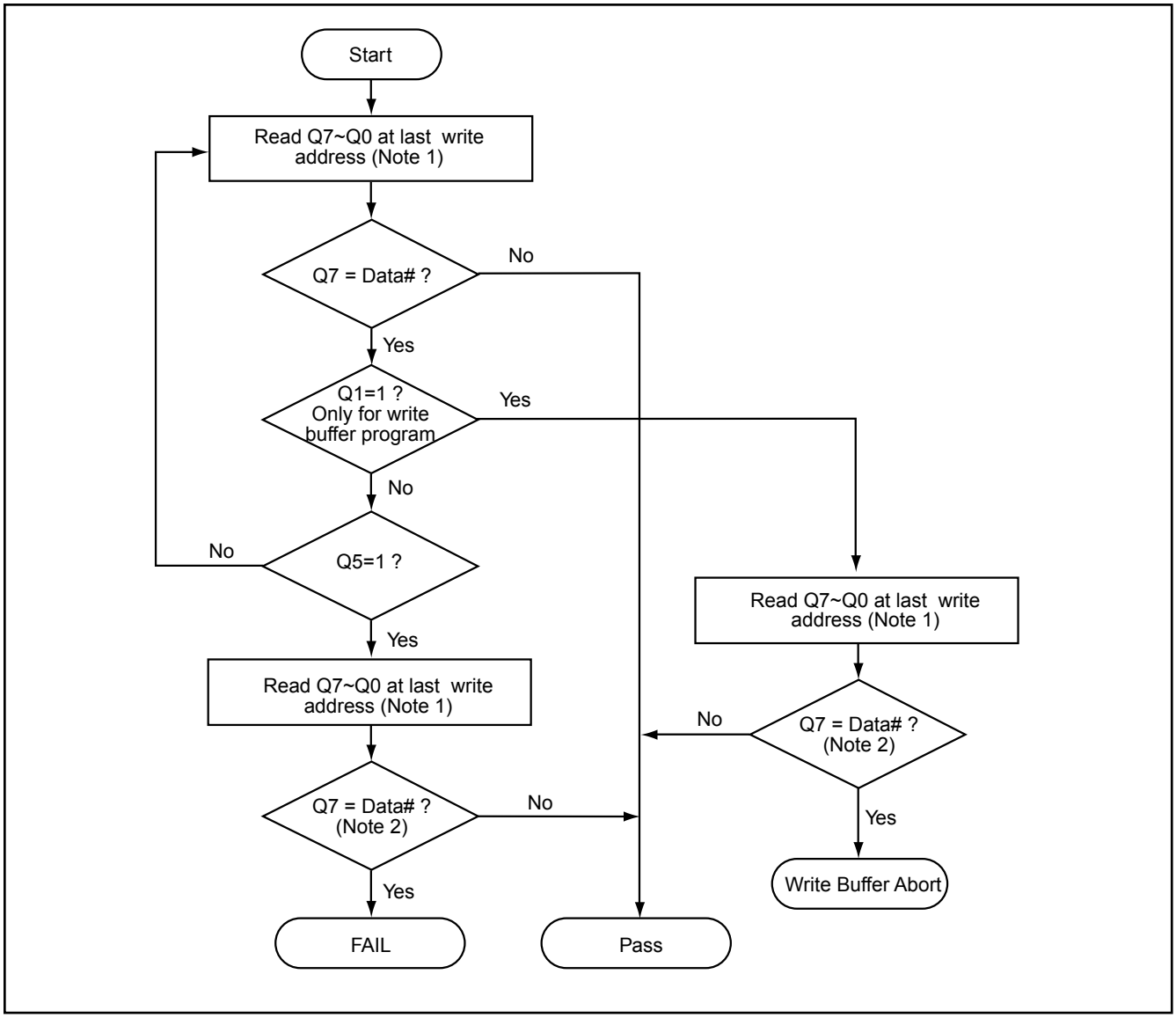
**Figure 6. STATUS POLLING FOR WORD PROGRAM/ERASE**




**Notes:**
1. For program, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.


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**Figure 7. STATUS POLLING FOR WRITE BUFFER PROGRAM**



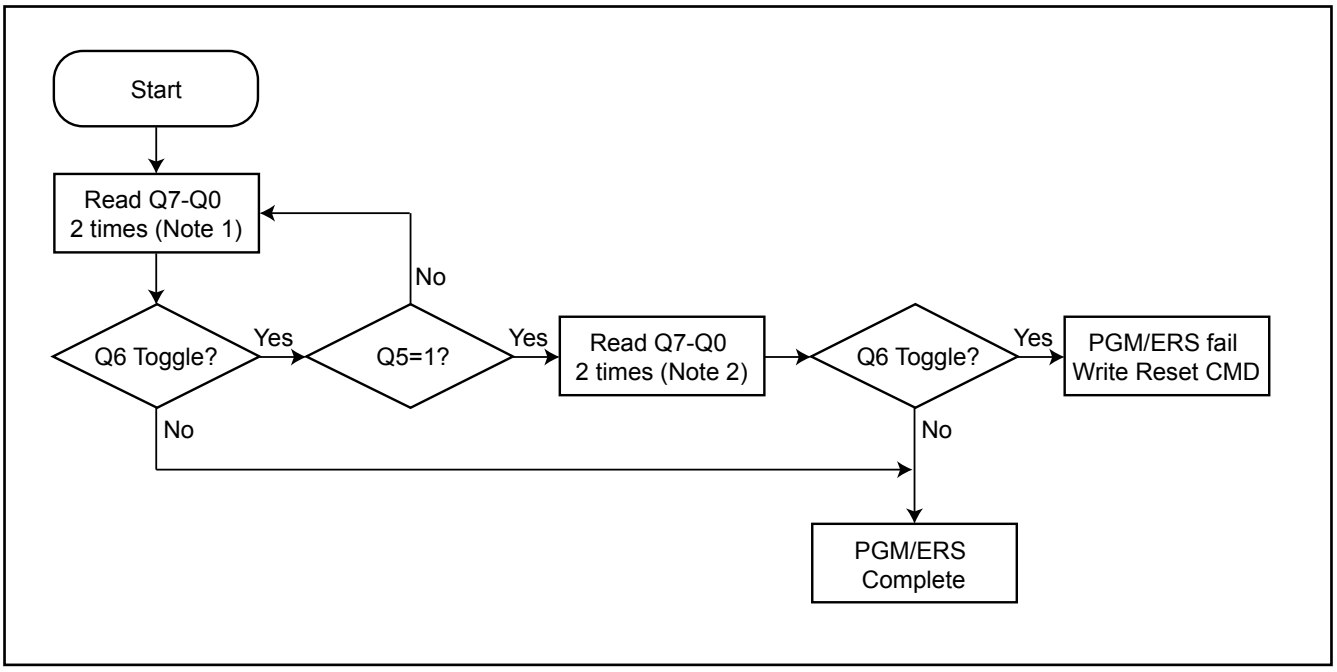

**Notes:**
1. For write to buffer programming, valid address means last write address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.


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### 9-12-2. Toggle Bit Method:

The toggle bit method checks Q6 (toggle bit) value during the operation. After the operation has fisnished, Q6 will stop toggling. Please refer to the following figure for the toggle bit flowchart.

**Figure 8. TOGGLE BIT ALGORITHM**




**Notes:**
1. Repeat Q7~Q0 read command 2 times to verify toggling status.
2. Q6 may stop toggling when Q5 switches to "1", need to verify toggling status once again.

### 9-12-3. Extended Status Register

Extended Status Register is a 16-bits register, which contains the program and erase status. These bits indicate whether the specific operations has completed successfully through the following bits:

- Erase Status (bit 5),
- Program Status (bit 4),
- Write Buffer Abort Status (bit 3),
- Sector Locked Status (bit 1)


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Extended Status Register can also refer to whether the current status is in process, suspended, or completed through:
• Device Ready (bit 7),
• Erase Suspended Status (bit 6)
• Program Suspended Status (bit 2)

Bits 15:8 and bits 0 are reserved and must be regarded as don't care from any software reading status. Please refer to Extended Status Register Table for further information.

**Table 4. EXTENDED STATUS REGISTER**

| Bit # | 15:8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| Description | Reserved | DRB (Device Ready) | ESSB (Erase Suspend Status) | ESB (Erase Status) | PSB (Program Status) | WBASB (Write Buffer Abort Status) | PSSB (Program Suspend Status) | SLSB (Sector Lock Status) | Reserved |
| Reset Status | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | X |
| Status Description | X | 1=Ready, 0=Busy | 0=No Erase in Suspension 1=Erase in Suspension | 0=Erase successful 1=Erase fail | 0=Program successful 1=Program fail | 0=Program not aborted 1=Program aborted during Write to Buffer command | 0=No Program in suspension 1=Program in suspension | 0=Sector not locked during operation 1=Sector locked error | X |

**Notes:**
1. While any operation is in progress, Bit 7=0 (busy). Bits 6 thru 1 are invalid while bit 7 = 0
2. User must read status continuously until DRB (Device Ready) becomes ready (=1) before issuing the Erase Suspend or Program Suspend Command.
3. Erase Resume Command will clear ESSB (Erase Suspend Status) to 0. Program Resume Command will clear PSSB (Program Suspend Status) to 0.
4. Program on erase suspended sector will result in Program fail (PSB [Program Status]=1).
5. SLSB (Sector Lock Status) represents the status of program or erase operation. While SLSB=1, it indicates that a program or erase operation has failed since the sector was locked.

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The Status information could be retrieved by performing the Read Extended Status Register command and a following read operation. When Read Extended Status Register Command has been written, the device captures the status information on the rising edge of WE#, and then places the status information in the device address locations.

The Clear Extended Status Register Command or reset command will clear these results related Extended Status Register bits (bit 5, bit 4, bit 3 and bit 1) to 0 without affecting the current state bits (bit 7, bit 6, and bit 2).

It's recommended to use Extended Status Register instead of Data Polling Status feature to determine device status. See the following figure for the Write Buffer Program and sector erase flowchart.

**Figure 9. EXTENDED STATUS REGISTER FOR WRITE BUFFER PROGRAM**

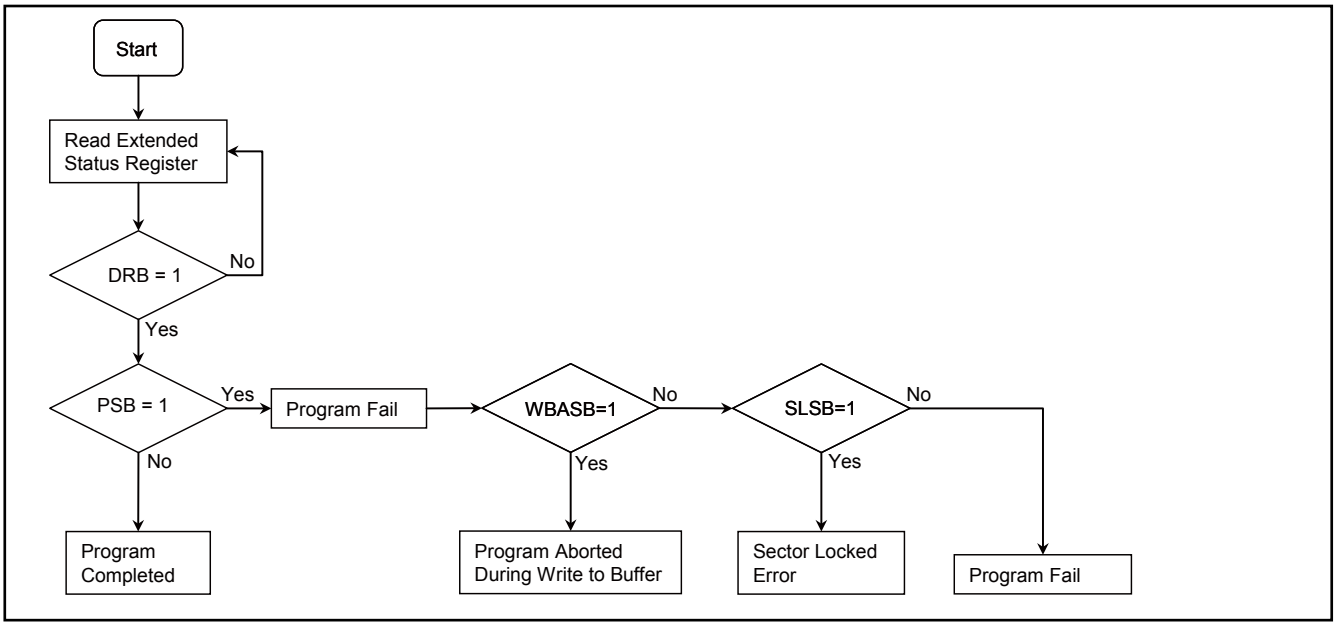
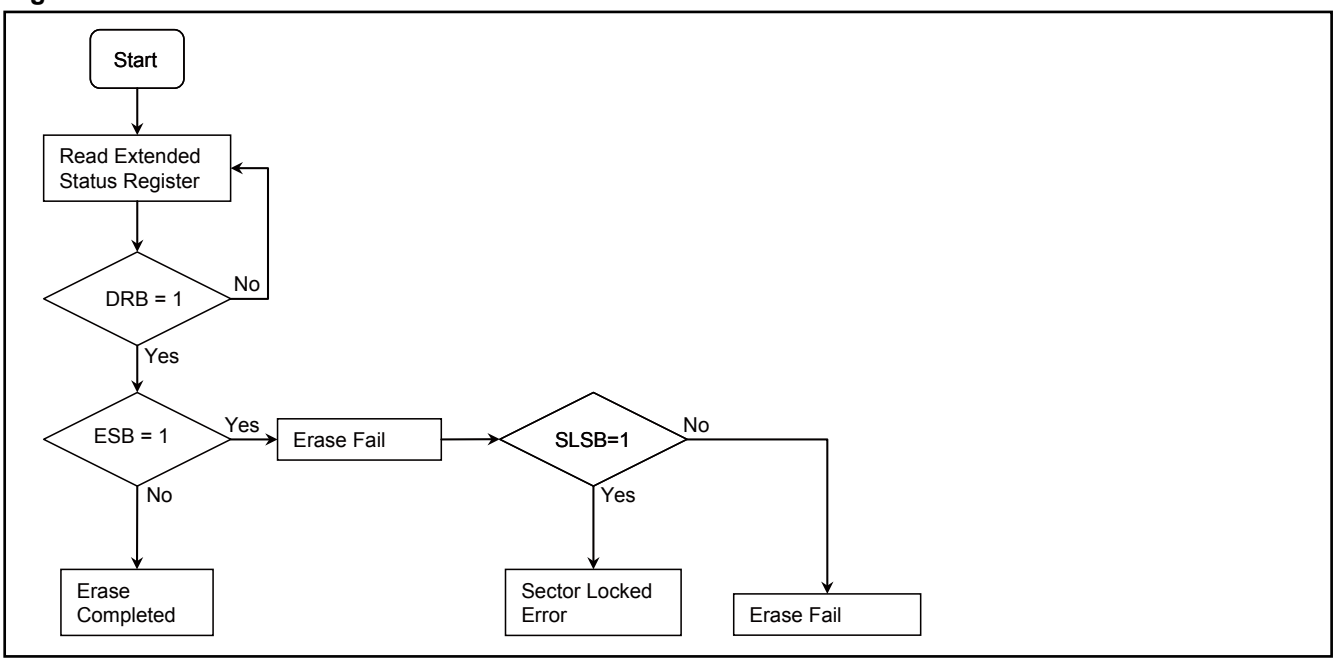



**Figure 10. EXTENDED STATUS REGISTER FOR SECTOR ERASE**





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## 9-13. STATUS REGISTER

The host system can use the status register bits shown in the following table to determine the current state of the device.

**Table 5. STATUS REGISTER**

| Status | | Q7 | Q6 | Q5 | Q3 | Q2 | Q1 | RY/BY# |
|---|---|---|---|---|---|---|---|---|
| Automatic programming | In progress | Q7# | Toggle | 0 | N/A | N/A | 0 | 0 |
| | Exceed time limit | Q7# | Toggle | 1 | N/A | N/A | N/A | 0 |
| Sector erase | In progress | 0 | Toggle | 0 | 1 | Toggle | N/A | 0 |
| | Exceed time limit | 0 | Toggle | 1 | 1 | Toggle | N/A | 0 |
| Chip erase | In progress | 0 | Toggle | 0 | N/A | Toggle | N/A | 0 |
| | Exceed time limit | 0 | Toggle | 1 | N/A | Toggle | N/A | 0 |
| Program suspend read | program suspended sector | Invalid | | | | | | 1 |
| | non-program suspended sector | Data | | | | | | 1 |
| Erase suspend read | erase suspended sector | 1 | No toggle | 0 | N/A | Toggle | N/A | 1 |
| | non-erase suspended sector | Data | | | | | | 1 |
| Erase suspend program in non-erase suspended sector | | Q7# | Toggle | 0 | N/A | N/A | N/A | 0 |
| Buffer Write | Busy | Q7# | Toggle | 0 | N/A | N/A | 0 | 0 |
| | Abort | Q7# | Toggle | 0 | N/A | N/A | 1 | 0 |
| | Exceed time limit | Q7# | Toggle | 1 | N/A | N/A | 0 | 0 |

**Notes:**
1. RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.
2. Erase Suspend and Read Extended Status Register are the valid commands that may be issued once the sector erase operation is in progress.
3. RY/BY# is open drain output pin and should be connected to VCC through a high value pull-up resistor.
4. When an attempt is made to erase only protected sector (s), the erase operation will abort thus preventing any data changes in the protected sector (s). Q7 will output "0" and Q6 will toggle briefly (100us or less) before aborting and returning the device to Read mode.
5. Q2 is a localized indicator showing a specified sector is undergoing erase operation or not. Q2 toggles when user reads at addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode).


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## 9-14. AUTOMATIC SELECT OPERATIONS

When the device is in Read mode, Program Suspended mode, Erase-Suspended Read mode, or CFI mode, the user can issue the Automatic Select command shown in *"Table 9. COMMAND DEFINITIONS"* (two unlock cycles followed by the Automatic Select command 90h) to enter Automatic Select mode. After entering Automatic Select mode, the user can query the Manufacturer ID, Device ID, Security Sector locked status, or Sector protected status multiple times without issuing a new Automatic Select command.

While In Automatic Select mode, issuing a Reset command (F0h) will return the device to Read mode (or Ease-Suspended Read mode if Erase-Suspend was active) or Program Suspended Read mode if Program Suspend was active.

### 9-14-1. AUTOMATIC SELECT COMMAND SEQUENCE

The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The Reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

**Table 6. AUTOMATIC SELECT ID VALUE**

| | Address (h) | | Data (h) | | |
|---|---|---|---|---|---|
| | Word Mode | Byte Mode | | | |
| Manufacturer ID | 00 | 00 | C2 | | |
| Device ID | 01/0E/0F | 02/1C/1E | | Word Mode | Byte Mode |
| | | | 512Mb | 227E/2223/2201 | 7E/23/01 |
| | | | 1Gb | 227E/2228/2201 | 7E/28/01 |
| Sector Protect Verify | (Sector address) 02 | (Sector address) 04 | 0: Sector Unprotected<br>1: Sector Protected | | |
| Security Sector Status | 03 | 06 | Bit15-Bit8 = 1 (Reserved)<br>Bit7: Factory Locked Area<br>1 = Locked, 0 = Unlocked<br>Bit6: Customer Locked Area<br>1 = Locked, 0 = Unlocked<br>Bit5 = 1 (Reserved)<br>Bit4: WP# Protects<br>0 = lowest address Sector protected<br>1 = highest address Sector protected<br>Bit3-Bit0 = 1 (Reserved) | | |
| Command Set Support | 0C | 18 | Bit15-Bit4 = 0 (Reserved)<br>Bit3-Bit2: Command Set<br>11/10=reserved,<br>01= Short version, 00= Full version<br>Bit1: Data# Polling<br>1=support, 0 =not support<br>Bit0: Extended Status Register<br>1=support, 0=not support | | |

**Notes:**
Page read feature is not support, while read address 02h or read between any other ID addresses and 02h.
After entering automatic select mode, no other commands are allowed except the reset command.


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### 9-14-2. AUTOMATIC SELECT HIGH VOLTAGE OPERATION

Another way to enter Automatic Select mode is to use high voltage operations as following Table. After the high voltage (Vhv) is removed from the A9 pin, the device will automatically return to Read mode or Erase-Suspended Read mode.

**Table 7. AUTOMATIC SELECT HIGH VOLTAGE OPERATION**

| Item | Control Input | | | AM to A12 | A11 to A10 | A9 | A8 to A7 | A6 | A5 to A4 | A3 to A2 | A1 | A0 | Q7 ~ Q0 | Q15 ~ Q8 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CE# | WE# | OE# | | | | | | | | | | | |
| Sector Protect Verify | L | H | L | SA | X | $V_{hv}$ | X | L | X | L | H | L | 01h or 00h *(Note 1)* | X |
| Security Sector Status | L | H | L | X | X | $V_{hv}$ | X | L | X | L | H | H | *(Note 2)* | X |
| Read Manufacturer ID | L | H | L | X | X | $V_{hv}$ | X | L | X | L | L | L | C2H | X |
| Read Device ID -- 512Mb/1Gb | | | | | | | | | | | | | | |
| Cycle 1 | L | H | L | X | X | $V_{hv}$ | X | L | X | L | L | H | 7EH | 22H(Word), XXH(Byte) |
| Cycle 2 | L | H | L | X | X | $V_{hv}$ | X | L | X | H | H | L | 23H 512Mb 28H 1Gb | 22H(Word), XXH(Byte) |
| Cycle 3 | L | H | L | X | X | $V_{hv}$ | X | L | X | H | H | H | 01H | 22H(Word), XXH(Byte) |

**Notes:**
1. Sector unprotected code: 00h. Sector protected code:01h.
2. The factory lock status should be presented on data bit Q7, and customer lock status should be presented on data bit Q6, refer Table 6 for detail value.
3. AM: MSB of address.
4. Page read feature is not supported in automatic select high voltage operation.

### READ MANUFACTURER ID OR DEVICE ID

The Manufacturer ID (identification) is a unique hexadecimal number assigned to each manufacturer by the JEDEC committee. Each company has its own manufacturer ID, which is different from the ID of all other companies. The number assigned to Macronix is C2h.

To determine the Manufacturer ID Code, the system performs a READ OPERATION with A9 raised to Vhv and address pins A6, A3, A2, A1, & A0 held LOW. The Macronix ID code of C2h should be presented on data bits Q7 to Q0.


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### SECTOR LOCK STATUS VERIFICATION

To determine the protected state of any sector using bus operations, the system performs a READ OPERATION with A9 raised to Vhv, the sector address applied to the highest address pins A24/A25(512Mb/1Gb), address pins A6, A3, A2 & A0 held LOW, and address pin A1 held HIGH. If data bit Q0 is LOW, the sector is not protected, and if Q0 is HIGH, the sector is protected.

### READ SECURITY SECTOR STATUS

To determine if the Security Sector has been locked at the factory, the system performs a READ OPERATION with A9 raised to Vhv, address pin A6, A3 & A2 held LOW, and address pins A1 & A0 held HIGH. The factory lock status should be presented on data bit Q7, and customer lock status should be presented on data bit Q6, refer Table 4 for detail value.

## 9-15. COMMON FLASH MEMORY INTERFACE (CFI) QUERY COMMAND

The device features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h"/"AAh" (depending on Word/Byte mode), the device will enter the CFI Query Mode, any time the device is ready to read array data. The system can read CFI information at the addresses given in *Table 10* ~*Table 13*.

Once user enters CFI query mode, user can issue reset command to exit CFI mode and return to read array mode.

## 9-16. RESET

In the following situations, executing reset command will reset device back to Read mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Auto-select mode
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in Auto-Select mode, CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

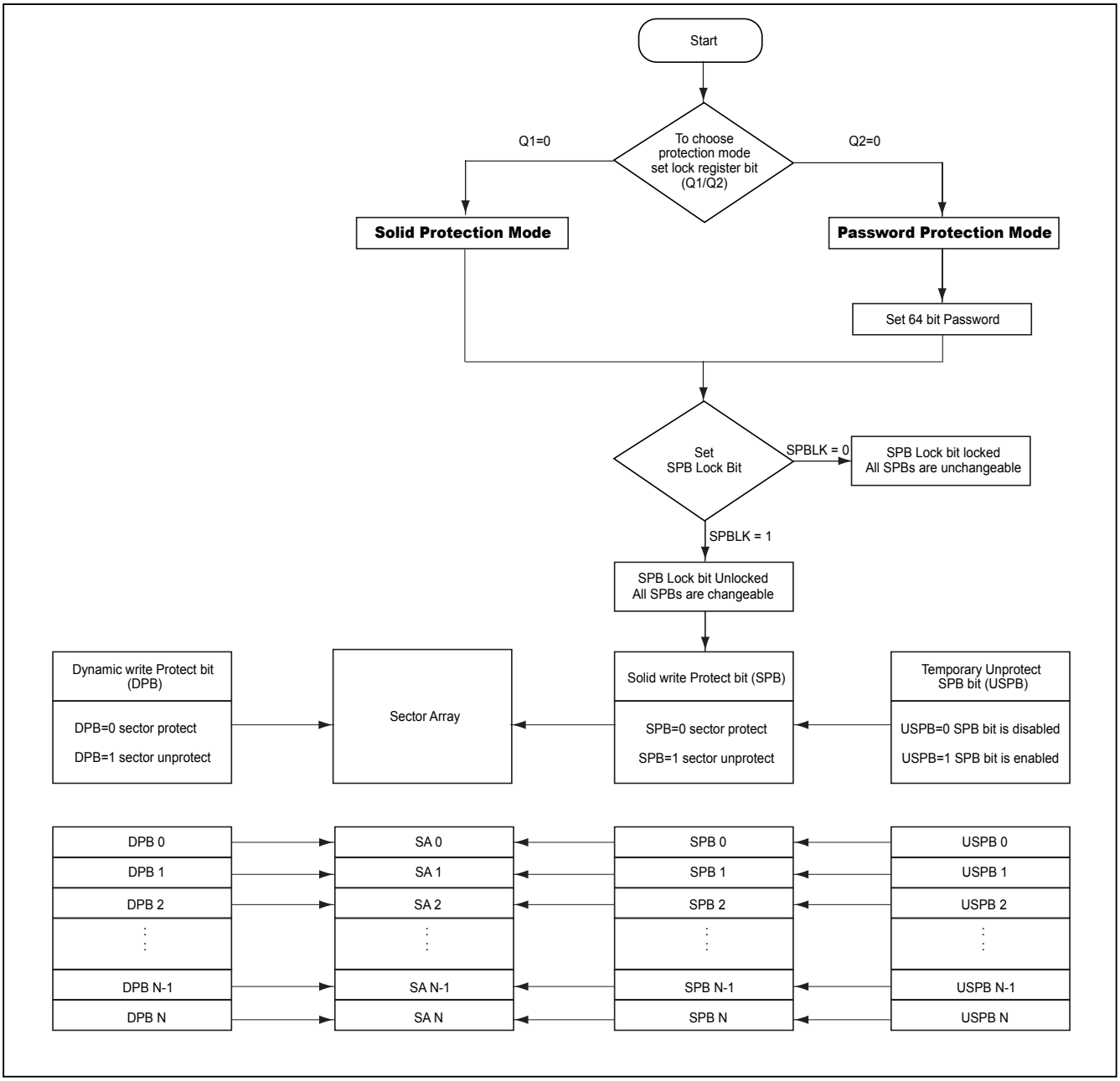

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## 9-17. ADVANCED SECTOR PROTECTION/UNPROTECTION

There are two ways to implement software Advanced Sector Protection on this device: Password method or Solid methods. Through these two protection methods, user can disable or enable the programming or erasing operation to any individual sector or the whole chip. The figure below helps to describe an overview of these methods.

The device is default to the Solid mode. All sectors are default as unprotected when shipped from factory.
The detailed algorithm of advance sector protection is shown as follows:

**Figure 11. ADVANCE SECTOR PROTECTION/UNPROTECTION SPB PROGRAM ALGORITHM**





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### 9-17-1. Lock Register

User can choose the sector protecting method via setting Lock Register bits as Q1 and Q2. Lock Register is a 16-bit one-time programmable register. Once programming either Q1 and Q2, they will be locked in that mode and the others will be disabled permanently. Q1 and Q2 can not be programmed at the same time, otherwise the device will abort the operation.

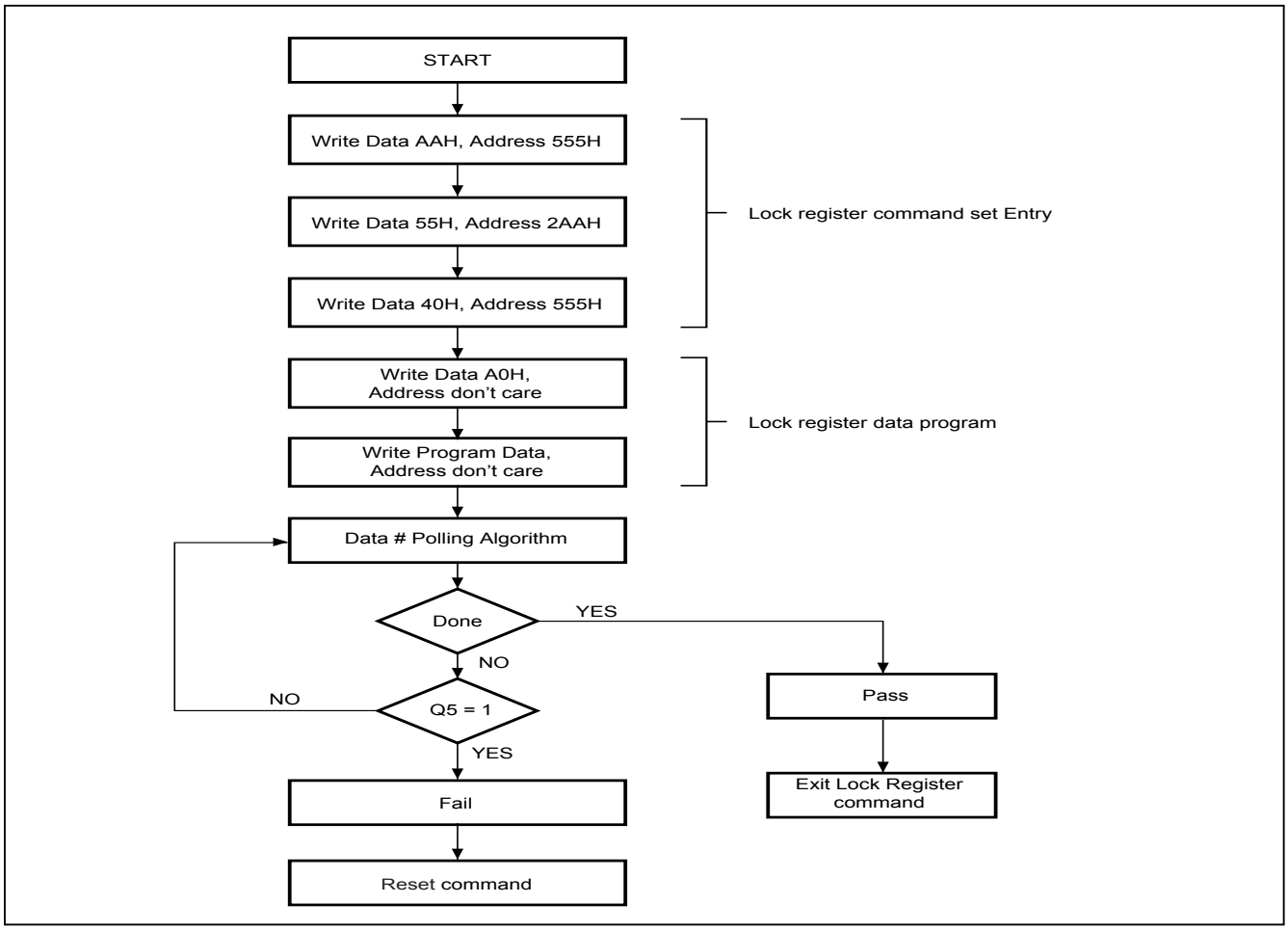
If users select Password Protection mode, the password setting is required. Users can set password by issuing password program command.

**Lock Register bits**

| Q15~Q7, Q5~Q3 | Q6 | Q2 | Q1 | Q0 |
|---|---|---|---|---|
| Reserved | Security Sector Customer Lock bit | Password Protection Mode Lock Bit | Solid Protection Mode Lock Bit | Security Sector Factory Lock bit |

Please refer to the command for Lock Register command set to read and program the Lock register.

**Figure 12. LOCK REGISTER PROGRAM ALGORITHM**





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### 9-17-2. Solid Protection Mode

**Solid write Protection Bits (SPB)**

The Solid write Protection bits (SPB) are nonvolatile bit with the same endurances as the Flash memory. Each SPB is assigned to each sector individually. The SPB is preprogrammed, and verified prior to erasure are managed by the device, so system monitoring is not necessary.

When SPB is set to "0", the associated sector may be protected, preventing any program or erase operation on this sector. Whether the sector is protected depends also upon the value of the USPB, as described elsewhere. The SPB bits are set individually by SPB program command. However, it cannot be cleared individually. Issuing the All SPB Erase command will erase all SPB in the same time. During SPB programming period, the read and write operations are disabled for normal sector until exiting this mode.

To unprotect a protected sector, the SPB lock bit must be cleared first by using a hardware reset or a power-up cycle. After the SPB lock bit is cleared, the SPB status can be changed to the desired settings. To lock the Solid Protection Bits after the modification has finished, the SPB Lock Bit must be set once again.

To verify the state of the SPB for a given sector, issuing a SPB Status Read Command to the device is required. Refer to the flow chart for details of SPB Program in *"Figure 13. SPB PROGRAM ALGORITHM"*.

**Dynamic Protection Bits (DPB)**

The Dynamic Protection features a volatile type protection to each individual sector. It can protect sectors from being unintentionally changed, and is easy to disable.

All Dynamic write Protection bit (DPB) can be modified individually. DPBs protect the unprotected sectors with their SPBs cleared. To modify the DPB status by issuing the DPB Set (to "0") or DPB Clear (to "1") commands, and place each sector in the protected or unprotected state separately. After the DPB Clear (to "1") command is issued, the sector may be modified depending on the SPB state of that sector.

The DPBs are default to be cleared (to "1") when first shipped from factory.


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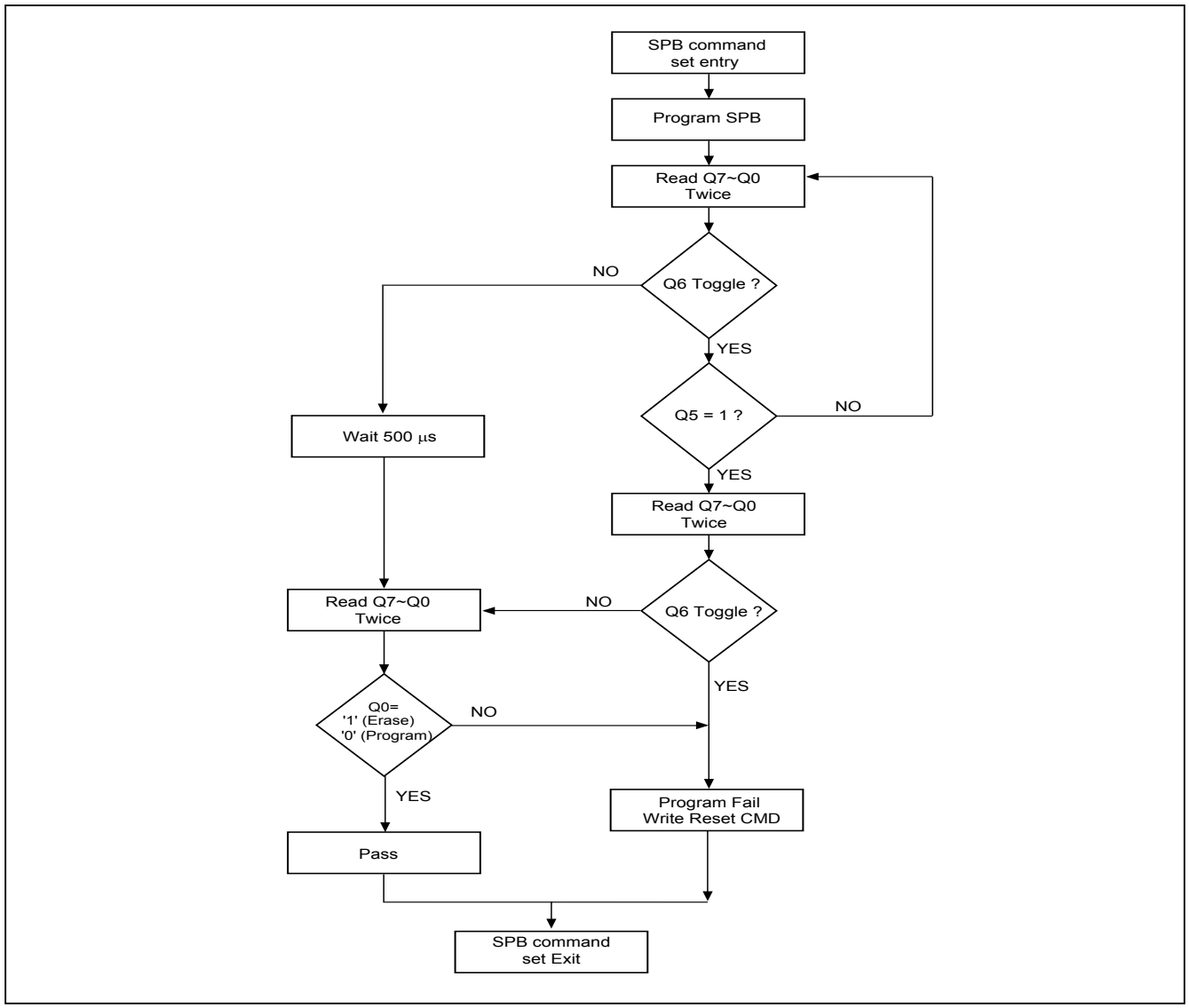
### Temporary Un-protect Solid write Protect Bits (USPB)

Temporary Un-protect Solid write Protect Bits are volatile. They are unique for each sector and can be individually modified. Software can temporarily unprotect write protect sectors despite of SPB's property when DPBs are cleared. While the USPB is set (to "0"), the corresponding sector's SPB property is masked.

**Notes:**
1. Upon power up, the USPBs are cleared (all "1"). The USPBs can be set (to "0") or cleared (to "1") as often as needed. The hardware reset will reset USPB/DPB to their default values.

2. To change the protected sector status of solid write protect bit, users don't need to clear all SPBs. The users can just implement software to set corresponding USPB to "0", in which the corresponding DPB status is cleared too. Consequently, the original solid write protect status of protected sectors can be temporarily changed.

**Figure 13. SPB PROGRAM ALGORITHM**




**Note:** SPB program/erase status polling flowchart: check Q6 toggle, when Q6 stop toggle, the read status is 00H /01H (00H for program/ 01H for erase), otherwise, the status is "fail" and "exit".


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### 9-17-3. Solid Protection Bit Lock Bit

The Solid Protection Bit Lock Bit (SPBLK) is assigned to control all SPB status. It is an unique and volatile. When SPBLK=0 (set), all SPBs are locked and can not be changed. When SPBLK=1 (cleared), all SPBs are allowed to be changed.

There is no software command sequence requested to unlock this bit, unless the device is in the password protection mode. To clear the SPB Lock Bit, just execute a hardware reset or a power-up cycle. In order to prevent modification, the SPB Lock Bit must be set (SPBLK=0) after all SPBs are set to desired status.

### 9-17-4. Password Protection Method

The security level of Password Protection Method is higher than the Solid protection mode. The 64 bit password is requested before modifying SPB lock bit status. When device is under password protection mode, the SPB lock bit is set as "0", after a power-up cycle or Reset Command.

A correct password is required for password Unlock command to unlock the SPB lock bit. Await 100us is necessary to unlock the device after a valid password is given. After that, the SPB bits are allowed to be changed. The Password Unlock command is issued slower than 100 μs every time, to prevent hacker from trying all the 64-bit password combinations.

There are a few steps to start password protection mode:
(1). Set a 64-bit password for verification before entering the password protection mode. This verification is only allowed in password programming.
(2). Set the Password Protection Mode Lock Bit to"0" to activate the password protection mode.

Once the password protection mode lock bit is programmed, the programmed Q2 bit can not be erased any more and the device will remain permanently in password protection mode. The previous set 64-bit password can not be retrieved or programmed. All the commands to the password-protected address will also be disabled.

All the combinations of the 64-bit password can be used as a password, and programming the password does not require special address. The password is defaulted to be all "1" when shipped from the factory. Under password program command, only "0" can be programmed. In order to prevent access, the Password Mode Locking Bit must be set after the Password is programmed and verified. To set the Password Mode Lock Bit will prevent this 64-bits password to be read on the data bus. Any modification is impossible then, and the password can not be checked anymore after the Password Mode Lock Bit is set.


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**Table 8. SECTOR PROTECTION STATUS TABLE**

| Protection Bit Status | | | Sector Status |
|---|---|---|---|
| DPB | SPB | USPB | |
| clear (1) | clear (1) | clear (1) | Unprotected |
| clear (1) | clear (1) | set (0) | Unprotected |
| clear (1) | set (0) | clear (1) | Protected |
| clear (1) | set (0) | set (0) | Unprotected |
| set (0) | clear (1) | clear (1) | Protected |
| set (0) | clear (1) | set (0) | Protected |
| set (0) | set (0) | clear (1) | Protected |
| set (0) | set (0) | set (0) | Protected |

**Notes:** If SPBLK is set, SPB will be unchangeable.
If SPBLK is cleared, SPB will be changeable.


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## 9-18. SECURITY SECTOR FLASH MEMORY REGION

The Security Sector region is an extra OTP memory space of 512 word in length. The security sector can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Status and/or Security Sector Protect Verify to query the lock status of the device.

The device will have a 512 word (1024 byte) in the security region 00000h to 003FEh in byte mode or 00000h to 001FFh in word mode.

## 9-19. FACTORY LOCKED: CAN BE PROGRAMMED AND PROTECTED AT THE FACTORY

IIn factory locked area, security sector region is protected when shipped from factory and permanently locked The Lock Register "Security Sector Factory Lock bit" DQ0 is set to "0".

| Security Sector Address Range | OTP Area Definition | OTP Length |
|---|---|---|
| 000000h-0000FFh | Factory Locked Area | 256 word |
| 000100h-0001FFh | Customer Locked Area | 256 word |

## 9-20. CUSTOMER LOCKED: NOT PROGRAMMED AND NOT PROTECTED AT FACTORY

In customer Locked area, security sector region is unprotected when shipped from factory. The Lock Register "Security Sector Customer Lock bit" DQ6 is set to "1" by default. Note that once the security sector is protected, there is no way to unprotect the security sector and the content of it can no longer be altered.

After the security sector is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.


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# 10. COMMAND REFERENCE SUMMARY

## 10-1. COMMAND DEFINITIONS

### Table 9. COMMAND DEFINITIONS

| Command | | Read Mode | Reset Mode | Enter Automatic Select Mode | | Enter CFI Mode | | Security Sector Region | | Exit Security Sector | | Read Extended Status Register | | Clear Extended Status Register | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | Addr | xxx | 555 | AAA | (SA) 55 | (SA) AA | 555 | AAA | 555 | AAA | 555 | AAA | 555 | AAA |
| | Data | Data | F0 | AA | AA | 98 | 98 | AA | AA | AA | AA | 70 | 70 | 71 | 71 |
| 2nd Bus Cycle | Addr | | | 2AA | 555 | | | 2AA | 555 | 2AA | 555 | xxx | xxx | | |
| | Data | | | 55 | 55 | | | 55 | 55 | 55 | 55 | Data | Data | | |
| 3rd Bus Cycle | Addr | | | (SA) 555 | (SA) AAA | | | (SA) 555 | (SA) AAA | 555 | AAA | | | | |
| | Data | | | 90 | 90 | | | 88 | 88 | 90 | 90 | | | | |
| 4th Bus Cycle | Addr | | | | | | | | | XXX | XXX | | | | |
| | Data | | | | | | | | | 00 | 00 | | | | |
| 5th Bus Cycle | Addr | | | | | | | | | | | | | | |
| | Data | | | | | | | | | | | | | | |
| 6th Bus Cycle | Addr | | | | | | | | | | | | | | |
| | Data | | | | | | | | | | | | | | |

| Command | | Program | | Write to Buffer Program | | Write to Buffer Program Abort Reset | | Write to Buffer Program confirm | |
|---|---|---|---|---|---|---|---|---|---|
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | 555 | AAA | 555 | AAA | 555 | AAA | SA | SA |
| | Data | AA | AA | AA | AA | AA | AA | 29 | 29 |
| 2nd Bus Cycle | Addr | 2AA | 555 | 2AA | 555 | 2AA | 555 | | |
| | Data | 55 | 55 | 55 | 55 | 55 | 55 | | |
| 3rd Bus Cycle | Addr | 555 | AAA | SA | SA | 555 | AAA | | |
| | Data | A0 | A0 | 25 | 25 | F0 | F0 | | |
| 4th Bus Cycle | Addr | Addr | Addr | SA | SA | | | | |
| | Data | Data | Data | N-1 | N-1 | | | | |
| 5th Bus Cycle | Addr | | | WA | WA | | | | |
| | Data | | | WD | WD | | | | |
| 6th Bus Cycle | Addr | | | WBL | WBL | | | | |
| | Data | | | WD | WD | | | | |

WA= Write Address
WD= Write Data
SA= Sector Address
N-1= Word Count
WBL= Write Buffer Location
PWD= Password
PWDn=Password word 0, word 1, word n
ID1/ID2/ID3: Refer to *"Table 7. AUTOMATIC SELECT HIGH VOLTAGE OPERATION"* for detailed ID.


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| Command | | Blank Check | | Chip Erase | | Sector Erase | | Program/ Erase Suspend | | Program/ Erase Resume | | Program Suspend Specific Method | | Program Resume Specific Method | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | (SA) 555 | (SA) AAA | 555 | AAA | 555 | AAA | xxx | xxx | xxx | xxx | xxx | xxx | xxx | xxx |
| | Data | 33 | 33 | AA | AA | AA | AA | B0 | B0 | 30 | 30 | 51 | 51 | 50 | 50 |
| 2nd Bus Cycle | Addr | | | 2AA | 555 | 2AA | 555 | | | | | | | | |
| | Data | | | 55 | 55 | 55 | 55 | | | | | | | | |
| 3rd Bus Cycle | Addr | | | 555 | AAA | 555 | AAA | | | | | | | | |
| | Data | | | 80 | 80 | 80 | 80 | | | | | | | | |
| 4th Bus Cycle | Addr | | | 555 | AAA | 555 | AAA | | | | | | | | |
| | Data | | | AA | AA | AA | AA | | | | | | | | |
| 5th Bus Cycle | Addr | | | 2AA | 555 | 2AA | 555 | | | | | | | | |
| | Data | | | 55 | 55 | 55 | 55 | | | | | | | | |
| 6th Bus Cycle | Addr | | | 555 | AAA | Sector | Sector | | | | | | | | |
| | Data | | | 10 | 10 | 30 | 30 | | | | | | | | |

| Command | | Deep Power Down | | | | Password Protection | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Enter | | Exit | | Password Command Set Entry | | Password Program | | Password Read | | Password Unlock | | Password Command Set Exit | |
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | 555 | AAA | XXX | XXX | 555 | AAA | XXX | XXX | 00 | 00 | 00 | 00 | XXX | XXX |
| | Data | AA | AA | AB | AB | AA | AA | A0 | A0 | PWD0 | PWD0 | 25 | 25 | 90 | 90 |
| 2nd Bus Cycle | Addr | 2AA | 555 | | | 2AA | 555 | PWA | PWA | 01 | 01 | 00 | 00 | XXX | XXX |
| | Data | 55 | 55 | | | 55 | 55 | PWD | PWD | PWD1 | PWD1 | 03 | 03 | 00 | 00 |
| 3rd Bus Cycle | Addr | XXX | XXX | | | 555 | AAA | | | 02 | 02 | 00 | 00 | | |
| | Data | B9 | B9 | | | 60 | 60 | | | PWD2 | PWD2 | PWD0 | PWD0 | | |
| 4th Bus Cycle | Addr | | | | | | | | | 03 | 03 | 01 | 01 | | |
| | Data | | | | | | | | | PWD3 | PWD3 | PWD1 | PWD1 | | |
| 5th Bus Cycle | Addr | | | | | | | | | | 04 | 02 | 02 | | |
| | Data | | | | | | | | | | PWD4 | PWD2 | PWD2 | | |
| 6th Bus Cycle | Addr | | | | | | | | | | 05 | 03 | 03 | | |
| | Data | | | | | | | | | | PWD5 | PWD3 | PWD3 | | |
| 7th Bus Cycle | Addr | | | | | | | | | | 06 | 00 | 04 | | |
| | Data | | | | | | | | | | PWD6 | 29 | PWD4 | | |
| 8th Bus Cycle | Addr | | | | | | | | | | 07 | | 05 | | |
| | Data | | | | | | | | | | PWD7 | | PWD5 | | |
| 9th Bus Cycle | Addr | | | | | | | | | | | | 06 | | |
| | Data | | | | | | | | | | | | PWD6 | | |
| 10th Bus Cycle | Addr | | | | | | | | | | | | 07 | | |
| | Data | | | | | | | | | | | | PWD7 | | |
| 11th Bus Cycle | Addr | | | | | | | | | | | | 00 | | |
| | Data | | | | | | | | | | | | 29 | | |


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| Command | | Lock Register | | | | | | | | Global Non-Volatile | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Lock register Command Set Entry | | Program | | Read | | Lock register Command Set Exit | | SPB Command Set Entry | | SPB Program | | All SPB Erase | | SPB Status Read | |
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | 555 | AAA | XXX | XXX | XXX | XXX | XXX | XXX | 555 | AAA | XXX | XXX | XXX | XXX | SA | SA |
| | Data | AA | AA | A0 | A0 | DATA | DATA | 90 | 90 | AA | AA | A0 | A0 | 80 | 80 | 00/01 | 00/01 |
| 2nd Bus Cycle | Addr | 2AA | 555 | XXX | XXX | | | XXX | XXX | 2AA | 555 | SA | SA | 00 | 00 | | |
| | Data | 55 | 55 | Data | Data | | | 00 | 00 | 55 | 55 | 00 | 00 | 30 | 30 | | |
| 3rd Bus Cycle | Addr | 555 | AAA | | | | | | | 555 | AAA | | | | | | |
| | Data | 40 | 40 | | | | | | | C0 | C0 | | | | | | |
| 4th Bus Cycle | Addr | | | | | | | | | | | | | | | | |
| | Data | | | | | | | | | | | | | | | | |
| 5th Bus Cycle | Addr | | | | | | | | | | | | | | | | |
| | Data | | | | | | | | | | | | | | | | |

| Command | | Global Non-Volatile | | Global Volatile Freeze | | | | | | | | Volatile | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SPB Command Set Exit | | SPB Lock Command Set Entry | | SPB Lock Set | | SPB Lock Status Read | | SPB Lock Command Set Exit | | DPB Command Set Entry | | DPB Set | | DPB Clear | |
| | | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | XXX | XXX | 555 | AAA | XXX | XXX | XXX | XXX | XXX | XXX | 555 | AAA | XXX | XXX | XXX | XXX |
| | Data | 90 | 90 | AA | AA | A0 | A0 | 00/01 | 00/01 | 90 | 90 | AA | AA | A0 | A0 | A0 | A0 |
| 2nd Bus Cycle | Addr | XXX | XXX | 2AA | 555 | XXX | XXX | | | XXX | XXX | 2AA | 555 | SA | SA | SA | SA |
| | Data | 00 | 00 | 55 | 55 | 00 | 00 | | | 00 | 00 | 55 | 55 | 00 | 00 | 01 | 01 |
| 3rd Bus Cycle | Addr | | | 555 | AAA | | | | | | | 555 | AAA | | | | |
| | Data | | | 50 | 50 | | | | | | | E0 | E0 | | | | |
| 4th Bus Cycle | Addr | | | | | | | | | | | | | | | | |
| | Data | | | | | | | | | | | | | | | | |
| 5th Bus Cycle | Addr | | | | | | | | | | | | | | | | |
| | Data | | | | | | | | | | | | | | | | |

| Command | | Volatile | | | |
|---|---|---|---|---|---|
| | | DPB Status Read | | DPB Command Set Exit | |
| | | Word | Byte | Word | Byte |
| 1st Bus Cycle | Addr | SA | SA | XXX | XXX |
| | Data | 00/01 | 00/01 | 90 | 90 |
| 2nd Bus Cycle | Addr | | | XXX | XXX |
| | Data | | | 00 | 00 |
| 3rd Bus Cycle | Addr | | | | |
| | Data | | | | |
| 4th Bus Cycle | Addr | | | | |
| | Data | | | | |
| 5th Bus Cycle | Addr | | | | |
| | Data | | | | |

**Notes:**

* It is not recommended to adopt any other code not in the command definition table which will potentially enter the hidden mode.
* For the SPB Lock and DPB Status Read "00" means lock (protect), "01" means unlock (unprotect).

## 10-2. COMMON FLASH MEMORY INTERFACE (CFI) MODE

The host system can read CFI information at the addresses given in the following *Table 10*~*Table 13*, the query data is always presented on the lowest order data outputs.

**Table 10. CFI MODE: IDENTIFICATION DATA VALUES**

(All values in these tables are in hexadecimal)

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) |
|---|---|---|---|
| Query-unique ASCII string "QRY" | 10 | 20 | 0051 |
| | 11 | 22 | 0052 |
| | 12 | 24 | 0059 |
| Primary vendor command set and control interface ID code | 13 | 26 | 0002 |
| | 14 | 28 | 0000 |
| Address for primary algorithm extended query table | 15 | 2A | 0040 |
| | 16 | 2C | 0000 |
| Alternate vendor command set and control interface ID code | 17 | 2E | 0000 |
| | 18 | 30 | 0000 |
| Address for alternate algorithm extended query table | 19 | 32 | 0000 |
| | 1A | 34 | 0000 |

**Table 11. CFI MODE: SYSTEM INTERFACE DATA VALUES**

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) | |
|---|---|---|---|---|
| Vcc supply minimum program/erase voltage | 1B | 36 | 0027 | |
| Vcc supply maximum program/erase voltage | 1C | 38 | 0036 | |
| VPP supply minimum program/erase voltage | 1D | 3A | 0000 | |
| VPP supply maximum program/erase voltage | 1E | 3C | 0000 | |
| Typical timeout per single word/byte write, $2^n$ us | 1F | 3E | 0005 | |
| Typical timeout for maximum-size buffer write, $2^n$ us (00h, not support) | 20 | 40 | 0009 | |
| Typical timeout per individual block erase, $2^n$ ms | 21 | 42 | 0008 | |
| Typical timeout for full chip erase, $2^n$ ms (00h, not support) | 22 | 44 | 512Mb | 0011 |
| | | | 1Gb | 0012 |
| Maximum timeout for word/byte write, $2^n$ times typical | 23 | 46 | 0003 | |
| Maximum timeout for buffer write, $2^n$ times typical | 24 | 48 | 0002 | |
| Maximum timeout per individual block erase, $2^n$ times typical | 25 | 4A | 0003 | |
| Maximum timeout for chip erase, $2^n$ times typical (00h, not support) | 26 | 4C | 0001 | |


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**Table 12. CFI MODE: DEVICE GEOMETRY DATA VALUES**

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) | |
|---|---|---|---|---|
| Device size = $2^n$ in number of bytes | 27 | 4E | 512Mb | 001A |
| | | | 1Gb | 001B |
| Flash Device Interface Description 0 = x8-only, 1 = x16-only, 2 = x8/x16 capable | 28 | 50 | 0002 | |
| | 29 | 52 | 0000 | |
| Maximum number of bytes in buffer write = $2^n$ (00h, not support) | 2A | 54 | 0009 | |
| | 2B | 56 | 0000 | |
| Number of erase regions within device (01h:uniform, 02h:boot) | 2C | 58 | 0001 | |
| Index for Erase Bank Area 1:<br>[2E,2D] = # of same-size sectors in region 1-1<br>[30, 2F] = sector size in multiples of 256-bytes | 2D | 5A | 00FF | |
| | 2E | 5C | 512Mb | 0001 |
| | | | 1Gb | 0003 |
| | 2F | 5E | 0000 | |
| | 30 | 60 | 0002 | |
| Index for Erase Bank Area 2 | 31 | 62 | 0000 | |
| | 32 | 64 | 0000 | |
| | 33 | 66 | 0000 | |
| | 34 | 68 | 0000 | |
| Index for Erase Bank Area 3 | 35 | 6A | 0000 | |
| | 36 | 6C | 0000 | |
| | 37 | 6E | 0000 | |
| | 38 | 70 | 0000 | |
| Index for Erase Bank Area 4 | 39 | 72 | 0000 | |
| | 3A | 74 | 0000 | |
| | 3B | 76 | 0000 | |
| | 3C | 78 | 0000 | |
| Reserved | 3D | 7A | FFFF | |
| | 3E | 7C | FFFF | |
| | 3F | 7E | FFFF | |


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**Table 13. CFI MODE: PRIMARY VENDOR-SPECIFIC EXTENDED QUERY DATA VALUES**

| Description | Address (h) (Word Mode) | Address (h) (Byte Mode) | Data (h) |
|---|---|---|---|
| Query - Primary extended table, unique ASCII string, PRI | 40 | 80 | 0050 |
| | 41 | 82 | 0052 |
| | 42 | 84 | 0049 |
| Major version number, ASCII | 43 | 86 | 0031 |
| Minor version number, ASCII | 44 | 88 | 0035 |
| Address sensitive unlock (bits 1 to 0)<br>00 = supported, 01 = not supported<br>Process Technology (bits 7 to 2) | 45 | 8A | 001C |
| Erase suspend (2= to both read and program) | 46 | 8C | 0002 |
| Sector protect (N= # of sectors/group) | 47 | 8E | 0001 |
| Temporary sector unprotect (1=supported) | 48 | 90 | 0001 |
| Sector protect/Chip unprotect scheme | 49 | 92 | 0008 |
| Simultaneous R/W operation (0=not supported) | 4A | 94 | 0000 |
| Burst mode (0=not supported) | 4B | 96 | 0000 |
| Page mode (0=not supported, 01 = 4 word page, 02 = 8 word page, 03=16 word page) | 4C | 98 | 0003 |
| Minimum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV | 4D | 9A | 0095 |
| Maximum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV | 4E | 9C | 00A5 |
| WP# Protection<br>04=Uniform sectors bottom WP# protect<br>05=Uniform sectors top WP# protect | 4F | 9E | 0004/<br>0005 |
| Program Suspend (0=not supported, 1=supported) | 50 | A0 | 0001 |
| Unlock Bypass 00 = Not Supported 01 = Supported | 51 | A2 | 0000 |
| Security Sector (Customer OTP Area) Size $2^N$ (bytes) | 52 | A4 | 0009 |
| Software Features<br>bit 0: extended status register<br>(1 = supported, 0 = not supported)<br>bit 1: DQ polling (1 = supported, 0 = not supported)<br>bit 2: new program suspend/resume commands<br>(1 = supported, 0 = not supported)<br>bit 3: word program (1 = supported, 0 = not supported)<br>bit 4: bit-field program (1 = supported, 0 = not supported) bit 5: autodetect program<br>(1 = supported, 0 = not supported)<br>bit 6: RFU<br>bit 7: multiple writes per Line (1 = supported, 0 = not supported) | 53 | A6 | 008F |
| Page Size = $2^N$ bytes | 54 | A8 | 0005 |
| Erase Suspend Timeout Maximum < $2^N$ (us) | 55 | AA | 0005 |
| Program Suspend Timeout Maximum < $2^N$ (us) | 56 | AC | 0005 |
| Reserved | 57-77 | AE-EE | FFFF |
| Embedded Hardware Reset Timeout Maximum < $2^N$ (us) Reset with Reset Pin | 78 | F0 | 0005 |
| Non-Embedded Hardware Reset Timeout Maximum < $2^N$ (us) Power on Reset | 79 | F2 | 0009 |

Note: Query data are always presented on the lowest-order data outputs only.


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# 11. ELECTRICAL CHARACTERISTICS

## 11-1. ABSOLUTE MAXIMUM STRESS RATINGS

| | | |
|---|---|---|
| Surrounding Temperature with Bias | | -65°C to +125°C |
| Storage Temperature | | -65°C to +150°C |
| Voltage Range | VCC | -0.5V to +4.0 V |
| | VI/O | -0.5V to +4.0 V |
| | A9 , WP#/ACC | -0.5V to +10.5 V |
| | The other pins. | -0.5V to Vcc +0.5V |
| Output Short Circuit Current (less than one second) | | 200 mA |

## 11-2. OPERATING TEMPERATURE AND VOLTAGE

| | | |
|---|---|---|
| **Industrial (I) Grade** | Surrounding Temperature ($T_A$) | -40°C to +85°C |
| **VCC Supply Voltages** | Full VCC range | +2.7 V to 3.6 V |
| | Regulated VCC range | +3.0 V to 3.6 V |
| | VI/O range | 1.65V to VCC |

**NOTICE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot GND to -2.0V and Vcc to +2.0V for periods up to 20ns, see below Figure.

**Figure 14. MAXIMUM NEGATIVE OVERSHOOT WAVEFORM**

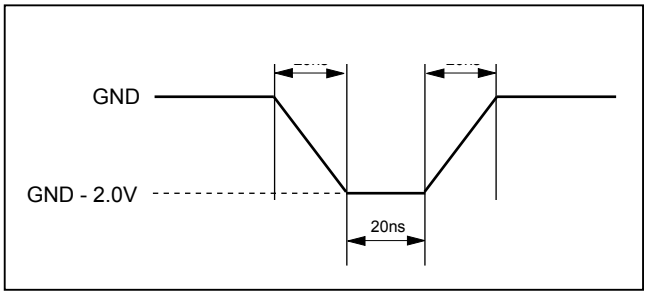
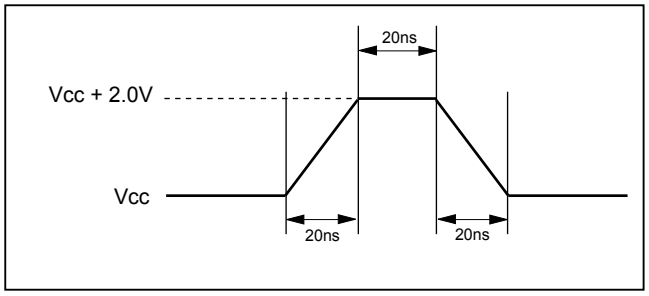



**Figure 15. MAXIMUM POSITIVE OVERSHOOT WAVEFORM**

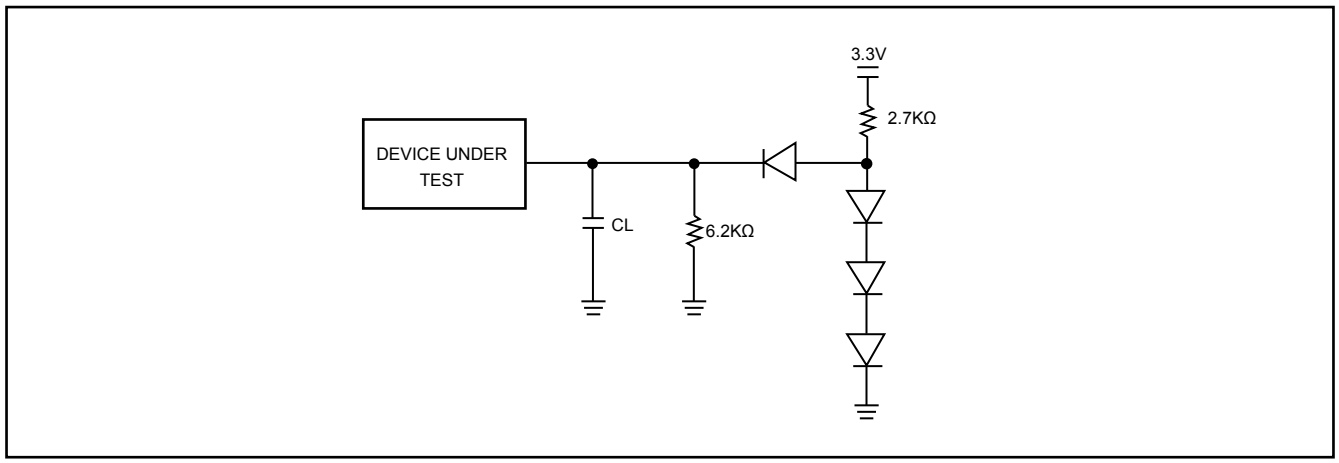




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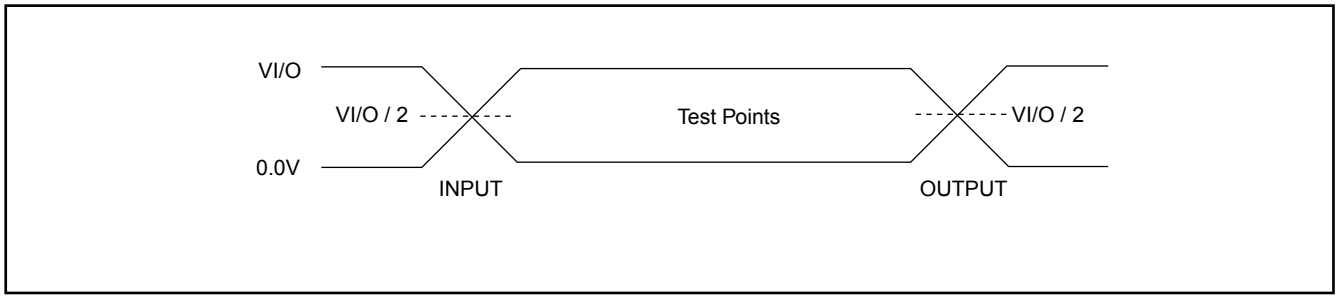
## 11-3. TEST CONDITIONS

**Figure 16. SWITCHING TEST CIRCUITS**




**Test Condition**
Output Load Capacitance, CL : 1TTL gate, 30pF
Rise/Fall Times : 5ns
Input Pulse levels :0.0 ~ VI/O
In/Out reference levels :0.5VI/O

**Figure 17. SWITCHING TEST WAVEFORMS**





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## 11-4. DC CHARACTERISTICS

### Table 14. DC CHARACTERISTICS

| Symbol | Description | | | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| Iilk | Input Leak | | | | | ±2.0 | uA | |
| Iilkw | WP#/ACC Leak | | 512Mb | | | ±4.0 | uA | |
| | | | 1Gb | | | ±8.0 | uA | |
| Iilk9 | A9 Leak | | 512Mb | | | 20 | uA | A9=10.5V |
| | | | 1Gb | | | 40 | uA | |
| Iolk | Output Leak | | | | | ±1.0 | uA | |
| Icr1 | Read Current | 1MHz | 512Mb | | 5 | 10 | mA | CE#=Vil, OE#=Vih, VCC=VCCmax; f=1MHz |
| | | | 1Gb | | 5 | 15 | mA | |
| | | 5MHz | 512Mb | | 12 | 30 | mA | CE#=Vil, OE#=Vih, VCC=VCCmax; f=5MHz |
| | | | 1Gb | | 12 | 35 | mA | |
| | | 10MHz | 512Mb | | 20 | 35 | mA | CE#=Vil, OE#=Vih, VCC=VCCmax; f=10MHz |
| | | | 1Gb | | 20 | 40 | mA | |
| Icr2 | VCC Page Read Current | 10MHz | 512Mb | | 4 | 8 | mA | CE#=Vil, OE#=Vih, VCC=VCCmax; f=10MHz |
| | | | 1Gb | | 8 | 15 | mA | |
| | | 33MHz | 512Mb | | 6 | 12 | mA | CE#=Vil, OE#=Vih, VCC=VCCmax; f=33MHz |
| | | | 1Gb | | 12 | 24 | mA | |
| Iio | VI/O non-active current | | 512Mb | | 0.2 | 10 | mA | |
| | | | 1Gb | | 0.4 | 20 | mA | |
| Icw | Write Current | | 512Mb | | 35 | 55 | mA | CE#=Vil, OE#=Vih, WE#=Vil |
| | | | 1Gb | | 35 | 55 | mA | |
| Isb | Standby Current | | 512Mb | | 20 | 90 | uA | VCC=VCCmax, CE#=OE#=RESET#=VIO |
| | | | 1Gb | | 40 | 180 | uA | |
| Isbr | Reset Current | | 512Mb | | 20 | 90 | uA | VCC=VCCmax, RESET#=GND, CE#=Vih |
| | | | 1Gb | | 40 | 180 | uA | |
| Isbs | Sleep Mode Current | | 512Mb | | 20 | 90 | uA | VCC=VCCmax, Vil=GND, Vih=VI/O |
| | | | 1Gb | | 40 | 180 | uA | |
| Idpd | Vcc deep power down current | | 512Mb | | 3 | 15 | uA | VCC=VCCmax, CE#=OE#=RESET#=VIO |
| | | | 1Gb | | 6 | 30 | uA | |


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| Symbol | Description | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Icp1 | Accelerated Pgm Current, WP#/ACC pin (Word/Byte) | | 2 | 5 | mA | CE#=Vil, OE#=Vih |
| Icp2 | Accelerated Pgm Current, VCC pin, (Word/Byte) | | 14 | 28 | mA | CE#=Vil, OE#=Vih |
| Vil | Input Low Voltage | -0.1V | | 0.3xVI/O | V | |
| Vih | Input High Voltage | 0.7xVI/O | | VI/O+0.3V | V | |
| Vhv | Very High Voltage for Auto Select/ Accelerated Program | 9.5 | | 10.5 | V | |
| Vol | Output Low Voltage | | | 0.45 | V | Iol=100uA |
| Voh | Ouput High Voltage | 0.85xVI/O | | | V | Ioh=-100uA |
| Vlko | Low Vcc Lock-out voltage | 2.1 | | 2.4 | V | |

**Note:** Sleep mode enables the lower power when address remain stable for taa+1us.


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## 11-5. AC CHARACTERISTICS

**Table 15. AC CHARACTERISTICS**

| Symbol | Description | | VCC=2.7V to 3.6V | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Taa | Valid data output after address | VI/O=VCC | | | 100 | ns |
| | | VI/O=1.65 to VCC | | | 110 | ns |
| Tpa | Page access time | VI/O=VCC | | | 15 | ns |
| | | VI/O=1.65 to VCC | | | 25 | ns |
| Tce | Valid data output after CE# low | VI/O=VCC | | | 100 | ns |
| | | VI/O=1.65 to VCC | | | 110 | ns |
| Toe | Valid data output after OE# low | VI/O=VCC | | | 25 | ns |
| | | VI/O=1.65 to VCC | | | 30 | ns |
| Tdf | Data output floating after OE# high or CE# high | | | | 20 | ns |
| Tsrw | Latency between read and write operation (Note) | | 35 | | | ns |
| Toh | Output hold time from the earliest rising edge of address, CE#, OE# | | 0 | | | ns |
| Trc | Read period time | | 100 | | | ns |
| Twc | Write period time | | 100 | | | ns |
| Tcwc | Command write period time | | 100 | | | ns |
| Tas | Address setup time | | 0 | | | ns |
| Taso | Address setup time to OE# low during toggle bit polling | | 15 | | | ns |
| Tah | Address hold time | | 45 | | | ns |
| Taht | Address hold time from CE# or OE# high during toggle bit polling | | 0 | | | ns |
| Tds | Data setup time | | 30 | | | ns |
| Tdh | Data hold time | | 0 | | | ns |
| Tvcs | Vcc setup time | | 500 | | | us |
| Tcs | Chip enable Setup time | | 0 | | | ns |
| Tch | Chip enable hold time | | 0 | | | ns |
| Toeh | Output enable hold time | Read | 0 | | | ns |
| | | Toggle & Data# Polling | 10 | | | ns |


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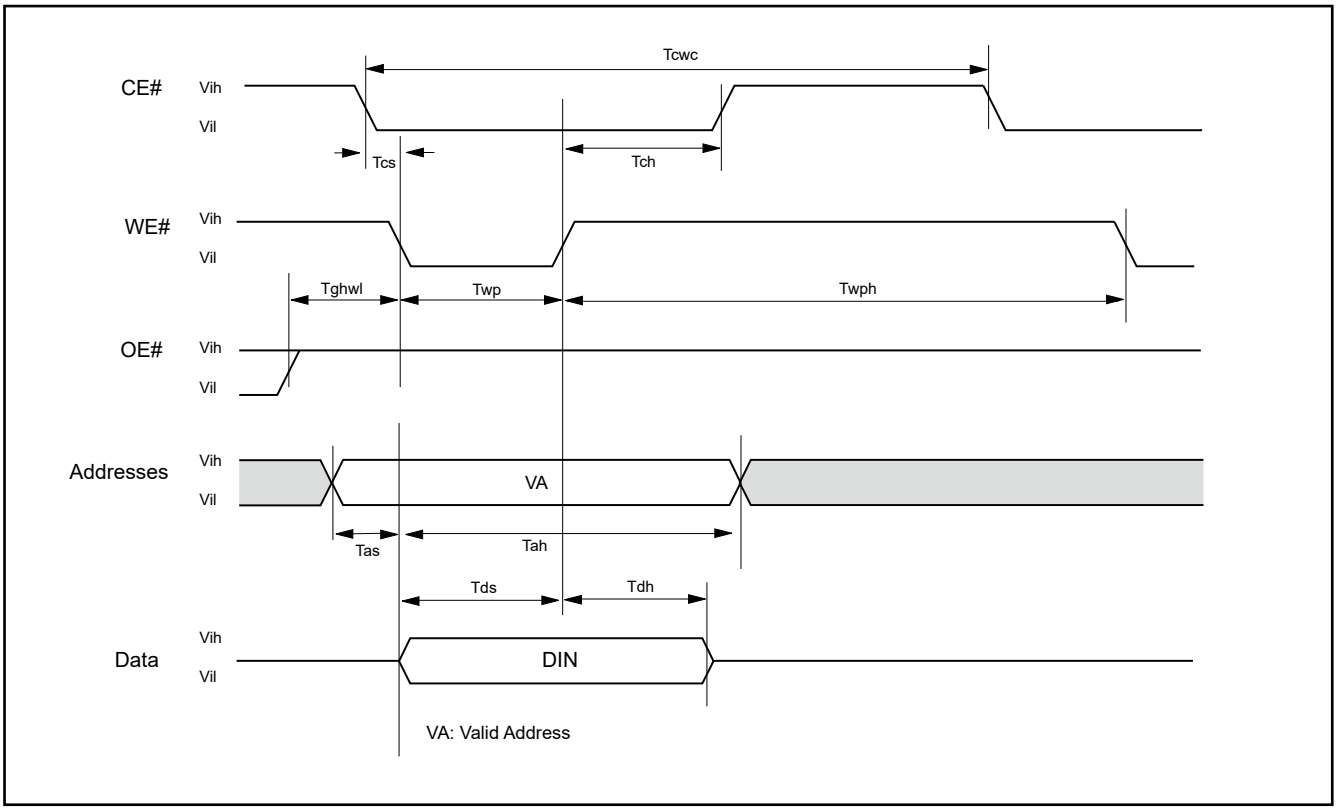
| Symbol | Description | | VCC=2.7V to 3.6V | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Tws | WE# setup time | | 0 | | | ns |
| Twh | WE# hold time | | 0 | | | ns |
| Tcepw | CE# pulse width | | 35 | | | ns |
| Tcepwh | CE# pulse width high | | 30 | | | ns |
| Twp | WE# pulse width | | 35 | | | ns |
| Twph | WE# pulse width high | | 30 | | | ns |
| Tbusy | Program/Erase active time by RY/BY# | VI/O=VCC | | | 100 | ns |
| | | VI/O=1.65 to VCC | | | 110 | ns |
| Tghwl | Read recover time before write (under WE# control) | | 0 | | | ns |
| Tghel | Read recover time before write (under CE# control) | | 0 | | | ns |
| Toeph | Output enable high during toggle bit polling or following extended status register read | | 20 | | | ns |
| Tceph | Chip enable high during toggle bit polling or following extended status register read | | 20 | | | ns |
| Twhwh1 | Program operation | Byte | | 30 | | us |
| | | Word | | 30 | | us |
| Twhwh2 | Sector erase operation | | | 0.25 | 1.4 | sec |

**Note:** Not 100% tested.


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## 11-6. WRITE COMMAND OPERATION

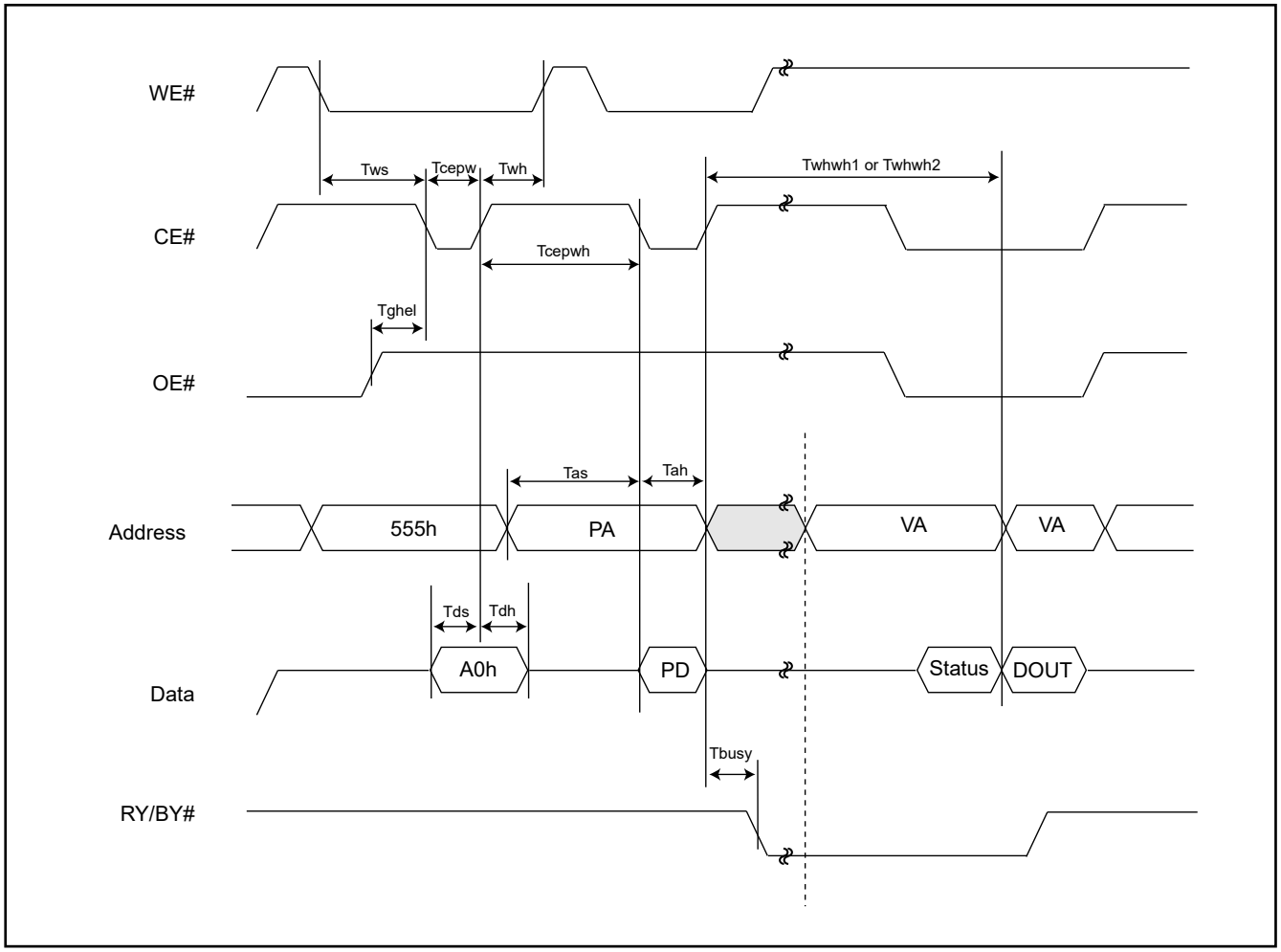
**Figure 18. COMMAND WRITE TIMING WAVEFORM (WE# CONTROLLED)**





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**Figure 19. COMMAND WRITE TIMING WAVEFORM (CE# CONTROLLED)**

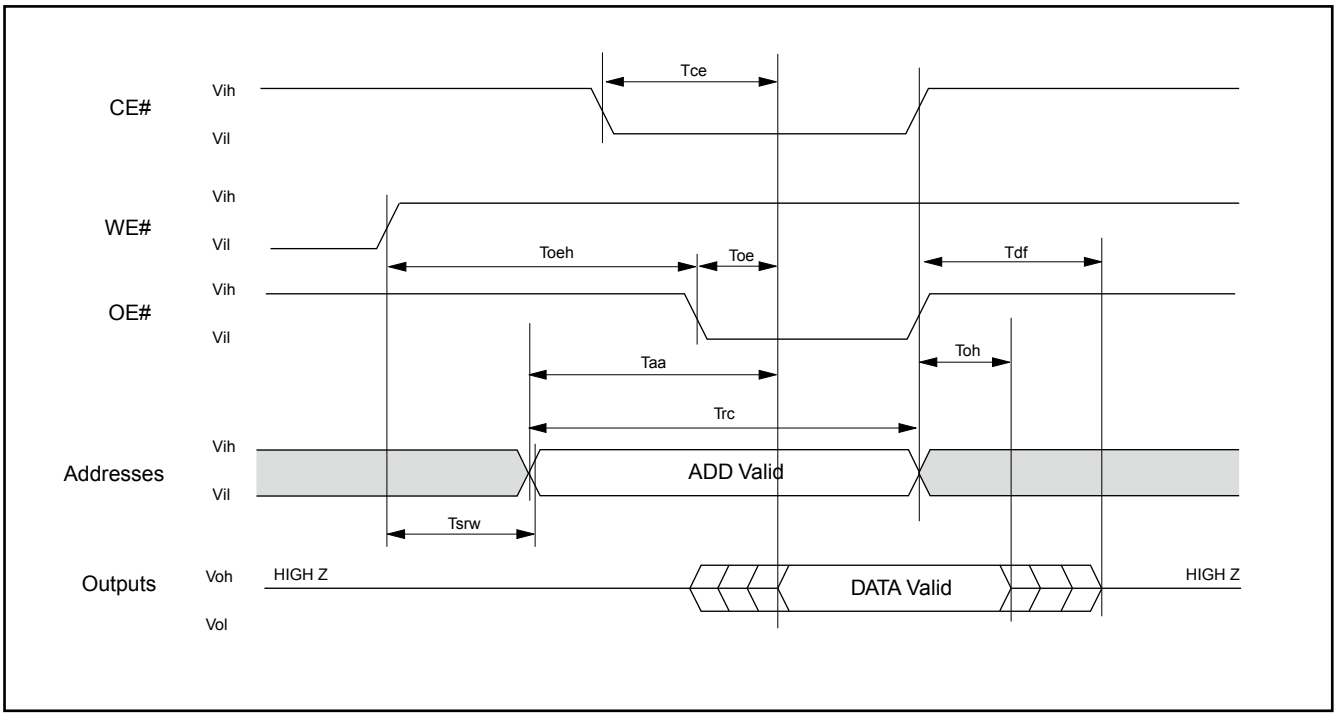




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## 11-7. READ/RESET OPERATION

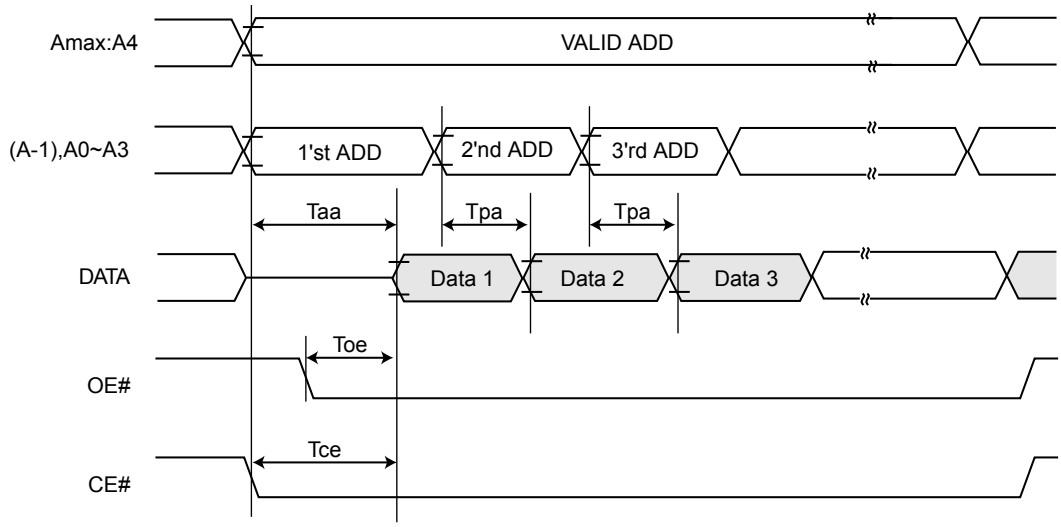
**Figure 20. READ TIMING WAVEFORM**





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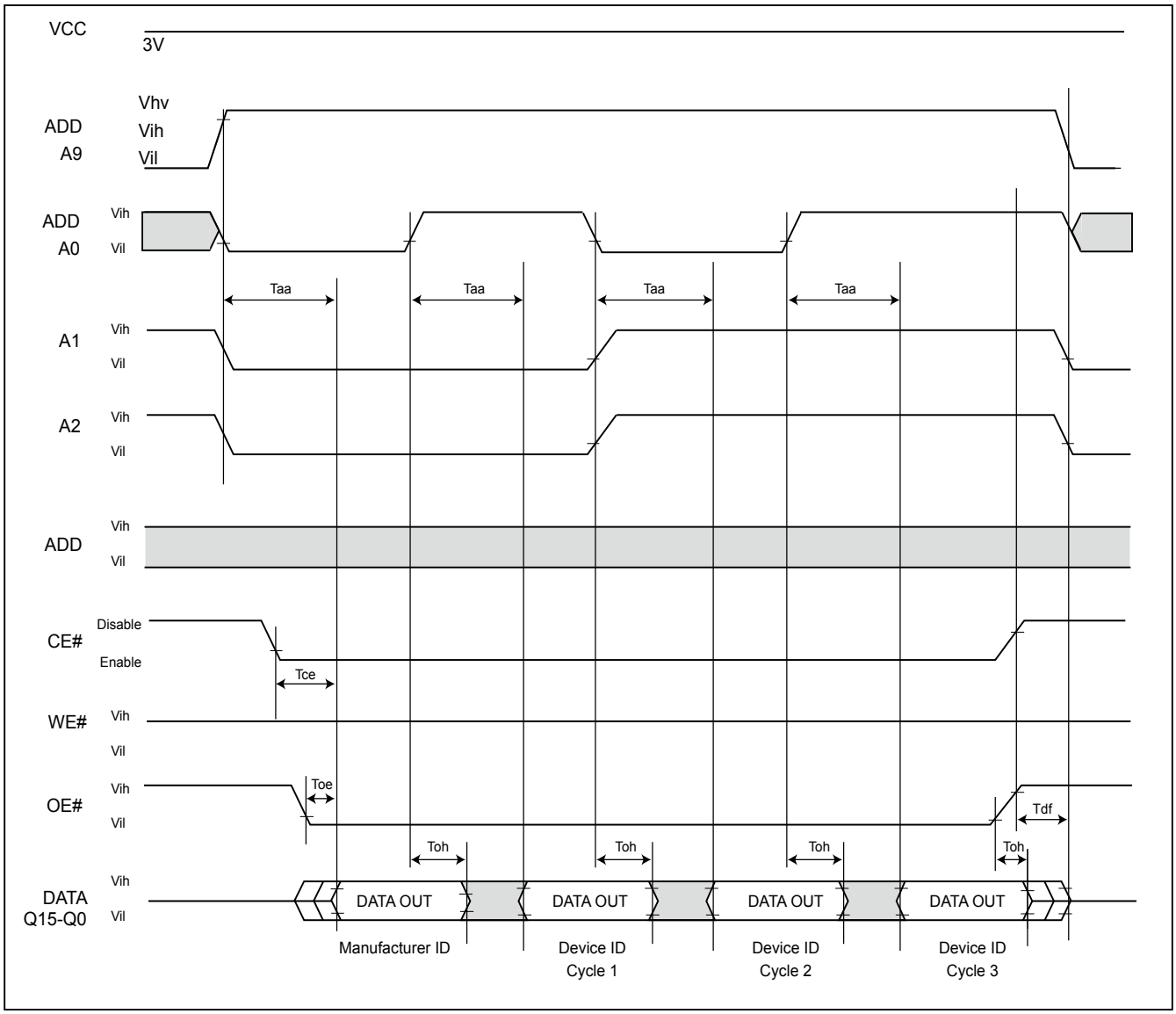
**Figure 21. PAGE READ TIMING WAVEFORM**




Note: CE#, OE# are enable.
Page size is 16 words in Word mode, 32 bytes in Byte mode.
Address are A3~A0 for Word mode, A3~A-1 for Byte mode.


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**Figure 22. READ MANUFACTURER ID OR DEVICE ID**





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**Figure 23. RESET# TIMING WAVEFORM**

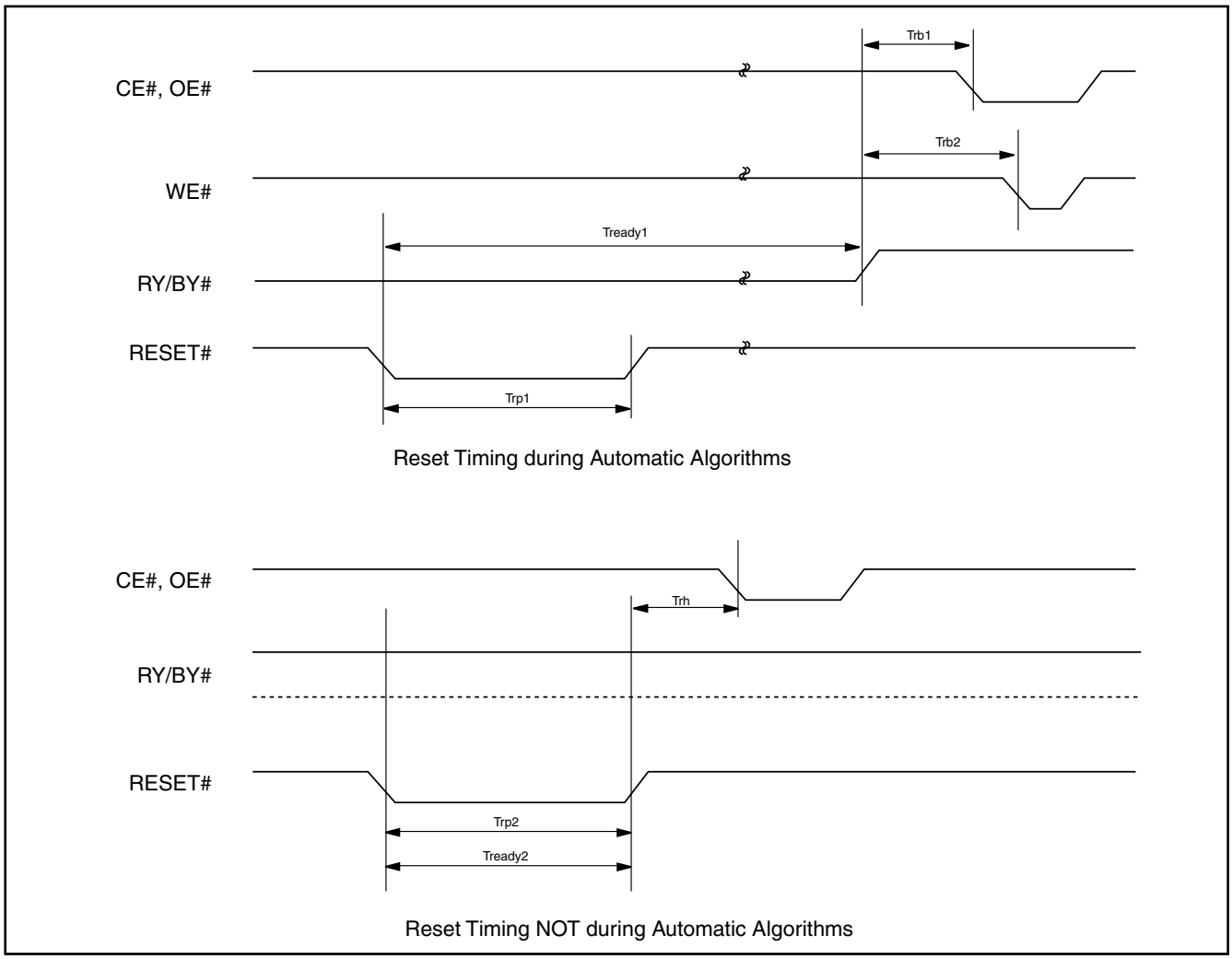



**Table 16. AC CHARACTERISTICS (RESET# TIMING)**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Trp1 | RESET# Pulse Width (During Automatic Algorithms) | 10 | | | us |
| Trp2 | RESET# Pulse Width (NOT During Automatic Algorithms) | 200 | | | ns |
| Trh | RESET# High Time Before Read | 50 | | | ns |
| Trb1 | RY/BY# Recovery Time (to CE#, OE# go low) | 0 | | | ns |
| Trb2 | RY/BY# Recovery Time (to WE# go low) | 50 | | | ns |
| Tready1 | RESET# PIN Low (During Automatic Algorithms) to Read or Write | | | 30 | us |
| Tready2 | RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write | | | 500 | ns |
| Tesl | Erase Suspend/Resume Latency | | | 30 | us |
| Tpsl | Program Suspend/Resume Latency | | | 30 | us |
| Tprs | Latency between program resume and next suspend | | 30 | | us |
| Ters | Latency between erase resume and next suspend | | 400 | | us |


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**Figure 24. DEEP POWER DOWN MODE TIMING WAVEFORM**

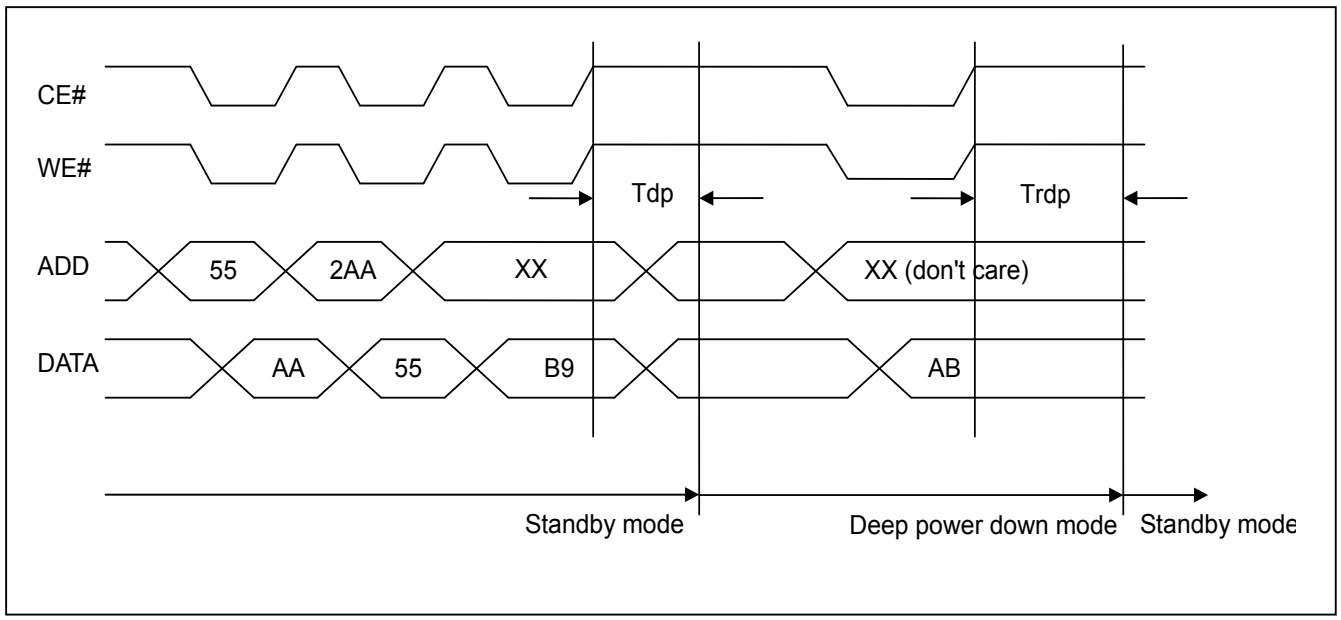



**Table 17. AC CHARACTERISTICS (Deep Power Down Mode TIMING)**

| Symbol | Description | Typ. | Max. | Unit |
|---|---|---|---|---|
| Trdp | WE# high to release from deep power down mode | 100us | 200us | us |
| Tdp | WE# high to deep power down mode | 10us | 20us | us |


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## 11-8. ERASE/PROGRAM OPERATION

**Figure 25. AUTOMATIC CHIP ERASE TIMING WAVEFORM**

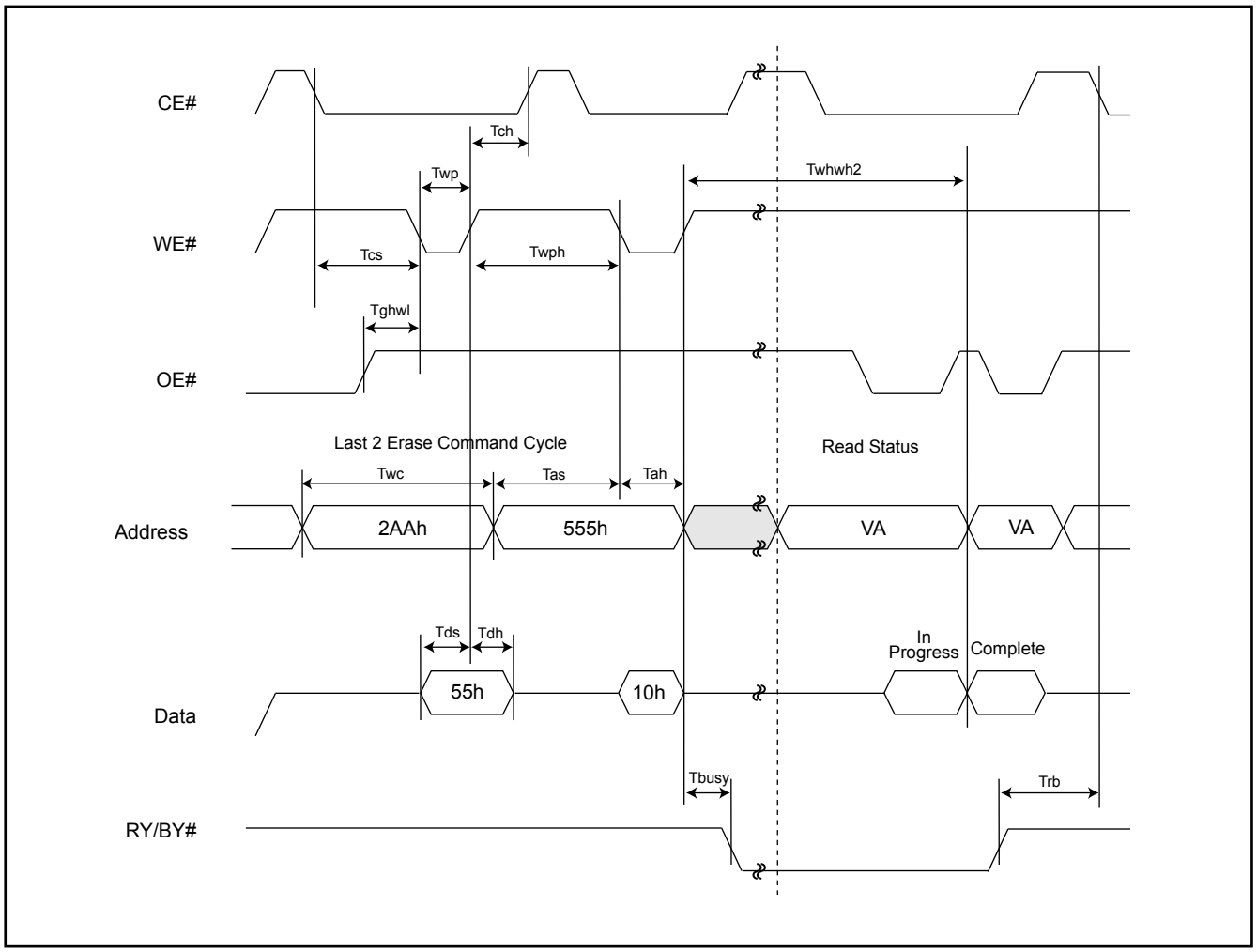
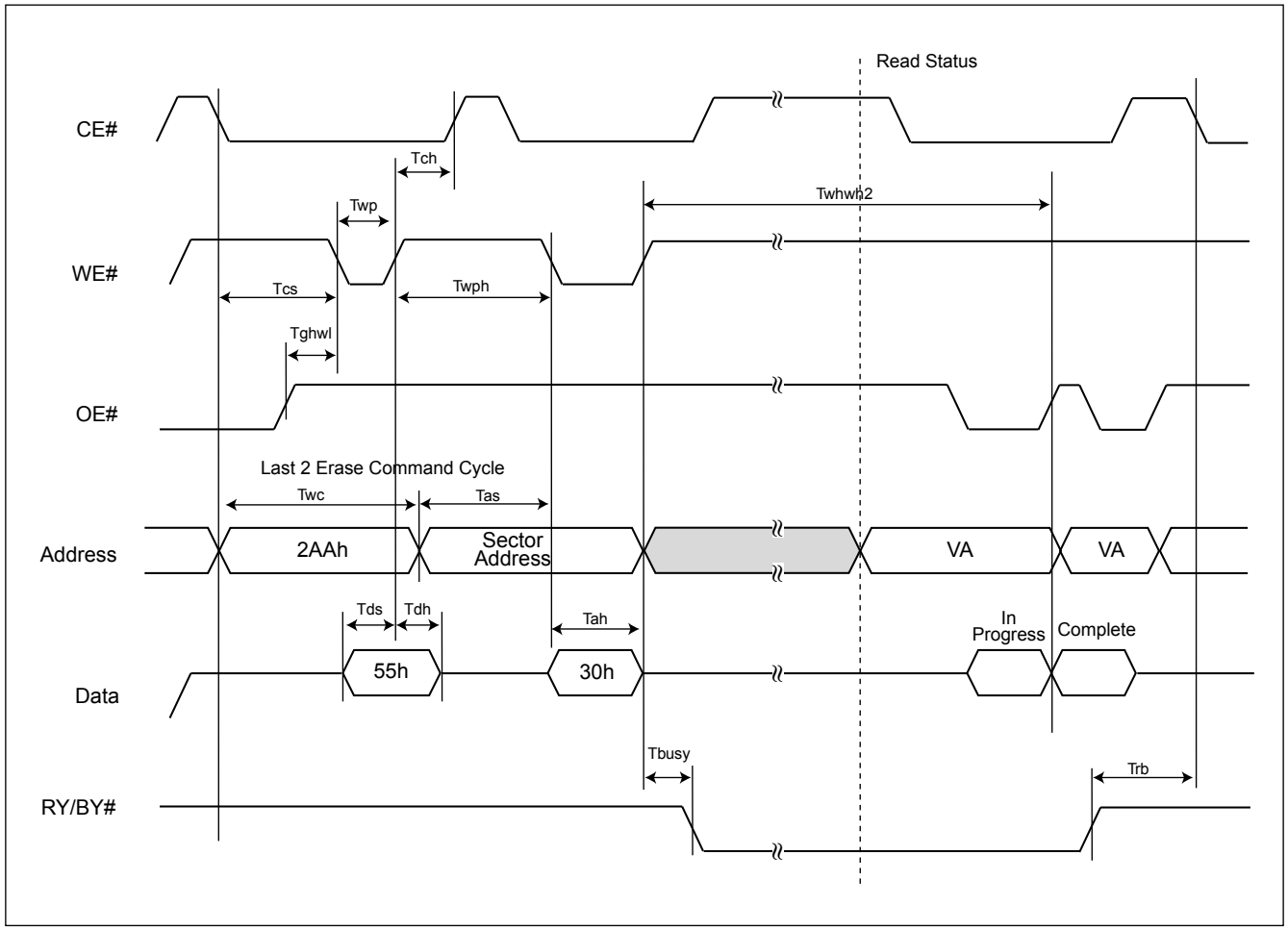


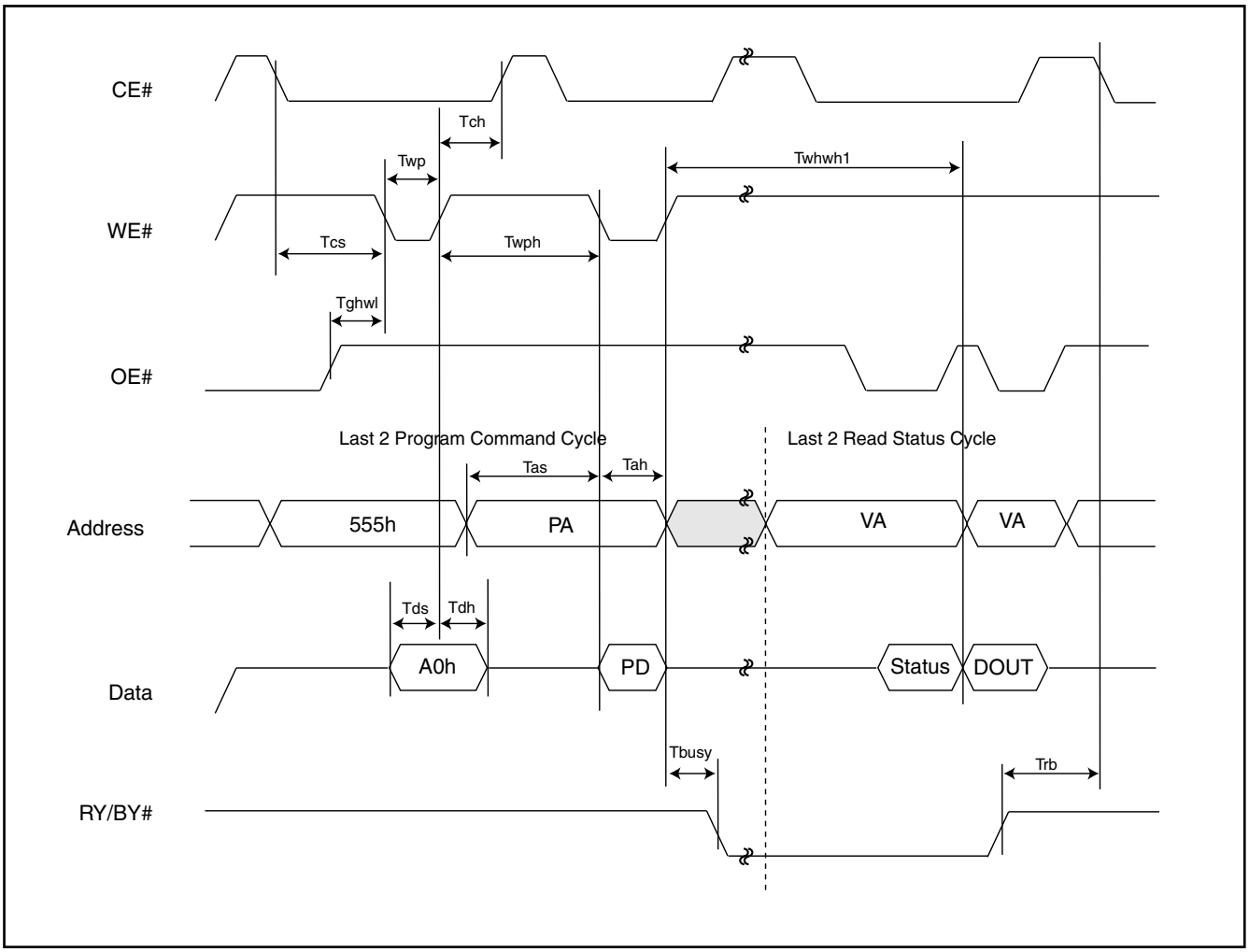
**Figure 26. AUTOMATIC SECTOR ERASE TIMING WAVEFORM**





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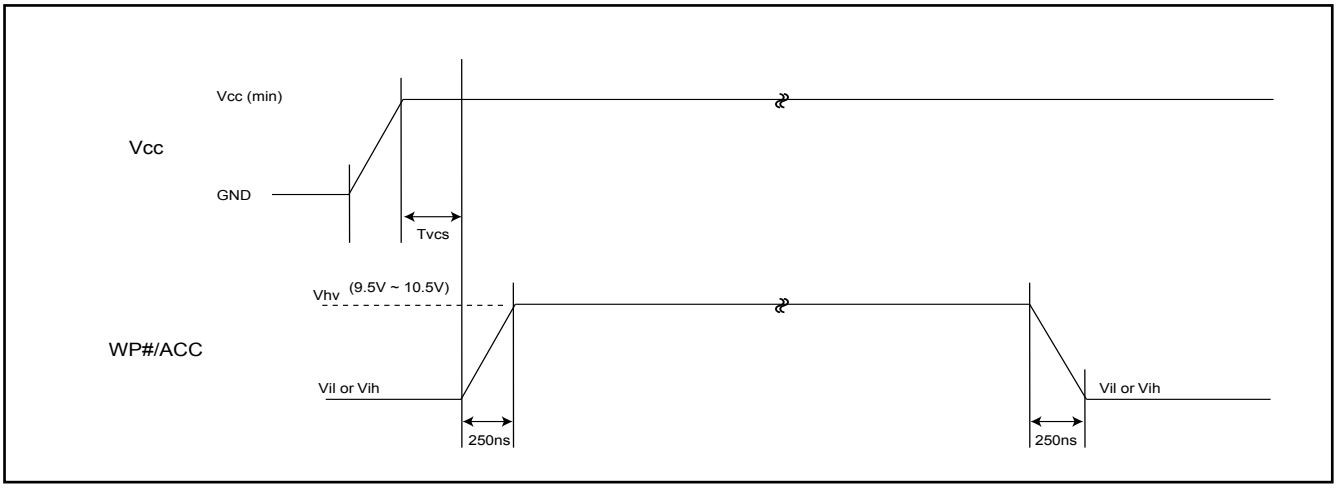
**Figure 27. AUTOMATIC PROGRAM TIMING WAVEFORM**





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**Figure 28. ACCELERATED PROGRAM TIMING WAVEFORM**

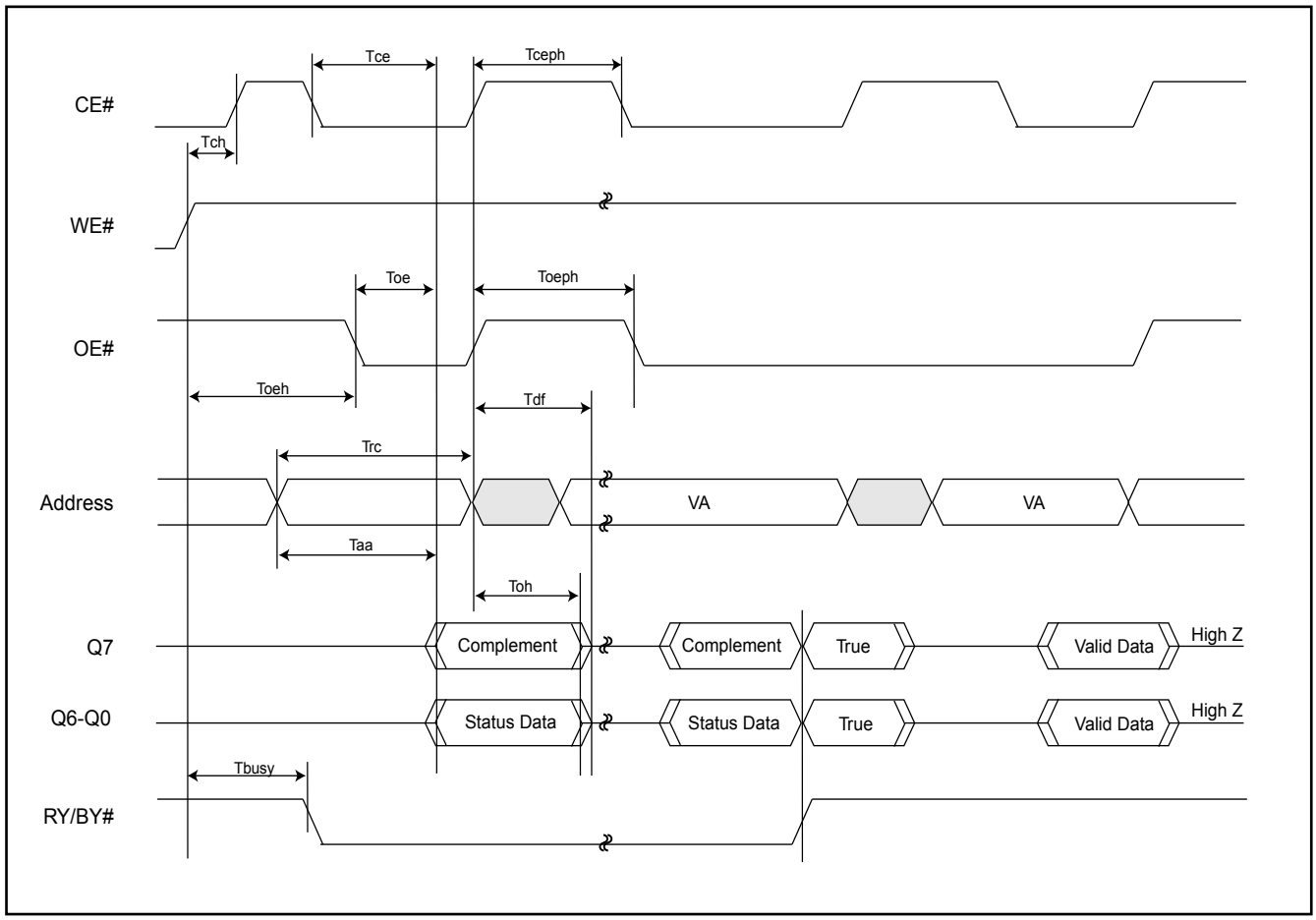




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## 11-9. WRITE STATUS OPERATION

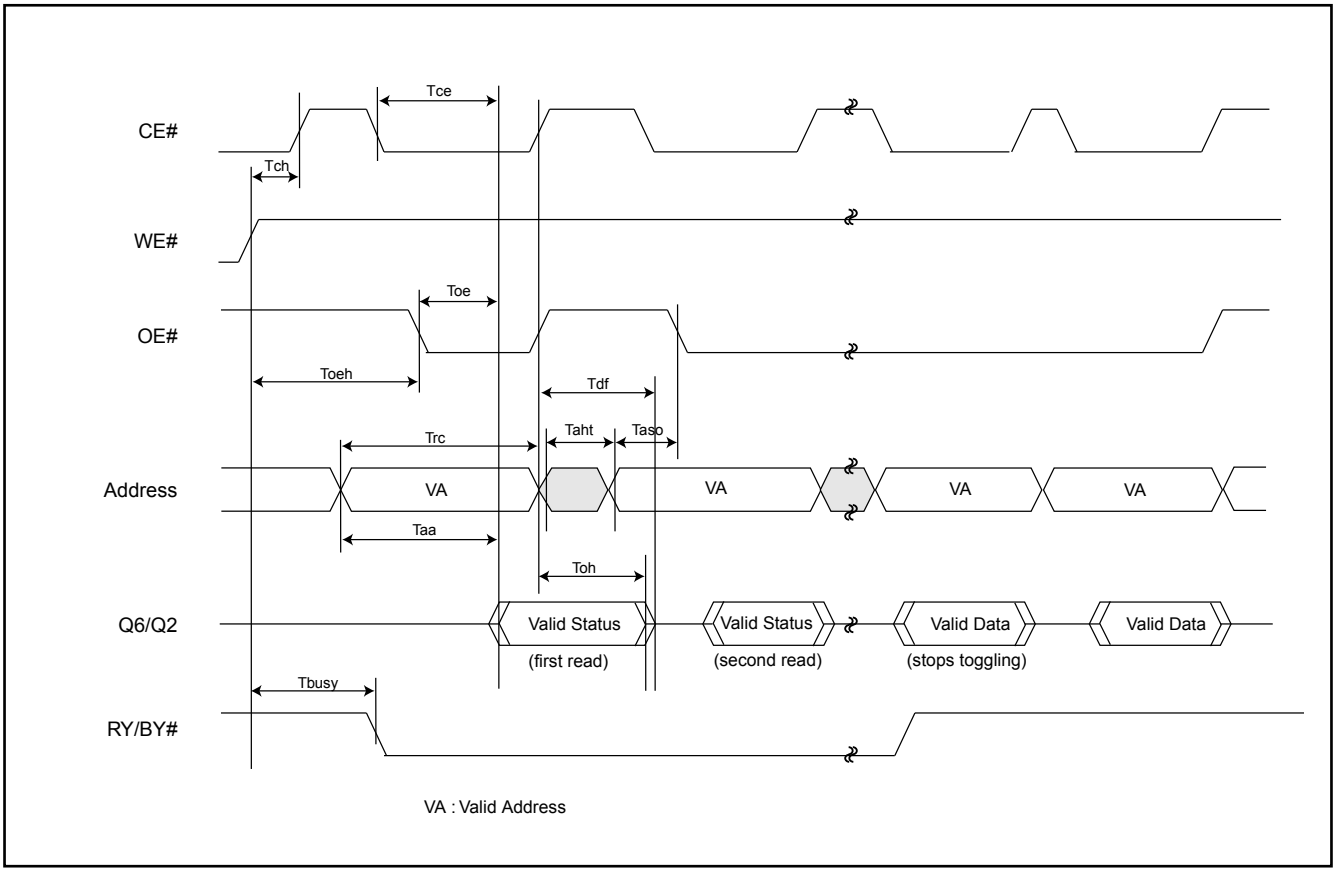
**Figure 29. DATA# POLLING TIMING WAVEFORM (for AUTOMATIC MODE)**





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**Figure 30. TOGGLE BIT TIMING WAVEFORM**





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## 11-10. RECOMMENDED OPERATING CONDITIONS

### 11-10-1. At Device Power-Up

AC timing illustrated in *"Figure 31. AC TIMING AT DEVICE POWER-UP"* is recommended for the supply voltages and the control signals at device power-up (e.g. Vcc and CE# ramp up simultaneously). If the timing in the figure is ignored, the device may not operate correctly.

**Figure 31. AC TIMING AT DEVICE POWER-UP**

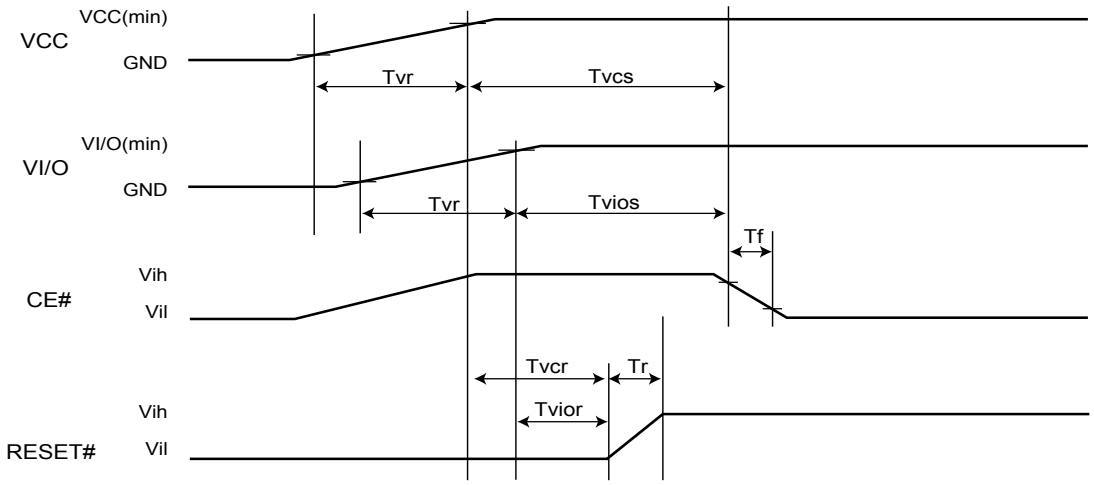



**Table 18. AC CHARACTERISTICS (AC TIMING AT DEVICE POWER-UP)**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| Tvr | VCC Rise Time | | 500000 | us/V |
| Tr | Input Signal Rise Time | | 20 | us/V |
| Tf | Input Signal Fall Time | | 20 | us/V |
| Tvcs/Tvcr | VCC Setup Time | 300 | | us |
| Tvios/Tvior | VI/O Setup Time | 300 | | us |

**Notes:**
1. Not 100% test.
2. VI/O < VCC+200mV.


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### 11-10-2. Power Up/Down and Voltage Drop

When powering down the device, VCC must drop below $V_{PWD}$ for at least $T_{PWD}$ to ensure the device will initialize correctly during power up. Please refer to *"Figure 32. POWER UP/DOWN AND VOLTAGE DROP"* and *"Table 19. AC CHARACTERISTICS (POWER UP/DOWN AND VOLTAGE DROP)"* below for more details.

**Figure 32. POWER UP/DOWN AND VOLTAGE DROP**

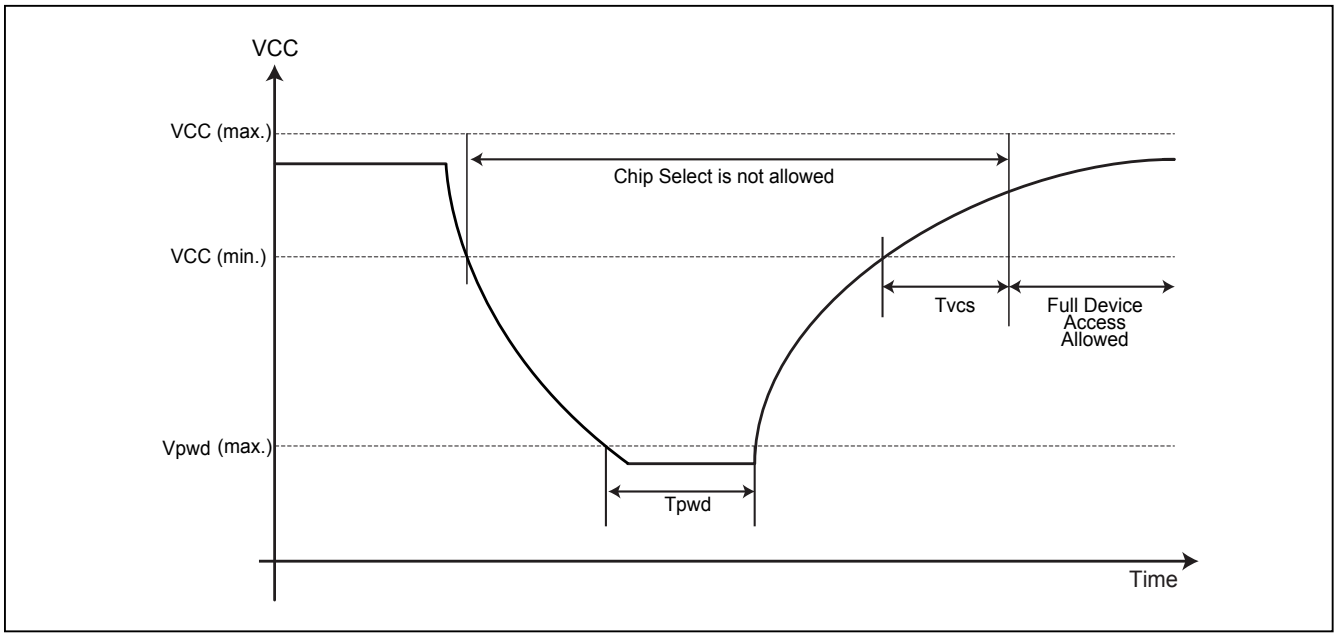



**Table 19. AC CHARACTERISTICS (POWER UP/DOWN AND VOLTAGE DROP)**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| Vpwd | Voltage level below which device needs to be re-initialized | | 0.9 | V |
| Tpwd | Time interval for VCC is below Vpwd | 300 | | us |
| Tvcs | VCC Setup Time | 300 | | us |
| Tvr | VCC Rise Time | | 500000 | us/V |
| VCC | VCC Power Supply | 2.7 | 3.6 | V |

**Notes:**
1. Not 100% test.


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## 11-11. ERASE AND PROGRAM PERFORMANCE

| Description | | Limits | | Units |
|---|---|---|---|---|
| | | Typ.(1) | Max.(2) | |
| Chip Erase Time | 512Mb | 100 | 250 | sec |
| | 1Gb | 200 | 500 | sec |
| Sector Erase Time | | 0.25 | 1.4 | sec |
| Word Program Time | | 30 | 230 | us |
| Total Write Buffer Time | | 284 | 1,400 | us |
| Total ACC Write Buffer Time | | 200 | | us |
| Erase/Program Cycles | | 100,000 | | Cycles |
| Blank Check | | | 10 | ms |

**Notes:**
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC. Program specifications assume checkboard data pattern.
2. Maximum values are measured at VCC = 3.0V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Erase/Program cycles comply with JEDEC JESD-47 & JESD 22-A117 standard.
4. Exclude 00h program before erase operation.

## 11-12. DATA RETENTION

| Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|
| Data retention | 55˚C | 20 | | years |

## 11-13. LATCH-UP CHARACTERISTICS

| Description | Min. | Max. |
|---|---|---|
| Input Voltage voltage difference with GND on WP#/ACC and A9 pins | -1.0V | 10.5V |
| Input Voltage voltage difference with GND on all normal pins input | -1.0V | 1.5Vcc |
| Vcc Current | -100mA | +100mA |

**Notes:**
1. All pins included except VCC. Test conditions: VCC = 3.0V, one pin per testing


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## 11-14. PIN CAPACITANCE

**Table 20. PIN CAPACITANCE: 56-TSOP**

| Symbol | Description | | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| CIN2 | Control Pin Capacitance | 512Mb | 3 | 7 | pF | VIN=0 |
| | | 1Gb | 6 | 14 | pF | |
| CIN | Input Capacitance | 512Mb | 7 | 8 | pF | VIN=0 |
| | | 1Gb | 14 | 16 | pF | |
| COUT | Output Capacitance | 512Mb | 5 | 6 | pF | VOUT=0 |
| | | 1Gb | 10 | 12 | pF | |
| RY/BY# | Output Capacitance | 512Mb | 3 | 4 | pF | VOUT=0 |
| | | 1Gb | 6 | 8 | pF | |

**Notes:**
1. Not 100% tested, WP#/ACC pin not included.

**Table 21. PIN CAPACITANCE: 64-LFBGA**

| Symbol | Description | | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| CIN2 | Control Pin Capacitance | 512Mb | 4 | 9 | pF | VIN=0 |
| | | 1Gb | 8 | 18 | pF | |
| CIN | Input Capacitance | 512Mb | 8 | 9 | pF | VIN=0 |
| | | 1Gb | 16 | 18 | pF | |
| COUT | Output Capacitance | 512Mb | 5 | 7 | pF | VOUT=0 |
| | | 1Gb | 10 | 14 | pF | |
| RY/BY# | Output Capacitance | 512Mb | 3 | 4 | pF | VOUT=0 |
| | | 1Gb | 6 | 8 | pF | |

**Notes:**
1. Not 100% tested, WP#/ACC pin not included.


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## 12. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

| PART NO. | ACCESS TIME (ns) | | PACKAGE | Remark |
|---|---|---|---|---|
| | Vcc=3.0 to 3.6V | Vcc=2.7 to 3.6V | | |
| ***MX29GL512G*** | | | | |
| MX29GL512GHXFI-10G | 100 | 100 | 64 LFBGA | VI/O=VCC |
| MX29GL512GLXFI-10G | 100 | 100 | 64 LFBGA | VI/O=VCC |
| MX29GL512GHT2I-10G | 100 | 100 | 56 Pin TSOP | VI/O=VCC |
| MX29GL512GLT2I-10G | 100 | 100 | 56 Pin TSOP | VI/O=VCC |
| MX29GL512GUXFI-11G | 110 | 110 | 64 LFBGA | VI/O=1.65 to VCC |
| MX29GL512GDXFI-11G | 110 | 110 | 64 LFBGA | VI/O=1.65 to VCC |
| MX29GL512GUT2I-11G | 110 | 110 | 56 Pin TSOP | VI/O=1.65 to VCC |
| MX29GL512GDT2I-11G | 110 | 110 | 56 Pin TSOP | VI/O=1.65 to VCC |
| MX29GL512GHXFI-10Q | 95 | 100 | 64 LFBGA | VI/O=VCC |
| MX29GL512GLXFI-10Q | 95 | 100 | 64 LFBGA | VI/O=VCC |
| MX29GL512GHT2I-10Q | 95 | 100 | 56 Pin TSOP | VI/O=VCC |
| MX29GL512GLT2I-10Q | 95 | 100 | 56 Pin TSOP | VI/O=VCC |
| MX29GL512GUXFI-11Q | 105 | 110 | 64 LFBGA | VI/O=1.65 to VCC |
| MX29GL512GDXFI-11Q | 105 | 110 | 64 LFBGA | VI/O=1.65 to VCC |
| MX29GL512GUT2I-11Q | 105 | 110 | 56 Pin TSOP | VI/O=1.65 to VCC |
| MX29GL512GDT2I-11Q | 105 | 110 | 56 Pin TSOP | VI/O=1.65 to VCC |
| ***MX68GL1G0G*** | | | | |
| MX68GL1G0GHT2I-10G | 100 | 100 | 56 Pin TSOP | VI/O=VCC |
| MX68GL1G0GLT2I-10G | 100 | 100 | 56 Pin TSOP | VI/O=VCC |
| MX68GL1G0GUT2I-11G | 110 | 110 | 56 Pin TSOP | VI/O=1.65 to VCC |
| MX68GL1G0GDT2I-11G | 110 | 110 | 56 Pin TSOP | VI/O=1.65 to VCC |
| MX68GL1G0GHT2I-10Q | 95 | 100 | 56 Pin TSOP | VI/O=VCC |
| MX68GL1G0GLT2I-10Q | 95 | 100 | 56 Pin TSOP | VI/O=VCC |
| MX68GL1G0GUT2I-11Q | 105 | 110 | 56 Pin TSOP | VI/O=1.65 to VCC |
| MX68GL1G0GDT2I-11Q | 105 | 110 | 56 Pin TSOP | VI/O=1.65 to VCC |
| MX68GL1G0GHXFI-10Q* | 95 | 100 | 64 LFBGA | VI/O=VCC |
| MX68GL1G0GLXFI-10Q* | 95 | 100 | 64 LFBGA | VI/O=VCC |
| MX68GL1G0GUXFI-11Q* | 105 | 110 | 64 LFBGA | VI/O=1.65 to VCC |
| MX68GL1G0GDXFI-11Q* | 105 | 110 | 64 LFBGA | VI/O=1.65 to VCC |

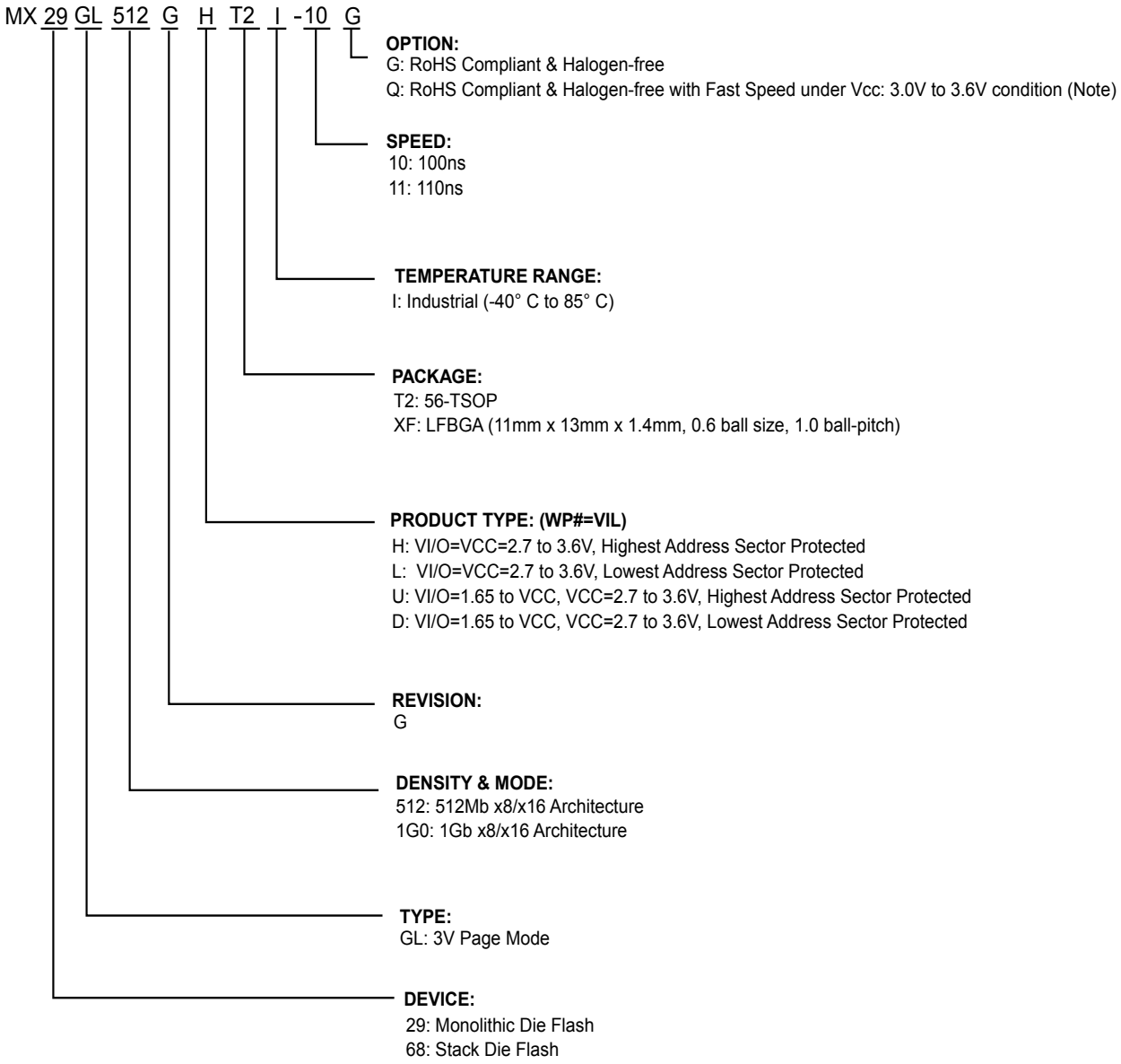
***Notes: *Advanced Information***

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## 13. PART NAME DESCRIPTION



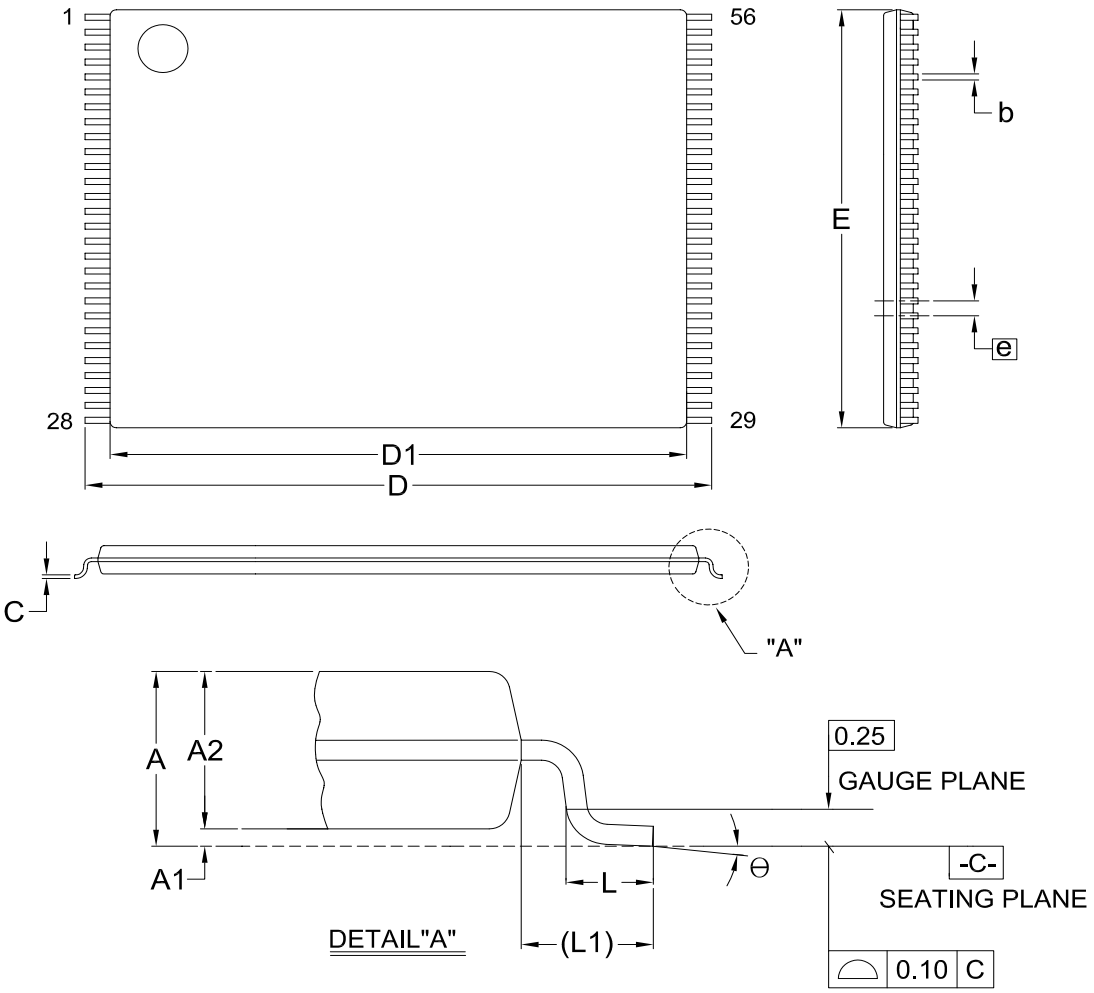

Note:10Q covers 2.7~3.6V for 100ns and 3.0~3.6V for 95ns
11Q covers 2.7~3.6V for 110ns and 3.0~3.6V for 105ns


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## 14. PACKAGE INFORMATION

**56-Pin TSOP**

Doc. Title: Package Outline for TSOP(I) 56L (14X20mm)



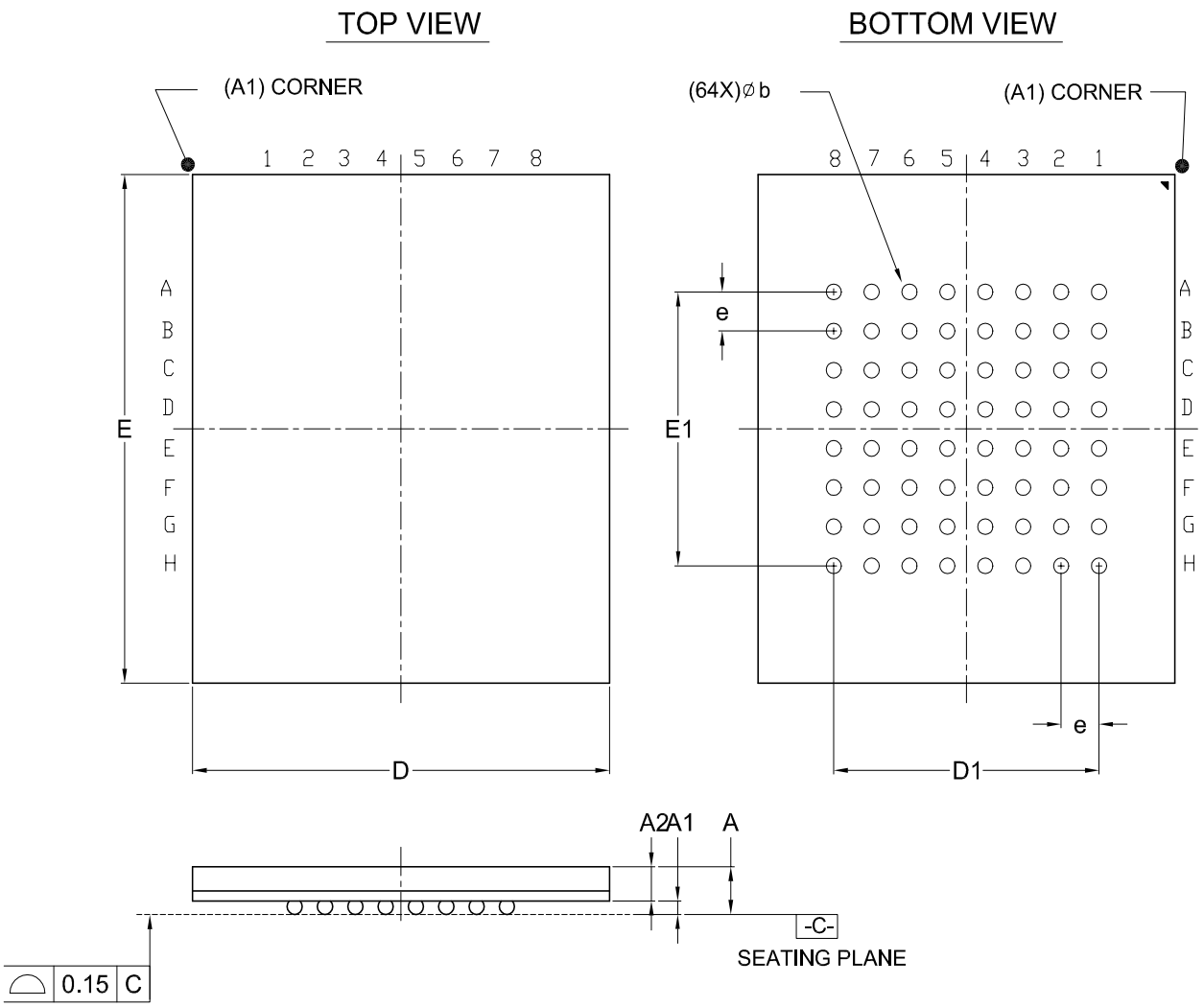

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | D1 | E | e | L | L1 | Θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | — | 0.05 | 0.95 | 0.17 | 0.10 | 19.80 | 18.30 | 13.90 | — | 0.50 | 0.70 | 0° |
| | Nom. | — | 0.10 | 1.00 | 0.20 | 0.13 | 20.00 | 18.40 | 14.00 | 0.50 | 0.60 | 0.80 | 5° |
| | Max. | 1.20 | 0.15 | 1.05 | 0.27 | 0.21 | 20.20 | 18.50 | 14.10 | — | 0.70 | 0.90 | 8° |
| Inch | Min. | — | 0.002 | 0.037 | 0.007 | 0.004 | 0.780 | 0.720 | 0.547 | — | 0.020 | 0.028 | 0° |
| | Nom. | — | 0.004 | 0.039 | 0.008 | 0.005 | 0.787 | 0.724 | 0.551 | 0.020 | 0.024 | 0.031 | 5° |
| | Max. | 0.047 | 0.006 | 0.041 | 0.011 | 0.008 | 0.795 | 0.728 | 0.555 | — | 0.028 | 0.035 | 8° |


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**64-Ball LFBGA (11mm x 13mm)**

Doc. Title: Package Outline for CSP 64BALL(11X13X1.4MM,BALL PITCH 1.00MM,BALL DIAMETER 0.6MM)




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.40 | 0.65 | 0.50 | 10.90 | | 12.90 | | |
| | Nom. | --- | 0.50 | --- | 0.60 | 11.00 | 7.00 | 13.00 | 7.00 | 1.00 |
| | Max. | 1.40 | 0.60 | --- | 0.70 | 11.10 | | 13.10 | | |
| Inch | Min. | --- | 0.016 | 0.026 | 0.020 | 0.429 | | 0.508 | | |
| | Nom. | --- | 0.020 | --- | 0.024 | 0.433 | 0.276 | 0.512 | 0.276 | 0.039 |
| | Max. | 0.055 | 0.024 | --- | 0.028 | 0.437 | | 0.516 | | |


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## 15. REVISION HISTORY

| Revision No. | Description | Page | Date |
|---|---|---|---|
| 0.01 | 1. Modified descriptions, figures and tables | All | JAN/23/2014 |
| | 2. Removed Multi-sector Erase Function | P21,22,62 | |
| | 3. Modified parameters of "CFI Mode" Table | P45~47 | |
| | 4. Modified parameters of "ERASE AND PROGRAM PERFORMANCE" Table | P6,53,69 | |
| | 5. Modified DC Characteristics, Reset timing & Program, Erase Suspend / Resume latency | P50,51,59 | |
| 1.0 | 1. Removed 56-Ball FBGA Package | P7,9 | MAY/29/2014 |
| | 2. Modified DC Characteristics Table | P50 | |
| | 3. Modified Reset#, AC Power-Up, Power Up/Down Timing Table | P59,67,68 | |
| | 4. Modified parameters of "Erase and Program Performance" Table | P69 | |
| | 5. Modified PIN Capacitance | P70 | |
| | 6. Separate 256Mb part from this datasheet revision | All | |
| | 7. Removed Preliminary status | All | |
| 1.1 | 1. Modified the ordering information of MX68GL1G0G | P71 | NOV/26/2015 |
| | 2. Content correction | P37 | |
| 1.2 | 1. Added a statement for product ordering information | P71 | FEB/17/2017 |
| | 2. Modified the ordering information of MX68GL1G0G | P71 | |
| | 3. Updated tVR descriptions. | P67-68 | |
| | 4. Description modifications. | P54-55 | |
| 1.3 | 1. Added "Macronix Proprietary" footnote. | All | JUL/05/2018 |
| | 2. Added part numbers of with Fast Speed under Vcc 3.0V to 3.6V condition | P71-72 | |
| | 3. Format modification. | P73-74 | |
| 1.4 | 1. Added PAGE BUFFER SRAM in the BLOCK DIAGRAM. | P10-11 | MAY/29/2020 |
| | 2. Revised AC CHARACTERISTICS. | P52 | |
| | 3. Updated the maximum Sector erase operation value and the descriptions of Tghwl and Tghel parameters. | P53 | |
| | 4. Revised Figure 18. COMMAND WRITE TIMING WAVEFORM (WE# CONTROLLED) and Figure 19. COMMAND WRITE TIMING WAVEFORM (CE# CONTROLLED). | P54-55 | |
| | 5. Added the maximum Total Write Buffer Time value. | P69 | |
| | 6. Updated the ordering information. | P71 | |


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