# MX25L8006E

## 3V, 8M-BIT [x 1/x 2]
## CMOS SERIAL FLASH MEMORY

### *Key Features*

- *Hold Feature*
- *Low Power Consumption*
- *Auto Erase and Auto Program Algorithms*
- *Additional 512 bit secured OTP for unique identifier*

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## 8M-BIT [x 1 / x 2] CMOS SERIAL FLASH

## FEATURES

### GENERAL

- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 8,388,608 x 1 bit structure or 4,194,304 x 2 bits (Dual Output mode) structure
- 256 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 16 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Program Capability
  - Byte base
  - Page base (256 bytes)
- Latch-up protected to 100mA from -1V to Vcc +1V

### PERFORMANCE

- High Performance
  - Fast access time: 86MHz serial clock
  - Serial clock of Dual Output mode : 80MHz
  - Fast program time: 0.6ms(typ.) and 3ms(max.)/page
  - Byte program time: 9us (typical)
  - Fast erase time: 40ms(typ.) /sector ; 0.4s(typ.) /block
- Low Power Consumption
  - Low active read current: 12mA(max.) at 86MHz
  - Low active programming current: 15mA (typ.)
  - Low active Sector/Block erase current: 9mA (typ.)
  - Low standby current: 15uA (typ.)
  - Deep power-down mode 2uA (typ.)
- Typical 100,000 erase/program cycles
- 20 years of data retention

### SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
    The BP2-BP0 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 512 bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode



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**HARDWARE FEATURES**

- PACKAGE
  - 8-pin SOP (150mil)
  - 8-pin SOP (200mil)
  - 8-pin PDIP (300mil)
  - 8-land WSON (6x5mm)
  - 8-land USON (4x4mm)
  - **All devices are RoHS Compliant and Halogen-free**

## GENERAL DESCRIPTION

The device features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in Dual Output read mode, the SI and SO pins become SIO0 and SIO1 pins for data output.

The device provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page basis, or word basis. Erase command is executed on sector, or block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

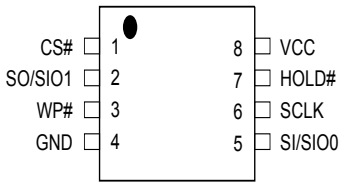
Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

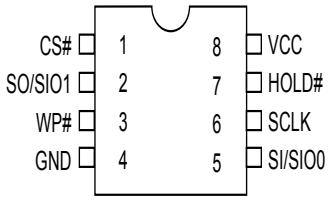
The device utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after typical 100,000 program and erase cycles.

## PIN CONFIGURATIONS

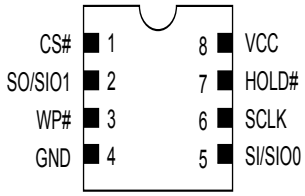
### 8-PIN SOP (200mil, 150mil)




### 8-PIN PDIP (300mil)




### 8-LAND WSON (6x5mm), USON (4x4mm)

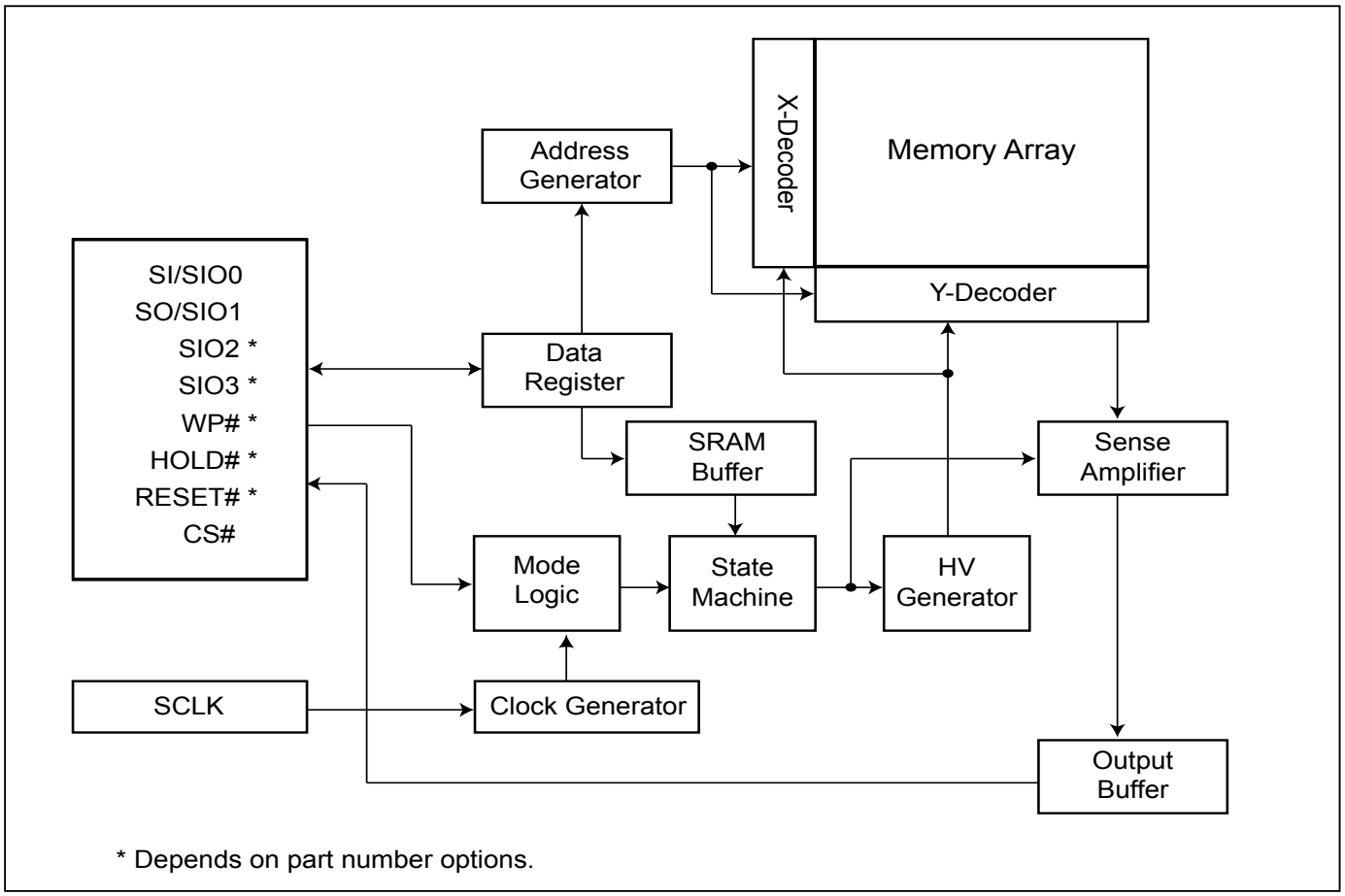



## PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| CS# | Chip Select |
| SI/SIO0 | Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for Dual Output mode) |
| SO/SIO1 | Serial Data Output (for 1 x I/O)/ Serial Data Output (for Dual Output mode) |
| SCLK | Clock Input |
| WP# | Write protection |
| HOLD# | Hold, to pause the device without deselecting the device |
| VCC | + 3.3V Power Supply |
| GND | Ground |


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## BLOCK DIAGRAM



## MEMORY ORGANIZATION

**Table 1. Memory Organization**

| Block | Sector | Address Range | |
|---|---|---|---|
| 15 | 255 | 0FF000h | 0FFFFFh |
| | : | : | : |
| | 240 | 0F0000h | 0F0FFFh |
| 14 | 239 | 0EF000h | 0EFFFFh |
| | : | : | : |
| | 224 | 0E0000h | 0E0FFFh |
| : | : | : | : |
| : | : | : | : |
| 0 | 15 | 00F000h | 00FFFFh |
| | : | : | : |
| | 3 | 003000h | 003FFFh |
| | 2 | 002000h | 002FFFh |
| | 1 | 001000h | 001FFFh |
| | 0 | 000000h | 000FFFh |

## DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z. The CS# falling time needs to follow tCHCL spec.

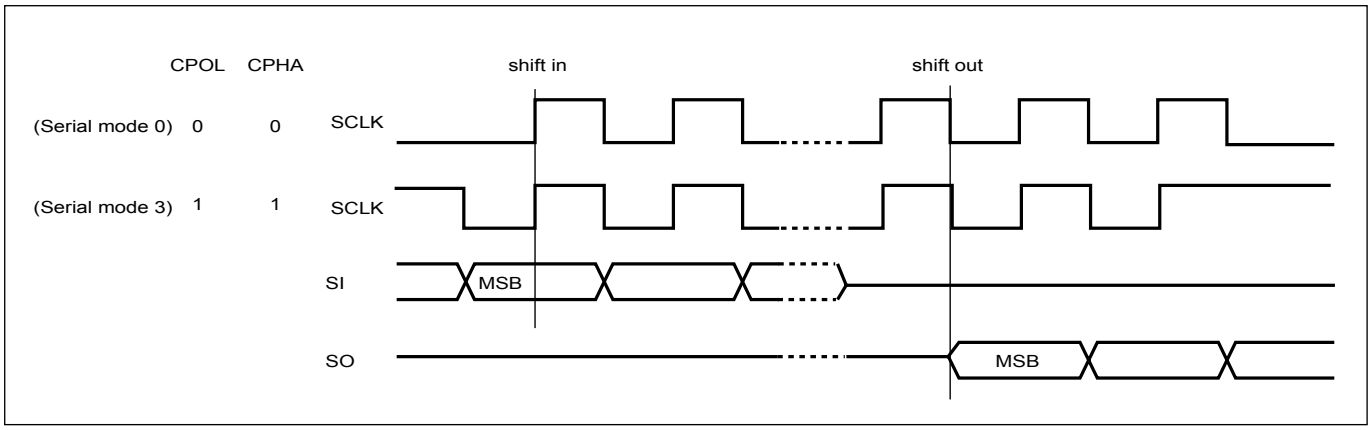
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge. The CS# rising time needs to follow tCLCH spec.

4. Input data is latched on the rising edge of Serial Clock(SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown in Figure 1.

5. For the following instructions:RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, DREAD, RES, and REMS the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, RDP, DP, ENSO, EXSO,and WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

**Figure 1. Serial Modes Supported**




Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.


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## DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).

- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

**I. Block lock protection**

- The Software Protected Mode (SPM):

MX25L8006E: use (BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The proected area definition is shown as *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP2 bits.

Please refer to *"Table 2. Protected Area Sizes"*.

- The Hardware Proteced Mode (HPM) uses WP# to protect the MX25L8006E:BP2-BP0 bits and SRWD bit.

**Table 2. Protected Area Sizes**

| Status bit | | | Protect Level |
|---|---|---|---|
| **BP2** | **BP1** | **BP0** | **MX25L8006E** |
| 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 1 | 1 (1block, block 15th) |
| 0 | 1 | 0 | 2 (2blocks, block 14th-15th) |
| 0 | 1 | 1 | 3 (4blocks, block 12th-15th) |
| 1 | 0 | 0 | 4 (8blocks, block 8th-15th) |
| 1 | 0 | 1 | 5 (All) |
| 1 | 1 | 0 | 6 (All) |
| 1 | 1 | 1 | 7 (All) |

**II. Additional 512 bit secured OTP** for unique identifier: to provide 512 bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to *"Table 3. 512 bit Secured OTP Definition"*.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 512 bit secured OTP by entering 512 bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 512 bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 8. SECURITY REGISTER DEFINITION"* for security register bit definition and *"Table 3. 512 bit Secured OTP Definition"* for address range definition.
- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 512 bit secured OTP mode, array access is not allowed.

**Table 3. 512 bit Secured OTP Definition**

| Address range | Size | Standard Factory Lock | Customer Lock |
|---|---|---|---|
| xxxx00-xxxx0F | 128-bit | ESN (electrical serial number) | Determined by customer |
| xxxx10-xxxx3F | 384-bit | N/A | |

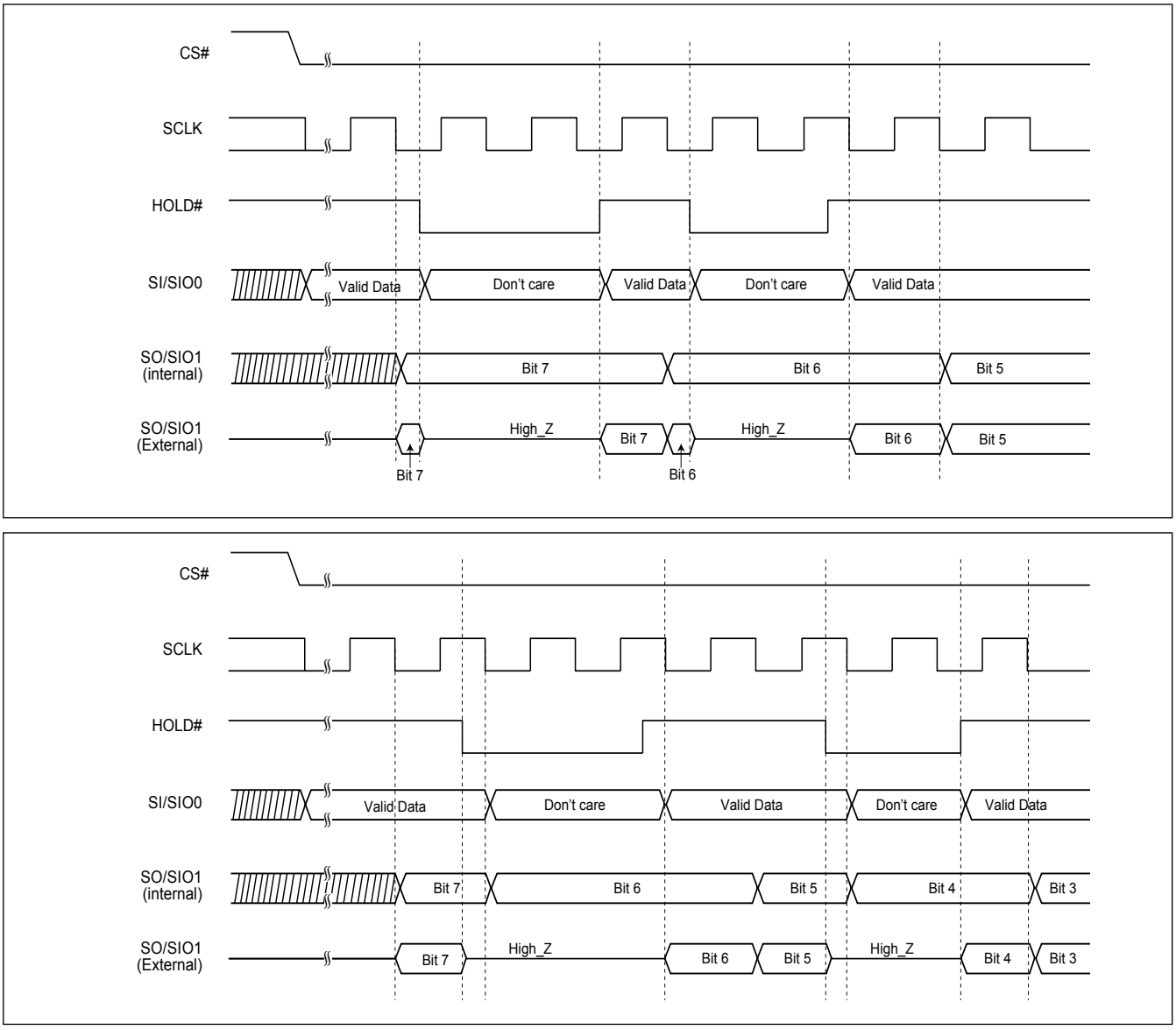

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## HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

**Figure 2. Hold Condition Operation**




During the HOLD operation, the Serial Data Output (SO) is high impedance when Hold# pin goes low and will keep high impedance until Hold# pin goes high and SCLK goes low. The Serial Data Input (SI) is don't care if both Serial Clock (SCLK) and Hold# pin goes low and will keep the state until SCLK goes low and Hold# pin goes high. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Note: The HOLD feature is disabled during Quad I/O mode.


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## COMMAND DESCRIPTION

**Table 4. COMMAND DEFINITION**

| Command (byte) | WREN (write enable) | WRDI (write disable) | WRSR (write status register) | RDID (read identific-ation) | RDSR (read status register) | READ (read data) | FAST READ (fast read data) |
|---|---|---|---|---|---|---|---|
| 1st byte | 06 (hex) | 04 (hex) | 01 (hex) | 9F (hex) | 05 (hex) | 03 (hex) | 0B (hex) |
| 2nd byte | | | | | | AD1 | AD1 |
| 3rd byte | | | | | | AD2 | AD2 |
| 4th byte | | | | | | AD3 | AD3 |
| 5th byte | | | | | | | Dummy |
| Action | sets the (WEL) write enable latch bit | resets the (WEL) write enable latch bit | to write new values to the status register | outputs JEDEC ID: 1-byte Manufact-urer ID & 2-byte Device ID | to read out the values of the status register | n bytes read out until CS# goes high | n bytes read out until CS# goes high |

| Command (byte) | RDSFDP (Read SFDP) | RES (read electronic ID) | REMS (read electronic manufacturer & device ID) | DREAD (Double Output Mode command) | SE (sector erase) | BE (block erase) | CE (chip erase) |
|---|---|---|---|---|---|---|---|
| 1st byte | 5A (hex) | AB (hex) | 90 (hex) | 3B (hex) | 20 (hex) | 52 or D8 (hex) | 60 or C7 (hex) |
| 2nd byte | AD1 | x | x | AD1 | AD1 | AD1 | |
| 3rd byte | AD2 | x | x | AD2 | AD2 | AD2 | |
| 4th byte | AD3 | x | ADD *(Note 1)* | AD3 | AD3 | AD3 | |
| 5th byte | Dummy | | | Dummy | | | |
| Action | Read SFDP mode | to read out 1-byte Device ID | output the Manufacturer ID & Device ID | n bytes read out by Dual Output until CS# goes high | to erase the selected sector | to erase the selected block | to erase whole chip |

| Command (byte) | PP (page program) | RDSCUR (read security register) | WRSCUR (write security register) | ENSO (enter secured OTP) | EXSO (exit secured OTP) | DP (Deep power down) | RDP (Release from deep power down) |
|---|---|---|---|---|---|---|---|
| 1st byte | 02 (hex) | 2B (hex) | 2F (hex) | B1 (hex) | C1 (hex) | B9 (hex) | AB (hex) |
| 2nd byte | AD1 | | | | | | |
| 3rd byte | AD2 | | | | | | |
| 4th byte | AD3 | | | | | | |
| 5th byte | | | | | | | |
| Action | to program the selected page | to read value of security register | to set the lock-down bit as "1" (once lock-down, cannot be updated) | to enter the 512 bit secured OTP mode | to exit the 512 bit secured OTP mode | enters deep power down mode | release from deep power down mode |

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
Note 2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.


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**(1) Write Enable (WREN)**

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, SE, BE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence is shown as *Figure 13*.

**(2) Write Disable (WRDI)**

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence is shown as *Figure 14*.

The WEL bit is reset by following situations:
- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion

**(3) Read Status Register (RDSR)**

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence is shown as *Figure 15*.

The definition of the status register bits is as below:

**WIP bit.** The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

**WEL bit.** The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and not affect value of WEL bit if it is applied to a protected memory area.

**BP2, BP1, BP0 bits.** The Block Protect (BP2-BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP2-BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase(CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed).


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**SRWD bit.** The Status Register Write Disable (SRWD) bit, non-volatile bit, and its default value is "0". SRWD bit is operated together with Write Protection (WP#) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP# pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP2-BP0) are read only. The SRWD bit defaults to be "0".

**Table 5. Status Register**

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| SRWD (status register write protect) | 0 | 0 | BP2 (level of protected block) | BP1 (level of protected block) | BP0 (level of protected block) | WEL (write enable latch) | WIP (write in progress bit) |
| 1=status register write disabled 0=status register write enabled | 0 | 0 | *(note 1)* | *(note 1)* | *(note 1)* | 1=write enable 0=not write enable | 1=write operation 0=not in write operation |
| Non-volatile bit | 0 | 0 | Non-volatile bit | Non-volatile bit | Non-volatile bit | volatile bit | volatile bit |

note 1: Please refer to the *"Table 2. Protected Area Sizes"*.

**(4) Write Status Register (WRSR)**

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP2-BP0) bits to define the protected area of memory (as shown in *"Table 2. Protected Area Sizes"*). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#) pin signal. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence is shown as *Figure 16*.

The WRSR instruction has no effect on b6, b1, b0 of the status register.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.


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**Table 6. Protection Modes**

| Mode | Status register condition | WP# and SRWD bit status | Memory |
|---|---|---|---|
| Software protection mode (SPM) | Status register can be written in (WEL bit is set to "1") and the SRWD, BP2-BP0 bits can be changed | WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1 | The protected area cannot be program or erase. |
| Hardware protection mode (HPM) | The SRWD, BP2-BP0 of status register bits cannot be changed | WP#=0, SRWD bit=1 | The protected area cannot be program or erase. |

Note:
1. As defined by the values in the Block Protect (BP2-BP0) bits of the Status Register, as shown in *"Table 2. Protected Area Sizes"*.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):
- When SRWD bit=0, no matter WP# is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP2-BP0. The protected area, which is defined by BP2-BP0 is at software protected mode (SPM).
- When SRWD bit=1 and WP# is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP2-BP0. The protected area, which is defined by BP2-BP0, is at software protected mode (SPM).

Note: If SRWD bit=1 but WP# is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):
- When SRWD bit=1, and then WP# is low (or WP# is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP2-BP0 and hardware protected mode by the WP# to against data modification.

Note: to exit the hardware protected mode requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP2-BP0.

**(5) Read Data Bytes (READ)**

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence is shown as *Figure 17*.

**(6) Read Data Bytes at Higher Speed (FAST_READ)**

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence is shown as *Figure 18*.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

**(7) Dual Output Mode (DREAD)**

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits(interleave on 1I/2O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the data out will perform as 2-bit instead of previous 1-bit.

The sequence is shown as *Figure 19*.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

The DREAD only perform read operation. Program/Erase /Read ID/Read status....operation do not support DREAD throughputs.

**(8) Sector Erase (SE)**

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see *"Table 1. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence is shown as *Figure 20*.


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The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Sector Erase cycle is in progress. The WIP sets during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP2-BP0 bits, the Sector Erase (SE) instruction will not be executed on the page.

**(9) Block Erase (BE)**

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte sector erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see *"Table 1. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence is shown as *Figure 21*.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP2-BP0 bits, the Block Erase (BE) instruction will not be executed on the page.

**(10) Chip Erase (CE)**

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). Any address of the sector (see *"Table 1. Memory Organization"*) is a valid address for Chip Erase (CE) instruction. The CS# must go high exactly at the byte boundary( the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence is shown as *Figure 22*.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the chip is protected by BP2-BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP2-BP0 all set to "0".

**(11) Page Program (PP)**

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The last address byte (the eight least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. The CS# must keep during the whole Page Program cycle. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the requested page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

The sequence is shown as *Figure 23*.


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The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP2-BP0 bits, the Page Program (PP) instruction will not be executed.

**(12) Deep Power-down (DP)**

The Deep Power-down (DP) instruction places the device into a minimum power consumption state, Deep Power-down mode, in which the quiescent current is reduced from ISB1 to ISB2.

The sequence of issuing DP instruction: CS# goes low→ send DP instruction code→ CS# goes high. The CS# must go high at the byte boundary (after exactly eighth bits of the instruction code have been latched-in); otherwise the instruction will not be executed. The sequence is shown as *Figure 24*.

After CS# goes high there is a delay of tDP before the device transitions from Stand-by mode to Deep Power-down mode and before the current reduces from ISB1 to ISB2. Once in Deep Power-down mode, all instructions will be ignored except Release from Deep Power-down (RDP).

The device exits Deep Power-down mode and returns to Stand-by mode if it receives a Release from Deep Power-down (RDP) instruction, power-cycle, or reset.

**(13) Release from Deep Power-down (RDP), Read Electronic Signature (RES)**

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *Table 13*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 7. ID DEFINITIONS"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The sequence is shown in *Figure 25* and *Figure 26*.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power Down Mode.


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### (14) Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID and Device ID are listed as *"Table 7. ID DEFINITIONS"*.

The sequence is shown as *Figure 27*.

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

### (15) Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in *"Table 7. ID DEFINITIONS"*.

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7-A0). After which the manufacturer ID for Macronix (C2h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first as shown in *"Figure 28. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)"*. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

**Table 7. ID DEFINITIONS**

| Command Type | MX25L8006E | | |
|---|---|---|---|
| RDID Command | Manufacturer ID | Memory Type | Memory Density |
| | C2 | 20 | 14 |
| RES Command | Electronic ID | | |
| | 13 | | |
| REMS | Manufacturer ID | Device ID | |
| | C2 | 13 | |

### (16) Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 512 bit secured OTP mode. While the device is in 512 bit secured OTP mode, array access is not available. The additional 512 bit secured OTP is independent from main array, and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

### (17) Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 512 bit secured OTP mode.


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### (18) Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence is shown as *Figure 29*.

The definition of the Security Register bits is as below:

**Secured OTP Indicator bit.** The Secured OTP indicator bit shows the chip is locked by factory or not. When it is "0", it indicates non- factory lock; "1" indicates factory- lock.

**Lock-down Secured OTP (LDSO) bit.** By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 512 bit Secured OTP area cannot be updated any more.

**Table 8. SECURITY REGISTER DEFINITION**

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| x | x | x | x | x | x | LDSO (indicate if lock-down | Secured OTP indicator bit |
| reserved | reserved | reserved | reserved | reserved | reserved | 0 = not lockdown 1 = lock-down (cannot program/erase OTP) | 0 = nonfactory lock 1 = factory lock |
| volatile bit | volatile bit | volatile bit | volatile bit | volatile bit | volatile bit | non-volatile bit | non-volatile bit |

### (19) Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. Unlike write status register, the WREN instruction is not required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 512 bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

The sequence is shown as *Figure 30*.


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### (20) Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a standard of JEDEC. JESD216. v1.0.

**Figure 3. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence**

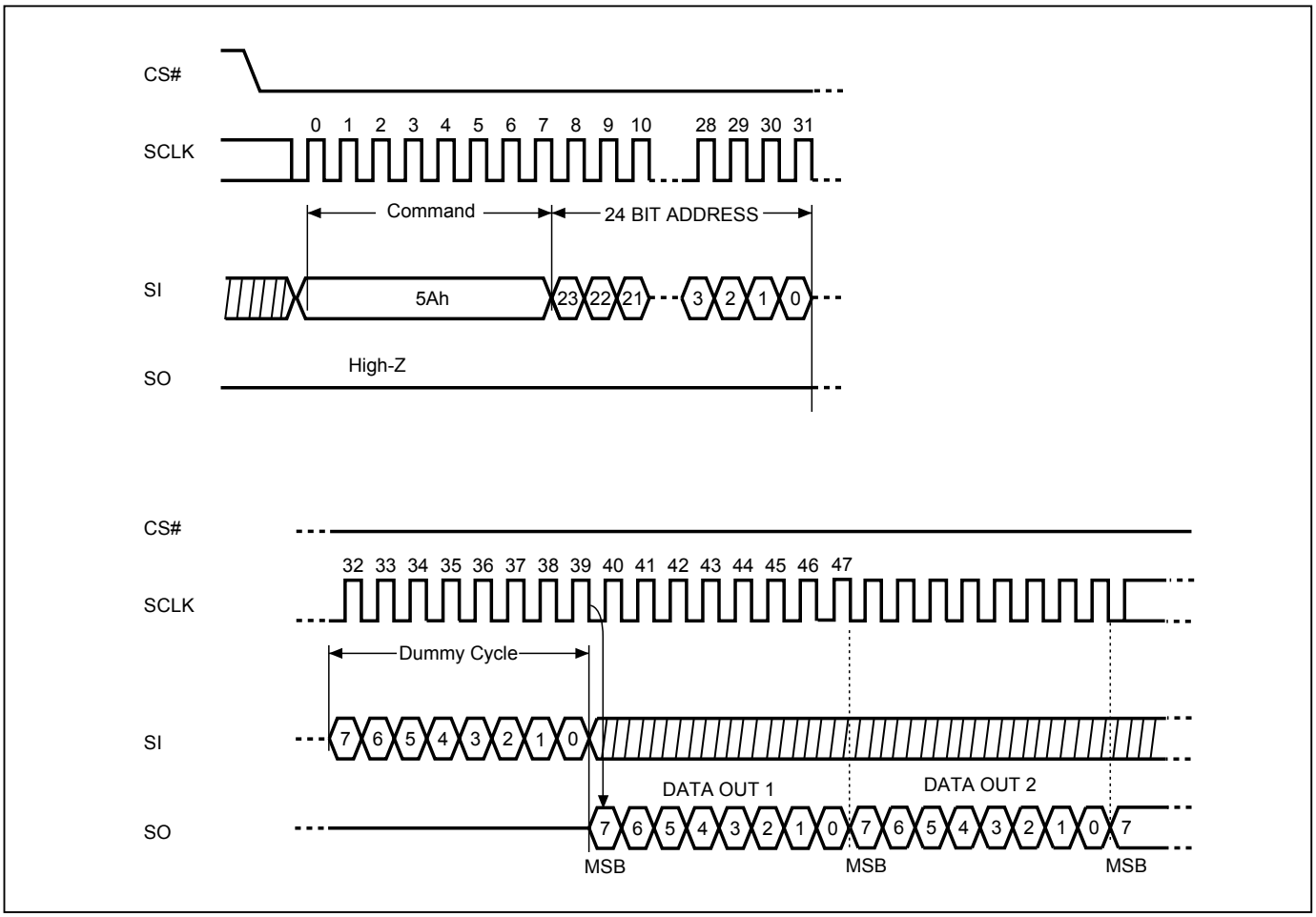


**Table 9. Signature and Parameter Identification Data Values**

SFDP Table below is for MX25L8006EM1I-12G, MX25L8006EM2I-12G, MX25L8006EPI-12G, MX25L8006EZNI-12G and MX25L8006EZUI-12G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|---|---|---|---|---|---|
| SFDP Signature | Fixed: 50444653h | 00h | 07:00 | 53h | 53h |
| | | 01h | 15:08 | 46h | 46h |
| | | 02h | 23:16 | 44h | 44h |
| | | 03h | 31:24 | 50h | 50h |
| SFDP Minor Revision Number | Start from 00h | 04h | 07:00 | 00h | 00h |
| SFDP Major Revision Number | Start from 01h | 05h | 15:08 | 01h | 01h |
| Number of Parameter Headers | This number is 0-based. Therefore, 0 indicates 1 parameter header. | 06h | 23:16 | 01h | 01h |
| Unused | | 07h | 31:24 | FFh | FFh |
| ID number (JEDEC) | 00h: it indicates a JEDEC specified header. | 08h | 07:00 | 00h | 00h |
| Parameter Table Minor Revision Number | Start from 00h | 09h | 15:08 | 00h | 00h |
| Parameter Table Major Revision Number | Start from 01h | 0Ah | 23:16 | 01h | 01h |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 0Bh | 31:24 | 09h | 09h |
| Parameter Table Pointer (PTP) | First address of JEDEC Flash Parameter table | 0Ch | 07:00 | 30h | 30h |
| | | 0Dh | 15:08 | 00h | 00h |
| | | 0Eh | 23:16 | 00h | 00h |
| Unused | | 0Fh | 31:24 | FFh | FFh |
| ID number (Macronix manufacturer ID) | it indicates Macronix manufacturer ID | 10h | 07:00 | C2h | C2h |
| Parameter Table Minor Revision Number | Start from 00h | 11h | 15:08 | 00h | 00h |
| Parameter Table Major Revision Number | Start from 01h | 12h | 23:16 | 01h | 01h |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 13h | 31:24 | 04h | 04h |
| Parameter Table Pointer (PTP) | First address of Macronix Flash Parameter table | 14h | 07:00 | 60h | 60h |
| | | 15h | 15:08 | 00h | 00h |
| | | 16h | 23:16 | 00h | 00h |
| Unused | | 17h | 31:24 | FFh | FFh |


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**Table 10. Parameter Table (0): JEDEC Flash Parameter Tables**

SFDP Table below is for MX25L8006EM1I-12G, MX25L8006EM2I-12G, MX25L8006EPI-12G, MX25L8006EZNI-12G and MX25L8006EZUI-12G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|---|---|---|---|---|---|
| Block/Sector Erase sizes | 00: Reserved, 01: 4KB erase,<br>10: Reserved,<br>11: not support 4KB erase | 30h | 01:00 | 01b | E5h |
| Write Granularity | 0: 1Byte, 1: 64Byte or larger | | 02 | 1b | |
| Write Enable Instruction Required for Writing to Volatile Status Registers | 0: not required<br>1: required 00h to be written to the status register | | 03 | 0b | |
| Write Enable Opcode Select for Writing to Volatile Status Registers | 0: use 50h opcode,<br>1: use 06h opcode<br>Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b. | | 04 | 0b | |
| Unused | Contains 111b and can never be changed | | 07:05 | 111b | |
| 4KB Erase Opcode | | 31h | 15:08 | 20h | 20h |
| (1-1-2) Fast Read (Note2) | 0=not support 1=support | 32h | 16 | 1b | 81h |
| Address Bytes Number used in addressing flash array | 00: 3Byte only, 01: 3 or 4Byte,<br>10: 4Byte only, 11: Reserved | | 18:17 | 00b | |
| Double Transfer Rate (DTR) Clocking | 0=not support 1=support | | 19 | 0b | |
| (1-2-2) Fast Read | 0=not support 1=support | | 20 | 0b | |
| (1-4-4) Fast Read | 0=not support 1=support | | 21 | 0b | |
| (1-1-4) Fast Read | 0=not support 1=support | | 22 | 0b | |
| Unused | | | 23 | 1b | |
| Unused | | 33h | 31:24 | FFh | FFh |
| Flash Memory Density | | 37h:34h | 31:00 | 007F FFFFh | |
| (1-4-4) Fast Read Number of Wait states (Note3) | 0 0000b: Wait states (Dummy Clocks) not support | 38h | 04:00 | 0 0000b | 00h |
| (1-4-4) Fast Read Number of Mode Bits (Note4) | 000b: Mode Bits not support | | 07:05 | 000b | |
| (1-4-4) Fast Read Opcode | | 39h | 15:08 | FFh | FFh |
| (1-1-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3Ah | 20:16 | 0 0000b | 00h |
| (1-1-4) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (1-1-4) Fast Read Opcode | | 3Bh | 31:24 | FFh | FFh |

SFDP Table below is for MX25L8006EM1I-12G, MX25L8006EM2I-12G, MX25L8006EPI-12G, MX25L8006EZNI-12G and MX25L8006EZUI-12G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|---|---|---|---|---|---|
| (1-1-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3Ch | 04:00 | 0 1000b | 08h |
| (1-1-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 07:05 | 000b | |
| (1-1-2) Fast Read Opcode | | 3Dh | 15:08 | 3Bh | 3Bh |
| (1-2-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3Eh | 20:16 | 0 0000b | 00h |
| (1-2-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (1-2-2) Fast Read Opcode | | 3Fh | 31:24 | FFh | FFh |
| (2-2-2) Fast Read | 0=not support 1=support | 40h | 00 | 0b | EEh |
| Unused | | | 03:01 | 111b | |
| (4-4-4) Fast Read | 0=not support 1=support | | 04 | 0b | |
| Unused | | | 07:05 | 111b | |
| Unused | | 43h:41h | 31:08 | FFh | FFh |
| Unused | | 45h:44h | 15:00 | FFh | FFh |
| (2-2-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 46h | 20:16 | 0 0000b | 00h |
| (2-2-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (2-2-2) Fast Read Opcode | | 47h | 31:24 | FFh | FFh |
| Unused | | 49h:48h | 15:00 | FFh | FFh |
| (4-4-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 4Ah | 20:16 | 0 0000b | 00h |
| (4-4-4) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (4-4-4) Fast Read Opcode | | 4Bh | 31:24 | FFh | FFh |
| Sector Type 1 Size | Sector/block size = 2^N bytes (Note5)<br>0x00b: this sector type doesn't exist | 4Ch | 07:00 | 0Ch | 0Ch |
| Sector Type 1 erase Opcode | | 4Dh | 15:08 | 20h | 20h |
| Sector Type 2 Size | Sector/block size = 2^N bytes<br>0x00b: this sector type doesn't exist | 4Eh | 23:16 | 10h | 10h |
| Sector Type 2 erase Opcode | | 4Fh | 31:24 | D8h | D8h |
| Sector Type 3 Size | Sector/block size = 2^N bytes<br>0x00b: this sector type doesn't exist | 50h | 07:00 | 00h | 00h |
| Sector Type 3 erase Opcode | | 51h | 15:08 | FFh | FFh |
| Sector Type 4 Size | Sector/block size = 2^N bytes<br>0x00b: this sector type doesn't exist | 52h | 23:16 | 00h | 00h |
| Sector Type 4 erase Opcode | | 53h | 31:24 | FFh | FFh |


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**Table 11. Parameter Table (1): Macronix Flash Parameter Tables**

SFDP Table below is for MX25L8006EM1I-12G, MX25L8006EM2I-12G, MX25L8006EPI-12G, MX25L8006EZNI-12G and MX25L8006EZUI-12G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|---|---|---|---|---|---|
| Vcc Supply Maximum Voltage | 2000h=2.000V<br>2700h=2.700V<br>3600h=3.600V | 61h:60h | 07:00<br>15:08 | 00h<br>36h | 00h<br>36h |
| Vcc Supply Minimum Voltage | 1650h=1.650V, 1750h=1.750V<br>2250h=2.250V, 2350h=2.350V<br>2650h=2.650V, 2700h=2.700V | 63h:62h | 23:16<br>31:24 | 00h<br>27h | 00h<br>27h |
| H/W Reset# pin | 0=not support 1=support | 65h:64h | 00 | 0b | 4FF6h |
| H/W Hold# pin | 0=not support 1=support | | 01 | 1b | |
| Deep Power Down Mode | 0=not support 1=support | | 02 | 1b | |
| S/W Reset | 0=not support 1=support | | 03 | 0b | |
| S/W Reset Opcode | Reset Enable (66h) should be issued before Reset Opcode | | 11:04 | 1111 1111b (FFh) | |
| Program Suspend/Resume | 0=not support 1=support | | 12 | 0b | |
| Erase Suspend/Resume | 0=not support 1=support | | 13 | 0b | |
| Unused | | | 14 | 1b | |
| Wrap-Around Read mode | 0=not support 1=support | | 15 | 0b | |
| Wrap-Around Read mode Opcode | | 66h | 23:16 | FFh | FFh |
| Wrap-Around Read data length | 08h:support 8B wrap-around read<br>16h:8B&16B<br>32h:8B&16B&32B<br>64h:8B&16B&32B&64B | 67h | 31:24 | FFh | FFh |
| Individual block lock | 0=not support 1=support | 6Bh:68h | 00 | 0b | CFFEh |
| Individual block lock bit (Volatile/Nonvolatile) | 0=Volatile 1=Nonvolatile | | 01 | 1b | |
| Individual block lock Opcode | | | 09:02 | 1111 1111b (FFh) | |
| Individual block lock Volatile protect bit default protect status | 0=protect 1=unprotect | | 10 | 1b | |
| Secured OTP | 0=not support 1=support | | 11 | 1b | |
| Read Lock | 0=not support 1=support | | 12 | 0b | |
| Permanent Lock | 0=not support 1=support | | 13 | 0b | |
| Unused | | | 15:14 | 11b | |
| Unused | | | 31:16 | FFh | FFh |
| Unused | | 6Fh:6Ch | 31:00 | FFh | FFh |


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Note 1: h/b is hexadecimal or binary.

Note 2: **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

Note 3: **Wait States** is required dummy clock cycles after the address bits or optional mode bits.

Note 4: **Mode Bits** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg,read performance enhance toggling bits)

Note 5: 4KB=2^0Ch,32KB=2^0Fh,64KB=2^10h

Note 6: All unused and undefined area data is blank FFh for SFDP Tables that are defined in Parameter Identification Header. All other areas beyond defined SFDP Table are reserved by Macronix.

## POWER-ON STATE

The device is at the following states after power-up:
- Standby mode ( please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.
Please refer to *"Figure 31. Power-up Timing"*.

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended.(generally around 0.1uF)

## INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).


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## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

| RATING | | VALUE |
|---|---|---|
| Ambient Operating Temperature | Industrial grade | -40°C to 85°C |
| Storage Temperature | | -65°C to 150°C |
| Applied Input Voltage | | -0.5V to VCC+0.5V |
| Applied Output Voltage | | -0.5V to VCC+0.5V |
| VCC to Ground Potential | | -0.5V to 4.0V |

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see *"Figure 4. Maximum Negative Overshoot Waveform"* and *"Figure 5. Maximum Positive Overshoot Waveform"*.

**Figure 4. Maximum Negative Overshoot Waveform**

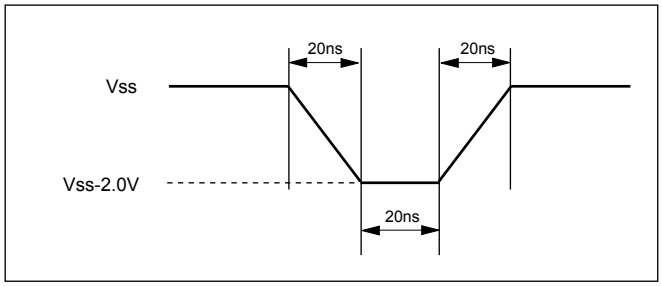
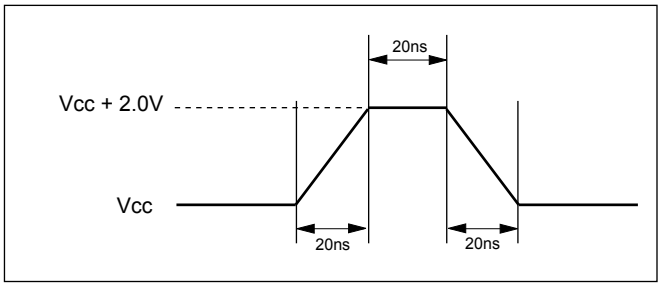



**Figure 5. Maximum Positive Overshoot Waveform**




### CAPACITANCE TA = 25°C, f = 1.0 MHz

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | | | 6 | pF | VIN = 0V |
| COUT | Output Capacitance | | | 8 | pF | VOUT = 0V |

**Figure 6. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL**

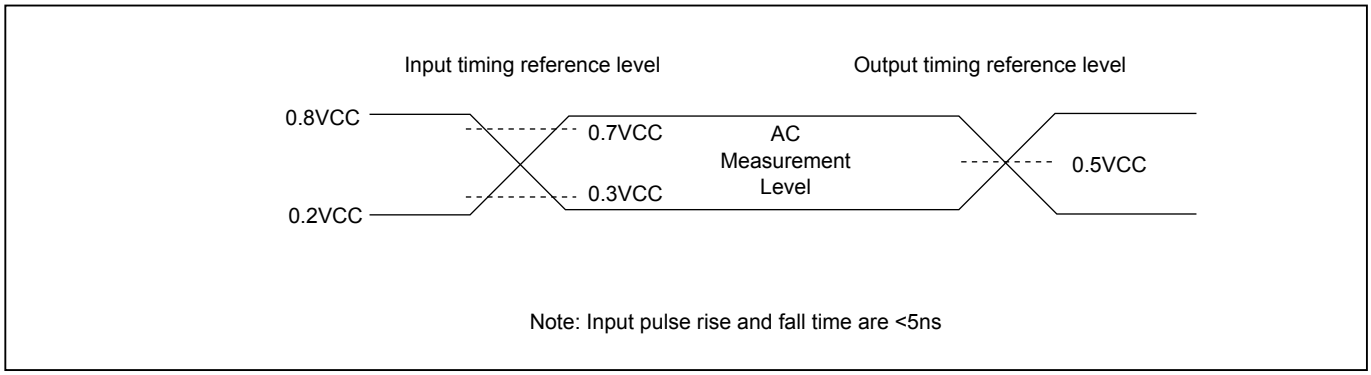



**Figure 7. OUTPUT LOADING**

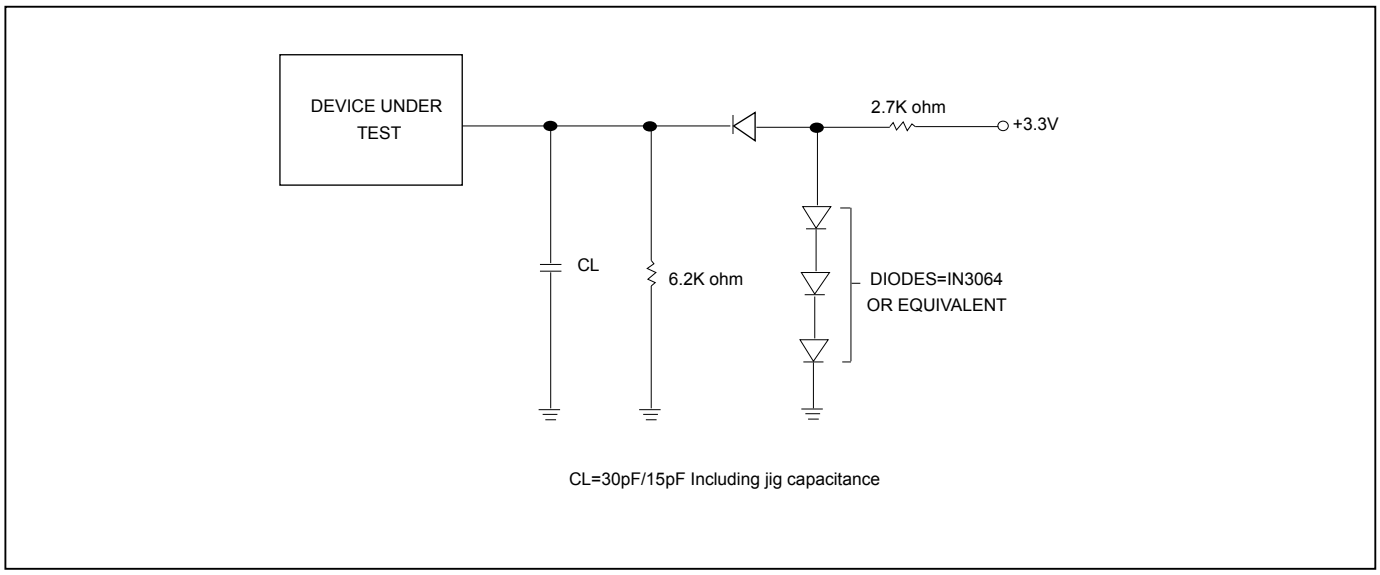



**Figure 8. SCLK TIMING DEFINITION**

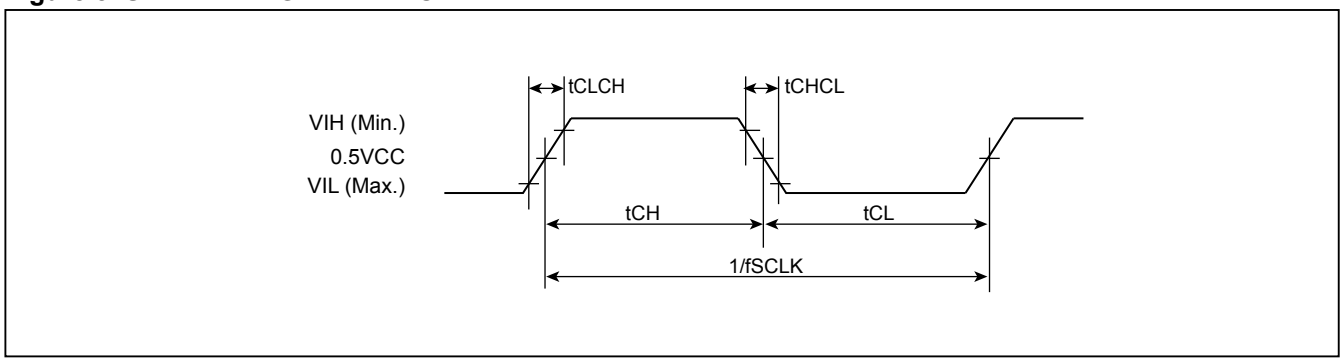


**Table 12. DC CHARACTERISTICS**

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| ILI | Input Load Current | 1 | | | ± 2 | uA | VCC = VCC Max, VIN = VCC or GND |
| ILO | Output Leakage Current | 1 | | | ± 2 | uA | VCC = VCC Max, VOUT = VCC or GND |
| ISB1 | VCC Standby Current | 1 | | 15 | 25 | uA | VIN = VCC or GND, CS# = VCC |
| ISB2 | Deep Power-down Current | | | 2 | 10 | uA | VIN = VCC or GND, CS# = VCC |
| ICC1 | VCC Read | 1 | | | 12 | mA | f=86MHz fT=80MHz (2 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open |
| | | 1 | | | 12 | mA | f=66MHz, SCLK=0.1VCC/0.9VCC, SO=Open |
| | | 1 | | | 4 | mA | f=33MHz, SCLK=0.1VCC/0.9VCC, SO=Open |
| ICC2 | VCC Program Current (PP) | 1 | | 15 | 20 | mA | Program in Progress, CS# =VCC |
| ICC3 | VCC Write Status Register (WRSR) Current | 1 | | 3 | 15 | mA | Program status register in progress, CS#=VCC |
| ICC4 | VCC Sector Erase Current (SE) | 1 | | 9 | 15 | mA | Erase in Progress, CS#=VCC |
| ICC5 | VCC Chip Erase Current (CE) | 1 | | 15 | 20 | mA | Erase in Progress, CS#=VCC |
| VIL | Input Low Voltage | | -0.5 | | 0.3VCC | V | |
| VIH | Input High Voltage | | 0.7VCC | | VCC+0.4 | V | |
| VOL | Output Low Voltage | | | | 0.4 | V | IOL = 1.6mA |
| VOH | Output High Voltage | | VCC-0.2 | | | V | IOH = -100uA |

Notes :
1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Not 100% tested.


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**Table 13. AC CHARACTERISTICS**

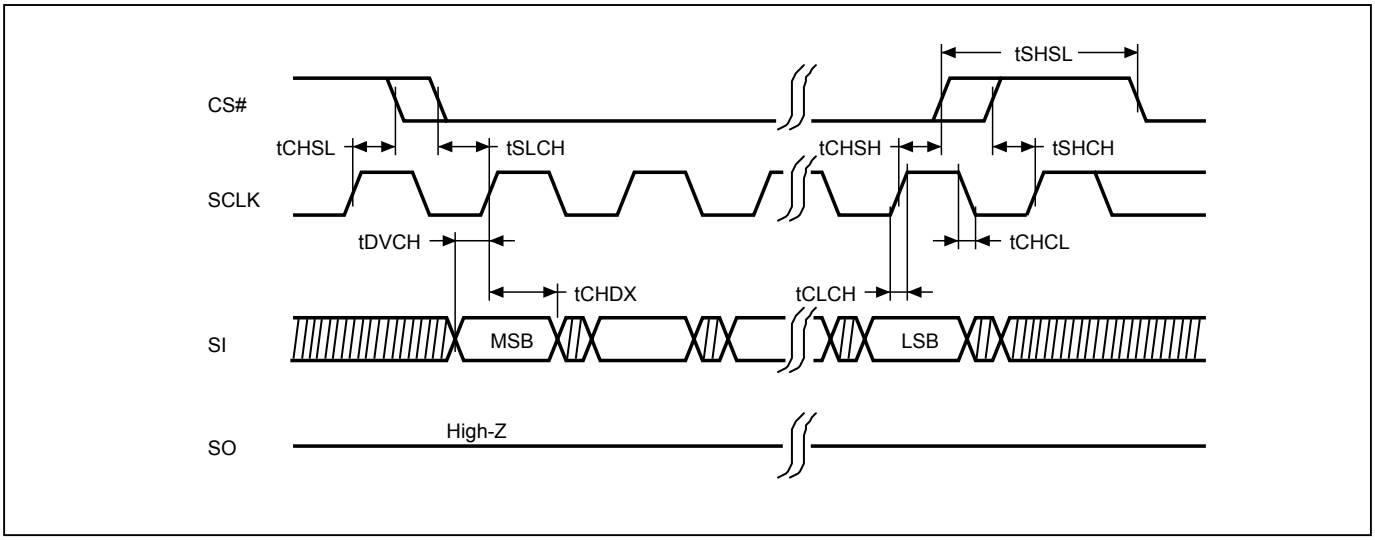
| Symbol | Alt. | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| fSCLK | fC | Clock Frequency for the following instructions: FAST_READ, RDSFDP, PP, SE, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR | | DC | | 86 | MHz |
| fRSCLK | fR | Clock Frequency for READ instructions | | DC | | 33 | MHz |
| fTSCLK | fT | Clock Frequency for DREAD instructions | | DC | | 80 | MHz |
| tCH(1) | tCLH | Clock High Time | fC=86MHz | 5.5 | | | ns |
| | | | fR=33MHz | 13 | | | ns |
| tCL(1) | tCLL | Clock Low Time | fC=86MHz | 5.5 | | | ns |
| | | | fR=33MHz | 13 | | | ns |
| tCLCH(2) | | Clock Rise Time (3) (peak to peak) | | 0.1 | | | V/ns |
| tCHCL(2) | | Clock Fall Time (3) (peak to peak) | | 0.1 | | | V/ns |
| tSLCH | tCSS | CS# Active Setup Time (relative to SCLK) | | 5 | | | ns |
| tCHSL | | CS# Not Active Hold Time (relative to SCLK) | | 5 | | | ns |
| tDVCH | tDSU | Data In Setup Time | | 2 | | | ns |
| tCHDX | tDH | Data In Hold Time | | 5 | | | ns |
| tCHSH | | CS# Active Hold Time (relative to SCLK) | | 5 | | | ns |
| tSHCH | | CS# Not Active Setup Time (relative to SCLK) | | 5 | | | ns |
| tSHSL | tCSH | CS# Deselect Time | Read | 15 | | | ns |
| | | | Write | 40 | | | ns |
| tSHQZ(2) | tDIS | Output Disable Time | | | | 6 | ns |
| tCLQV | tV | Clock Low to Output Valid, Loading 30pF/15pF | | | | 8/6 | ns |
| tCLQX | tHO | Output Hold Time | | 0 | | | ns |
| tHLCH | | HOLD# Setup Time (relative to SCLK) | | 5 | | | ns |
| tCHHH | | HOLD# Hold Time (relative to SCLK) | | 5 | | | ns |
| tHHCH | | HOLD Setup Time (relative to SCLK) | | 5 | | | ns |
| tCHHL | | HOLD Hold Time (relative to SCLK) | | 5 | | | ns |
| tHHQX(2) | tLZ | HOLD to Output Low-Z | | | | 6 | ns |
| tHLQZ(2) | tHZ | HOLD# to Output High-Z | | | | 6 | ns |
| tWHSL(4) | | Write Protect Setup Time | | 20 | | | ns |
| tSHWL (4) | | Write Protect Hold Time | | 100 | | | ns |
| tDP(2) | | CS# High to Deep Power-down Mode | | | | 10 | us |
| tRES1(2) | | CS# High to Standby Mode without Electronic Signature Read | | | | 8.8 | us |
| tRES2(2) | | CS# High to Standby Mode with Electronic Signature Read | | | | 8.8 | us |
| tW | | Write Status Register Cycle Time | | | 5 | 40 | ms |
| tBP | | Byte-Program | | | 9 | 50 | us |
| tPP | | Page Program Cycle Time | | | 0.6 | 3 | ms |
| tSE | | Sector Erase Cycle Time | | | 40 | 200 | ms |
| tBE | | Block Erase Cycle Time | | | 0.4 | 2 | s |
| tCE | | Chip Erase Cycle Time | | | 3.5 | 6 | s |

***Notes:***
1. tCH + tCL must be greater than or equal to 1/ fC. For Fast Read, tCL/tCH=5.5/5.5.
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
5. Test condition is shown as *"Figure 6. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL"* & *"Figure 7. OUTPUT LOADING"*.
6. The CS# rising time needs to follow tCLCH spec and CS# falling time needs to follow tCHCL spec.


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## Timing Analysis

### Figure 9. Serial Input Timing




### Figure 10. Output Timing

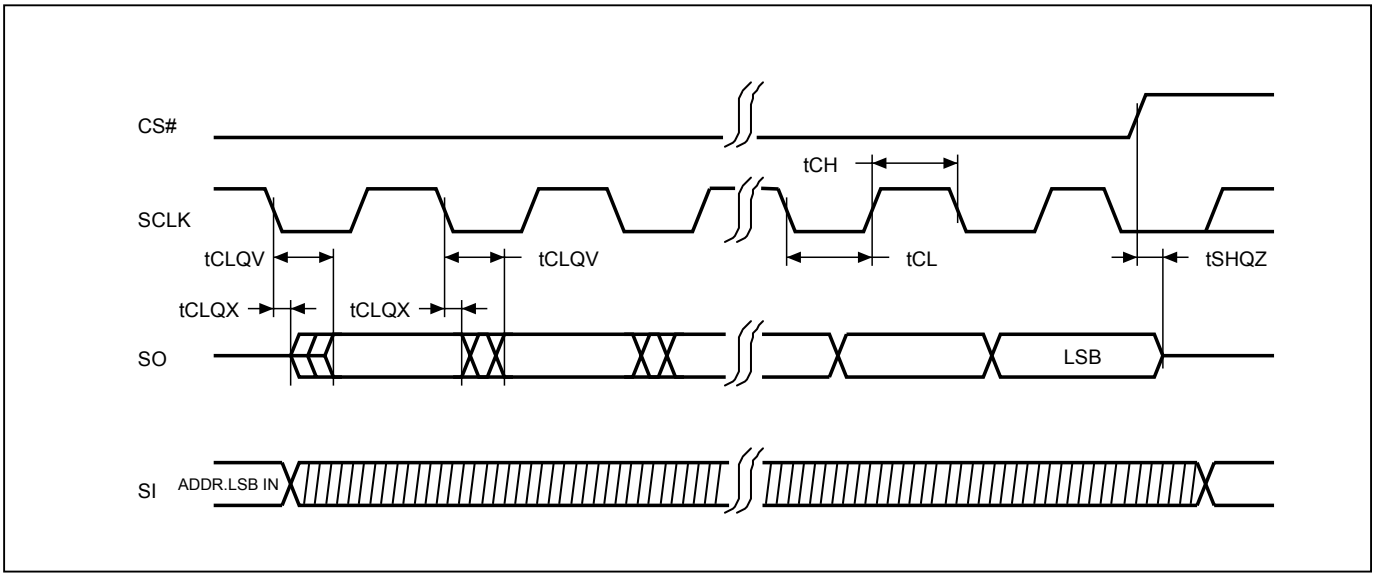
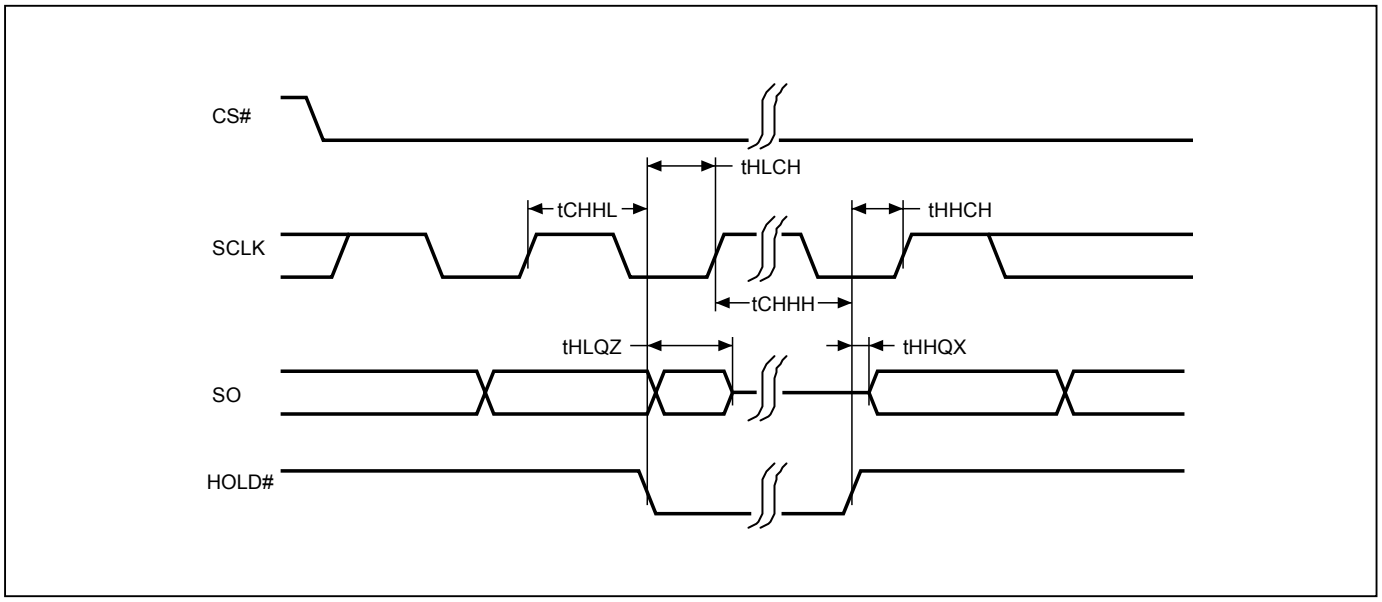


**Figure 11. Hold Timing**




* SI is "don't care" during HOLD operation.

**Figure 12. WP# Disable Setup and Hold Timing during WRSR when SRWD=1**

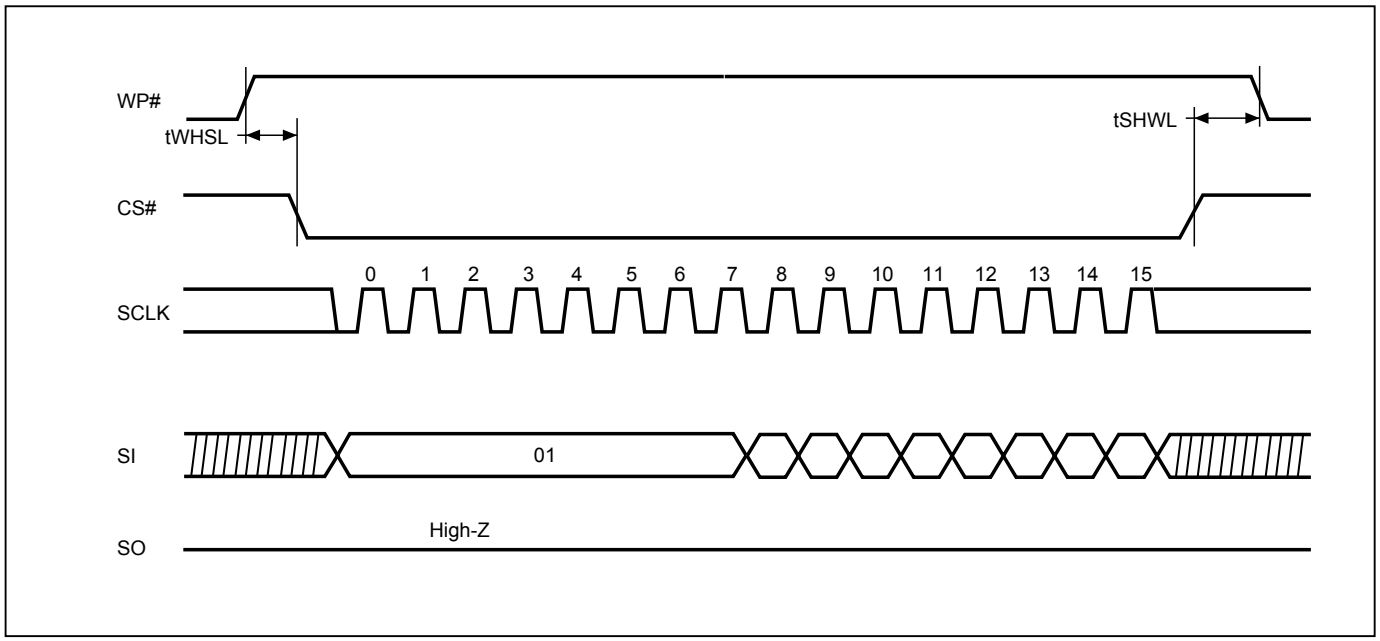


**Figure 13. Write Enable (WREN) Sequence (Command 06)**

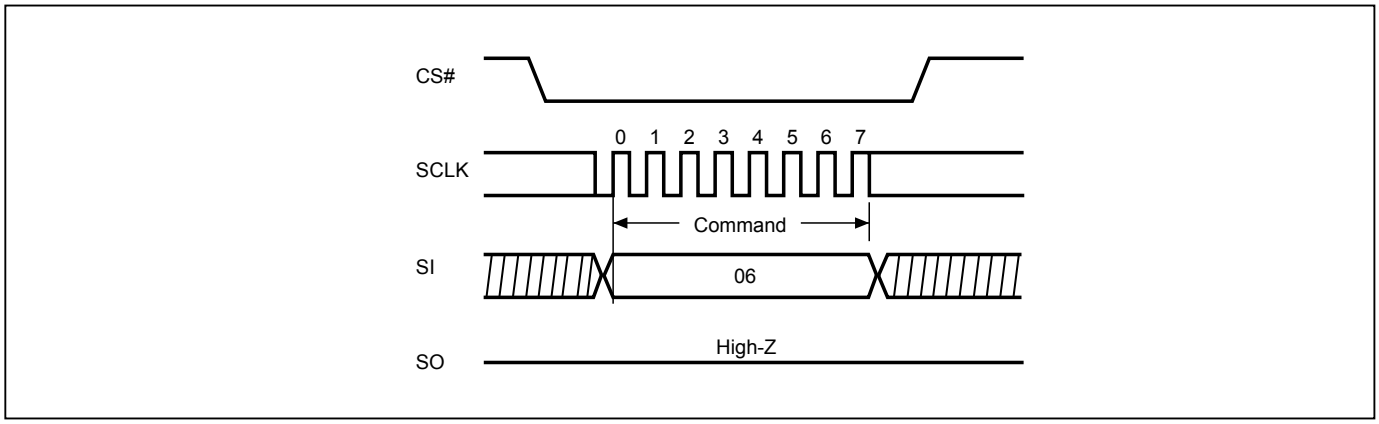



**Figure 14. Write Disable (WRDI) Sequence (Command 04)**

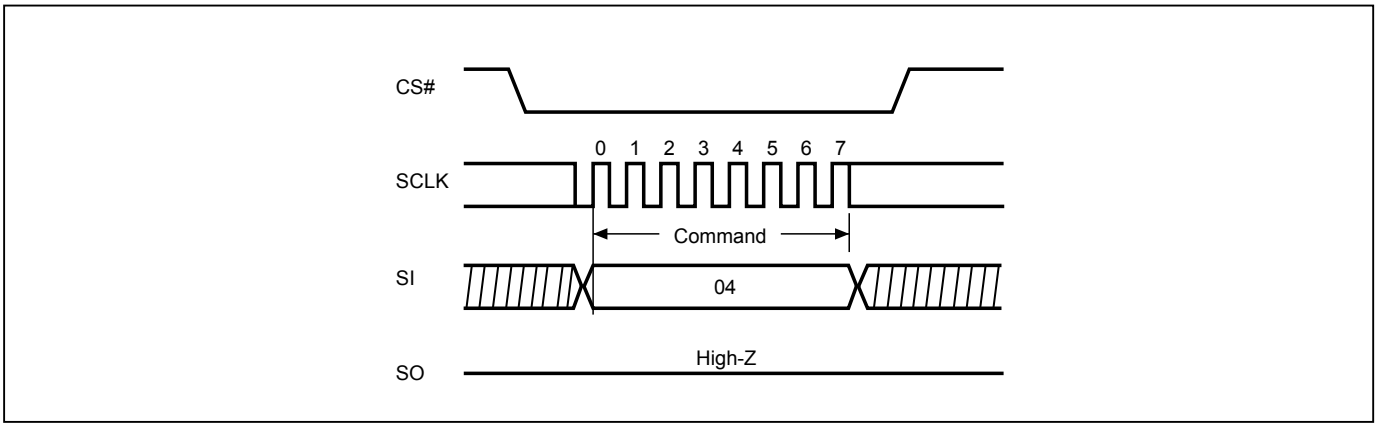


**Figure 15. Read Status Register (RDSR) Sequence (Command 05)**

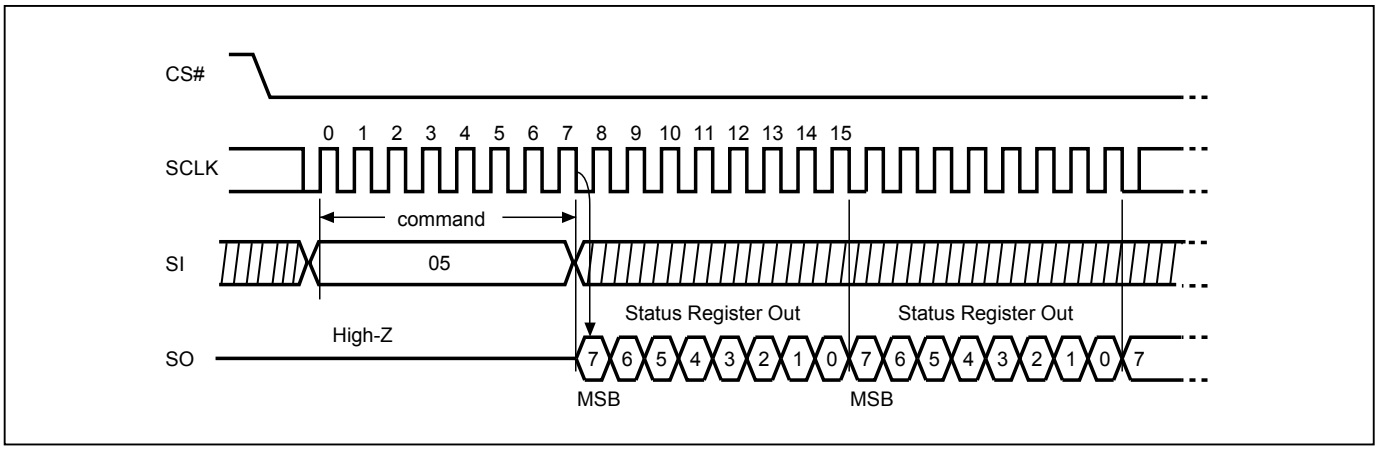



**Figure 16. Write Status Register (WRSR) Sequence (Command 01)**

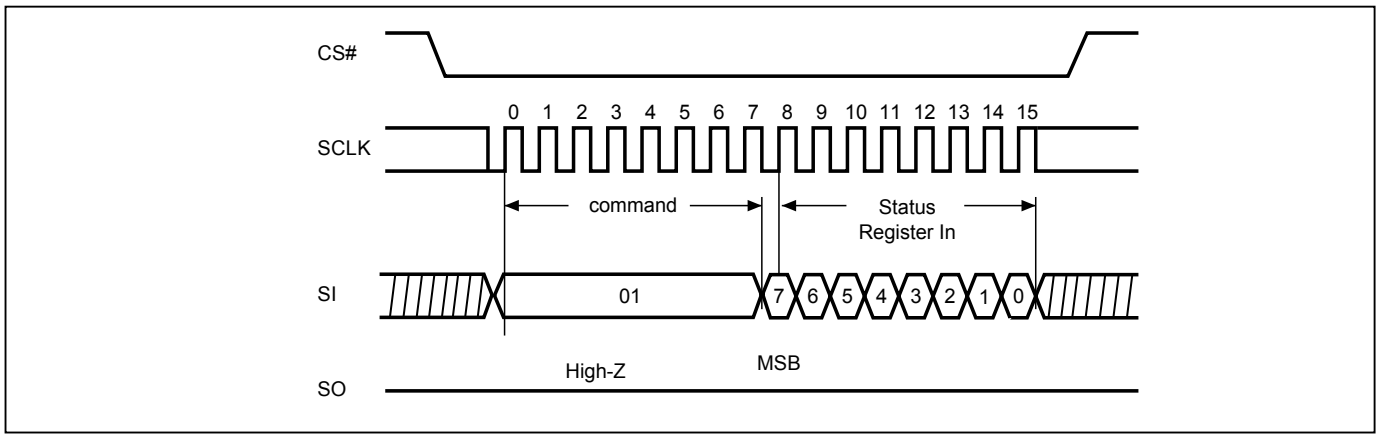



**Figure 17. Read Data Bytes (READ) Sequence (Command 03)**

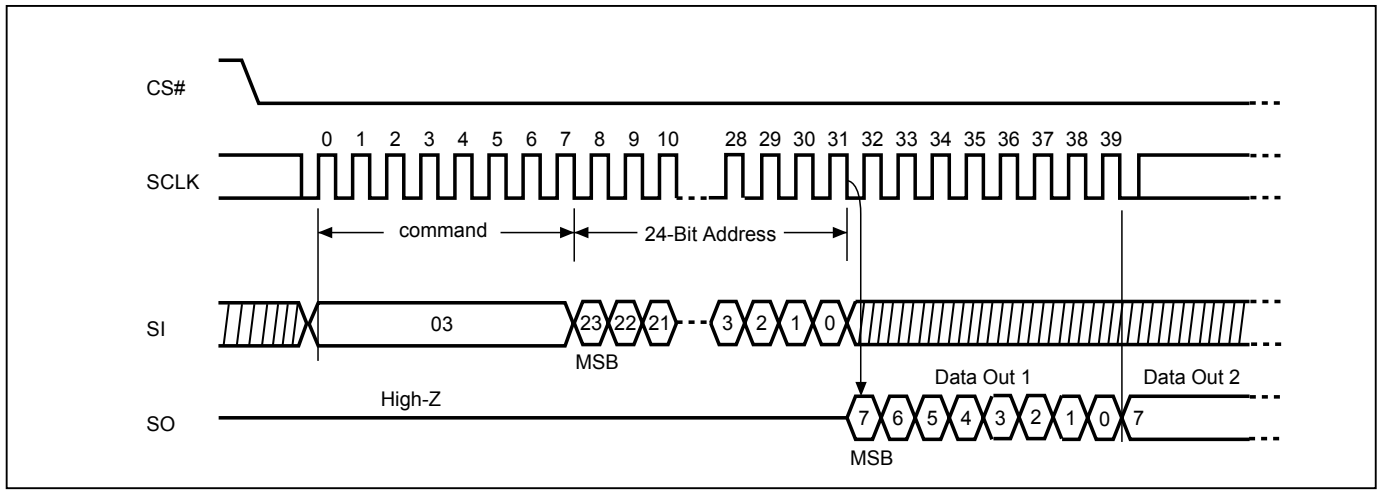


**Figure 18. Read at Higher Speed (FAST_READ) Sequence (Command 0B)**

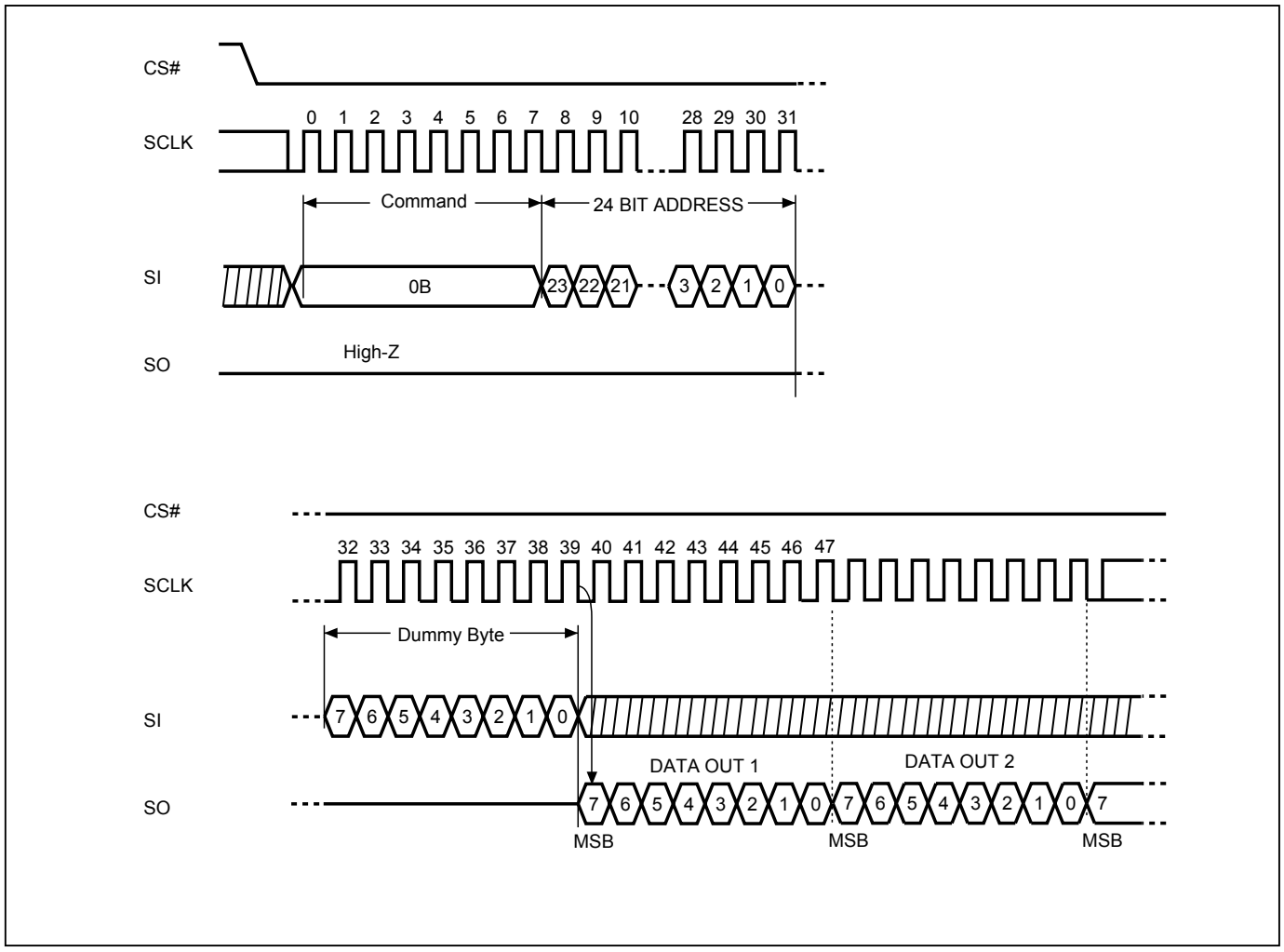


**Figure 19. Dual Output Read Mode Sequence (Command 3B)**

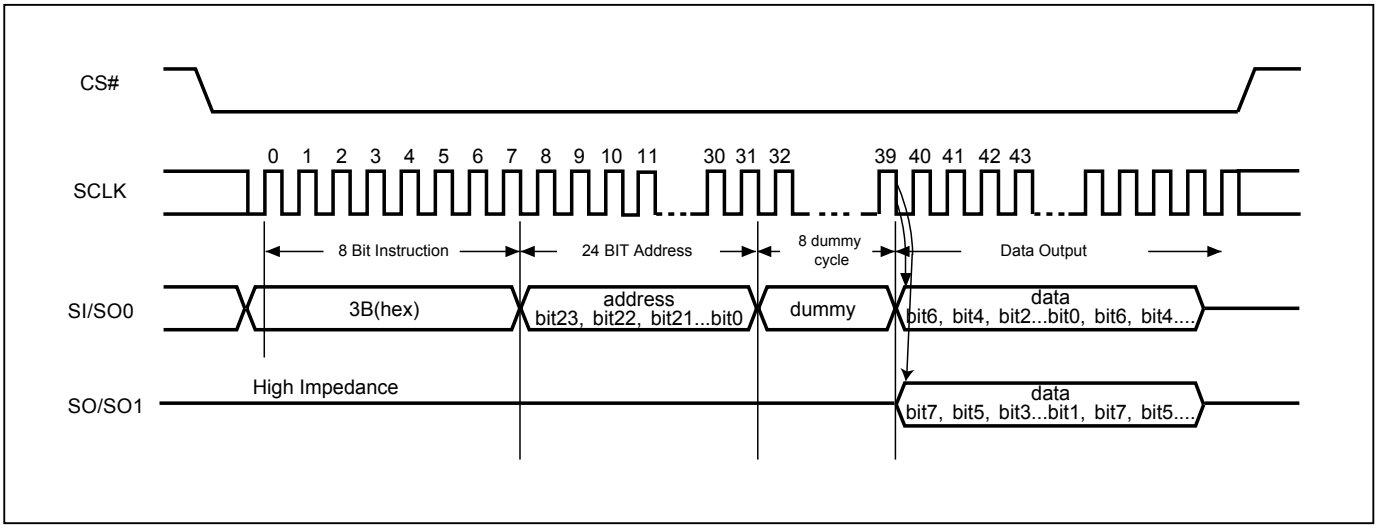
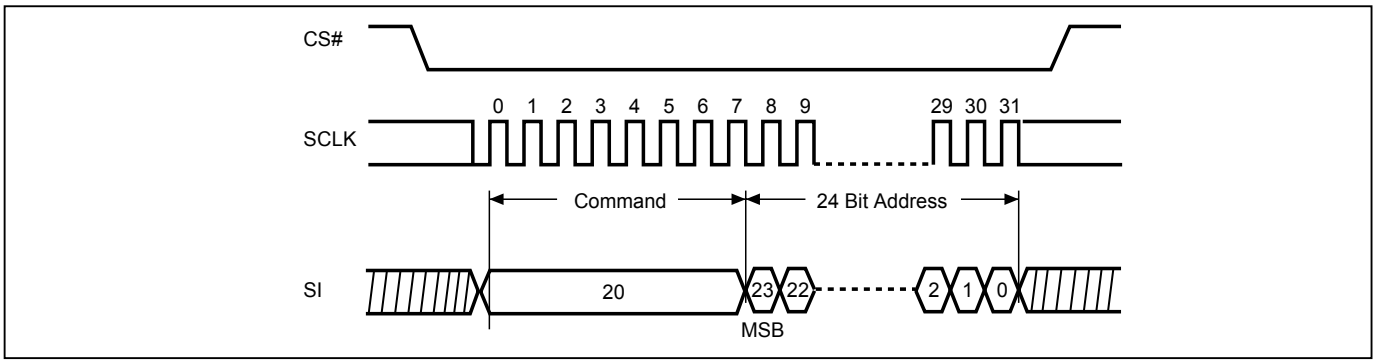
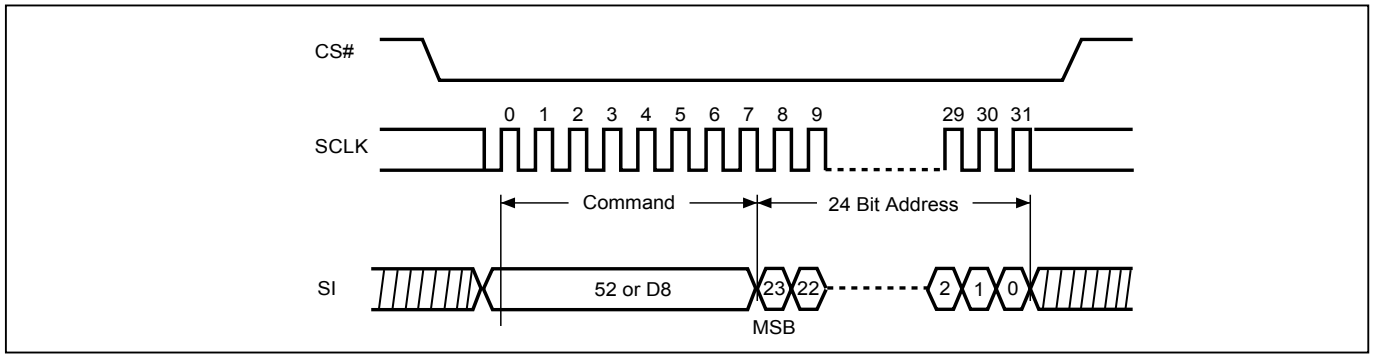



**Figure 20. Sector Erase (SE) Sequence (Command 20)**



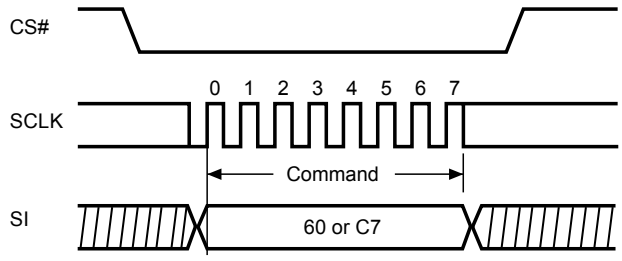

Note: SE command is 20(hex).

**Figure 21. Block Erase (BE) Sequence (Command 52 or D8)**




Note: BE command is 52 or D8(hex).

**Figure 22. Chip Erase (CE) Sequence (Command 60 or C7)**




Note: CE command is 60(hex) or C7(hex).

**Figure 23. Page Program (PP) Sequence (Command 02)**

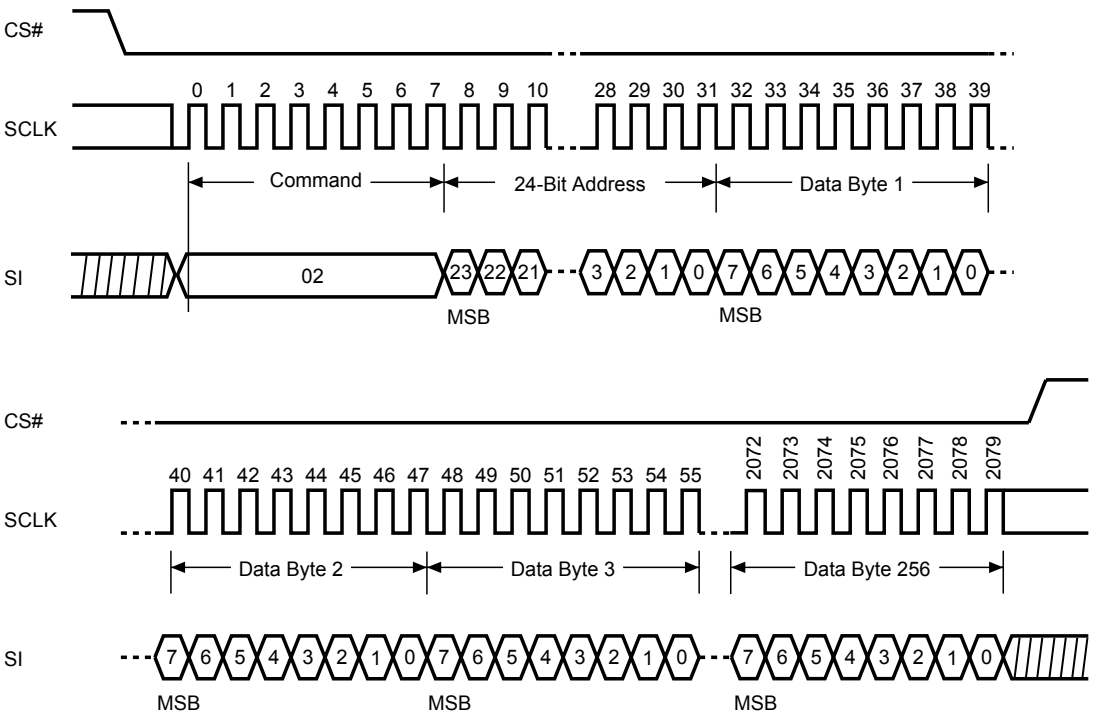


**Figure 24. Deep Power-down (DP) Sequence (Command B9)**

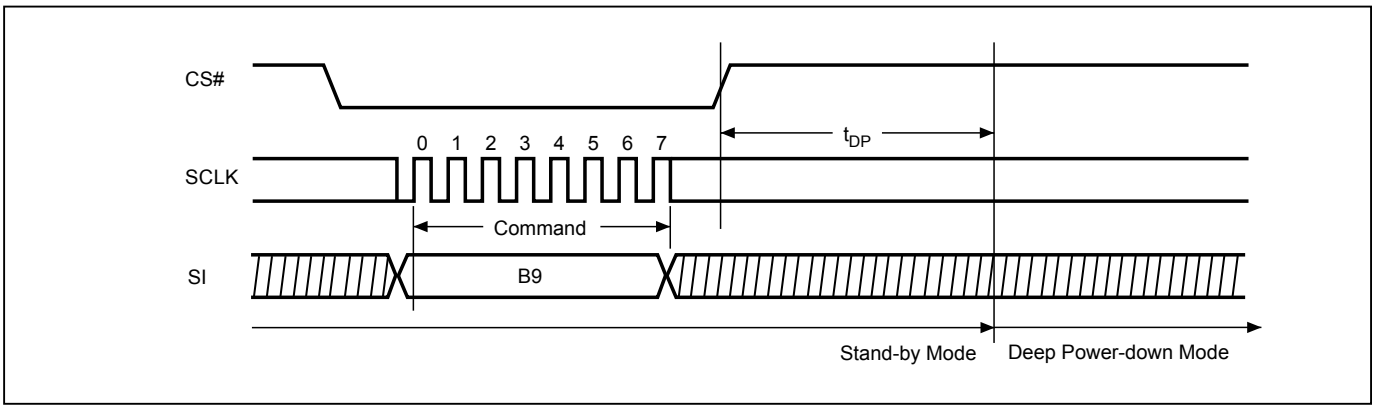



**Figure 25. Release from Deep Power-down (RDP) Sequence (Command AB)**

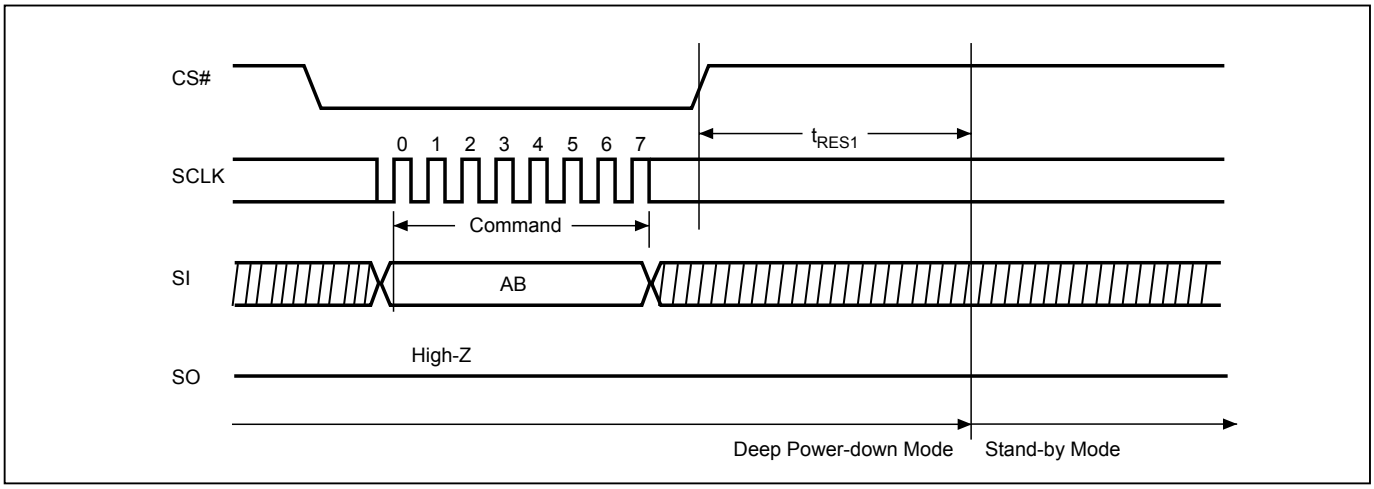



**Figure 26. Read Electronic Signature (RES) Sequence (Command AB)**

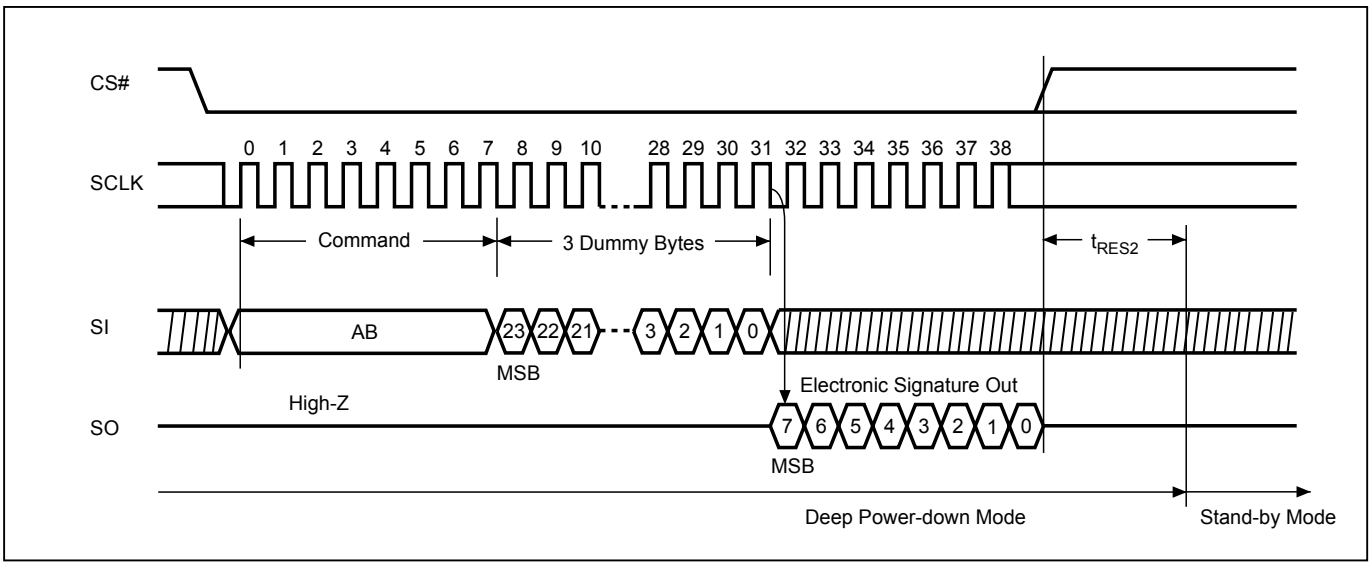


**Figure 27. Read Identification (RDID) Sequence (Command 9F)**

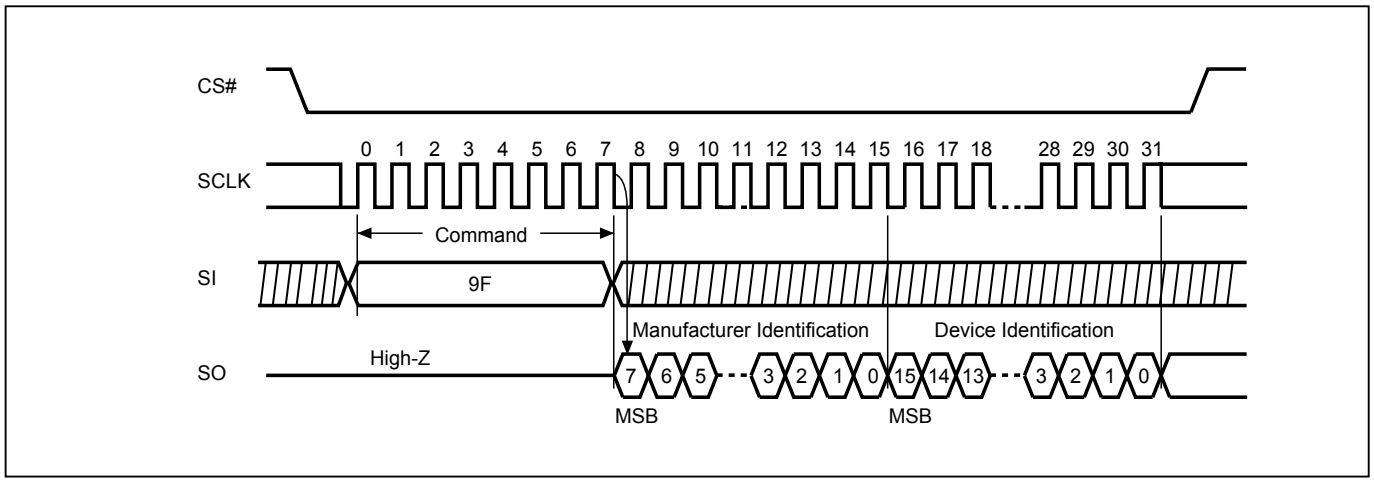
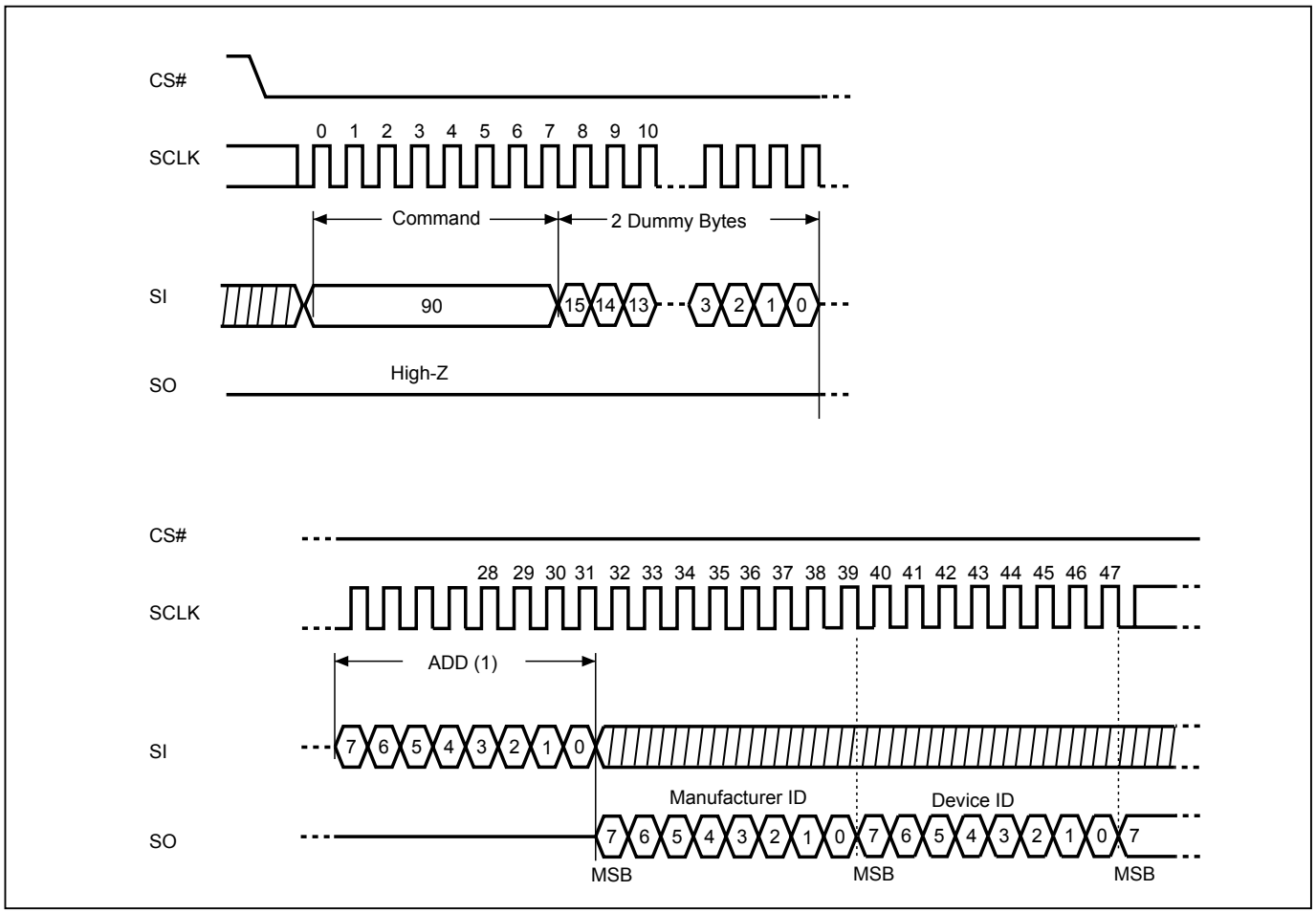



**Figure 28. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)**




***Notes:***

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first

(2) Instruction is either 90(hex).

**Figure 29. Read Security Register (RDSCUR) Sequence (Command 2B)**

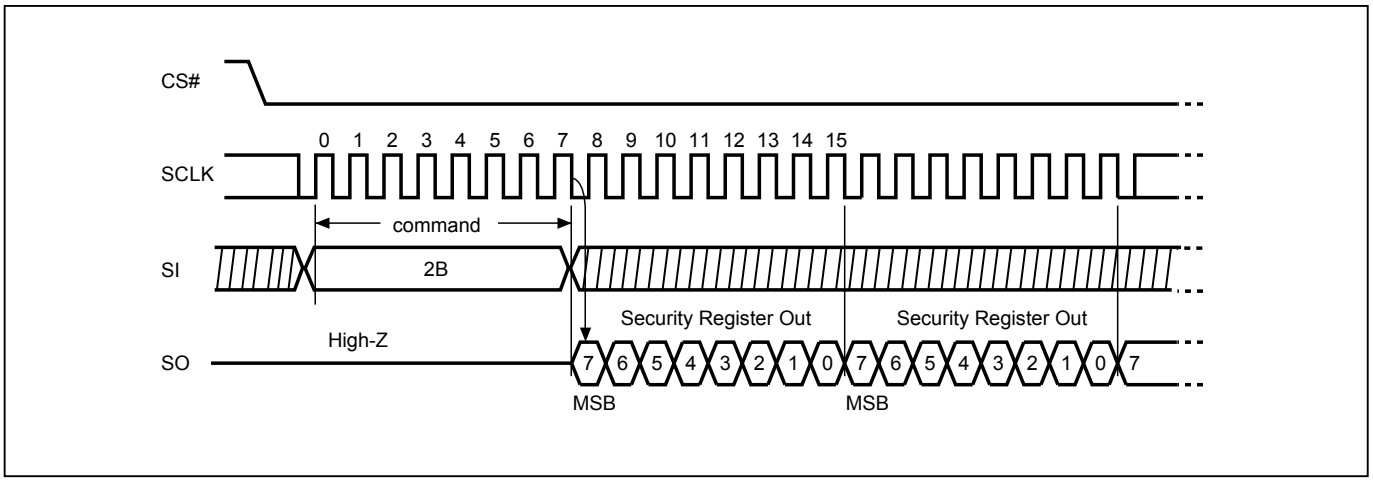



**Figure 30. Write Security Register (WRSCUR) Sequence (Command 2F)**

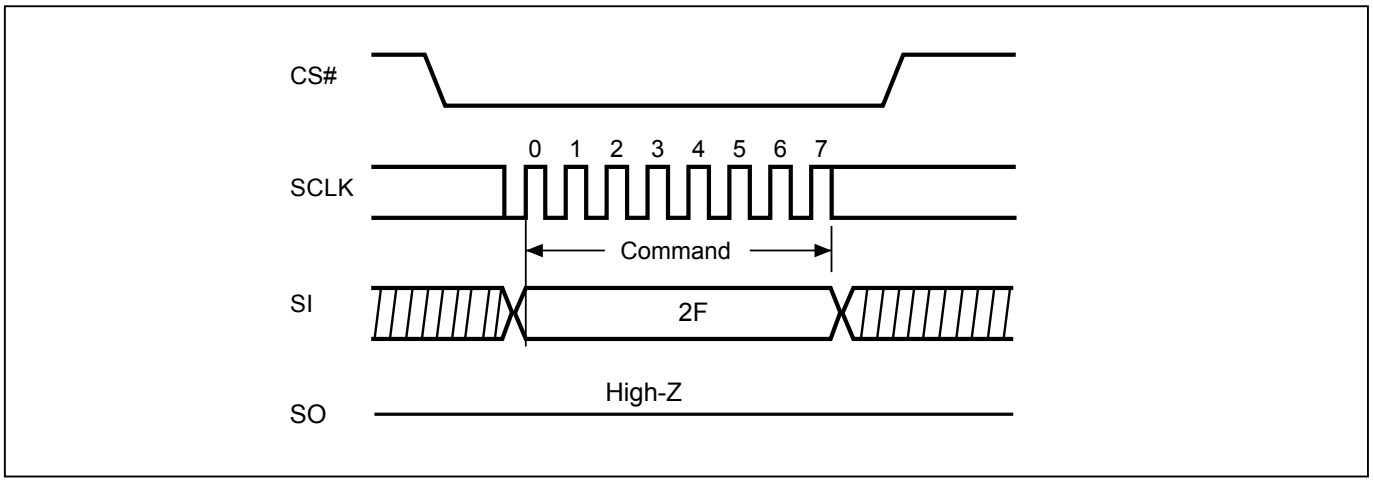
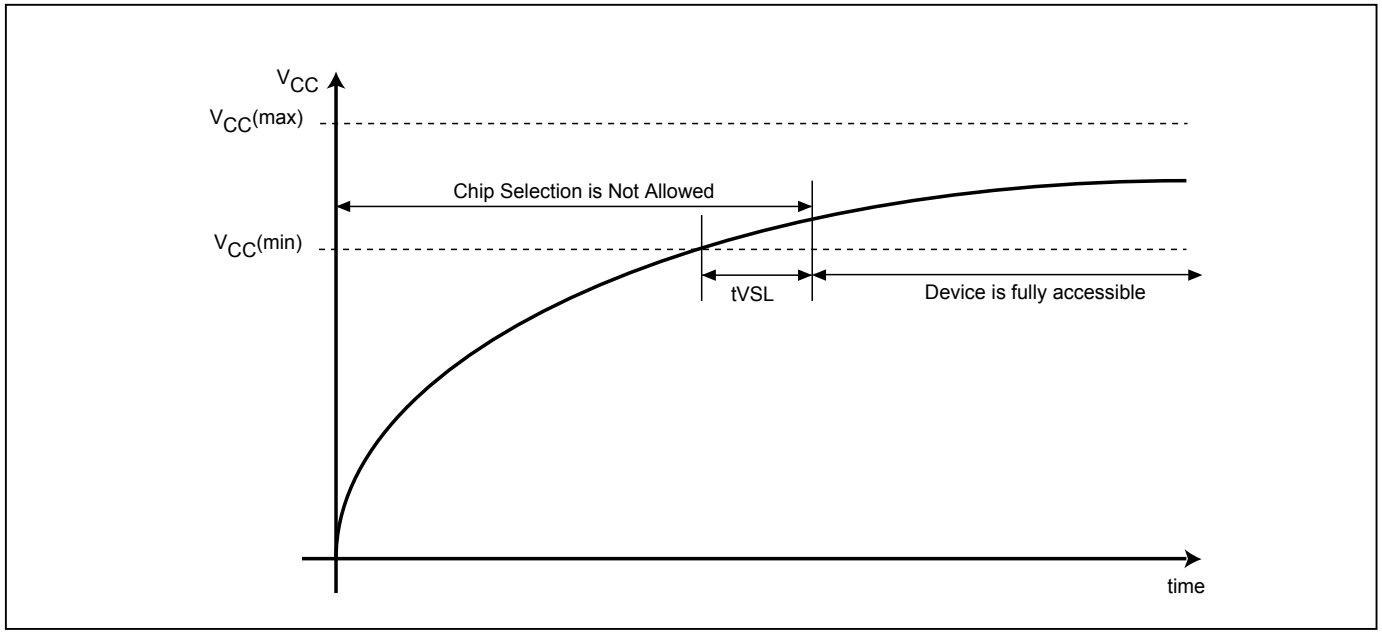


**Figure 31. Power-up Timing**




Note: VCC (max.) is 3.6V and VCC (min.) is 2.7V.

**Table 14. Power-Up Timing**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tVSL*(1)* | VCC(min) to CS# low | 200 | | us |

Note: 1. The parameter is characterized only.

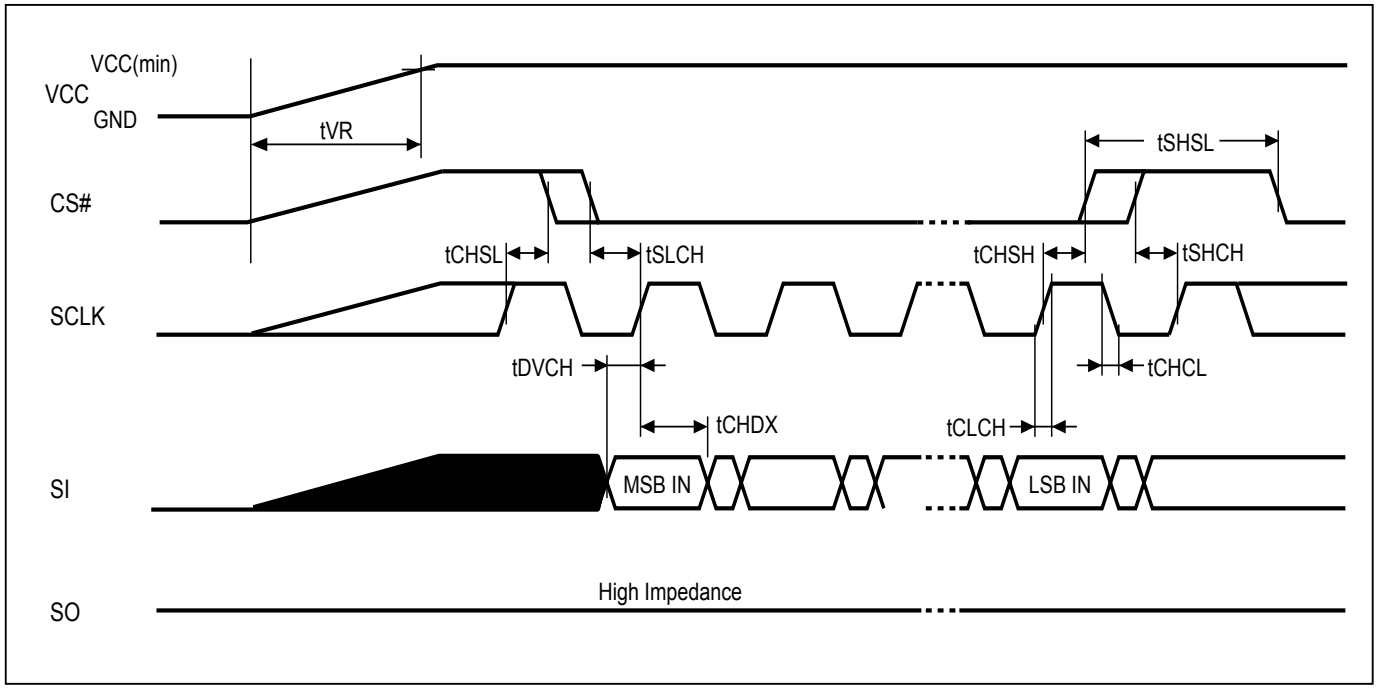
## OPERATING CONDITIONS

### At Device Power-Up and Power-Down

AC timing illustrated in *"Figure 32. AC Timing at Device Power-Up"* and *"Figure 33. Power-Down Sequence"* are the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power down, CS# need to follow the voltage applied on VCC to keep the device not be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

**Figure 32. AC Timing at Device Power-Up**

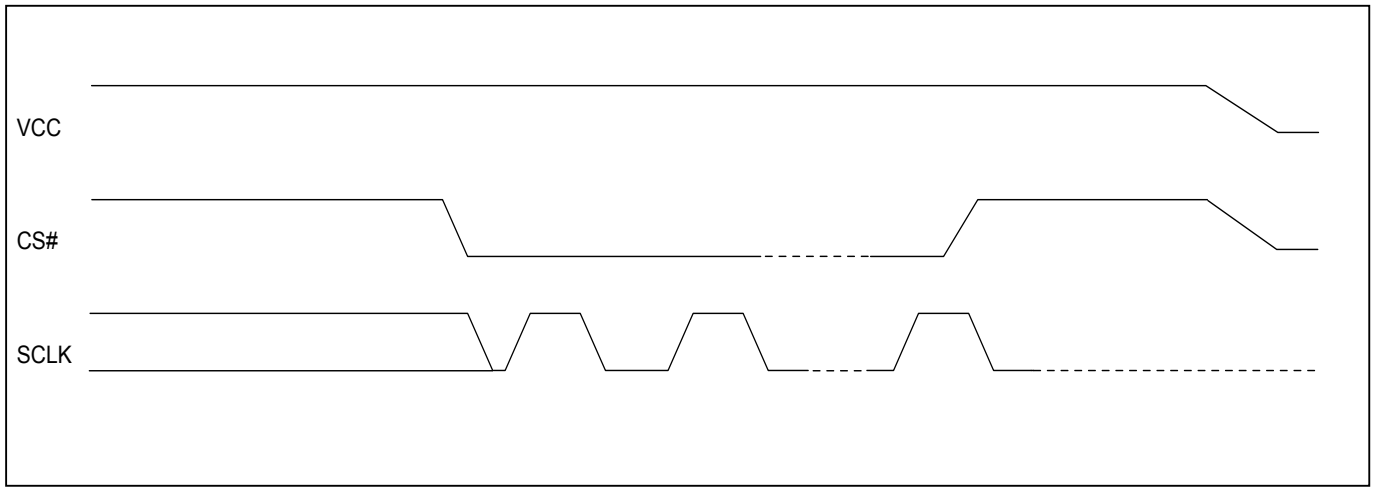



| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| tVR | VCC Rise Time | 1 | | 500000 | us/V |

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *"Table 13. AC CHARACTERISTICS".*

**Figure 33. Power-Down Sequence**

During power down, CS# need to follow the voltage drop on VCC to avoid mis-operation.



## ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Min. | Typ. (1) | Max. (2) | Unit |
|---|---|---|---|---|
| Write Status Register Time | | 5 | 40 | ms |
| Sector Erase Time | | 40 | 200 | ms |
| Block Erase Time | | 0.4 | 2 | s |
| Chip Erase Time | | 3.5 | 6 | s |
| Byte Program Time (via page program command) | | 9 | 50 | us |
| Page Program Time | | 0.6 | 3 | ms |
| Erase/Program Cycle | | 100,000 | | cycles |

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checkerboard pattern.
2. Under worst conditions of 85°C and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. Erase/Program cycles comply with JEDEC: JESD-47 & JESD22-A117 standard.

## DATA RETENTION

| Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|
| Data retention | 55˚C | 20 | | years |

## LATCH-UP CHARACTERISTICS

| | Min. | Max. |
|---|---|---|
| Input Voltage with respect to GND on all power pins, SI, CS# | -1.0V | 2 VCCmax |
| Input Voltage with respect to GND on SO | -1.0V | VCC + 1.0V |
| Current | -100mA | +100mA |
| Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time. | | |


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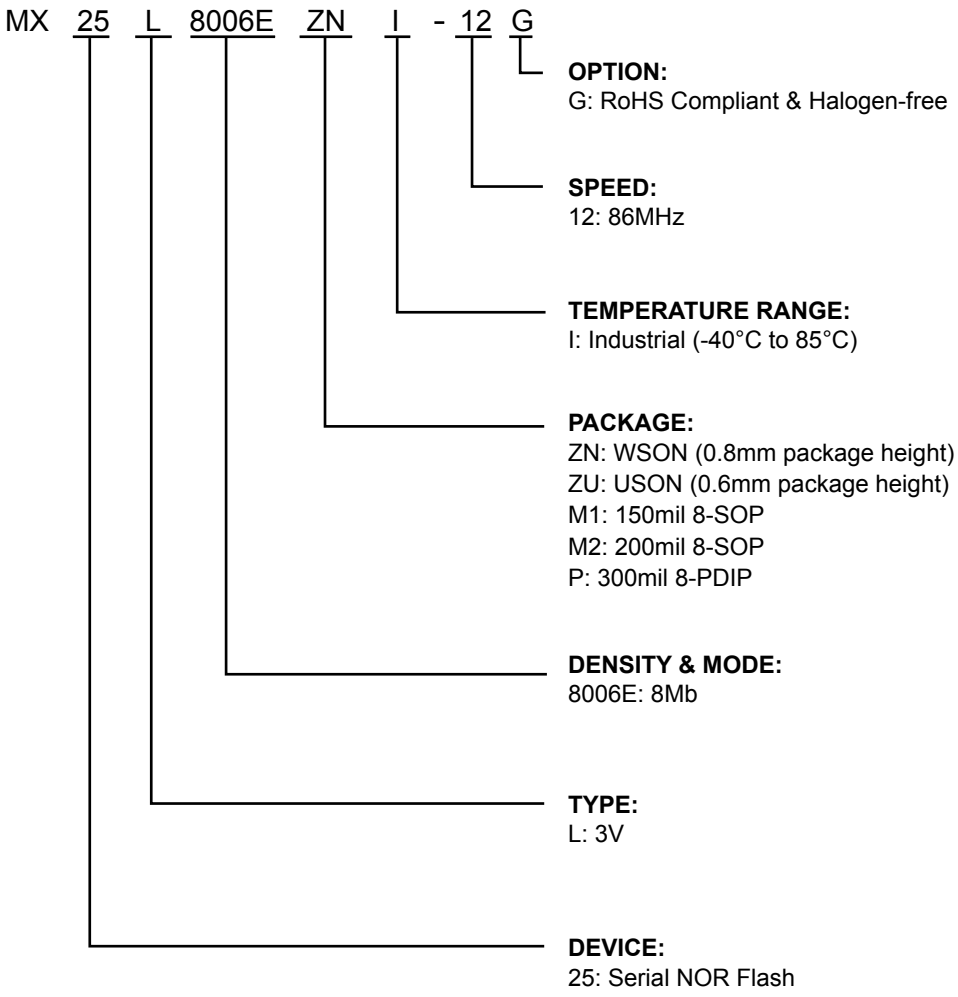
## ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

| PART NO. | CLOCK (MHz) | OPERATING CURRENT MAX. (mA) | STANDBY CURRENT MAX. (uA) | Temperature | Package | Remark |
|---|---|---|---|---|---|---|
| MX25L8006EM1I-12G | 86 | 12 | 25 | -40°C to 85°C | 8-SOP (150mil) | RoHS Compliant |
| MX25L8006EM2I-12G | 86 | 12 | 25 | -40°C to 85°C | 8-SOP (200mil) | RoHS Compliant |
| MX25L8006EPI-12G | 86 | 12 | 25 | -40°C to 85°C | 8-PDIP (300mil) | RoHS Compliant |
| MX25L8006EZNI-12G | 86 | 12 | 25 | -40°C to 85°C | 8-WSON (6x5mm) | RoHS Compliant |
| MX25L8006EZUI-12G | 86 | 12 | 25 | -40°C to 85°C | 8-USON (4x4mm) | RoHS Compliant |


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## PART NAME DESCRIPTION

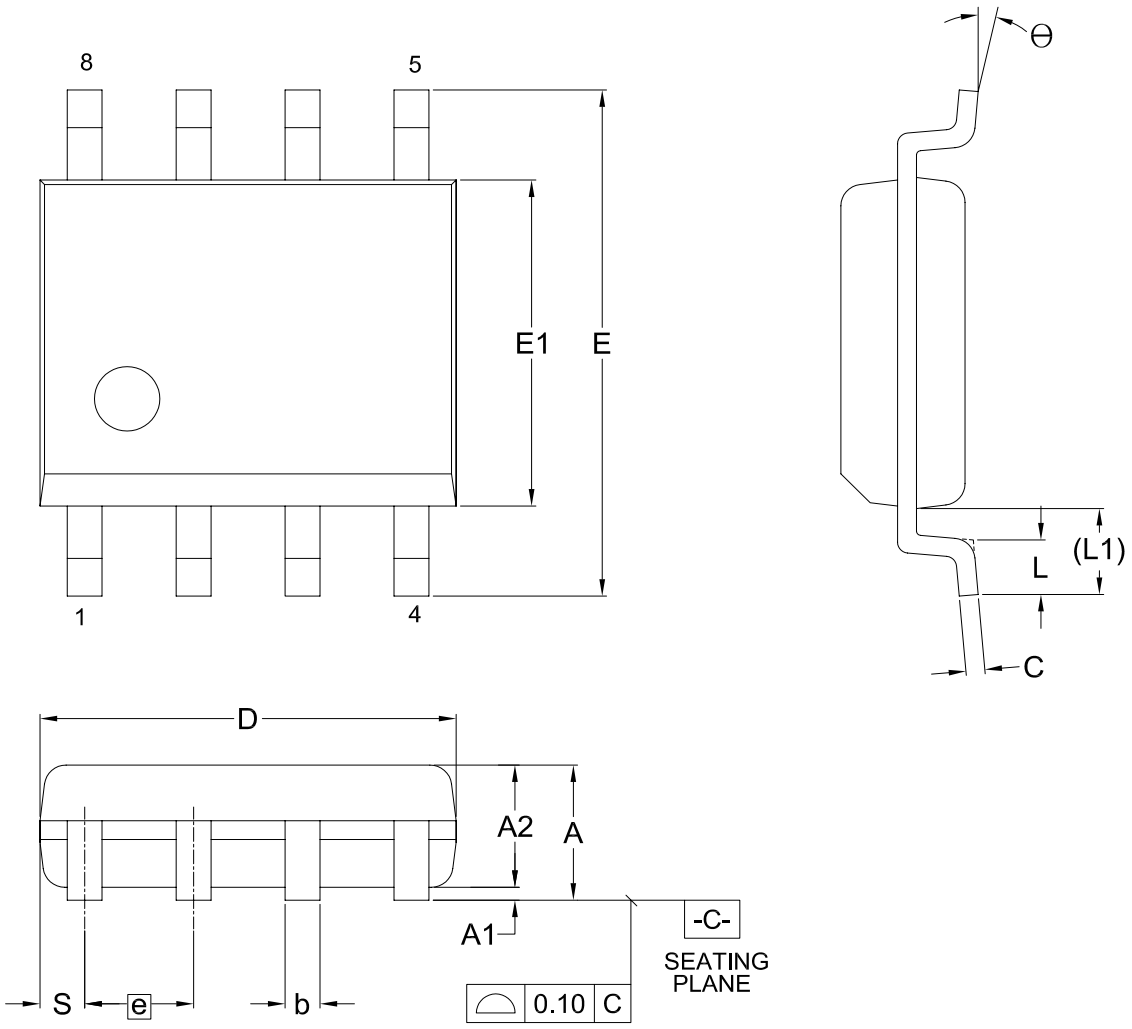




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## PACKAGE INFORMATION

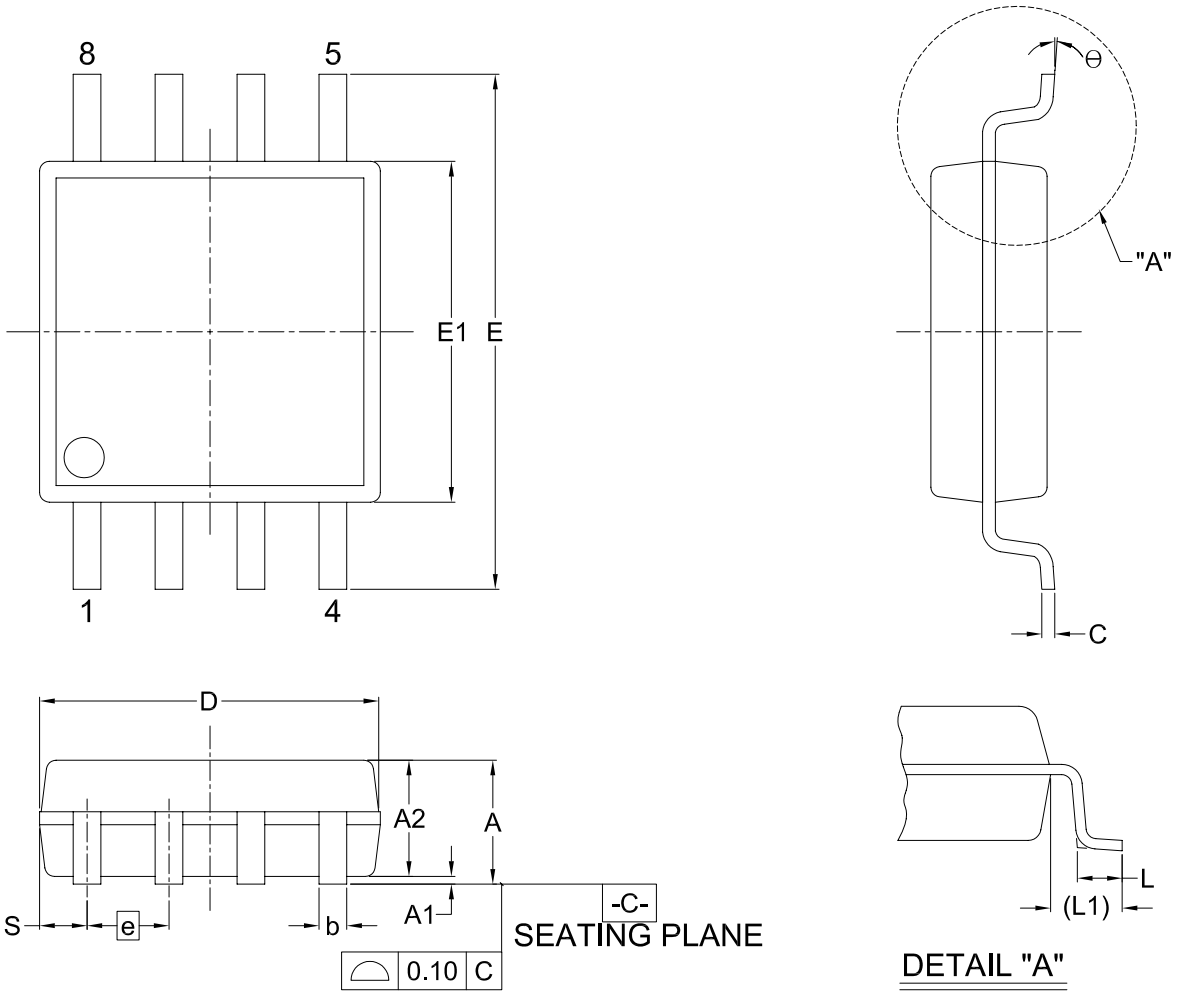
Doe. Title: Package Outline for SOP 8L (150MIL)




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | E | E1 | e | L | L1 | S | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.10 | 1.35 | 0.36 | 0.15 | 4.77 | 5.80 | 3.80 | — | 0.46 | 0.85 | 0.41 | 0° |
| | Nom. | — | 0.15 | 1.45 | 0.41 | 0.20 | 4.90 | 5.99 | 3.90 | 1.27 | 0.66 | 1.05 | 0.54 | 5° |
| | Max. | 1.75 | 0.20 | 1.55 | 0.51 | 0.25 | 5.03 | 6.20 | 4.00 | — | 0.86 | 1.25 | 0.67 | 8° |
| Inch | Min. | — | 0.004 | 0.053 | 0.014 | 0.006 | 0.188 | 0.228 | 0.150 | — | 0.018 | 0.033 | 0.016 | 0° |
| | Nom. | --- | 0.006 | 0.057 | 0.016 | 0.008 | 0.193 | 0.236 | 0.154 | 0.050 | 0.026 | 0.041 | 0.021 | 5° |
| | Max. | 0.069 | 0.008 | 0.061 | 0.020 | 0.010 | 0.198 | 0.244 | 0.158 | — | 0.034 | 0.049 | 0.026 | 8° |

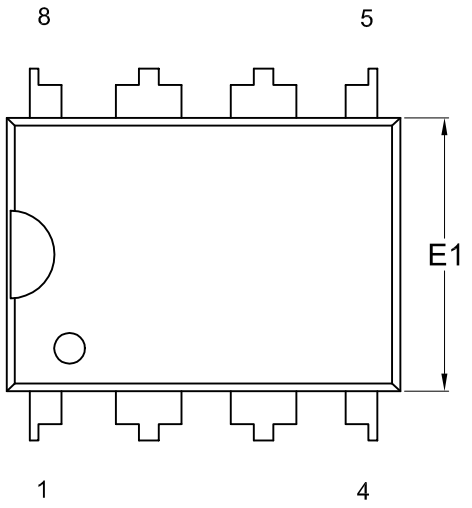
Doc. Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)

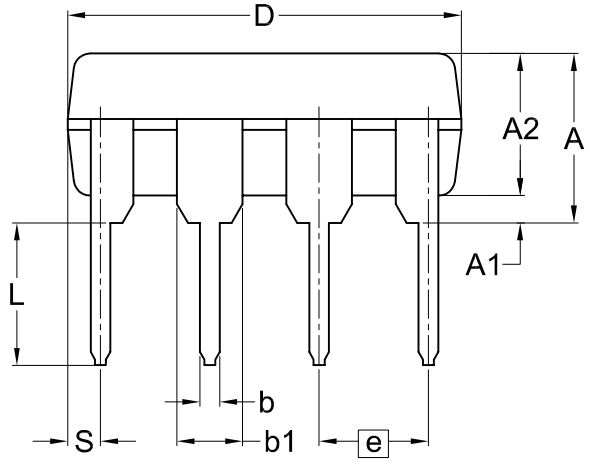


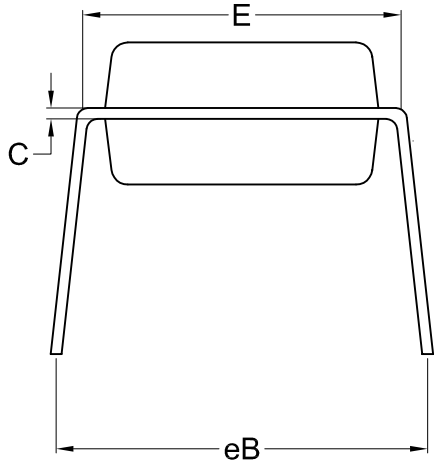

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | E | E1 | e | L | L1 | S | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 1.75 | 0.05 | 1.70 | 0.36 | 0.19 | 5.13 | 7.70 | 5.18 | --- | 0.50 | 1.21 | 0.62 | 0° |
| | Nom. | 1.95 | 0.15 | 1.80 | 0.41 | 0.20 | 5.23 | 7.90 | 5.28 | 1.27 | 0.65 | 1.31 | 0.74 | 5° |
| | Max. | 2.16 | 0.20 | 1.91 | 0.51 | 0.25 | 5.33 | 8.10 | 5.38 | --- | 0.80 | 1.41 | 0.88 | 8° |
| Inch | Min. | 0.069 | 0.002 | 0.067 | 0.014 | 0.007 | 0.202 | 0.303 | 0.204 | --- | 0.020 | 0.048 | 0.024 | 0° |
| | Nom. | 0.077 | 0.006 | 0.071 | 0.016 | 0.008 | 0.206 | 0.311 | 0.208 | 0.050 | 0.026 | 0.052 | 0.029 | 5° |
| | Max. | 0.085 | 0.008 | 0.075 | 0.020 | 0.010 | 0.210 | 0.319 | 0.212 | --- | 0.031 | 0.056 | 0.035 | 8° |

Doc. Title: Package Outline for PDIP 8L (300MIL)



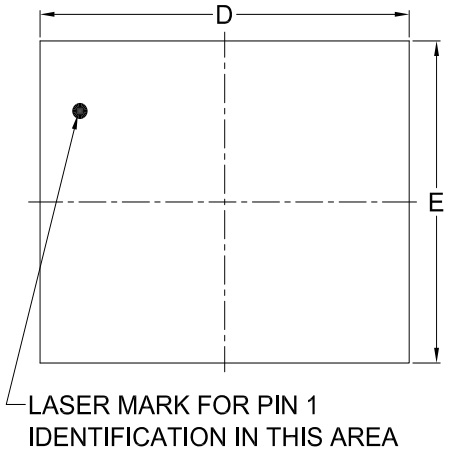



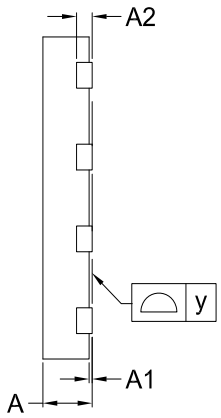

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | b1 | C | D | E | E1 | e | eB | L | S |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | — | 0.38 | 3.18 | 0.36 | 1.14 | 0.20 | 9.02 | 7.62 | 6.22 | --- | 7.87 | 2.92 | 0.76 |
| | Nom. | — | — | 3.30 | 0.46 | 1.52 | 0.25 | 9.27 | 7.87 | 6.35 | 2.54 | 8.89 | 3.30 | 1.14 |
| | Max. | 5.33 | — | 3.43 | 0.56 | 1.78 | 0.36 | 10.16 | 8.13 | 6.48 | --- | 9.53 | 3.81 | 1.52 |
| Inch | Min. | --- | 0.015 | 0.125 | 0.014 | 0.045 | 0.008 | 0.355 | 0.300 | 0.245 | --- | 0.310 | 0.115 | 0.030 |
| | Nom. | --- | — | 0.130 | 0.018 | 0.060 | 0.010 | 0.365 | 0.310 | 0.250 | 0.100 | 0.350 | 0.130 | 0.045 |
| | Max. | 0.210 | — | 0.135 | 0.022 | 0.070 | 0.014 | 0.400 | 0.320 | 0.255 | --- | 0.375 | 0.150 | 0.060 |

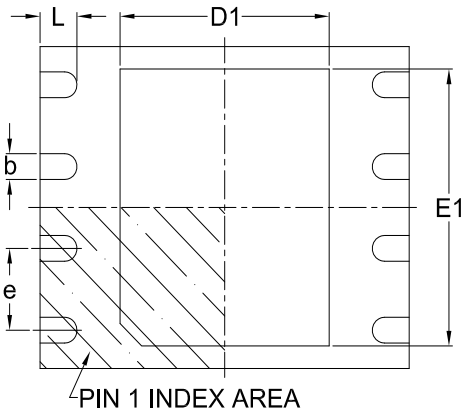
**Doc. Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)**




TOP VIEW




SIDE VIEW




BOTTOM VIEW

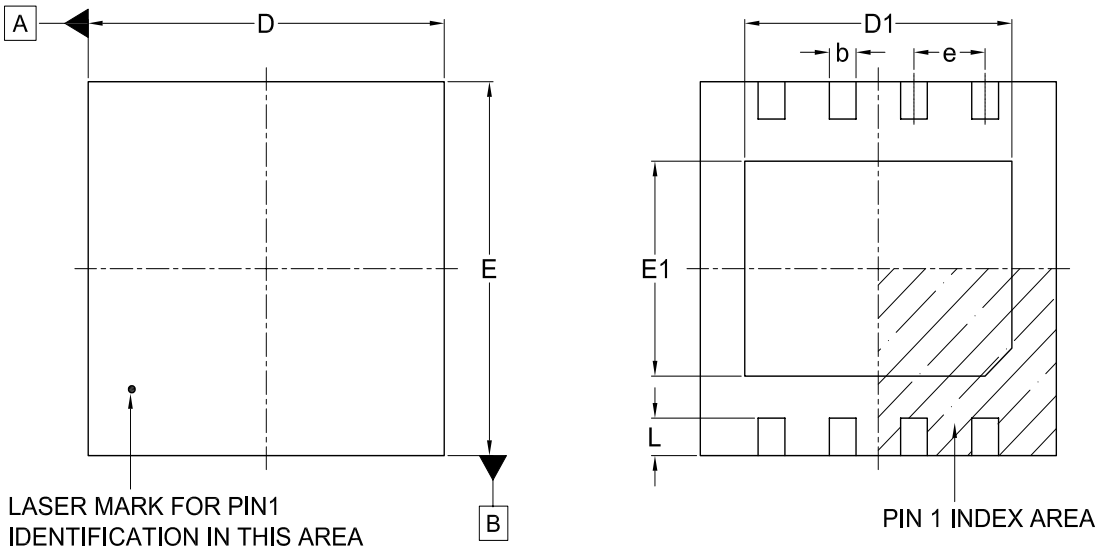
Note:

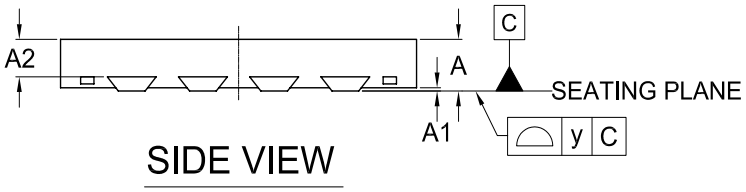
This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | L | e | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 0.70 | --- | --- | 0.35 | 5.90 | 3.35 | 4.90 | 3.95 | 0.55 | --- | 0.00 |
| | Nom. | --- | --- | 0.20 | 0.40 | 6.00 | 3.40 | 5.00 | 4.00 | 0.60 | 1.27 | --- |
| | Max. | 0.80 | 0.05 | --- | 0.48 | 6.10 | 3.45 | 5.10 | 4.05 | 0.65 | --- | 0.05 |
| Inch | Min. | 0.028 | --- | --- | 0.014 | 0.232 | 0.132 | 0.193 | 0.156 | 0.022 | --- | 0.00 |
| | Nom. | --- | --- | 0.008 | 0.016 | 0.236 | 0.134 | 0.197 | 0.157 | 0.024 | 0.05 | --- |
| | Max. | 0.032 | 0.002 | --- | 0.019 | 0.240 | 0.136 | 0.201 | 0.159 | 0.026 | --- | 0.002 |

**Doc. Title: Package Outline for USON 8L (4x4x0.6MM, LEAD PITCH 0.8MM)**




Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | L | e | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 0.50 | --- | --- | 0.25 | 3.90 | 2.90 | 3.90 | 2.20 | 0.35 | --- | 0.00 |
| | Nom. | 0.55 | 0.04 | 0.40 | 0.30 | 4.00 | 3.00 | 4.00 | 2.30 | 0.40 | 0.80 | --- |
| | Max. | 0.60 | 0.05 | 0.43 | 0.35 | 4.10 | 3.10 | 4.10 | 2.40 | 0.45 | --- | 0.08 |
| Inch | Min. | 0.020 | --- | --- | 0.010 | 0.154 | 0.114 | 0.154 | 0.087 | 0.014 | --- | 0.00 |
| | Nom. | 0.022 | 0.002 | 0.016 | 0.011 | 0.157 | 0.118 | 0.157 | 0.091 | 0.016 | 0.031 | --- |
| | Max. | 0.024 | 0.002 | 0.017 | 0.014 | 0.161 | 0.122 | 0.161 | 0.094 | 0.018 | --- | 0.003 |

## REVISION HISTORY

| Revision No. | Description | Page | Date |
|---|---|---|---|
| 1.1 | 1. Added RDSCUR & WRSCUR diagram form | P38 | SEP/02/2011 |
| | 2. Added CS# rising and falling time description | P10,28 | |
| | 3. Modified tW from 40(typ.)/100(max.) to 5(typ.)/40(max.) | P28,42 | |
| | 4. Modified description for RoHS compliance | P6,43,44 | |
| 1.2 | 1. Added Read SFDP (RDSFDP) Mode | P6,10,15, P24~29,34 | FEB/10/2012 |
| 1.3 | 1. Modified ABSOLUTE MAXIMUM RATINGS table | P31 | SEP/05/2013 |
| | 2. Modified WRSCUR Figure | P44 | |
| 1.4 | 1. Updated parameters for DC/AC Characteristics | P33,34 | NOV/06/2013 |
| | 2. Updated Erase and Programming Performance | P5,48 | |
| 1.5 | 1. Modified Hold figure and description | P14 | OCT/16/2014 |
| | 2. Modified notes for SFDP table | P29 | |
| 1.6 | 1. Updated tVR descriptions | P46 | AUG/28/2017 |
| | 2. Updated *"BLOCK DIAGRAM"*. | P8 | |
| | 2. Modified SRWD bit descriptions. | P17 | |
| | 3. Content and format modifications for 8-WSON package outline | P54 | |
| | 4. Updated the descriptions of REMS command. | P22 | |
| | 5. Added *"Figure 8. SCLK TIMING DEFINITION"*. | P32 | |
| | 6. Added a statement for product ordering information. | P49 | |
| | 7. Format modifications for package outline | P51-53,55 | |
| | 8. Content correction | P16-17,19-23 | |

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