# MX25L12872F

## 3V, 128M-BIT [x 1/x 2/x 4]
## CMOS MXSMIO® (SERIAL MULTI I/O)
## FLASH MEMORY

### *Key Features*

- *Protocol Support - Single I/O, Dual I/O and Quad I/O*
- *Quad Peripheral Interface (QPI) available*
- *Supports clock frequencies up to 133MHz*
- *Program/Erase Suspend and Resume*
- *Additional 8K-bit secured OTP*
- *Quad I/O mode is permanently enabled*

深圳市满度科技有限公司
Web:www.manduic.com

Tel:150-1290-5940
Email:sales@manduic.com

微信扫码咨询客服

# Contents

**1. FEATURES ..... 4**
**2. GENERAL DESCRIPTION ..... 5**
Table 1. Read performance Comparison ..... 5
**3. PIN CONFIGURATIONS ..... 6**
**4. PIN DESCRIPTION ..... 6**
**5. BLOCK DIAGRAM ..... 7**
**6. DATA PROTECTION ..... 8**
Table 2. Protected Area Sizes ..... 9
Table 3. 8K-bit Secured OTP Definition ..... 10
**7. Memory Organization ..... 11**
Table 4. Memory Organization ..... 11
**8. DEVICE OPERATION ..... 12**
8-1. Quad Peripheral Interface (QPI) Read Mode ..... 14
**9. COMMAND DESCRIPTION ..... 15**
Table 5. Command Set ..... 15
9-1. Write Enable (WREN) ..... 18
9-2. Write Disable (WRDI) ..... 19
9-3. Factory Mode Enable (FMEN) ..... 20
9-4. Read Identification (RDID) ..... 21
9-5. Release from Deep Power-down (RDP), Read Electronic Signature (RES) ..... 22
9-6. Read Electronic Manufacturer ID & Device ID (REMS) ..... 24
9-7. QPI ID Read (QPIID) ..... 25
Table 6. ID Definitions ..... 25
9-8. Read Status Register (RDSR) ..... 26
9-9. Read Configuration Register (RDCR) ..... 27
Table 7. Status Register ..... 30
Table 8. Configuration Register Table ..... 31
Table 9. Output Driver Strength Table ..... 32
Table 10. Dummy Cycle and Frequency Table (MHz) ..... 32
9-10. Write Status Register (WRSR) ..... 33
Table 11. Protection Modes ..... 34
9-11. Read Data Bytes (READ) ..... 36
9-12. Read Data Bytes at Higher Speed (FAST_READ) ..... 37
9-13. Dual Output Read Mode (DREAD) ..... 38
9-14. 2 x I/O Read Mode (2READ) ..... 39
9-15. Quad Read Mode (QREAD) ..... 40
9-16. 4 x I/O Read Mode (4READ) ..... 41
9-17. Burst Read ..... 43
9-18. Performance Enhance Mode - XIP (execute-in-place) ..... 44
9-19. Sector Erase (SE) ..... 47
9-20. Block Erase (BE32K) ..... 48
9-21. Block Erase (BE) ..... 49
9-22. Chip Erase (CE) ..... 50
9-23. Page Program (PP) ..... 51


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

9-24. 4 x I/O Page Program (4PP) ..... 53
9-25. Deep Power-down (DP) ..... 54
9-26. Write Security Register (WRSCUR) ..... 55
9-27. Read Security Register (RDSCUR) ..... 56
9-28. Enter Secured OTP (ENSO) ..... 57
9-29. Exit Secured OTP (EXSO) ..... 57
Table 12. Security Register Definition ..... 58
9-30. Write Protection Selection (WPSEL) ..... 59
9-31. Advanced Sector Protection ..... 61
Table 13. Lock Register ..... 62
Table 14. SPB Register ..... 63
Table 15. DPB Register ..... 65
9-32. Program/Erase Suspend/Resume ..... 67
9-33. Erase Suspend ..... 67
9-34. Program Suspend ..... 67
9-35. Write-Resume ..... 69
9-36. No Operation (NOP) ..... 69
9-37. Software Reset (Reset-Enable (RSTEN) and Reset (RST)) ..... 69
9-38. Read SFDP Mode (RDSFDP) ..... 71
**10. RESET ..... 72**
Table 16. Reset Timing-(Other Operation) ..... 72
**11. POWER-ON STATE ..... 73**
**12. ELECTRICAL SPECIFICATIONS ..... 74**
Table 17. ABSOLUTE MAXIMUM RATINGS ..... 74
Table 18. CAPACITANCE TA = 25°C, f = 1.0 MHz ..... 74
Table 19. DC CHARACTERISTICS ..... 76
Table 20. AC CHARACTERISTICS ..... 77
**13. OPERATING CONDITIONS ..... 79**
Table 21. Power-Up/Down Voltage and Timing ..... 81
13-1. INITIAL DELIVERY STATE ..... 81
**14. ERASE AND PROGRAMMING PERFORMANCE ..... 82**
**15. ERASE AND PROGRAMMING PERFORMANCE (Factory Mode) ..... 82**
**16. DATA RETENTION ..... 83**
**17. LATCH-UP CHARACTERISTICS ..... 83**
**18. ORDERING INFORMATION ..... 84**
**19. PART NAME DESCRIPTION ..... 85**
**20. PACKAGE INFORMATION ..... 86**
20-1. 8-pins SOP (200mil) ..... 86
20-2. 8-land WSON (6x5mm) ..... 87
**21. REVISION HISTORY ..... 88**


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

# 3V 128M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

## 1. FEATURES

### GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- Single Power Supply Operation
  - 2.7 to 3.6 volts for read, erase, and program operations
- 134,217,728 x 1 bit structure
  or 67,108,864 x 2 bits (two I/O mode) structure
  or 33,554,432 x 4 bits (four I/O mode) structure
- Protocol Support
  - Single I/O, Dual I/O and Quad I/O
- Latch-up protected to 100mA from -1V to Vcc +1V
- Fast read for SPI mode
  - Supports clock frequencies up to 133MHz for all protocols
  - Supports Fast Read, 2READ, DREAD, 4READ, QREAD instructions.
  - Configurable dummy cycle number for fast read operation
- Supports Performance Enhance Mode - XIP (execute-in-place)
- Default Quad I/O enable (QE bit=1), and cannot be changed
- Quad Peripheral Interface (QPI) available
- Equal 4K byte sectors, or Equal Blocks with 32K bytes or 64K bytes each
  - Any Block can be erased individually
- Programming :
  - 256byte page buffer
  - Quad Input/Output page program(4PP) to enhance program performance
- Typical 100,000 erase/program cycles
- 20 years data retention

### SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
  The BP0-BP3 and T/B status bit defines the size of the area to be protection against program and erase instructions
  - Advanced sector protection function (Solid Protect)
- Additional 8K bit security OTP
  - Features unique identifier
  - Factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Supports Serial Flash Discoverable Parameters (SFDP) mode

### HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SIO2
  - Serial Data Input/Output for 4 x I/O read mode
- SIO3
  - Serial Data Input/Output for 4 x I/O read mode
- PACKAGE
  -8-pin SOP (200mil)
  -8-land WSON (6x5mm)
  - **All devices are RoHS Compliant and Halogen-free**

深圳市满度科技有限公司
Web:www.manduic.com
P/N: PM2541



Tel:150-1200-5940
Email:sales@manduic.com

## 2. GENERAL DESCRIPTION

MX25L12872F is 128Mb bits Serial NOR Flash memory, which is configured as 16,777,216 x 8 internally. When it is in two or four I/O mode, the structure becomes 67,108,864 bits x 2 or 33,554,432 bits x 4. MX25L12872F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin, and SIO2 pin and SIO3 pin are also enabled for address/dummy bits input and data output.

The MX25L12872F MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please refer to security features section for more details.

When the device is not in operation and CS# is high, it will remain in standby mode.

The MX25L12872F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

**Table 1. Read performance Comparison**

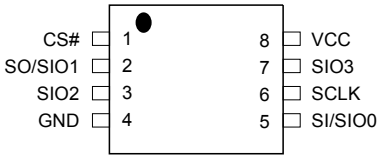
| Numbers of Dummy Cycles | Fast Read (MHz) | Dual Output Fast Read (MHz) | Quad Output Fast Read (MHz) | Dual IO Fast Read (MHz) | Quad IO Fast Read (MHz) |
|---|---|---|---|---|---|
| 4 | - | - | - | 84* | 66 |
| 6 | 104 | 104 | 84 | 104 | 84* |
| 8 | 104* | 104* | 104* | 104 | 104 |
| 10 | 133 | 133 | 133 | 133 | 120/133R |

**Notes:**
1. * Default Status.
2. R means VCC range = 3.0V-3.6V.

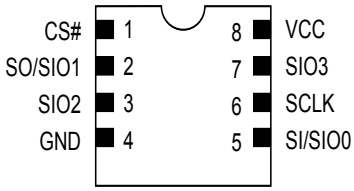

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 3. PIN CONFIGURATIONS

### 8-PIN SOP (200mil)




### 8-WSON (6x5mm)

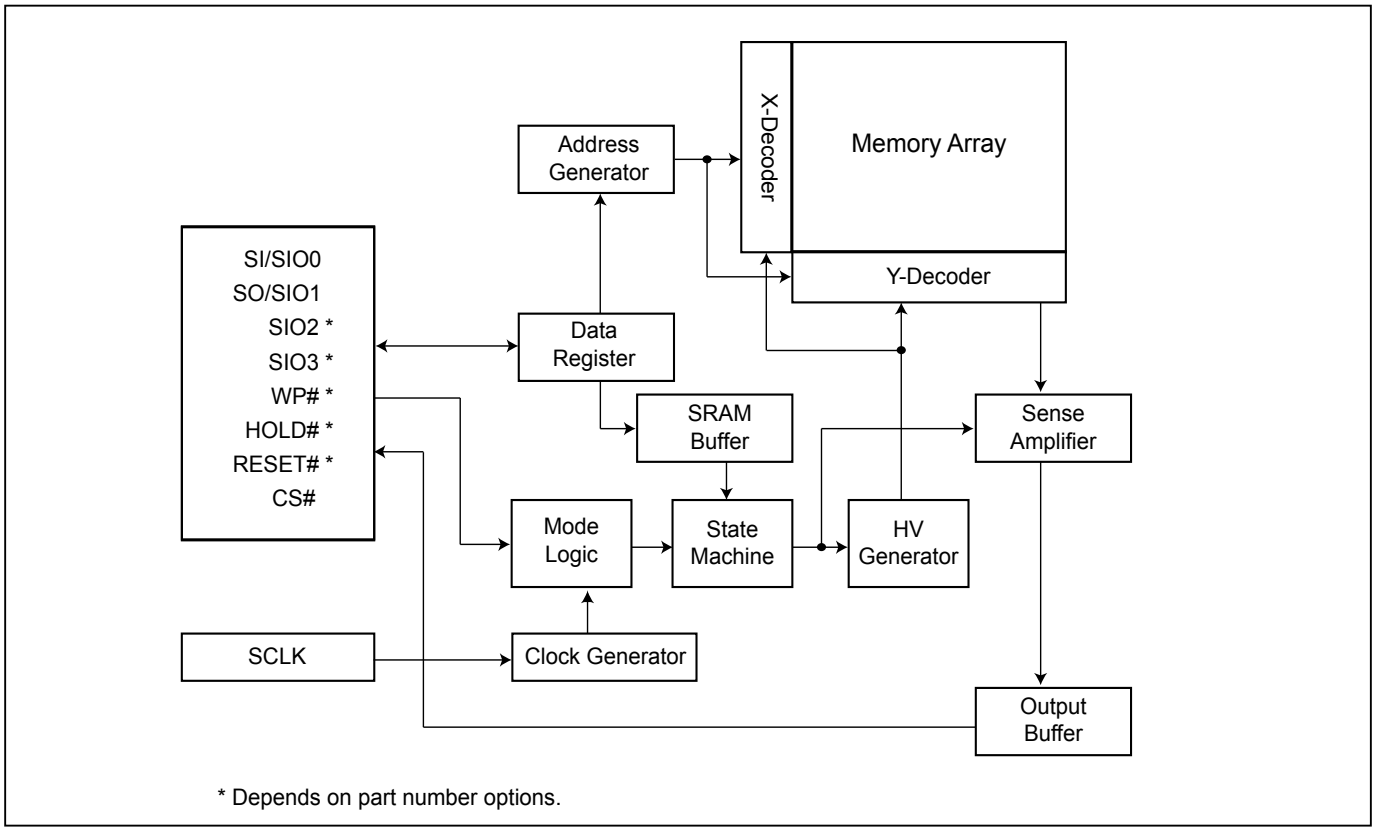



## 4. PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| CS# | Chip Select |
| SI/SIO0 | Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode) |
| SO/SIO1 | Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode) |
| SCLK | Clock Input |
| SIO2 | Serial Data Input & Output (for 4xI/O read mode) |
| SIO3 | Serial Data Input & Output (for 4xI/O read mode) |
| VCC | + 3V Power Supply |
| GND | Ground |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 5. BLOCK DIAGRAM





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other commands to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**I. Block lock protection**

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

**Table 2. Protected Area Sizes**

**Protected Area Sizes (T/B bit = 0)**

| Status bit | | | | Protect Level |
|---|---|---|---|---|
| BP3 | BP2 | BP1 | BP0 | 128Mb |
| 0 | 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 0 | 1 | 1 (1 block, protected block 255th) |
| 0 | 0 | 1 | 0 | 2 (2 blocks, block 254th-255th) |
| 0 | 0 | 1 | 1 | 3 (4 blocks, block 252nd-255th) |
| 0 | 1 | 0 | 0 | 4 (8 blocks, block 248th-255th) |
| 0 | 1 | 0 | 1 | 5 (16 blocks, block 240th-255th) |
| 0 | 1 | 1 | 0 | 6 (32 blocks, block 224th-255th) |
| 0 | 1 | 1 | 1 | 7 (64 blocks, block 192nd-255th) |
| 1 | 0 | 0 | 0 | 8 (128 blocks, block 128th-255th) |
| 1 | 0 | 0 | 1 | 9 (256 blocks, protected all) |
| 1 | 0 | 1 | 0 | 10 (256 blocks, protected all) |
| 1 | 0 | 1 | 1 | 11 (256 blocks, protected all) |
| 1 | 1 | 0 | 0 | 12 (256 blocks, protected all) |
| 1 | 1 | 0 | 1 | 13 (256 blocks, protected all) |
| 1 | 1 | 1 | 0 | 14 (256 blocks, protected all) |
| 1 | 1 | 1 | 1 | 15 (256 blocks, protected all) |

**Protected Area Sizes (T/B bit = 1)**

| Status bit | | | | Protect Level |
|---|---|---|---|---|
| BP3 | BP2 | BP1 | BP0 | 128Mb |
| 0 | 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 0 | 1 | 1 (1 block, protected block 0th) |
| 0 | 0 | 1 | 0 | 2 (2 blocks, protected block 0th-1st) |
| 0 | 0 | 1 | 1 | 3 (4 blocks, protected block 0th-3rd) |
| 0 | 1 | 0 | 0 | 4 (8 blocks, protected block 0th-7th) |
| 0 | 1 | 0 | 1 | 5 (16 blocks, protected block 0th-15th) |
| 0 | 1 | 1 | 0 | 6 (32 blocks, protected block 0th-31st) |
| 0 | 1 | 1 | 1 | 7 (64 blocks, protected block 0th-63rd) |
| 1 | 0 | 0 | 0 | 8 (128 blocks, protected block 0th-127th) |
| 1 | 0 | 0 | 1 | 9 (256 blocks, protected all) |
| 1 | 0 | 1 | 0 | 10 (256 blocks, protected all) |
| 1 | 0 | 1 | 1 | 11 (256 blocks, protected all) |
| 1 | 1 | 0 | 0 | 12 (256 blocks, protected all) |
| 1 | 1 | 0 | 1 | 13 (256 blocks, protected all) |
| 1 | 1 | 1 | 0 | 14 (256 blocks, protected all) |
| 1 | 1 | 1 | 1 | 15 (256 blocks, protected all) |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

II. **Additional 8K-bit secured OTP** for an unique identifier to provide an 8K-bit one-time program area for setting a device unique serial number. This may be accomplished in the factory or by an end systems customer.

The 8K-bit secured OTP area is composed of two rows of 4K-bit. Customer could lock the first 4K-bit OTP area and factory could lock the other.

- Security register bit 0 indicates whether the second 4K-bit is locked by factory or not.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 12. Security Register Definition"* for security register bit definition and *"Table 3. 8K-bit Secured OTP Definition"* for address range definition.

- The 8K-bit secured OTP area is programmed by entering secured OTP mode (with the Enter Security OTP command), and going through a normal program procedure. Exiting secured OTP mode is done by issuing the Exit Security OTP command.

**Note:** Once lock-down whatever by factory or customer, the corresponding secured area cannot be changed any more. While in 8K-bit Secured OTP mode, array access is not allowed.

**Table 3. 8K-bit Secured OTP Definition**

| Address range | Size | Customer Lock | Standard Factory Lock |
|---|---|---|---|
| xxx000-xxx1FF | 4096-bit | Determined by customer | N/A |
| xxx200-xxx3FF | 4096-bit | N/A | Determined by factory |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 7. Memory Organization

### Table 4. Memory Organization

| Block(64K-byte) | Block(32K-byte) | Sector | Address Range | |
|---|---|---|---|---|
| 255 | 511 | 4095 | FFF000h | FFFFFFh |
| | | ⋮ | | |
| | | 4088 | FF8000h | FF8FFFh |
| | 510 | 4087 | FF7000h | FF7FFFh |
| | | ⋮ | | |
| | | 4080 | FF0000h | FF0FFFh |
| 254 | 509 | 4079 | FEF000h | FEFFFFh |
| | | ⋮ | | |
| | | 4072 | FE8000h | FE8FFFh |
| | 508 | 4071 | FE7000h | FE7FFFh |
| | | ⋮ | | |
| | | 4064 | FE0000h | FE0FFFh |
| 253 | 507 | 4063 | FDF000h | FDFFFFh |
| | | ⋮ | | |
| | | 4056 | FD8000h | FD8FFFh |
| | 506 | 4055 | FD7000h | FD7FFFh |
| | | ⋮ | | |
| | | 4048 | FD0000h | FD0FFFh |
| 2 | 5 | 47 | 02F000h | 02FFFFh |
| | | ⋮ | | |
| | | 40 | 028000h | 028FFFh |
| | 4 | 39 | 027000h | 027FFFh |
| | | ⋮ | | |
| | | 32 | 020000h | 020FFFh |
| 1 | 3 | 31 | 01F000h | 01FFFFh |
| | | ⋮ | | |
| | | 24 | 018000h | 018FFFh |
| | 2 | 23 | 017000h | 017FFFh |
| | | ⋮ | | |
| | | 16 | 010000h | 010FFFh |
| 0 | 1 | 15 | 00F000h | 00FFFFh |
| | | ⋮ | | |
| | | 8 | 008000h | 008FFFh |
| | 0 | 7 | 007000h | 007FFFh |
| | | ⋮ | | |
| | | 0 | 000000h | 000FFFh |

individual 16 sectors lock/unlock unit:4K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When an incorrect command is written to this device, it enters standby mode and stays in standby mode until the next CS# falling edge. In standby mode, This device's SO pin should be High-Z.

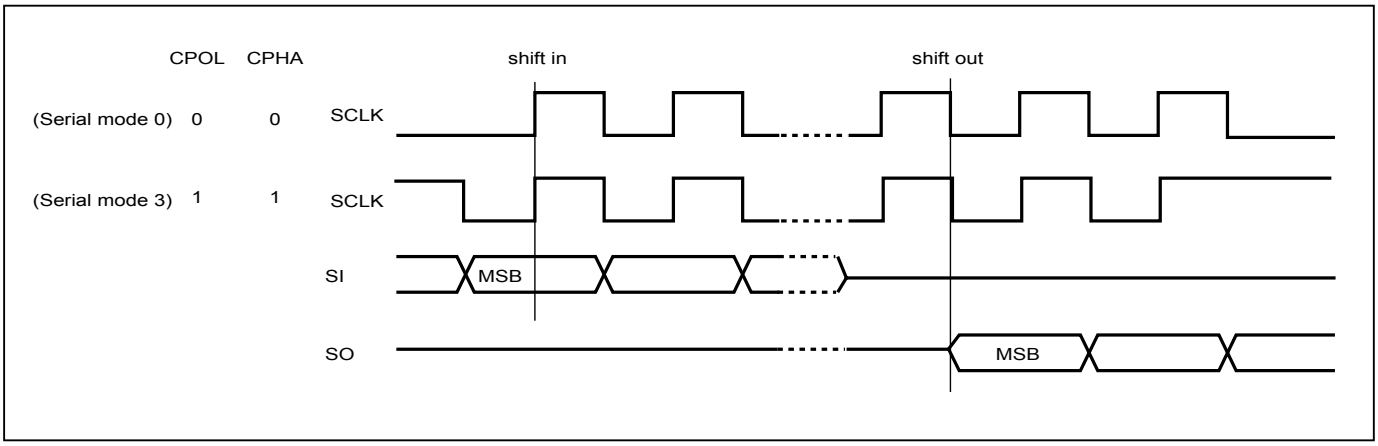
3. When a correct command is written to this device, it enters active mode and stays in active mode until the next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, 2READ, DREAD, 4READ, QREAD, RDSFDP, RES, REMS, QPIID, RDDPB, RDSPB, RDLR, RDCR the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, WPSEL, GBLK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program, or Erase operation is in progress, access to the memory array is ignored and will not affect the current operation of Write Status Register, Program, or Erase.

**Figure 1. Serial Modes Supported**




**Note:**
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 2. Serial Input Timing**

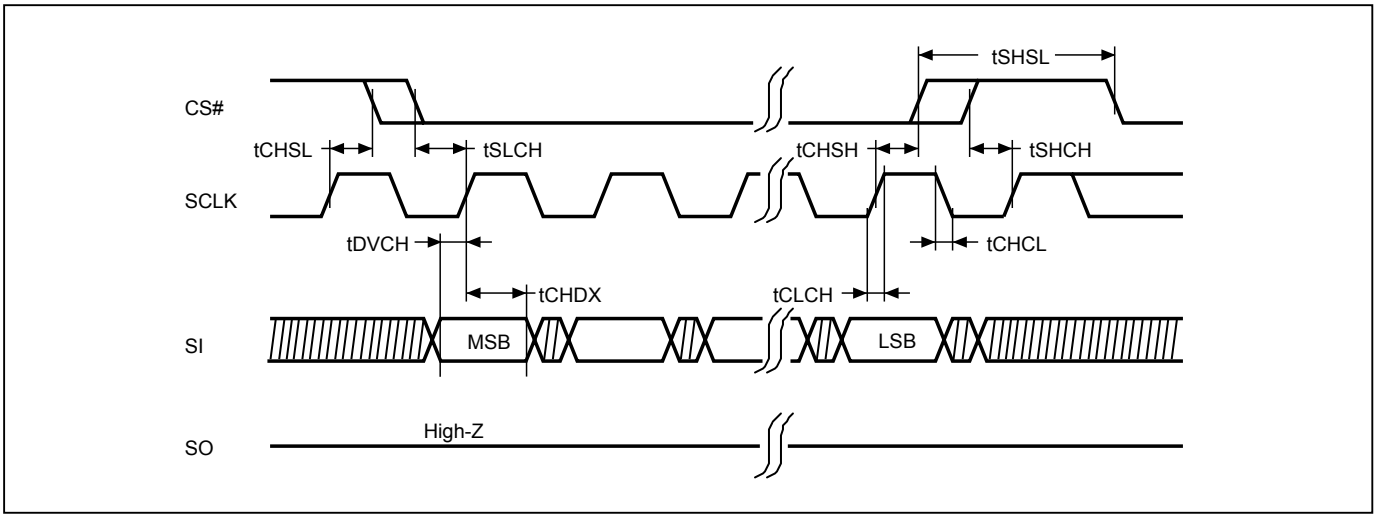
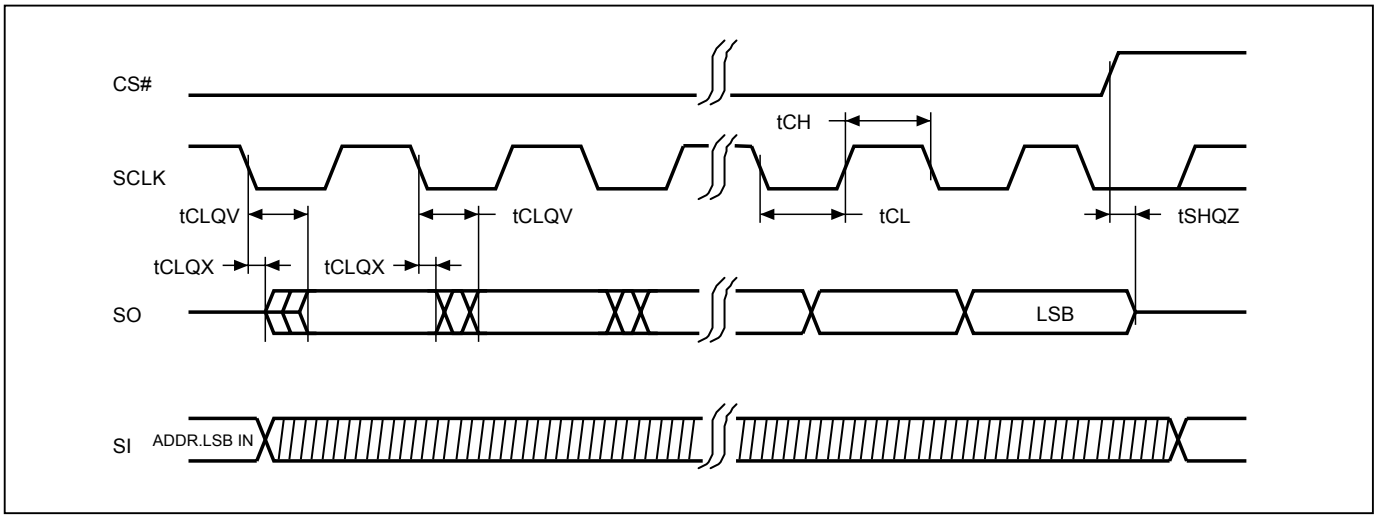



**Figure 3. Output Timing**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

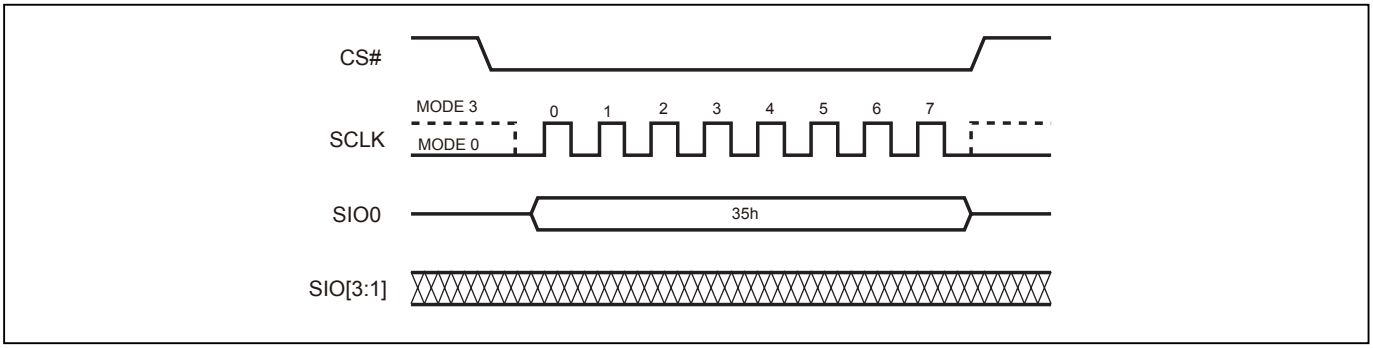
### 8-1. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial NOR Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

#### Enable QPI mode

By issuing EQIO command (35h), the QPI mode is enabled. After QPI mode has been enabled, the device enter quad mode (4-4-4) without QE bit status changed.

**Figure 4. Enable QPI Sequence**

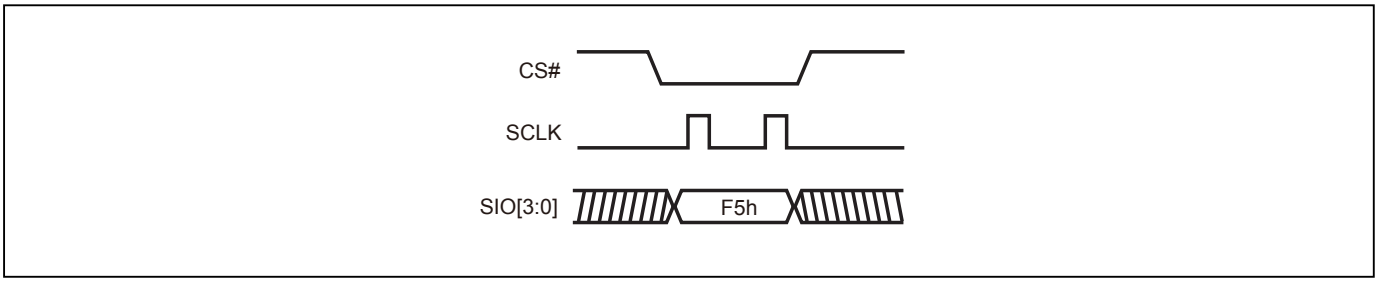



#### Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5h) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

**Note:**
For EQIO and RSTQIO commands, CS# high width has to follow "From Write/Erase/Program to Read Status Register spec" tSHSL (as defined in *"Table 20. AC CHARACTERISTICS"*) for next instruction.

**Figure 5. Reset QPI Mode**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 9. COMMAND DESCRIPTION

### Table 5. Command Set

| | Command Code | SPI | QPI | Address Byte | | | | | Dummy Cycle | Data Byte |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Total ADD Byte | Byte 1 | Byte 2 | Byte 3 | Byte 4 | | |
| **Array access** | | | | | | | | | | |
| READ (normal read) | 03 (hex) | V | | 3 | ADD1 | ADD2 | ADD3 | | 0 | 1- ∞ |
| FAST READ (fast read data) | 0B (hex) | V | | 3 | ADD1 | ADD2 | ADD3 | | 8 * | 1- ∞ |
| 2READ (2 x I/O read command) | BB (hex) | V | | 3 | ADD1 | ADD2 | ADD3 | | 4 * | 1- ∞ |
| DREAD (1I 2O read) | 3B (hex) | V | | 3 | ADD1 | ADD2 | ADD3 | | 8 * | 1- ∞ |
| 4READ (4 I/O read) | EB (hex) | V | V | 3 | ADD1 | ADD2 | ADD3 | | 6 * | 1- ∞ |
| QREAD (1I 4O read) | 6B (hex) | V | | 3 | ADD1 | ADD2 | ADD3 | | 8 * | 1- ∞ |
| PP (page program) | 02 (hex) | V | V | 3 | ADD1 | ADD2 | ADD3 | | 0 | 1-256 |
| 4PP (quad page program) | 38 (hex) | V | | 3 | ADD1 | ADD2 | ADD3 | | 0 | 1-256 |
| SE (sector erase) | 20 (hex) | V | V | 3 | ADD1 | ADD2 | ADD3 | | 0 | 0 |
| BE 32K (block erase 32KB) | 52 (hex) | V | V | 3 | ADD1 | ADD2 | ADD3 | | 0 | 0 |
| BE (block erase 64KB) | D8 (hex) | V | V | 3 | ADD1 | ADD2 | ADD3 | | 0 | 0 |
| CE (chip erase) | 60 or C7 (hex) | V | V | 0 | | | | | 0 | 0 |
| **Device operation** | | | | | | | | | | |
| WREN (write enable) | 06 (hex) | V | V | 0 | | | | | 0 | 0 |
| WRDI (write disable) | 04 (hex) | V | V | 0 | | | | | 0 | 0 |
| WPSEL (Write Protect Selection) | 68 (hex) | V | V | 0 | | | | | 0 | 0 |
| EQIO (Enable QPI) | 35 (hex) | V | | 0 | | | | | 0 | 0 |
| RSTQIO (Reset QPI) | F5 (hex) | | V | 0 | | | | | 0 | 0 |
| PGM/ERS Suspend (Suspends Program/ Erase) | 75 or B0 (hex) | V | V | 0 | | | | | 0 | 0 |
| PGM/ERS Resume (Resumes Program/ Erase) | 7A or 30 (hex) | V | V | 0 | | | | | 0 | 0 |
| DP (Deep power down) | B9 (hex) | V | V | 0 | | | | | 0 | 0 |
| RDP (Release from deep power down) | AB (hex) | V | V | 0 | | | | | 0 | 0 |

* Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

| | Command Code | SPI | QPI | Address Byte | | | | | Dummy Cycle | Data Byte |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Total ADD Byte | Byte 1 | Byte 2 | Byte 3 | Byte 4 | | |
| NOP (No Operation) | 00 (hex) | V | V | 0 | | | | | 0 | 0 |
| RSTEN (Reset Enable) | 66 (hex) *(Note2)* | V | V | 0 | | | | | 0 | 0 |
| RST (Reset Memory) | 99 (hex) *(Note2)* | V | V | 0 | | | | | 0 | 0 |
| GBLK (gang block lock) | 7E (hex) | V | V | 0 | | | | | 0 | 0 |
| GBULK (gang block unlock) | 98 (hex) | V | V | 0 | | | | | 0 | 0 |
| FMEN (factory mode enable) | 41 (hex) | V | V | 0 | | | | | 0 | 0 |
| **Register Access** | | | | | | | | | | |
| RDID (read identification) | 9F (hex) | V | | 0 | | | | | 0 | 3 |
| RES (read electronic ID) | AB (hex) | V | V | 0 | | | | | 24 | 1 |
| REMS (read electronic manufacturer & device ID) | 90 (hex) | V | | 0 | ADD1 | | | | 16 | 2 |
| QPIID (QPI ID Read) | AF (hex) | | V | 0 | | | | | 0 | 3 |
| RDSFDP (Read SFDP Table) | 5A (hex) | V | | 3 | ADD1 | ADD2 | ADD3 | | 8 | 1- ∞ |
| RDSR (read status register) | 05 (hex) | V | V | 0 | | | | | 0 | 1 |
| RDCR (read configuration register) | 15 (hex) | V | V | 0 | | | | | 0 | 1 |
| WRSR (write status/configuration register) | 01 (hex) | V | V | 0 | | | | | 0 | 1-2 |
| RDSCUR (read security register) | 2B (hex) | V | V | 0 | | | | | 0 | 1 |
| WRSCUR (write security register) | 2F (hex) | V | V | 0 | | | | | 0 | 0 |
| SBL (Set Burst Length) | C0 (hex) | V | V | 0 | | | | | 0 | 1 |
| ENSO (enter secured OTP) | B1 (hex) | V | V | 0 | | | | | 0 | 0 |
| EXSO (exit secured OTP) | C1 (hex) | V | V | 0 | | | | | 0 | 0 |
| WRLR (write Lock register) | 2C (hex) | V | | 0 | | | | | 0 | 2 |
| RDLR (read Lock register) | 2D (hex) | V | | 0 | | | | | 0 | 2 |
| WRSPB (SPB bit program) | E3 (hex) | V | | 4 | ADD1 | ADD2 | ADD3 | ADD4 | 0 | 0 |
| ESSPB (all SPB bit erase) | E4 (hex) | V | | 0 | | | | | 0 | 0 |
| RDSPB (read SPB status) | E2 (hex) | V | | 4 | ADD1 | ADD2 | ADD3 | ADD4 | 0 | 1 |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

| | Command Code | SPI | QPI | Address Byte | | | | | Dummy Cycle | Data Byte |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Total ADD Byte | Byte 1 | Byte 2 | Byte 3 | Byte 4 | | |
| WRDPB (write DPB register) | E1 (hex) | V | | 4 | ADD1 | ADD2 | ADD3 | ADD4 | 0 | 1 |
| RDDPB (read DPB register) | E0 (hex) | V | | 4 | ADD1 | ADD2 | ADD3 | ADD4 | 0 | 1 |

*Note 1:* It is not recommended to adopt any other code/address not in the command definition table, which will potentially enter the hidden mode.

*Note 2:* The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-1. Write Enable (WREN)

The Write Enable (WREN) instruction sets the Write Enable Latch (WEL) bit. Instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR that are intended to change the device content, should be preceded by the WREN instruction.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care in SPI mode.

**Figure 6. Write Enable (WREN) Sequence (SPI Mode)**

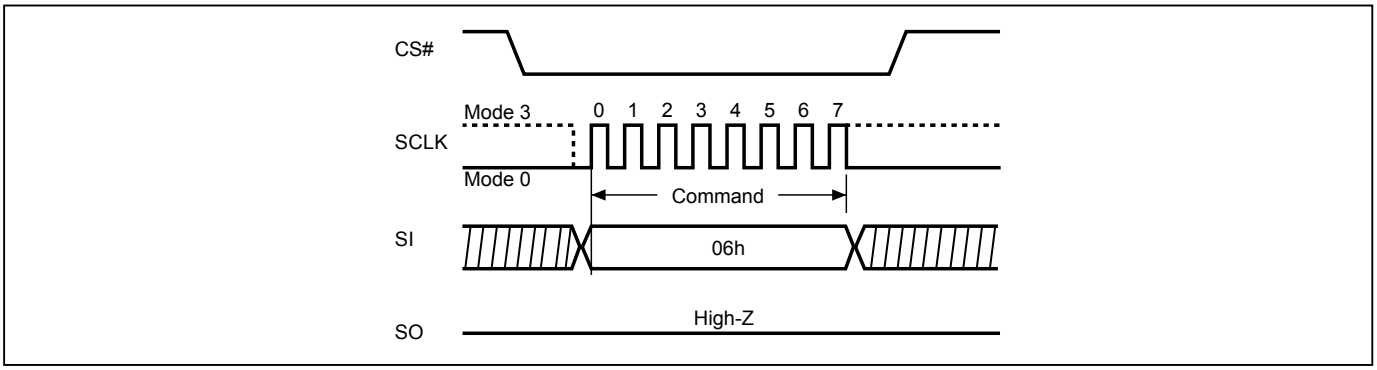
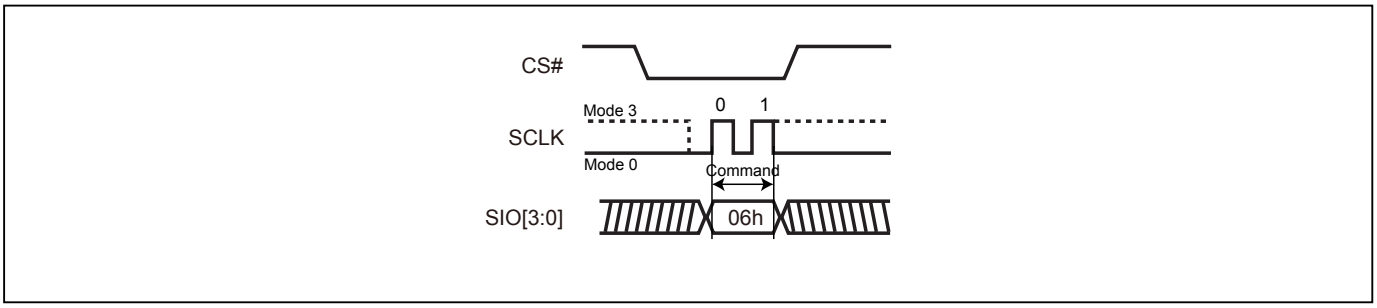



**Figure 7. Write Enable (WREN) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction resets the Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care in SPI mode.

The WEL bit is reset in the following situations:

- Power-up
- WRDI command completion
- WRSR command completion
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WPSEL command completion
- GBLK command completion
- GBULK command completion
- WRLR command completion
- WRSPB command completion
- ESSPB command completion
- WRDPB command completion

**Figure 8. Write Disable (WRDI) Sequence (SPI Mode)**

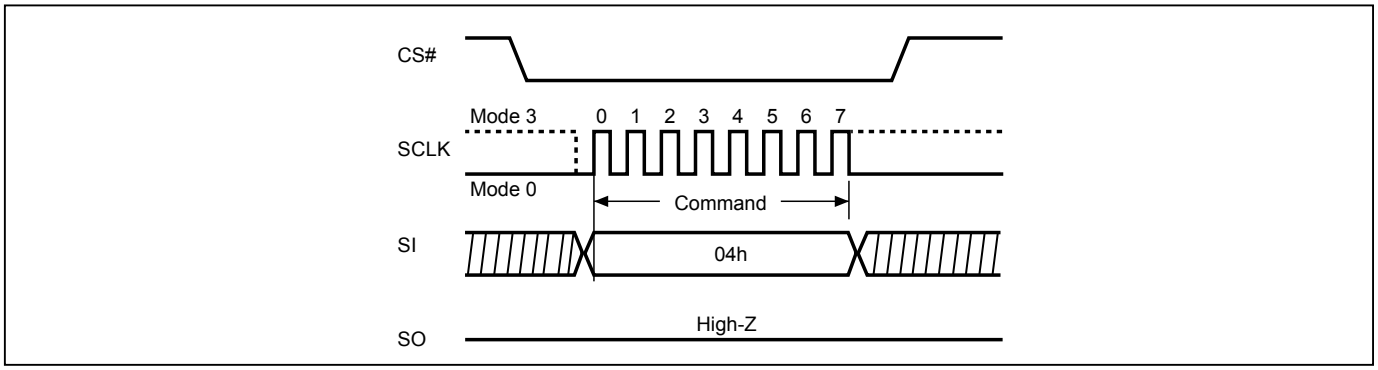
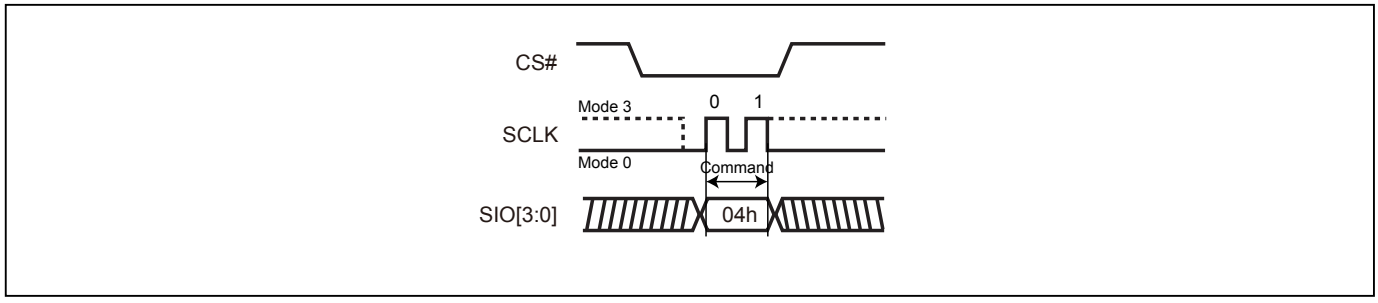



**Figure 9. Write Disable (WRDI) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-3. Factory Mode Enable (FMEN)

The Factory Mode Enable (FMEN) instruction enhances Program and Erase performance to increase factory production throughput. The FMEN instruction needs to be combined with the instructions which are intended to change the device content, like PP, 4PP, SE, BE32K, BE, and CE.

The sequence of issuing FMEN instruction is: CS# goes low→send FMEN instruction code→ CS# goes high. A valid factory mode operation need to included three sequences: WREN instruction → FMEN instruction→ Program or Erase instruction.

Suspend command is not acceptable under factory mode.

The FMEN is reset in the following situations

- Power-up
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- Softreset command completion

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care in SPI mode.

**Figure 10. Factory Mode Enable (FMEN) Sequence (SPI Mode)**

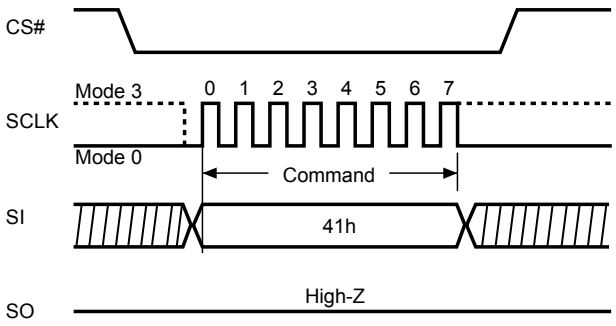
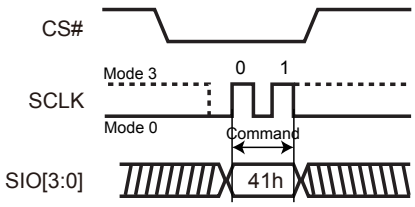



**Figure 11. Factory Mode Enable (FMEN) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

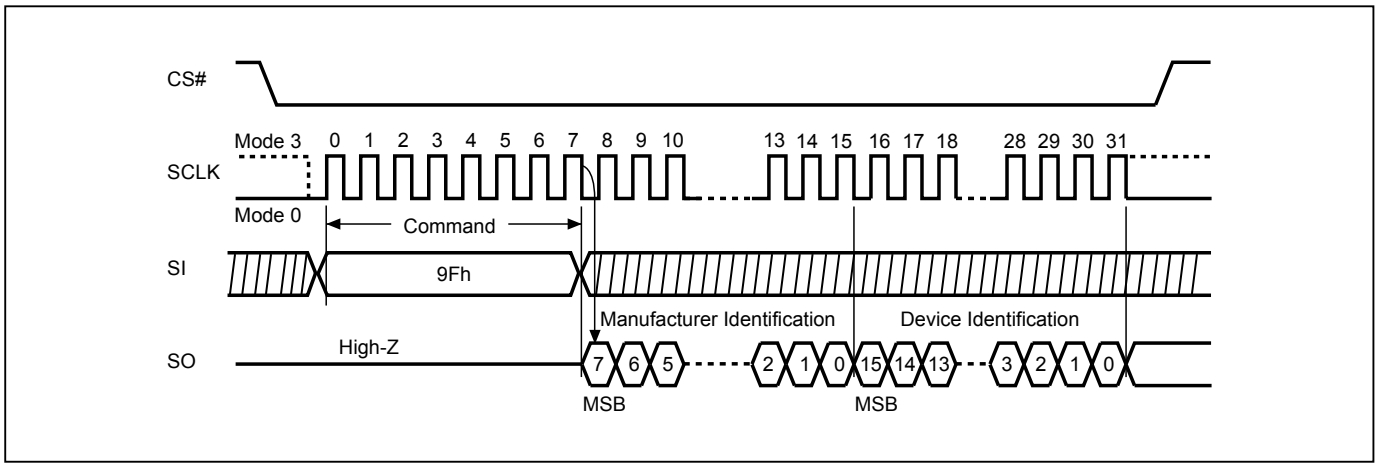
### 9-4. Read Identification (RDID)

The RDID instruction is for reading the 1-byte manufacturer ID and the 2-byte Device ID that follows. The Macronix Manufacturer ID and Device ID are listed as *"Table 6. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ send RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

**Figure 12. Read Identification (RDID) Sequence (SPI mode only)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-5. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 20. AC CHARACTERISTICS"*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode.

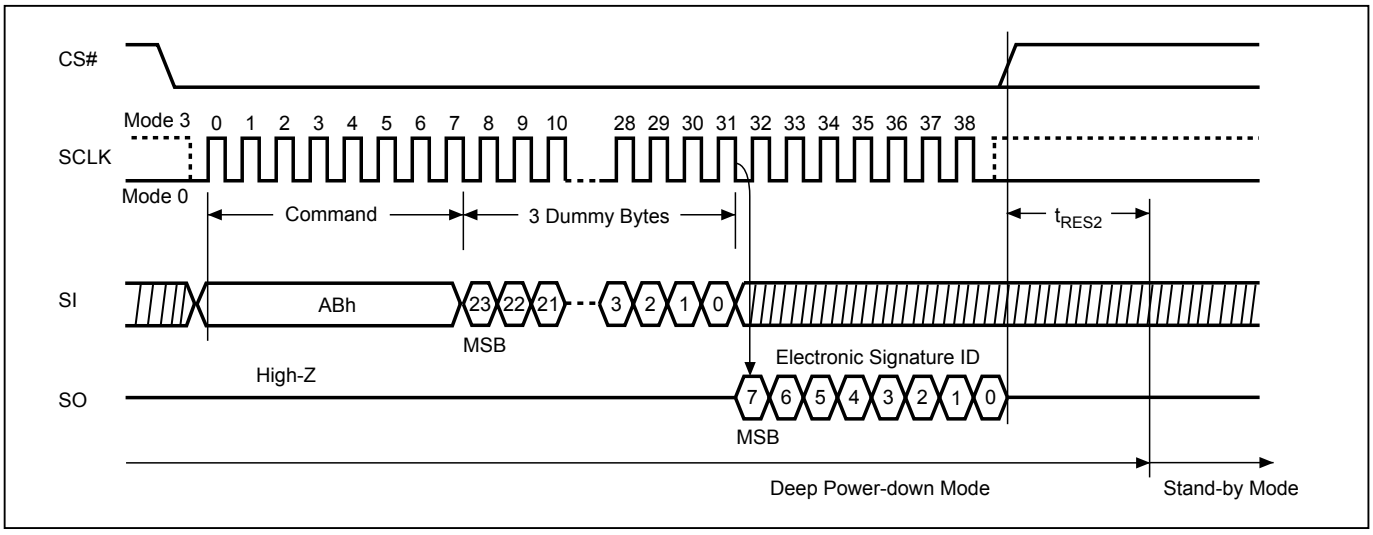
RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 6. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

The RDP and RES are allowed to execute in Deep power-down mode, except if the device is in progress of program/erase/write cycle; In this case, there is no effect on the current program/erase/write cycle that is in progress.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The RES instruction ends when CS# goes high, after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

**Figure 13. Read Electronic Signature (RES) Sequence (SPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 14. Read Electronic Signature (RES) Sequence (QPI Mode)**

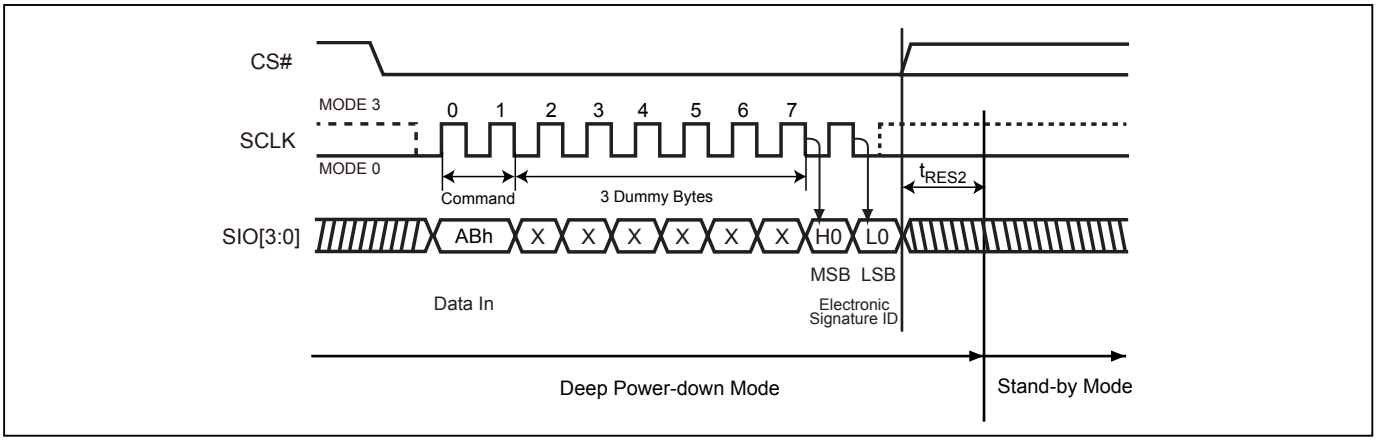



**Figure 15. Release from Deep Power-down (RDP) Sequence (SPI Mode)**

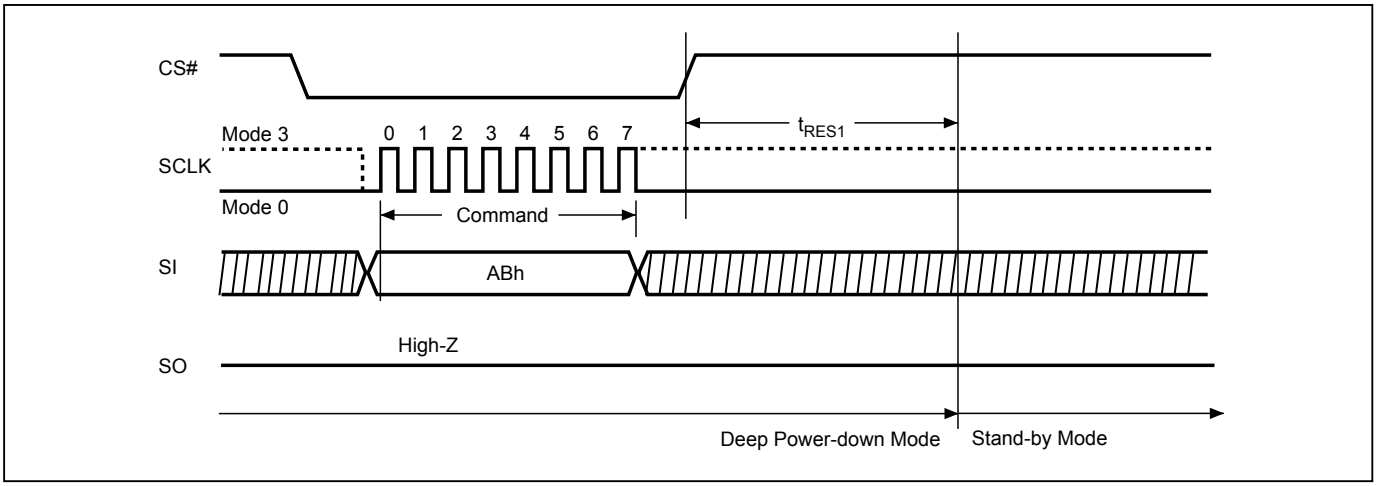
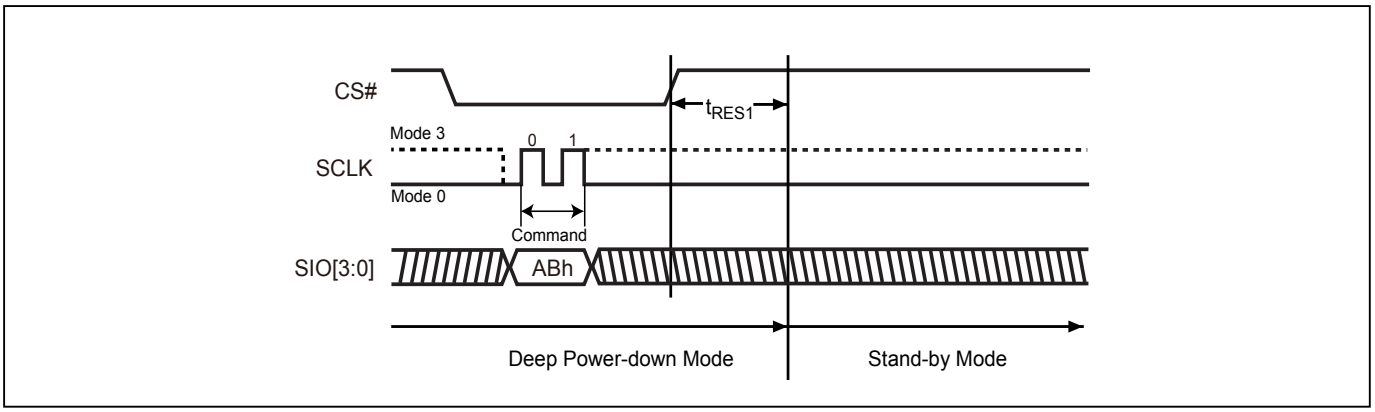



**Figure 16. Release from Deep Power-down (RDP) Sequence (QPI Mode)**





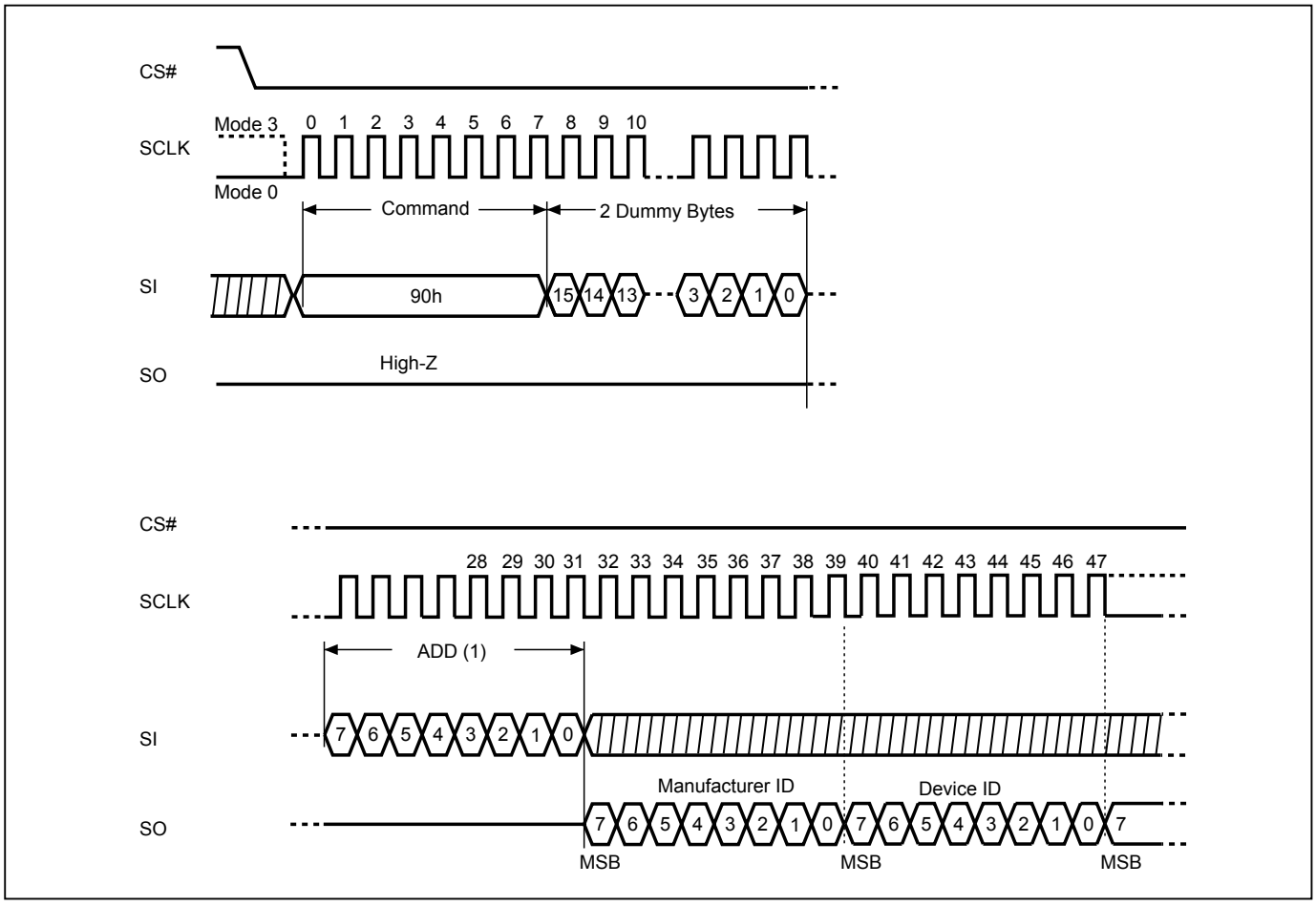
深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-6. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in *"Table 6. ID Definitions"*.

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7~A0). After which the manufacturer ID for Macronix (C2h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

**Figure 17. Read Electronic Manufacturer & Device ID (REMS) Sequence (SPI Mode only)**




**Note: (1)** ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-7. QPI ID Read (QPIID)

The QPIID Read instruction can be used to identify the Device ID and Manufacturer ID. The sequence of issuing the QPIID instruction is as follows: CS# goes low→send QPI ID instruction→Data out on SO→CS# goes high. Most significant bit (MSB) first.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The Manufacturer ID, Memory Type, and Memory Density data byte will be output continuously, until the CS# goes high.

**Table 6. ID Definitions**

| Command Type | | MX25L12872F | | |
|---|---|---|---|---|
| RDID | 9Fh | Manufacturer ID | Memory Type | Memory Density |
| | | C2 | 20 | 18 |
| RES | ABh | Electronic ID | | |
| | | 17 | | |
| REMS | 90h | Manufacturer ID | Device ID | |
| | | C2 | 17 | |
| QPIID | AFh | Manufacturer ID | Memory Type | Memory Density |
| | | C2 | 20 | 18 |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-8. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ send RDSR instruction code→ Status Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

**Figure 18. Read Status Register (RDSR) Sequence (SPI Mode)**

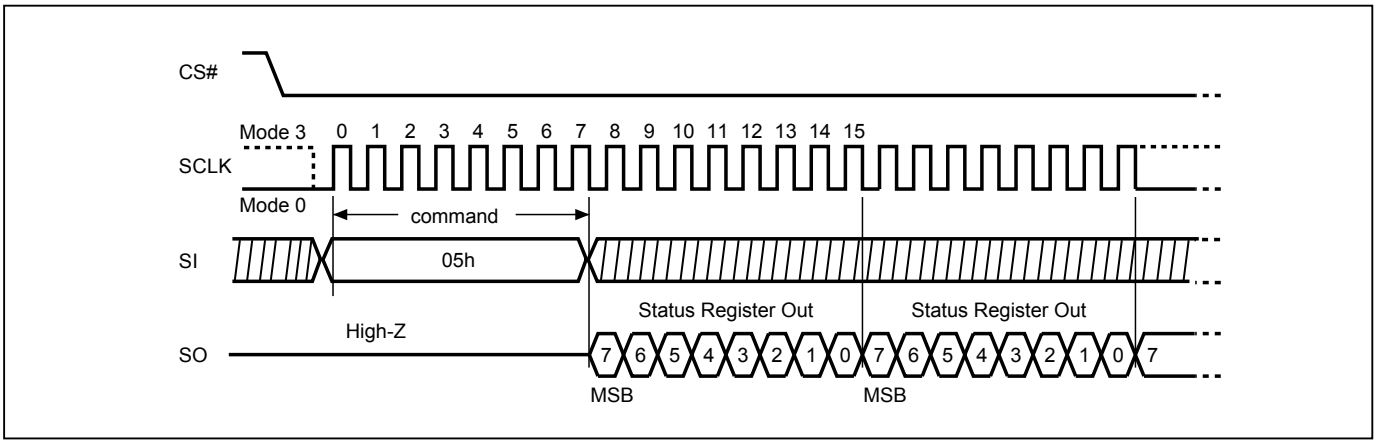
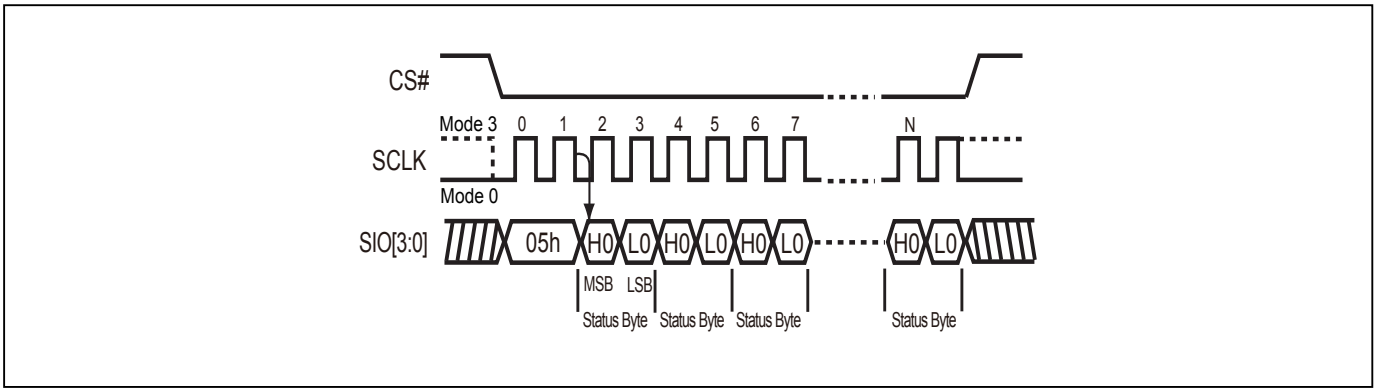



**Figure 19. Read Status Register (RDSR) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-9. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ send RDCR instruction code→ Configuration Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

**Figure 20. Read Configuration Register (RDCR) Sequence (SPI Mode)**

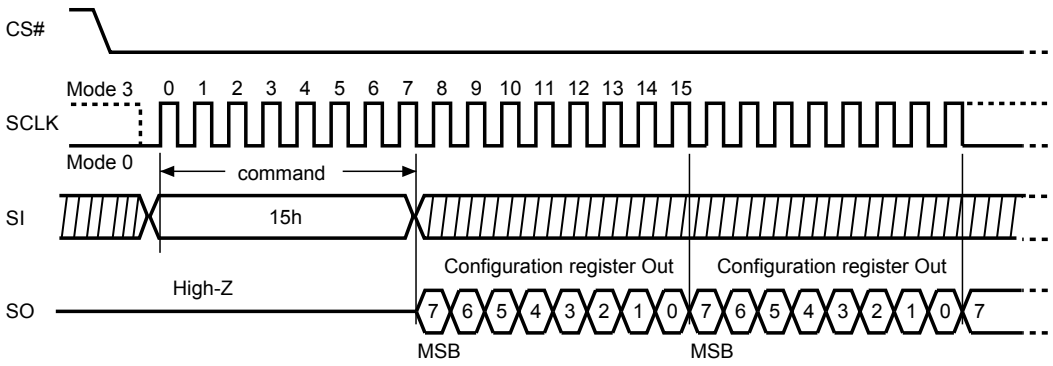
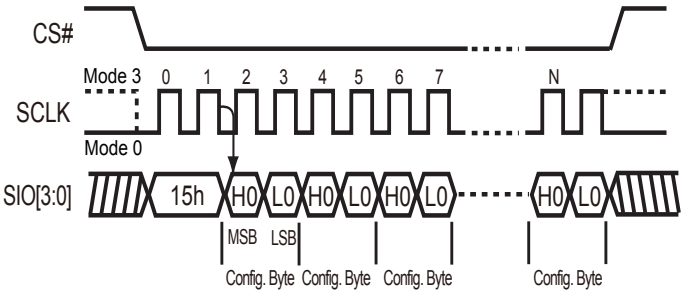



**Figure 21. Read Configuration Register (RDCR) Sequence (QPI Mode)**

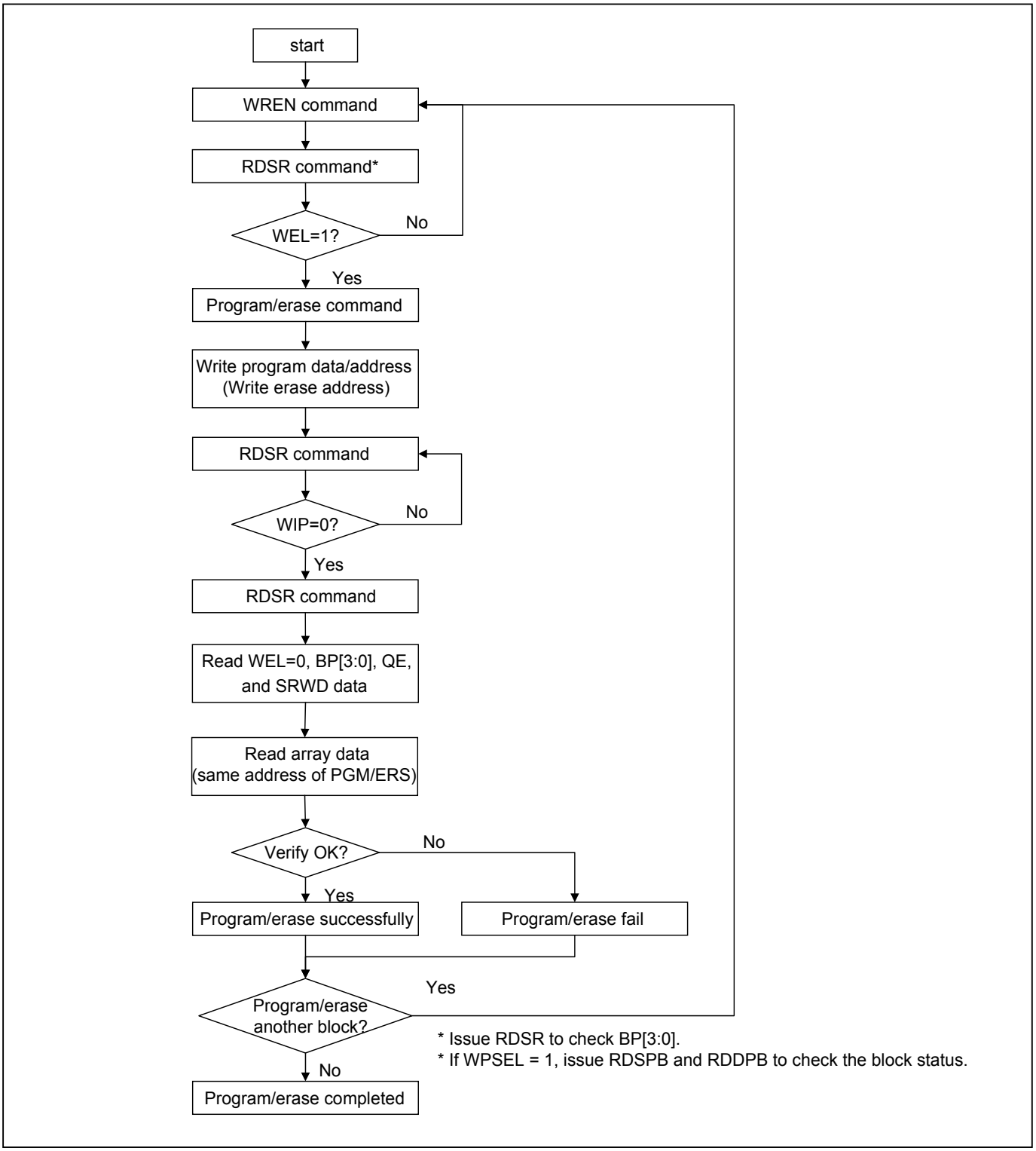




深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

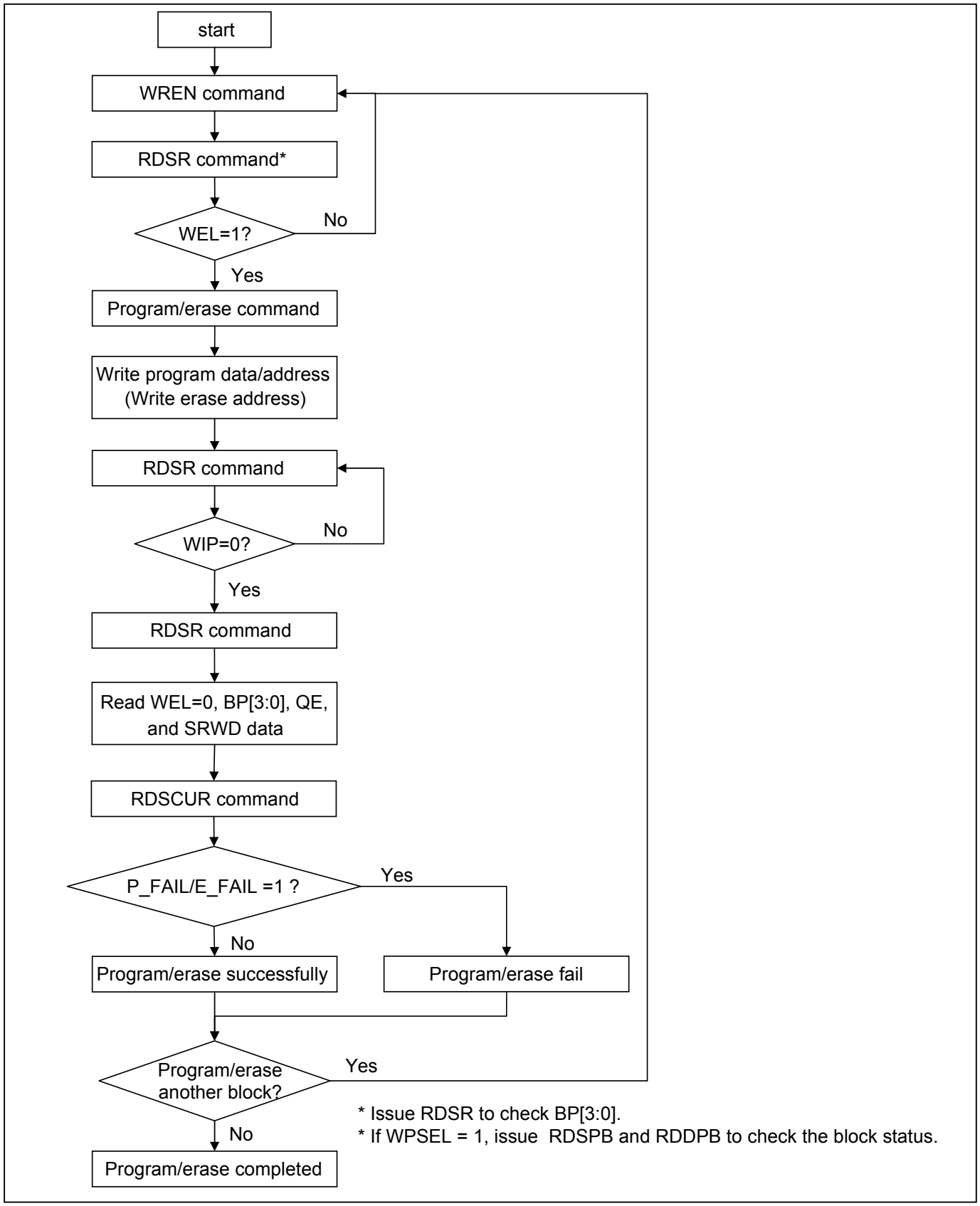
**Figure 22. Program/Erase flow with read array data**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 23. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### Status Register

The definition of the status register bits is as below:

**WIP bit.** The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

**WEL bit.** The Write Enable Latch (WEL) bit is a volatile bit that is set to "1" by the WREN instruction. WEL needs to be set to "1" before the device can accept program and erase instructions, otherwise the program and erase instructions are ignored. WEL automatically clears to "0" when a program or erase operation completes. To ensure that both WIP and WEL are "0" and the device is ready for the next program or erase operation, it is recommended that WIP be confirmed to be "0" before checking that WEL is also "0". If a program or erase instruction is applied to a protected memory area, the instruction will be ignored and WEL will clear to "0".

**BP3, BP2, BP1, BP0 bits.** The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is unprotected.

**QE bit.** The Quad Enable (QE) bit is permanently set to "1". When QE is "1", Quad mode is enabled and Quad mode commands are supported along with Single and Dual mode commands.

**SRWD bit.** The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0".

**Table 7. Status Register**

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| SRWD (status register write protect) | QE (Quad Enable) | BP3 (level of protected block) | BP2 (level of protected block) | BP1 (level of protected block) | BP0 (level of protected block) | WEL (write enable latch) | WIP (write in progress bit) |
| 1=status register write disable 0=status register write enable | 1=Quad Enabled | *(note 1)* | *(note 1)* | *(note 1)* | *(note 1)* | 1=write enable 0=not write enable | 1=write operation 0=not in write operation |
| Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | volatile bit | volatile bit |

**Note 1:** Please refer to the *"Table 2. Protected Area Sizes"*.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

**ODS bit**

The output driver strength (ODS2, ODS1, ODS0) bits are volatile bits, which indicate the output driver level (as defined in *"Table 9. Output Driver Strength Table"*) of the device. The Output Driver Strength is defaulted as 30 Ohms when delivered from factory. To write the ODS bits requires the Write Status Register (WRSR) instruction to be executed.

**TB bit**

The Top/Bottom (TB) bit is a non-volatile OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as "0", which means Top area protect. When it is set as "1", the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

**Table 8. Configuration Register Table**

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| DC1 (Dummy cycle 1) | DC0 (Dummy cycle 0) | Reserved | Reserved | TB (top/bottom selected) | ODS 2 (output driver strength) | ODS 1 (output driver strength) | ODS 0 (output driver strength) |
| *(note 2)* | *(note 2)* | x | x | 0=Top area protect 1=Bottom area protect (Default=0) | *(note 1)* | *(note 1)* | *(note 1)* |
| volatile bit | volatile bit | x | x | OTP | volatile bit | volatile bit | volatile bit |

Note 1: Please refer to *"Table 9. Output Driver Strength Table"*
Note 2: Please refer to *"Table 10. Dummy Cycle and Frequency Table (MHz)"*


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Table 9. Output Driver Strength Table**

| ODS2 | ODS1 | ODS0 | Output Driver Strength | |
|---|---|---|---|---|
| | | | Resistance (Ohm) | % |
| 0 | 0 | 0 | Reserved | - |
| 0 | 0 | 1 | 90 Ohms | 25% |
| 0 | 1 | 0 | 45 Ohms | 45% |
| 0 | 1 | 1 | 45 Ohms | 45% |
| 1 | 0 | 0 | Reserved | - |
| 1 | 0 | 1 | 15 Ohms | 100% |
| 1 | 1 | 0 | 15 Ohms | 100% |
| 1 | 1 | 1 | 30 Ohms (Default) | 75% (Default) |

**Table 10. Dummy Cycle and Frequency Table (MHz)**

| DC[1:0] | Numbers of Dummy clock cycles | Fast Read | Dual Output Fast Read | Quad Output Fast Read |
|---|---|---|---|---|
| **00 (default)** | 8 | 104 | 104 | 104 |
| **01** | 6 | 104 | 104 | 84 |
| **10** | 8 | 104 | 104 | 104 |
| **11** | 10 | 133 | 133 | 133 |

| DC[1:0] | Numbers of Dummy clock cycles | Dual IO Fast Read |
|---|---|---|
| **00 (default)** | 4 | 84 |
| **01** | 6 | 104 |
| **10** | 8 | 104 |
| **11** | 10 | 133 |

| DC[1:0] | Numbers of Dummy clock cycles | Quad IO Fast Read |
|---|---|---|
| **00 (default)** | 6 | 84 |
| **01** | 4 | 66 |
| **10** | 8 | 104 |
| **11** | 10 | 120/133R |

**Note:** "R" mean VCC range= 3.0V-3.6V.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

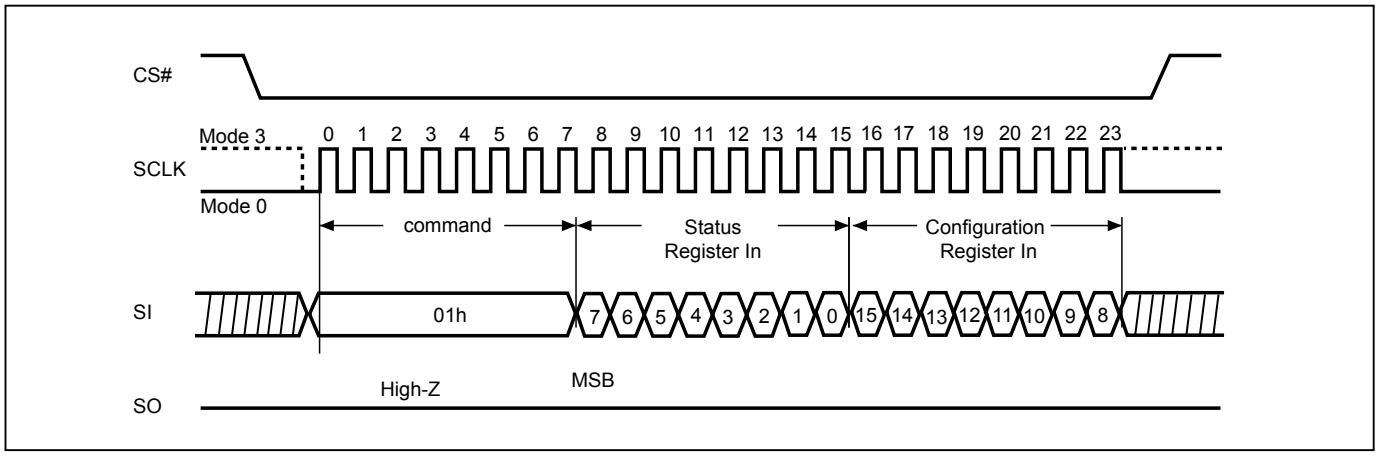
### 9-10. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 2. Protected Area Sizes"*).

The sequence of issuing WRSR instruction is: CS# goes low→ send WRSR instruction code→ Status Register data on SI→Configuration Register data on SI→CS# goes high.

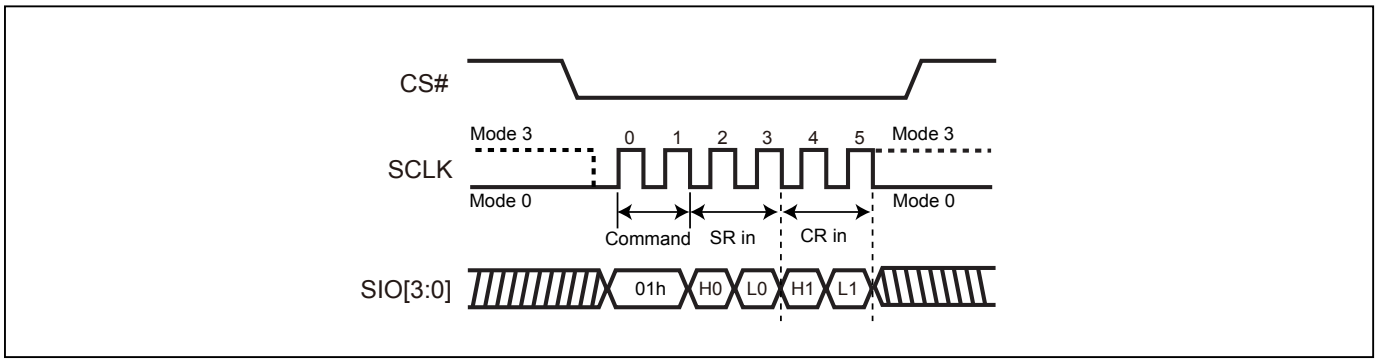
The CS# must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

**Figure 24. Write Status Register (WRSR) Sequence (SPI Mode)**




Note: The CS# must go high exactly at 8 bits or 16 bits data boundary to completed the write register command.

**Figure 25. Write Status Register (WRSR) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Software Protected Mode (SPM):**

- When SRWD bit is defaulted as 0, the WREN instruction may set the WEL bit and can change the values of BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0 and T/B bit, is at software protected mode (SPM).

**Table 11. Protection Modes**

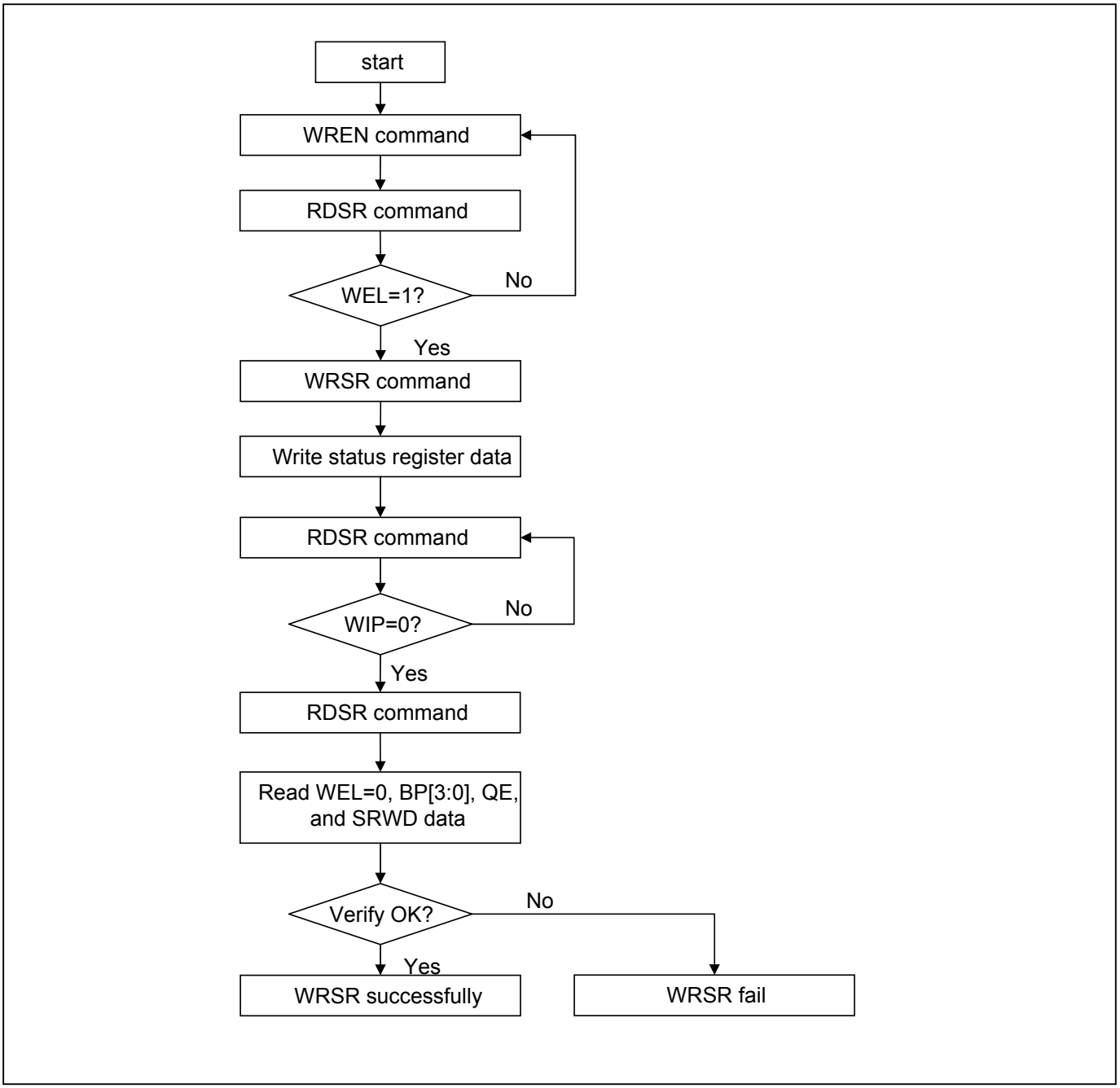
| Mode | Status register condition | SRWD bit status | Memory |
|---|---|---|---|
| Software protection mode (SPM) | Status register can be written in (WEL bit is set to "1") and BP0-BP3 bits can be changed | SRWD bit=0 | The protected area cannot be programmed or erased. |

Note:

1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 2. Protected Area Sizes"*.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 26. WRSR flow**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

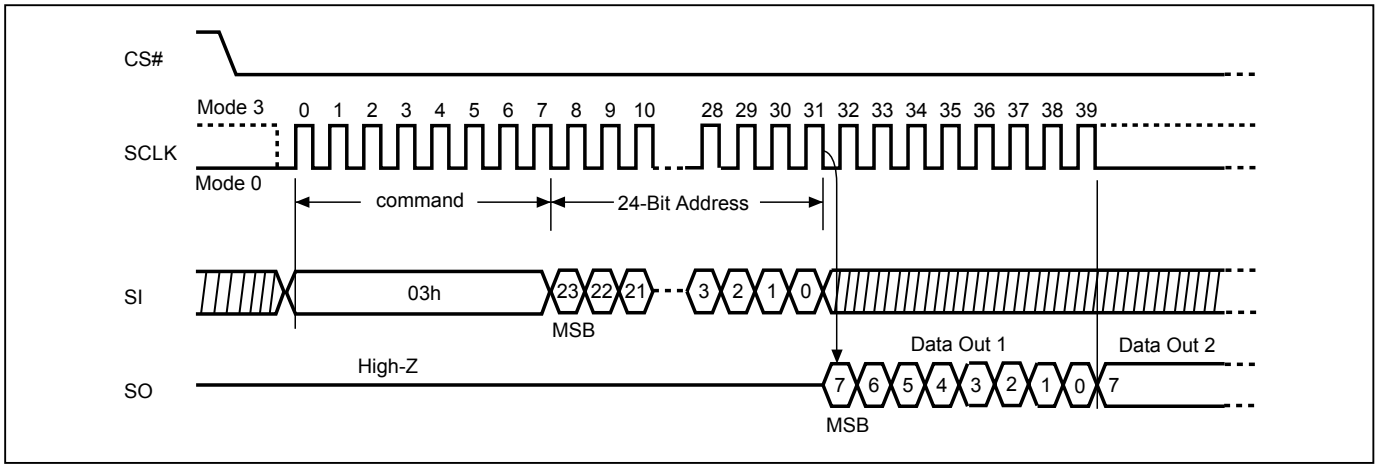
### 9-11. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

**Figure 27. Read Data Bytes (READ) Sequence (SPI Mode only)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-12. Read Data Bytes at Higher Speed (FAST_READ)

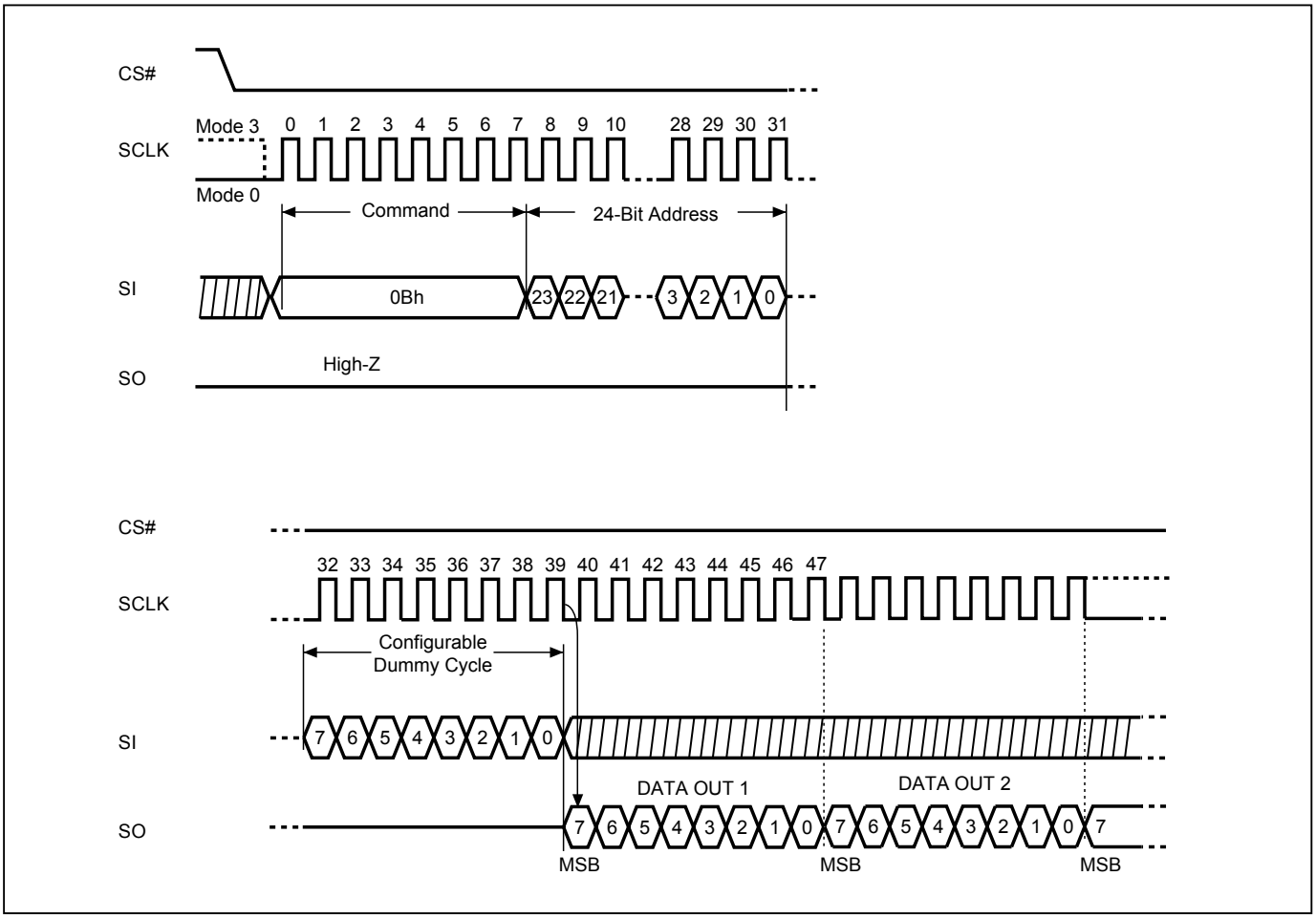
The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ send FAST_READ instruction code→ 3-byte address on SI→ 8 dummy cycles (default)→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h,5Ah,F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

**Figure 28. Read at Higher Speed (FAST_READ) Sequence (SPI Mode only)**




Notes: Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

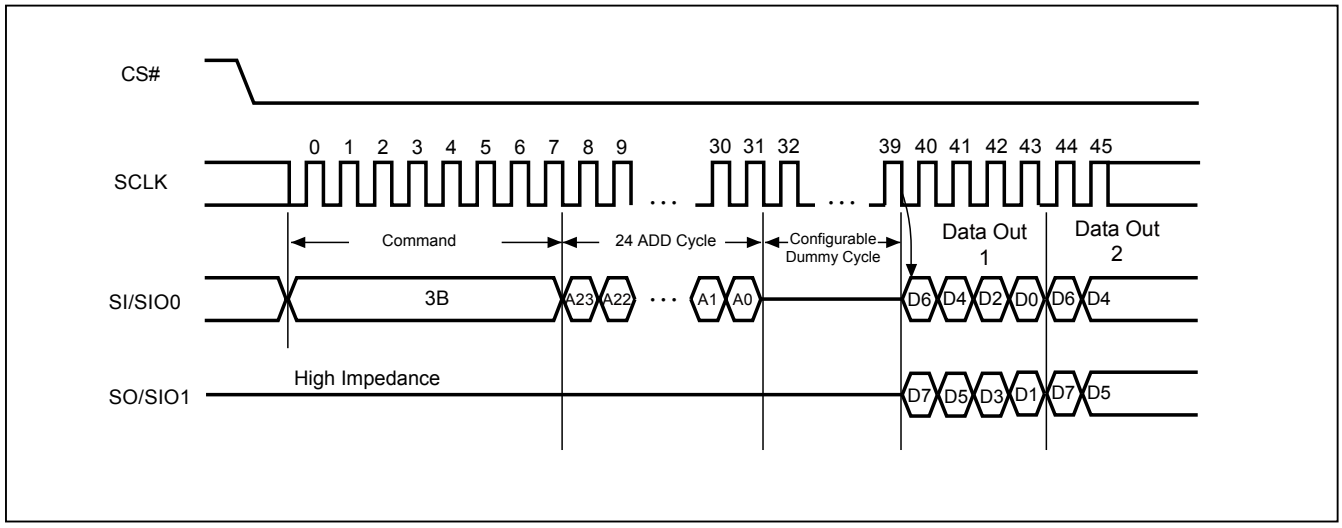
### 9-13. Dual Output Read Mode (DREAD)

The DREAD instruction enables double throughput of the Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low→ send DREAD instruction→3-byte address on SIO0→ 8 dummy cycles (default) on SIO0→ data out interleave on SIO1 & SIO0→ to end DREAD operation, raise CS# high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

**Figure 29. Dual Read Mode Sequence (SPI Mode only)**




Notes: Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

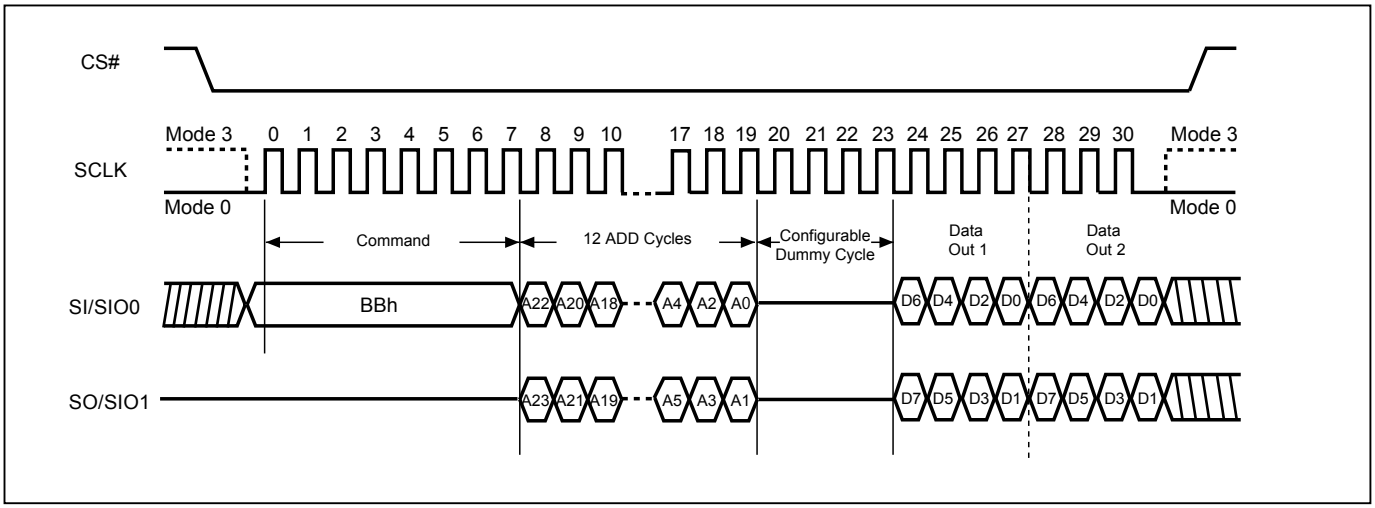
### 9-14. 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 3-byte address interleave on SIO1 & SIO0→ 4 dummy cycles (default) on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

**Figure 30. 2 x I/O Read Mode Sequence (SPI Mode only)**




Notes: Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

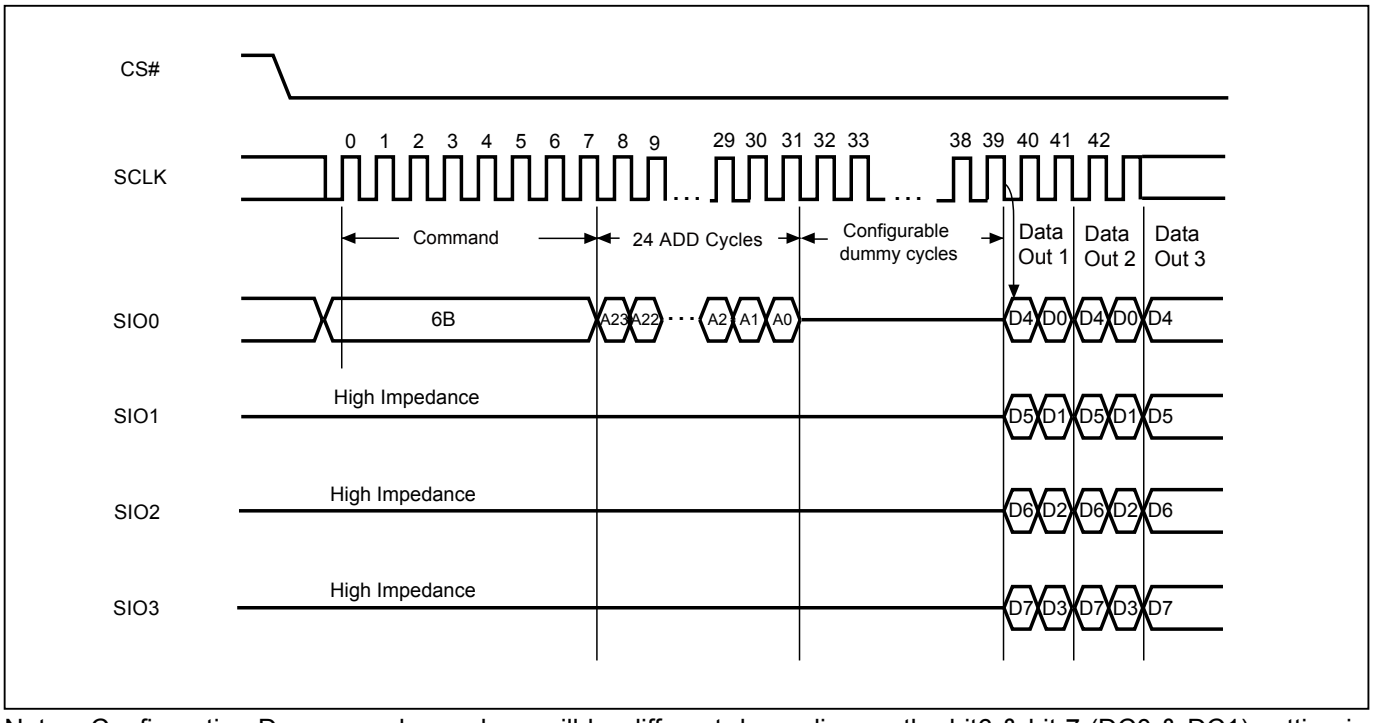
### 9-15. Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte address on SI → 8 dummy cycle (Default) → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

**Figure 31. Quad Read Mode Sequence (SPI Mode only)**




Notes: Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-16. 4 x I/O Read Mode (4READ)

The 4READ instruction enables quad throughput of the Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

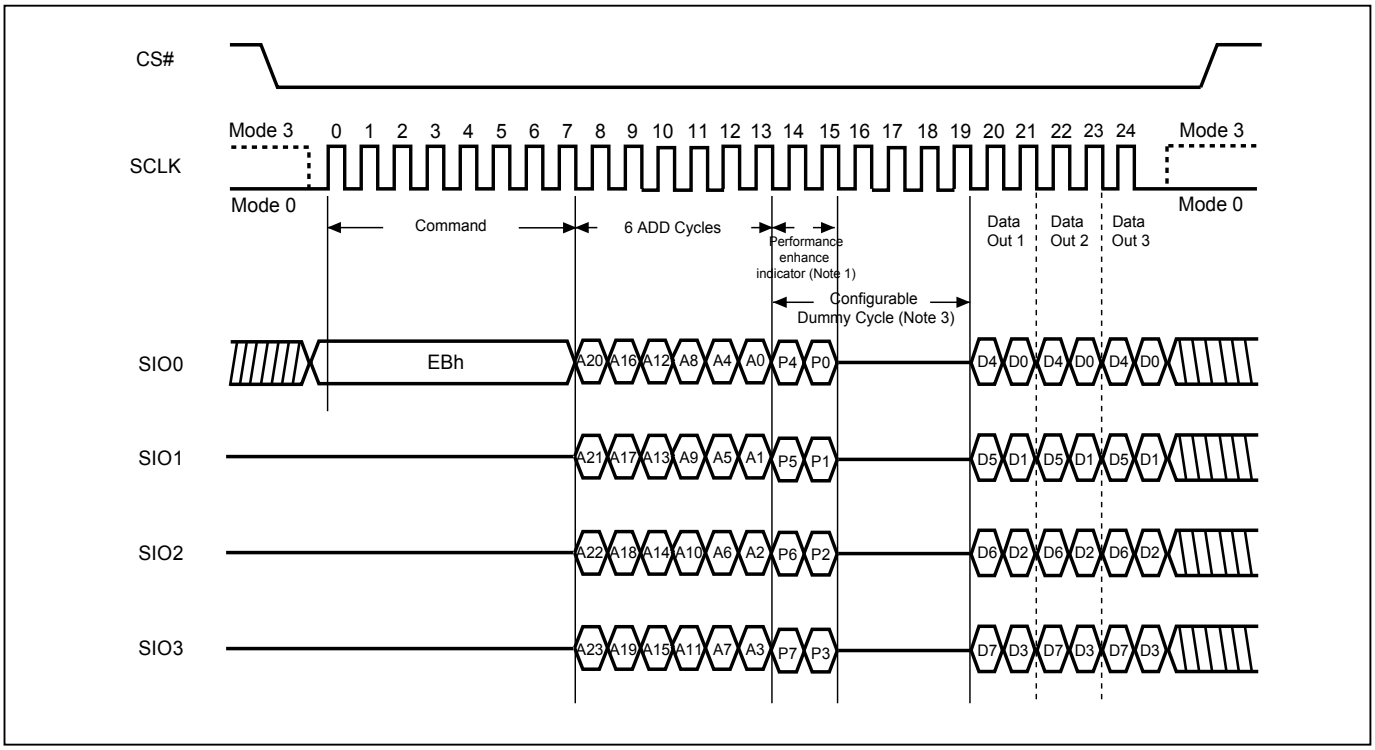
**4 x I/O Read on SPI Mode (4READ)** The sequence of issuing 4READ instruction is: CS# goes low→ send 4READ instruction→ 3-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles (Default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

**4 x I/O Read on QPI Mode (4READ)** The 4READ instruction also support on QPI command mode. The sequence of issuing 4READ instruction QPI mode is: CS# goes low→ send 4READ instruction→ 3-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles (Default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

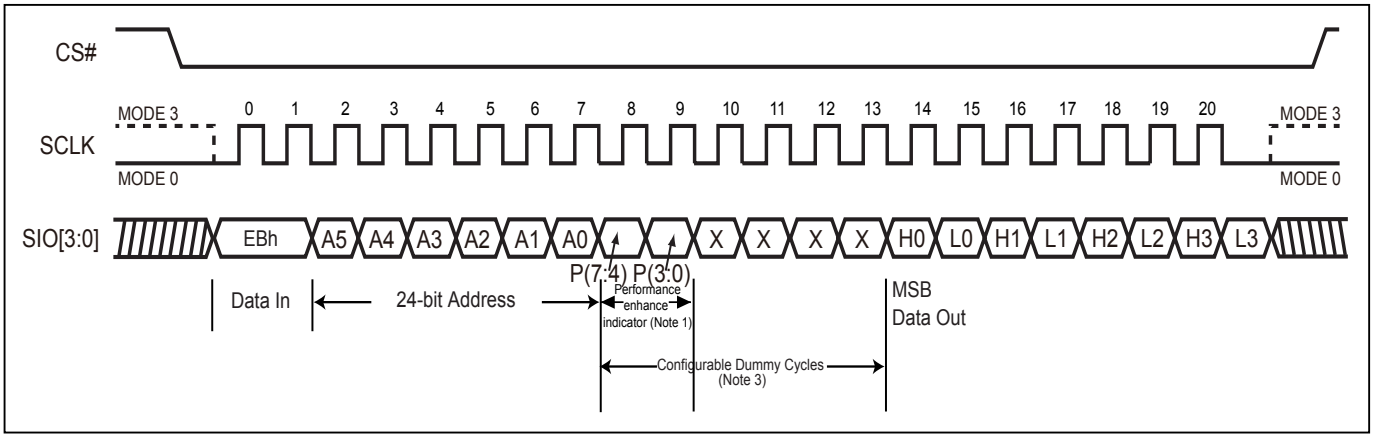

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 32. 4 x I/O Read Mode Sequence (SPI Mode)**




Notes:
1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

**Figure 33. 4 x I/O Read Mode Sequence (QPI Mode)**




Notes:
1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-17. Burst Read

The Burst Read feature allows applications to fill a cache line with a fixed length of data without using multiple read commands. Burst Read is disabled by default at power-up or reset. Burst Read is enabled by setting the Burst Length. When the Burst Length is set, reads will wrap on the selected boundary (8/16/32/64-bytes) containing the initial target address. For example if an 8-byte Wrap Depth is selected, reads will wrap on the 8-byte-page-aligned boundary containing the initial read address.

To set the Burst Length, drive CS# low → send SET BURST LENGTH instruction code (C0h) → send WRAP CODE →drive CS# high. Refer to the table below for valid 8-bit Wrap Codes and their corresponding Wrap Depth.

| Data | Wrap Around | Wrap Depth |
|---|---|---|
| 00h | Yes | 8-byte |
| 01h | Yes | 16-byte |
| 02h | Yes | 32-byte |
| 03h | Yes | 64-byte |
| 1xh | No | X |

Once Burst Read is enabled, it will remain enabled until the device is power-cycled or reset. The SPI and QPI mode 4READ read commands support the wrap around feature after Burst Read is enabled. To change the wrap depth, resend the Burst Read instruction with the appropriate Wrap Code. To disable Burst Read, send the Burst Read instruction with Wrap Code 1xh. QPI and SPI “EBh” support wrap around feature after wrap around is enabled. Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

**Figure 34. Burst Read - SPI Mode**

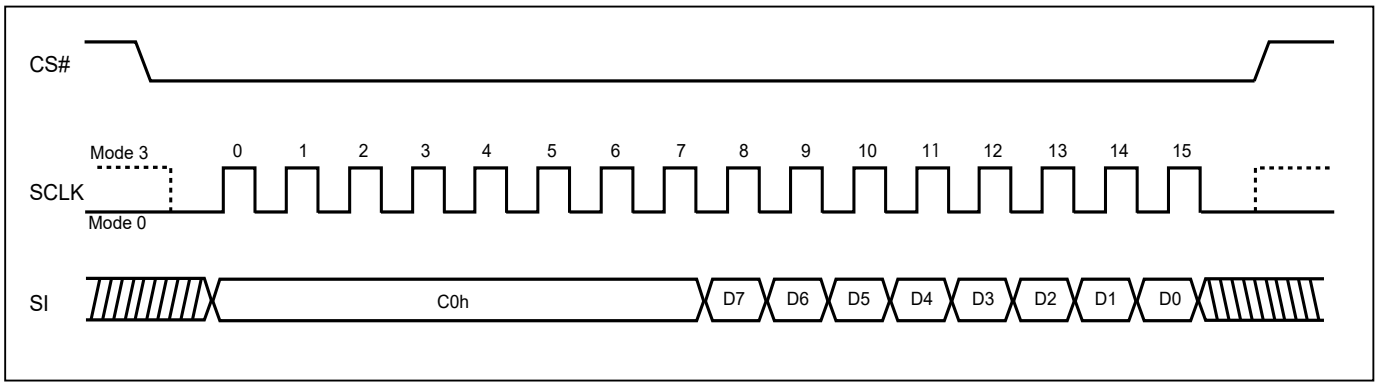
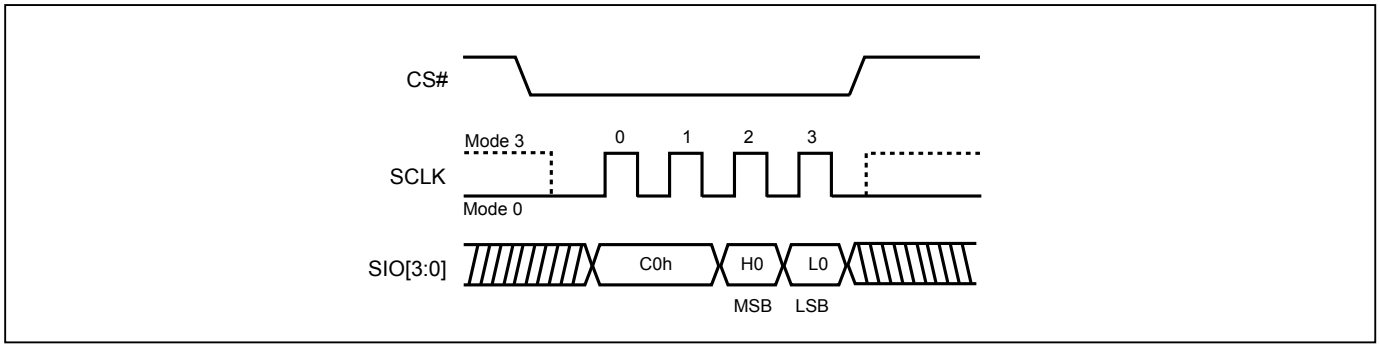



**Figure 35. Burst Read - QPI Mode**




Note: MSB=Most Significant Bit
LSB=Least Significant Bit


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-18. Performance Enhance Mode - XIP (execute-in-place)

The device could waive the command cycle bits if the two cycle bits after address cycle toggles.

Performance enhance mode is supported in both SPI and QPI mode.

In QPI mode, “EBh” and SPI “EBh” commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.

To enter performance-enhancing mode, P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and skip the next 4READ instruction. To leave enhance mode, P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h along with CS# is afterwards raised and then lowered. Issuing ”FFh” data cycle can also exit enhance mode. The system then will leave performance enhance mode and return to normal operation.

After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

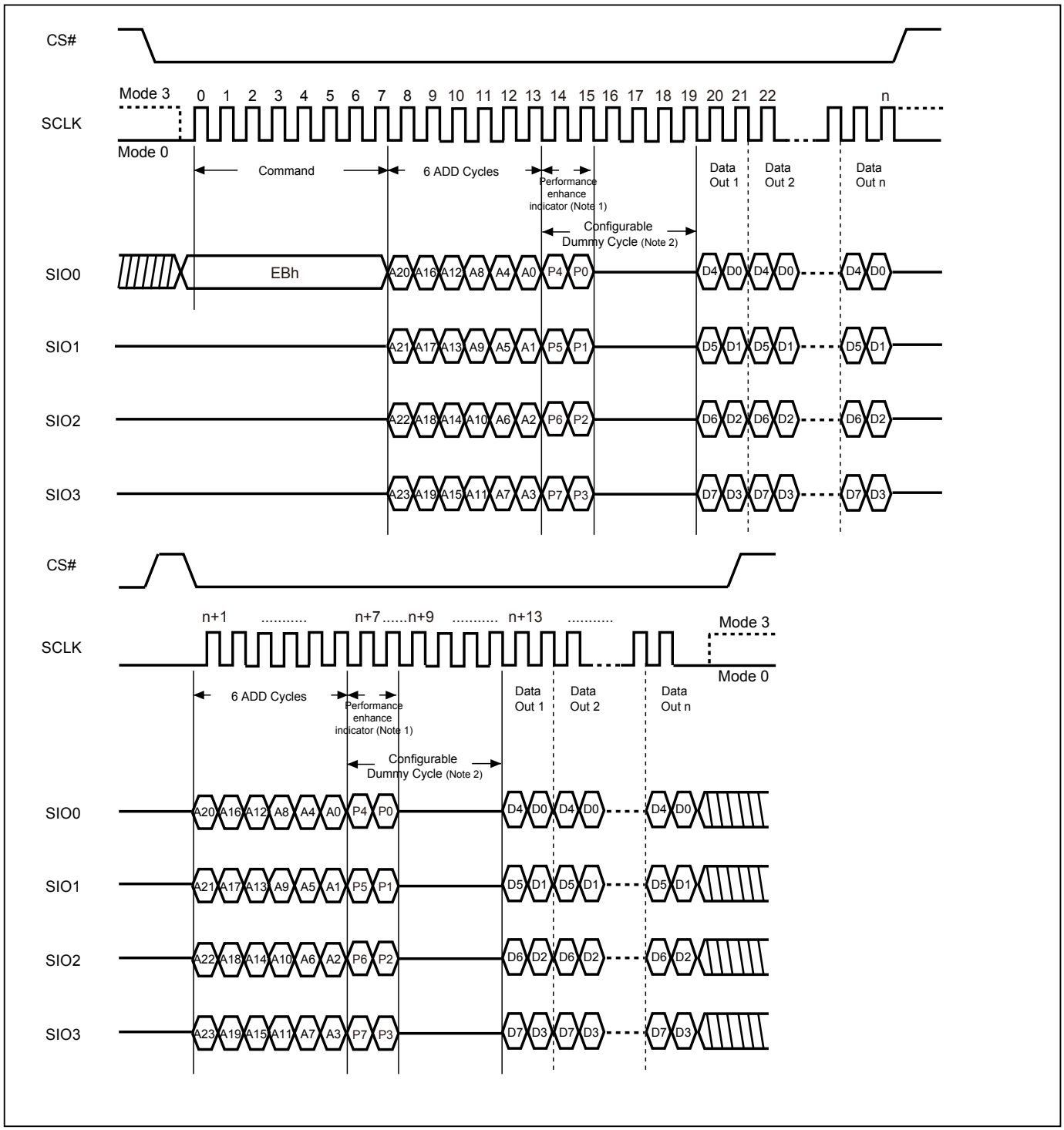
This sequence of issuing 4READ instruction is especially useful in random access: CS# goes low→send 4READ instruction→3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles (Default) →data out until CS# goes high → CS# goes low (The following 4READ instruction is not allowed, hence 8 cycles of 4READ can be saved comparing to normal 4READ mode) → 3-bytes random access address.

To conduct the Performance Enhance Mode Reset operation in SPI mode, FFh data cycle, 8 clocks, should be issued in 1I/O sequence. In QPI Mode, FFFFFFFFh data cycle, 8 clocks, in 4I/O should be issued.

If the system controller is being Reset during operation, the flash device will return to the standard SPI operation.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 36. 4 x I/O Read enhance performance Mode Sequence (SPI Mode)**

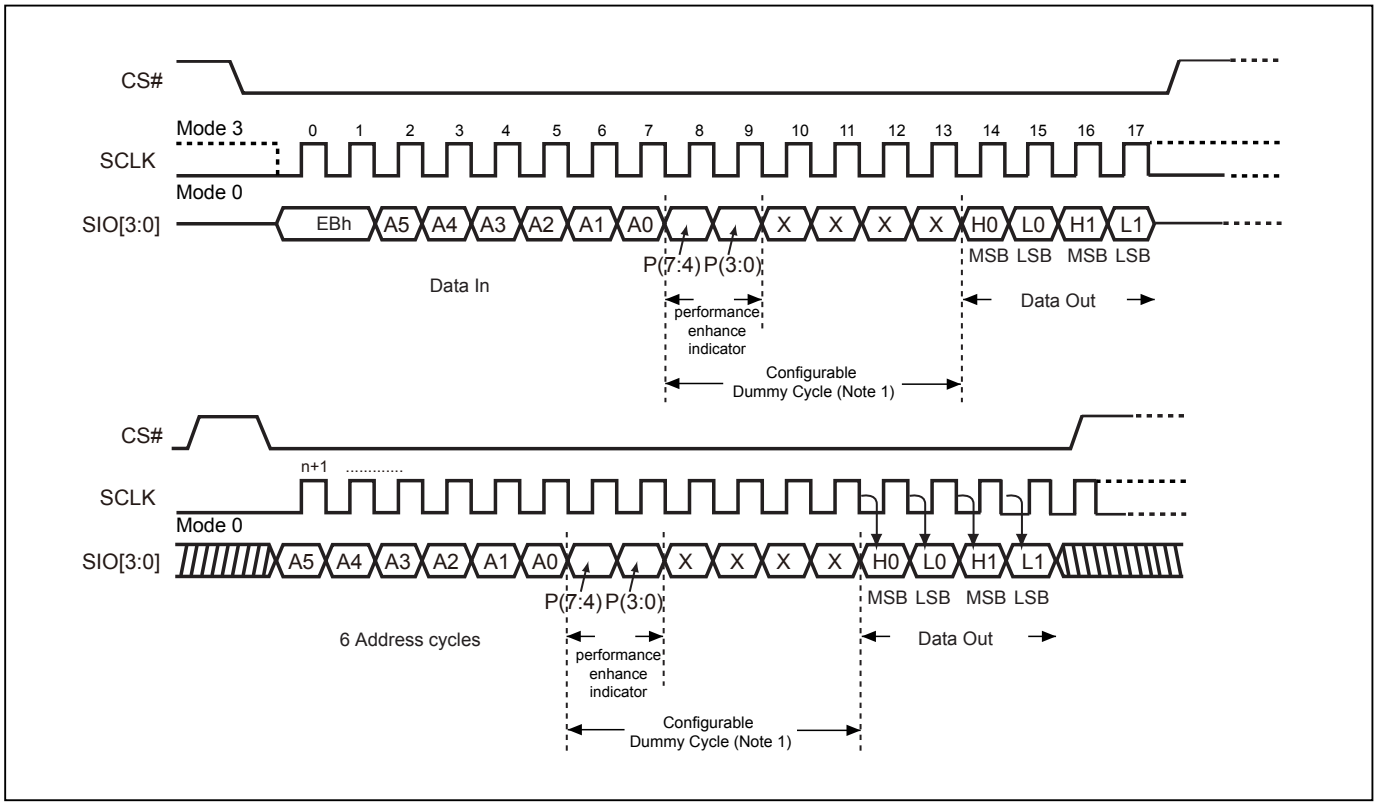



Notes:

1. If not using performance enhance recommend to keep 1 or 0 in performance enhance indicator. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 37. 4 x I/O Read enhance performance Mode Sequence (QPI Mode)**




Notes:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.
2. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-19. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (please refer to *"Table 4. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→ send SE instruction code→ 3-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (WPSEL=0; Block Lock (BP) protection mode) or SPB/DPB (WPSEL=1; Advanced Sector Protection mode), the Sector Erase (SE) instruction will not be executed on the block.

**Figure 38. Sector Erase (SE) Sequence (SPI Mode)**

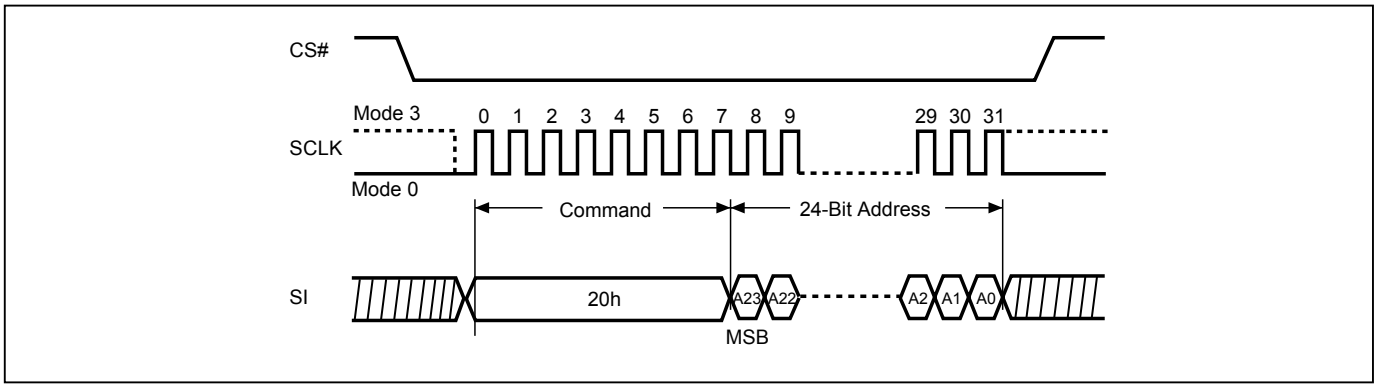
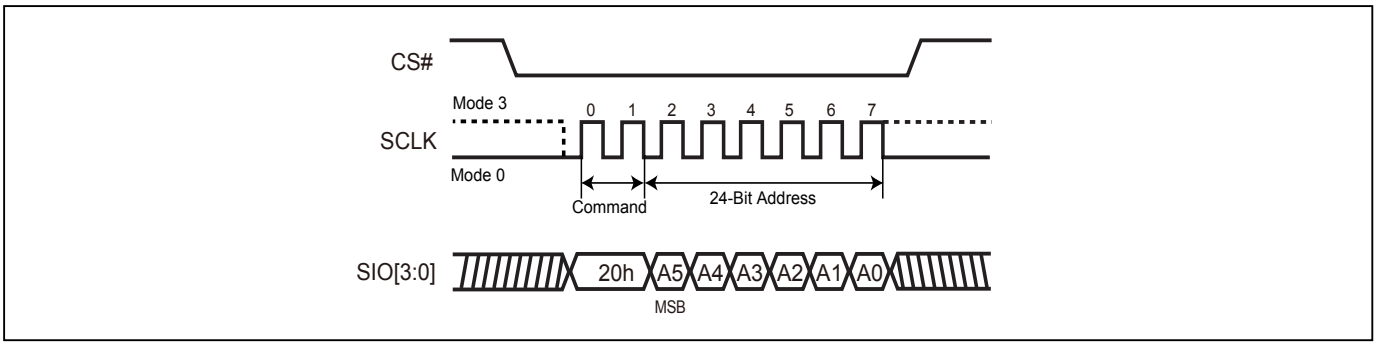



**Figure 39. Sector Erase (SE) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-20. Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (Please refer to *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low→ send BE32K instruction code→ 3-byte address on SI→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while during the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (WPSEL=0; Block Lock (BP) protection mode) or SPB/DPB (WPSEL=1; Advanced Sector Protection mode), the Block Erase (BE32K) instruction will not be executed on the block.

**Figure 40. Block Erase 32KB (BE32K) Sequence (SPI Mode)**

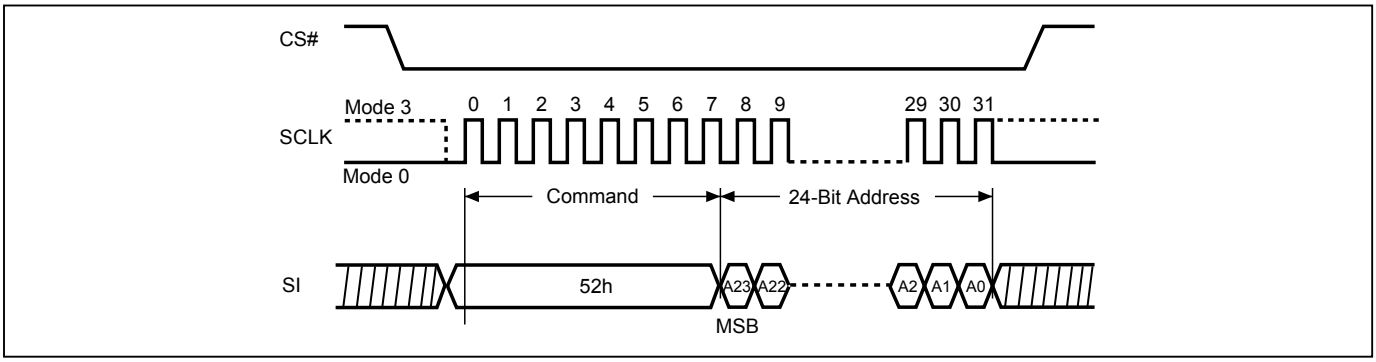
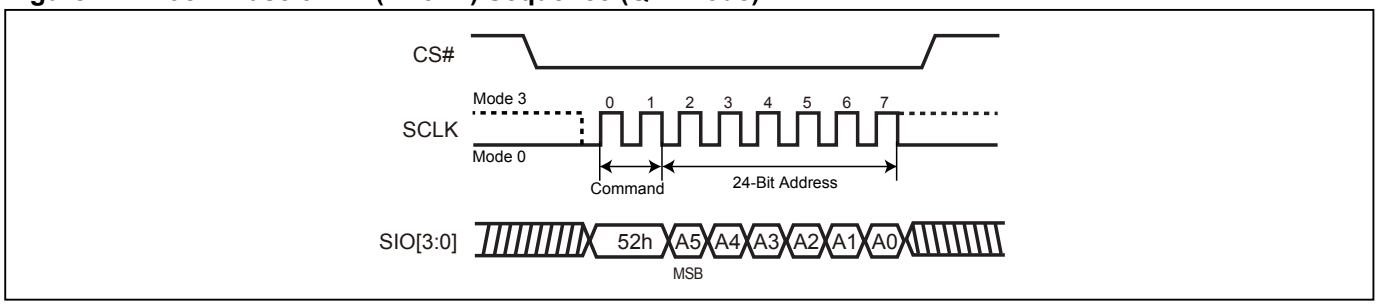



**Figure 41. Block Erase 32KB (BE32K) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-21. Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ send BE instruction code→ 3-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the Block is protected by BP bits (WPSEL=0; Block Lock (BP) protection mode) or SPB/DPB (WPSEL=1; Advanced Sector Protection mode), the Block Erase (BE) instruction will not be executed on the block.

**Figure 42. Block Erase (BE) Sequence (SPI Mode)**

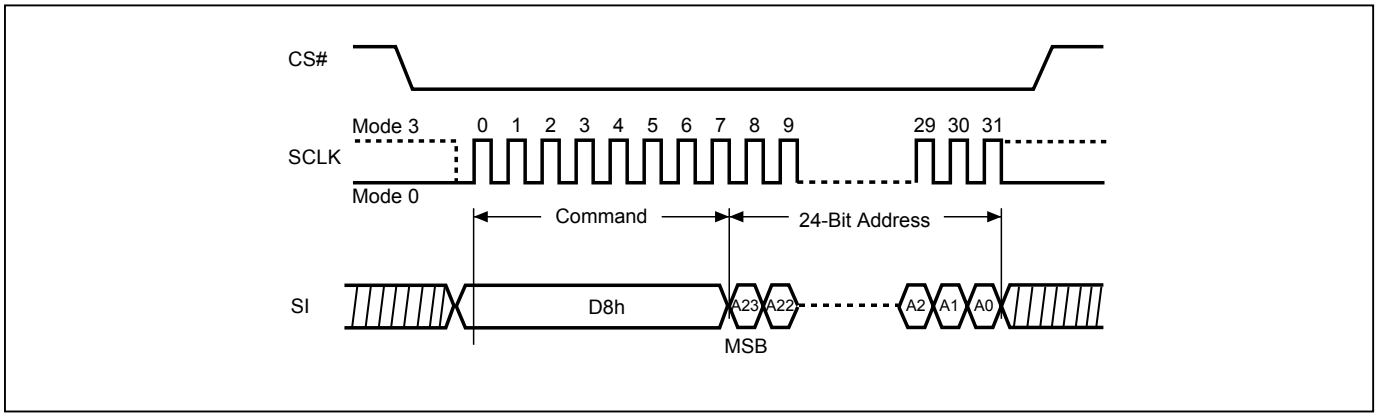
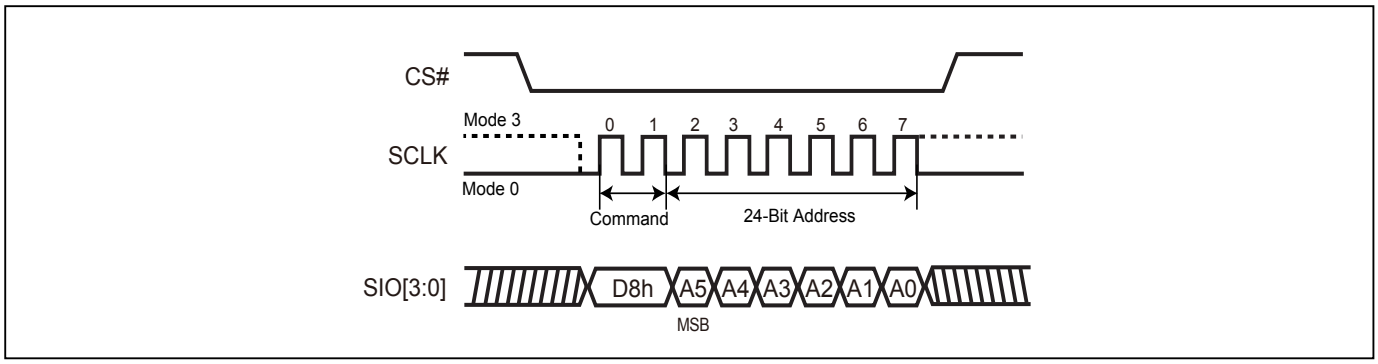



**Figure 43. Block Erase (BE) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-22. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→send CE instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

When the chip is under "Block Lock (BP) protection mode" (WPSEL=0): The Chip Erase(CE) instruction will not be executed, if one (or more) sector is protected by BP3-BP0 bits. It will be only executed when BP3-BP0 all set to "0".

When the chip is under "Advanced Sector Protection mode" (WPSEL=1): The Chip Erase (CE) instruction will be executed on unprotected block. The protected Block will be skipped. If one (or more) 4K byte sector was protected in top or bottom 64K byte block, the protected block will also skip the chip erase command.

**Figure 44. Chip Erase (CE) Sequence (SPI Mode)**

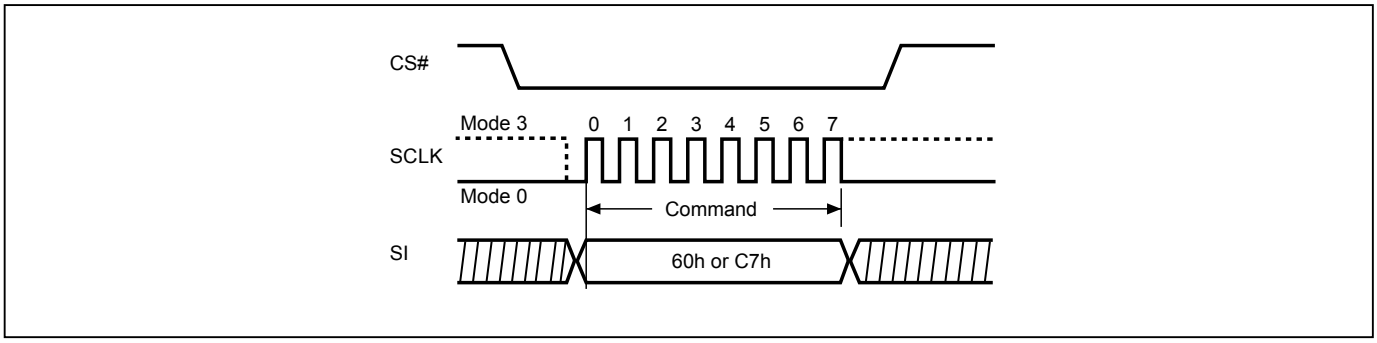
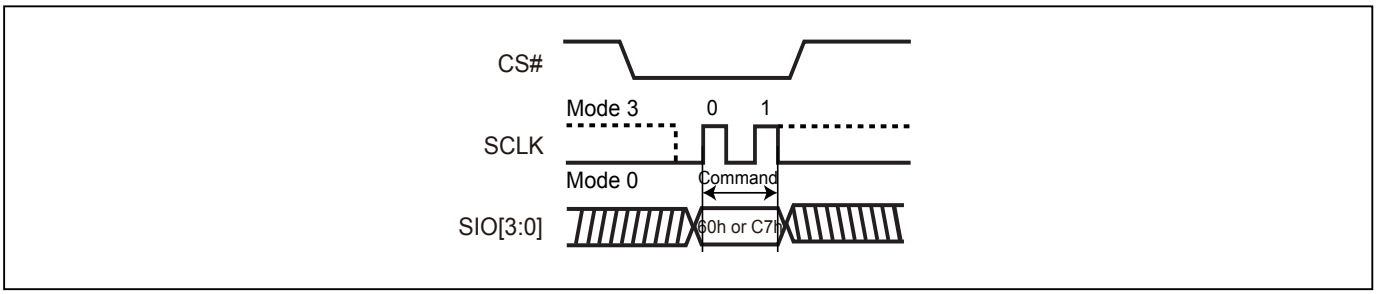



**Figure 45. Chip Erase (CE) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-23. Page Program (PP)

The Page Program (PP) instruction is for programming memory bits to "0". One to 256 bytes can be sent to the device to be programmed. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If more than 256 data bytes are sent to the device, only the last 256 data bytes will be accepted and the previous data bytes will be disregarded. The Page Program instruction requires that all the data bytes fall within the same 256-byte page. The low order address byte A[7:0] specifies the starting address within the selected page. Bytes that will cross a page boundary will wrap to the beginning of the selected page. The device can accept (256 minus A[7:0]) data bytes without wrapping. If 256 data bytes are going to be programmed, A[7:0] should be set to 0.

The sequence of issuing PP instruction is: CS# goes low→ send PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary ( the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (WPSEL=0; Block Lock (BP) protection mode) or SPB/DPB (WPSEL=1; Advanced Sector Protection mode) the Page Program (PP) instruction will not be executed.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 46. Page Program (PP) Sequence (SPI Mode)**

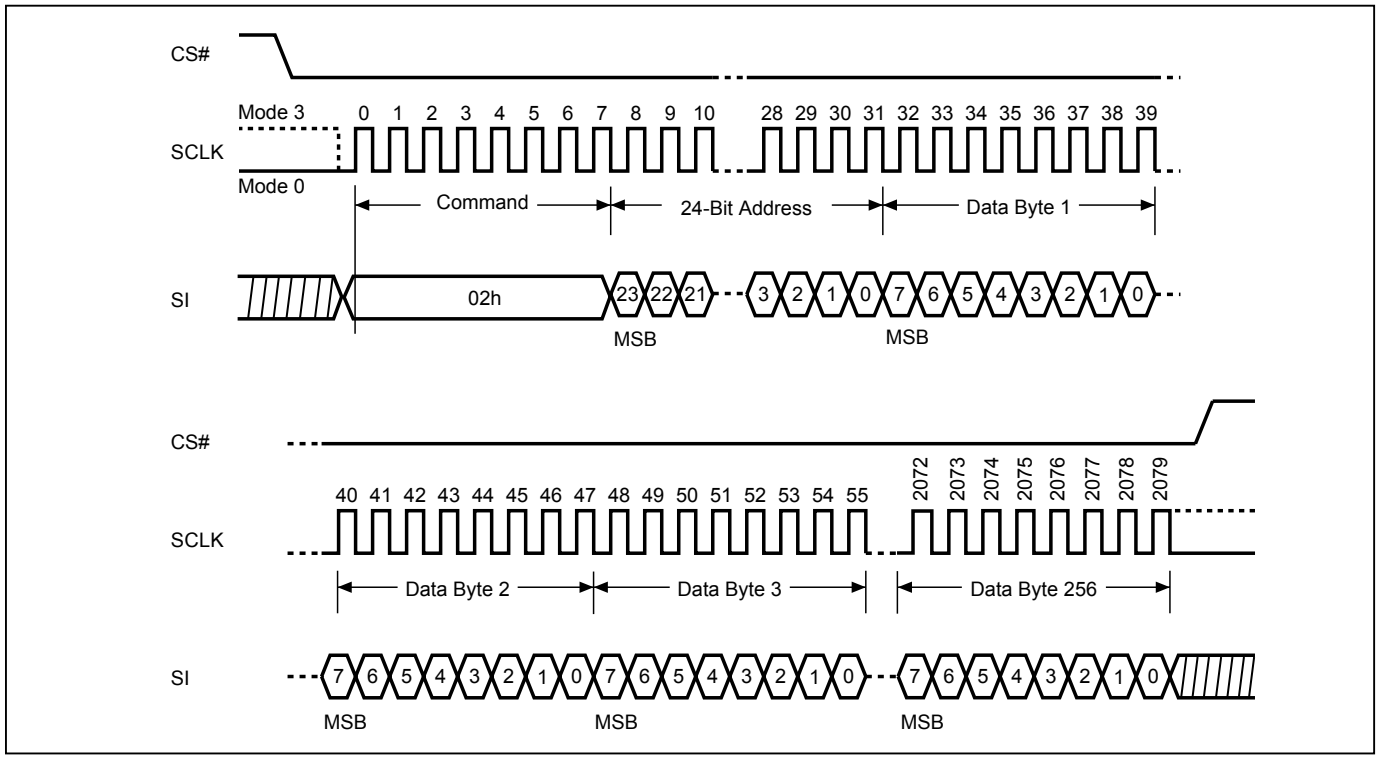
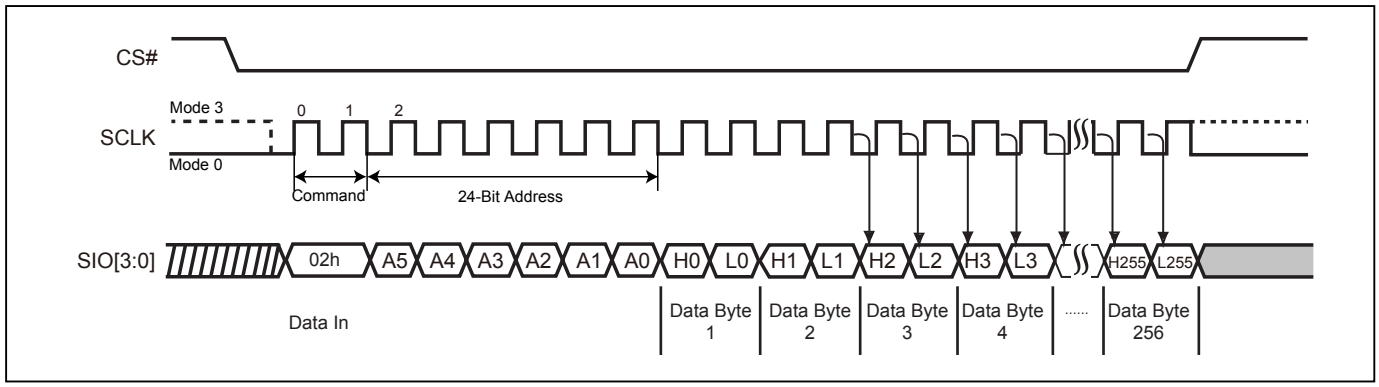



**Figure 47. Page Program (PP) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

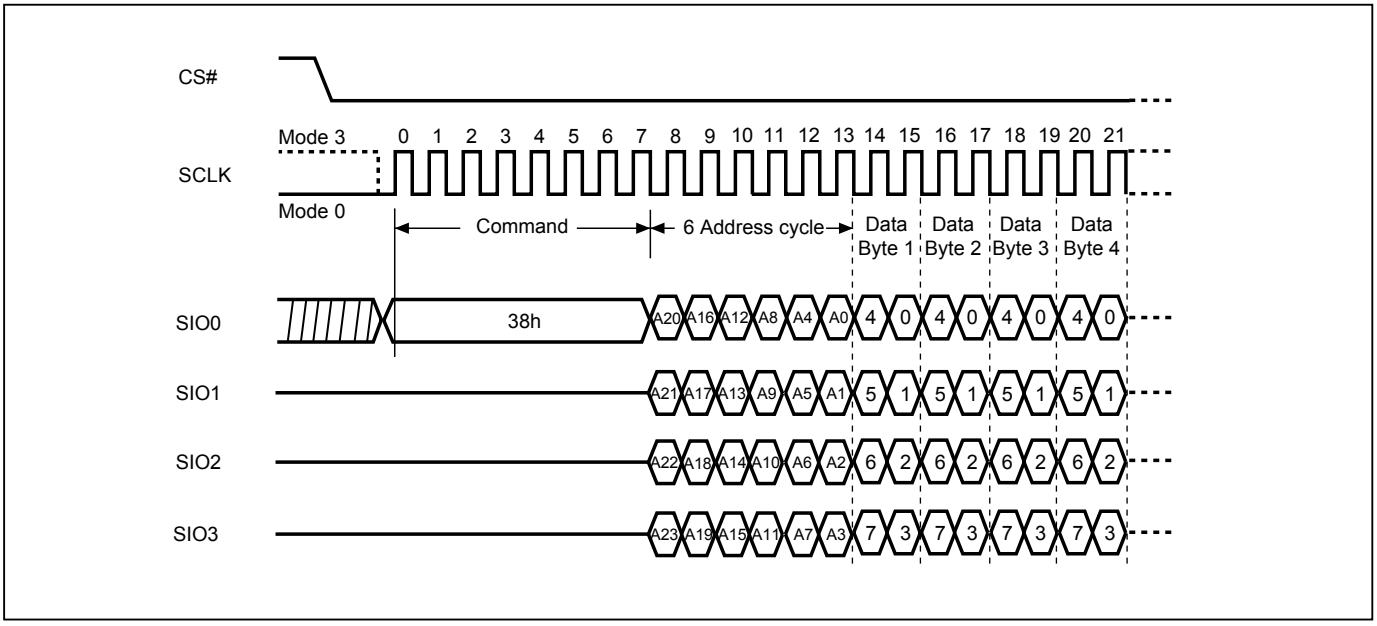
### 9-24. 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ send 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high.

If the page is protected by BP bits (WPSEL=0; Block Lock (BP) protection mode) or SPB/DPB (WPSEL=1; Advanced Sector Protection mode), the Quad Page Program (4PP) instruction will not be executed.

**Figure 48. 4 x I/O Page Program (4PP) Sequence (SPI Mode only)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-25. Deep Power-down (DP)

The Deep Power-down (DP) instruction places the device into a minimum power consumption state, Deep Power-down mode, in which the quiescent current is reduced from ISB1 to ISB2.

The sequence of issuing DP instruction: CS# goes low→ send DP instruction code→ CS# goes high. The CS# must go high at the byte boundary (after exactly eighth bits of the instruction code have been latched-in); otherwise the instruction will not be executed. Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. SIO[3:1] are "don't care".

After CS# goes high there is a delay of tDP before the device transitions from Stand-by mode to Deep Power-down mode and before the current reduces from ISB1 to ISB2. Once in Deep Power-down mode, all instructions will be ignored except Release from Deep Power-down (RDP).

The device exits Deep Power-down mode and returns to Stand-by mode if it receives a Release from Deep Powerdown (RDP) instruction, power-cycle, or reset. Please refer to *"Figure 15. Release from Deep Power-down (RDP) Sequence (SPI Mode)"* and *"Figure 16. Release from Deep Power-down (RDP) Sequence (QPI Mode)"*.

**Figure 49. Deep Power-down (DP) Sequence (SPI Mode)**

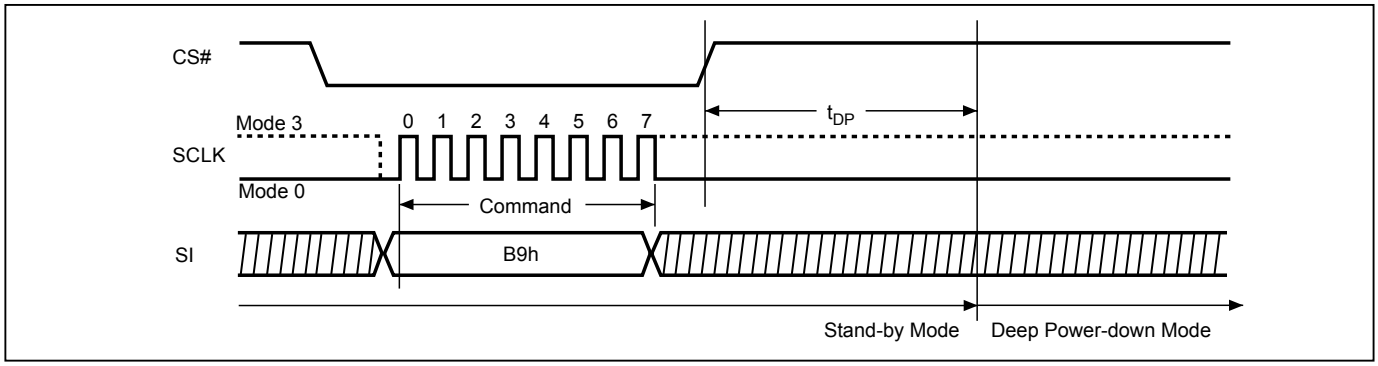
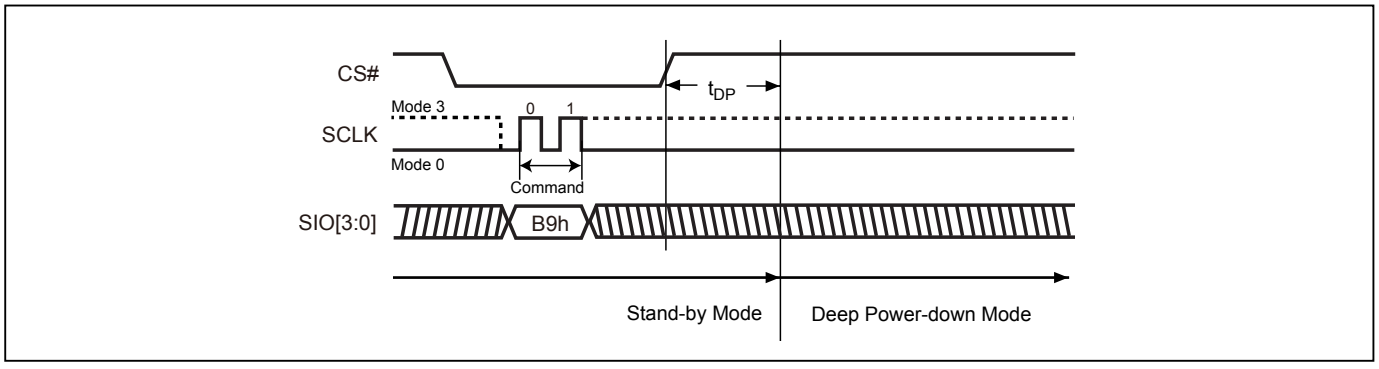



**Figure 50. Deep Power-down (DP) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-26. Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 1st 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ send WRSCUR instruction → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

**Figure 51. Write Security Register (WRSCUR) Sequence (SPI Mode)**

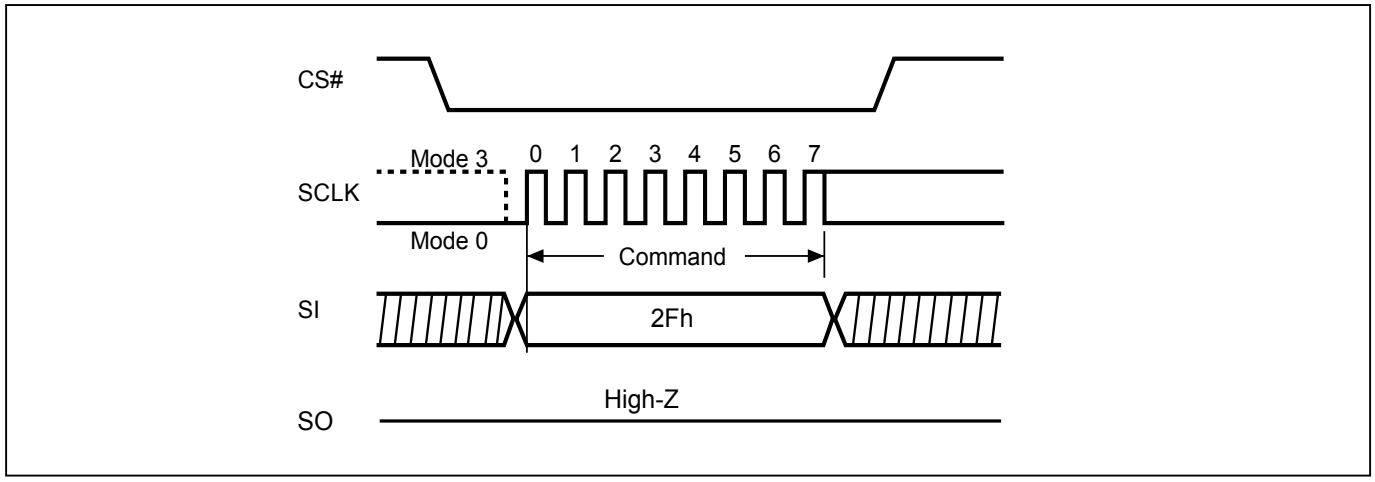
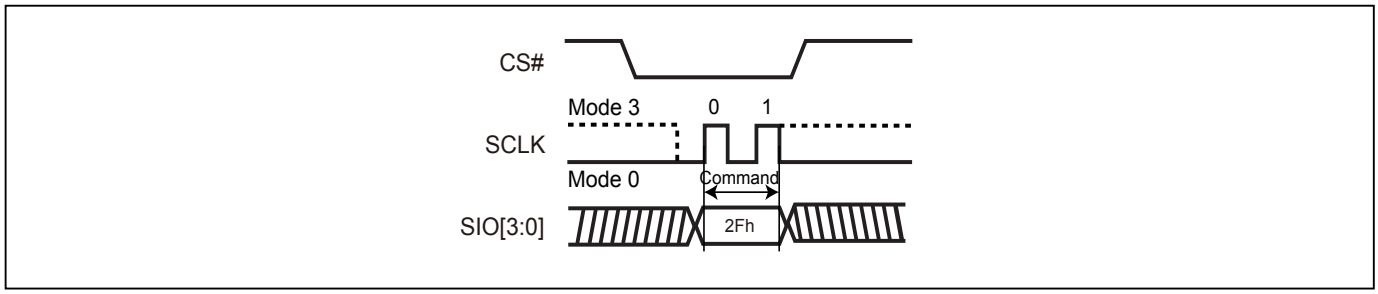



**Figure 52. Write Security Register (WRSCUR) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-27. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→send RDSCUR instruction→Security Register data out on SO→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

**Figure 53. Read Security Register (RDSCUR) Sequence (SPI Mode)**

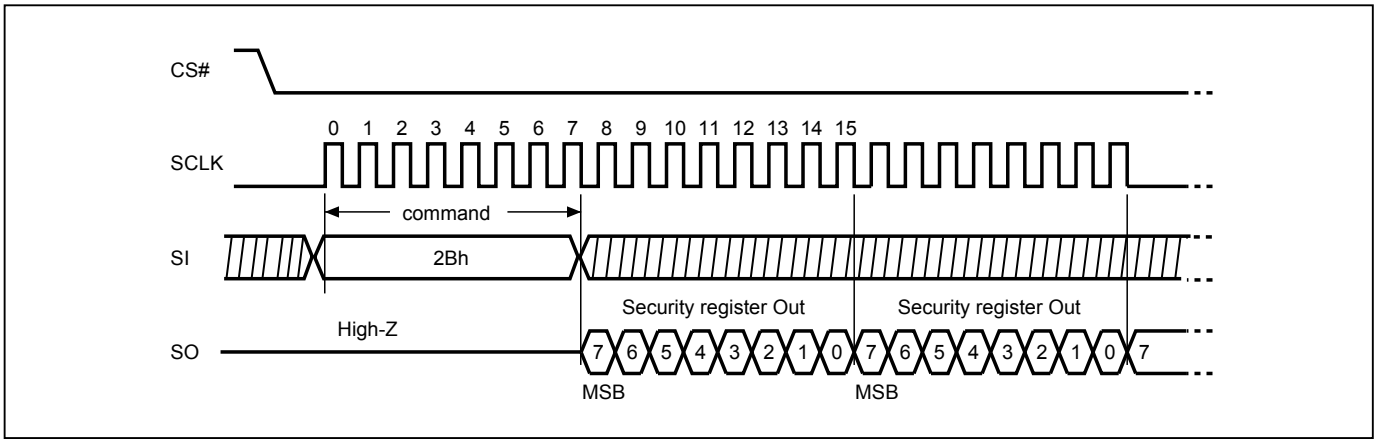
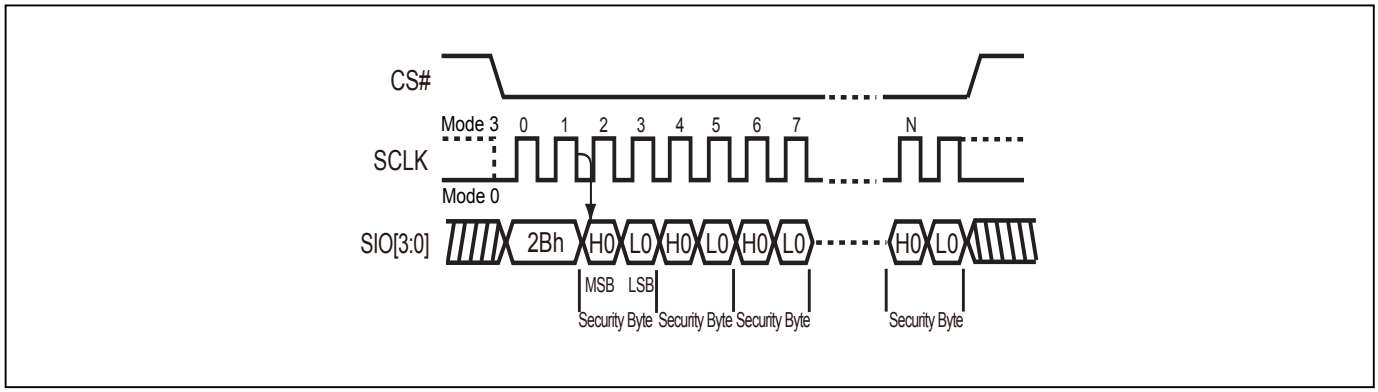



**Figure 54. Read Security Register (RDSCUR) Sequence (QPI Mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-28. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 8K-bit secured OTP mode. The additional 8K-bit secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ send ENSO instruction to enter Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

Please note that after issuing ENSO command user can only access secure OTP region with standard read or program procedure. Furthermore, once security OTP is lock down, only read related commands are valid.

### 9-29. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 8K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ send EXSO instruction to exit Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### Security Register

The definition of the Security Register bits is as below:

**Write Protection Selection bit**. Please reference to *"9-30. Write Protection Selection (WPSEL)"*.

**Erase Fail bit.** The Erase Fail bit indicates the status of last Erase operation. The bit will be set to "1" if the erase operation failed or the erase region is protected. It will be automatically cleared to "0" if the next erase operation succeeds. Please note that it does not interrupt or stop any operation in the flash memory.

**Program Fail bit.** The Program Fail bit indicates the status of last Program operation. The bit will be set to "1" if the program operation failed or the program region is protected. It will be automatically cleared to "0" if the next program operation succeeds. Please note that it does not interrupt or stop any operation in the flash memory.

**Erase Suspend bit**. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

**Program Suspend bit.** Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

**Lock-down Secured OTP (LDSO) bit.** By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 1st 4K-bit Secured OTP area cannot be updated any more. While it is in 8K-bit secured OTP mode, main array access is not allowed.

**Secured OTP Indicator bit.** The Secured OTP indicator bit shows the 2nd 4K-bit Secured OTP area is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

**Table 12. Security Register Definition**

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| WPSEL | E_FAIL | P_FAIL | Reserved | ESB (Erase Suspend bit) | PSB (Program Suspend bit) | LDSO (lock-down 1st 4K-bit Secured OTP) | Secured OTP Indicator bit (2nd 4K-bit Secured OTP) |
| 0= Block Lock (BP) protection mode 1= Advanced Sector Protection (default=0) | 0= normal Erase succeed 1= indicate Erase failed (default=0) | 0= normal Program succeed 1= indicate Program failed (default=0) | - | 0= Erase is not suspended 1= Erase suspended (default=0) | 0= Program is not suspended 1= Program suspended (default=0) | 0= not lockdown 1= lock-down (Secured OTP can no longer be programmed) | 0= nonfactory lock 1= factory lock |
| Non-volatile bit (OTP) | Volatile bit | Volatile bit | Volatile bit | Volatile bit | Volatile bit | Non-volatile bit (OTP) | Non-volatile bit (OTP) |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-30. Write Protection Selection (WPSEL)

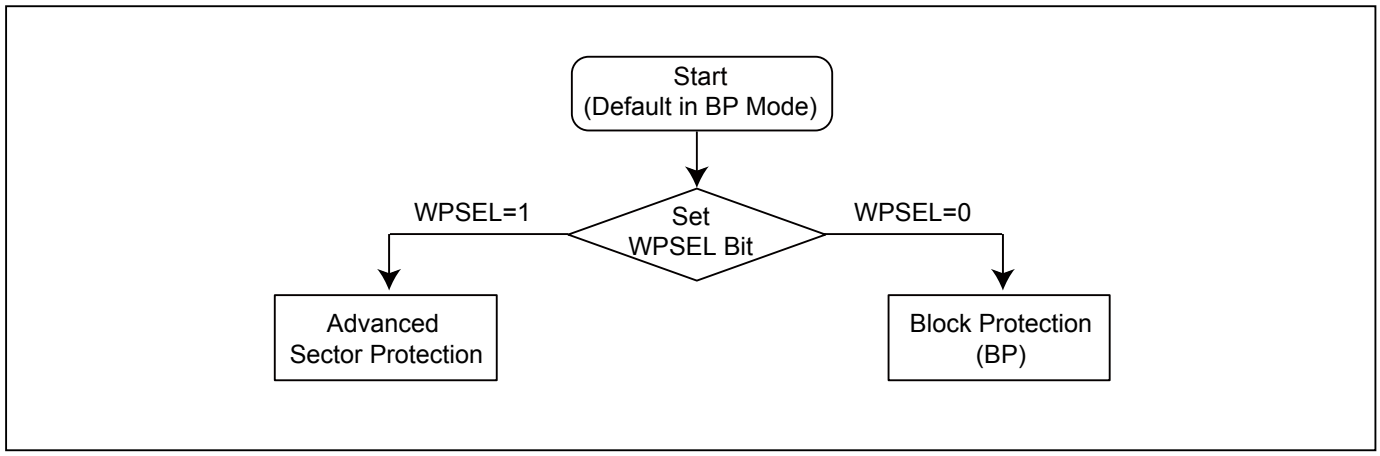
There are two write protection methods provided on this device, (1) Block Protection (BP) mode or (2) Advanced Sector Protection mode. The protection modes are mutually exclusive. The WPSEL bit selects which protection mode is enabled. If WPSEL=0 (factory default), BP mode is enabled and Individual Sector Protection mode is disabled. If WPSEL=1, Advanced Sector Protection mode is enabled and BP mode is disabled. The WPSEL command is used to set WPSEL=1. A WREN command must be executed to set the WEL bit before sending the WPSEL command. Please note that the WPSEL bit is an OTP bit. Once WPSEL is set to "1", it cannot be programmed back to "0".

When WPSEL = 0: Block Lock (BP) protection mode,
The memory array is write protected by the BP3-BP0 bits.

When WPSEL =1: Advanced Sector Protection mode,
Blocks are individually protected by their own SPB or DPB. On power-up, all blocks are write protected by the Dynamic Protection Bits (DPB) by default. The Individual Sector Protection instructions WRLR, RDLR, WRSPB, ESSPB, WRDPB, RDDPB, GBLK, and GBULK are activated. The BP3-BP0 bits of the Status Register are disabled and have no effect.

The sequence of issuing WPSEL instruction is: CS# goes low → send WPSEL instruction to enable the Individual Sector Protect mode → CS# goes high.

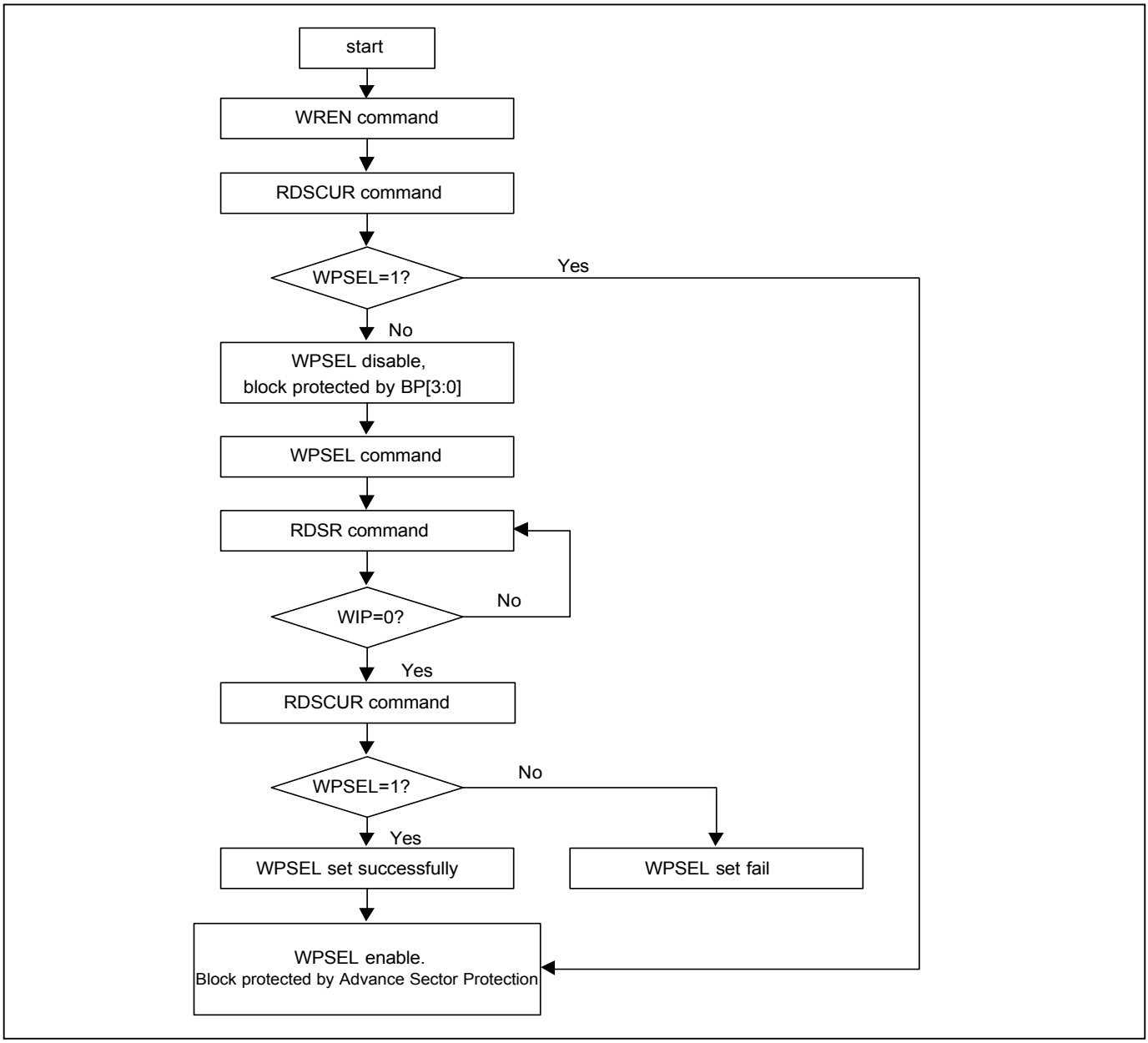
**Figure 55. Write Protection Selection**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 56. WPSEL Flow**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-31. Advanced Sector Protection

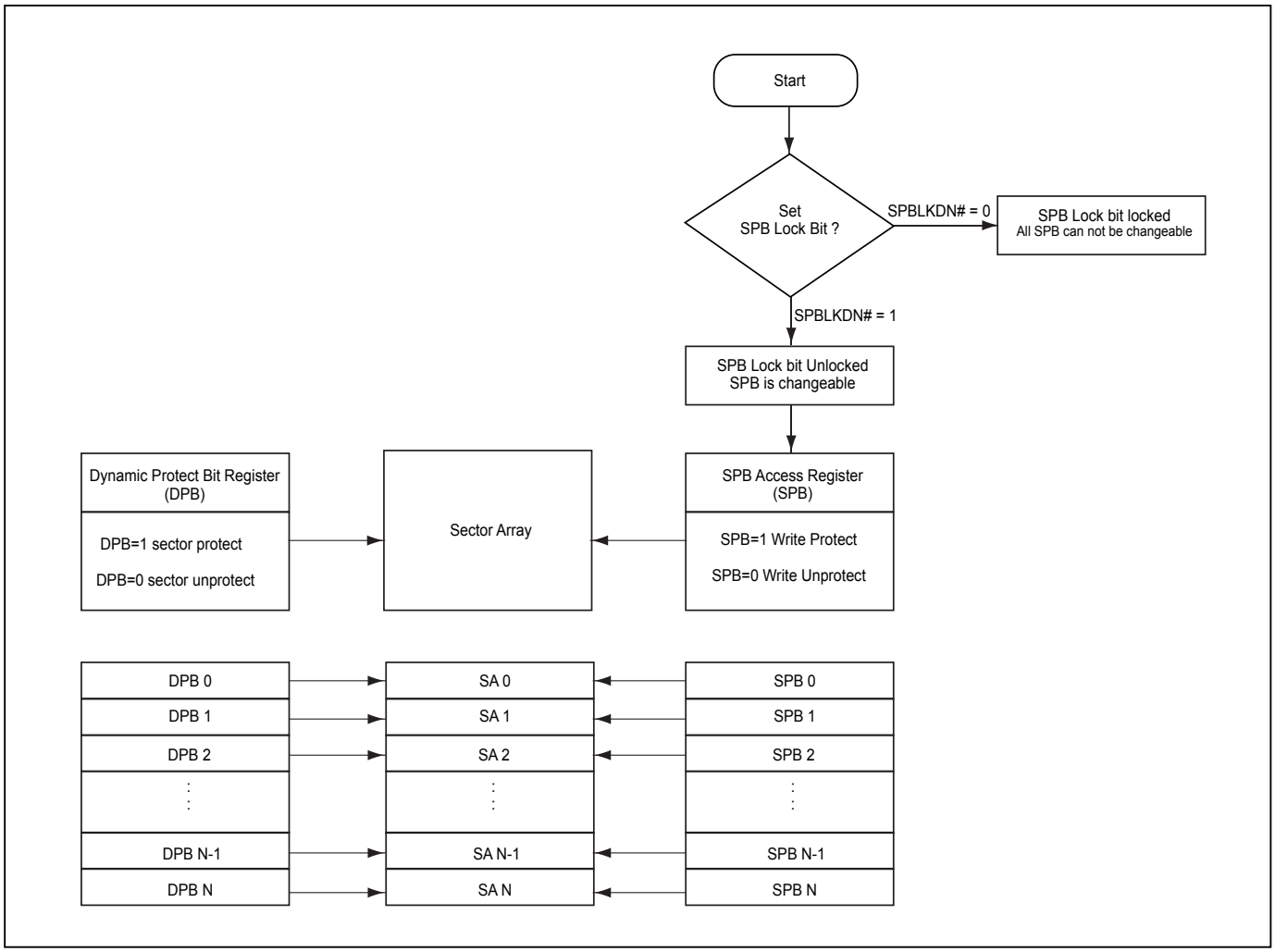
Advanced Sector Protection can protect individual 4KB sectors in the bottom and top 64KB of memory and protect individual 64KB blocks in the rest of memory.

There is one non-volatile Solid Protection Bit (SPB) and one volatile Dynamic Protection Bit (DPB) assigned to each 4KB sector at the bottom and top 64KB of memory and to each 64KB block in the rest of memory. A sector or block is write-protected from programming or erasing when its associated SPB or DPB is set to “1”.

The figure below helps describing an overview of these methods. The device is default to the Solid mode when shipped from factory. The detail algorithm of advanced sector protection is shown as follows:

Solid Protection mode permits the SPB bits to be modified after power-on or a reset. The figure below is an overview of Advanced Sector Protection.

**Figure 57. Advanced Sector Protection Overview**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-31-1. Lock Register

The Lock Register is a 16-bit one-time programmable register. Lock Register bit [6] is SPB Lock Down Bit (SPBLKDN) which is an unique bit assigned to control all SPB bit status.

When SPBLKDN is 1, SPB can be changed. When it is locked as 0, all SPB can not be changed anymore, and SPBLKDN bit itself can not be altered anymore, either.

The Lock Register is programmed using the WRLR (Write Lock Register) command. A WREN command must be executed to set the WEL bit before sending the WRLR command.

**Table 13. Lock Register**

| Bits | Field Name | Function | Type | Default State | Description |
|---|---|---|---|---|---|
| 15 to 7 | RFU | Reserved | OTP | 1 | Reserved for Future Use |
| 6 | SPBLKDN | SPB Lock Down | OTP | 1 | 1 = SPB changeable<br>0 = freeze SPB |
| 5 to 0 | RFU | Reserved | OTP | 1 | Reserved for Future Use |

**Figure 58. Read Lock Register (RDLR) Sequence**

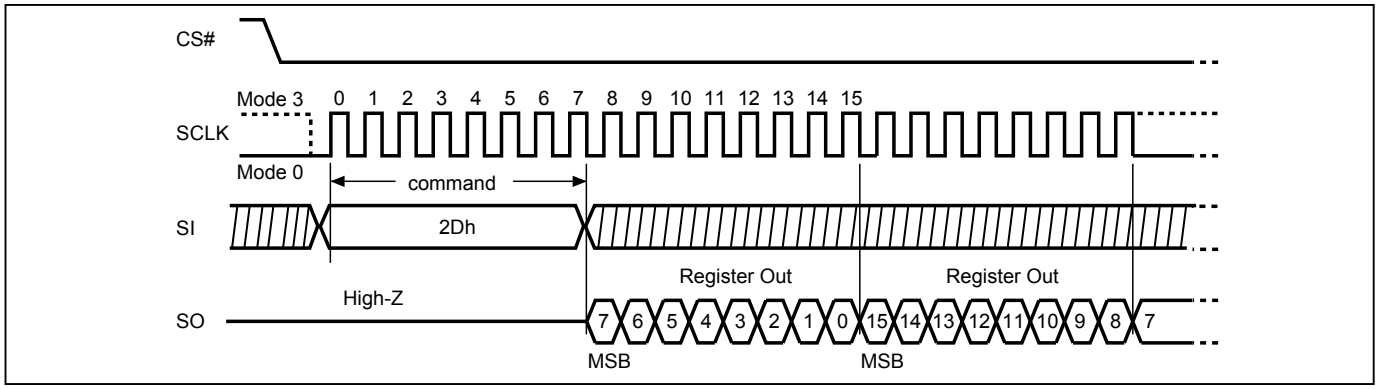
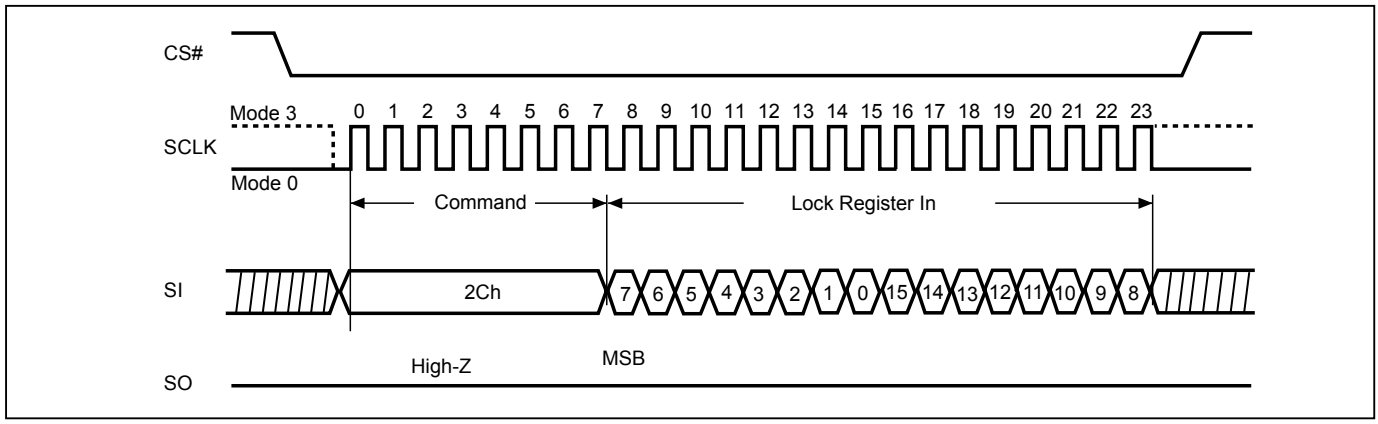



**Figure 59. Write Lock Register (WRLR) Sequence**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-31-2. Solid Protection Bits

The Solid Protection Bits (SPBs) are nonvolatile bits for enabling or disabling write-protection to sectors and blocks. The SPB bits have the same endurance as the Flash memory. An SPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the remaining memory. The factory default state of the SPB bits is “0”, which has the sector/block write-protection disabled.

When an SPB is set to “1”, the associated sector or block is write-protected. Program and erase operations on the sector or block will be inhibited. SPBs can be individually set to “1” by the WRSPB command. However, the SPBs cannot be individually cleared to “0”. Issuing the ESSPB command clears all SPBs to “0”. A WREN command must be executed to set the WEL bit before sending the WRSPB or ESSPB command.

The RDSPB command reads the status of the SPB of a sector or block. The RDSPB command returns 00h if the SPB is “0”, indicating write-protection is disabled. The RDSPB command returns FFh if the SPB is “1”, indicating write-protection is enabled.

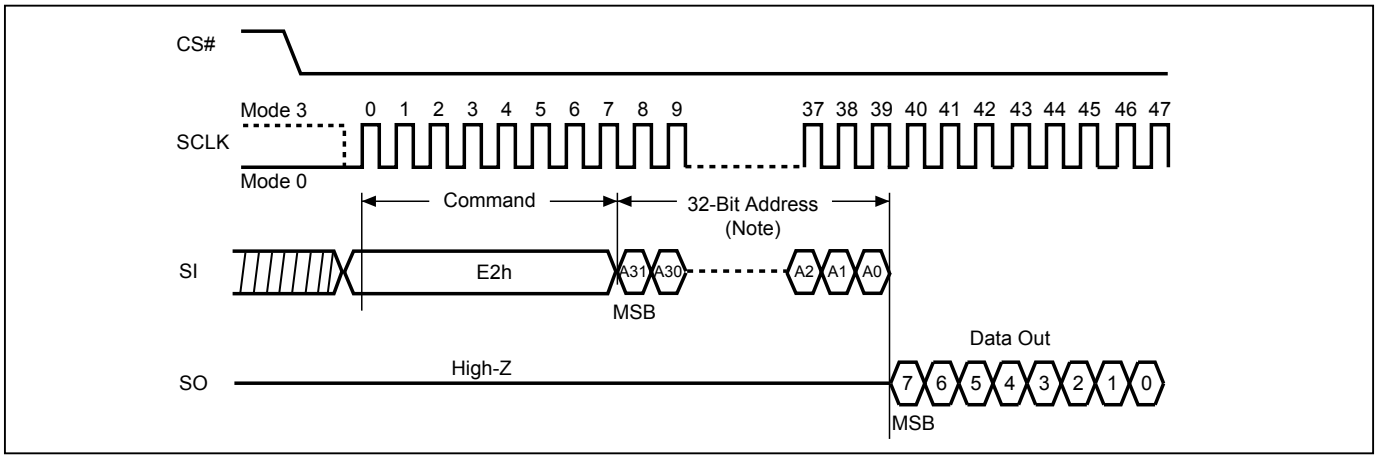
***Note:*** If SPBLKDN=0, commands to set or clear the SPB bits will be ignored.

**Table 14. SPB Register**

| Bit | Description | Bit Status | Default | Type |
|---|---|---|---|---|
| 7 to 0 | SPB (Solid Protection Bit) | 00h = Unprotect Sector / Block<br>FFh = Protect Sector / Block | 00h | Non-volatile |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 60. Read SPB Status (RDSPB) Sequence**




**Note:** A31-A24 are don't care.

**Figure 61. SPB Erase (ESSPB) Sequence**

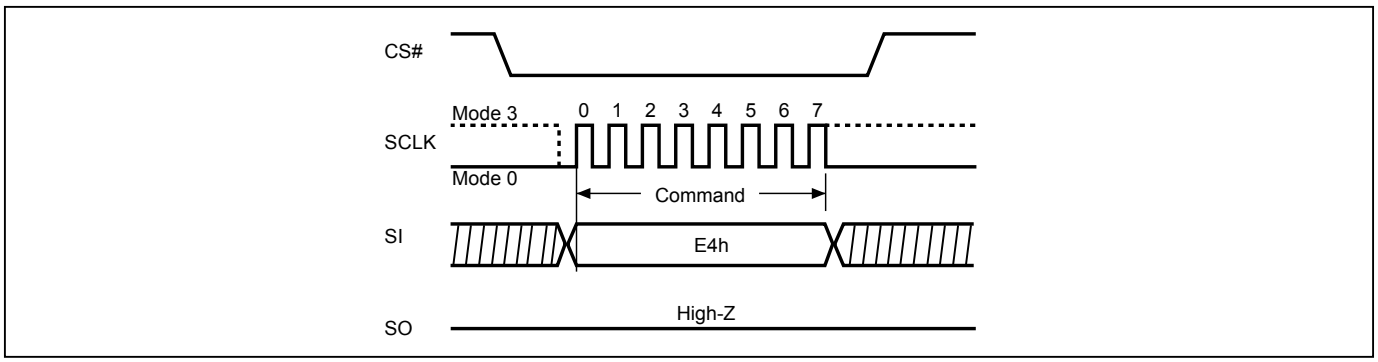
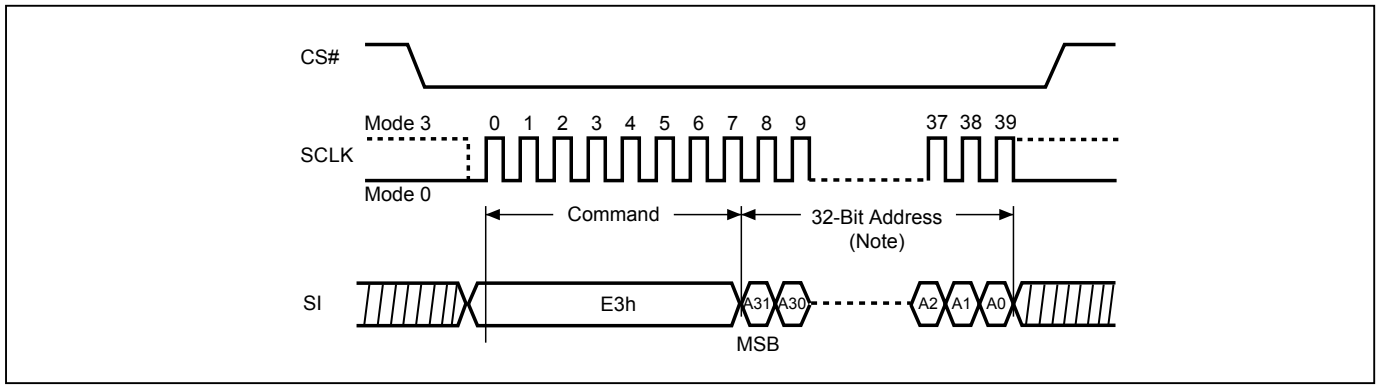



**Figure 62. SPB Program (WRSPB) Sequence**




**Note:** A31-A24 are don't care


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-31-3. Dynamic Protection Bits

The Dynamic Protection Bits (DPBs) are volatile bits for quickly and easily enabling or disabling write-protection to sectors and blocks. A DPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the rest of the memory. The DBPs can enable write-protection on a sector or block regardless of the state of the corresponding SPB. However, the DPB bits can only unprotect sectors or blocks whose SPB bits are "0" (unprotected).

When a DPB is "1", the associated sector or block will be write-protected, preventing any program or erase operation on the sector or block. All DPBs default to "1" after power-on or reset. When a DPB is cleared to "0", the associated sector or block will be unprotected if the corresponding SPB is also "0".

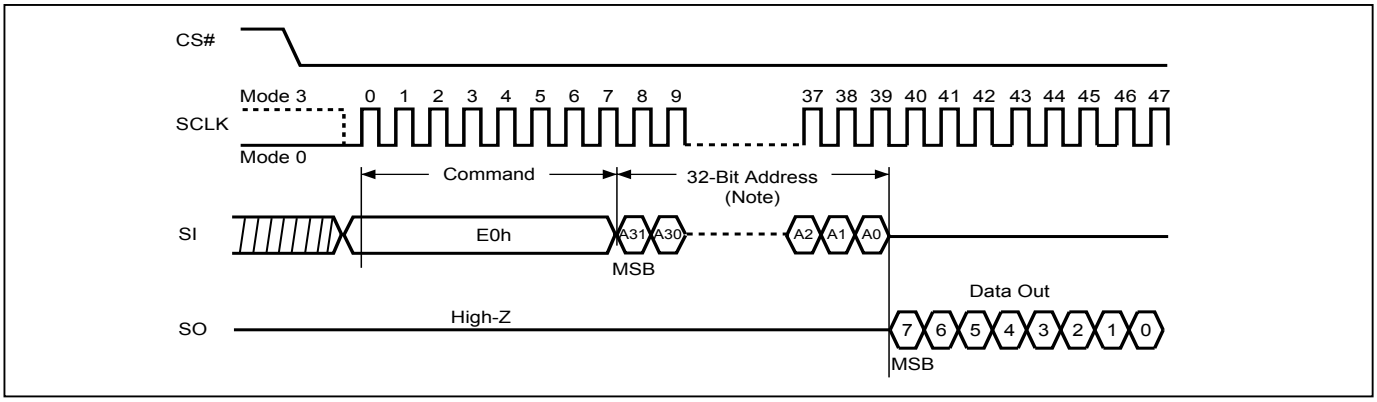
DPB bits can be individually set to "1" or "0" by the WRDPB command. The DBP bits can also be globally cleared to "0" with the GBULK command or globally set to "1" with the GBLK command. A WREN command must be executed to set the WEL bit before sending the WRDPB, GBULK, or GBLK command.

The RDDPB command reads the status of the DPB of a sector or block. The RDDPB command returns 00h if the DPB is "0", indicating write-protection is disabled. The RDDPB command returns FFh if the DPB is "1", indicating write-protection is enabled.

**Table 15. DPB Register**

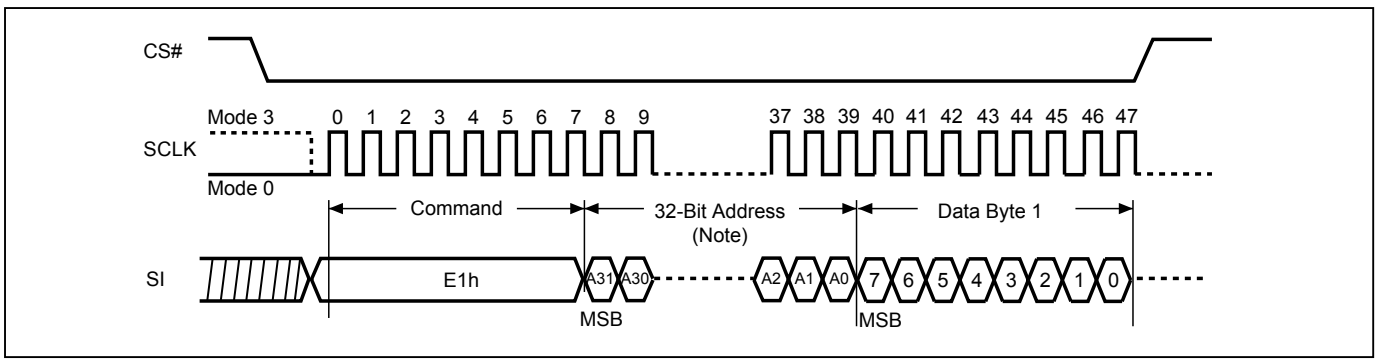
| Bit | Description | Bit Status | Default | Type |
|---|---|---|---|---|
| 7 to 0 | DPB (Dynamic Protection Bit) | 00h = Unprotect Sector / Block<br>FFh = Protect Sector / Block | FFh | Volatile |

**Figure 63. Read DPB Register (RDDPB) Sequence**




**Note:** A31-A24 are don't care.

**Figure 64. Write DPB Register (WRDPB) Sequence**




**Note:** A31-A24 are don't care.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-31-4. Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective if WPSEL=1. The GBLK and GBULK instructions provide a quick method to set or clear all DPB bits at once.

The WREN (Write Enable) instruction is required before issuing the GBLK/GBULK instruction.
The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction →CS# goes high.

The GBLK and GBULK commands are accepted in both SPI and QPI mode.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

### 9-31-5. Sector Protection States Summary Table

| Protection Status | | Sector/Block Protection State |
|---|---|---|
| DPB | SPB | |
| 0 | 0 | Unprotected |
| 0 | 1 | Protected |
| 1 | 0 | Protected |
| 1 | 1 | Protected |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-32. Program/Erase Suspend/Resume

The device allow the interruption of Sector-Erase, Block-Erase or Page-Program operations and conduct other operations.

After issue suspend command, the system can determine if the device has entered the Erase-Suspended mode through Bit2 (PSB) and Bit3 (ESB) of security register. (please refer to *"Table 12. Security Register Definition"*)

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

### 9-33. Erase Suspend

Erase suspend allow the interruption of all erase operations. After the device has entered Erase-Suspended mode, the system can read any sector(s) or Block(s) except those being erased by the suspended erase operation. Reading the sector or Block being erase suspended is invalid.

After erase suspend, WEL bit will be clear, only read related, resume and reset command can be accepted. (including: 03h, 0Bh, 3Bh, 6Bh, BBh, EBh, 5Ah, C0h, 06h, 04h, 2Bh, 9Fh, AFh, 05h, ABh, 90h, B1h, C1h, B0h, 30h, 66h, 99h, 00h, 35h, F5h, 15h, 2Dh, E2h, E0h)

If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended mode until tESL time has elapsed.

Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

### 9-34. Program Suspend

Program suspend allows the interruption of all program operations. After the device has entered Program-Suspended mode, the system can read any sector(s) or Block(s) except those being programmed by the suspended program operation. Reading the sector or Block being program suspended is invalid.

After program suspend, WEL bit will be cleared, only read related, resume and reset command can be accepted. (including: 03h, 0Bh, 3Bh, 6Bh, BBh, EBh, 5Ah, C0h, 06h, 04h, 2Bh, 9Fh, AFh, 05h, ABh, 90h, B1h, C1h, B0h, 30h, 66h, 99h, 00h, 35h, F5h, 15h, 2Dh, E2h, E0h)

Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 65. Suspend to Read Latency**

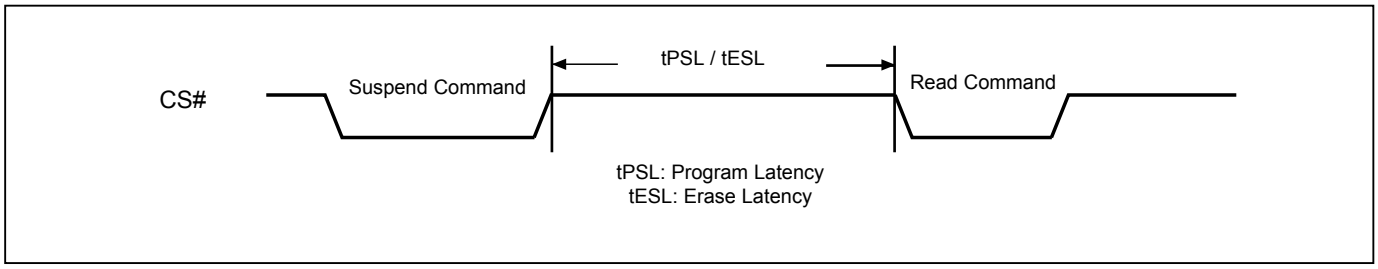



**Figure 66. Resume to Read Latency**

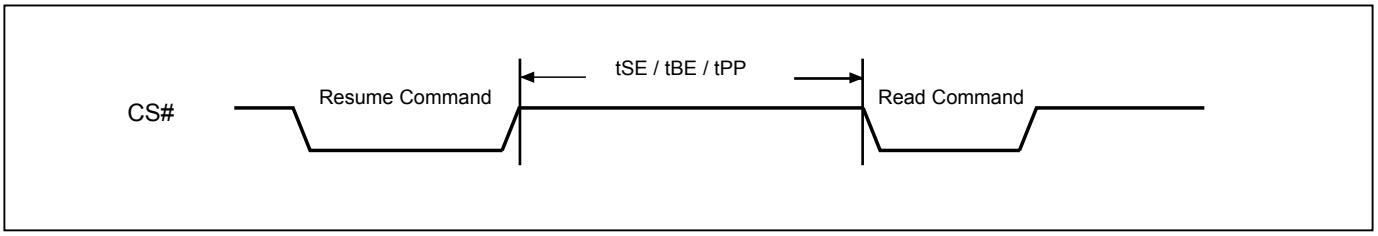
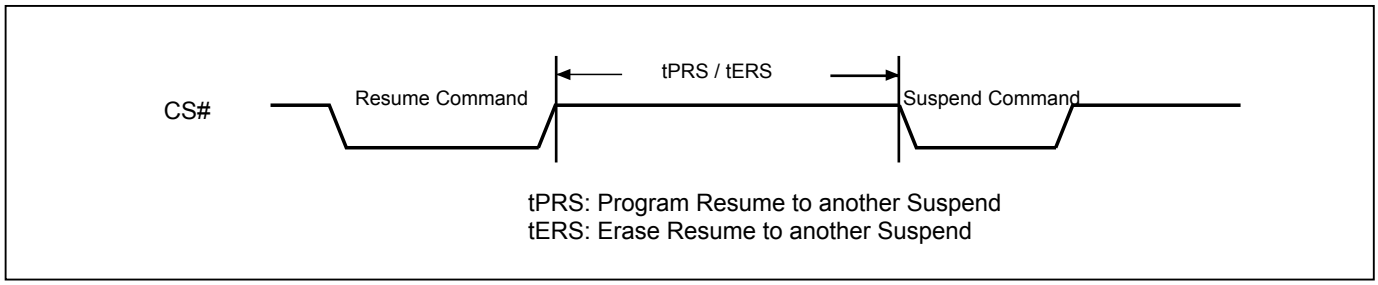



**Figure 67. Resume to Suspend Latency**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-35. Write-Resume

The Write operation is being resumed when Write-Resume instruction issued. ESB or PSB (suspend status bit) in Status register will be changed back to “0”.

The operation of Write-Resume is as follows: CS# drives low → send write resume command cycle (30H) → drive CS# high. By polling Busy Bit in status register, the internal write operation status could be checked to be completed or not. The user may also wait the time lag of tSE, tBE, tPP for Sector-erase, Block-erase or Page-programming. WREN (command "06h") is not required to issue before resume. Resume to another suspend operation requires latency time of 1ms.

Please note that, if "performance enhance mode" is executed during suspend operation, the device can not be resumed. To restart the write command, disable the "performance enhance mode" is required. After the "performance enhance mode" is disabled, the write-resume command is effective.

### 9-36. No Operation (NOP)

The “No Operation” command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

### 9-37. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command following a Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

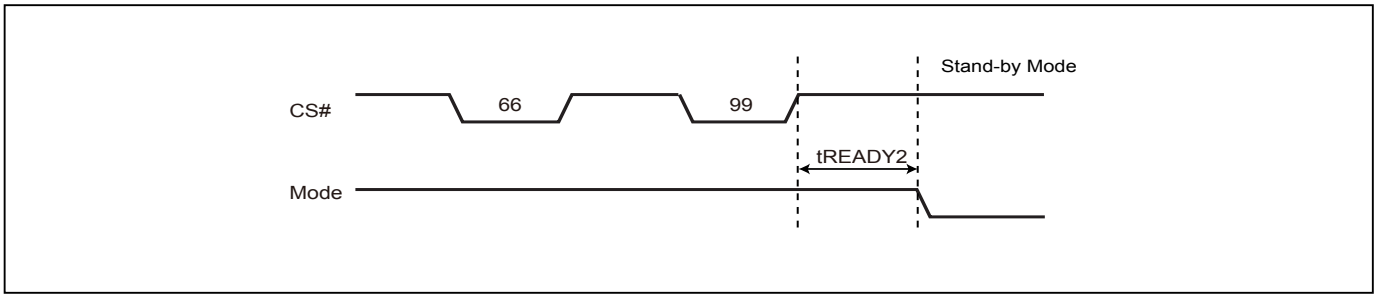
Both SPI (8 clocks) and QPI (2 clocks) command cycles can be accepted by this instruction. The SIO[3:1] are don't care during SPI mode.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. For details, please refer to *"Table 16. Reset Timing-(Reset Recovery time)"* for tREADY2.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 68. Software Reset Recovery**




Note: Refer to *"Table 16. Reset Timing-(Reset Recovery time)"* for tREADY2.

**Figure 69. Reset Sequence (SPI mode)**

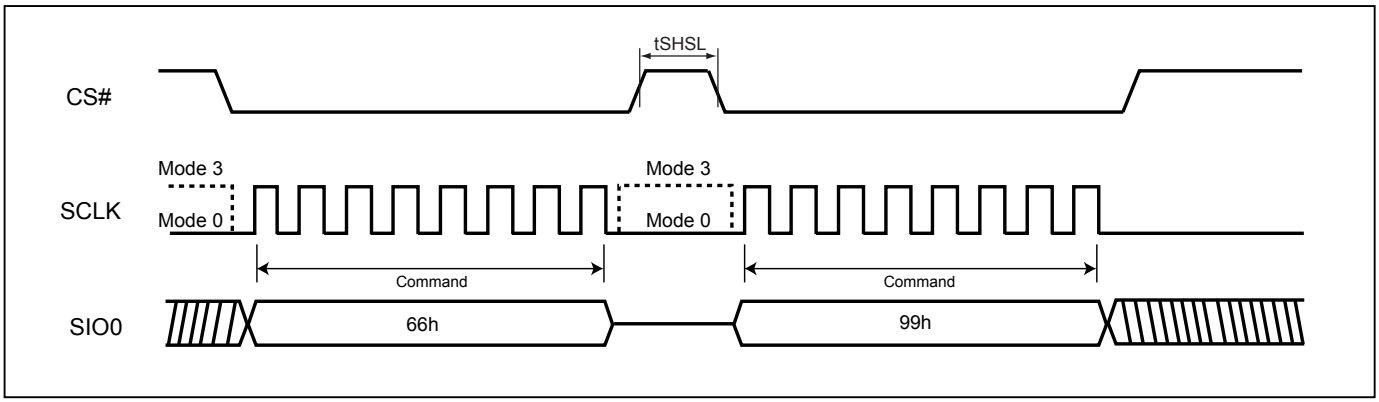
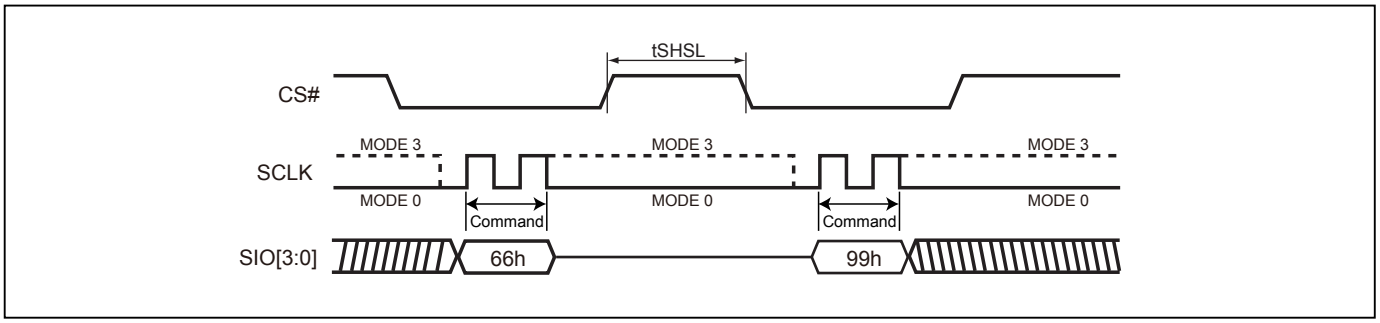



**Figure 70. Reset Sequence (QPI mode)**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 9-38. Read SFDP Mode (RDSFDP)

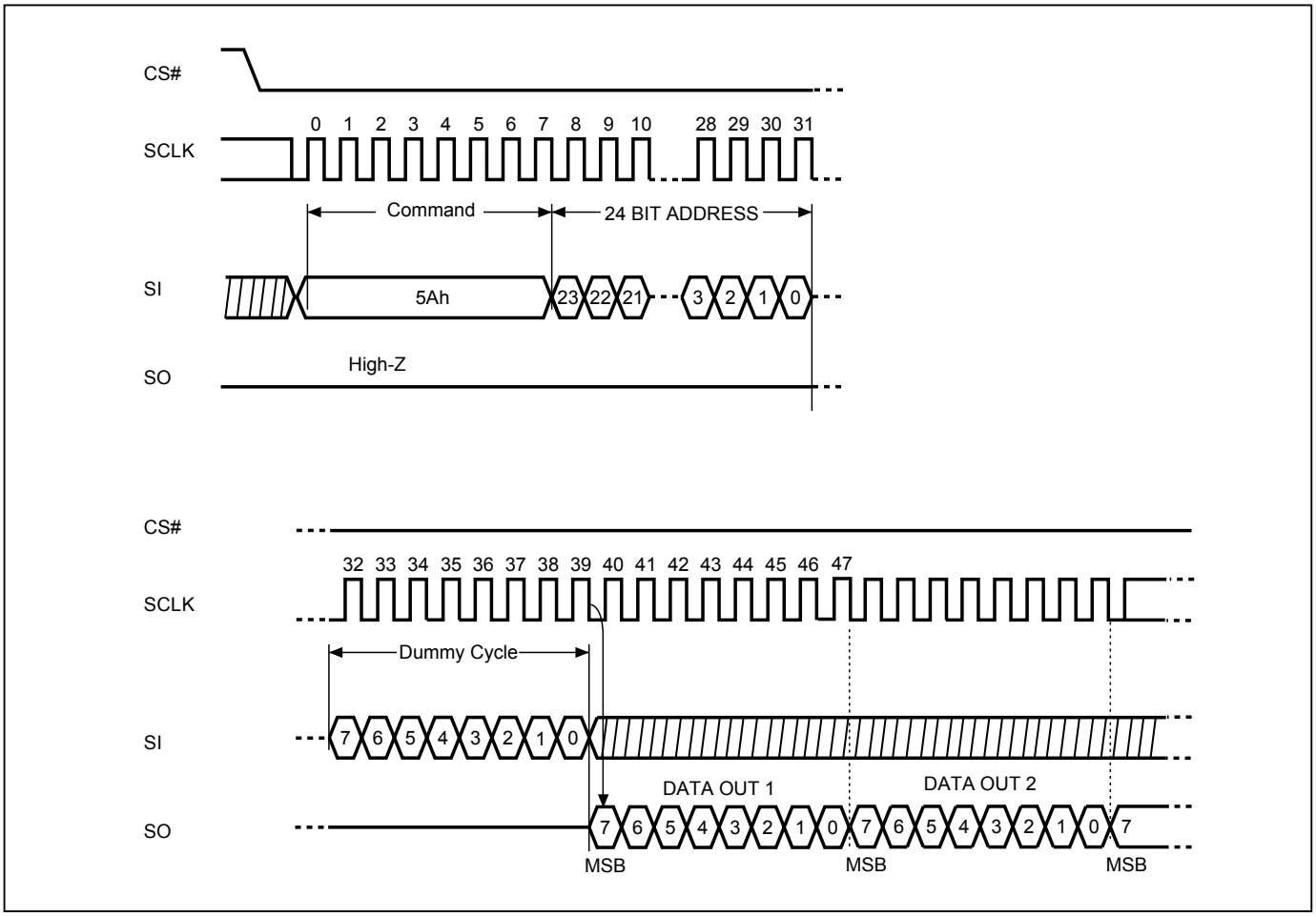
The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216B.

For SFDP register values detail, please contact local Macronix sales channel for Application Note.

**Figure 71. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 10. RESET

After reset cycle, the device is in the following states:
- Standby mode
- All the volatile bits such as WEL/WIP/SRAM lock bit will return to the default status as power on.

**Table 16. Reset Timing-(Reset Recovery time)**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| tREADY2 | Reset Recovery time (During instruction decoding) | 40 | | | us |
| | Reset Recovery time (for read operation) | 35 | | | us |
| | Reset Recovery time (for program operation) | 310 | | | us |
| | Reset Recovery time(for SE4KB operation) | 12 | | | ms |
| | Reset Recovery time (for BE64K/BE32KB operation) | 25 | | | ms |
| | Reset Recovery time (for Chip Erase operation) | 100 | | | ms |
| | Reset Recovery time (for WRSR operation) | 40 | | | ms |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 11. POWER-ON STATE

The device is in the states below when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

Please refer to the *"Figure 79. Power-up Timing"*.

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 12. ELECTRICAL SPECIFICATIONS

### Table 17. ABSOLUTE MAXIMUM RATINGS

| RATING | | VALUE |
|---|---|---|
| Ambient Operating Temperature | Industrial grade | -40°C to 85°C |
| Storage Temperature | | -65°C to 150°C |
| Applied Input Voltage | | -0.5V to VCC+0.5V |
| Applied Output Voltage | | -0.5V to VCC+0.5V |
| VCC to Ground Potential | | -0.5V to 4.0V |

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, please refer to *Figure 72* and *Figure 73.*

**Figure 72. Maximum Negative Overshoot Waveform**

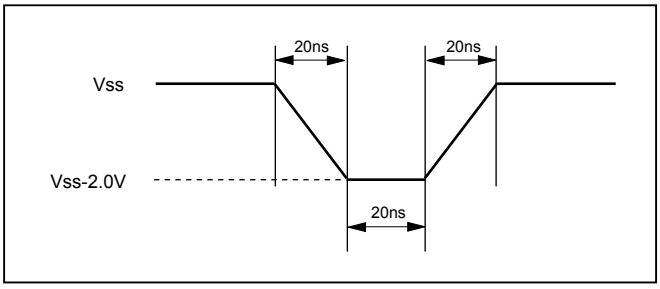
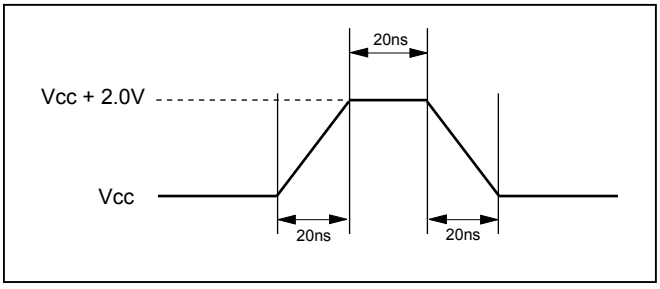



**Figure 73. Maximum Positive Overshoot Waveform**




### Table 18. CAPACITANCE TA = 25°C, f = 1.0 MHz

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | | | 6 | pF | VIN = 0V |
| COUT | Output Capacitance | | | 8 | pF | VOUT = 0V |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 74. DATA INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL**

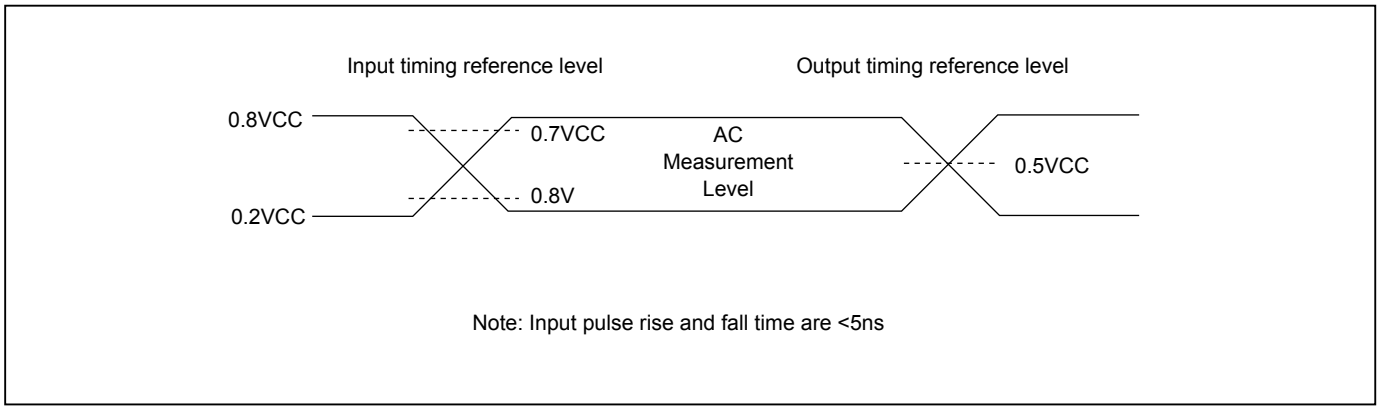



**Figure 75. OUTPUT LOADING**

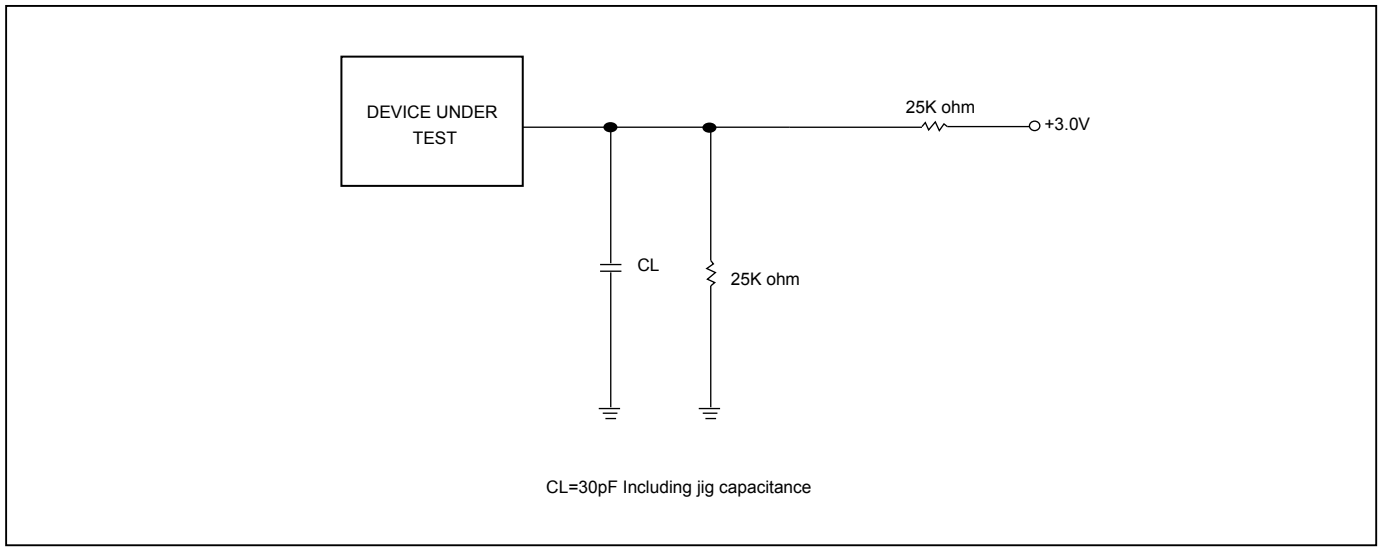
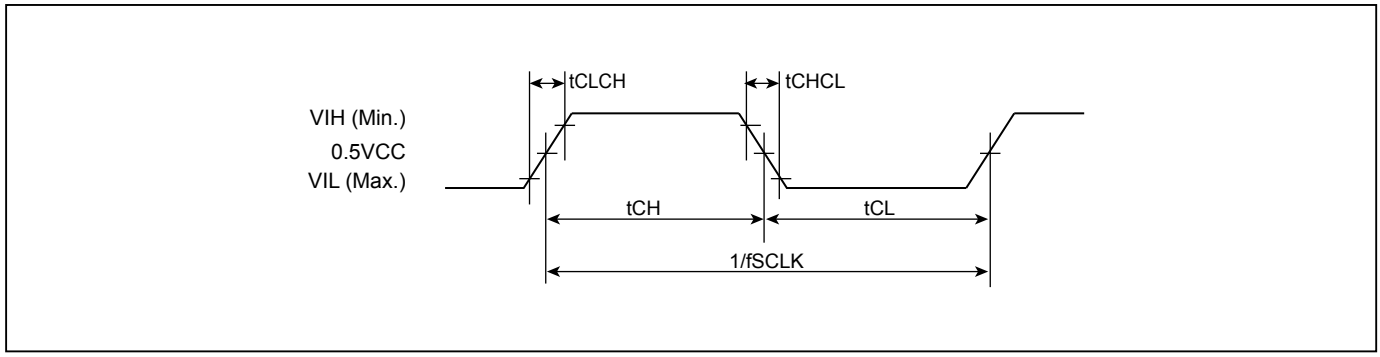



**Figure 76. SCLK TIMING DEFINITION**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Table 19. DC CHARACTERISTICS**

**(Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V)**

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| ILI | Input Load Current | 1 | | | ±2 | uA | VCC = VCC Max, VIN = VCC or GND |
| ILO | Output Leakage Current | 1 | | | ±2 | uA | VCC = VCC Max, VOUT = VCC or GND |
| ISB1 | VCC Standby Current | 1 | | 10 | 50 | uA | VIN = VCC or GND, CS# = VCC |
| ISB2 | Deep Power-down Current | | | 2 | 20 | uA | VIN = VCC or GND, CS# = VCC |
| ICC1 | VCC Read | 1 | | 14 | 25 | mA | f=133MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open |
| | | | | | 20 | mA | f=104MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open |
| | | | | | 15 | mA | f=84MHz, SCLK=0.1VCC/0.9VCC, SO=Open |
| ICC2 | VCC Program Current (PP) | 1 | | 14 | 20 | mA | Program in Progress, CS# = VCC |
| ICC3 | VCC Write Status Register (WRSR) Current | | | 10 | 12 | mA | Program status register in progress, CS#=VCC |
| ICC4 | VCC Sector/Block (32K, 64K) Erase Current (SE/BE/BE32K) | 1 | | 14 | 25 | mA | Erase in Progress, CS#=VCC |
| ICC5 | VCC Chip Erase Current (CE) | 1 | | 14 | 25 | mA | Erase in Progress, CS#=VCC |
| VIL | Input Low Voltage | | -0.5 | | 0.8 | V | |
| VIH | Input High Voltage | | 0.7VCC | | VCC+0.4 | V | |
| VOL | Output Low Voltage | | | | 0.2 | V | IOL = 100uA |
| VOH | Output High Voltage | | VCC-0.2 | | | V | IOH = -100uA |

***Notes :***

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Table 20. AC CHARACTERISTICS**

**(Temperature = -40°C to 85°C, VCC = 2.7V - 3.6V)**

| Symbol | Alt. | Parameter | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| fSCLK | fC | Clock Frequency for all commands (except Read) | | | D.C. | | 133 | MHz |
| fRSCLK | fR | Clock Frequency for READ instructions | | | | | 50 | MHz |
| fTSCLK | fT | Clock Frequency for 2READ/DREAD instructions | | | Please refer to *"Table 10. Dummy Cycle and Frequency Table (MHz)"* | | | MHz |
| | fQ | Clock Frequency for 4READ/QREAD instructions | | | | | | MHz |
| tCH(1) | tCLH | Clock High Time | Others (fSCLK) | > 66MHz | 45% x (1/fSCLK) | | | ns |
| | | | | ≤ 66MHz | 7 | | | ns |
| | | | Normal Read (fRSCLK) | | 7 | | | ns |
| tCL(1) | tCLL | Clock Low Time | Others (fSCLK) | > 66MHz | 45% x (1/fSCLK) | | | ns |
| | | | | ≤ 66MHz | 7 | | | ns |
| | | | Normal Read (fRSCLK) | | 7 | | | ns |
| tCLCH(3) | | Clock Rise Time (peak to peak) | | | 0.1 | | | V/ns |
| tCHCL(3) | | Clock Fall Time (peak to peak) | | | 0.1 | | | V/ns |
| tSLCH | tCSS | CS# Active Setup Time (relative to SCLK) | | | 3 | | | ns |
| tCHSL | | CS# Not Active Hold Time (relative to SCLK) | | | 3 | | | ns |
| tDVCH | tDSU | Data In Setup Time | | | 2 | | | ns |
| tCHDX | tDH | Data In Hold Time | | | 2 | | | ns |
| tCHSH | | CS# Active Hold Time (relative to SCLK) | | | 3 | | | ns |
| tSHCH | | CS# Not Active Setup Time (relative to SCLK) | | | 3 | | | ns |
| tSHSL | tCSH | CS# Deselect Time | From Read to next Read | | 7 | | | ns |
| | | | From Write/Erase/Program to Read Status Register | | 30 | | | ns |
| tSHQZ(3) | tDIS | Output Disable Time | | | | | 8 | ns |
| tCLQV | tV | Clock Low to Output Valid Loading: 30pF/15pF | Loading: 30pF | | | | 8 | ns |
| | | | Loading: 15pF | | | | 6 | ns |
| tCLQX | tHO | Output Hold Time | Loading: 30pF | | 1 | | | ns |
| | | | Loading: 15pF | | 1 | | | ns |
| tDP(3) | | CS# High to Deep Power-down Mode | | | | | 10 | us |
| tRES1(3) | | CS# High to Standby Mode without Electronic Signature Read | | | | | 30 | us |
| tRES2(3) | | CS# High to Standby Mode with Electronic Signature Read | | | | | 30 | us |
| tW | | Write Status/Configuration Register Cycle Time | | | | | 40 | ms |
| tBP | | Byte-Program | | | | 16 | 40 | us |
| tPP | | Page Program Cycle Time | | | | 0.33 | 1.2 | ms |
| tSE | | Sector Erase Cycle Time | | | | 25 | 120 | ms |
| tBE32 | | Block Erase (32KB) Cycle Time | | | | 140 | 650 | ms |
| tBE | | Block Erase (64KB) Cycle Time | | | | 250 | 650 | ms |
| tCE | | Chip Erase Cycle Time | | | | 26 | 60 | s |
| tESL(5) | | Erase Suspend Latency | | | | | 25 | us |
| tPSL(5) | | Program Suspend Latency | | | | | 25 | us |
| tPRS(6) | | Latency between Program Resume and next Suspend | | | 0.3 | 100 | | us |
| tERS(7) | | Latency between Erase Resume and next Suspend | | | 0.3 | 400 | | us |

深圳市满度科技有限公司
Web:www.manduic.com
P/N:PM2541
Macronix Proprietary
Rev. 1.1, April 09, 2021
Tel:150-1200-5940
Email:sales@manduic.com

**Notes:**

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. The value guaranteed by characterization, not 100% tested in production.
4. Test condition is shown as *"Figure 74. DATA INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL"* and *"Figure 75. OUTPUT LOADING"*.
5. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
6. For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
7. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

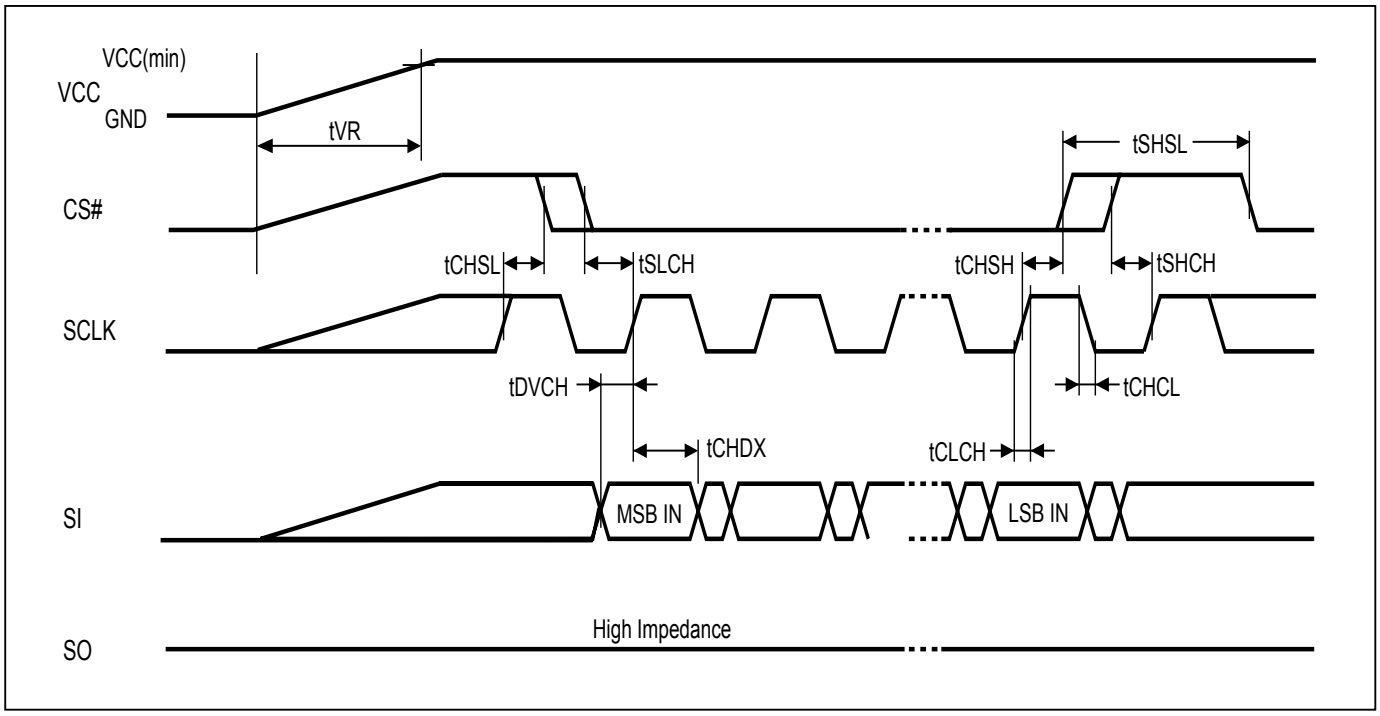
## 13. OPERATING CONDITIONS

### At Device Power-Up and Power-Down

AC timing illustrated in *"Figure 77. AC Timing at Device Power-Up"* and *"Figure 78. Power-Down Sequence"* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

**Figure 77. AC Timing at Device Power-Up**




| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| tVR | VCC Rise Time | 1 | | 500000 | us/V |

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *Table 17.* AC CHARACTERISTICS.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 78. Power-Down Sequence**

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

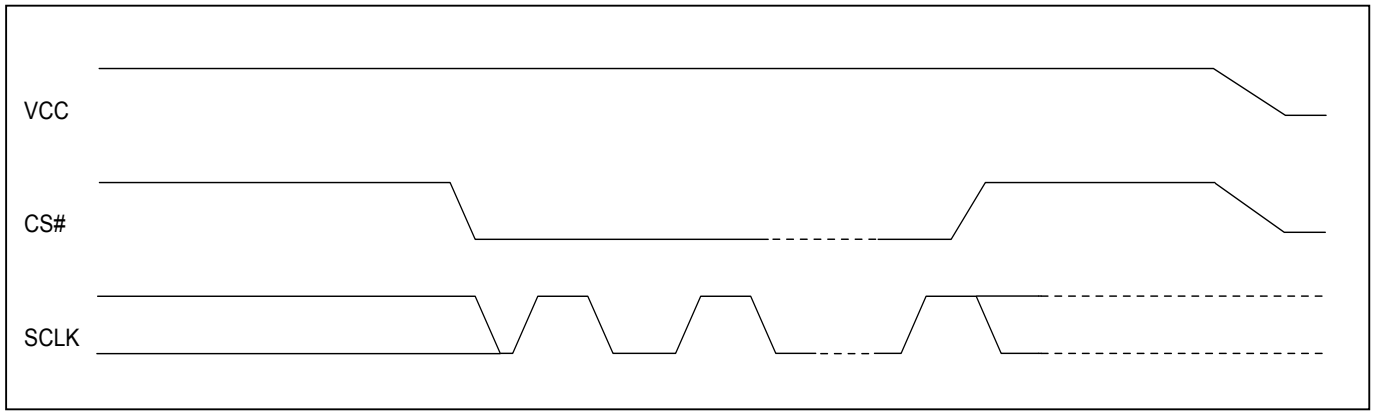
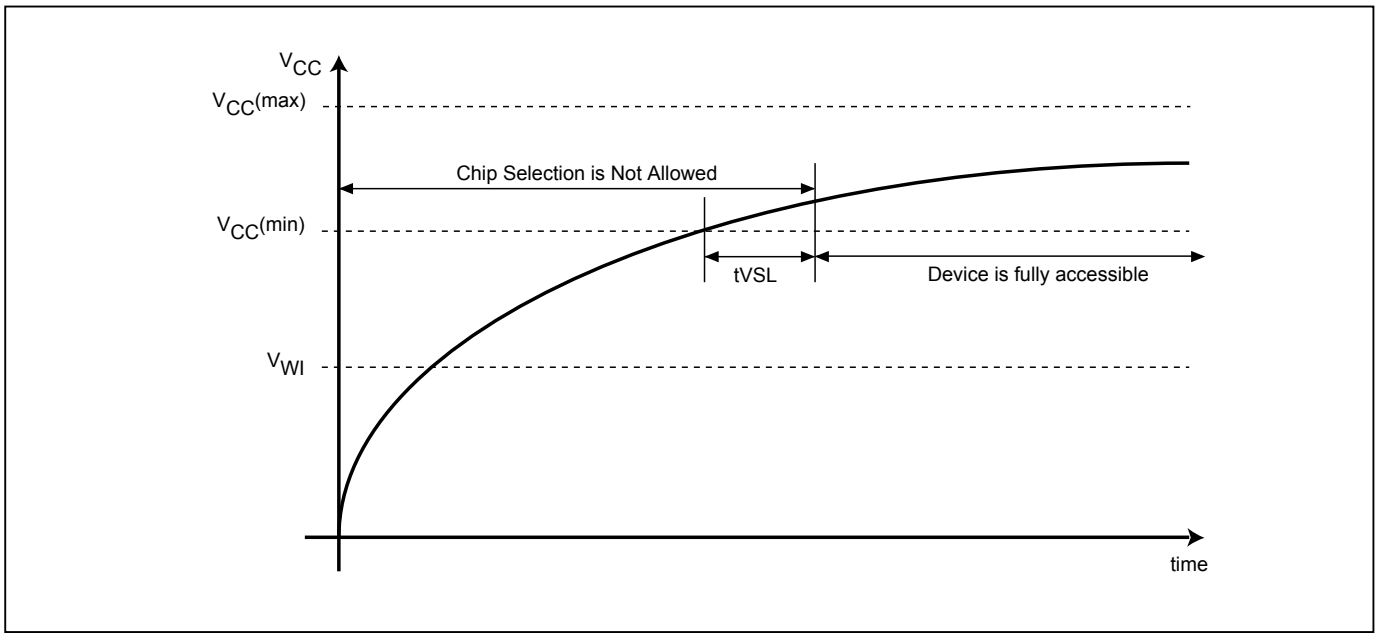



**Figure 79. Power-up Timing**





深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

**Figure 80. Power Up/Down and Voltage Drop**

When powering down the device, VCC must drop below $V_{PWD}$ for at least tPWD to ensure the device will initialize correctly during power up. Please refer to *"Figure 80. Power Up/Down and Voltage Drop"* and *"Table 21. Power-Up/Down Voltage and Timing"* below for more details.

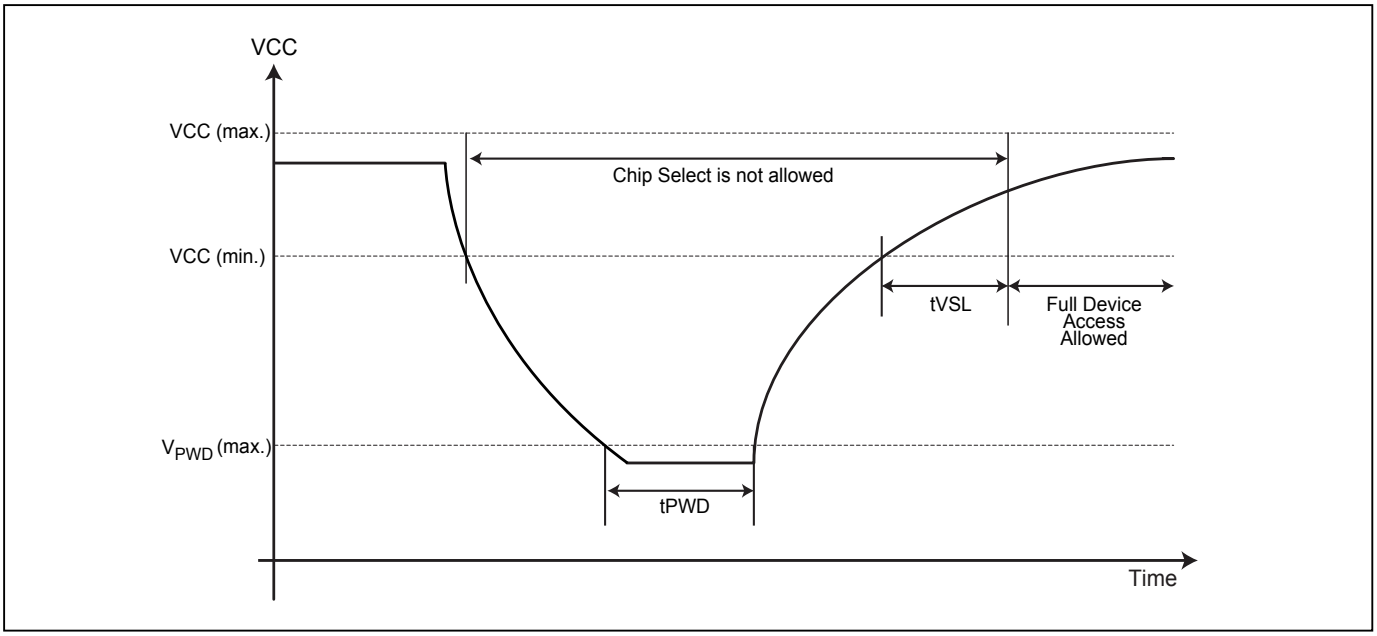



**Table 21. Power-Up/Down Voltage and Timing**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tVSL | VCC(min.) to device operation | 800 | | us |
| VWI | Write Inhibit Voltage | 1.5 | 2.5 | V |
| $V_{PWD}$ | VCC voltage needed to below $V_{PWD}$ for ensuring initialization will occur | | 0.9 | V |
| tPWD | The minimum duration for ensuring initialization will occur | 300 | | us |
| VCC | VCC Power Supply | 2.7 | 3.6 | V |

Note: These parameters are characterized only.

## 13-1. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 40h (all Status Register bits are 0 except QE bit: QE=1).


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 14. ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Min. | Typ. (1) | Max. (2) | Unit |
|---|---|---|---|---|
| Write Status Register Cycle Time | | | 40 | ms |
| Sector Erase Cycle Time (4KB) | | 25 | 120 | ms |
| Block Erase Cycle Time (32KB) | | 0.14 | 0.65 | s |
| Block Erase Cycle Time (64KB) | | 0.25 | 0.65 | s |
| Chip Erase Cycle Time | | 26 | 60 | s |
| Byte Program Time (via page program command) | | 16 | 40 | us |
| Page Program Time | | 0.33 | 1.2 | ms |
| Erase/Program Cycle | | 100,000 | | cycles |

**Note:**
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checkerboard pattern.
2. Under worst conditions of 2.7V, highest operation temperature, post program/erase cycling.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.

## 15. ERASE AND PROGRAMMING PERFORMANCE (Factory Mode)

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Sector Erase Cycle Time (4KB) | | 15 | | ms |
| Block Erase Cycle Time (32KB) | | 100 | | ms |
| Block Erase Cycle Time (64KB) | | 200 | | ms |
| Chip Erase Cycle Time | | 25 | | s |
| Page Program Time | | 0.33 | | ms |
| Erase/Program Cycle | | | 50 | cycles |

**Notice:**
1. Factory Mode must be operated in 20°C to 45°C and VCC 3.0V-3.6V.
2. In Factory mode, the Erase/Program operation should not exceed 50 cycles, and "ERASE AND PROGRAMMING PERFORMANCE" 100k cycles will not be affected.
3. During factory mode, Suspend command (75h or B0h) cannot be executed.


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 16. DATA RETENTION

| Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|
| Data retention | 55°C | 20 | | years |

## 17. LATCH-UP CHARACTERISTICS

| | Min. | Max. |
|---|---|---|
| Input Voltage with respect to GND on all power pins | | 1.5 VCCmax |
| Input Current on all non-power pins | -100mA | +100mA |
| Test conditions: VCC = VCCmax, one pin at a time (compliant to JEDEC JESD78 standard). | | |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

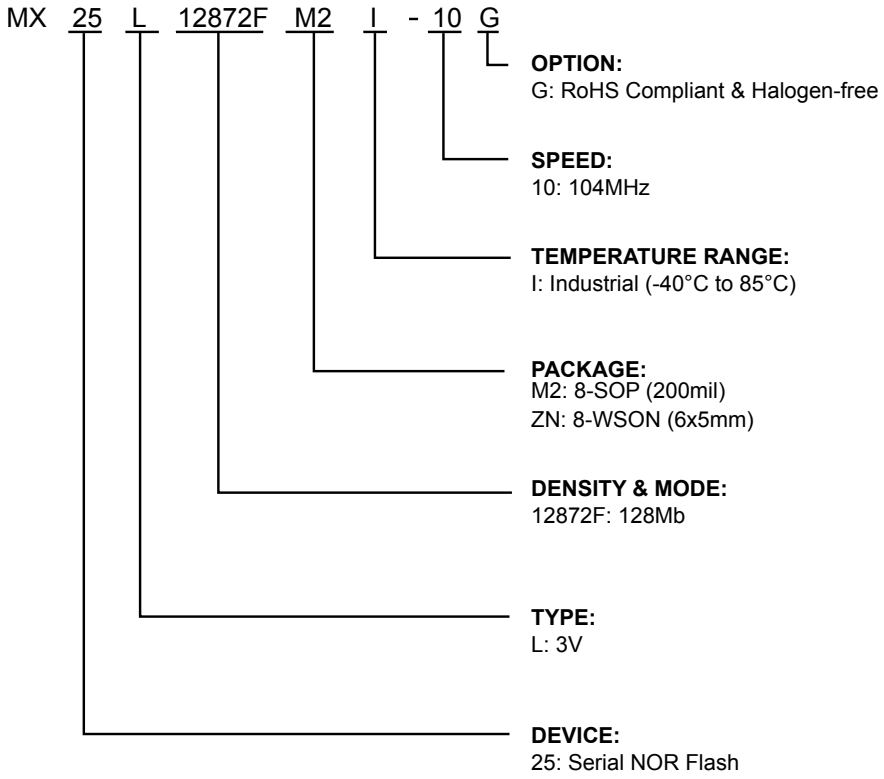
## 18. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

| PART NO. | TEMPERATURE | PACKAGE | Remark |
|---|---|---|---|
| MX25L12872FM2I-10G | -40°C to 85°C | 8-SOP (200mil) | Support Factory Mode |
| MX25L12872FZNI-10G | -40°C to 85°C | 8-WSON (6x5mm) | Support Factory Mode |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 19. PART NAME DESCRIPTION



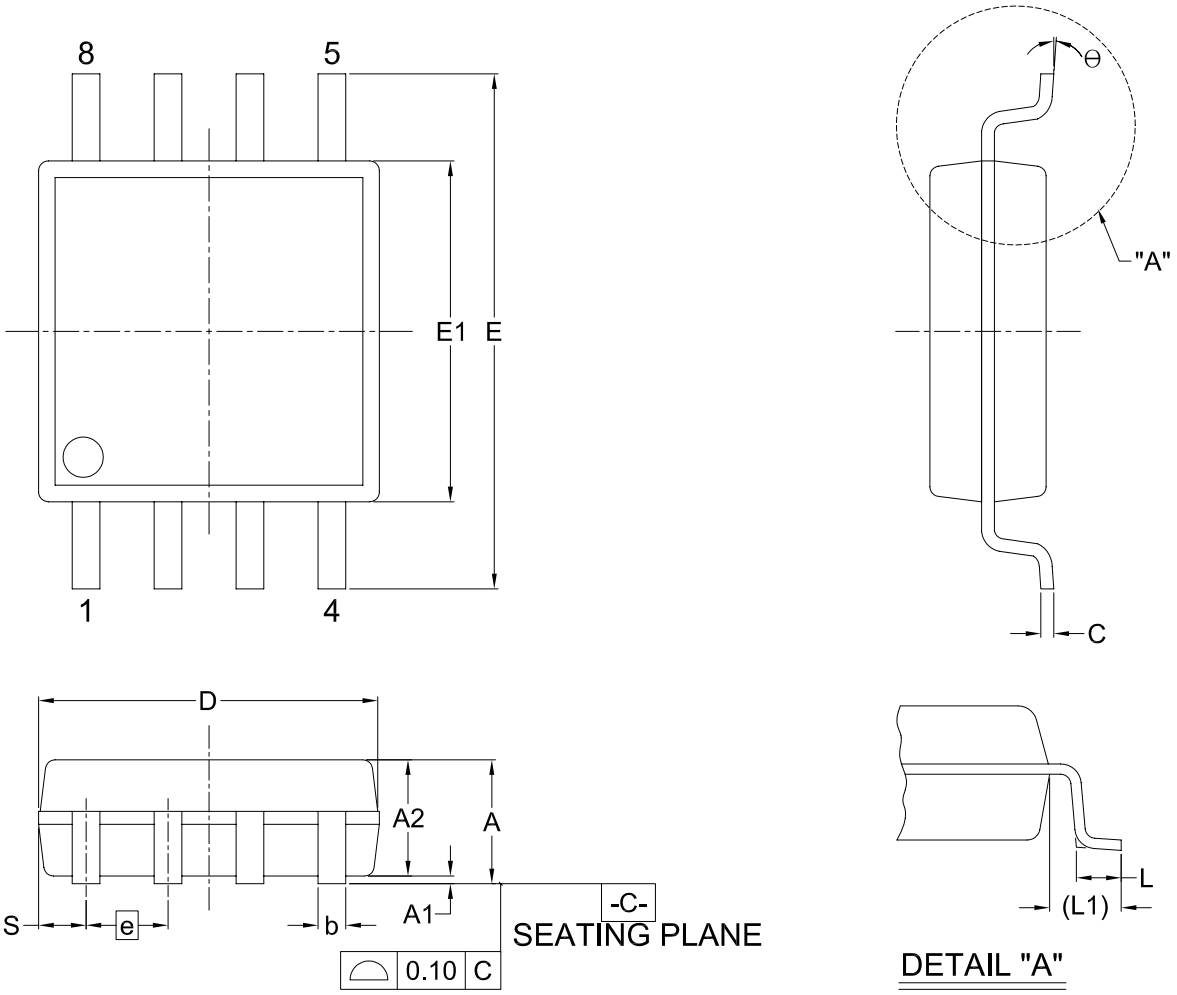


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

## 20. PACKAGE INFORMATION

### 20-1. 8-pins SOP (200mil)

Doc. Title: Package Outline for SOP 8L 200MIL



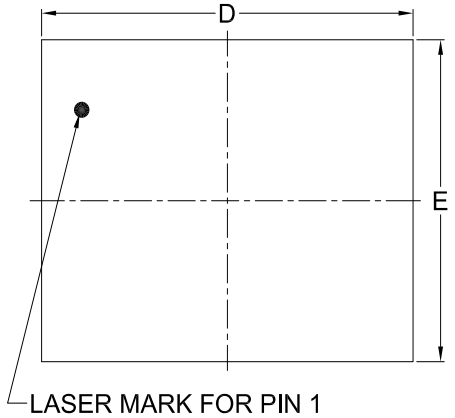

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | E | E1 | e | L | L1 | S | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 1.75 | 0.05 | 1.70 | 0.36 | 0.19 | 5.13 | 7.70 | 5.18 | --- | 0.50 | 1.21 | 0.62 | 0° |
| | Nom. | 1.95 | 0.15 | 1.80 | 0.41 | 0.20 | 5.23 | 7.90 | 5.28 | 1.27 | 0.65 | 1.31 | 0.74 | 5° |
| | Max. | 2.16 | 0.20 | 1.91 | 0.51 | 0.25 | 5.33 | 8.10 | 5.38 | --- | 0.80 | 1.41 | 0.88 | 8° |
| Inch | Min. | 0.069 | 0.002 | 0.067 | 0.014 | 0.007 | 0.202 | 0.303 | 0.204 | --- | 0.020 | 0.048 | 0.024 | 0° |
| | Nom. | 0.077 | 0.006 | 0.071 | 0.016 | 0.008 | 0.206 | 0.311 | 0.208 | 0.050 | 0.026 | 0.052 | 0.029 | 5° |
| | Max. | 0.085 | 0.008 | 0.075 | 0.020 | 0.010 | 0.210 | 0.319 | 0.212 | --- | 0.031 | 0.056 | 0.035 | 8° |

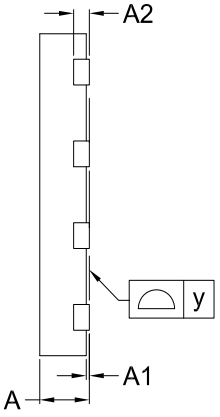

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

### 20-2. 8-land WSON (6x5mm)

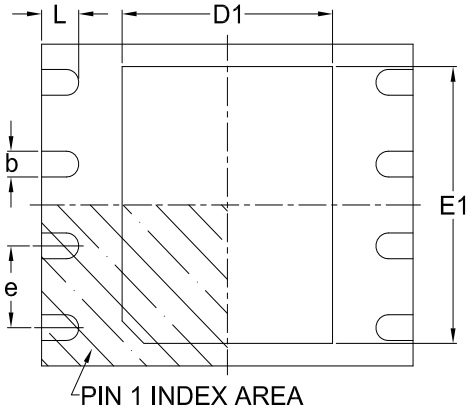
**Doc. Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)**




TOP VIEW




SIDE VIEW




BOTTOM VIEW

Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | L | e | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 0.70 | --- | --- | 0.35 | 5.90 | 3.35 | 4.90 | 3.95 | 0.55 | --- | 0.00 |
| | Nom. | --- | --- | 0.20 | 0.40 | 6.00 | 3.40 | 5.00 | 4.00 | 0.60 | 1.27 | --- |
| | Max. | 0.80 | 0.05 | --- | 0.48 | 6.10 | 3.45 | 5.10 | 4.05 | 0.65 | --- | 0.05 |
| Inch | Min. | 0.028 | --- | --- | 0.014 | 0.232 | 0.132 | 0.193 | 0.156 | 0.022 | --- | 0.00 |
| | Nom. | --- | --- | 0.008 | 0.016 | 0.236 | 0.134 | 0.197 | 0.157 | 0.024 | 0.05 | --- |
| | Max. | 0.032 | 0.002 | --- | 0.019 | 0.240 | 0.136 | 0.201 | 0.159 | 0.026 | --- | 0.002 |

深圳市满度科技有限公司
Web:www.manduic.com
P/N: PM2541
Macronix Proprietary

Tel:150-1200-5940
Email:sales@manduic.com

## 21. REVISION HISTORY

| Revision | Descriptions | Page |
|---|---|---|
| September 07, 2017 | | |
| 0.00 | 1. Initial Release. | All |
| October 17, 2017 | 1. Removed document status "Advanced Information". | All |
| 1.0 | 2. Added 8-land WSON (6X5mm) package informaion. | P4, 6, 84-85, 87 |
| | 3. Updated Program and Erase values. | P77, 82 |
| | 4. Added WRSCUR and RDSCUR command figures. | P55-56 |
| | 5. Content modifications. | P5, 34, 44, 84 |
| April 09, 2021 | | |
| 1.1 | 1. Added "Support Performance Enhance Mode - XIP(execute-in-place)" | P4,44 |
| | 2. Modified "LATCH-UP CHARACTERISTICS" table | P83 |
| | 3. Added "Macronix Proprietary" footnote. | ALL |
| | 4. Revised Doc. Title of package outline | P86 |
| | 5. Clarified single, dual, and quad I/O mode supporting in QE bit setting descriptions. | P30 |
| | 6. Corrected "Read Electronic Signature (RES) Sequence" figures. | P22-23 |
| | 7. Corrected the Data Byte information of WRSCUR & WRSPB. | P16 |
| | 8. Added Output Driver Strength percentage information. | P32 |
| | 9. Modified the note descriptions for fTSCLK. | P77-78 |
| | 10. Content modification | P1, 4, 10, 12-13, 15, 16, 18, 20-22, 25, 33, 36-40, 42-43, 47-51, 53, 58-59, 72, 75, 81 |
| | 11. Modified the notes of ERASE AND PROGRAMMING PERFORMANCE Table. | P82 |


深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1200-5940
Email:sales@manduic.com

Except for customized products which have been expressly identified in the applicable agreement, Macronix's products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and not for use in any applications which may, directly or indirectly, cause death, personal injury, or severe property damages. In the event Macronix products are used in contradicted to their target usage above, the buyer shall take any and all actions to ensure said Macronix's product qualified for its actual use in accordance with the applicable laws and regulations; and Macronix as well as it's suppliers and/or distributors shall be released from any and all liability arisen therefrom.

Copyright© Macronix International Co., Ltd. 2017-2021. All rights reserved, including the trademarks and tradename thereof, such as Macronix, MXIC, MXIC Logo, MX Logo, Integrated Solutions Provider, Nbit, Macronix NBit, HybridNVM, HybridFlash, HybridXFlash, XtraROM, KH Logo, BE-SONOS, KSMC, Kingtech, MXSMIO, Macronix vEE, RichBook, Rich TV, OctaBus, FitCAM, ArmorFlash, LybraFlash. The names and brands of third party referred thereto (if any) are for identification purposes only.

For the contact and order information, please visit Macronix's Web site at: http://www.macronix.com



深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com