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e.MMC Memory

MTFC32GAZAQHD-WT, MTFC32GAZAQHD-IT, MTFC64GAZAQHD-WT, MTFC64GAZAQHD-IT, MTFC128GAZAQJP-IT

Features

- MultiMediaCard (MMC) controller and NAND flash
- JEDEC/MMC standard version 5.1-compliant (JEDEC Standard No. JESD84-B51)[1]
- V_{CC}: 2.7–3.6V
- V_{CCQ}: 1.70–1.95V
- Storage temperature range:
  - WT: From –40°C to +85°C
  - IT: From –40°C to +95°C
- Advanced 12-signal interface
- ×1, ×4, and ×8 I/Os, selectable by host
- e.MMC I/F boot frequency: 0 to 52 MHz
- e.MMC I/F clock frequency: 0 to 200 MHz
- HS200/HS400 mode
- Command classes: Class 0 (basic); Class 2 (block read); Class 4 (block write); Class 5 (erase); Class 6 (write protection); Class 7 (lock card)
- Command queue
- BKOPS control
- Temporary write protection
- Boot operation (high-speed boot)
- Sleep mode
- Replay-protected memory block (RPMB)
- Hardware reset signal
- Multiple partitions with enhanced attribute
- Permanent and power-on write protection
- High-priority interrupt (HPI)
- Data strobe pin
- Field firmware update (FFU)
- Device health report
- Sleep notification
- Background operation
- Reliable write
- Discard and sanitize
- Power-off notification
- Backward compatible with previous MMC
- ECC and block management implemented
- Enhanced strobe
- Extended reflow capability
- Retention:
  - 1 year @55°C at maximum PE
  - 10 years @55°C at 10% of PE

Options	Marking
• Density	
– 32GB	32G
– 64GB	64G
– 128GB	128G
• NAND component	
– 256Gb	AZ
• Controller	AQ
• Packages – JEDEC-standard, RoHS-compliant	
– 153-ball VFBGA	HD
– 153-ball VFBGA	JP
• Operating temperature range[2]	
– From –25°C to +85°C	WT
– From –40°C to +95°C	IT

Notes: 1. The JEDEC specification is available at www.jedec.org/sites/default/files/docs/JESD84-B51.pdf.
2. Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the package.

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Part Numbering Information

Micron® e.MMC memory devices are available in different configurations and densities.

Figure 1: e.MMC Part Numbering

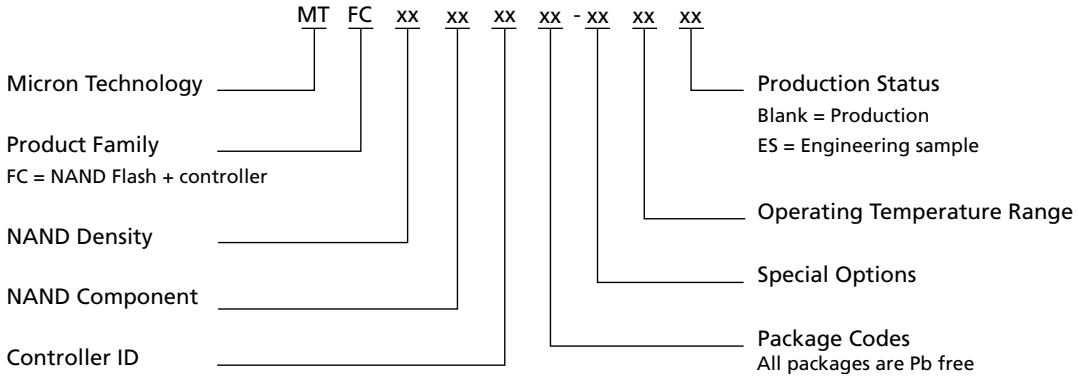


Table 1: Ordering Information

Base Part Number	Density	Package	Shipping
MTFC32GAZAQHD-WT MTFC32GAZAQHD-IT	32GB	153-ball VFBGA 11.5mm × 13mm × 0.9mm	Tray
			Tape and reel
MTFC64GAZAQHD-WT MTFC64GAZAQHD-IT	64GB	153-ball VFBGA 11.5mm × 13mm × 0.9mm	Tray
			Tape and reel
MTFC128GAZAQJP-IT	128GB	153-ball VFBGA 11.5mm × 13mm × 1.0mm	Tray
			Tape and reel

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder.

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e.MMC Performance

Performance in the following tables are retrieved with these conditions: Bus in x8 I/O; Temperature 25°C; Sequential access of 512KB chunk; Cache on (write); Command queueing enabled with queue depth 32 commands.

Additional performance data, such as system performance on a specific application board, is provided in a separate document upon customer request.

Table 2: HS400 Performance

Condition	Typical Values			Unit
	32GB	64GB	128GB	
Sequential write	100	215	215	MB/s
Sequential read	300	320	320	MB/s

Table 3: HS200 Performance

Condition	Typical Values			Unit
	32GB	64GB	128GB	
Sequential write	100	140	140	MB/s
Sequential read	175	175	175	MB/s

e.MMC Current Consumption

Current consumption in the following tables are retrieved with these conditions: Bus in x8 I/O; V_{CC} = 3.6V and V_{CCQ} = 1.95V; Temperature 25°C; Measurements done as average RMS current consumption; I_{CCQ} in READ operation measurements with tester load disconnected.

Table 4: HS400 Current Consumption

Condition	Typical Values (I_{CC}/I_{CCQ})			Unit
	32GB	64GB	128GB	
Write[1]	50/110	50/110	50/110	mA
Read[1]	50/190	50/190	50/190	mA
Sleep (V_{CC} off)	0/280	0/300	0/315	µA
Auto standby	25/350	45/360	75/405	µA

Note: 1. Command queueing enabled with queue depth 32 commands.

Table 5: HS200 Current Consumption

Condition	Typical Values (I_{CC}/I_{CCQ})			Unit
	32GB	64GB	128GB	
Write	40/105	40/105	40/105	mA
Read	40/150	40/150	40/150	mA
Sleep (V_{CC} off)	0/280	0/300	0/315	µA

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Table 5: HS200 Current Consumption (Continued)

Condition	Typical Values (I_{CC}/I_{CCQ})			Unit
	32GB	64GB	128GB	
Auto standby	25/350	45/360	75/405	µA

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General Description

Micron e.MMC is a communication and mass data storage device that includes a MultiMediaCard (MMC) interface, a NAND Flash component, and a controller on an advanced 12-signal bus, which is compliant with the MMC system specification. Its cost per bit, small package sizes, and high reliability make it an ideal choice for automotive applications, including information and entertainment, navigation tools, advanced driving assistance systems, and a variety of other industrial and portable products.

The nonvolatile e.MMC draws no power to maintain stored data, delivers high performance across a wide range of operating temperatures, and resists shock and vibration disruption.

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Signal Descriptions

Table 6: Signal Descriptions

Symbol	Type	Description
CLK	Input	Clock: Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency.
RST_n	Input	Reset: The RST_n signal is used by the host for resetting the device, moving the device to the pre-idle state. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it.
CMD	I/O	Command: This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode (see Operating Modes). Commands are sent from the MMC host to the device, and responses are sent from the device to the host.
DAT[7:0]	I/O	Data I/O: These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer either using DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode). *e*·MMC includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT[3:1] lines. Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines.
DS	Output	Data strobe: Generated by the device and used for data output and CRC status response output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output, each cycle of this signal directs two bits transfer (2x) on the data, one bit for the positive edge and the other bit for the negative edge. For CRC status response output, the CRC status is latched on the positive edge only, and is "Don't Care" on the negative edge.
VSF[7:1]	Input/output	Vendor specific function: VSF[7:1] must be left floating; Exposing VSF balls on test points is recommended.
V_{CC}	Supply	V_{CC}: NAND Flash power supply.
V_{CCQ}	Supply	V_{CCQ}: *e*·MMC controller core, *e*·MMC interface I/O, and NAND interface I/O power supply.
V_{SS}[1]	Supply	V_{SS}: NAND interface I/O and NAND Flash ground connection.
V_{SSQ}[1]	Supply	V_{SSQ}: *e*·MMC controller core and *e*·MMC interface ground connection.
V_{DDIM}		Internal voltage node: At least a 0.1µF capacitor is required to connect V_{DDIM} to ground. A 1µF capacitor is recommended. Do not tie to supply voltage or ground.
NC	–	No connect: No internal connection is present.
RFU	–	Reserved for future use: No internal connection is present. Leave it floating externally.

Note: 1. V_{SS} and V_{SSQ} are connected internally.

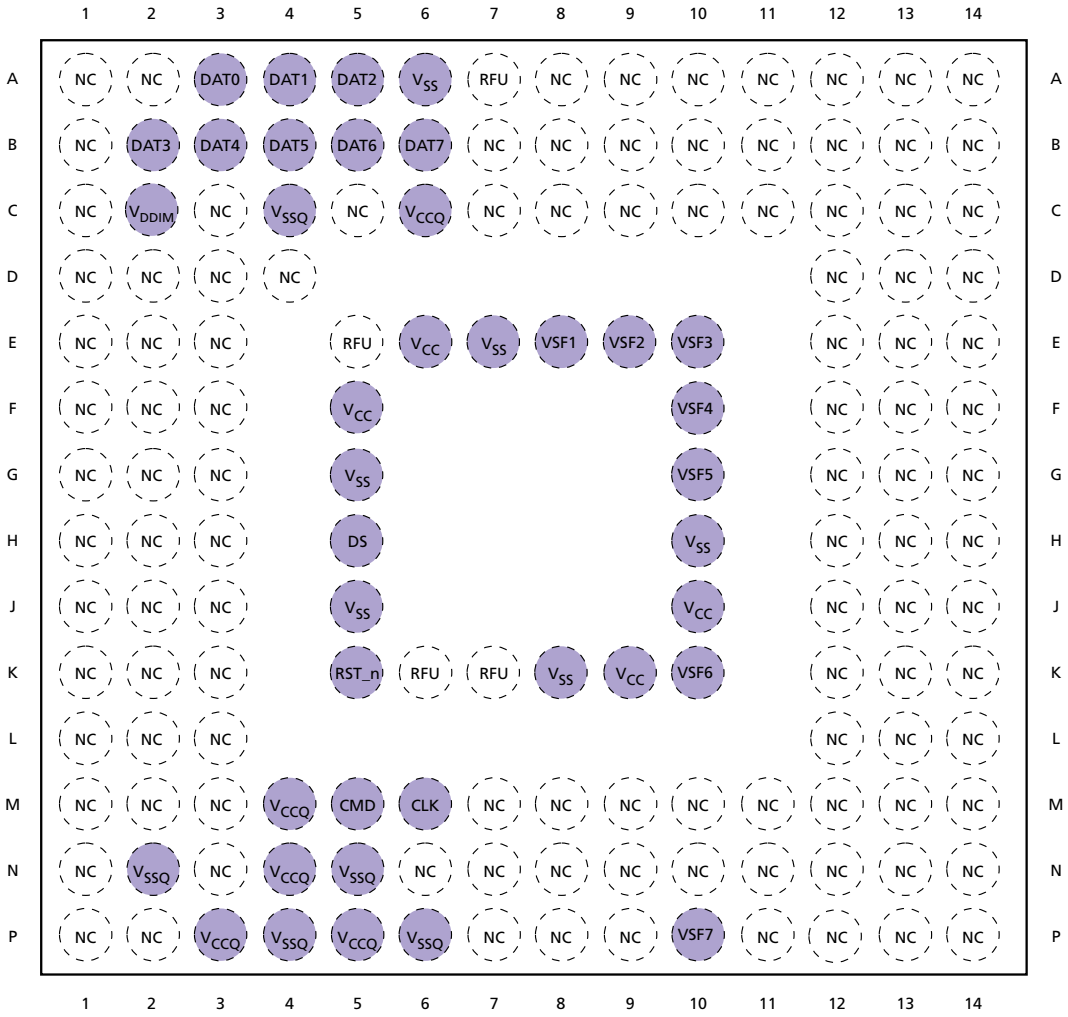
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153-Ball Signal Assignments

Figure 2: 153 Ball (Top View, Ball Down)



Top View

Notes: 1. Some previous versions of the JEDEC product or mechanical specification had defined reserved for future use (RFU) balls as no connect (NC) balls. NC balls assigned in the previous specifications could have been connected to ground on the system board. To enable new feature introduction, some of these balls are assigned as RFU in the v4.4 mechanical specification. Any new PCB footprint implementations should use the new ball assignments and leave the RFU balls floating on the system board.

2. V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} balls must all be connected on the system board.

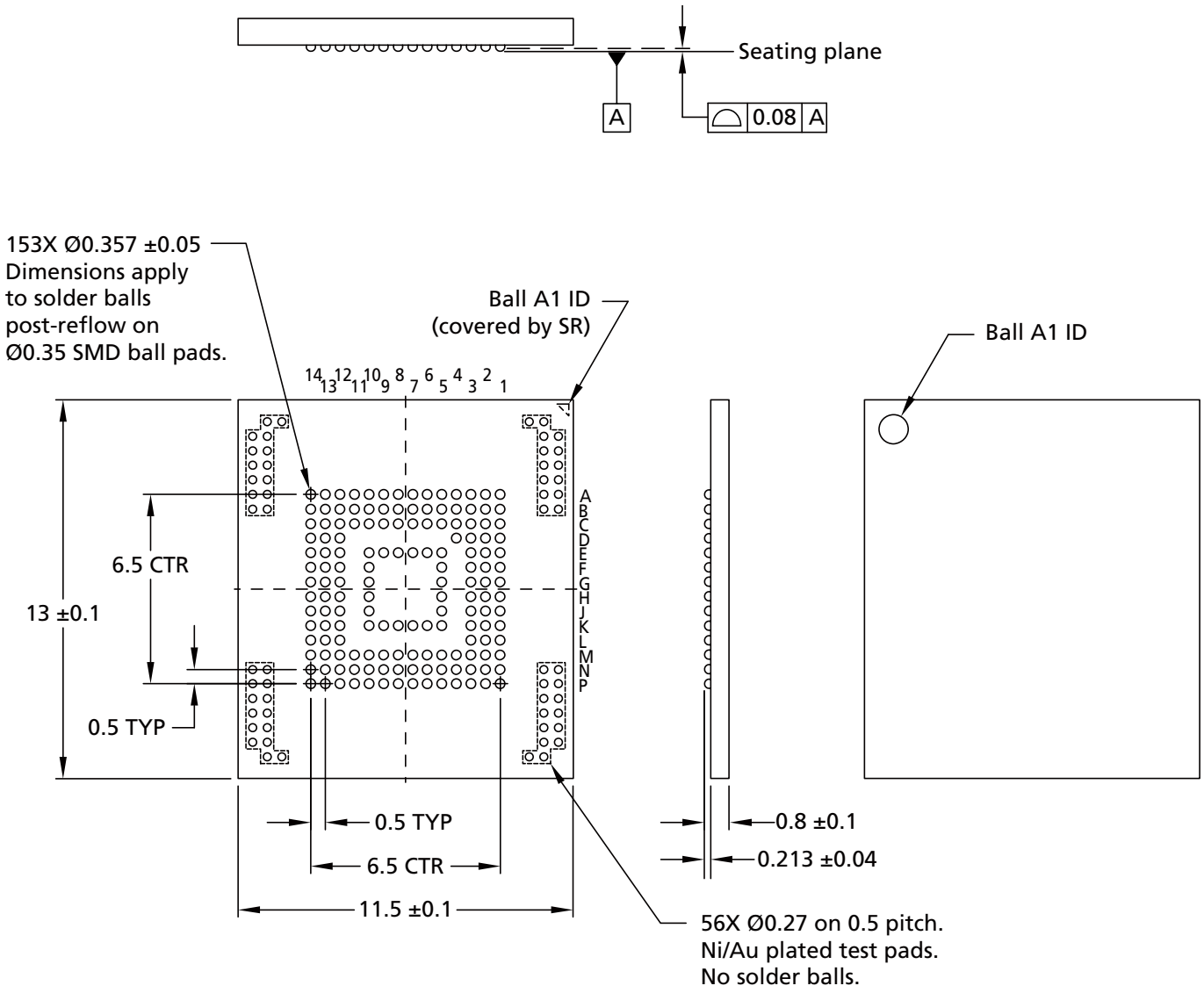
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Package Dimensions

Figure 3: 153-Ball VFBGA – 11.5mm x 13.0mm x 0.9mm (Package Code: HD)

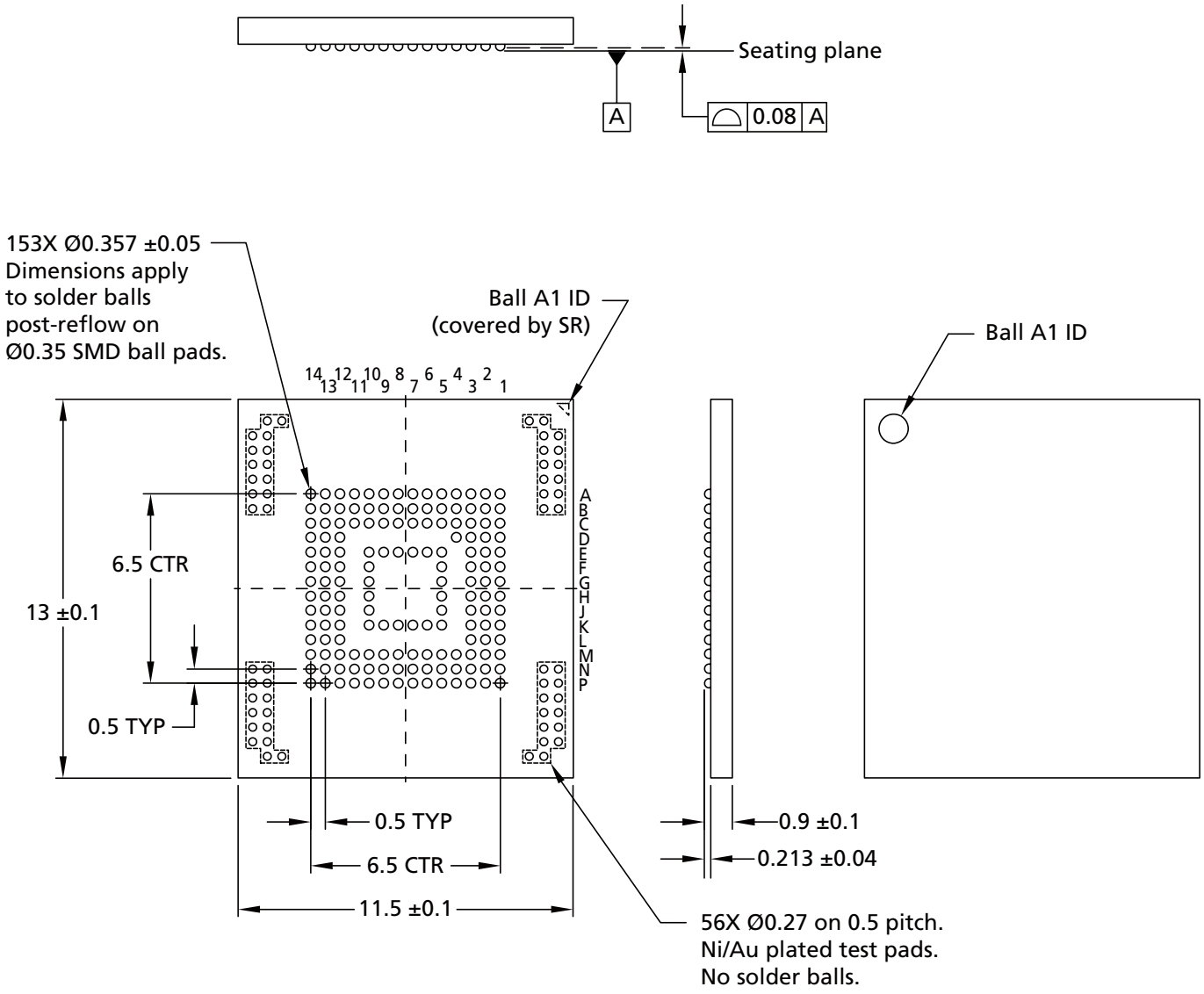


Notes: 1. Dimensions are in millimeters.
2. The package height does not include room temperature warpage.
3. In the whole eMMC package area, solder mask is recommended to cover the via pad in the PCB in order to avoid possible contact with Ni/Au plated test pads on the eMMC package. The Ni/Au plated test pads are reserved for Micron internal use only.

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Figure 4: 153-Ball VFBGA – 11.5mm x 13.0mm x 1.0mm (Package Code: JP)



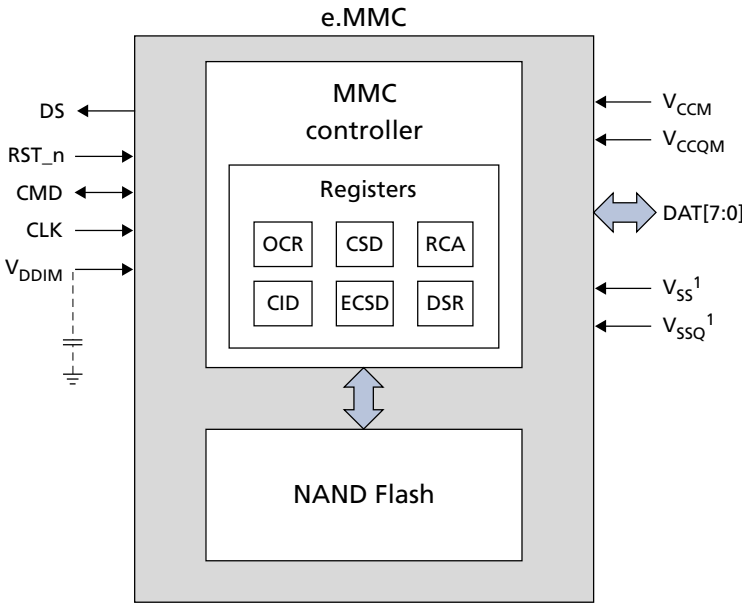
Notes: 1. Dimensions are in millimeters.
2. The package height does not include room temperature warpage.
3. In the whole eMMC package area, solder mask is recommended to cover the via pad in the PCB in order to avoid possible contact with Ni/Au plated test pads on the eMMC package. The Ni/Au plated test pads are reserved for Micron internal use only.

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Architecture

Figure 5: e.MMC Functional Block Diagram



Note: 1. V_{SS} and V_{SSQ} are internally connected.

MMC Protocol Independent of NAND Flash Technology

The MMC specification defines the communication protocol between a host and a device. The protocol is independent of the NAND flash features included in the device. The device has an intelligent on-board controller that manages the MMC communication protocol.

The controller also handles block management functions such as logical block allocation and wear leveling. These management functions require complex algorithms and depend entirely on NAND flash technology (generation or memory cell type). The device handles these management functions internally, making them invisible to the host processor.

Defect and Error Management

Micron e.MMC incorporates advanced technology for defect and error management. If a defective block is identified, the device completely replaces it with a spare block. This process is invisible to the host and does not affect user-allocated data space.

The device also includes a built-in error correction code (ECC) algorithm to ensure data integrity is maintained. To best implement these advanced technologies and ensure proper data loading and storage over the life of the device, the host must follow these precautions:

- Check the status after WRITE, READ, and ERASE operations.
- Avoid power-down during WRITE and ERASE operations.

As best practice, Micron recommends the usage of Power Off Notification (PON) and refresh mechanism.

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OCR Register

The 32-bit operation conditions register (OCR) stores the voltage profile of the card and the access mode indication. In addition, this register includes a status information bit.

Table 7: OCR Parameters

OCR Bits	OCR Value	Description
[31]	1b (ready)/0b (busy)[1]	Device power-on status bit
[30:29]	10b	Sector mode
[28:24]	0 0000b	Reserved
[23:15]	1 1111 1111b	2.7–3.6V voltage range
[14:8]	000 0000b	2.0–2.7V voltage range
[7]	1b	1.70–1.95V voltage range
[6:0]	000 0000b	Reserved

Note: 1. OCR = C0FF8080h after the device has completed power-up.

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CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by e.MMC protocol. Each device is created with a unique identification number.

Table 8: CID Register Field Parameters

Name	Field	Width	CID Bits	CID Value
Manufacturer ID	MID	8	[127:120]	13h
Reserved	–	6	[119:114]	–
Card/BGA	CBX	2	[113:112]	01h
OEM/application ID	OID	8	[111:104]	–
Product name	PNM	48	[103:56]	32GB: 47314D31354Ch (G1M15L)
				64GB: 47314D31354Dh (G1M15M)
				128GB:47314D31354Eh (G1M15N)
Product revision	PRV	8	[55:48]	–
Product serial number	PSN	32	[47:16]	–
Manufacturing date	MDT	8	[15:8]	–
CRC7 checksum	CRC	7	[7:1]	–
Not used; Always 1	–	1	[0]	–

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CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

Table 9: CSD Register Field Parameters

Name	Field	Density	Size (Bits)	Cell Type[1]	CSD Bits	CSD Value
CSD structure	CSD_STRUCTURE	–	2	R	[127:126]	3h
System specification version	SPEC_VERS	–	4	R	[125:122]	4h
Reserved[2]	–	–	2	R	[121:120]	–
Data read access time 1	TAAC[3]	–	8	R	[119:112]	7Fh
Data read access time 2 in CLK cycles (NSAC × 100)	NSAC[3]	–	8	R	[111:104]	01h
Maximum bus clock frequency	TRAN_SPEED	–	8	R	[103:96]	32h
Card command classes	CCC	–	12	R	[95:84]	8F5h
Maximum read data block length	READ_BL_LEN	–	4	R	[83:80]	09h
Partial blocks for reads supported	READ_BL_PARTIAL	–	1	R	[79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	–	1	R	[78]	0h
Read block misalignment	READ_BLK_MISALIGN	–	1	R	[77]	0h
DSR implemented	DSR_IMP	–	1	R	[76]	0h
Reserved	–	–	2	R	[75:74]	–
Device size	C_SIZE	–	12	R	[73:62]	FFFh
Maximum read current at $V_{DD,min}$	VDD_R_CURR_MIN	–	3	R	[61:59]	0h
Maximum read current at $V_{DD,max}$	VDD_R_CURR_MAX	–	3	R	[58:56]	0h
Maximum write current at $V_{DD,min}$	VDD_W_CURR_MIN	–	3	R	[55:53]	0h
Maximum write current at $V_{DD,max}$	VDD_W_CURR_MAX	–	3	R	[52:50]	0h
Device size multiplier	C_SIZE_MULT	–	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	–	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	–	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	–	5	R	[36:32]	0Fh
Write protect group enable	WP_GRP_ENABLE	–	1	R	[31]	1h
Manufacturer default ECC	DEFAULT_ECC	–	2	R	[30:29]	0h
Write-speed factor	R2W_FACTOR[3]	–	3	R	[28:26]	03h
Maximum write data block length	WRITE_BL_LEN	–	4	R	[25:22]	09h

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Table 9: CSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bits)	Cell Type[1]	CSD Bits	CSD Value
Partial blocks for writes supported	WRITE_BL_PARTIAL	–	1	R	[21]	0h
Reserved	–	–	4	R	[20:17]	–
Content protection application	CONTENT_PROT_APP	–	1	R	[16]	0h
File-format group	FILE_FORMAT_GRP	–	1	R/W	[15]	0h
Copy flag (OTP)	COPY	–	1	R/W	[14]	0h
Permanent write protection	PERM_WRITE_PROTECT	–	1	R/W	[13]	0h
Temporary write protection	TMP_WRITE_PROTECT	–	1	R/W/E	[12]	0h
File format	FILE_FORMAT	–	2	R/W	[11:10]	0h
ECC	ECC	–	2	R/W/E	[9:8]	0h
CRC	CRC	–	7	R/W/E	[7:1]	–
Not used, always 1	–	–	1	–	[0]	–

Notes: 1. R = Read-only;
R/W = One-time programmable and readable;
R/W/E = Multiple writable with value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable
2. Reserved bits should be read as 0.
3. Host should calculate the write time-out conditions as per JEDEC specification, using CSD register values TAAC, NSAC, and R2W_FACTOR, or higher. Lower time out values may result in application hang, loop forced reset, or re-boot. Additional information is provided in a separate document upon customer request.

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ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

Table 10: ECSD Register Field Parameters

Name	Field	Density	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Properties Segment						
Reserved[2]	–	–	6	TBD	[511:506]	–
Extended security error support	EXT_SECURITY_ERR	–	1	R	[505]	00h
Supported command sets	S_CMD_SET	–	1	R	[504]	01h
HPI features	HPI_FEATURES	–	1	R	[503]	01h
Background operations support	BKOPS_SUPPORT	–	1	R	[502]	01h
Max-packed READ commands	MAX_PACKED_READS	–	1	R	[501]	00h
Max-packed WRITE commands	MAX_PACKED_WRITES	–	1	R	[500]	00h
Data tag support	DATA_TAG_SUPPORT	–	1	R	[499]	01h
Tag unit size	TAG_UNIT_SIZE	–	1	R	[498]	03h
Tag resources size	TAG_RES_SIZE	–	1	R	[497]	00h
Context management capabilities	CONTEXT_CAPABILITIES	–	1	R	[496]	05h
Large unit size	LARGE_UNIT_SIZE_M1	–	1	R	[495]	03h
Extended partitions attribute support	EXT_SUPPORT	–	1	R	[494]	03h
Supported modes	SUPPORTED_MODES	–	1	R	[493]	01h
Field firmware update features	FFU_FEATURES	–	1	R	[492]	00h
Operation code timeout	OPERATION_CODE_TIMEOUT	–	1	R	[491]	00h
Field firmware update arguments	FFU_ARG	–	4	R	[490:487]	0000FFFFh
Barrier support	BARRIER_SUPPORT	–	1	R	[486]	01h
Reserved	–	–	177	TBD	[485:309]	–
CMD queuing support	CMDQ_SUPPORT	–	1	R	[308]	01h
CMD queuing depth	CMDQ_DEPTH	–	1	R	[307]	1Fh
Reserved	–	–	1	TBD	[306]	–
Number of firmware sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	–	4	R	[305:302]	00h

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Table 10: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Vendor proprietary health report	VENDOR_PROPRI-ETARY_HEALTH_REPORT	–	32	R	[301:270]	00h
Device life time estimate type B	DEVICE_LIFE_TIME_EST_TYP_B	–	1	R	[269]	01h
Device life time estimate type A	DEVICE_LIFE_TIME_EST_TYP_A	–	1	R	[268]	01h
Pre-end of life information	PRE_EOL_INFO	–	1	R	[267]	01h
Optimal read size	OPTIMAL_READ_SIZE	–	1	R	[266]	00h
Optimal write size	OPTIMAL_WRITE_SIZE	–	1	R	[265]	40h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	–	1	R	[264]	00h
Device version	DEVICE_VERSION	–	2	R	[263:262]	0000h
Firmware version	FIRMWARE_VERSION	–	8	R	[261:254]	–
Power class for 200 MHz DDR at V_{CC} = 3.6V	PWR_CL_DDR_200_360	–	1	R	[253]	00h
Cache size	CACHE_SIZE	32GB	4	R	[252:249]	00000800h
		64GB				
		128GB				
Generic CMD6 timeout	GENERIC_CMD6_TIME	–	1	R	[248]	0Ah
Power-off notification (long) timeout	POWER_OFF_LONG_TIME	–	1	R	[247]	32h
Background operations status	BKOPS_STATUS	–	1	R	[246]	00h
Number of correctly programmed sectors	CORRECTLY_PROG_SECTORS_-NUM	–	4	R	[245:242]	00000000h
First initialization time after partitioning (first CMD1 to device ready)	INI_TIMEOUT_AP	–	1	R	[241]	0Ah
Cache flushing policy	CACHE_FLUSH_POLICY	–	1	R	[240]	01h
Power class for 52 MHz, DDR at 3.6V	PWR_CL_DDR_52_360	–	1	R	[239]	00h
Power class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195	–	1	R	[238]	00h
Power class for 200 MHz at 1.95V	PWR_CL_200_195	–	1	R	[237]	00h
Power class for 200 MHz, at 1.3V	PWR_CL_200_130	–	1	R	[236]	00h
Minimum write performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52	–	1	R	[235]	00h
Minimum read performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52	–	1	R	[234]	00h

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Table 10: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Reserved	–	–	1	TBD	[233]	–
TRIM multiplier	TRIM_MULT	–	1	R	[232]	01h
Secure feature support	SEC_FEATURE_SUPPORT	–	1	R	[231]	51h
Secure erase multiplier	SEC_ERASE_MULT	–	1	R	[230]	01h
Secure trim multiplier	SEC_TRIM_MULT	–	1	R	[229]	01h
Boot information	BOOT_INFO	–	1	R	[228]	07h
Reserved	–	–	1	TBD	[227]	–
Boot partition size[3]	BOOT_SIZE_MULT	–	1	R	[226]	FCh
Access size	ACC_SIZE	–	1	R	[225]	00h
High-capacity erase unit size	HC_ERASE_GRP_SIZE	–	1	R	[224]	01h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	–	1	R	[223]	01h
Reliable write-sector count	REL_WR_SEC_C	–	1	R	[222]	01h
High-capacity write protect group size	HC_WP_GRP_SIZE	32GB	1	R	[221]	10h
		64GB				20h
		128GB				40h
Sleep current (V_{CC})	S_C_VCC	–	1	R	[220]	00h
Sleep current (V_{CCQ})	S_C_VCCQ	–	1	R	[219]	00h
Production state awareness timeout	PRODUCTION_STATE_AWARE-NESS_TIMEOUT	–	1	R	[218]	00h
Sleep/awake timeout	S_A_TIMEOUT	–	1	R	[217]	14h
Sleep notification timeout	SLEEP_NOTIFICATION_TIME	–	1	R	[216]	0Eh
Sector count	SEC_COUNT	32GB	4	R	[215:212]	03B48000h
		64GB				07690000h
		128GB				0ED20000h
Secure write protect information	SECURE_WP_INFO	–	1	R	[211]	01h
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52	–	1	R	[210]	00h
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52	–	1	R	[209]	00h
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52	–	1	R	[208]	00h
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52	–	1	R	[207]	00h
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26	–	1	R	[206]	00h

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Table 10: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26	–	1	R	[205]	00h
Reserved	–	–	1	TBD	[204]	–
Power class for 26 MHz at 3.6V	PWR_CL_26_360	–	1	R	[203]	00h
Power class for 52 MHz at 3.6V	PWR_CL_52_360	–	1	R	[202]	00h
Power class for 26 MHz at 1.95V	PWR_CL_26_195	–	1	R	[201]	00h
Power class for 52 MHz at 1.95V	PWR_CL_52_195	–	1	R	[200]	00h
Partition switching timing	PARTITION_SWITCH_TIME	–	1	R	[199]	01h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	–	1	R	[198]	0Fh
I/O driver strength	DRIVER_STRENGTH	–	1	R	[197]	1Fh
Device type	DEVICE_TYPE	–	1	R	[196]	57h
Reserved	–	–	1	TBD	[195]	–
CSD structure version	CSD_STRUCTURE	–	1	R	[194]	02h
Reserved	–	–	1	TBD	[193]	–
Extended CSD revision	EXT_CSD_REV	–	1	R	[192]	08h
Modes Segment						
Command set	CMD_SET	–	1	R/W/E_P	[191]	00h
Reserved	–	–	1	TBD	[190]	–
Command set revision	CMD_SET_REV	–	1	R	[189]	00h
Reserved	–	–	1	TBD	[188]	–
Power class	POWER_CLASS	–	1	R/W/E_P	[187]	00h
Reserved	–	–	1	TBD	[186]	–
High-speed interface timing	HS_TIMING	–	1	R/W/E_P	[185]	00h
Strobe support	STROBE_SUPPORT	–	1	R	[184]	01h
Bus width mode	BUS_WIDTH	–	1	W/E_P	[183]	00h
Reserved	–	–	1	TBD	[182]	–
Erased memory content	ERASED_MEM_CONT	–	1	R	[181]	00h
Reserved	–	–	1	TBD	[180]	–
Partition configuration	PARTITION_CONFIG	–	1	R/W/E, R/W/E_P	[179]	00h
Boot configuration protection	BOOT_CONFIG_PROT	–	1	R/W, R/W/C_P	[178]	00h
Boot bus conditions	BOOT_BUS_CONDITIONS	–	1	R/W/E	[177]	00h
Reserved	–	–	1	TBD	[176]	–

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Table 10: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
High-density erase group definition	ERASE_GROUP_DEF	–	1	R/W/E_P	[175]	00h
Boot write protection status registers	BOOT_WP_STATUS	–	1	R	[174]	00h
Boot area write protection register	BOOT_WP	–	1	R/W, R/W/C_P	[173]	00h
Reserved	–	–	1	TBD	[172]	–
User write protection register	USER_WP	–	1	R/W, R/W/C_P, R/W/E_P	[171]	00h
Reserved	–	–	1	TBD	[170]	–
Firmware configuration	FW_CONFIG	–	1	R/W	[169]	00h
RPMB size	RPMB_SIZE_MULT	–	1	R	[168]	20h
Write reliability setting register[4] Write reliability parameter register	WR_REL_SET	–	1	R/W	[167]	1Fh
	WR_REL_PARAM	–	1	R	[166]	15h
SANITIZE START operation	SANITIZE_START	–	1	W/E_P	[165]	00h
Manually start background operations	BKOPS_START	–	1	W/E_P	[164]	00h
Enable background operations handshake	BKOPS_EN	–	1	R/W, R/W/E	[163]	02h
Hardware reset function	RST_n_FUNCTION	–	1	R/W	[162]	00h
HPI management	HPI_MGMT	–	1	R/W/E_P	[161]	00h
Partitioning support	PARTITIONING_SUPPORT	–	1	R	[160]	07h
Maximum enhanced area size	MAX_ENH_SIZE_MULT	32GB	3	R	[159:157]	0004F0h
		64GB				0004F0h
		128GB				0004F0h
Partitions attribute	PARTITIONS_ATTRIBUTE	–	1	R/W	[156]	00h
Partitioning setting	PARTITION_SETTING_COMPLETED	–	1	R/W	[155]	00h
General-purpose partition size	GP_SIZE_MULT	–	12	R/W	[154:143]	00h
Enhanced user data area size	ENH_SIZE_MULT	–	3	R/W	[142:140]	000000h
Enhanced user data start address	ENH_START_ADDR	–	4	R/W	[139:136]	00000000h
Reserved	–	–	1	TBD	[135]	–
Bad block management mode	SEC_BAD_BLK_MGMNT	–	1	R/W	[134]	00h
Production state awareness	PRODUCTION_STATE_AWARENESS	–	1	R/W/E	[133]	00h
Package case temperature is controlled	TCASE_SUPPORT	–	1	W/E_P	[132]	00h

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Table 10: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Periodic wake-up	PERIODIC_WAKEUP	–	1	R/W/E	[131]	00h
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	–	1	R	[130]	01h
Reserved	–	–	2	TBD	[129:128]	–
Vendor specific fields	VENDOR_SPECIFIC_FIELD	–	64	<vendor specific>	[127:64]	–
Native sector size	NATIVE_SECTOR_SIZE	–	1	R	[63]	00h
Sector size emulation	USE_NATIVE_SECTOR	–	1	R/W	[62]	00h
Sector size	DATA_SECTOR_SIZE	–	1	R	[61]	00h
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	–	1	R	[60]	00h
Class 6 commands control	CLASS_6_CTRL	–	1	R/W/E_P	[59]	00h
Number of addressed group to be released	DYNCAP_NEEDED	–	1	R	[58]	00h
Exception events control	EXCEPTION_EVENTS_CTRL	–	2	R/W/E_P	[57:56]	0000h
Exception events status	EXCEPTION_EVENTS_STATUS	–	2	R	[55:54]	0000h
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	–	2	R/W	[53:52]	0000h
Context configuration	CONTEXT_CONF	–	15	R/W/E_P	[51:37]	00h
Packed command status	PACKED_COMMAND_STATUS	–	1	R	[36]	00h
Packed command failure index	PACKED_FAILURE_INDEX	–	1	R	[35]	00h
Power-off notification	POWER_OFF_NOTIFICATION	–	1	R/W/E_P	[34]	00h
Control to turn the cache on/off	CACHE_CTRL	–	1	R/W/E_P	[33]	00h
Flushing of the cache	FLUSH_CACHE	–	1	W/E_P	[32]	00h
Control to turn the barrier on/off	BARRIER_CTRL	–	1	R/W	[31]	00h
Mode configuration	MODE_CONFIG	–	1	R/W/E_P	[30]	00h
Mode operation codes	MODE_OPERATION_CODES	–	1	W/E_P	[29]	00h
Reserved	–	–	2	TBD	[28:27]	–
Field firmware update status	FFU_STATUS	–	1	R	[26]	00h
Pre-loading data size	PRE LOADING DATA SIZE	–	4	R/W/E_P	[25:22]	00h
Maximum pre-loading data size	MAX_PRE_LOADING_DATA_SIZE	32GB	4	R	[21:18]	035B9400h
		64GB				06B72800h
		128GB				0D6E5000h
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	–	1	R/W/E&R	[17]	03h
Secure removal type	SECURE_REMOVAL_TYPE	–	1	R/W&R	[16]	01h

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Table 10: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Command queue mode enable	CMDQ_MODE_EN	–	1	R/W/E_P	[15]	00h
Reserved	–	–	15	TBD	[14:0]	–

Notes: 1. R = Read-only;
R/W = One-time programmable and readable;
R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable;
R/W/C_P = Writable after the value is cleared by a power cycle and assertion of the RST_n signal (the value not cleared by CMD0 reset) and readable;
R/W/E_P = Multiple writable with the value reset after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable;
W/E_P = Multiple writable with the value reset after power cycle, assertion of the RST_n signal, and any CMD0 reset, and not readable
2. Reserved bits should be read as 0.
3. Boot partition size is configurable by host. Refer to local Micron support for information.
4. Micron has tested power failure under best-application knowledge conditions with positive results. Customers may request a dedicated test for their specific application condition. Micron set this register during factory test and used the one-time programming option.

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DC Electrical Specifications – Device Power

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is used for the NAND Flash device ; V_{CCQ} is used for the controller and for the e.MMC and NAND interface voltage.

Figure 6: Device Power Diagram

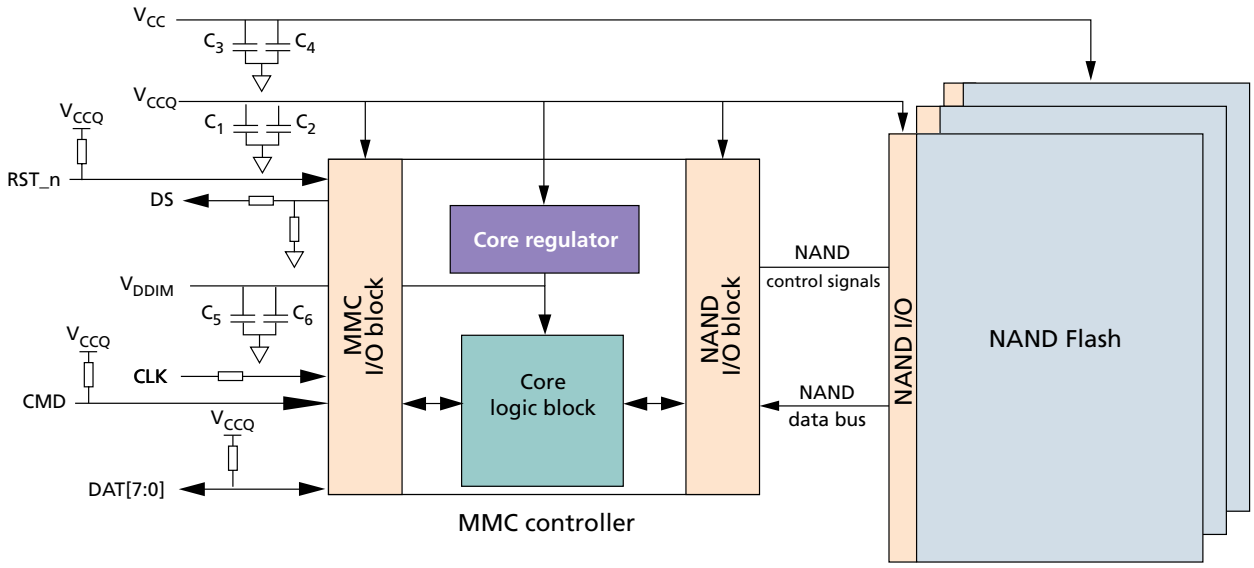


Table 11: Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Voltage input	V_{IN}	–0.2	2.4	V
V_{CC} supply	V_{CC}	–0.6	4.6	V
V_{CCQ} supply	V_{CCQ}	–0.2	2.4	V

Note: 1. Voltage on any pin relative to V_{SS}.

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Table 12: Capacitor and Resistance Specifications

Parameter	Symbol	Min	Max	Typ	Units	Notes
Pull-up resistance: CMD	R_CMD	4.7	50	10	kΩ	1
Pull-up resistance: DAT[7:0]	R_DAT	10	50	50	kΩ	1
Pull-up resistance: RST_n	R_RST_n	4.7	50	50	kΩ	2
CLK/CMD/DS/DAT[7:0] impedance		45	55	50	Ω	3
Serial resistance on CLK	SR_CLK	0	47	22	Ω	
Serial resistance on DS	SR_DS	0	47	22	Ω	4
Pull-down resistance: DS	R_DS	10	100	–	kΩ	
V_{CCQ} capacitor	C1	2.2	4.7	2.2	µF	5
	C2	0.1	0.22	0.1		
V_{CC} capacitor	C3	2.2	4.7	2.2	µF	6
	C4	0.1	0.22	0.1		
V_{DDIM} capacitor (C_{reg})	C5	1	4.7	1	µF	7
	C6	0.1	0.1	0.1		

Notes: 1. Used to prevent bus floating.
2. If host does not use H/W RESET (RST_n), pull-up resistance is not needed on RST_n line (Extended_CSD[162] = 00h).
3. Impedance match.
4. Recommended in order to compensate eventual impedance mismatch on the PCB.
5. The coupling capacitor should be connected with V_{CCQ} and V_{SSQ} as closely as possible.
6. The coupling capacitor should be connected with V_{CC} and V_{SS} as closely as possible.
7. The coupling capacitor should be connected with V_{DDIM} and V_{SS} as closely as possible.

Product Features

The list below shows the JEDEC features not supported. See the full JEDEC/MMC Standard No. 84-B51 available at www.jedec.org/sites/default/files/docs/JESD84-B51.pdf

- Packed CMDs
- Context ID/Data tag (this feature is implemented at the protocol level)
- Dynamic device capacity
- Thermal spec
- Large sector size - 4KB (<256GB)
- Extended security protocol
- Secure erase/secure trim*
- Forced erase*

* The feature implements as logical erase mode: It moves the mapped host address range to the unmapped host address range. When the operation is complete, the data still exists, but the mapped device address range behaves as if overwritten with all 0s.

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Revision History

Rev. C – 09/2021

- Updated legal status to Production
- Updated temperature ranges
- Remove ES from WT MPNs
- Updated VSF pins description
- Updated CSD register: Updated write-speed factor value; Added note 3

Rev. B – 05/2021

- Updated Features section
- Added Note 3 to Package Dimensions section
- Updated Ordering Information Table: Removed ES from IT MPNs
- Updated ECSD Register Field Parameters table

Rev. A – 01/2021

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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