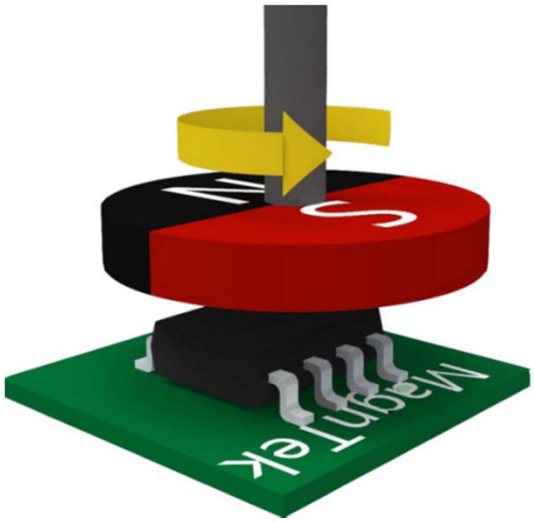
MT6815

Magnetic Angle Position Encoder Sensor

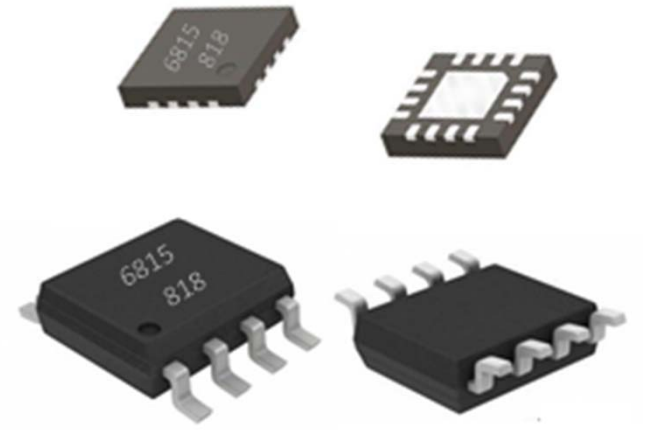
Features and Benefits

- Based on advanced AMR Sensing Technology with 0°~360° Full Range Angle Sensing
- Contactless Angle Measurement
- Independent Output Interface: I²C, SPI, Analog， ABZ, PWM and UVW
- Incremental ABZ programmable binary and decimal pulse-counts: 32, 48, 64, 128, 256, 512, 1024, 2048, 100, 200, 500, 1000, 2000, 2500 pulses per cycle
- 14 bit Core Resolution
- 12 bit DAC/PWM Resolution
- User Programmable Resolution & Zero Index Position
- RoHS Compliant 2011/65/EU
- SOP-8 or QFN-16 Package



Applications

- Absolute Linear Position Sensor
- BLDC Motor Control
- Robotics Control
- Contactless Potentiometer



General Description

The MagnTek rotary position sensor MT6815 is an IC based on advanced AMR magnetic sensing technology. A rotating magnetic field in the x-y sensor plane delivers two sinusoidal output signals indicating the angle (α) between the sensor and the magnetic field direction. Within a homogeneous field in the x-y plane, the output signals are relatively independent of the physical placement in the z direction.

The sensor is only sensitive to the magnetic field direction as the sensing element output is specially designed to be independent from the magnet field strength. This allows the device to be less sensitive to magnet variations, stray magnetic fields, air gap changes and off-axis misalignment.

The incremental ABZ output mode is available in this sensor series, making the chip suitable to replace various optical encoders. The maximum resolution is 2048 pulse/8192 steps per revolution in binary mode and 2500 pulse/10000 steps per revolution in decimal mode.

A standard I²C or SPI (3-Wire or 4-Wrie) interface allows a host microcontroller to read the 14-bit absolute angle position data from MT6815. The absolute angle position is also provided as PWM output or linear analog signal proportional to

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1. Pin Configuration

1. 1 SOP-8 Package

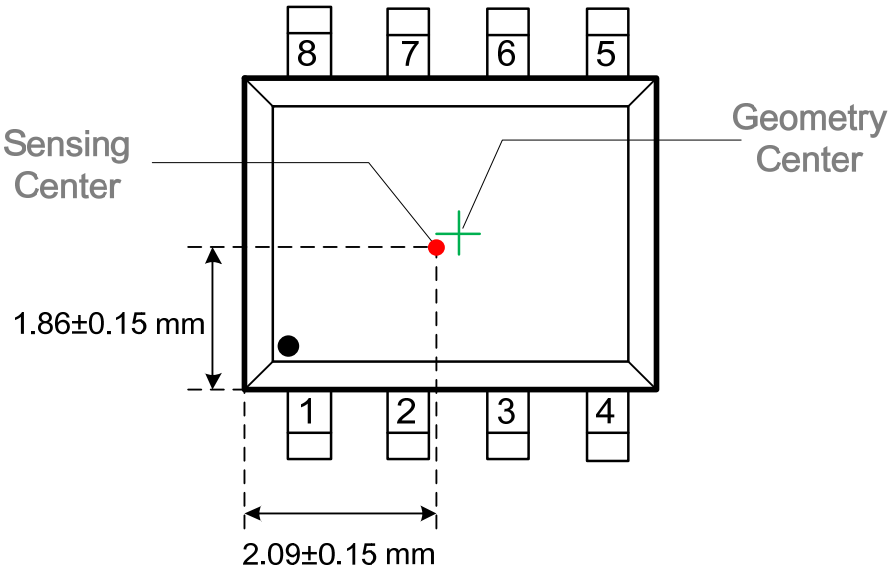


Figure 1: Pin Configuration for SOP-8 Package

Pin List

Name	#	Type	Description
CSN	1	Digital Input	SPI/I²C Selection
HVPP	2	Analog Input	OTP Programming Supply or SPI/I²C Selection
OUT	3	Analog/Digital Output	Analog or PWM Output
VDD	4	Power Supply	3.3~5.0V Supply
A/U	5	Digital Input/output	Incremental Signal A/U or Speed or SPI MOSI, SDAT or I²C Data
B/V	6	Digital Input/output	Incremental Signal B/V or Direction or SPI MISO
Z/W	7	Digital Input	Incremental Signal Z/W or Index or SPI Clock or I²C Clock
GND	8	Ground	Ground

Family Members

Part Number	Description
MT6815CT	SOP-8 Package, Tube Pack (100pcs/Tube) or Tape & Reel Pack (3000pcs/Reel)

SOP-8 Reflow Sensitivity Classification: MSL-3

1. 2 QFN-16 Package

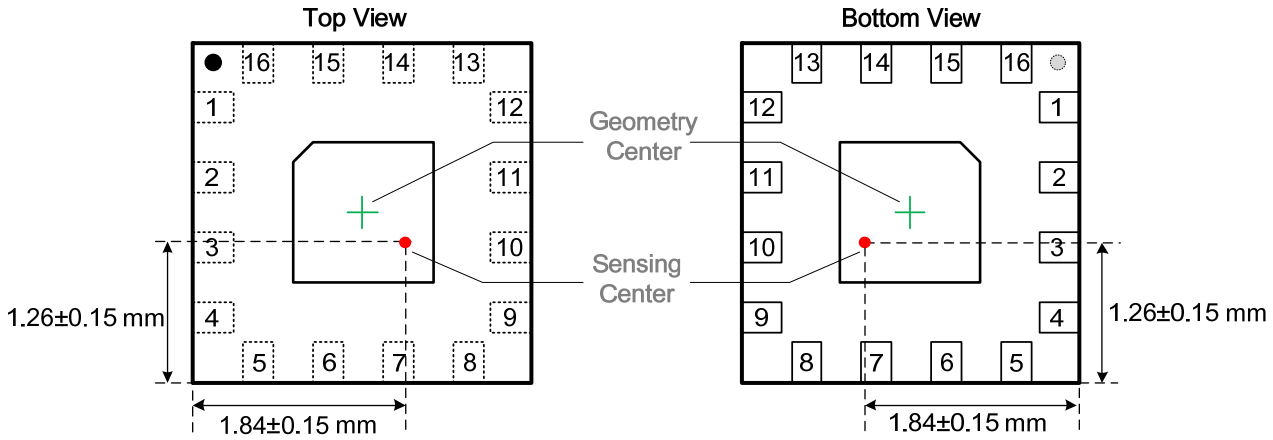


Figure 2: Pin Configuration for QFN-16 Package

Pin List

Name	#	Type	Description
A	1	Digital Input/output	Incremental Signal A or Speed or SPI MOSI, SDAT or I²C Data
B	2	Digital Input/output	Incremental Signal B or Direction or SPI MISO
Z	3	Digital Input	Incremental Signal Z or Index or SPI Clock or I²C Clock
GND	4	Ground	Ground
CSN	5	Digital Input	SPI/I²C Selection
NC	6	-	-
NC	7	-	-
NC	8		-
NC	9	-	-
NC	10	-	-
OUT	11	Analog/Digital Output	Analog or PWM Output
HVPP	12	Analog Input	OTP Programming Supply or SPI/I²C Selection
W	13	-	Incremental Output W
V	14	-	Incremental Output V or –B
U	15	-	Incremental Output U or –A
VDD	16	Power Supply	3.3~5.0V Supply

Family Members

Part Number	Description
MT6815QT	QFN-16 Package, Reel Pack (3000pcs/Reel)

QFN-16 Reflow Sensitivity Classification: MSL-1

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Web:www.manduic.com
Email:sales@manduic.com

2. Functional Diagram

The MT6815 is manufactured in a CMOS standard process and uses advanced magnet sensing technology to sense the magnetic field distribution across the surface of the chip. The integrated magnetic sensing element array is placed around the center of the device and delivers a voltage representation of the magnetic field at the surface of the IC.

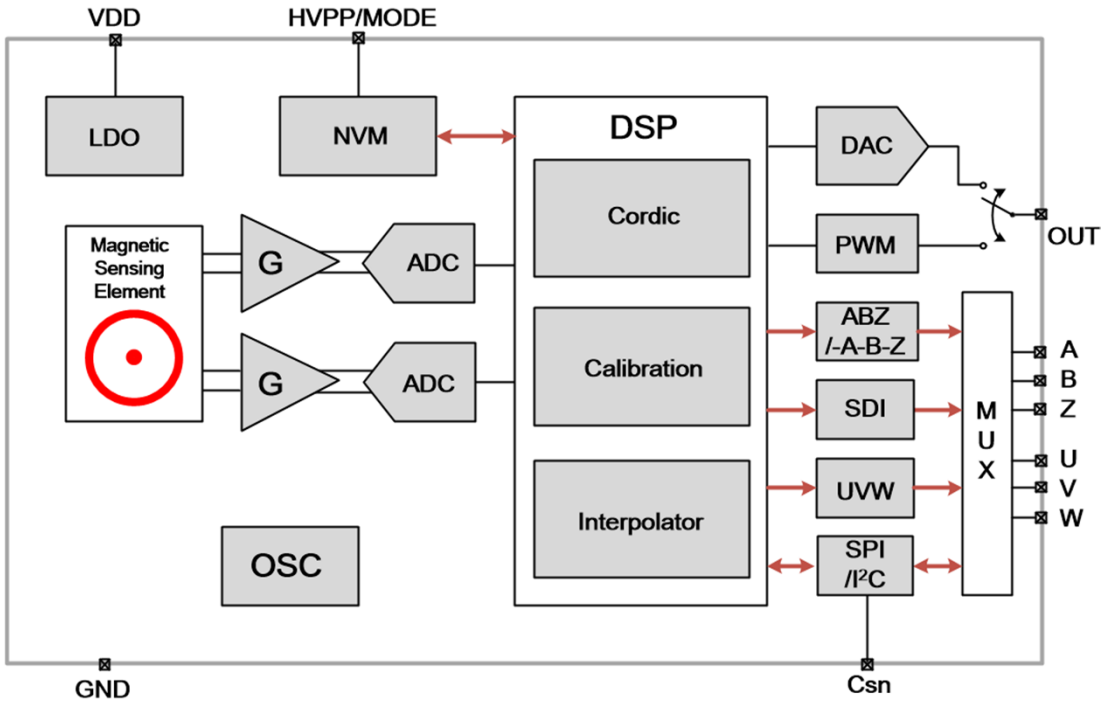


Figure 3: Block Diagram

Figure 3 shows a simplified block diagram of the chip, consisting of the magnetic sensing element modeled by two interleaved Wheatstone bridges to generate cosine and sine signals, gain stages, analog-to-digital converters (ADC) for signal conditioning, and a digital signal processing (DSP) unit for encoding. Other supporting blocks such as LDO, etc. are also included.

3. Absolute Maximum Ratings (Non-Operating)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Name	Min.	Max.	Unit
DC Voltage at Pin VDD	-0.5	7	V
DC Voltage at Pin HVPP	-0.5	8	V
Storage Temperature	-55	150	℃
Operating Temperature	-40	125	℃
Electrostatic Discharge (HBM)	-	±3.0	KV
Electrostatic Discharge (CDM)	-	±1.5	KV

4. Electrical Characteristics

Operation conditions: Ta=-40 to 125℃, VDD=3.0~5.5V unless otherwise noted.

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-	3.0	3.3~5.0	5.5	V
HVPP	Supply Voltage	-	6.75	7.0	7.25	V
Idd	Supply Current	-	-	6.0	9.0	mA
LSB	Resolution (ABZ or SDI Mode)	N Steps per Cycle		360°/N		°
INL	Integral Non-Linearity	Note (1)	-	±1	±1.5	°
DNL	Differential Non-Linearity (ABZ or SDI Mode), Figure 4	≤10 bit	-	-	±0.1	LSB
		>10bit	-	-	±0.03	°
TN	Transition Noise (ABZ or SDI Mode)	25℃	-	-	0.011	°rms
Hyst	Hysteresis (ABZ Mode)	≤12bit	-	0.5	-	LSB
		>12bit	-	0.176	-	°
T_{PwrUp}	Power-Up Time	VDD Ramp<10us	-	-	1.0	ms
T_{Delay}	Propagation Delay	Without Delay Compensation		400	480	μs
		With Delay Compensation		20	30	μs
Analog Output Specification						
R_{OUT}	Analog Output Resistance	-	-	15	30	Ω
R_L	Pull-Up or Pull-Down	-	1K	-	-	Ω
C_L	Loading Capacitor	-	-	-	100	nF
V_{Sat_High}	Saturation High Voltage	I_{Load}=1mA	95	98	-	%VDD
V_{Sat_Low}	Saturation Low Voltage	I_{Load}=1mA	-	2	5	%VDD
DAC_LSB	DAC LSB	12 bit DAC	-	0.025		%VDD
DAC_INL	DAC Integral Non-Linearity	-	-	-	±3	LSB
DAC_DNL	DAC Differential Non-Linearity	-	-	-	±1.5	LSB
V_{Noise}	Analog Output Noise	Ta=25℃, RMS Value excluding DAC Quantization Noise			0.02	%VDD
Erm	Ratiometric Error	Note (2)	-0.3	-	0.3	%
PWM Output Characteristics						
FPWM	PWM Frequency	Programmable	-5% @27℃	625 /1250 /2500 /5000	+5% @27℃	Hz
T_{Rise}	Rising Time	C_L=1nF	-	-	1	us
T_{Fall}	Falling Time	C_L=1nF	-	-	1	us

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Digital I/O Characteristics (Push-Pull Type in Normal Mode)						
V_{IH}	High Level Input Voltage	-	0.7*VDD	-	-	V
V_{IL}	Low Level Input Voltage	-	-	-	0.3*VDD	V
V_{OH}	GPIO Output High Level	Push-pull (Iout=2mA)	VDD-0.1	-	-	V
V_{OL}	GPIO Output Low Level	Push-pull (Iout=2mA)	-	-	0.1	V
I_{LK}	Input Leakage Current	-	-	-	±1	μA
Timing Specifications						
Tiov	Incremental Output Valid Time	Programmable	-	-	1	μs

Note (1): The typical error value can be achieved at room temperature and with no off-axis misalignment error. The maximum error value can be achieved over operation temperature range, at maximum air gap and with worst-case off-axis misalignment error.

Note (2): The analog output is by design ratiometric, i.e. it is proportional to the supply voltage VDD. The ratiometric error is calculated as follows.

$$\mathrm{Erm} = [\frac{Vout(V_{DD})}{V_{DD}} - \frac{Vout(5\mathrm{V})}{5V}] \cdot 100\%$$

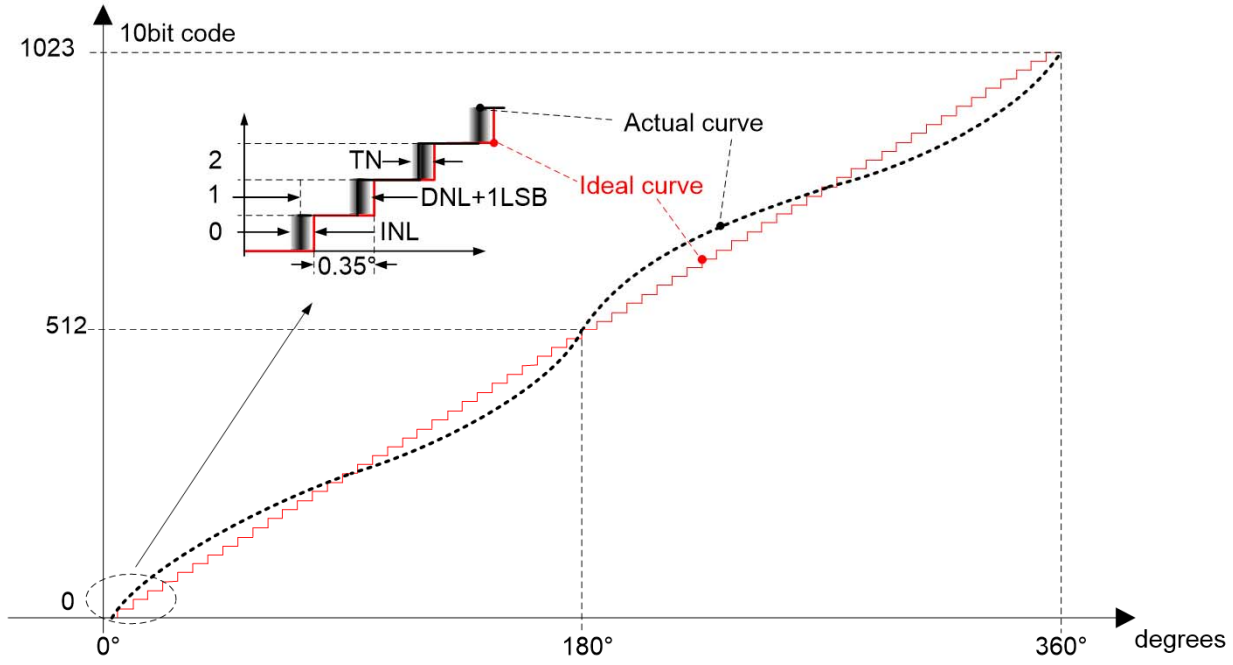


Figure 4: Drawing Illustration INL, DNL and TN (for 10 bit case)

5. Magnetic Input Specifications

Operation conditions: Ta=-40 to 125℃, VDD=3.0~5.5V unless otherwise noted, two-pole cylindrical diametrically magnetized source.

Symbol	Parameter	Conditions/Notes	Min.	Typ.	Max.	Unit
Dmag	Diameter of Magnet	Recommended Magnet: Ø8mm x 2.5mm for Cylindrical Magnets	-	8.0	-	mm
Tmag	Thickness of Magnet		-	2.5	-	mm
Bpk	Magnetic Input Field Amplitude	Measure at the IC Surface	200	-	10000	Guass
AG	Air Gap	Magnetic to IC Surface Distance	-	-	3.0	mm
RS	Rotation Speed		-	-	10000	RPM
DISP	Off Axis Misalignment	Misalignment Error Between Sensor Sensing Center and Magnet Axis (See Figure 5)	-	-	0.3	mm
TCmag1	Recommended Magnet Material and Temperature Drift Coefficient	NdFeB (Neodymium Iron Boron)	-	-0.12	-	%/℃
TCmag2		SmCo (Samarium Cobalt)	-	-0.035	-	

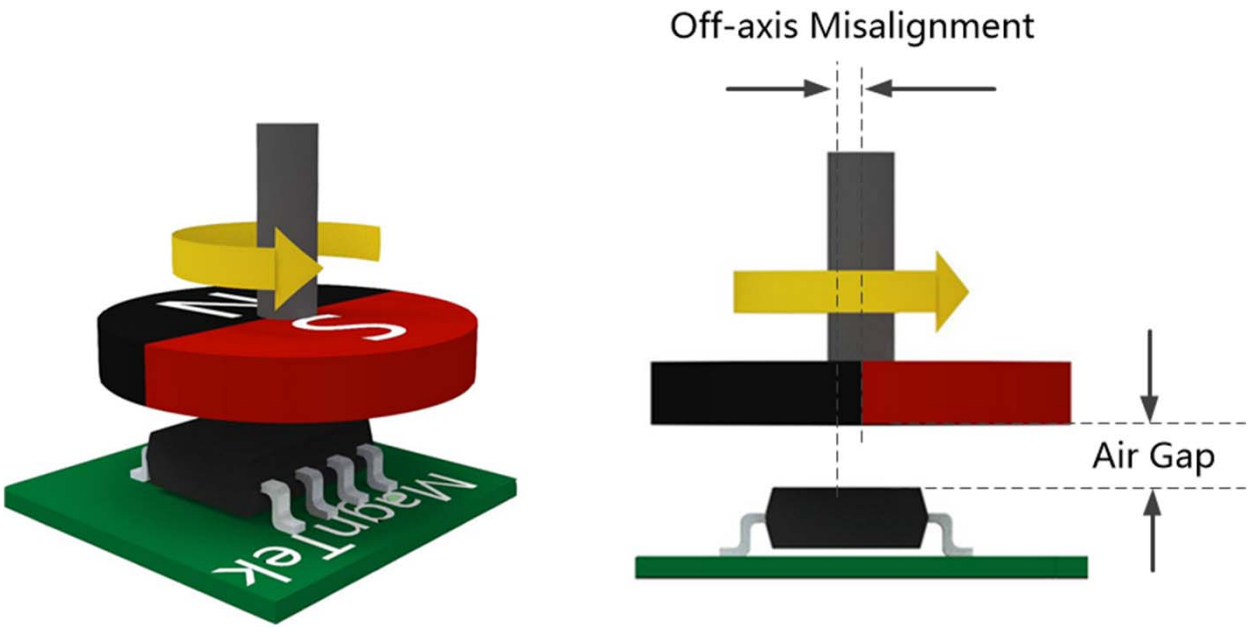


Figure 5: Magnet Arrangement

6. Output Mode

The MT6815 provides ABZ, SDI, UVW, Analog and PWM at output pins, also angle position data could be transferred by I²C or SPI interface.

6.1 I/O Pin Configuration

For SOP-8 package, ABZ (Single-end), SDI (Single-end), I²C and SPI are configured to Pin.5, Pin.6 and Pin.7. Analog and PWM output is configured to Pin.3.

SOP-8 Package I/O Pin Configuration

Pin#	I²C	3-Wire SPI	4-Wire SPI	ABZ Single	SDI Single	UVW	AB Differential	SD Differential
5	SDA	SDAT	MOSI	A	S	U	NA	NA
6			MISO	B	D	V	NA	NA
7	SCL	SCK	SCK	Z	I	W	NA	NA

For QFN-16 package, ABZ (Single-end or AB differential), SDI (Single-end or SD differential), UVW, I²C and SPI are configured to Pin.1, Pin.2 and Pin.3. Analog and PWM output is configured to Pin.11.

QFN-16 Package I/O Pin Configuration

Pin#	I²C	3-Wire SPI	4-Wire SPI	ABZ Single	SDI Single	UVW	AB Differential	SD Differential
1	SDA	SDAT	MOSI	A	S	-	A	S
2	-	-	MISO	B	D	-	B	D
3	SCL	SCK	SCK	Z	I	-	Z	I
13	-	-	-	-	-	W	-	-
14	-	-	-	-	--	V	-B	-D
15	-	-	-	-		U	-A	-S

Output Mode Register (OTP)

Reg. Output_Mode<1:0>	Pin.3 (SOP-8), Pin.11 (QFN-16)
00	ABZ Mode
01	SDI Mode
10	UVW Mode
11	NA

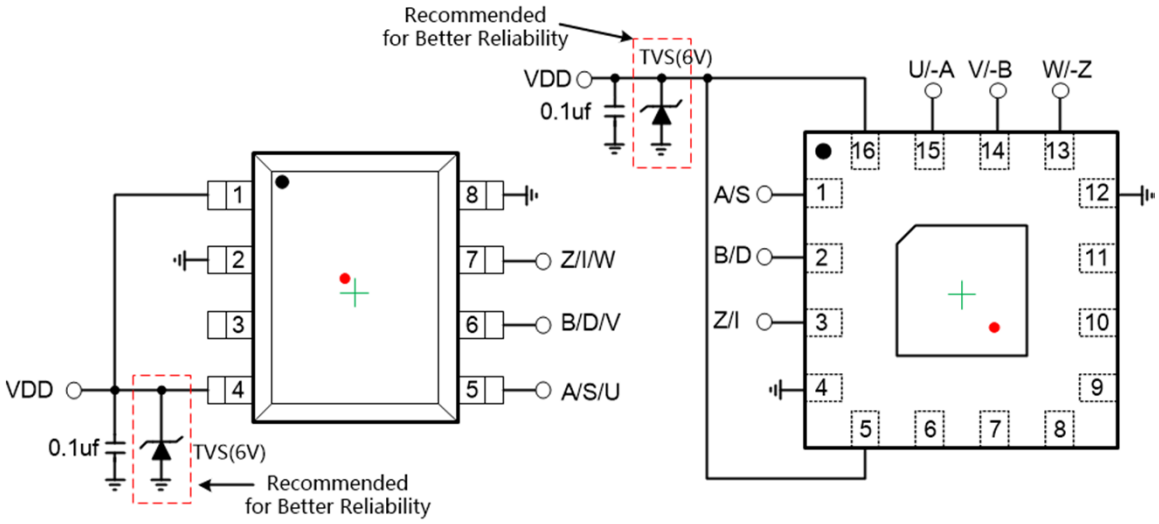


Figure 6: ABZ, SDI, UVW Output Reference Circuit

6.2 Step, Direction and Index Output (SDI Mode)

In this mode, output 'Step' has a pulse width of 1 LSB, output 'Dir' indicates the direction of the magnet rotation; Output Index is the same as output Z in Quadrature A/B mode as shown in Figure 7.

6.3 Quadrature A,B and Zero-Position Output (ABZ Mode)

As shown in Figure 7, when the magnet rotates clock-wise (CW), output A leads output B by 1/4 cycle (or 1 LSB); When the magnet rotates counter-clock-wise (CCW), output B leads output A by 1/4 cycle. Output Z indicates the zero position of the magnet and the pulse width of Z is selectable as 1, 2 or 4 LSBs. It is guaranteed that one Z pulse is generated for every rotation. The zero position is user programmable。

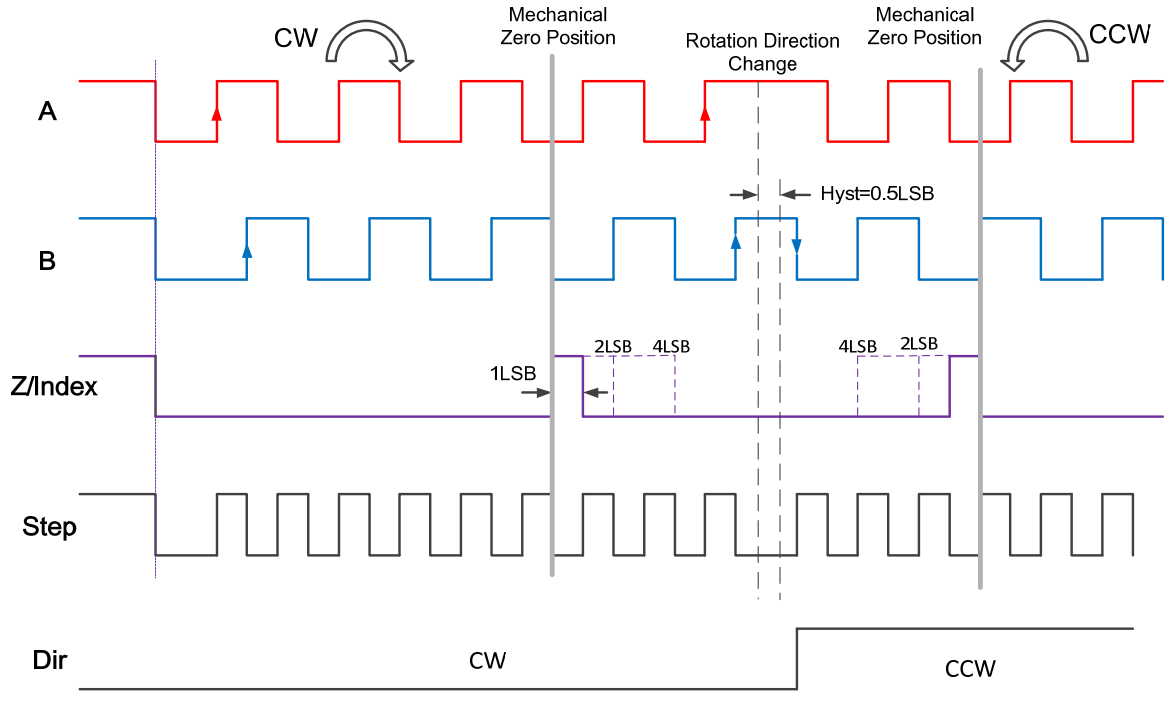


Figure 7: Typical Output Waveform for ABZ and SDI Mode

The mechanical zero position could be programmed, it is a 12 bits data for 0~360°.

Z/Index Pulse Width Register (OTP)

Reg. Z_Pulse_Width<1:0>	Width (LSBs)
00	1
01	2
10	3
11	4

Zero Position Register (MTP)

Register	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Zero_LSB	Zero<7:0>							
Zero_MSB	NA	NA	NA	NA	Zero<11:8>			

ABZ Resolution Register (OTP)

Reg. ABZ_Res<2:0>	Reg.ABZ_INT	Steps per Cycle	Pulses per Cycle
000	0	1024	256
001	0	512	128
010	0	256	64
011	0	128	32
100	0	2048	512
101	0	4096	1024
110/111	0	8192	2048
000	1	2000	500
001	1	800	200
010	1	400	100
011	1	192	48
100	1	4000	1000
101	1	8000	2000
110/111	1	10000	2500

6.4 UVW Output Mode

The MT6815 provides U, V and W pulses which are 120° (electrical) out of phase as shown in Figure 8. The cycles of UVW per rotation can be programmed.

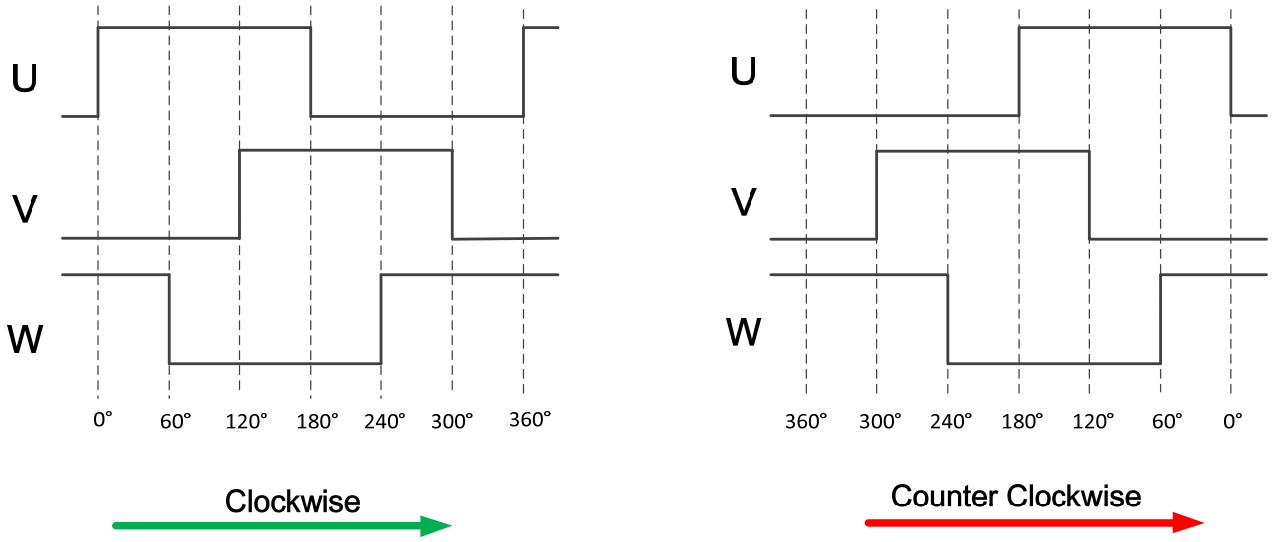


Figure 8: Typical Output Waveform for UVW Mode

UVW Pole Pairs Register (OTP)

Reg. UVW_Paris<3:0>	UVW Pole Pairs
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	2
1001	4
1010	6
1011	8
1100	10
1101	12
1110	14
1111	16

6.5 Analog Output Mode

The MT6815 provides a rail-to-rail linear analog output by a build-in 12 bit DAC as shown in Figure 9. It's a linear transfer function of absolute angle and output voltage. To enable analog output, register 'Enable Analog' should be programmed to high.

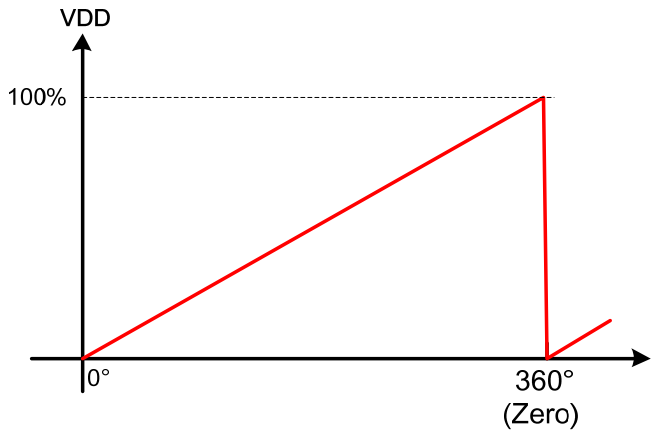


Figure 9: Default Analog Output

Analog or PWM Output Control Register (OTP)

Reg. Enable Analog	Pin.3 (SOP-8), Pin.11 (QFN-16)
0	PWM
1	Analog

The reference circuit for analog output is shown in Figure 10, an external decoupling capacitor C1 (typical 10nf, maximum 100nf) is suggested for better performance.

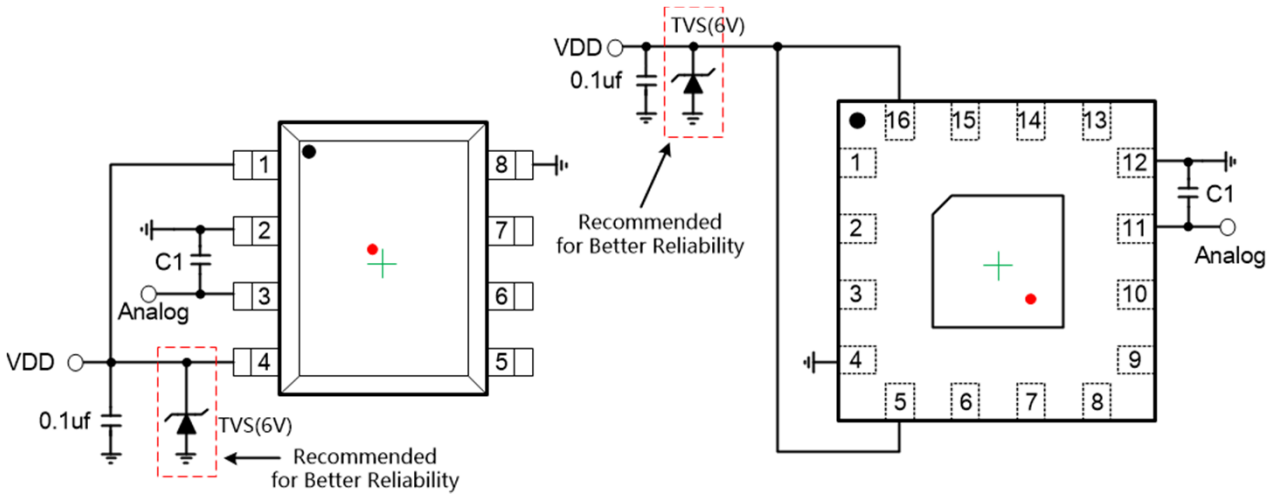


Figure 10: Analog Output Mode Reference Circuit

The angle and voltage value of start-point, Clamp_Low and Clamp_High could be user programmed, also the Zero Point could be user programmed as shown in Figure 11.

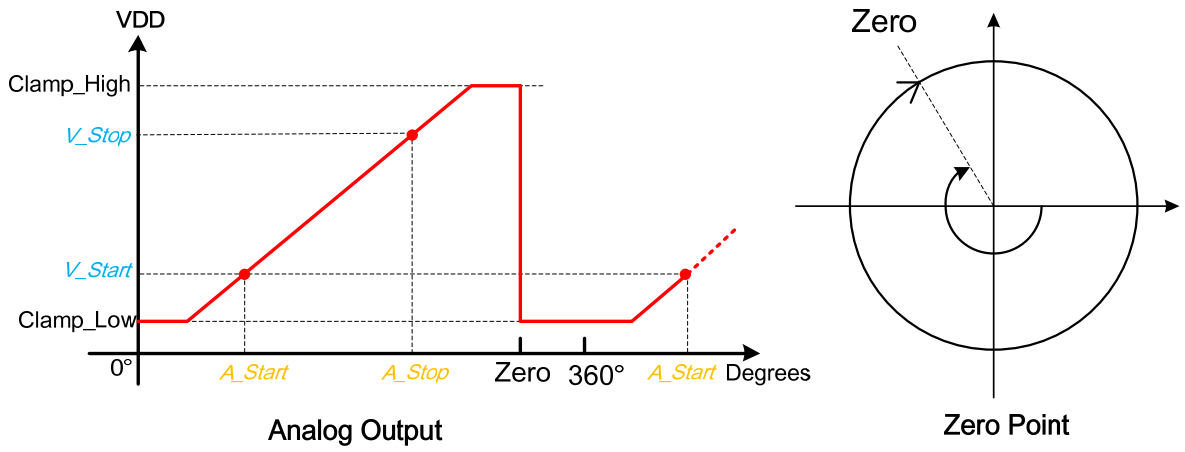


Figure 11: Analog Output Transfer Function and Zero Point

Analog Output Registers (MTP)

Register	Bit<7:4>	Bit<3:0>
Clamp_Low_LSB	Clamp_Low<7:0>	
Clamp_High_LSB	Clamp_High<7:0>	
Clamp_Msb	Clamp_High<11:8>	Clamp_Low<11:8>
Zero_Lsb	Zero<7:0>	
Zero_MSB	NA	Zero<11:8>
Start_Angle_Lsb	A_Start<7:0>	
Start_Angle_Msb	NA	A_Start<11:8>
Stop_Angle_Lsb	A_Stop<7:0>	
Stop_Angle_Msb	NA	A_Stop<11:8>
Start_Voltage_Lsb	V_Start<7:0>	
Stop_Voltage_Lsb	V_Stop<7:0>	
Voltage_Msb	V_Stop<11:8>	V_Start<11:8>

6.6 Pulse Width Modulation (PWM) Output Mode

The MT6815 provides a digital Pulse Width Modulation (PWM) output, whose duty cycle is proportional to the measured angle as shown in Figure 13. PWM is a default output of Pin.3 (SOP-8) and Pin.11 (QFN-16).

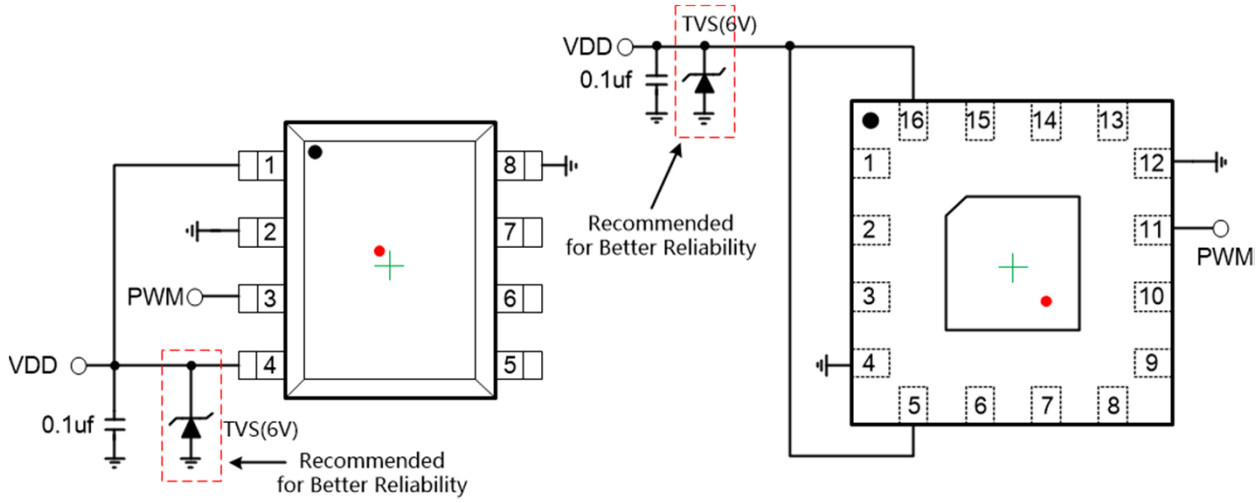


Figure 12: PWM Output Reference Circuit

PWM Resolution Register (OTP)

Reg. PWM_Res<1:0>	Resolution	PWM Frequency
00	10 bit	2.5 KHz
01	9 bit	5 KHz
10	11 bit	1.25 KHz
11	12 bit	625 Hz

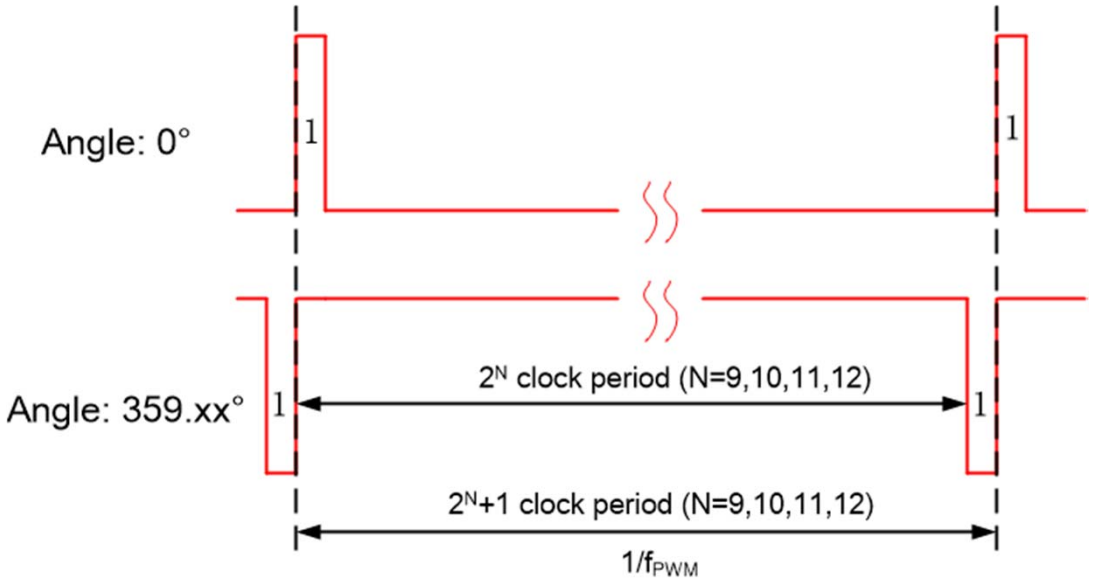


Figure 13: PWM Output

6.7 I²C Interface

The MT6815 provides a slave I²C interface for host MCU to read back digital absolute angle information from its internal registers. The reference circuit for I²C interface is shown in Figure 14, whether the need for pull-up resistor on SCL is determined by MCU, for MT6815 SCL is a digital input.

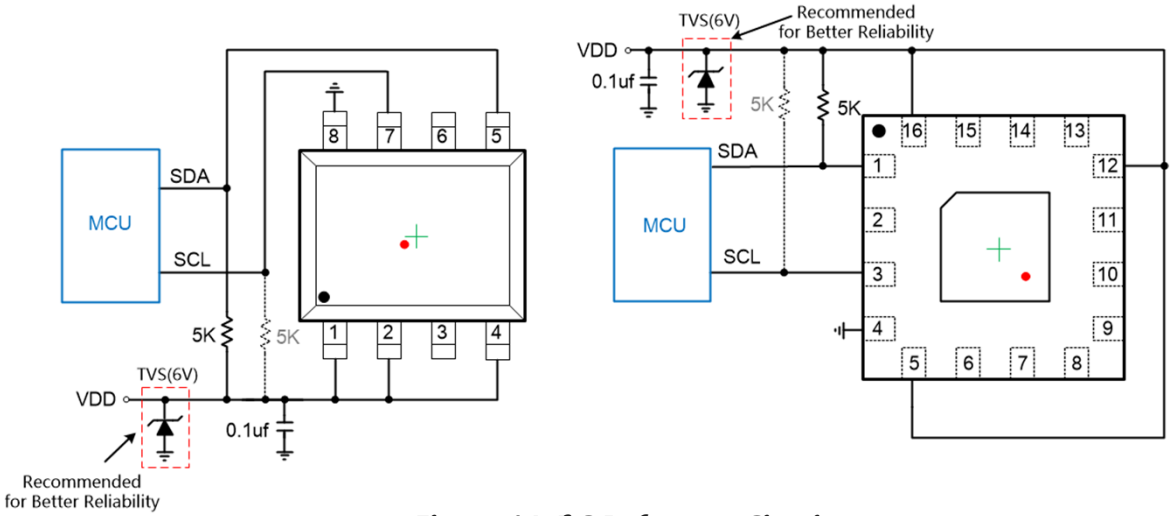


Figure 14: I²C Reference Circuit

6.7.1 I²C Timing Diagram

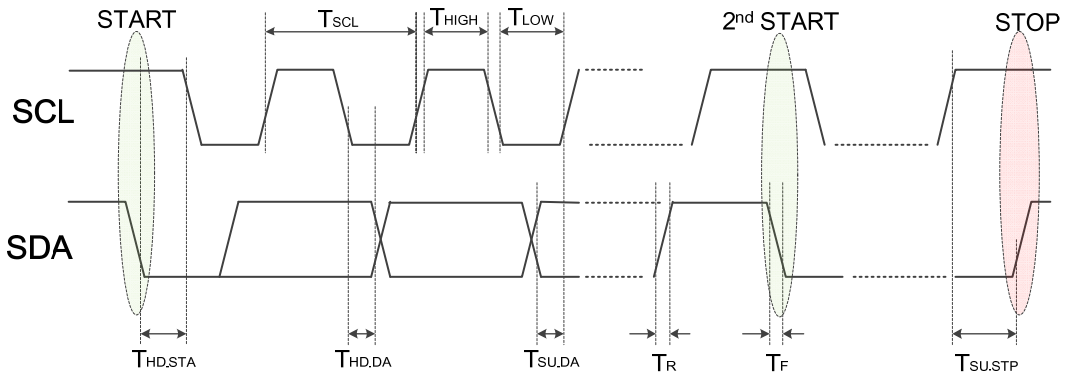


Figure 15: I²C Timing Diagram

I²C Timing Parameter

Parameter	Notes	Min.	Max.	Unit
T_{SCL}	SCL Clock Period	1	-	μs
$T_{HD.STA}$	Hold Time of 'START'	250	-	ns
T_{LOW}	Low Phase of SCL	250	-	ns
T_{HIGH}	High Phase of SCL	250	-	ns
$T_{SU.DA}$	Setup Time of SDA	100	-	ns
$T_{HD.DA}$	Hold Time of SDA	50	-	ns
T_R	Rising Time of SDA/SCL	-	150	ns
T_F	Falling Time of SDA/SCL	-	150	ns
$T_{SU.STP}$	Setup Time of 'Stop'	250	-	ns

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6.7.2 I²C Read Angle Registers

The slave ID of MT6815 is b' 0000110 in 7 bit binary form. The 14 bits angle data is stored in internal register 0x03 and 0x04. Please follow the I²C timing of Figure 16 to read the angle data from 0x03 and 0x04 registers.

Note: Please read Register 0x03 first and then read 0x04

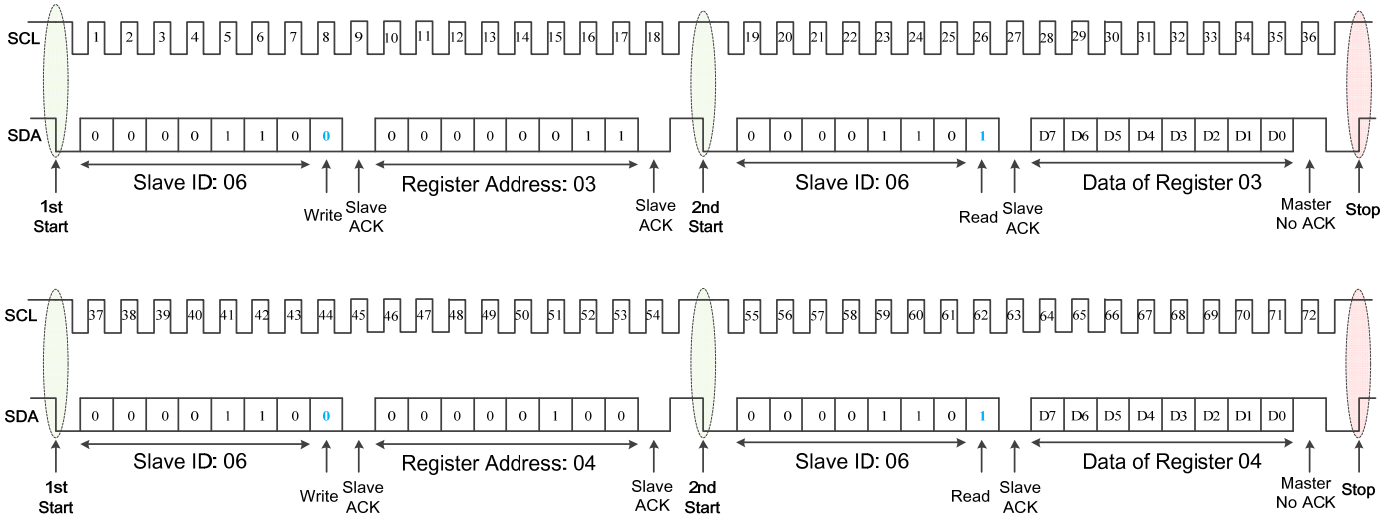


Figure 16: I²C Single Byte Read

Angle Data Register

Reg. Addresss	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Angle<13:6>							
0x04	Angle<5:0>						No_Mag_Warning	NA

0~360° absolute angle θ could be calculated by the below formula:

$$\theta = \frac{\sum_{i=0}^{13} Angle<i> \cdot 2^i}{16384} \cdot 360°$$

Bit 0x04[1] is a diagnosed bit for No Magnet Detected. When the MT6815 could not detect enough magnetic field for proper operation, this bit is set to high.

6.7.3 I²C Burst Read

The MT6815 provides an I²C burst read mode as shown in Figure 17 for faster data rate than single byte read mode.

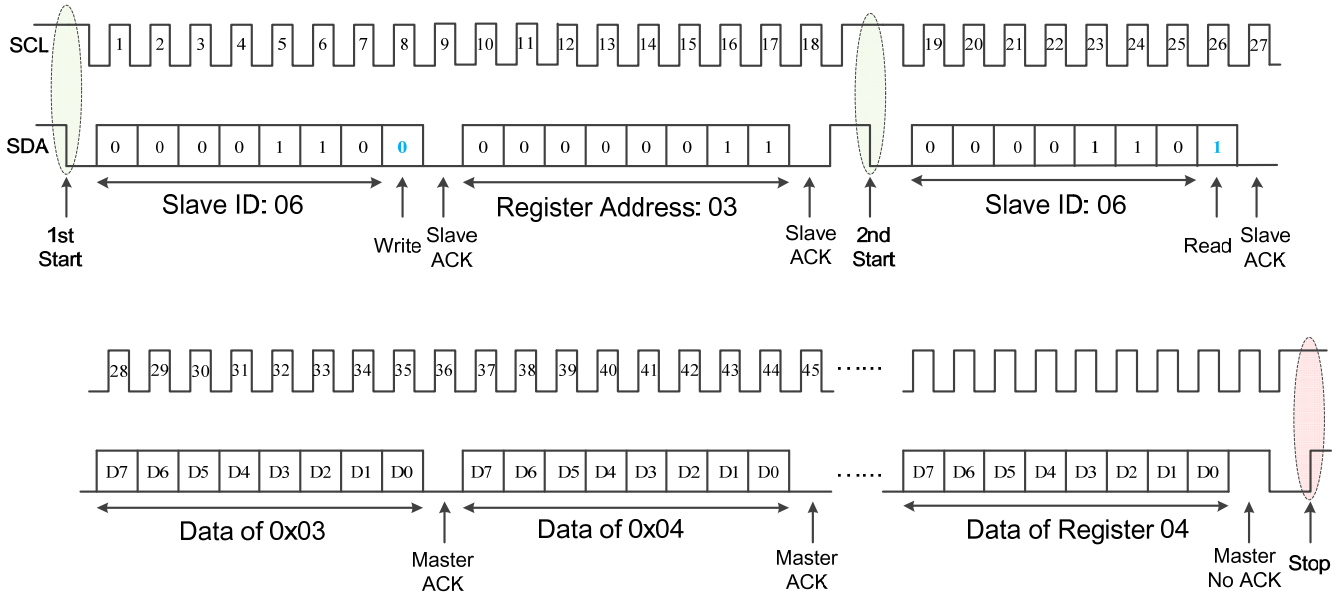


Figure 17: I²C Burst Read

6.7.4 I²C Write

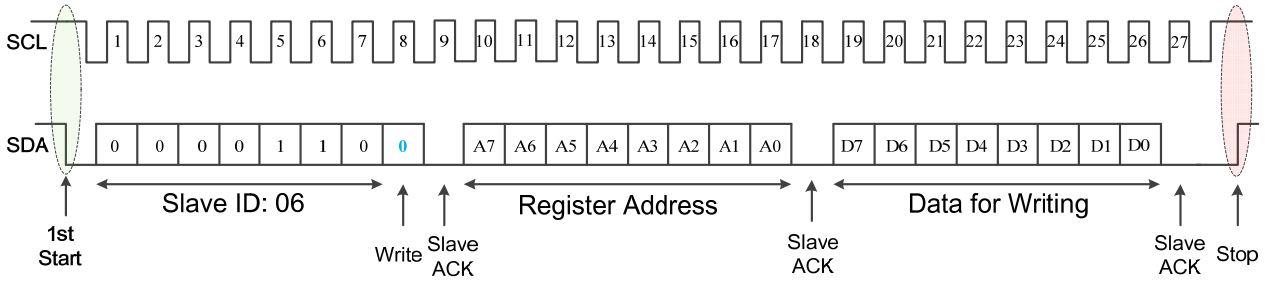


Figure 18: I²C Write

6.8 SPI Interface

The MT6815 also provides a 4-Wire or 3-Wire SPI (Register 3W_SPI should be programmed to 'High' to enable 3-Wire SPI Mode) interface for host MCU to read back digital absolute angle information from its internal registers. The reference circuit for SPI interface is shown in Figure 19 and Figure 20.

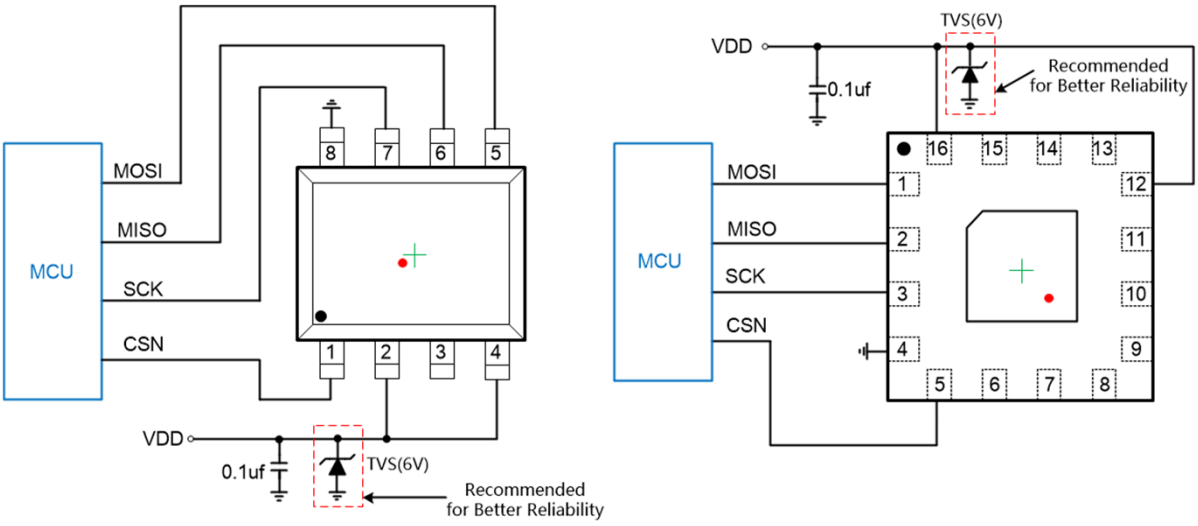


Figure 19: 4-Wire SPI Reference Circuit

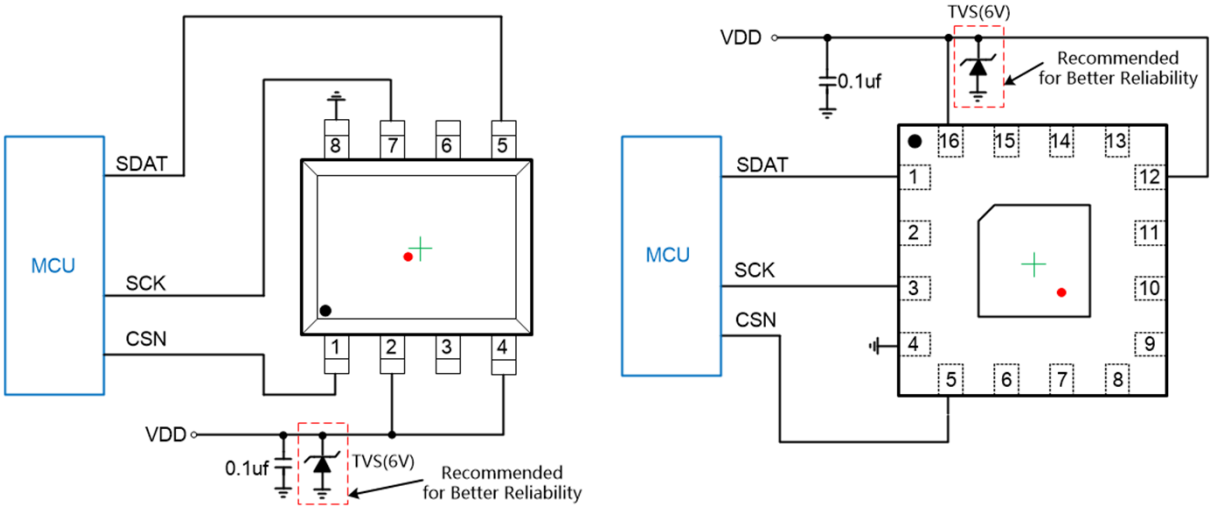


Figure 20: 3-Wire SPI Reference Circuit

3-Wire SPI Enable Register (OTP)

Reg. 3W_SPI	SPI Interface
0	4 Wire
1	3 Wire

6.8.1 SPI Timing Diagram

The MT6815 SPI uses mode=3 (CPOL=1, CPHA=1) to exchange data. As shown in Figure 21, a data transfer starts with the falling edge of CSN. The MT6815 samples data on the rising edge of SCK, and the data transfer finally stops with the rising edge of CSN.

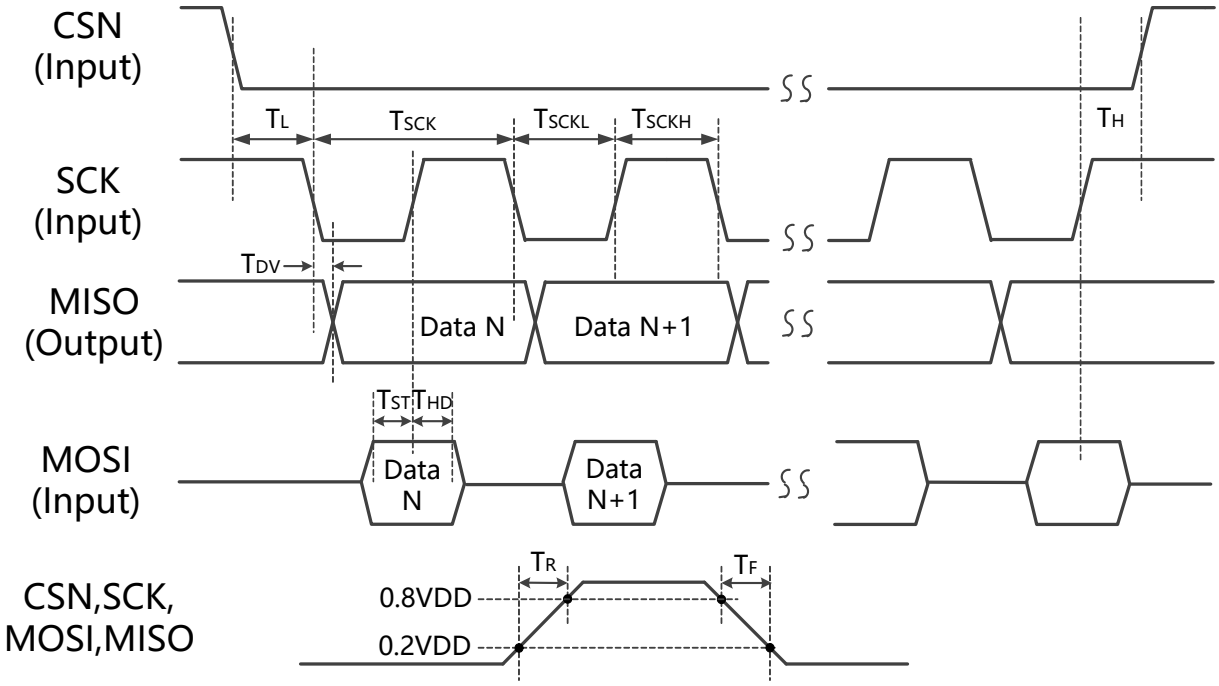


Figure 21: SPI Timing Diagram

SPI Timing Parameter

Symbol	Notes	Min.	Max.	Unit
T_L	Time between CSN falling edge and SCK falling edge	250	-	ns
T_{SCK}	Clock period	400(1)	-	ns
T_{SCKL}	Low period of clock	200(2)	-	ns
T_{SCKH}	High period of clock	200(2)	-	ns
T_H	Time between SCK last rising edge and CSN rising edge	0.5•TSCK	-	ns
T_R	Rise Time of Digital Signal (with 20pf Loading Condition)	-	30	ns
T_F	Fall Time of Digital Signal (with 20pf Loading Condition)	-	30	ns
T_{DV}	Data valid time of MISO (with 20pf Loading Condition)	-	30	ns
T_{ST}	Setup time of MOSI data	40	-	ns
T_{HD}	Hold time of MOSI data	40	-	ns

Notes:

(1) The MT6815 has a burst mode. When this mode is enabled, the chip internal clock frequency is doubled and the minimum T_{SCK} also could be reduced to 200ns

(2) The MT6815 has a burst mode. When this mode is enabled, the chip internal clock frequency is doubled and the minimum T_{SCKL} and T_{SCKH} also could be reduced to 100ns

6.8.2 4-Wire SPI

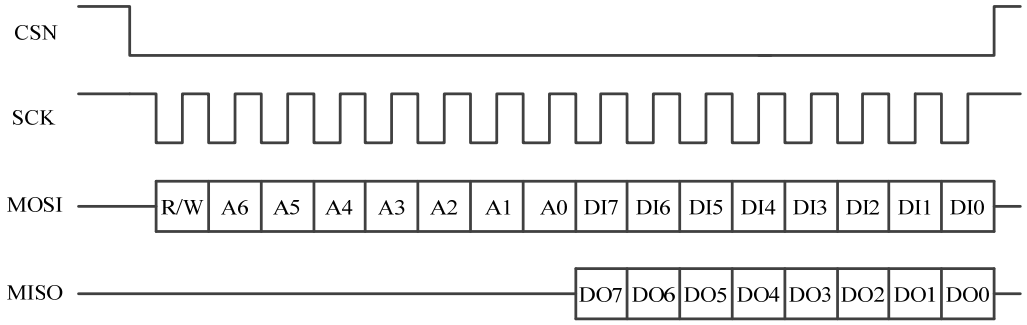


Figure 22: 4-Wire SPI Timing

An SPI data transfer starts with the falling edge of CSN and stops at the rising edge of CSN. SCK is the Serial Port Clock and it is controlled by the SPI master, it is high when there is no SPI transmission. MOSI (master output slave input) and MISO (master input slave output) is the Serial Port Data Input and Output, it is driven at the falling edge of SCK and should be captured at the rising edge of SCK.

Bit 0: R/W bit, when it is 0, the data DI7~DI0 is written into the device, when it is 1, the data DO7~DO0 from the device is read.
Bit 1-7: Address A6~A0. This is the address field of the indexed register.
Bit 8-15: Data DI7~DI0 (write mode). This is the data that will be written into the device (MSB first).
Bit 8-15: Data DO7~DO0 (read mode). This is the data that will be read from the device (MSB first).

6.8.3 3-Wire SPI

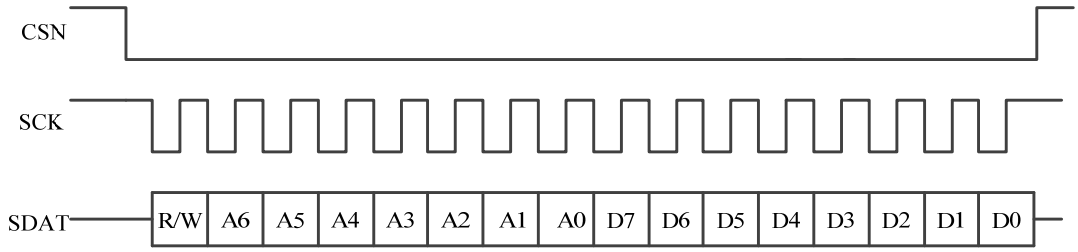


Figure 23: 3-Wire SPI Timing

An SPI data transfer starts with the falling edge of CSN and stops at the rising edge of CSN. SCK is the Serial Port Clock and it is controlled by the SPI master, it is high when there is no SPI transmission. SDAT is the Serial Port Data Input and Output, and it is driven at the falling edge of SCK and should be captured at the rising edge of SCK.

Bit 0: RW bit. When 0, the data D7~D0 is written into the device. When 1, the data D7~D0 from the device is read.
Bit 1-7: address A6~A0. This is the address field of the indexed register.
Bit 8-15: data D7~D0 (write mode). This is the data that will be written into the device (MSB first).
Bit 8-15: data D7~D0 (read mode). This is the data that will be read from the device (MSB first).

6.8.4 SPI Read Angle Register (e.g. 4-Wire SPI)

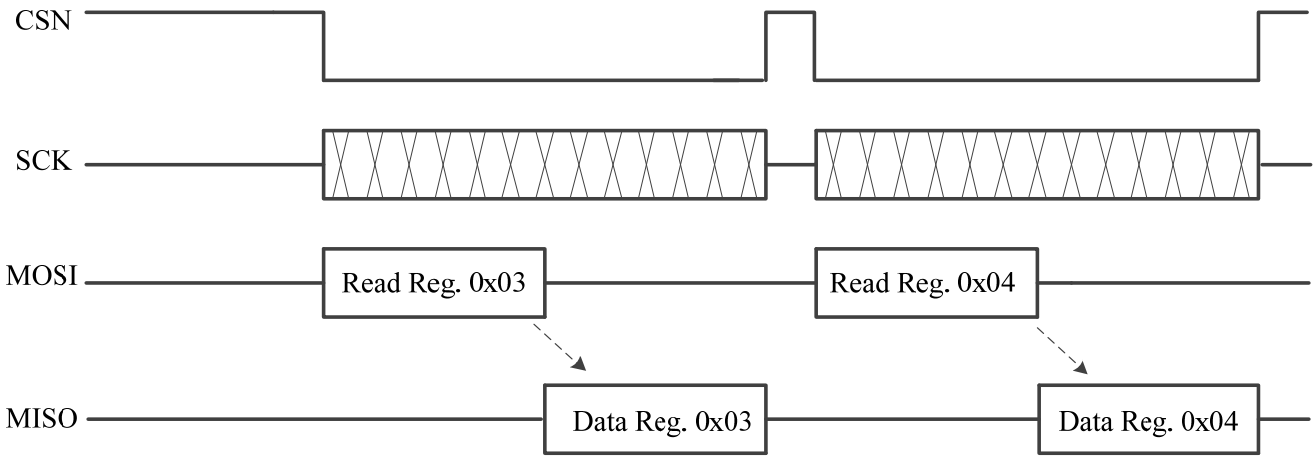


Figure 24: 4-Wire SPI Single Byte Read Angle Register

Angle Data Register

Reg. Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Angle<13:6>							
0x04	Angle<5:0>						No_Mag_Warning	NA

0~360° absolute angle θ could be calculated by the below formula:

$$\theta = \frac{\sum_{i=0}^{13} Angle<i> \cdot 2^i}{16384} \bullet 360°$$

Bit 0x04[1] is a diagnosed bit for No Magnet Detected. When the MT6815 could not detect enough magnetic field for proper operation, this bit is set to high.

For SPI reading angle data, MangTek provides a special data processing MCU code for better accuracy, please contact us for it.

The MT6815 provides an SPI burst read mode for faster data rate than single byte read mode as shown in Figure 25.

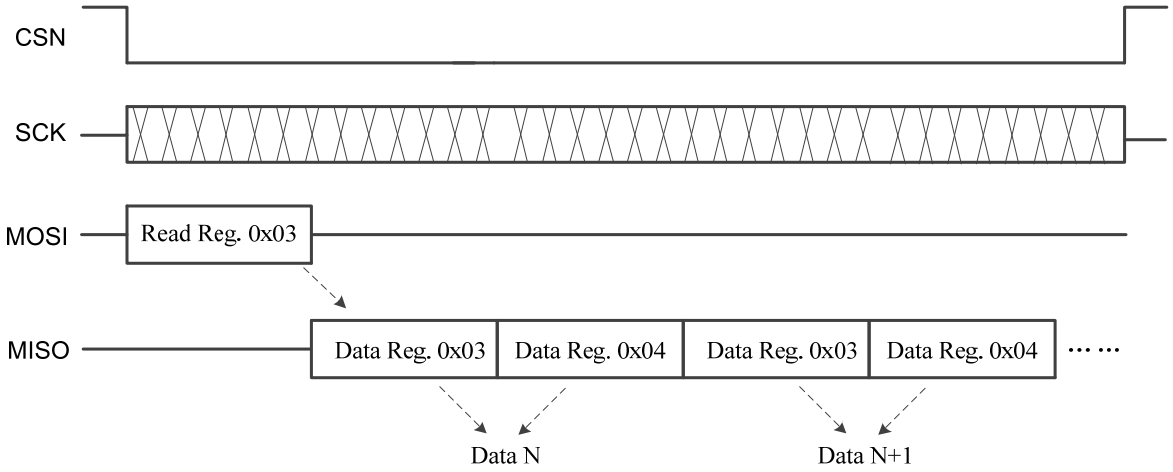


Figure 25: 4-Wire SPI Burst Read Angle Registers

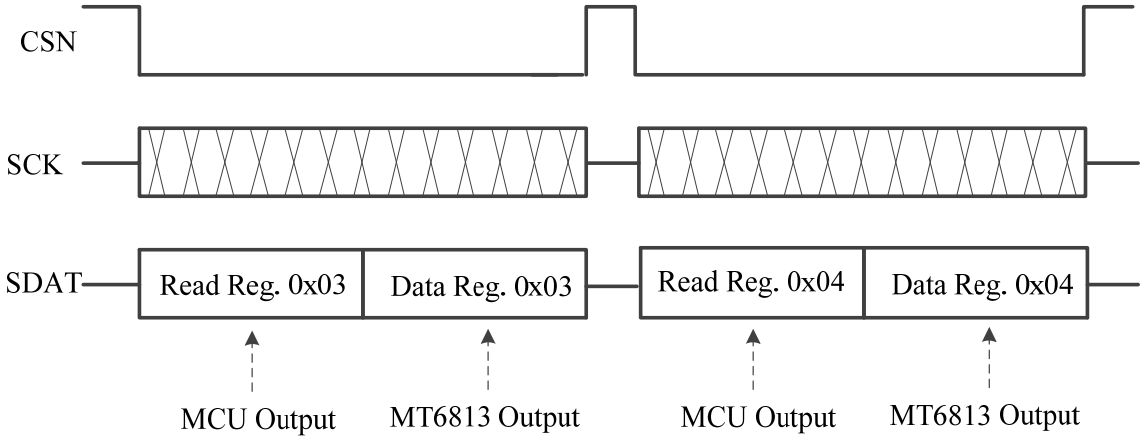


Figure 26: 3-Wire SPI Single Byte Read Angle Registers

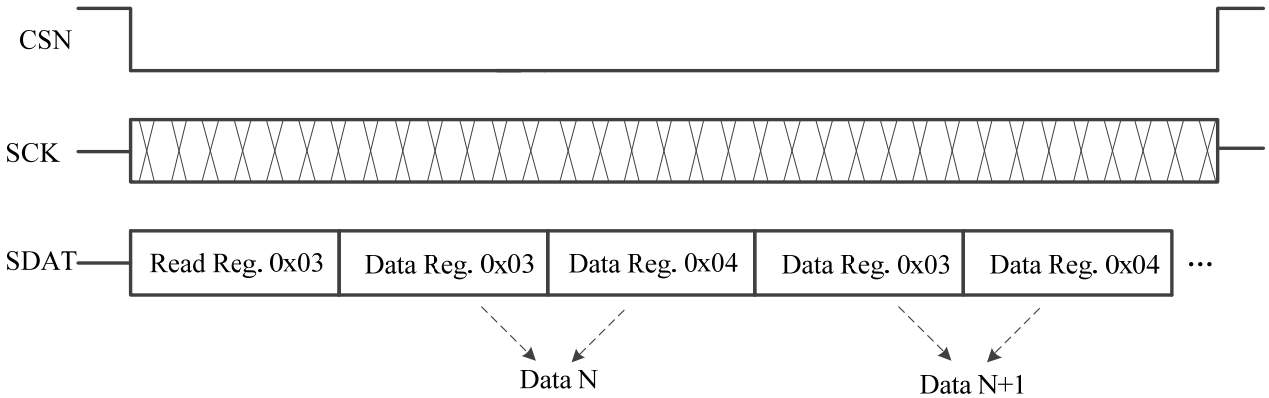
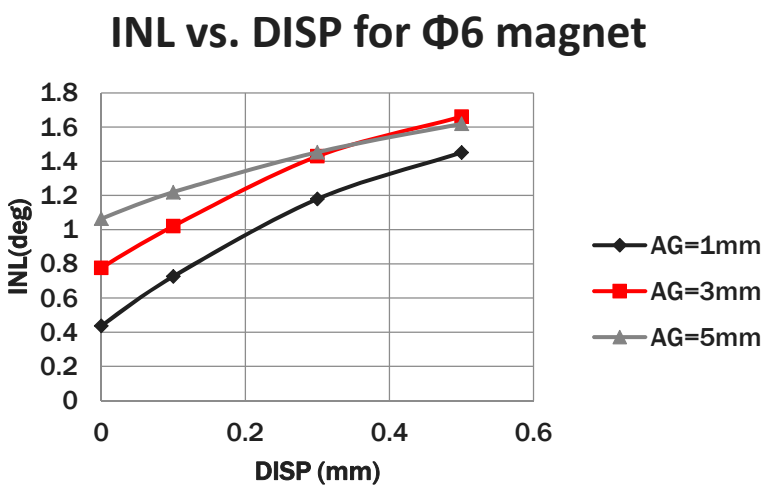
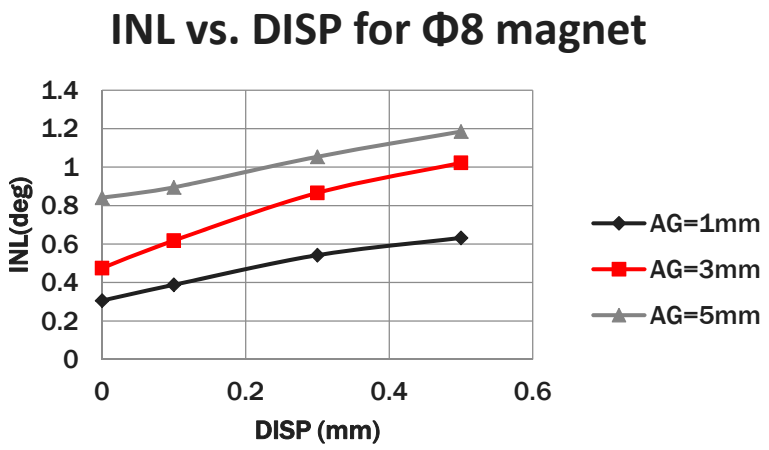


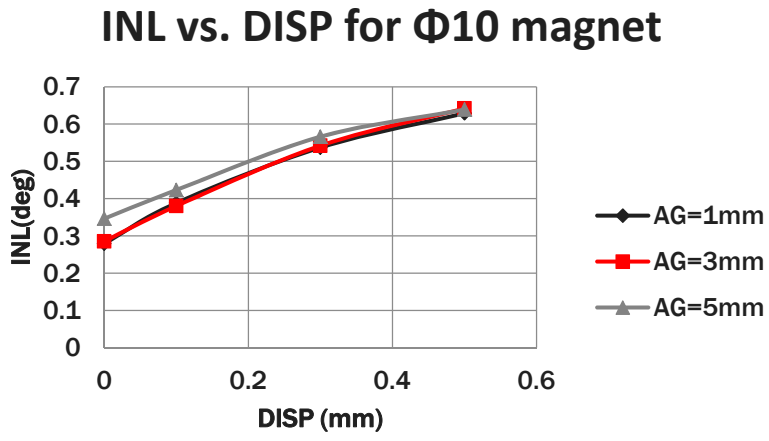
Figure 27: 3-Wire SPI Burst Read Angle Registers

7. Magnet Placement

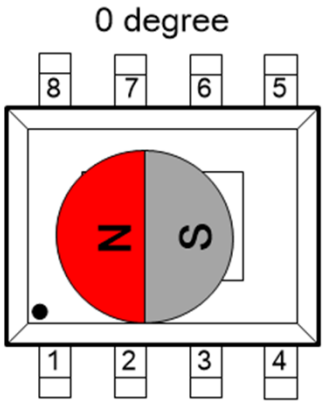
It is required that the magnet' s center axis be aligned with the sensing element center of MT6815 with the air-gap as small as possible. Any misalignment introduces additional angle error and big air-gap also weakens the magnet field which could be sensed by the device. Magnets with larger diameter are more tolerant to DISP (off-axis misalignment) and big AG (air-gap between Magnet and device).

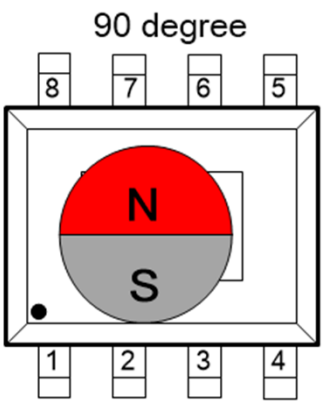


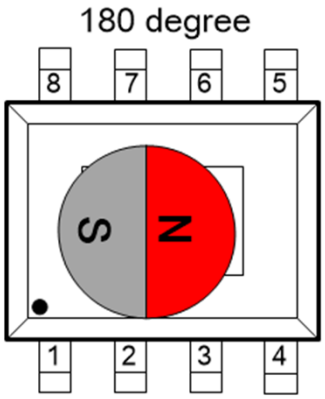


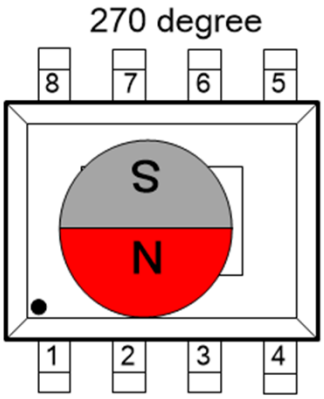


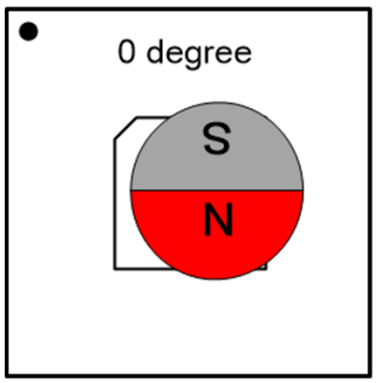
8. Mechanical Angle Direction

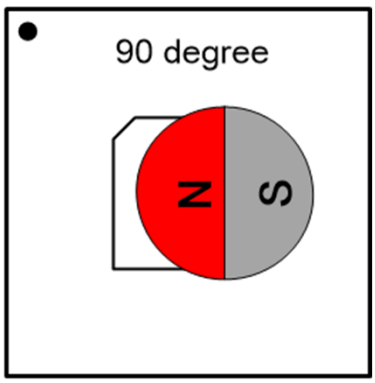


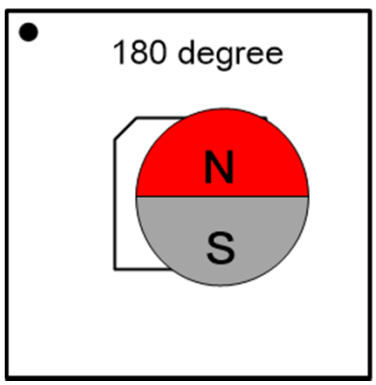


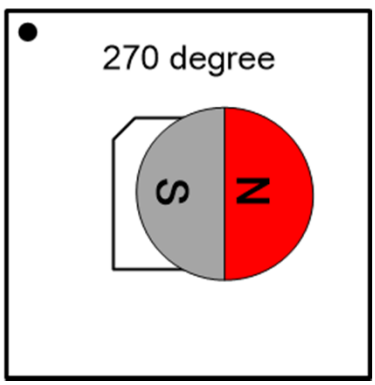






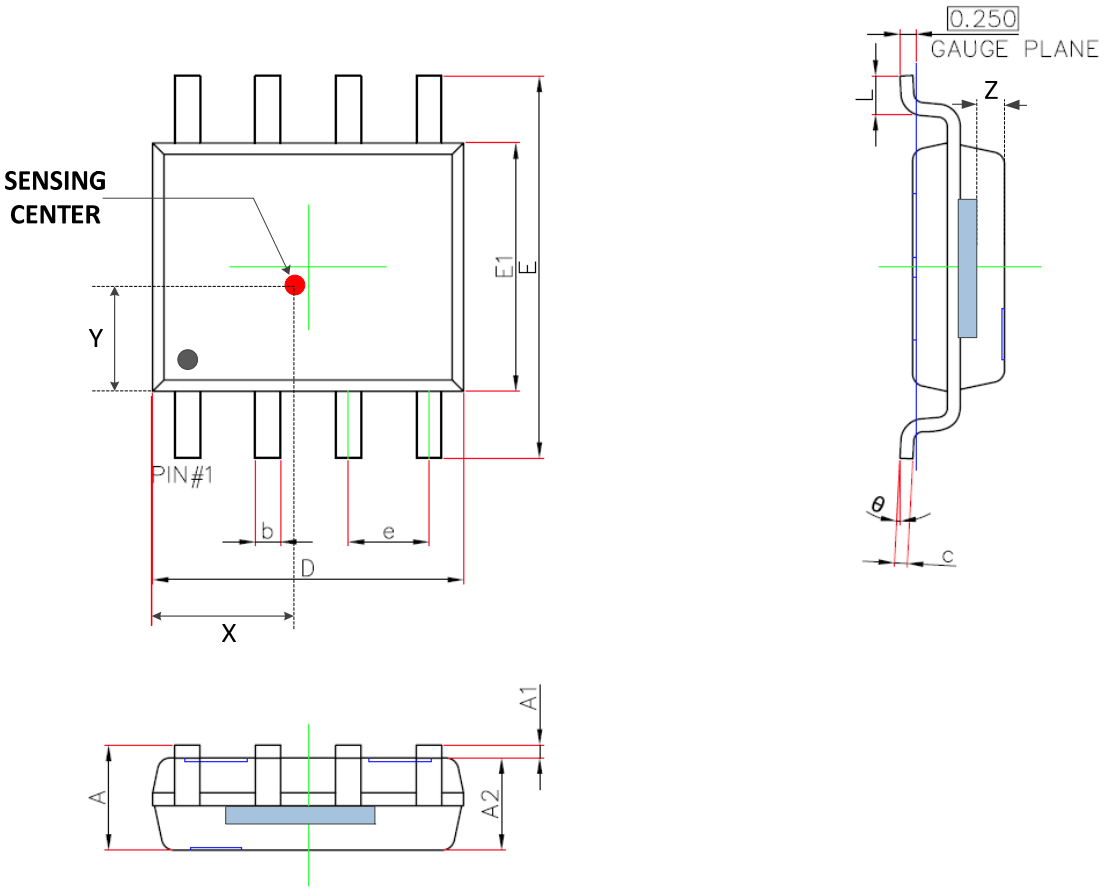






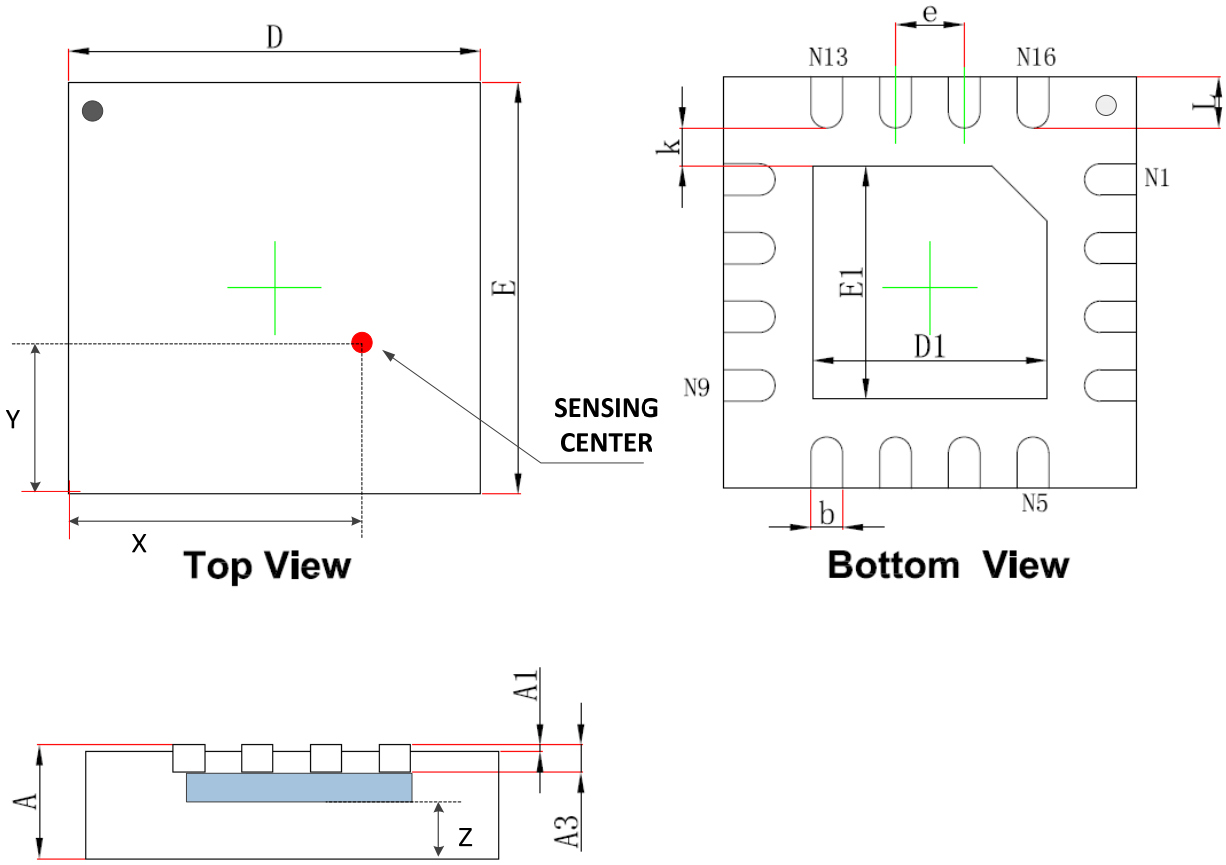
9. Package Information

9.1 SOP-8 Package



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°
X	1.94	2.24	0.076	0.088
Y	1.71	2.01	0.067	0.079
Z	0.42	0.62	0.016	0.024

9.2 QFN-16 Package



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0.275REF		0.011REF	
b	0.180	0.300	0.007	0.012
e	0.500REF		0.020REF	
L	0.300	0.500	0.012	0.020
X	1.690	1.990	0.066	0.078
Y	1.110	1.410	0.043	0.055
Z	0.420	0.620	0.016	0.024

深圳市满度科技有限公司
Tel:150-1290-5940
Web:www.manduic.com
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