NAND Flash Memory

MT29F4G08ABBFAH4

Features

- Open NAND Flash Interface (ONFI) 1.0-compliant[1]
- Single-level cell (SLC) technology
- Organization
  - Page size ×8: 4352 bytes (4096 + 256 bytes)
  - Block size: 64 pages
  - Number of planes: 1
  - Device size: 4Gb
- Asynchronous I/O performance
  - ^{t}RC/^{t}WC: 30ns (1.8V)
- Array performance
  - Read page: 115µs (MAX) with on-die ECC enabled
  - Read page: 25µs (MAX) with on-die ECC disabled
  - Program page: 200µs (TYP) with on-die ECC disabled
  - Program page: 240µs (TYP) with on-die ECC enabled
  - Erase block: 2ms (TYP)
- Command set: ONFI NAND Flash protocol
- Advanced command set
  - Program page cache mode
  - Read page cache mode
  - Permanent block locking (blocks 47:0)
  - One-time programmable (OTP) mode
  - Block lock
  - Programmable drive strength
  - Read unique ID
  - Internal data move
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/Fail condition
  - Write-protect status
- Ready/Busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: Write protect entire device
- ECC: 8-bit internal ECC is disabled at default[2] (it can be toggled using the SET FEATURE command)
- Blocks 7–0 are valid when shipped from factory with ECC; for minimum required ECC, see Error Management.
- RESET (FFh) required as first command after power-on
- Alternate method of automatic device initialization after power-up (contact factory)
- Internal data move operations supported within the plane from which data is read
- Quality and reliability
  - Endurance: 100,000 PROGRAM/ERASE cycles
  - Data retention: JESD47G-compliant; see qualification report
  - Additional: Uncycled data retention: 10 years 24/7 @ 85°C

Options	Marking
• Operating voltage range	
– V_{CC}: 1.7–1.95V	A
• Operating temperature range	
– Industrial (IT): –40°C to +85°C	IT
• Package	
– 63-ball VFBGA (9mm × 11mm × 1.0mm)	H4

Notes:
1. The ONFI 1.0 specification is available at www.onfi.org.
2. Refer to the Part Numbering Information to check the status of the ECC.

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Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Marketing Part Number Chart

MT 29F 4G 08 A B A F A H4 - AAT ES :F

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Product Family
29F = NAND Flash memory

Density
1G = 1Gb
2G = 2Gb
4G = 4Gb
8G = 8Gb
16G = 16Gb

Device Width
08 = 8-bit
16 = 16-bit

Level
A = SLC

Classification

Mark	Die	nCE	RnB	I/O Channel
B	1	1	1	1
D	2	1	1	1
J	4	2	2	1

Operating Voltage Range
A = 3.3V (2.7–3.6V)
B = 1.8V (1.7–1.95V)
C = V_{CC}: 3.3V (2.7–3.6V); V_{CCQ}: 1.8V (1.7–1.95V)

Generation Feature Set
D = Feature set D
E = Feature set E
F = Feature set F
G = Feature set G

Design Revision (shrink)
D = Design Revision D
E = Design Revision E
F = Design Revision F
G = Design Revision G

Production Status
Blank = Production
ES = Engineering sample
MS = Mechanical sample
QS = Qualification sample

Special Options
E = Internal ECC enabled by default (Parallel)
Blank = Internal ECC disabled by default (Parallel)

Operating Temperature Range
Blank = Commercial (0°C to +70°C)
IT = Industrial (–40°C to +85°C)
AIT = Automotive Industrial (–40°C to +85°C)
AAT = Automotive (–40°C to +105°C)

Speed Grade
12 = 166 MT/s (synchronous mode)
Blank = Asynchronous mode

Package Code
SF = 16-pin SO (10.3mm x 10.3mm x 2.65mm)
WB = 8-pin U-PDFN (8mm x 6mm x 0.65mm)
W9 = 8-pin W-PDFN (8mm x 6mm)
12 = 24-ball TBGA (6mm x 8mm x 1.2mm)
WP = 48-pin TSOP Type 1
HC = 63-ball VFBGA (10.5mm x 13mm x 1.0mm)
H4 = 63-ball VFBGA (9mm x 11mm x1.0mm)

Interface
A = Asynchronous only
B = Sync/Async

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General Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection and monitor device status (R/B#).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. An NAND Flash die is the minimum unit that can independently execute commands and report status. An NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). There is at least one NAND Flash die per chip enable signal. For further details, see Device and Array Organization.

Signal Descriptions

Table 1: Signal Definitions

Signal[1]	Type	Description[2]
ALE	Input	**Address latch enable:** Loads an address from I/O[7:0] into the address register.
CE#	Input	**Chip enable:** Enables or disables one or more die (LUNs) in a target.
CLE	Input	**Command latch enable:** Loads a command from I/O[7:0] into the command register.
LOCK	Input	When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. To disable the BLOCK LOCK, connect LOCK to V_{SS} during power-up, or leave it disconnected (internal pull-down).
RE#	Input	**Read enable:** Transfers serial data from the NAND Flash to the host system.
WE#	Input	**Write enable:** Transfers commands, addresses, and serial data from the host system to the NAND Flash.
WP#	Input	**Write protect:** Enables or disables array PROGRAM and ERASE operations.
I/O[7:0] (x8) I/O[15:0] (x16)	I/O	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and command information.
R/B#	Output	**Ready/busy:** An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.
V_{CC}	Supply	**V_{CC}:** Core power supply
V_{SS}	Supply	**V_{SS}:** Core ground connection
NC	–	**No connect:** NCs are not internally connected. They can be driven or left unconnected.
DNU	–	**Do not use:** DNUs must be left unconnected.

Notes:
1. See Device and Array Organization for detailed signal connections.
2. See Asynchronous Interface Bus Operation for detailed asynchronous interface signal descriptions.

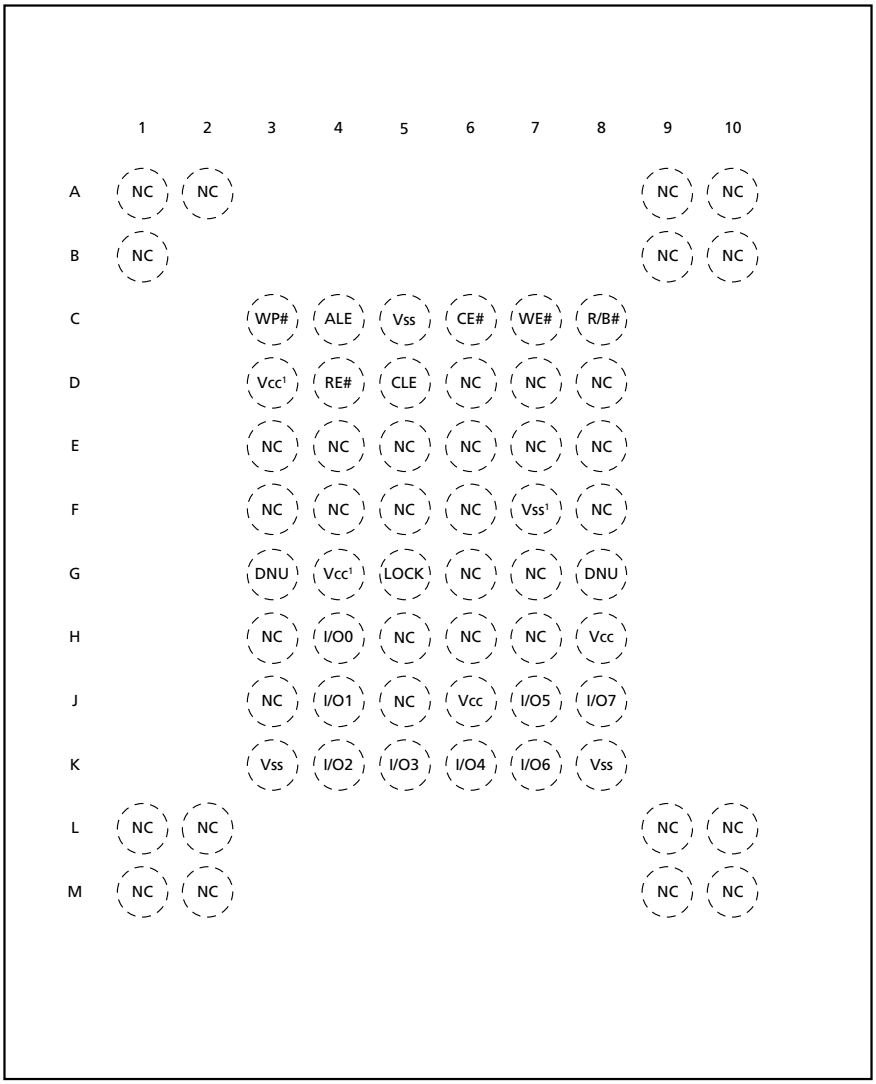
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Signal Assignments

Figure 2: 63-Ball VFBGA, x8 (Balls Down, Top View)



Note: 1. These pins might not be bonded in the package; however, Micron recommends that the customer connect these pins to the designated external sources for ONFI compatibility.

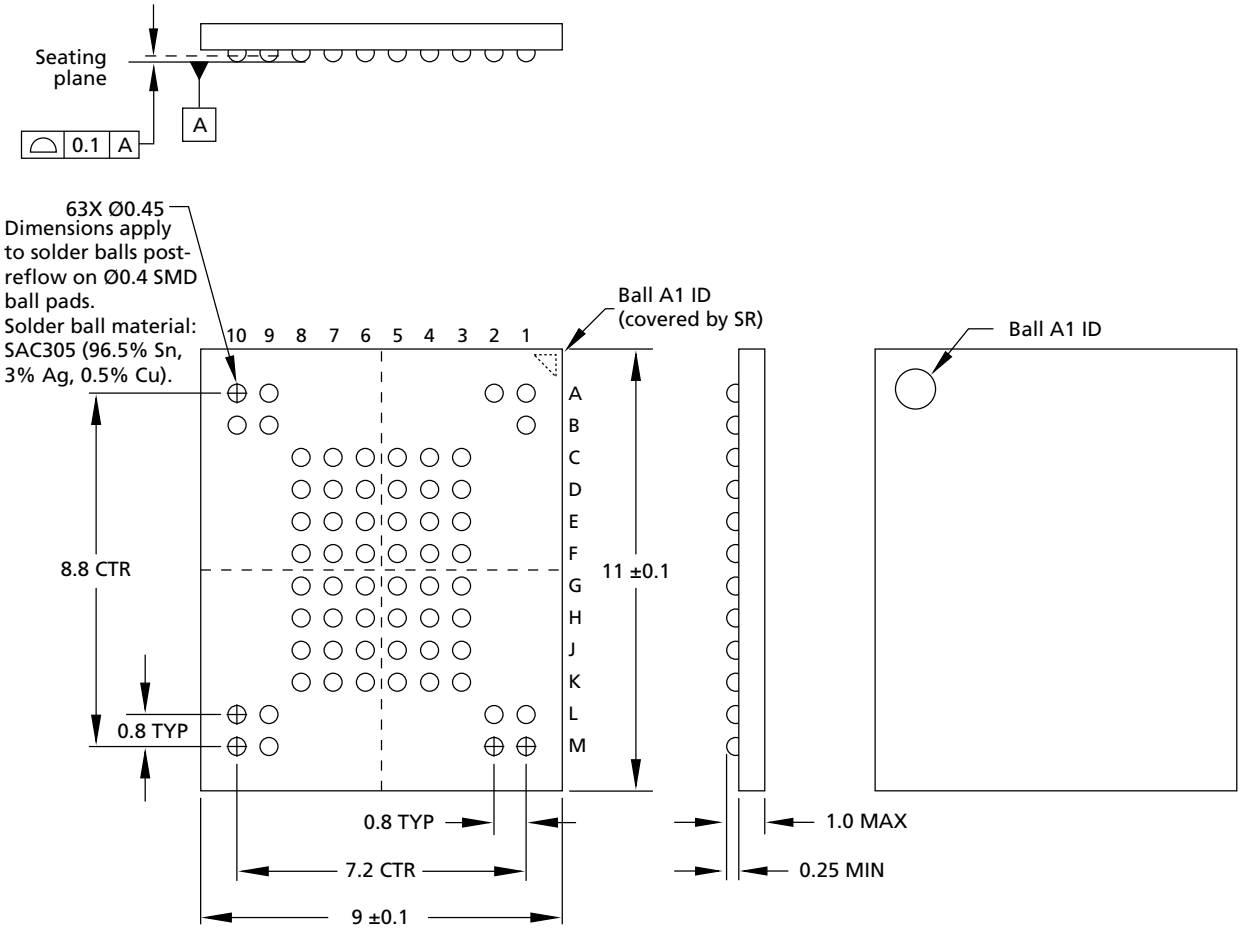
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Package Dimensions

Figure 3: 63-Ball VFBGA



Note: 1. All dimensions are in millimeters.

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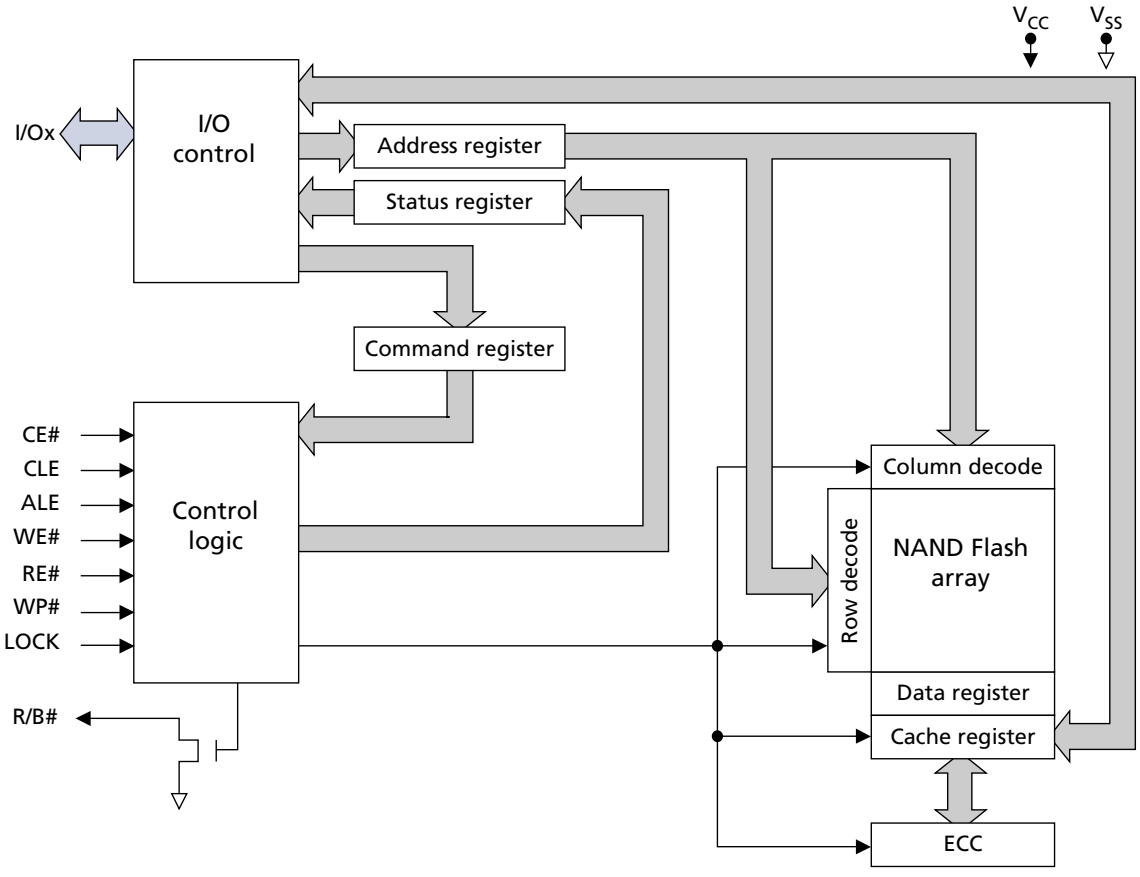
Architecture

These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte (x8) or word by word (x16), through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput. The status register reports the status of die operations.

Figure 4: NAND Flash Die (LUN) Functional Block Diagram



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Device and Array Organization

Figure 5: Array Organization - MT29F4G08

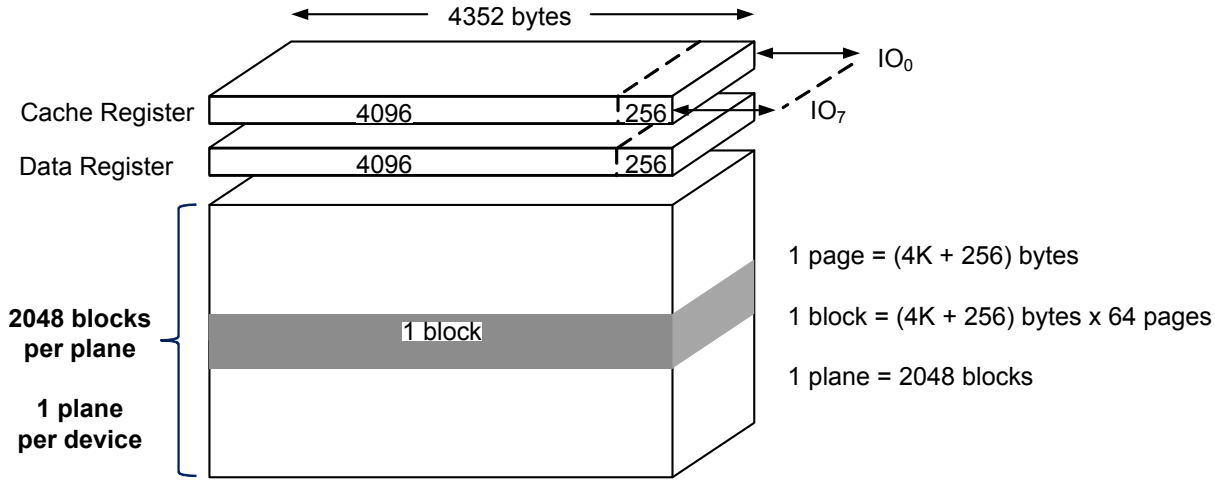


Table 2: Array Addressing (×8)

Cycle	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12[2]	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA16

Notes:
1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. If CA12 is 1, then CA[11:8] must be 0.

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Asynchronous Interface Bus Operation

The bus on the device is multiplexed. Data I/O, addresses, and commands all share the same pins. I/O[15:8] are used only for data in the ×16 configuration. Addresses and commands are always supplied on I/O[7:0].

The command sequence typically consists of a COMMAND LATCH cycle, ADDRESS INPUT cycles, and one or more DATA cycles, either READ or WRITE.

Table 3: Asynchronous Interface Mode Selection

Mode[1]	CE#	CLE	ALE	WE#	RE#	I/Ox	WP#
Standby[2]	H	X	X	X	X	X	0V/V_{CC}
Command input	L	H	L	↑	H	X	H
Address input	L	L	H	↑	H	X	H
Data input	L	L	L	↑	H	X	H
Data output	L	L	L	H	↓	X	X
Write protect	X	X	X	X	X	X	L

Notes:
1. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.
2. WP# should be biased to CMOS LOW or HIGH for standby.

Asynchronous Enable/Standby

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps to reduce power consumption.

The CE# "Don't Care" operation enables the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

Asynchronous Commands

An asynchronous command is written from I/O[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, including READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs) even when they are busy.

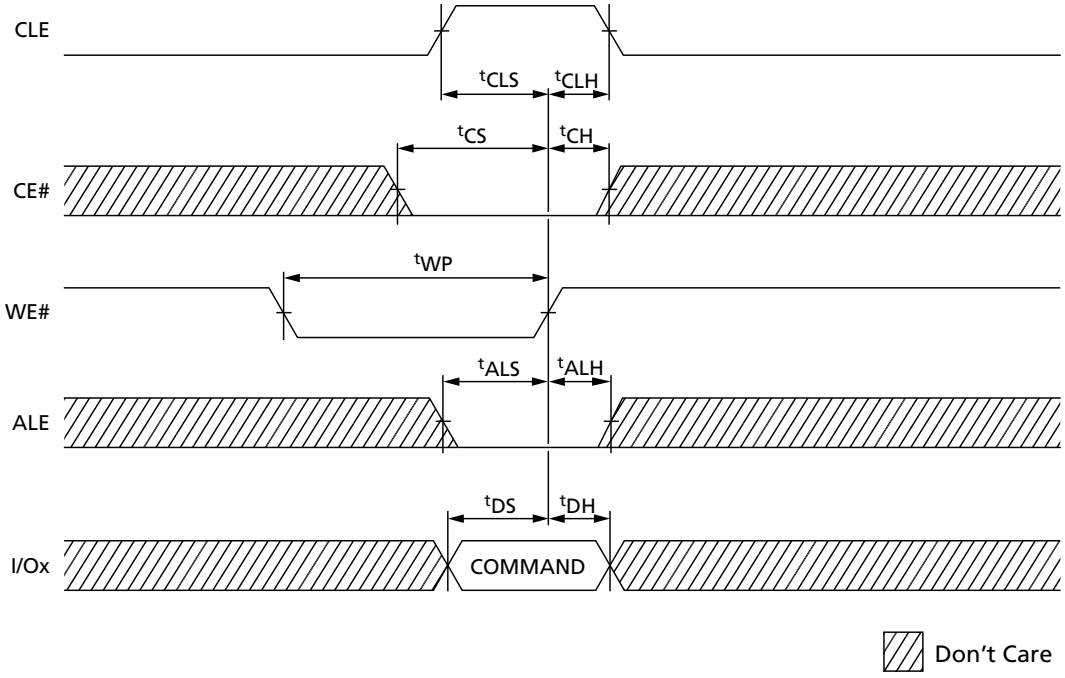
For devices with a ×16 interface, I/O[15:8] must be written with zeros when a command is issued.

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Figure 6: Asynchronous Command Latch Cycle



Asynchronous Addresses

An asynchronous address is written from I/O[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits that are not part of the address space must be LOW (see Device and Array Organization). The number of cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

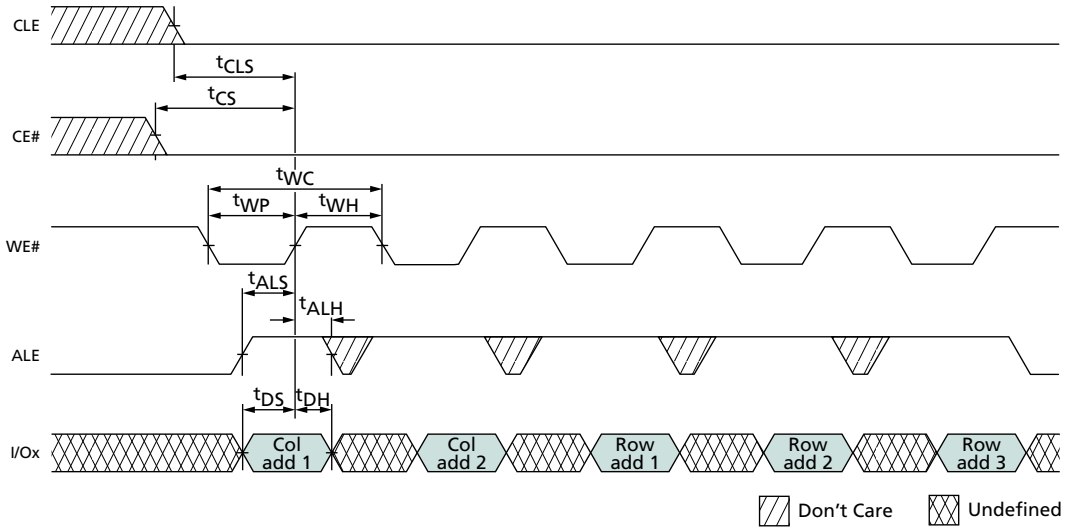
Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses are accepted by die (LUNs) even when they are busy; for example, like address cycles that follow the READ STATUS ENHANCED (78h) command.

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Figure 7: Asynchronous Address Latch Cycle



Asynchronous Data Input

Data is written from I/O[7:0] to the cache register of the selected die (LUN) on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is LOW, and RE# is HIGH.

Data input is ignored by die (LUNs) that are not selected or are busy (RDY = 0). Data is written to the data register on the rising edge of WE# when CE#, CLE, and ALE are LOW, and the device is not busy.

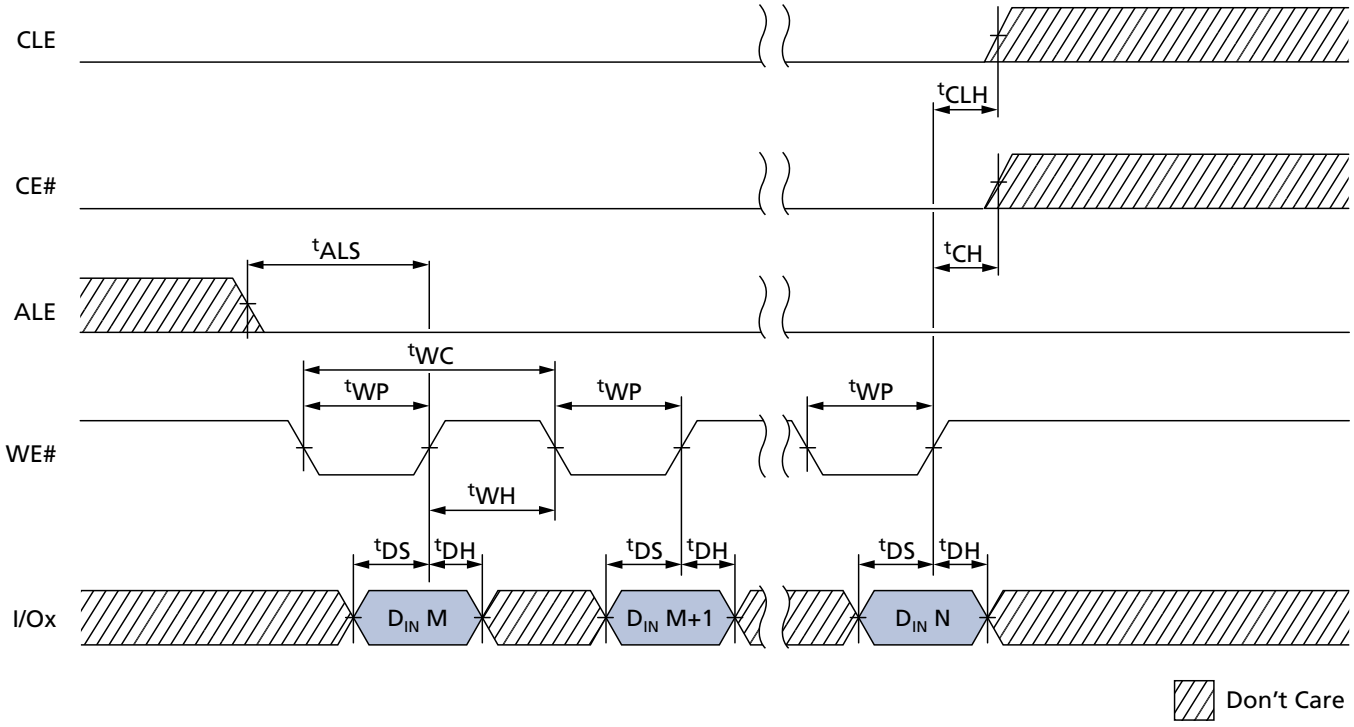
Data input utilizes I/O[7:0] on ×8 devices and I/O[15:0] on ×16 devices.

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Figure 8: Asynchronous Data Input Cycles



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Asynchronous Data Output

Data can be output from a die (LUN) if it is in a ready state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the cache register of the selected die (LUN) to IO bus on the falling edge of RE# when CE# is LOW, ALE is LOW, CLE is LOW, and WE# is HIGH.

If the host controller is using a ^{t}RC of 30ns or greater, the host can latch the data on the rising edge of RE# (see the figure below for proper timing). If the host controller is using a ^{t}RC of less than 30ns, the host can latch the data on the next falling edge of RE#.

Using the READ STATUS ENHANCED (78h) command prevents data contention following an interleaved die (multi-LUN) operation. After issuing the READ STATUS ENHANCED (78h) command, to enable data output, issue the READ MODE (00h) command.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by first issuing the READ STATUS or READ STATUS ENHANCED (78h) command.

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Figure 9: Asynchronous Data Output Cycles

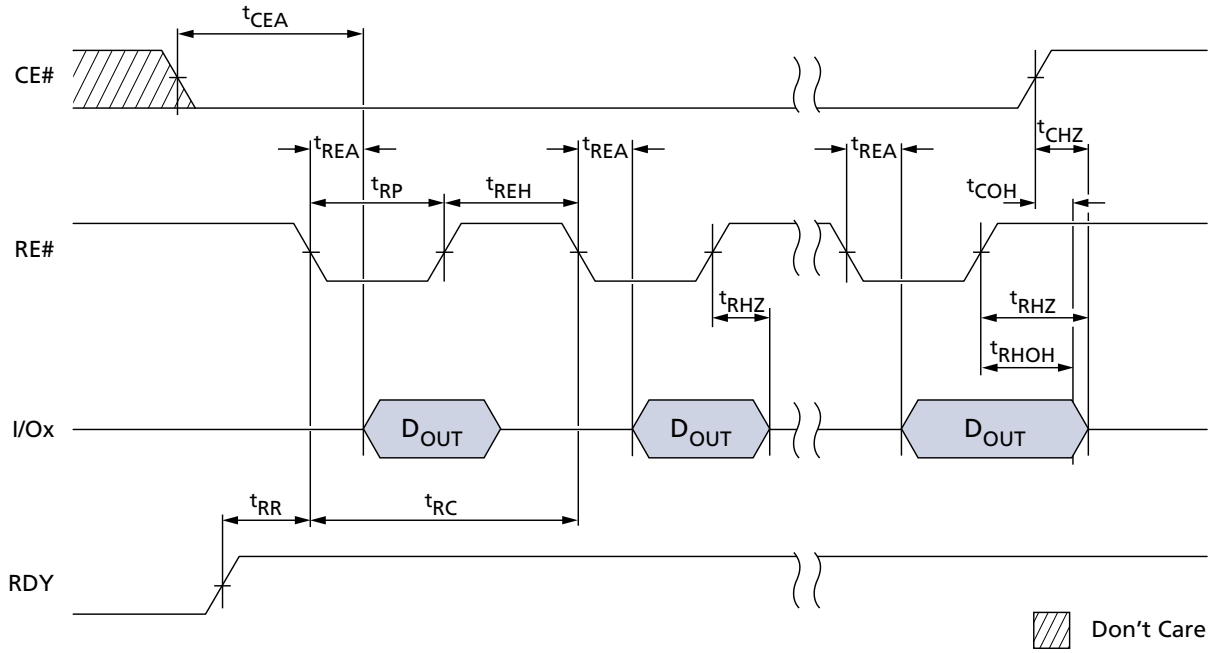
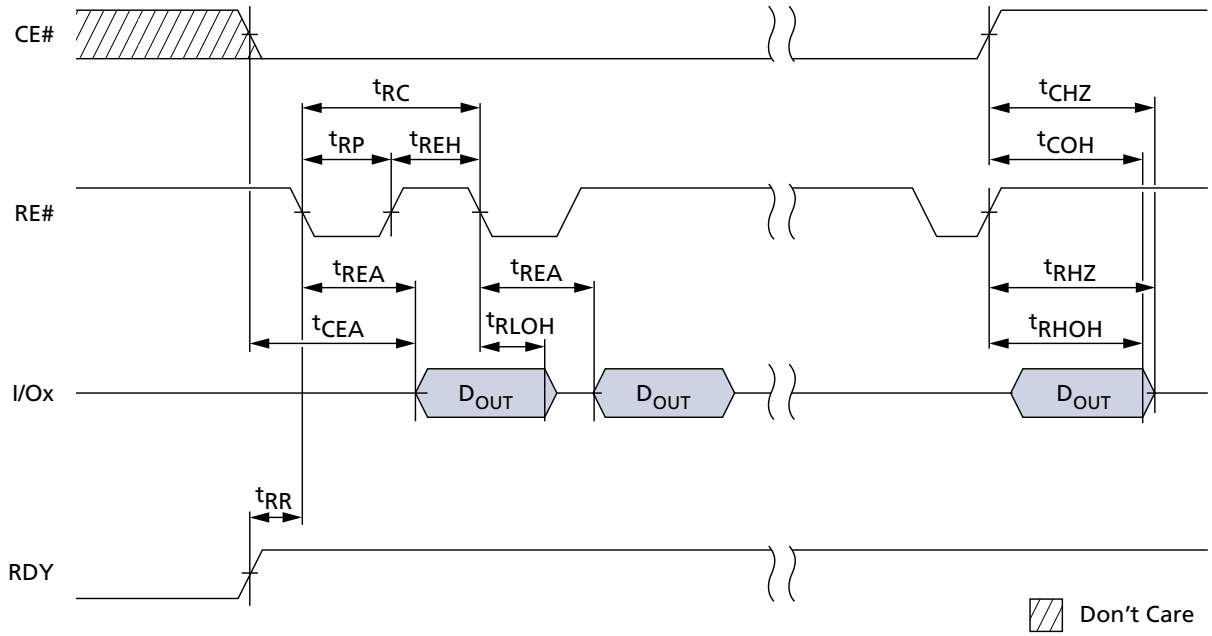


Figure 10: Asynchronous Data Output Cycles (EDO Mode)



Write Protect#

The write protect# (WP#) signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.

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It is recommended that the host drive WP# LOW during power-on until V_{CC} is stable to prevent inadvertent PROGRAM and ERASE operations (see Device Initialization for additional details).

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned, the host must wait ^{t}WW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy#

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy (RDY = 0). A target is ready when all of its die (LUNs) are ready (RDY = 1). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Status Operations for details regarding die (LUN) status).

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. Between the 10% and 90% points on the R/B# waveform, the rise time is approximately two time constants (T_C).

$$T_C = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 14 (page 23).

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

$$Rp = \frac{V_{CC}\,(MAX) - V_{OL}\,(MAX)}{I_{OL} + \Sigma_{IL}}$$

Where Σ_{IL} is the sum of the input currents of all devices tied to the R/B# pin.

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Figure 11: READ/BUSY# Open Drain

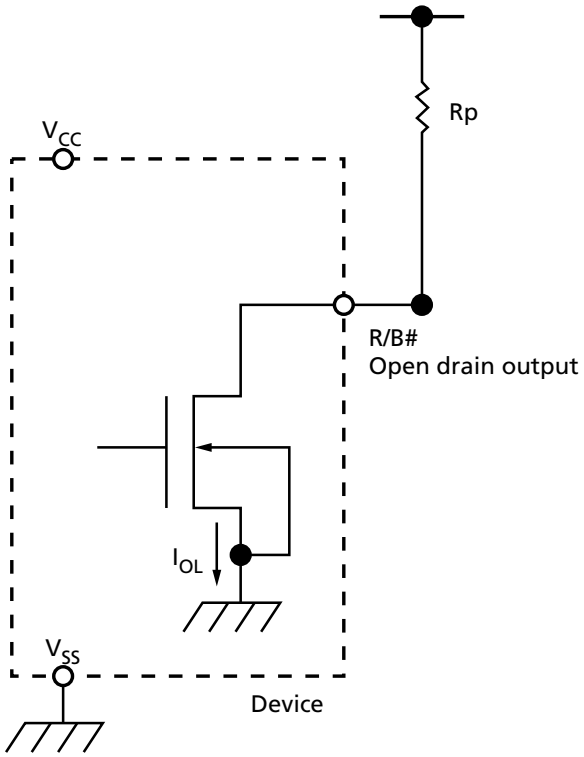
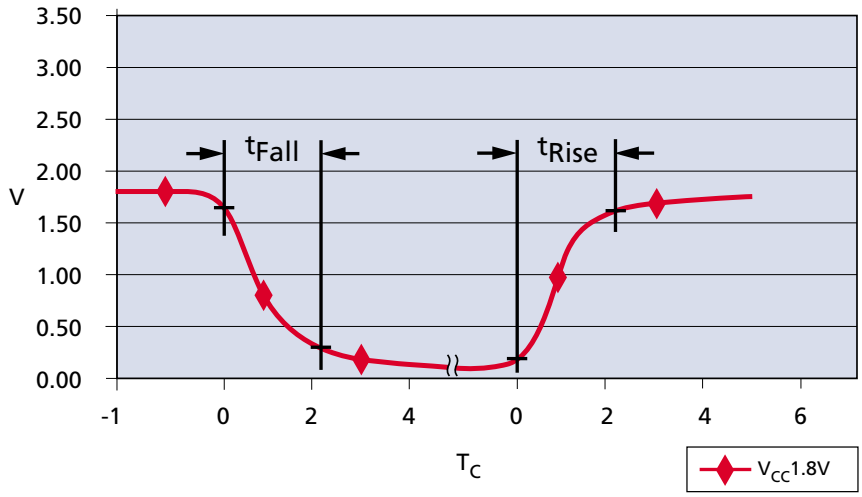


Figure 12: tFall and tRise (1.8V V_{CC})



Notes:
1. tFall and tRise are calculated at 10% and 90% points.
2. tRise is primarily dependent on external pull-up resistor and external capacitive loading.
3. tFall ≈ 7ns at 1.8V.
4. See TC values in Figure 14 (page 23) for TC and approximate Rp value.

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Figure 13: I_{OL} vs. Rp (1.8V V_{CC})

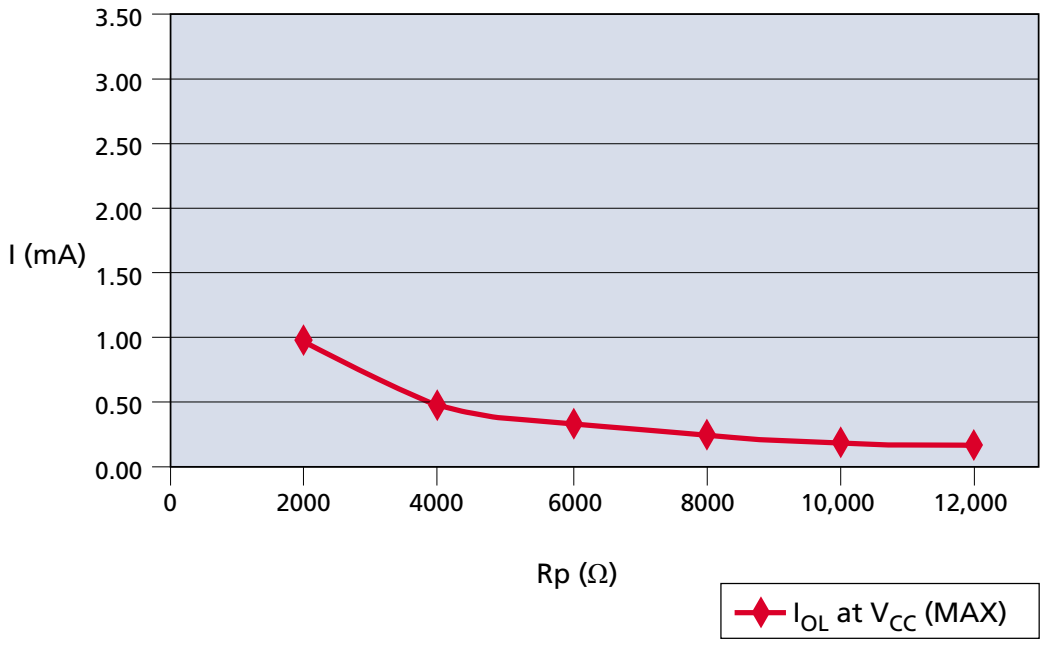
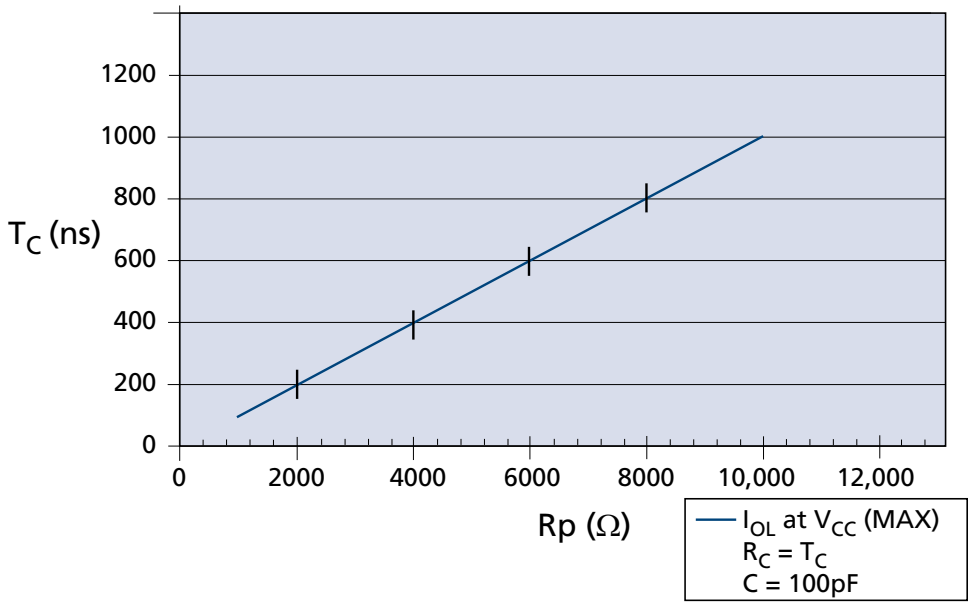


Figure 14: TC vs. Rp



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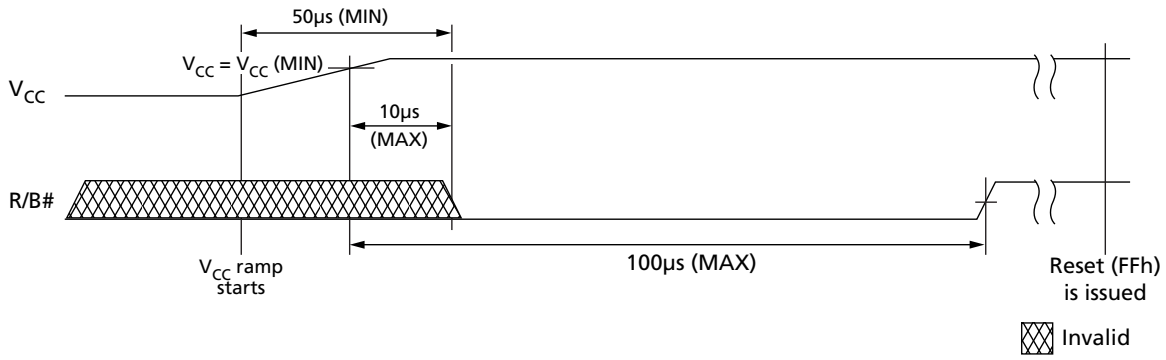
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Device Initialization

Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. (The WP# signal supports additional hardware protection during power transitions.) When ramping V_{CC}, use the following procedure to initialize the device:

1. Ramp V_{CC}.
2. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target. The R/B# signal becomes valid when 50µs has elapsed since the beginning the V_{CC} ramp, and 10µs has elapsed since V_{CC} reaches $V_{CC,min}$.
3. If not monitoring R/B#, the host must wait at least 100µs after V_{CC} reaches $V_{CC,min}$. If monitoring R/B#, the host must wait until R/B# is HIGH.
4. The asynchronous interface is active by default for each target. Each LUN draws less than an average of 10mA (I_{ST}) measured over intervals of 1ms until the RESET (FFh) command is issued.
5. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for 1ms after a RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.
6. The device is now initialized and ready for normal operation.

Figure 15: R/B# Power-On Behavior



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Power Cycle Requirements

Upon power-down the NAND device requires a maximum voltage and minimum time that the host must hold V_{CC} and V_{CCQ} below the voltage prior to power-on.

Table 4: Power Cycle Requirements

Device can not operate correctly when V_{CC} is lower than 2.5V@3.3V or 1.5V@1.8V.

Parameter	Value	Unit
Maximum V_{CC}/V_{CCQ}	100	mV
Minimum time below maximum voltage	100	nS

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Command Definitions

Table 5: Command Set

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[1]	Notes
Reset Operations							
RESET	FFh	0	–	–	Yes	Yes	–
Identification Operation							
READ ID	90h	1	–	–	No	No	–
READ PARAMETER PAGE	ECh	1	–	–	No	No	–
READ UNIQUE ID	EDh	1	–	–	No	No	–
Feature Operations							
GET FEATURES	EEh	1	–	–	No	No	–
SET FEATURES	EFh	1	4	–	No	No	–
Status Operations							
READ STATUS	70h	0	–	–	Yes	N/A	–
READ STATUS ENHANCED	78h	3	–	–	Yes	Yes	2
Column Address Operations							
RANDOM DATA READ	05h	2	–	E0h	No	Yes	–
RANDOM DATA INPUT	85h	2	Optional	–	No	Yes	–
PROGRAM FOR INTERNAL DATA MOVE	85h	5	Optional	–	No	Yes	3
READ Operations							
READ MODE	00h	0	–	–	No	Yes	–
READ PAGE	00h	5	–	30h	No	Yes	–
READ PAGE CACHE SEQUENTIAL	31h	0	–	–	No	Yes	4
READ PAGE CACHE RANDOM	00h	5	–	31h	No	Yes	4
READ PAGE CACHE LAST	3Fh	0	–	–	No	Yes	4
Program Operations							
PROGRAM PAGE	80h	5	Yes	10h	No	Yes	2
PROGRAM PAGE CACHE	80h	5	Yes	15h	No	Yes	2, 5
Erase Operations							
ERASE BLOCK	60h	3	–	D0h	No	Yes	–
Internal Data Move Operations							
READ FOR INTERNAL DATA MOVE	00h	5	–	35h	No	Yes	3

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Table 5: Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[1]	Notes
PROGRAM FOR INTERNAL DATA MOVE	85h	5	Optional	10h	No	Yes	–
Block Lock Operations							
BLOCK UNLOCK LOW	23h	3	–	–	No	Yes	–
BLOCK UNLOCK HIGH	24h	3	–	–	No	Yes	–
BLOCK LOCK	2Ah	–	–	–	No	Yes	–
BLOCK LOCK-TIGHT	2Ch	–	–	–	No	Yes	–
BLOCK LOCK READ STATUS	7Ah	3	–	–	No	Yes	–
PERMANENT BOOT BLOCK PROTECT	–	–	–	–	No	Yes	–
PERMANENT BOOT BLOCK PROTECT	83h	5	–	10h	No	Yes	–
PERMANENT BOOT BLOCK PROTECT Disable	80h	5	Yes	10h	No	No	–
One-Time Programmable (OTP) Operations							
OTP DATA LOCK BY BLOCK (ONFI)	80h	5	No	10h	No	No	6
OTP DATA PROGRAM (ONFI)	80h	5	Yes	10h	No	No	6
OTP DATA READ (ONFI)	00h	5	No	30h	No	No	6

Notes:
1. Busy means RDY = 0.
2. These commands can be used for interleaved die (multi-LUN) operations (applicable to Multi-LUN Operations).
3. Do not cross plane address boundaries when using READ for INTERNAL DATA MOVE and PROGRAM for INTERNAL DATA MOVE.
4. Issuing a READ PAGE CACHE series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE series command; otherwise, it is prohibited.
5. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.
6. OTP commands can be entered only after issuing the SET FEATURES command with the feature address.

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Reset Operations

RESET (FFh)

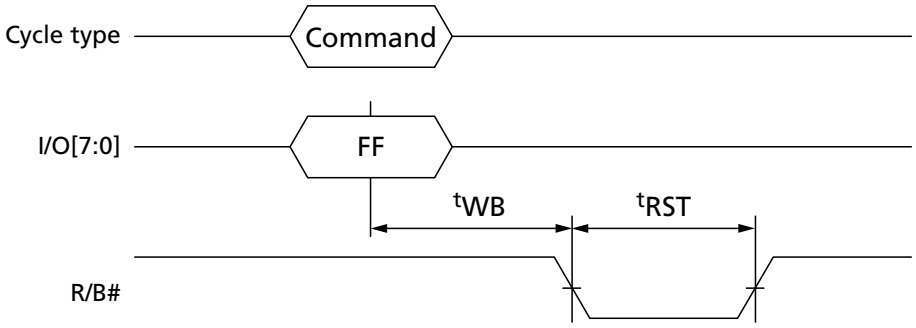
The RESET command is used to put the memory device into a known condition and to abort the command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are marked invalid.

The status register contains the value E0h when WP# is HIGH; otherwise it is written with a 60h value. R/B# goes LOW for ^{t}RST after the RESET command is written to the command register.

The RESET command must be issued to all CE#s as the first command after power-on. The device will be busy for a maximum of 1ms.

Figure 16: RESET (FFh) Operation



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Identification Operations

READ ID (90h)

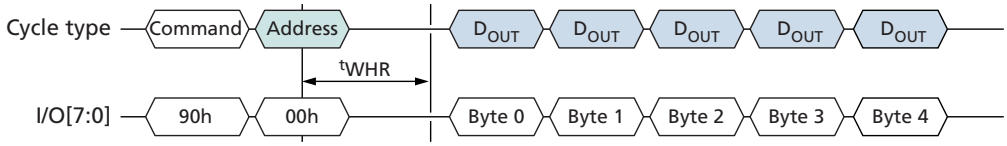
The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by an 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information.

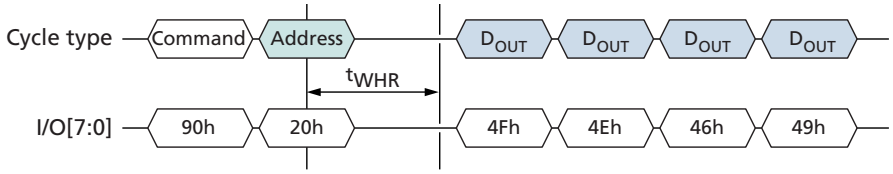
When the 90h command is followed by a 20h address cycle, the target returns the 4-byte ONFI identifier code.

Figure 17: READ ID (90h) with 00h Address Operation



Note: 1. See READ ID Parameter tables for byte definitions.

Figure 18: READ ID (90h) with 20h Address Operation



Note: 1. See READ ID Parameter tables for byte definitions.

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READ ID Parameter Tables

Table 6: READ ID Parameters for Address 00h

Byte	Options	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00	Value
Byte 0 – Manufacturer ID										
Manufacturer	Micron	0	0	1	0	1	1	0	0	2Ch
Byte 1 – Device ID										
MT29F4G08ABBFA	4Gb, ×8, 1.8V	1	0	1	0	1	1	0	0	ACh
Byte 2										
Number of die per CE	1							0	0	00b
Cell type	SLC					0	0			00b
Number of simultaneously programmed pages	1			0	0					00b
Interleaved operations between multiple die	Not supported for 4Gb		0							0b
Cache programming	Supported	1								1b
Byte value	4Gb	1	0	0	0	0	0	0	0	80h
Byte 3										
Page size	4KB							1	0	10b
Spare area size (bytes)	256B						1			1b
Block size (without spare)	256KB			1	0					10b
Organization	×8		0							0b
Serial access (MIN) 1.8V	30ns	0				0				0b
Byte value	×8, 1.8V	0	0	1	0	0	1	1	0	26h
Byte 4										
Internal ECC level	8-bit ECC/512B (main) + 16B (Spare)+16B (parity) bytes							1	0	10b
Planes per CE#	1					0	1			01b
Plane size	4Gb		1	1	0					110b
Internal ECC	ECC Disabled	0								0b
Byte value	4Gb	0	1	1	0	0	0	1	0	62h

Note: 1. b = binary; h = hexadecimal.

Table 7: READ ID Parameters for Address 20h

Byte	Options	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00	Value
0	“O”	0	1	0	0	1	1	1	1	4Fh
1	“N”	0	1	0	0	1	1	1	0	4Eh
2	“F”	0	1	0	0	0	1	1	0	46h
3	“I”	0	1	0	0	1	0	0	1	49h

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Table 7: READ ID Parameters for Address 20h (Continued)

Byte	Options	I/07	I/06	I/05	I/04	I/03	I/02	I/01	I/00	Value
4	Undefined	X	X	X	X	X	X	X	X	XXh

Note: 1. h = hexadecimal; X = V_{IH} or V_{IL}.

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READ PARAMETER PAGE (ECh)

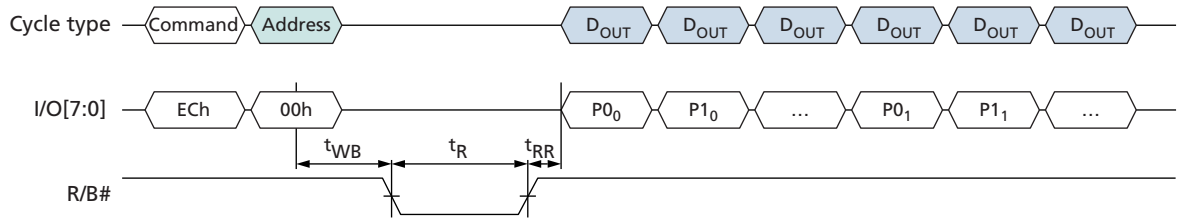
The READ PARAMETER PAGE (ECh) command is used to read the ONFI parameter page programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. Use of the READ STATUS ENHANCED (78h) command is prohibited while the target is busy and during data output.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the RANDOM DATA READ (05h-E0h) command can be used to change the location of data output.

Figure 19: READ PARAMETER (ECh) Operation



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Parameter Page Data Structure Table

Table 8: Parameter Page Data Structure

Byte	Description	Value (hex)
0–3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4–5	Revision number	02h, 00h
6–7	Feature support	x8: 10h, 00h
8–9	Optional commands support	3Fh, 00h
10–31	Reserved	00h
32–43	Device manufacturer	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44–63	Device model: MT29F4G08ABBFA	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 30h, 38h, 41h, 42h, 42h, 46h, 41h, 33h, 57h, 20h, 20h, 20h, 20h
44–63	Device model: MT29F4G16ABBFA	4Dh, 54h, 32h, 39h, 46h, 34h, 47h, 31h, 36h, 41h, 42h, 42h, 46h, 41h, 33h, 57h, 20h, 20h, 20h, 20h
64	Manufacturer ID	2Ch
65–66	Date code	00h
67–79	Reserved	00h
80–83	Number of data bytes per page	00h, 10h, 00h, 00h
84–85	Number of spare bytes per page	00h, 01h
86–89	Number of data bytes per partial page	00h, 04h, 00h, 00h
90–91	Number of spare bytes per partial page	40h, 00h
92–95	Number of pages per block	40h, 00h, 00h, 00h
96–99	Number of blocks per unit	00h, 08h, 00h, 00h
100	Number of logical units	01h
101	Number of address cycles	23h
102	Number of bits per cell	01h
103–104	Bad blocks maximum per unit	28h, 00h
105–106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	08h
108–109	Block endurance for guaranteed valid blocks	00h
110	Number of programs per page	04h
111	Partial programming attributes	00h
112	Number of ECC bits	08h
113	Number of interleaved address bits	01h
114	Interleaved operation attributes	0Eh
115–127	Reserved	00h
128	I/O pin capacitance	08h
129–130	Timing mode support	0Fh, 00h
131–132	Program cache timing	0Fh, 00h
133–134	^{t}PROG (MAX) page program time	58h, 02h

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Table 8: Parameter Page Data Structure (Continued)

Byte	Description	Value (hex)
135–136	^{t}ERS (MAX) block erase time	10h, 27h
137–138	^{t}R (MAX) page read time	AAh, 00h
139–140	^{t}CCS (MIN)	64h, 00h
141–163	Reserved	00h
164–165	Vendor-specific revision number	01h, 00h
166–179	Vendor-specific	00h, 00h, 00h, 02h, 04h, 80h, 01h, 81h, 04h, 03h, 02h, 01h, 30h, 90h
180–247	Reserved	00h
248	ECC maximum correct ability	00h
249	Die select feature	00h
250–253	Reserved	00h
254–255	Integrity CRC	Calculated
256–512	2nd copy of the parameter table	
513–768	3rd copy of the parameter table	
769–2048	Additional redundant parameter pages	

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READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

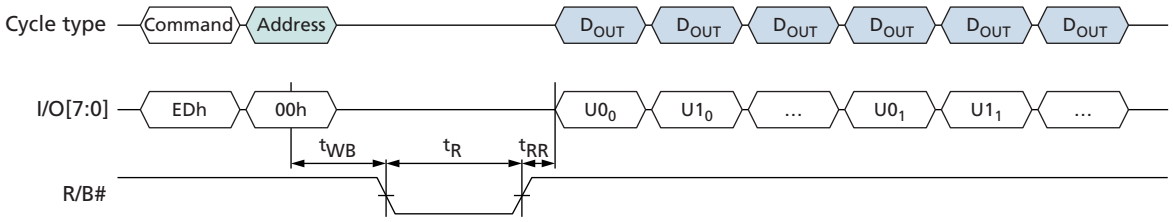
When the EDh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After ^{t}R completes, the host enables data output mode to read the unique ID. When the asynchronous interface is active, one data byte is output per RE# toggle.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the RANDOM DATA READ (05h-E0h) command can be used to change the data output location.

The upper eight I/Os on a x16 device are not used and are a "Don't Care" for x16 devices.

Figure 20: READ UNIQUE ID (EDh) Operation



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Feature Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which sub-feature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in below. The SET FEATURES (EFh) command writes sub-feature parameters (P1–P4) to the specified feature address. The GET FEATURES command reads the sub-feature parameters (P1–P4) at the specified feature address.

Table 9: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable RB# pull-down strength
82h–FFh	Reserved
90h	Array operation mode

Table 10: Feature Addresses 90h: Timing Mode

Sub-feature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Timing mode	Normal	Reserved (0)							0	00h	1
	OTP operation	Reserved (0)							1	01h	
	OTP protection	Reserved (0)						1	1	03h	
	Disable ECC	Reserved (0)				0	0	0	0	00h	3
	Enable ECC	Reserved (0)				1	0	0	0	08h	1, 2
	Permanent block lock disable	Reserved (0)			1	0	0	0	0	10h	4
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Notes:
1. These bits are reset to 00h after power cycle.
2. Bit3 is used to enable/disable ECC. For ECC always on or ECC always off configuration, bit3 is reserved (0) and should be set to 0.
3. For MPNs with "-ITE" ECC enabled by default, this bit is Reserved.

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4. If Permanent block lock disable sequence is issued again to a part that has already been disabled, the part will be busy for tOBSY and exit with SR=60h. The part will be busy for tOBSY_ECC when ECC is enabled.

SET FEATURES (EFh)

The SET FEATURES (EFh) command writes the subfeature parameters (P1–P4) to the specified feature address to enable or disable target-specific features.

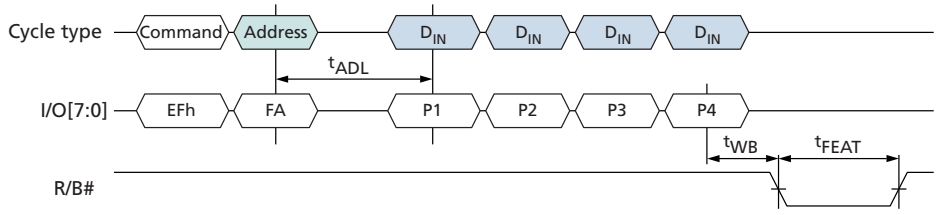
Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address. The host waits for tADL before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#.

After all four subfeature parameters are input, the target goes busy for tFEAT. The READ STATUS (70h) command can be used to monitor for command completion.

Feature address 01h (timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for tITC.

Figure 21: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

The GET FEATURES (EEh) command reads the subfeature parameters (P1–P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for tFEAT. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the READ STATUS ENHANCED (78h) command is prohibited.

After tFEAT completes, the host enables data output mode to read the subfeature parameters.

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Figure 22: GET FEATURES (EEh) Operation

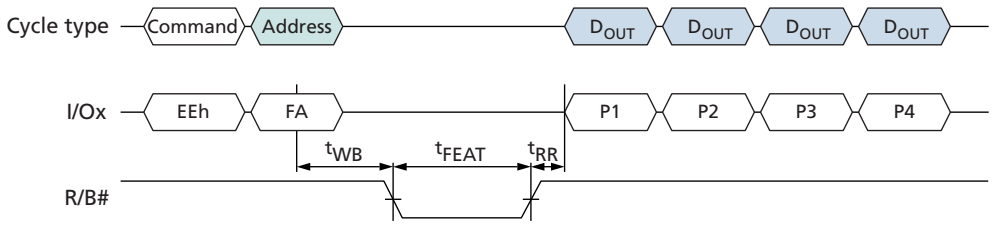


Table 11: Feature Addresses 01h: Timing Mode

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Timing mode	Mode 0 (default)	Reserved (0)					0	0	0	00h	1
	Mode 1	Reserved (0)					0	0	1	01h	
	Mode 2	Reserved (0)					0	1	0	02h	
	Mode 3	Reserved (0)					0	1	1	03h	
	Mode 4	Reserved (0)					1	0	0	04h	
	Mode 5	Reserved (0)					1	0	1	05h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note: 1. The timing mode feature address is used to change the default timing mode. The timing mode should be selected to indicate the maximum speed at which the device will receive commands, addresses, and data cycles. The five supported settings for the timing mode are shown. The default timing mode is mode 0. The device returns to mode 0 when the device is power cycled. Supported timing modes are reported in the parameter page.

Table 12: Feature Addresses 80h: Programmable I/O Drive Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											

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Table 12: Feature Addresses 80h: Programmable I/O Drive Strength (Continued)

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note: 1. The programmable drive strength feature address is used to change the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive strength settings. The default drive strength is full strength. The device returns to the default drive strength mode when the device is power cycled. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.

Table 13: Feature Addresses 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarters							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

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Status Operations

Each die (LUN) provides its status independently of other die (LUNs) on the same target through its 8-bit status register.

When a READ STATUS (70h) or READ STATUS ENHANCED (78h) command is issued, status register output is enabled. Status register contents are returned on I/O[7:0] for each data output request.

When the asynchronous interface is active and status register output is enabled, changes in the status register are seen on I/O[7:0] when CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

While monitoring the status register for completion of a data transfer from the Flash array to the data register (^{t}R), the host must issue the READ MODE (00h) command to disable the status register and enable data output (see Read Operations).

The READ STATUS (70h) command returns the status of the most recently selected die (LUN). To prevent data contention during or following an interleaved die (multi-LUN) operation, the host must enable only one die (LUN) for status output by using the READ STATUS ENHANCED (78h) command (see Interleaved Die (Multi-LUN) Operations).

Table 14: Status Register Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Description
7	Write protect	Write protect	Write protect	Write protect	Write protect	0 = Protected 1 = Not protected
6	RDY	RDY cache	RDY	RDY cache	RDY	0 = Busy (PROGRAM operation in progress) 1 = Ready (Cache can accept data; R/B# follows)
5	ARDY	ARDY	ARDY	ARDY	ARDY	0 = Busy (PROGRAM operation in progress) 1 = Ready (Internal operations completed, if cache mode is used)
4	0	0	ECC status[1]	ECC status (N–1)[1]	0	00 = Normal or uncorrectable 01 = 4~6 10 = 1~3 11 = 7~8 (Rewrite recommended)
3	0	0			0	
2	–	–	–	–	–	Don't Care
1	FAILC (N–1)	FAILC (N–1)	Reserved	–	–	0 = Pass 1 = Fail This bit is valid only when RDY (SR bit 6) is 1. This bit retains the status of the previous valid program operation when the most recent program operation is complete.

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Table 14: Status Register Definition (Continued)

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Description
0	FAIL	FAIL (N)	FAIL[2]	FAIL (N-1)	FAIL	0 = Pass 1 = Fail This bit is set if the most recent finished operation on the selected die (LUN) failed. This bit is valid only when ARDY (SR bit 5) is 1.

Notes:
1. Bit = 11 when a rewrite is recommended because the page includes READ errors per sector (512-Byte [main] + 16-Byte [spare] + 16-Byte [parity]). When ECC is enabled, up to 7~8-bit error is corrected automatically.
2. A status register bit defined as FAIL signifies that an uncorrectable READ error has occurred.

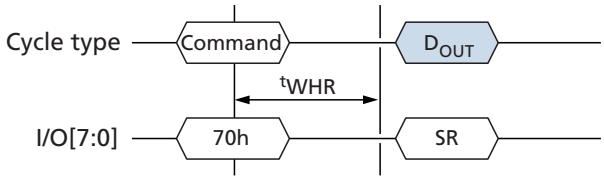
READ STATUS (70h)

The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select the die (LUN) that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more die (LUNs) could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single die (LUN) operations.

Figure 23: READ STATUS (70h) Operation



READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

Writing 78h to the command register, followed by row address cycles containing the page, block, and LUN addresses, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

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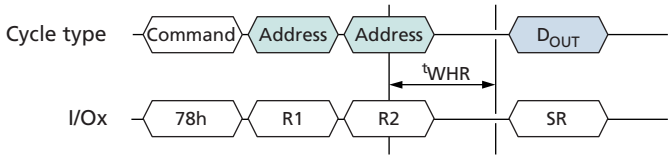
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The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all planes on the selected die (LUN). The FAILC and FAIL bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output.

Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other reset, identification, and configuration operations. See individual operations for specific details.

Figure 24: READ STATUS ENHANCED (78h) Operation



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Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

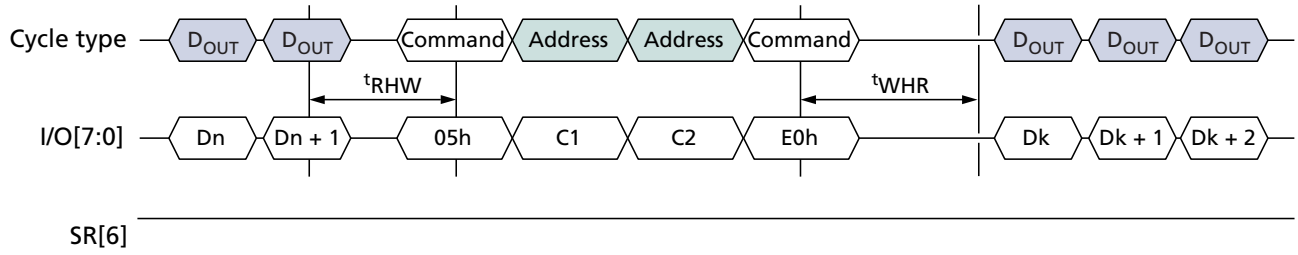
RANDOM DATA READ (05h-E0h)

The RANDOM DATA READ (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE READ operations (RDY = 1; ARDY = 0).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least ^{t}WHR before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be issued prior to issuing the RANDOM DATA READ (05h-E0h). In this situation, using the RANDOM DATA READ (05h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention because two or more die (LUNs) could output data.

Figure 25: RANDOM DATA READ (05h-E0h) Operation



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RANDOM DATA INPUT (85h)

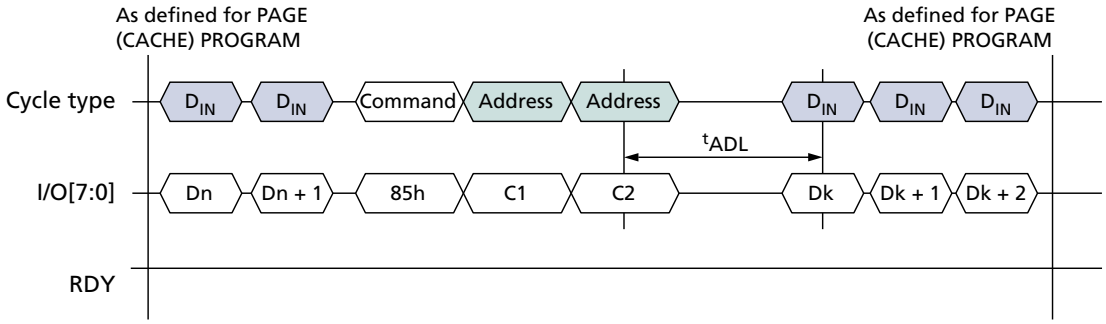
The RANDOM DATA INPUT (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache program operations (RDY = 1; ARDY = 0).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least ^{t}ADL before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The RANDOM DATA INPUT (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE CACHE (80h-15h) and PROGRAM FOR INTERNAL DATA MOVE (85h-10h).

In devices that have more than one die (LUN) per target, the RANDOM DATA INPUT (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

Figure 26: RANDOM DATA INPUT (85h) Operation



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PROGRAM FOR INTERNAL DATA INPUT (85h)

The PROGRAM FOR INTERNAL DATA INPUT (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache programming operations (RDY = 1; ARDY = 0).

Write 85h to the command register. Then write two column address cycles and row address cycles. This updates the page and block destination of the selected device for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least ^{t}ADL before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The PROGRAM FOR INTERNAL DATA INPUT (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE CACHE (80h-15h) and PROGRAM FOR INTERNAL DATA MOVE (85h-10h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

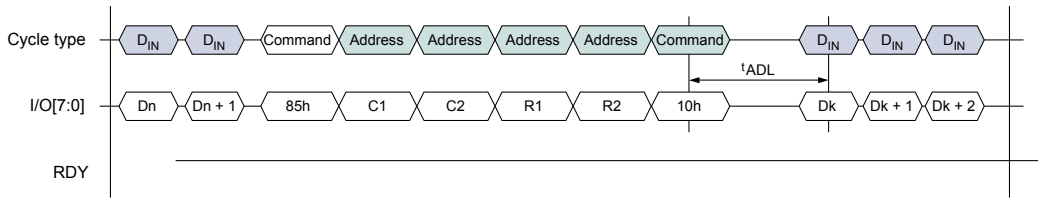
The PROGRAM FOR INTERNAL DATA INPUT (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

The PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used with the RANDOM DATA READ (05h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM FOR INTERNAL DATA MOVE command sequence to modify one or more bytes of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

Figure 27: PROGRAM FOR INTERNAL DATA INPUT (85h) Operation



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Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: RANDOM DATA READ (05h-E0h) and RANDOM DATA INPUT (85h).

Read Cache Operations

To increase data throughput, the READ PAGE CACHE series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

To begin a read page cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command. R/B# goes LOW during ^{t}R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h) – copies the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h) – copies the page specified in this command from the NAND Flash array to its corresponding data register

After the READ PAGE CACHE series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the next page begins copying data from the array to the data register. After ^{t}RCBSY, R/B# goes HIGH and the die's (LUN's) status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache register becomes available and the page requested in the READ PAGE CACHE operation is transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data output by the die (LUN).

After outputting the desired number of bytes from the cache register, either an additional READ PAGE CACHE series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the data register is copied into the cache register. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache register is available and that the die (LUN) is ready. Data can then be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), READ PAGE CACHE series (31h, 00h-31h), RANDOM DATA READ (05h-E0h), and RESET (FFh).

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READ MODE (00h)

The READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register after a READ operation (00h-30h, 00h-3Ah, 00h-35h) has been monitored with a status operation (70h, 78h). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to issuing the READ MODE (00h) command. This prevents bus contention.

READ PAGE (00h-30h)

The READ PAGE (00h–30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, write the 00h command to the command register, then write *n* address cycles to the address registers, and conclude with the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

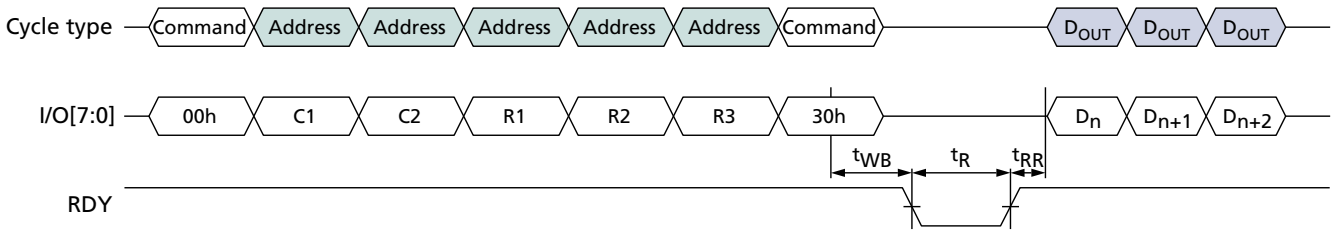
To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

During data output the RANDOM DATA READ (05h-E0h) command can be issued.

When internal ECC is enabled, the READ STATUS (70h) command is required after the completion of the data transfer ($^{t}R_ECC$) to determine whether an uncorrectable read error occured. ($^{t}R_ECC$ is the data transferred with internal ECC enabled.)

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to the issue of the READ MODE (00h) command. This prevents bus contention.

Figure 28: READ PAGE (00h-30h) Operation

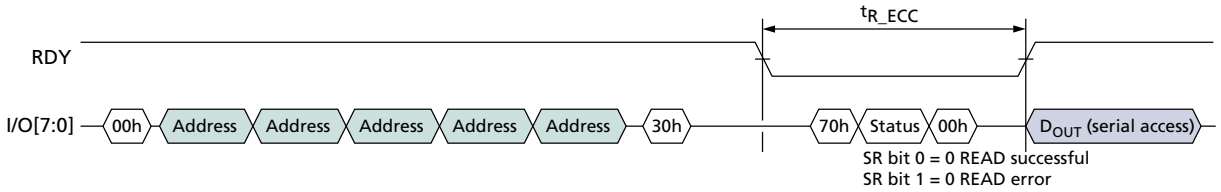


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Figure 29: READ PAGE (00h-30h) Operation with Internal ECC Enabled



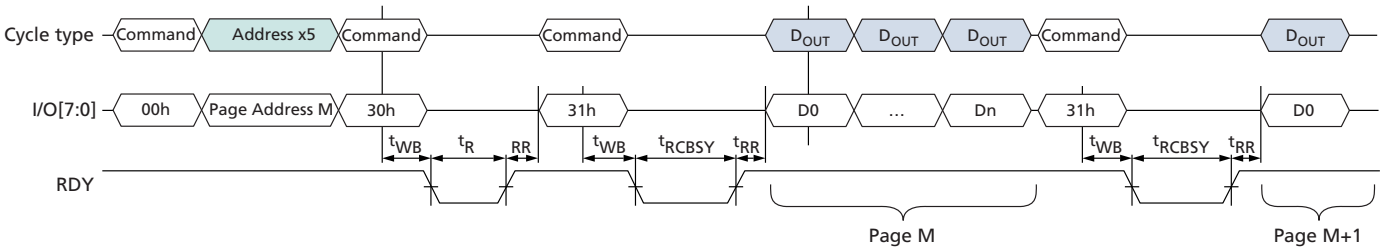
READ PAGE CACHE SEQUENTIAL (31h)

The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 31h to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for tRCBSY. After tRCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in which the 31h command was issued. Do not issue the READ PAGE CACHE SEQUENTIAL (31h) to cross die (LUN) boundaries. Instead, issue the READ PAGE CACHE LAST (3Fh) command.

Figure 30: READ PAGE CACHE SEQUENTIAL (31h) Operation



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READ PAGE CACHE RANDOM (00h-31h)

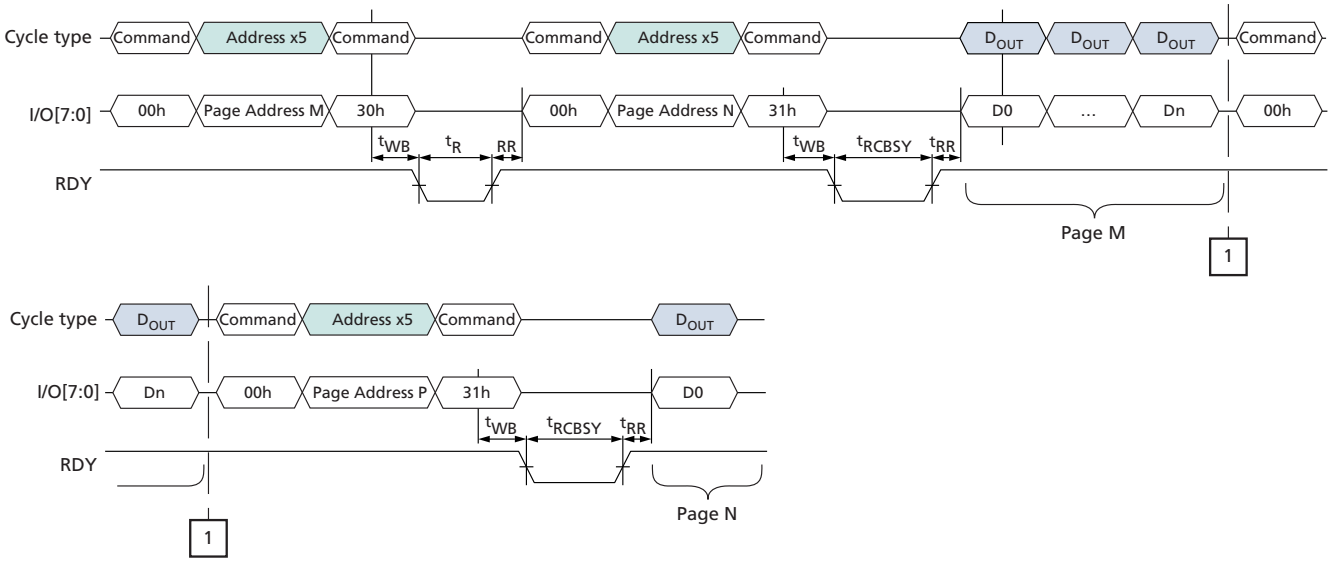
The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 00h to the command register, then write *n* address cycles to the address register, and conclude by writing 31h to the command register. The column address in the address specified is ignored. The die (LUN) address must match the same die (LUN) address as the previous READ PAGE (00h-30h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

Figure 31: READ PAGE CACHE RANDOM (00h-31h) Operation



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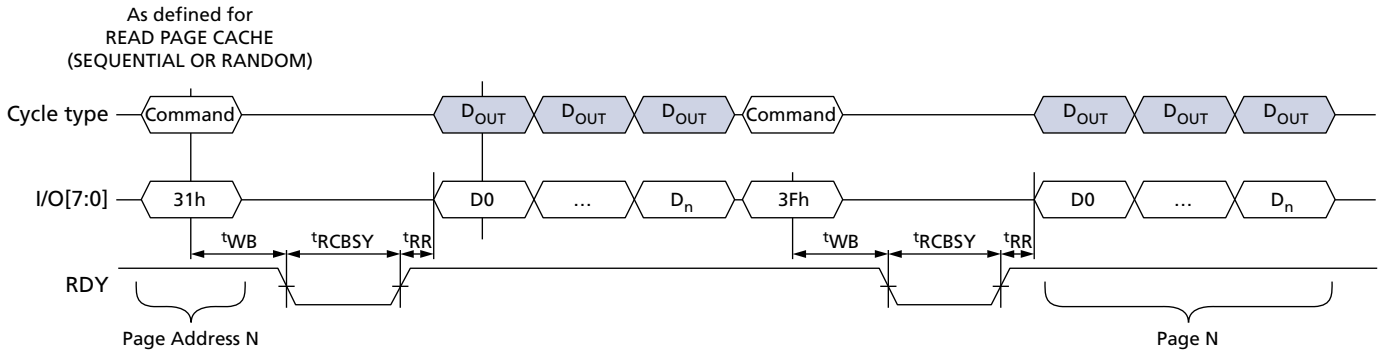
READ PAGE CACHE LAST (3Fh)

The READ PAGE CACHE LAST (3Fh) command ends the read page cache sequence and copies a page from the data register to the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue the READ PAGE CACHE LAST (3Fh) command, write 3Fh to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, data can be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

Figure 32: READ PAGE CACHE LAST (3Fh) Operation



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Program Operations

Program operations are used to move data from the cache or data registers to the NAND array. During a program operation the contents of the cache and/or data registers are modified by the internal control logic.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (0, 1, 2, ….., 63). During a program operation, the contents of the cache and/or data registers are modified by the internal control logic.

Program Operations

The PROGRAM PAGE (80h-10h) command programs one page from the cache register to the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

Program Cache Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve program operation system performance. When this command is issued, the die (LUN) goes busy (RDY = 0, ARDY = 0) while the cache register contents are copied to the data register, and the die (LUN) is busy with a PROGRAM CACHE operation (RDY = 1, ARDY = 0. While the contents of the data register are moved to the NAND Flash array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) command.

For PROGRAM PAGE CACHE series (80h-15h) operations, during the die (LUN) busy times, ^{t}CBSY and ^{t}LPROG, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and reset (FFh). When RDY = 1 and ARDY = 0, the only valid commands during PROGRAM PAGE CACHE series (80h-15h) operations are status operations (70h, 78h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE (80h-10h), RANDOM DATA INPUT (85h), PROGRAM FOR INTERNAL DATA INPUT (85h), and RESET (FFh).

PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and moves the data from the cache register to the specified block and page address in the array of the selected die (LUN). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) when it is busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write *n* address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT (85h) and PROGRAM FOR INTERNAL DATA INPUT (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PROG as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

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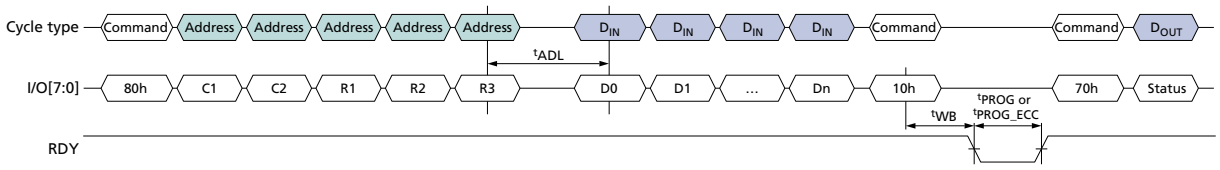
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In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

When internal ECC is enabled, the duration of array programming time is ^{t}PROG_ECC. During ^{t}PROG_ECC, the internal ECC generates parity bits when error detection is complete.

Figure 33: PROGRAM PAGE (80h-10h) Operation



PROGRAM PAGE CACHE (80h-15h)

The PROGRAM PAGE CACHE (80h-15h) command enables the host to input data to a cache register; copies the data from the cache register to the data register; then moves the data register contents to the specified block and page address in the array of the selected die (LUN). After the data is copied to the data register, the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) commands. The PROGRAM PAGE CACHE (80h-15h) command is accepted by the die (LUN) when it is ready (RDY =1, ARDY = 1). It is also accepted by the die (LUN) when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register to move it to the NAND array at the block and page address specified, write 80h to the command register. Issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write *n* address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT (85h) and PROGRAM FOR INTERNAL DATA INPUT (85h) commands may be issued. When data input is complete, write 15h to the command register. The selected LUN will go busy
(RDY = 0, ARDY = 0) for ^{t}CBSY to allow the data register to become available from a previous program cache operation, to copy data from the cache register to the data register, and then to begin moving the data register contents to the specified page and block address.

To determine the progress of ^{t}CBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is busy with a PROGRAM CACHE operation (RDY = 1, ARDY = 0), the host should check the status of the FAILC bit to see if a previous cache operation was successful.

If, after ^{t}CBSY, the host wants to wait for the PROGRAM CACHE operation to complete, without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is 1. The host should then check the status of the FAIL and FAILC bits.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be

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used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

Figure 34: PROGRAM PAGE CACHE (80h–15h) Operation (Start)

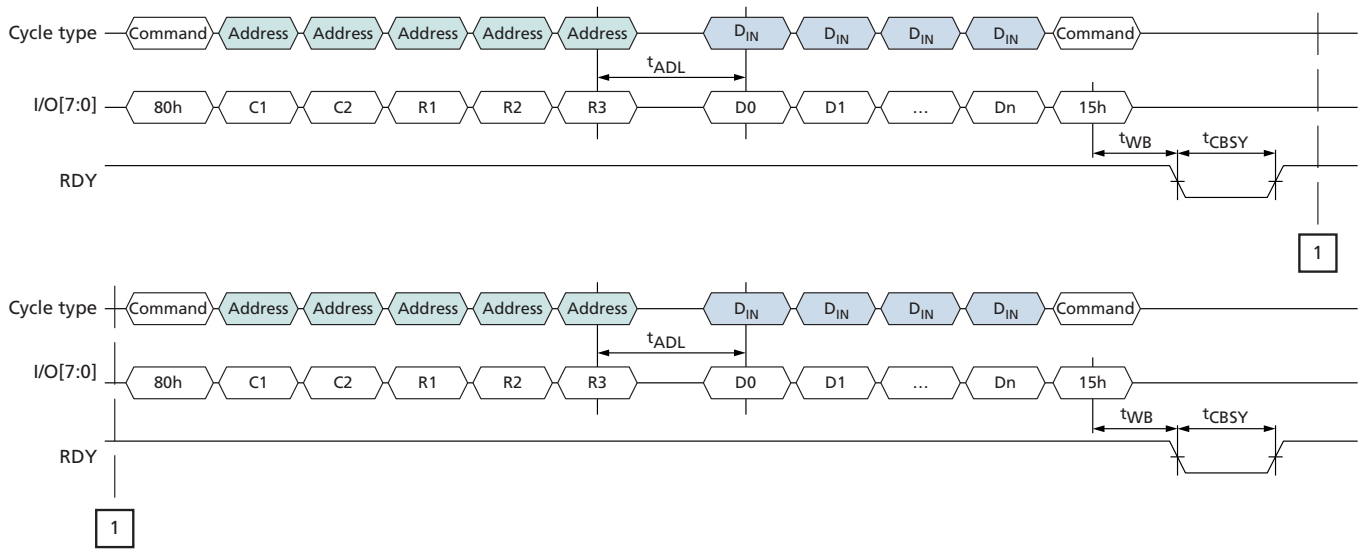
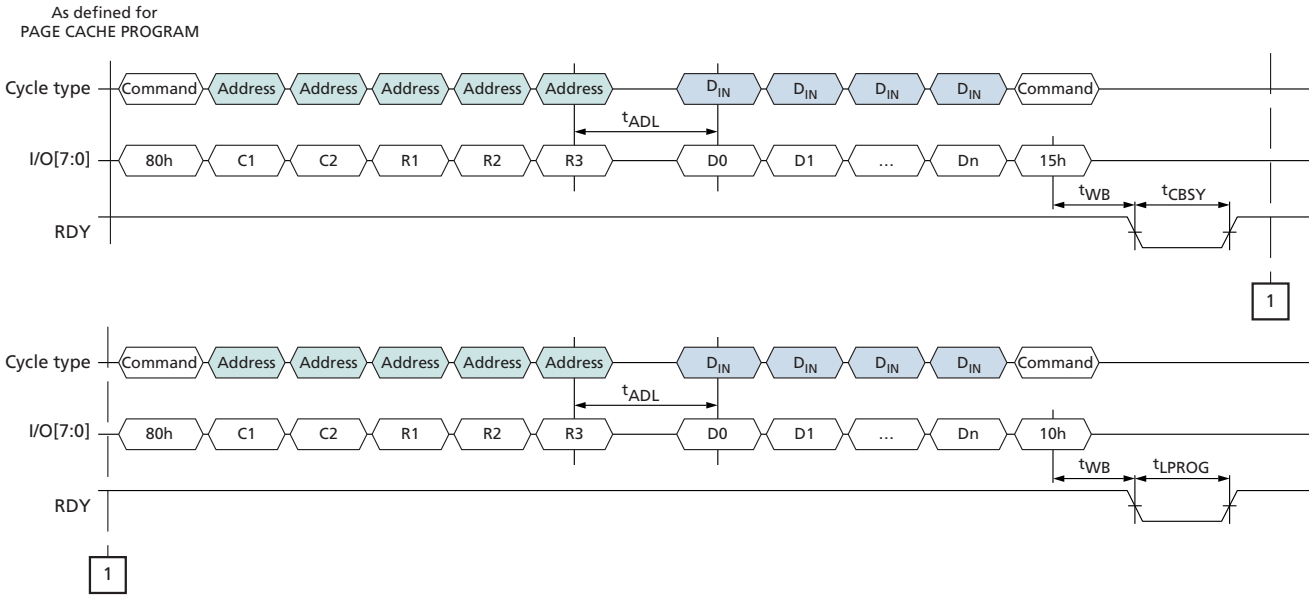


Figure 35: PROGRAM PAGE CACHE (80h–15h) Operation (End)



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Erase Operations

Erase operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command, erases one block in the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

ERASE BLOCK (60h-D0h)

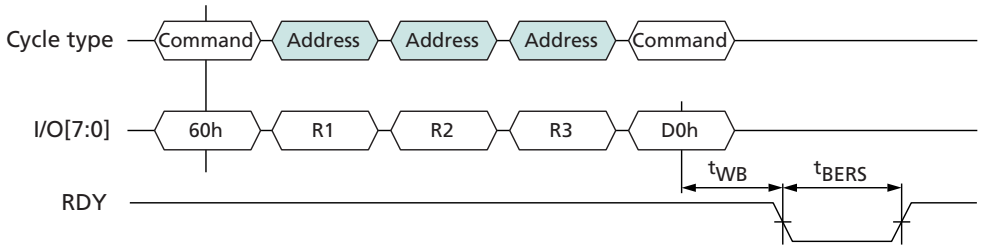
The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}BERS while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the die (LUN) is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

Figure 36: ERASE BLOCK (60h-D0h) Operation



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Internal Data Move Operations

Internal data move operations make it possible to transfer data within a device from one page to another, on the same plane, using the cache register. This is particularly useful for block management and wear leveling.

It is not possible to use the READ FOR INTERNAL DATA MOVE operation to move data from one die (LUN) to another. Instead, use a READ PAGE (00h-30h) or READ FOR INTERNAL DATA MOVE (00h-35h) command to read the data out of the NAND, and then use a PROGRAM PAGE (80h-10h) command with data input to program the data to a new die (LUN).

Between the READ FOR INTERNAL DATA MOVE (00h-35h) and PROGRAM FOR INTERNAL DATA MOVE (85h-10h) commands, the following commands are supported: status operations (70h, 78h) and column address operations (05h-E0h, 06h-E0h, 85h). The RESET operation (FFh) can be issued after READ FOR INTERNAL DATA MOVE (00h-35h), but the contents of the cache registers on the target are not valid.

In devices that have more than one die (LUN) per target, once the READ FOR INTERNAL DATA MOVE (00h-35h) is issued, interleaved die (multi-LUN) operations are prohibited until after the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command is issued.

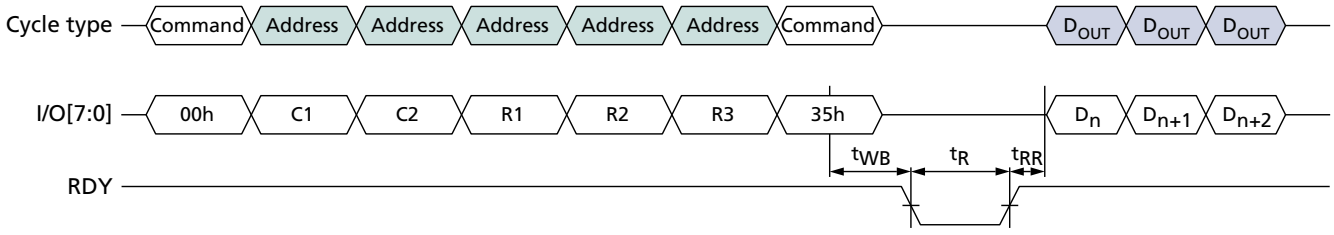
READ FOR INTERNAL DATA MOVE (00h-35h)

The READ FOR INTERNAL DATA MOVE (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command to prevent the propagation of data errors.

If internal ECC is enabled, the data does not need to be toggled out by the host to be corrected and moving data can then be written to a new page without data reloading, which improves system performance.

Figure 37: READ FOR INTERNAL DATA MOVE (00h-35h) Operation



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Figure 38: READ FOR INTERNAL DATA MOVE (00h–35h) with RANDOM DATA READ (05h–E0h)

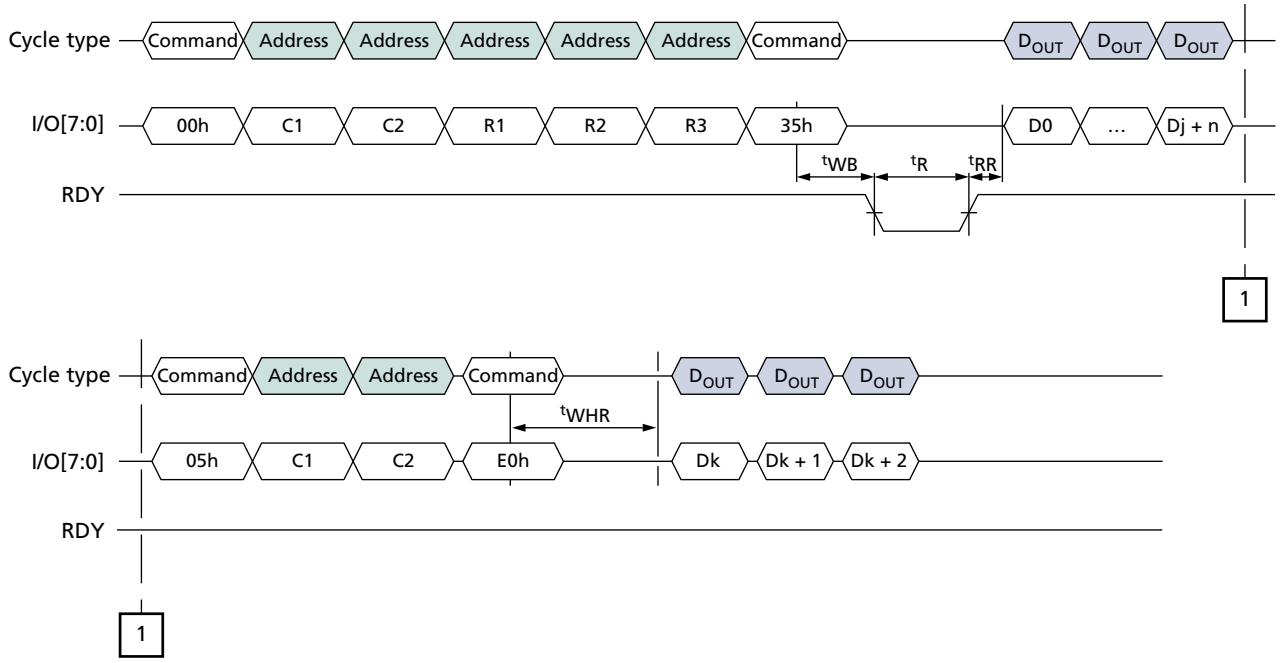


Figure 39: INTERNAL DATA MOVE (85h-10h) with Internal ECC Enabled

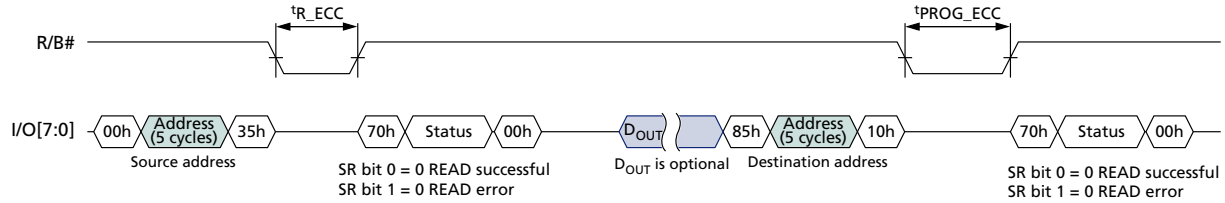
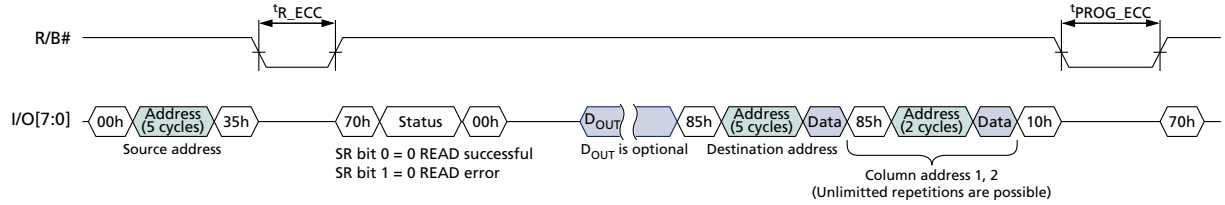


Figure 40: INTERNAL DATA MOVE (85h-10h) with RANDOM DATA INPUT with Internal ECC Enabled



PROGRAM FOR INTERNAL DATA MOVE (85h–10h)

The PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared.

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Figure 41: PROGRAM FOR INTERNAL DATA MOVE (85h–10h) Operation

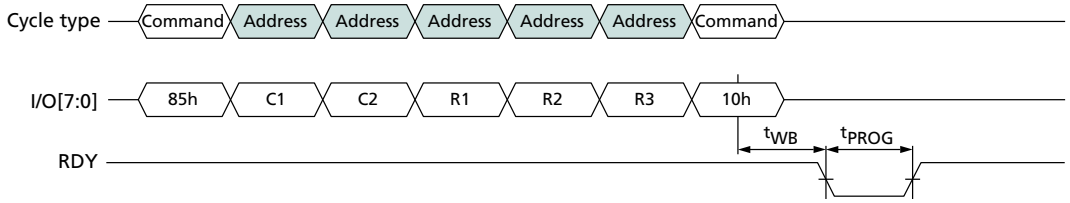
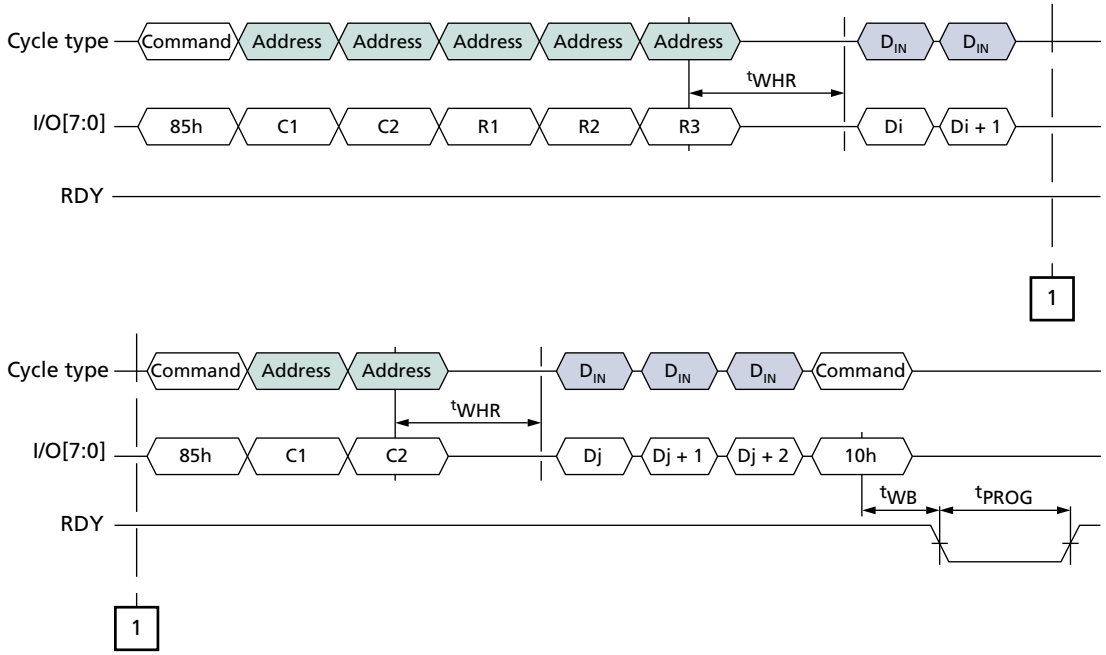


Figure 42: PROGRAM FOR INTERNAL DATA MOVE (85h-10h) with RANDOM DATA INPUT (85h)



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Block Lock Feature

The block lock feature protects either the entire device or ranges of blocks from being programmed and erased. Using the block lock feature is preferable to using WP# to prevent PROGRAM and ERASE operations.

Block lock is enabled and disabled at power-on through the LOCK pin. At power-on, if LOCK is LOW, all BLOCK LOCK commands are disabled. However if LOCK is HIGH at power-on, the BLOCK LOCK commands are enabled and, by default, all the blocks on the device are protected, or locked, from PROGRAM and ERASE operations, even if WP# is HIGH.

Before the contents of the device can be modified, the device must first be unlocked. Either a range of blocks or the entire device may be unlocked. PROGRAM and ERASE operations complete successfully only in the block ranges that have been unlocked. Blocks, once unlocked, can be locked again to protect them from further PROGRAM and ERASE operations.

Blocks that are locked can be protected further, or locked tight. When locked tight, the device's blocks can no longer be locked or unlocked.

WP# and Block Lock

The following is true when the block lock feature is enabled:

- Holding WP# LOW locks all blocks, provided the blocks are not locked tight.
- If WP# is held LOW to lock blocks, then returned to HIGH, a new UNLOCK command must be issued to unlock blocks.

UNLOCK (23h-24h)

By default at power-on, if LOCK is HIGH, all the blocks are locked and protected from PROGRAM and ERASE operations. The UNLOCK (23h) command is used to unlock a range of blocks. Unlocked blocks have no protection and can be programmed or erased.

The UNLOCK command uses two registers, a lower boundary block address register and an upper boundary block address register, and the invert area bit to determine what range of blocks are unlocked. When the invert area bit = 0, the range of blocks within the lower and upper boundary address registers are unlocked. When the invert area bit = 1, the range of blocks outside the boundaries of the lower and upper boundary address registers are unlocked. The lower boundary block address must be less than the upper boundary block address. The figures below show examples of how the lower and upper boundary address registers work with the invert area bit.

To unlock a range of blocks, issue the UNLOCK (23h) command followed by the appropriate address cycles that indicate the lower boundary block address. Then issue the 24h command followed by the appropriate address cycles that indicate the upper boundary block address. The least significant page address bit, PA0, should be set to 1 if setting the invert area bit; otherwise, it should be 0. The other page address bits should be 0.

Only one range of blocks can be specified in the lower and upper boundary block address registers. If after unlocking a range of blocks the UNLOCK command is again issued, the new block address range determines which blocks are unlocked. The previous unlocked block address range is not retained.

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Figure 43: Flash Array Protected: Invert Area Bit = 0

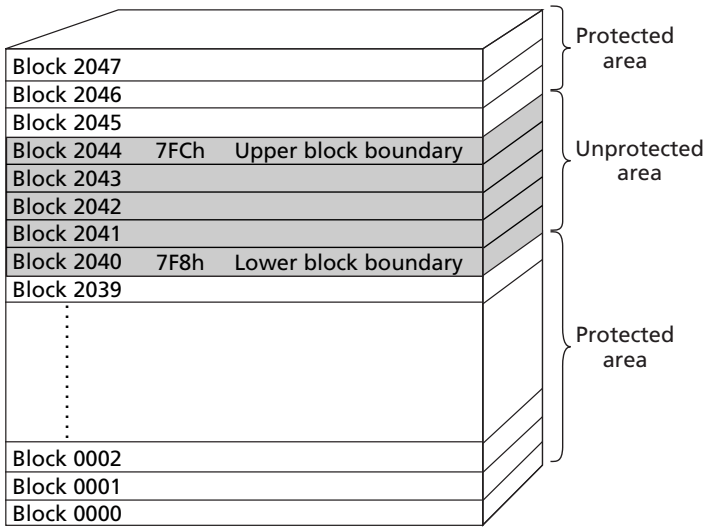


Figure 44: Flash Array Protected: Invert Area Bit = 1

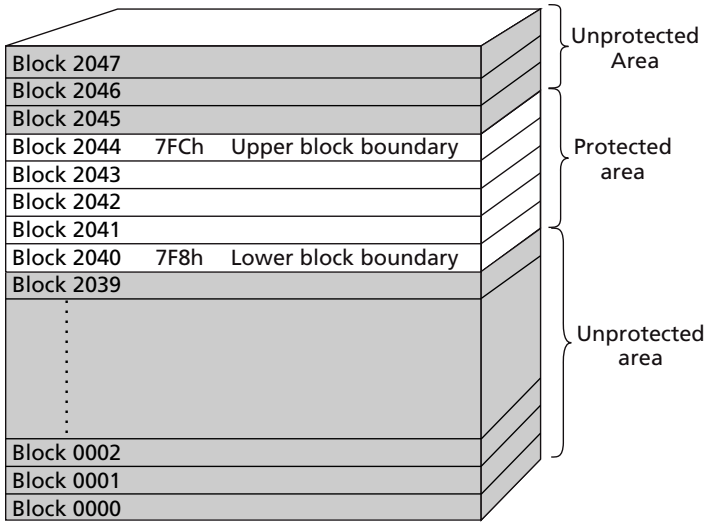


Table 15: Block Lock Address Cycle Assignments

ALE Cycle	I/O[15:8][1]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	BA7	BA6	LOW	LOW	LOW	LOW	LOW	Invert area bit[2]
Second	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Third	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

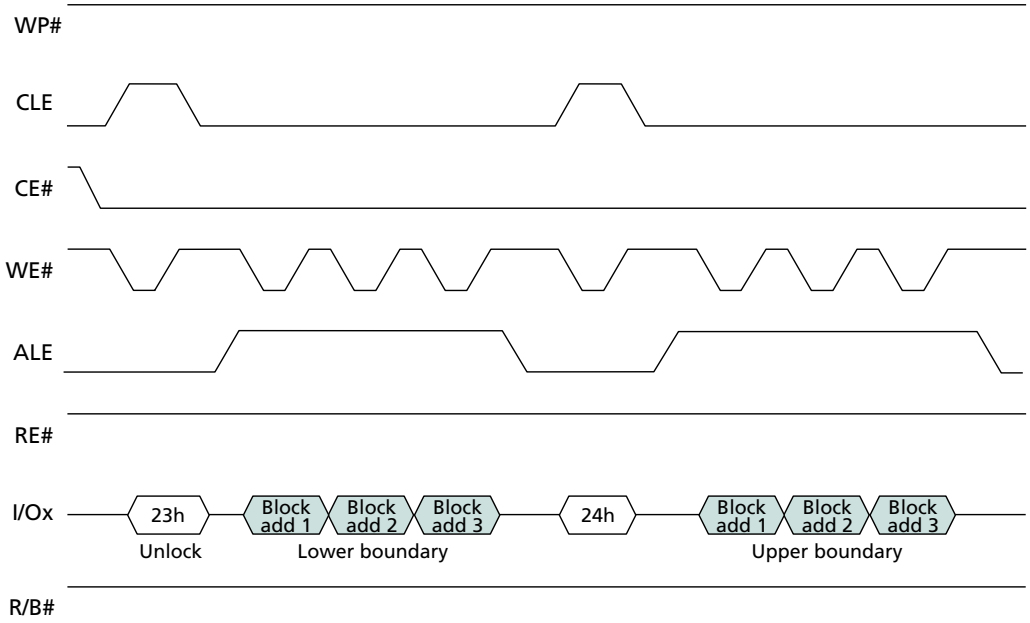
Notes:
1. I/O[15:8] is applicable only for x16 devices.
2. Invert area bit is applicable for 24h command; it may be LOW or HIGH for 23h command.

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Figure 45: UNLOCK Operation



LOCK (2Ah)

By default at power-on, if LOCK is HIGH, all the blocks are locked and protected from PROGRAM and ERASE operations. If portions of the device are unlocked using the UNLOCK (23h) command, they can be locked again using the LOCK (2Ah) command. The LOCK command locks all of the blocks in the device. Locked blocks are write-protected from PROGRAM and ERASE operations.

To lock all of the blocks in the device, issue the LOCK (2Ah) command.

When a PROGRAM or ERASE operation is issued to a locked block, R/B# goes LOW for ^{t}LBSY. The PROGRAM or ERASE operation does not complete. Any READ STATUS command reports bit 7 as 0, indicating that the block is protected.

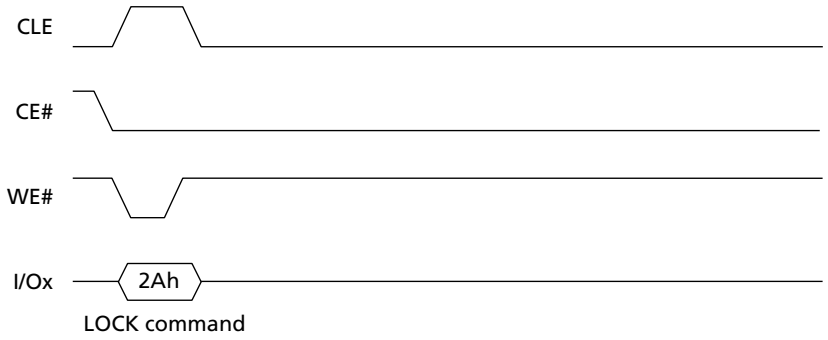
The LOCK (2Ah) command is disabled if LOCK is LOW at power-on or if the device is locked tight.

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Figure 46: LOCK Operation



LOCK TIGHT (2Ch)

The LOCK TIGHT (2Ch) command prevents locked blocks from being unlocked and also prevents unlocked blocks from being locked. When this command is issued, the UNLOCK (23h) and LOCK (2Ah) commands are disabled. This provides an additional level of protection against inadvertent PROGRAM and ERASE operations to locked blocks.

To implement LOCK TIGHT in all of the locked blocks in the device, verify that WP# is HIGH and then issue the LOCK TIGHT (2Ch) command.

When a PROGRAM or ERASE operation is issued to a locked block that has also been locked tight, R/B# goes LOW for ^{t}LBSY. The PROGRAM or ERASE operation does not complete. The READ STATUS (70h) command reports bit 7 as 0, indicating that the block is protected. PROGRAM and ERASE operations complete successfully to blocks that were not locked at the time the LOCK TIGHT command was issued.

After the LOCK TIGHT command is issued, the command cannot be disabled via a software command. Lock tight status can be disabled only by power cycling the device or toggling WP#. When the lock tight status is disabled, all of the blocks become locked, the same as if the LOCK (2Ah) command had been issued.

The LOCK TIGHT (2Ch) command is disabled if LOCK is LOW at power-on.

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Figure 47: LOCK TIGHT Operation

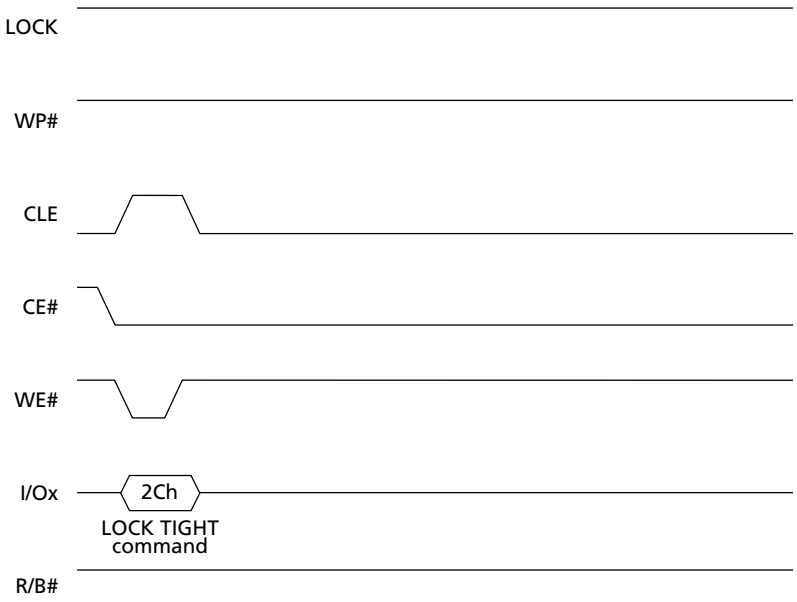
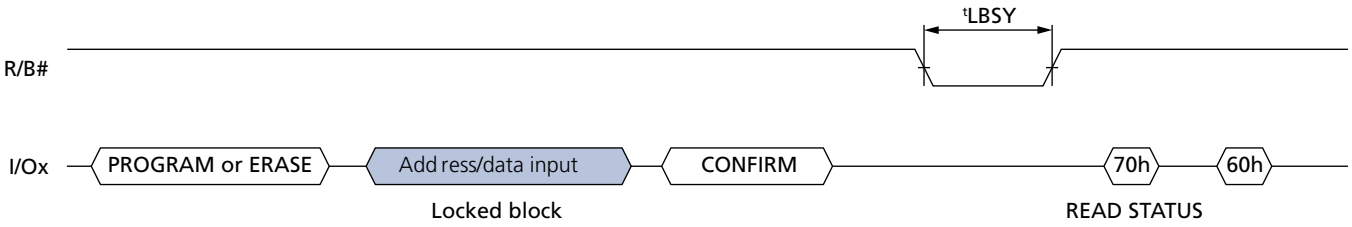


Figure 48: PROGRAM/ERASE Issued to Locked Block



BLOCK LOCK READ STATUS (7Ah)

The BLOCK LOCK READ STATUS (7Ah) command is used to determine the protection status of individual blocks. The address cycles have the same format, as shown below, and the invert area bit should be set LOW. On the falling edge of RE# the I/O pins output the block lock status register, which contains the information on the protection status of the block.

Table 16: Block Lock Status Register Bit Definitions

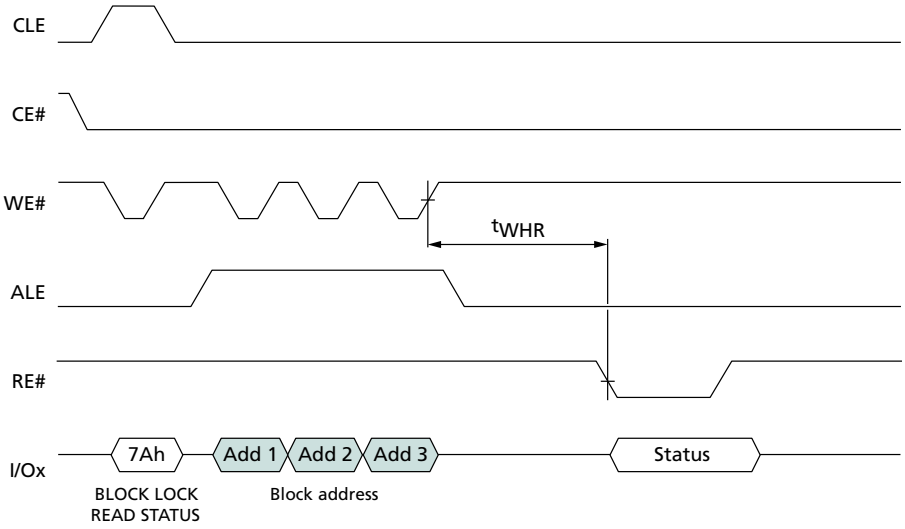
Block Lock Status Register Definitions	I/O[7:4]	I/O3 (Protect#)	I/O2 (Lock#)	I/O1 (LT#)	I/O0 (LT)
Block is locked tight	X	1	0	0	1
Block is locked	X	1	0	1	0
Block is unlocked, and device is locked tight	X	1	1	0	1
Block is unlocked, and device is not locked tight	X	1	1	1	0
Block is permanently protected	X	0	x	x	x

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Figure 49: BLOCK LOCK READ STATUS

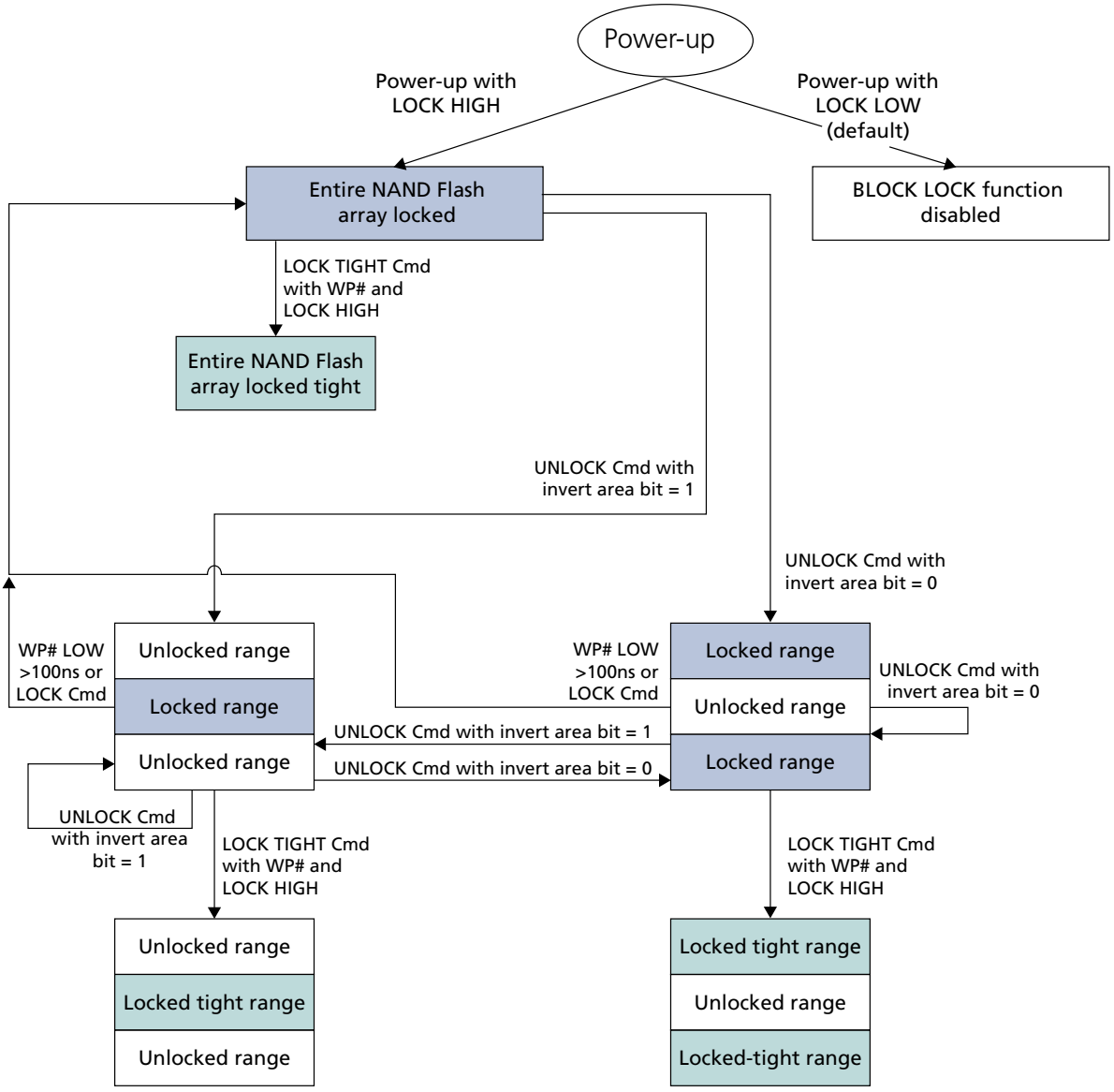


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Figure 50: BLOCK LOCK Flowchart



PROTECT Command

Blocks 00h–07h are guaranteed valid with ECC when shipped from the factory. The PROTECT command provides nonvolatile, irreversible protection of up to twelve groups (48 blocks total). Implementation of the protection is group-based, which means that a minimum of one group (4 blocks) is protected when the PROTECT command is issued.

Because block protection is nonvolatile, a power-on or power-off sequence does not affect the block status after the PROTECT command is issued. The device ships from the factory with no blocks protected so that users can program or erase the blocks before issuing the PROTECT command. Block protection is also irreversible in that when pro-

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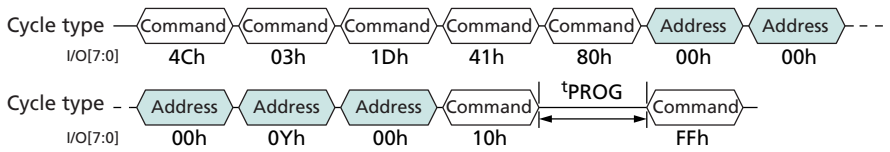
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tection is enabled by the issuing PROTECT command, the protected blocks can no longer be programmed or erased.

The PROTECT command includes the steps detailed below.

Figure 51: Address and Command Cycles



Note: 1. In the 4th address cycle, 0YH is the last 4 bits and represents the group of blocks to be protected. There are always 12 Groups, so Y = 0000b-1011b: Y = 0000 protects Group0 = blks 0, 1, 2, 3; Y = 0001 protects Group1 = blks 4, 5, 6, 7; Y = 1011 protects Group11 = blks 44, 45, 46, 47.

Protection Command Details

To enable protection, four bus WRITE cycles set up the 4Ch, 03h, 1Dh, and 41h commands. Next, one bus WRITE cycle sets up the PAGE PROGRAM command (80h).

Then, five bus WRITE cycles are required to input the targeted block group information: 00h, 00h, 00h, 0Yh, 00h. In this 4th address cycle, 0YH is the last 4 bits and represents the group of blocks to be protected. There are always 12 Groups, so Y = 0000b-1011b:

- Y = 0000 protects Group0 = blks 0, 1, 2, 3.
- Y = 0001 protects Group1 = blks 4, 5, 6, 7.
- Y = 1011 protects Group11 = blks 44, 45, 46, 47.

One bus cycle is required to issue the PAGE PROGRAM CONFIRM command. After ^{t}PROG, the targeted block groups are protected. The EXIT protection command (FFh) is issued to ensure the device exits protection mode.

(4Ch-03h-1Dh-41h)-80h-addr(00h-00h-00h-0Yh-00h)-10h-^{t}PROG-FFh

The enable protection step is four bytes wide to prevent implementing involuntary protection. In addition, any spurious command/address/data cycles between each byte invalidates the entire process and the next PROGRAM command does not affect the block protection status. Likewise, any spurious command/address/data cycle between enable protection and setting up the PAGE PROGRAM command invalidates the entire protection command process.

If enable protection is followed by an operation other than the PROGRAM operation, such as a PAGE READ or BLOCK ERASE operation, this other operation is executed without affecting block protection status. Therefore, the PROTECT operation must still be executed to protect the block. The PROTECT operation is inhibited if WP# is LOW. Upon PROTECT operation failure, the status register reports a value of E1h. Upon PROTECT operation success, the status register reports value of E0h.

The following is an example of boot block protection:

Protect group 5 (blks20-23): (4Ch-03h-1Dh-41h)-80h-addr(00h-00h-00h-05h-00h)-10h-^{t}PROG-FFh

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Permanent Block Lock Disable Mode

The PROTECT command provides nonvolatile, irreversible protection of up to twelve groups (48 blocks total), these blocks are permanent locked once the PROTECT command is issued to them. The permanent block lock disable mode provides the command sequence to freeze the block lock status, it is highly recommended for customers to follow this operation to prevent unintentional or malicious changes but not limited to these scenarios:

- Only certain number of groups of blocks need to be permanently locked, the rest of the block groups do not need to be permanently locked
- Customer do not need permanent block lock feature, and all 48 blocks are normal blocks

In permanent block lock disable mode, the following program sequence is used to disable protection command to add more permanent locked block groups:

- SET FEATURE command (EFh) with feature address 90h and data value 10h-00h-00h-00h to enter permanent block lock disable mode
- PROGRAM command (80h-10h) with block/page address all "0", and data input 0x00
- READ STATUS command 70h to check the operation status and success

READ command also could be used in permanent block lock disable mode to check whether PROTECT command is disabled by reading out all "0"; all "1" indicates Protection command is not disabled.

If permanent block lock disable sequence is issued again to the part that has already been disabled, the part will be busy for ^{t}OBSY and exit with SR = 60h. The part will be busy for ^{t}OBSY_ECC when ECC is enabled.

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One-Time Programmable (OTP) Operations

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. 48 full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Customers can use the OTP area any way they choose; typical uses include programming serial numbers or other data for permanent storage.

The OTP area leaves the factory in an unwritten state (all bits are 1s). Programming or partial-page programming enables the user to program only 0 bits in the OTP area. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

Micron provides a unique way to program and verify data before permanently protecting it and preventing future changes. The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the SET FEATURE (EFh) command to feature address 90h and write 01h to P1, followed by three cycles of 00h to P2-P4. For parameters to enter OTP mode, see Features Operations.

When the device is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area. The OTP area is assigned to page addresses 02h-31h. To program an OTP page, issue the PROGRAM PAGE (80h-10h) command. The pages must be programmed in the ascending order. Similarly, to read an OTP page, issue the PAGE READ (00h-30h) command.

Protecting the OTP is done by entering OTP protect mode. To set the device to OTP protect mode, issue the SET FEATURE (EFh) command to feature address 90h and write 03h to P1, followed by three cycles of 00h to P2-P4.

To determine whether the device is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command.

To exit OTP operation or protect mode, write 00h to P1 at feature address 90h.

Legacy OTP Commands

For legacy OTP commands, OTP DATA PROGRAM (A0h-10h), OTP DATA PROTECT (A5h-10h), and OTP DATA READ (AFh-30h).

OTP DATA PROGRAM (80h-10h)

The OTP DATA PROGRAM (80h-10h) command is used to write data to the pages within the OTP area. An OTP page allows only four partial-page programs. There is no ERASE operation for OTP pages.

PROGRAM PAGE enables programming into an offset of an OTP page using two bytes of the column address (CA[12:0]). The command is compatible with the RANDOM DATA INPUT (85h) command. The PROGRAM PAGE command will not execute if the OTP area has been protected.

To use the PROGRAM PAGE command, issue the 80h command. Issue *n* address cycles. The first two address cycles are the column address. For the remaining cycles, select a page in the range of 02h-00h through 31h-00h. Next, write *n* bytes of data. After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification.

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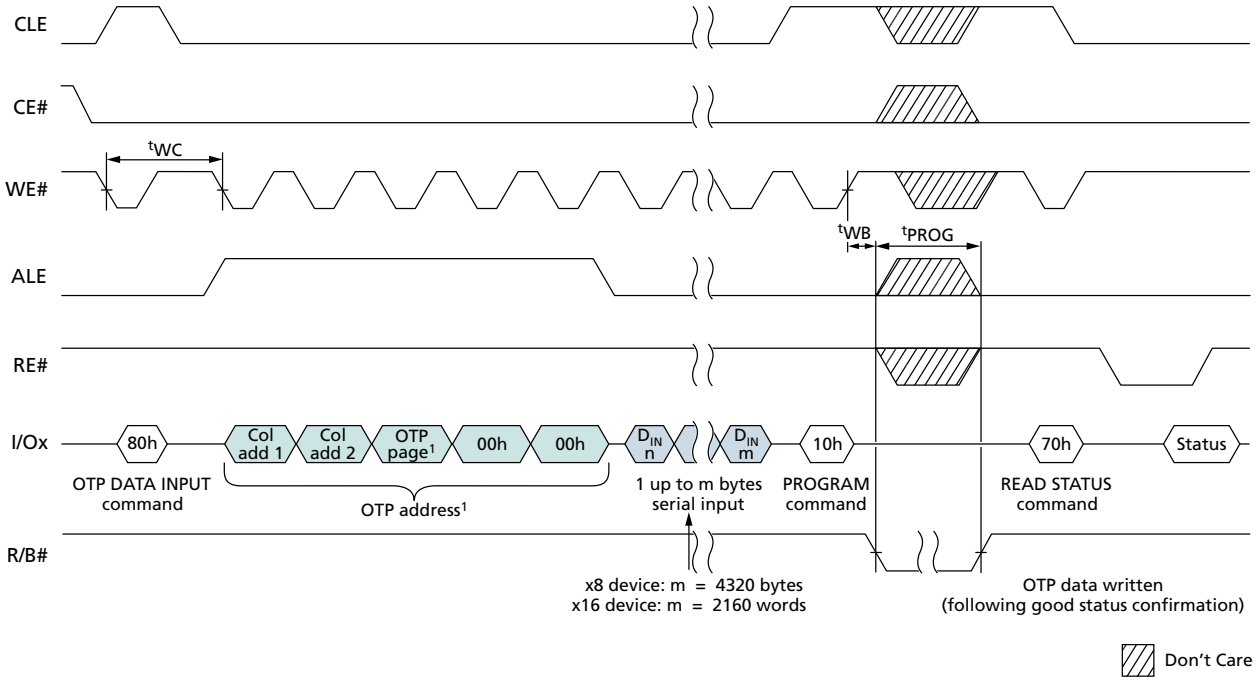
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R/B# goes LOW for the duration of the array programming time (tPROG). The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B#. When the device is ready, read bit 0 of the status register to determine whether the operation passed or failed (see Status Operations). Each OTP page can be programmed to 4 partial-page programming.

RANDOM DATA INPUT (85h)

After the initial OTP data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to the OTP PAGE WRITE (10h) command being issued.

Figure 52: OTP DATA PROGRAM (After Entering OTP Operation Mode)



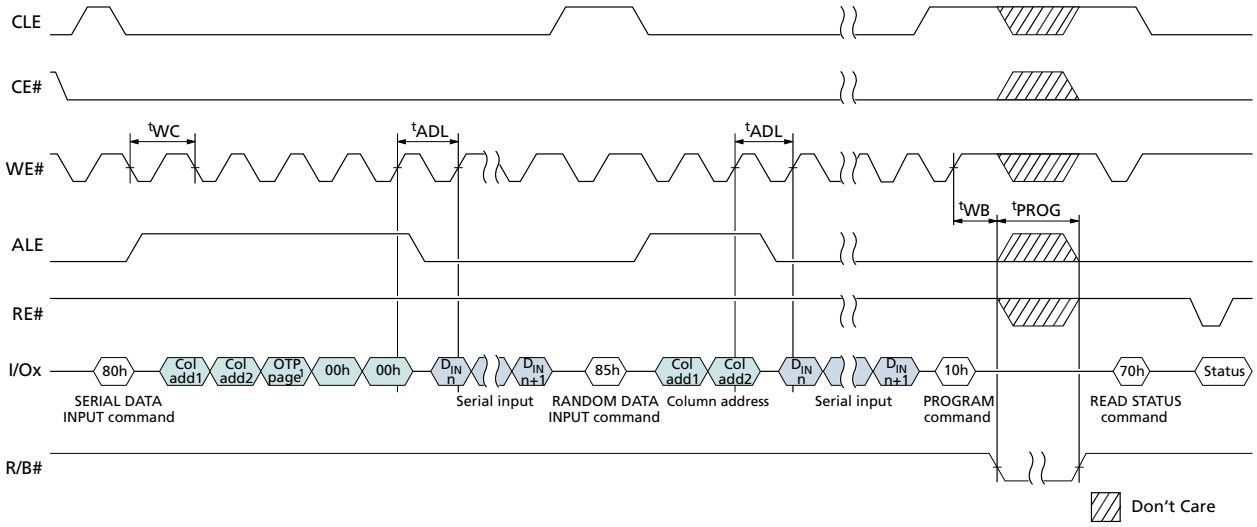
Note: 1. The OTP page must be within the 02h–31h range.

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Figure 53: OTP DATA PROGRAM Operation with RANDOM DATA INPUT (After Entering OTP Operation Mode)



OTP DATA PROTECT (80h-10)

The OTP area is protected on a block basis. To protect a block, set the device to OTP protect mode, then issue the PROGRAM PAGE (80h-10h) command and write OTP address 00h, 00h, 00h, 00h. To set the device to OTP protect mode, issue the SET FEATURE (EFh) command to 90h (feature address) and write 03h to P1, followed by three cycles of 00h to P2-P4.

After the data is protected, it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

To use the PROGRAM PAGE command to protect the OTP area, issue the 80h command, followed by *n* address cycles, write 00h data, data cycle of 00h, followed by the 10h command. (An example of the address sequence is shown in the following figure.) If an OTP DATA PROGRAM command is issued after the OTP area has been protected, R/B# will go LOW for tOBSY.

The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B#.

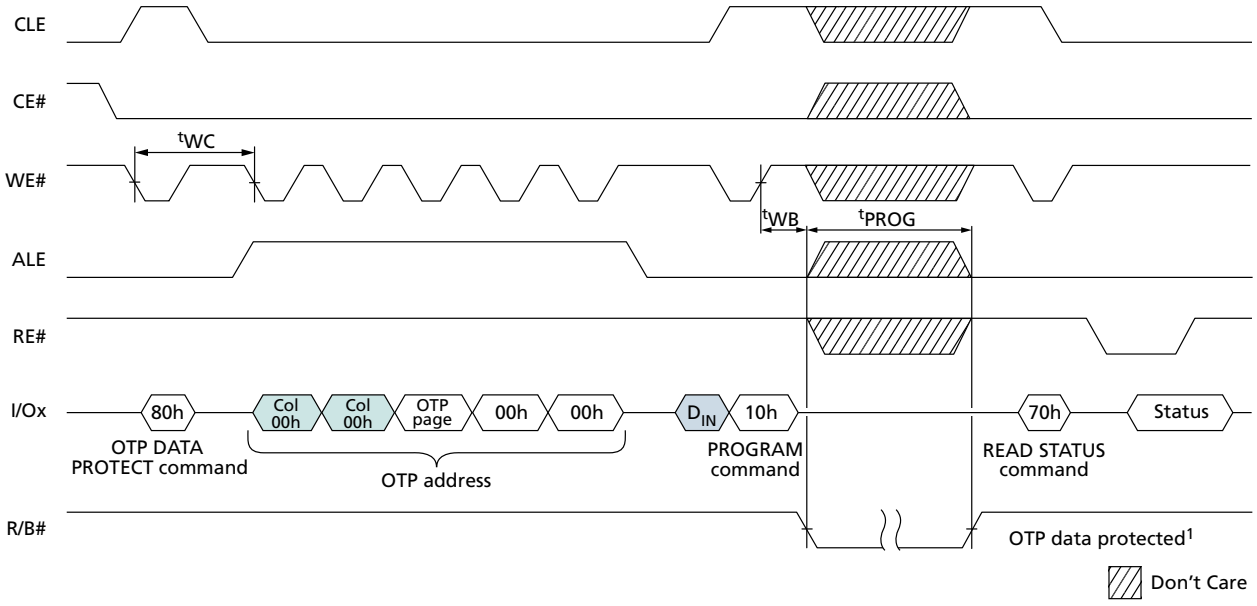
When the device is ready, read bit 0 of the status register to determine whether the operation passed or failed (see Status Operations).

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Figure 54: OTP DATA PROTECT Operation (After Entering OTP Protect Mode)



Note: 1. OTP data is protected following a good status confirmation.

OTP DATA READ (00h-30h)

To read data from the OTP area, set the device to OTP operation mode, then issue the PAGE READ (00h-30h) command. Data can be read from OTP pages within the OTP area whether the area is protected or not.

To use the PAGE READ command for reading data from the OTP area, issue the 00h command, and then issue five address cycles: for the first two cycles, the column address; and for the remaining address cycles, select a page in the range of 02h-00h-00h through 31h-00h-00h. Lastly, issue the 30h command. The PAGE READ CACHE MODE command is not supported on OTP pages.

R/B# goes LOW (^{t}R) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B# (see Status Operations).

Normal READ operation timings apply to OTP read accesses. Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

The PAGE READ command is compatible with the RANDOM DATA OUTPUT (05h-E0h) command.

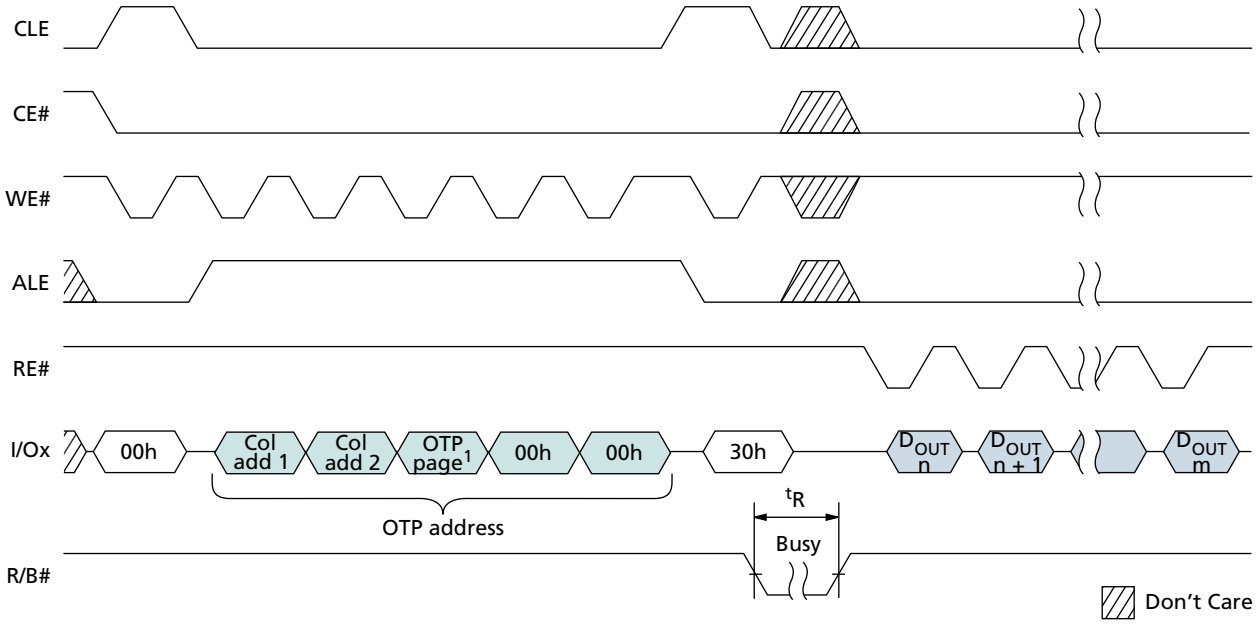
Only data on the current page can be read. Pulsing RE# outputs data sequentially.

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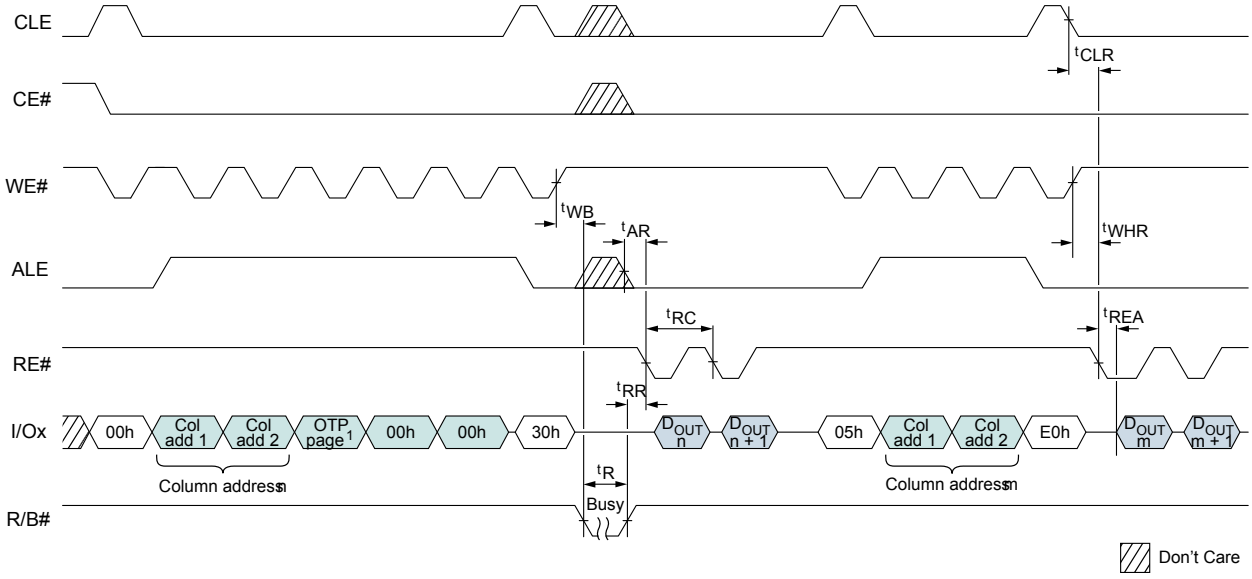
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Figure 55: OTP DATA READ



Note: 1. The OTP page must be within the 02h–31h range.

Figure 56: OTP DATA READ with RANDOM DATA READ Operation



Note: 1. The OTP page must be within the range 02h–31h.

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ECC Protection

Internal ECC enables 9-bit detection and 8-bit correction in 512 bytes (x8) of main area and 16 bytes (x8) of spare area or 256 words (x16) of the main area and 8 words (x16) of spare area. During the busy time for PROGRAM operations, internal ECC generates parity bits when error detection is complete. During READ operations the device executes the internal ECC engine (9-bit detection and 8-bit error correction). When the READ operation is complete, read status bit 0 must be checked to determine whether errors larger than eight bits have occurred.

Following the READ STATUS command, the device must be returned to read mode by issuing the 00h command.

Limitations of internal ECC include the spare area, defined in the Spare Area Mapping (x8) and (x16) tables, and ECC parity areas that cannot be written to. Each ECC user area (referred to main and spare) must be written within one partial-page program so that the NAND device can calculate the proper ECC parity. The number of partial-page programs within a page cannot exceed four.

During a PROGRAM operation, the device calculates an ECC code on the 4K page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a 1- to 8-bit error is detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether the error correction was successful. The Spare Area Mapping (x8) and (x16) tables that follow show the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:

- Spare area definitions provided in the Spare Area Mapping table below.
- WRITEs to ECC are supported for main and spare areas 0 and 1. WRITEs to the ECC area are prohibited (see the Spare Area Mapping table below).
- When using partial-page programming, the following conditions must both be met: First, in the main user area and in user meta data area, single partial-page programming operations must be used (see the Spare Area Mapping table below). Second, within a page, the user can perform a maximum of four partial-page programming operations.

Table 17: Spare Area Mapping (×8)

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
User Data				
1FFh	000h	Yes	Main 0	User data 0
3FFh	200h	Yes	Main 1	User data 1
5FFh	400h	Yes	Main 2	User data 2
7FFh	600h	Yes	Main 3	User data 3
9FFh	800h	Yes	Main 4	User data 4
BFFh	A00h	Yes	Main 5	User data 5

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Table 17: Spare Area Mapping (×8) (Continued)

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
DFFh	C00h	Yes	Main 6	User data 6
FFFh	E00h	Yes	Main 7	User data 7
User Meta Data				
100Fh	1000h	Yes	Spare 0	User meta data
101Fh	1010h	Yes	Spare 1	User meta data
102Fh	1020h	Yes	Spare 2	User meta data
103Fh	1030h	Yes	Spare 3	User meta data
104Fh	1040h	Yes	Spare 4	User meta data
105Fh	1050h	Yes	Spare 5	User meta data
106Fh	1060h	Yes	Spare 6	User meta data
107Fh	1070h	Yes	Spare 7	User meta data
ECC				
108Fh	1080h	Yes	Spare 0	ECC for main/spare 0
109Fh	1090h	Yes	Spare 1	ECC for main/spare 1
10AFh	10A0h	Yes	Spare 2	ECC for main/spare 2
10BFh	10B0h	Yes	Spare 3	ECC for main/spare 3
10CFh	10C0h	Yes	Spare 4	ECC for main/spare 4
10DFh	10D0h	Yes	Spare 5	ECC for main/spare 5
10EFh	10E0h	Yes	Spare 6	ECC for main/spare 6
10FFh	10F0h	Yes	Spare 7	ECC for main/spare 7

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Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad block mark. However, the first spare area location in each bad block is guaranteed to contain the bad block mark. This method is compliant with ONFI Factory Defect Mapping requirements.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation
- Under typical conditions, use the minimum required ECC (see table below)
- Use bad block management and wear-leveling algorithms

Table 18: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	2008
Total available blocks per LUN	2048
First spare area location	×8: byte 4096 ×16: word 2048
Bad block mark	×8: 00h ×16: 0000h
Minimum required ECC	8-bit ECC per 544 bytes of data
Minimum ECC with internal ECC enabled	8-bit ECC per 528 bytes (user data) + 16 bytes (parity data)

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Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 19: Absolute Maximum Ratings

Parameter/Condition		Symbol	Min	Max	Unit
Voltage input	1.8V	V_{IN}	–0.6	+2.4	V
V_{CC} supply voltage	1.8V	V_{CC}	–0.6	+2.4	V
Storage temperature		T_{STG}	–65	+150	°C
Electrostatic discharge voltage		V_{ESD}	–2000	2000	V

Note: 1. All specified voltages are with respect to V_{SS}.

Table 20: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
V_{CC} supply voltage	1.8V	V_{CC}	1.7	1.8	1.95	V
Ground supply voltage		V_{SS}	0	0	0	V
Operating temperature	Extended	T_A	–40	–	+85	°C

Note: 1. All specified voltages are with respect to V_{SS}.

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Table 21: Capacitance

Description	Symbol	Max	Unit	Notes
Input/output capacitance (I/O)	C_{IO}	8	pF	1, 2
Input capacitance	C_{IN}	6	pF	1, 2

Notes:
1. These parameters will be verified in device characterization.
2. Test conditions: T_C = 25°C; f = 1 MHz; Vin = 0V.

Table 22: Test Conditions

Parameter	Value	Notes
Input pulse levels	0.0V to V_{CC}	
Input rise and fall times	5ns	
Input and output timing levels	$V_{CC}/2$	
Output load	1 TTL GATE and CL = 30pF (1.8V)	1

Note:
1. These parameters will be verify in device characterization.

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Electrical Specifications – DC Characteristics and Operating Conditions

Table 23: DC Characteristics and Operating Conditions (1.8V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential read current ECC off	$^{t}RC = {}^{t}RC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1}	–	13	20	mA	1, 2
Sequential read current ECC on	$^{t}RC = {}^{t}RC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	–	–	25	35	mA	1, 2
Program current ECC off	–	I_{CC2}	–	13	20	mA	1, 2
Program current ECC on	–	I_{CC2}	–	20	25	mA	1, 2
Erase current	–	I_{CC3}	–	15	20	mA	1, 2
Standby current (TTL)	CE# = V_{IH}; LOCK = WP# = 0V/V_{CC}	I_{SB1}	–	–	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; LOCK = WP# = 0V/V_{CC}	I_{SB2}	–	15	50	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	–	–	10 per die	mA	3
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA	
Input high voltage	I/O[7:0], I/O[15:0], CE#, CLE, ALE, WE#, RE#, WP#, R/B#, LOCK	V_{IH}	0.8 × V_{CC}	–	V_{CC} + 0.3	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	0.2 × V_{CC}	V	
Output high voltage	I_{OH} = –100µA	V_{OH}	V_{CC} - 0.2	–	–	V	4
Output low voltage	I_{OL} = 100µA	V_{OL}	–	–	0.2	V	4
Output low current	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	–	mA	5

Notes:
1. Typical and maximum values are for single-plane operation only.
2. Values are for single die operations. Values could be higher for interleaved die operations.
3. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches $V_{CC,min}$.
4. Test conditions for V_{OH} and V_{OL}.
5. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full.

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Electrical Specifications – AC Characteristics and Operating Conditions

Table 24: AC Characteristics: Command, Data, and Address Input

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	^{t}ADL	100	–	ns	1
ALE hold time	^{t}ALH	5	–	ns	
ALE setup time	^{t}ALS	10	–	ns	
CE# hold time	^{t}CH	5	–	ns	
CLE hold time	^{t}CLH	5	–	ns	
CLE setup time	^{t}CLS	10	–	ns	
CE# setup time	^{t}CS	25	–	ns	
Data hold time	^{t}DH	5	–	ns	
Data setup time	^{t}DS	10	–	ns	
WRITE cycle time	^{t}WC	30	–	ns	1
WE# pulse width HIGH	^{t}WH	10	–	ns	1
WE# pulse width	^{t}WP	15	–	ns	1
WP# transition to WE# LOW	^{t}WW	100	–	ns	

Note: 1. Timing for ^{t}ADL begins in the address cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.

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Table 25: AC Characteristics: Normal Operation

Note 1 applies to all

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	tAR	10	–	ns	
CE# access time	tCEA	–	30	ns	
CE# HIGH to output High-Z	tCHZ	–	50	ns	2
CLE to RE# delay	tCLR	10	–	ns	
CE# HIGH to output hold	tCOH	15	–	ns	
Output High-Z to RE# LOW	tIR	0	–	ns	
READ cycle time	tRC	30	–	ns	
RE# access time	tREA	–	25	ns	
RE# HIGH hold time	tREH	10	–	ns	
RE# HIGH to output hold	tRHOH	15	–	ns	
RE# HIGH to WE# LOW	tRHW	100	–	ns	2
RE# HIGH to output High-Z	tRHZ	–	65	ns	
RE# pulse width	tRP	15	–	ns	
Ready to RE# LOW	tRR	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	tRST	–	7/13/600	µs	3
WE# HIGH to busy	tWB	–	100	ns	4
WE# HIGH to RE# LOW	tWHR	80	–	ns	

Notes:
1. AC characteristics may need to be relaxed if I/O drive strength is not set to "full."
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100% tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will go busy for a maximum of 1ms. Thereafter, the device goes busy for a maximum of 5µs.
4. Do not issue a new command during tWB, even if R/B# is ready.

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Electrical Specifications – Program/Erase Characteristics

Table 26: Program/Erase Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial-page programs	NOP	–	4	cycles	1
BLOCK ERASE operation time	^{t}BERS	2	10	ms	
Busy time for PROGRAM CACHE operation	^{t}CBSY	3	600	µs	2
Cache read busy time ECC OFF	^{t}RCBSY	5	25	µs	
Cache read busy time ECC ON	^{t}RCBSY_ECC	90	170	µs	
Busy time for SET FEATURES and GET FEATURES operations	^{t}FEAT	–	1	µs	
LAST PAGE PROGRAM operation time	^{t}LPROG	–	–	–	3
Busy time for OTP DATA PROGRAM operation if OTP is protected (ECC disabled)	^{t}OBSY	–	30	µs	
Busy time for OTP DATA PROGRAM operation if OTP is protected (ECC enabled)	^{t}OBSY_ECC	–	90	µs	
Busy time for PROGRAM/ERASE on locked blocks	^{t}LBSY	–	3	µs	
PROGRAM PAGE ECC OFF operation time	^{t}PROG	200	600	µs	
PROGRAM PAGE ECC ON operation time	^{t}PROG_ECC	240	600	µs	
Power-on reset time	^{t}POR	–	1	ms	
READ PAGE operation time ECC OFF	^{t}R	–	25	µs	
READ PAGE operation time ECC ON	^{t}R_ECC	90	170	µs	

Notes:
1. Four total partial-page programs to the same page.
2. ^{t}CBSY (MAX) time depends on timing between internal program completion and data-in.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last - 1 page) - command load time (last page) - address load time (last page) - data load time (last page).

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Asynchronous Interface Timing Diagrams

Figure 57: RESET Operation

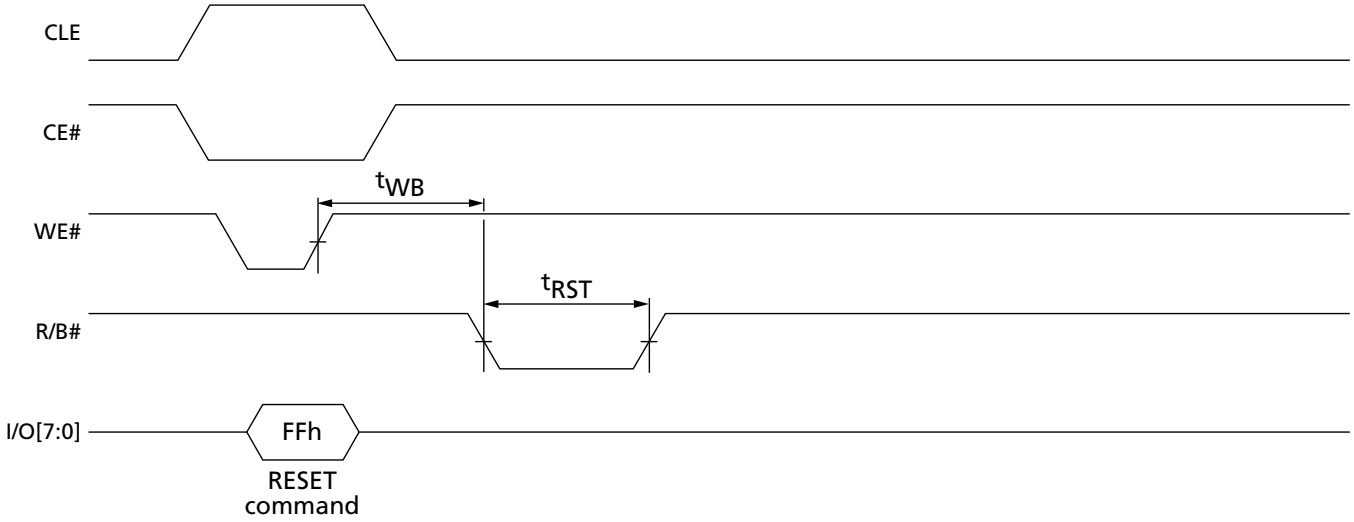
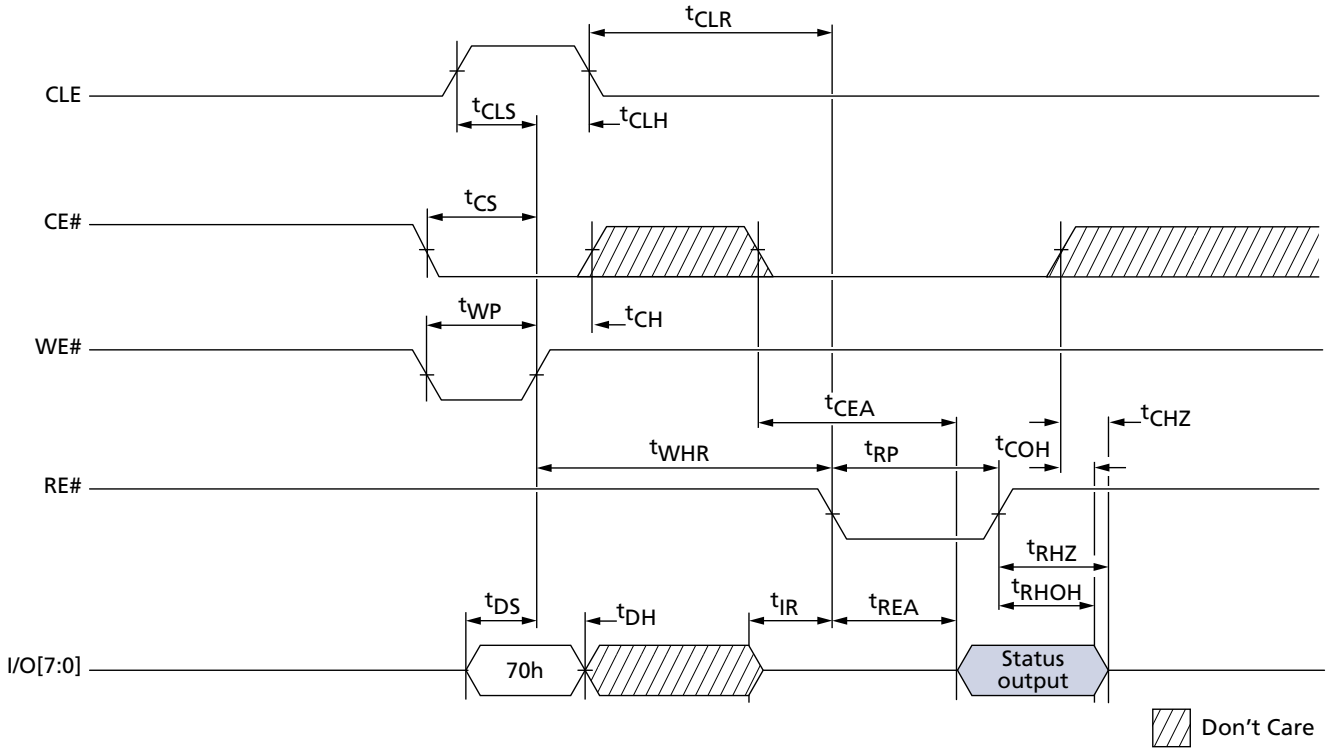


Figure 58: READ STATUS Cycle



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Figure 59: READ STATUS ENHANCED Cycle

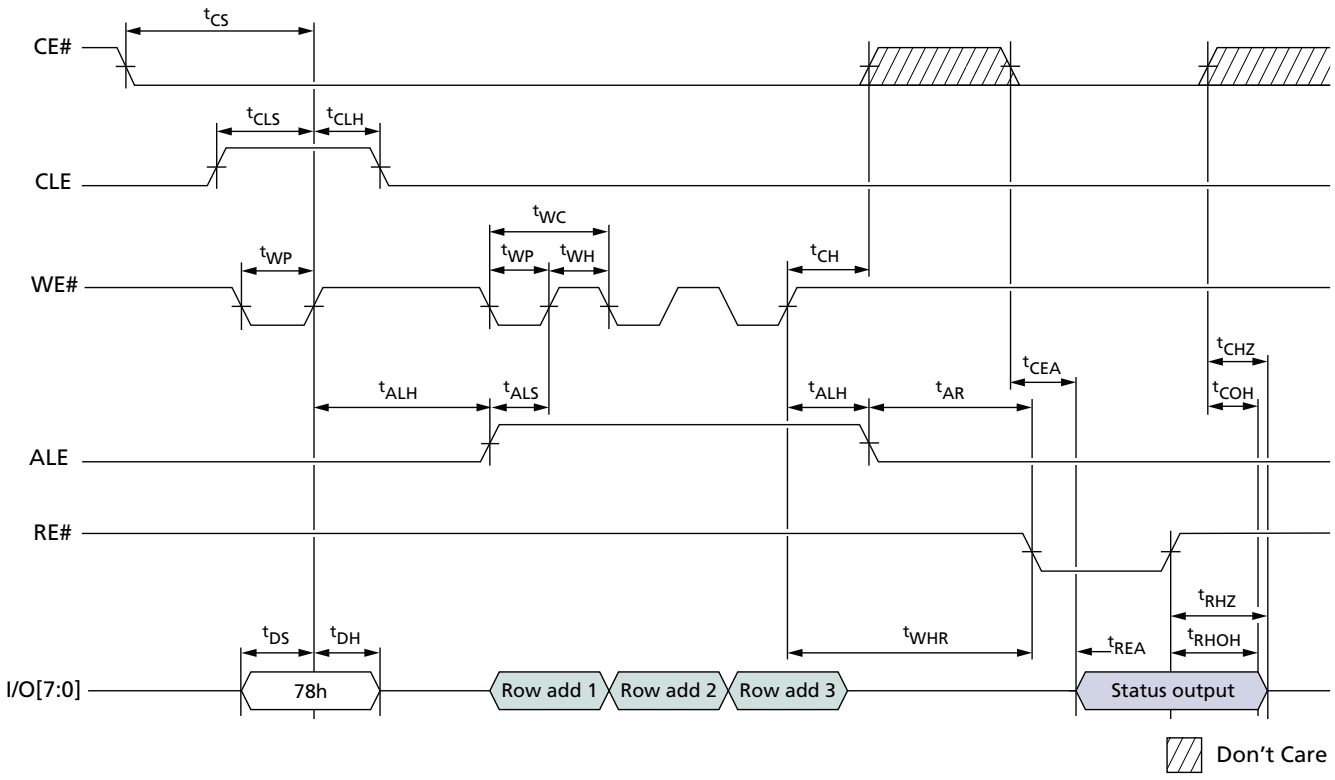
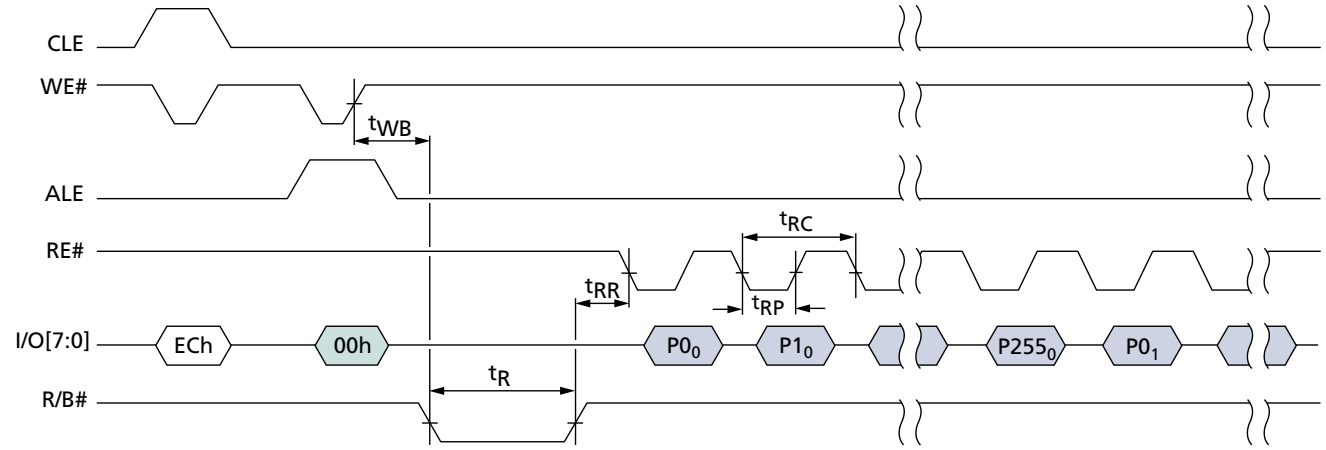


Figure 60: READ PARAMETER PAGE

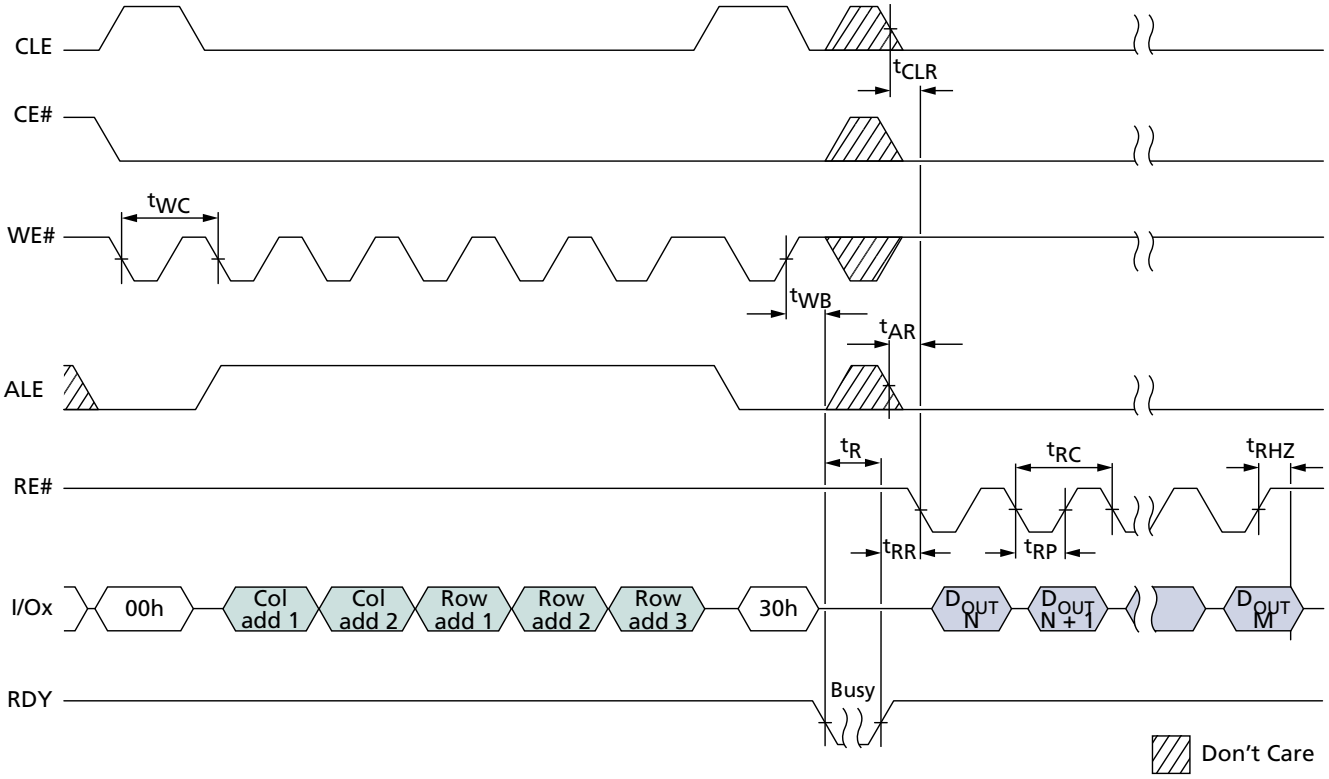


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Figure 61: READ PAGE



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Figure 62: READ PAGE Operation with CE# "Don't Care"

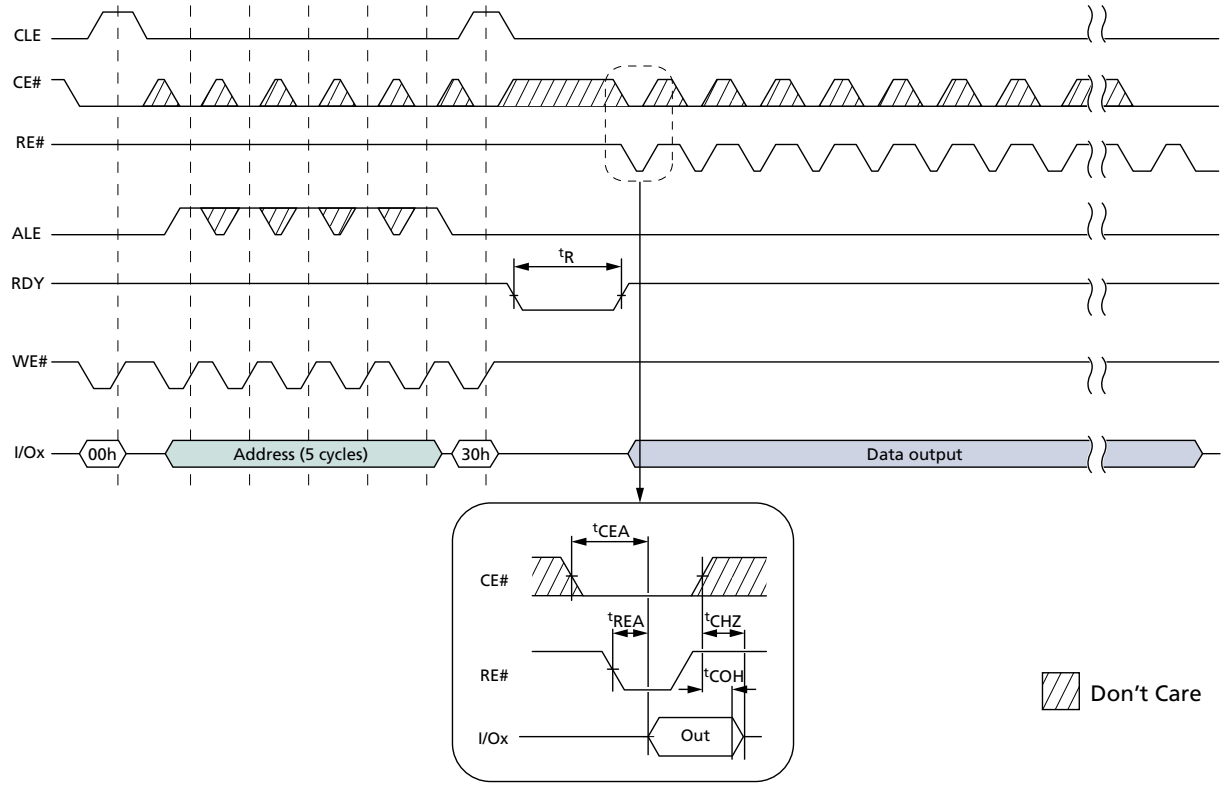
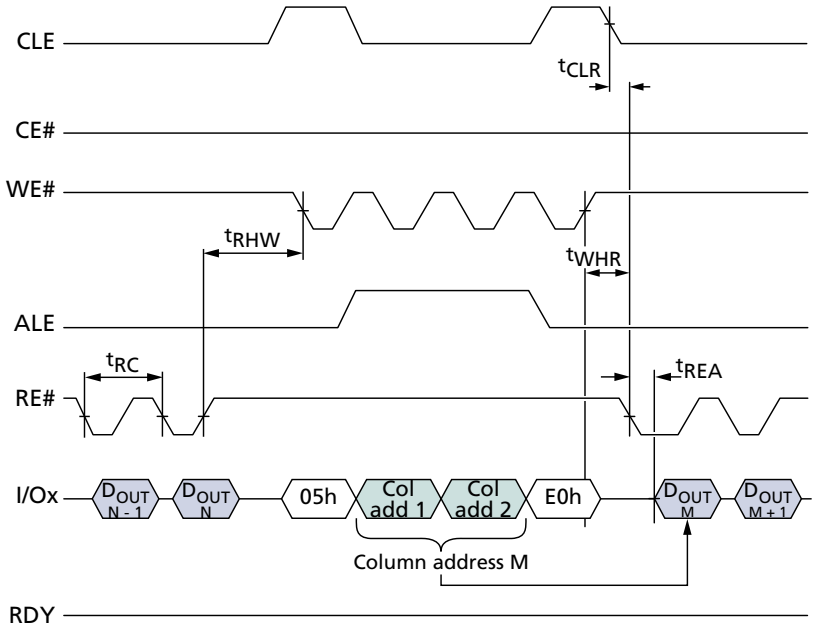


Figure 63: RANDOM DATA READ

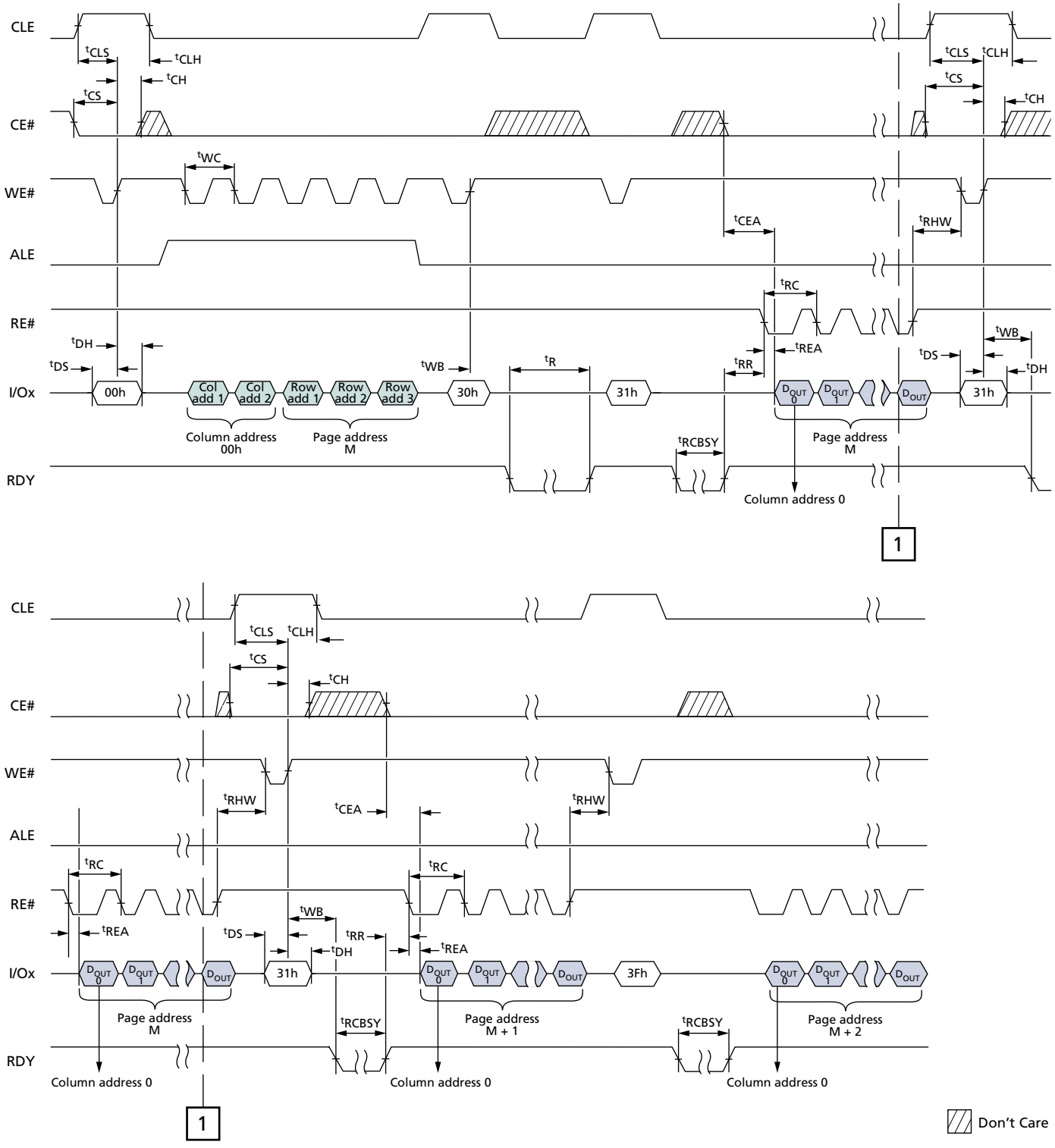


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Figure 64: READ PAGE CACHE SEQUENTIAL

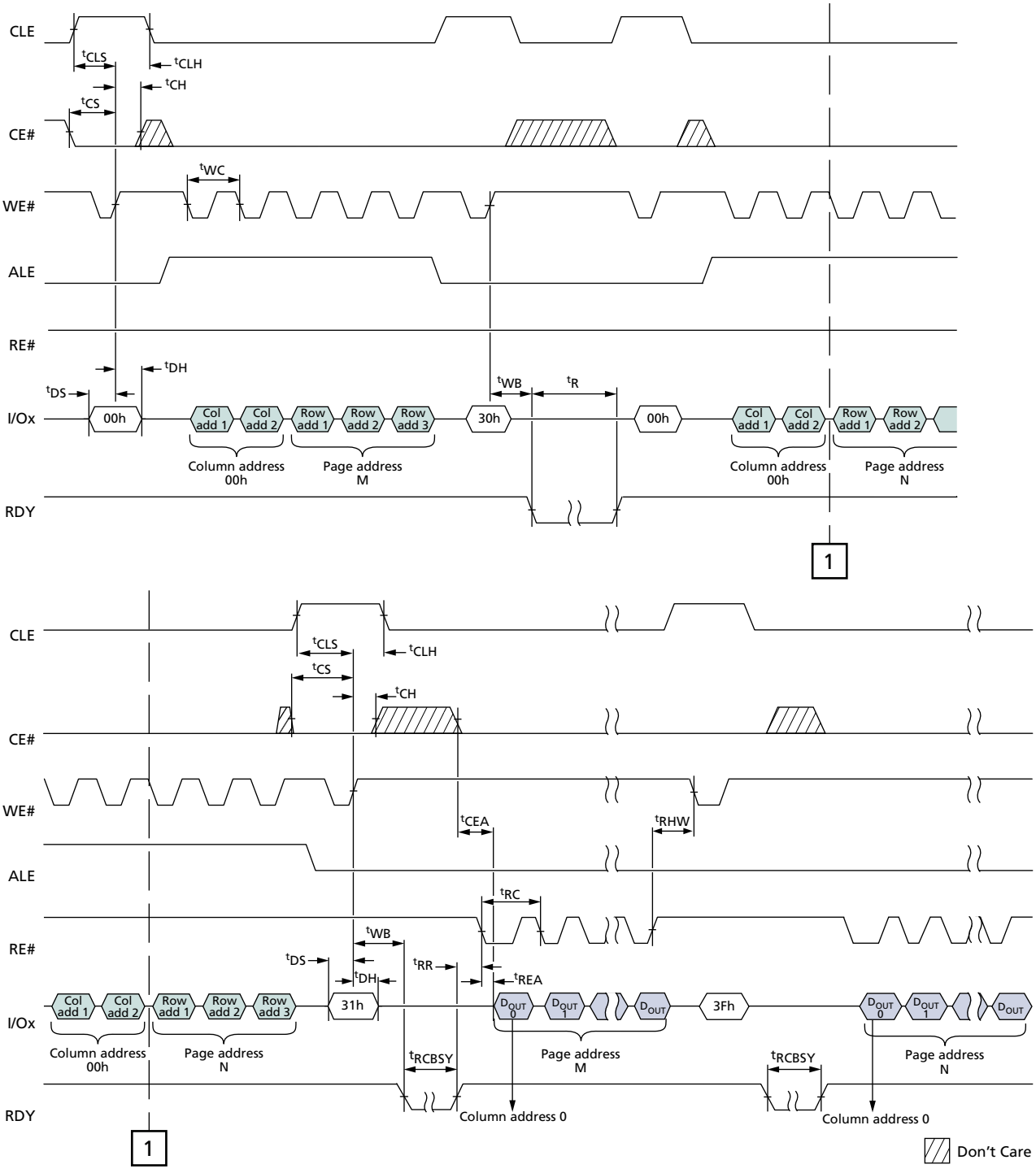


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Figure 65: READ PAGE CACHE RANDOM



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Figure 66: READ ID Operation

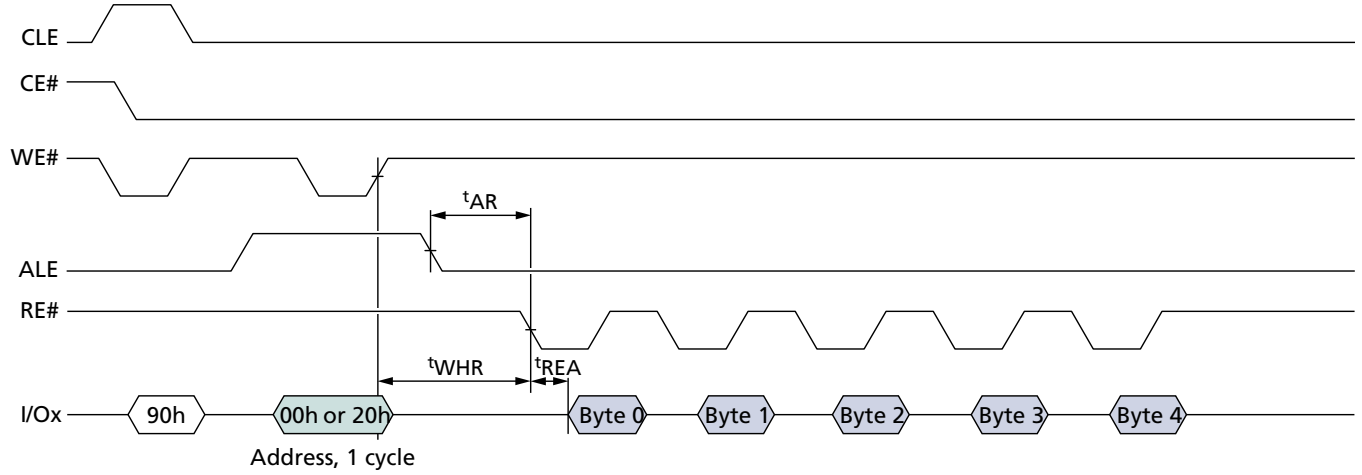
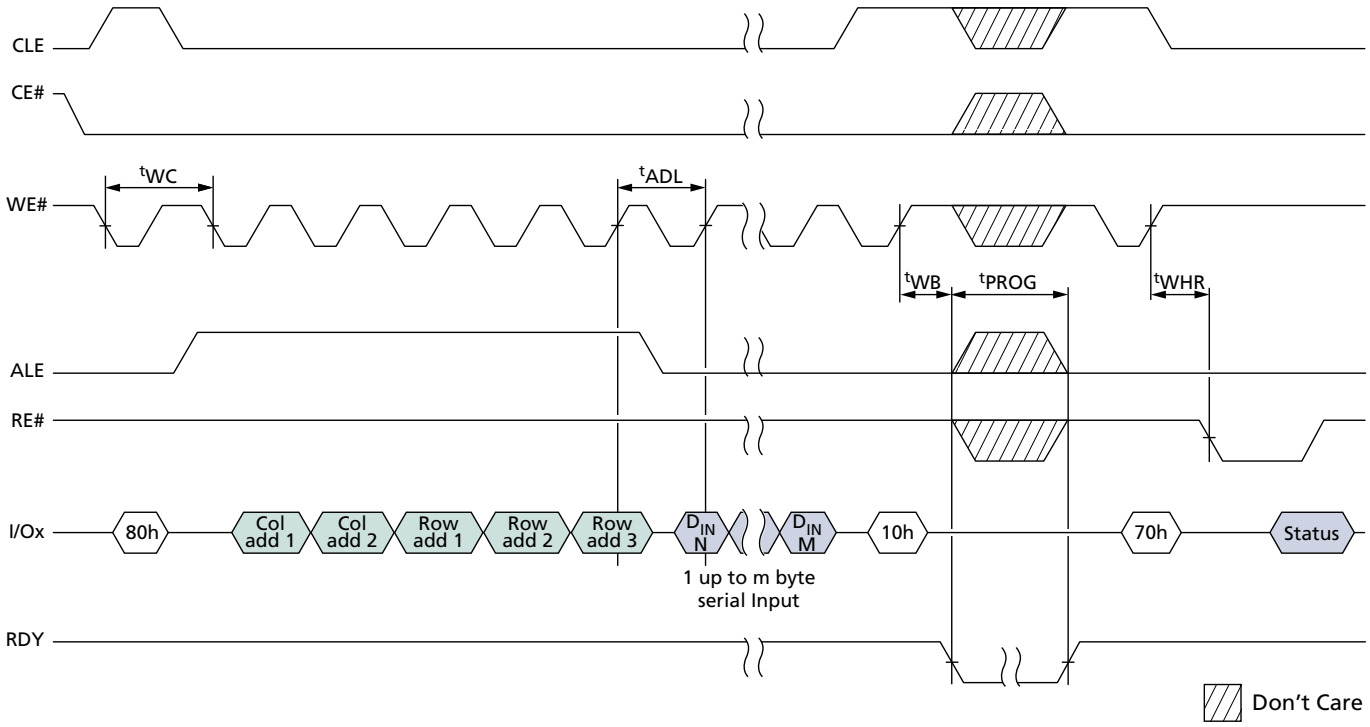


Figure 67: PROGRAM PAGE Operation



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Figure 68: PROGRAM PAGE Operation with CE# "Don't Care"

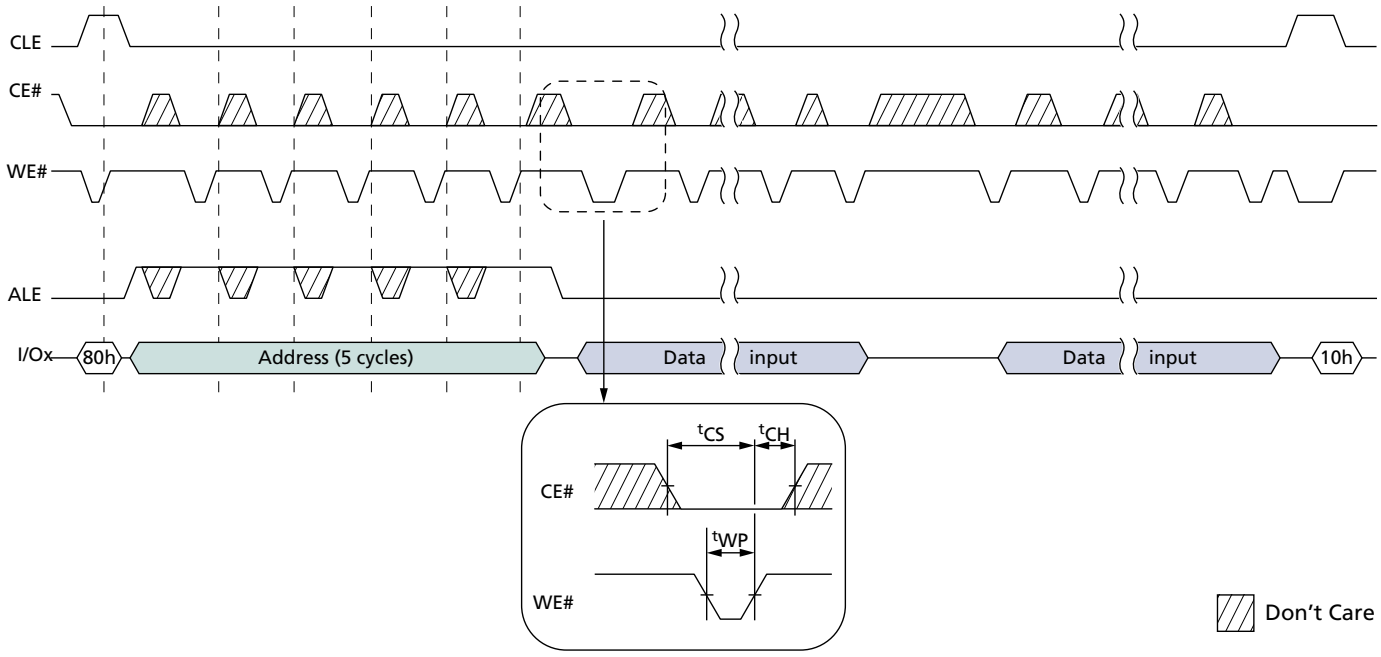
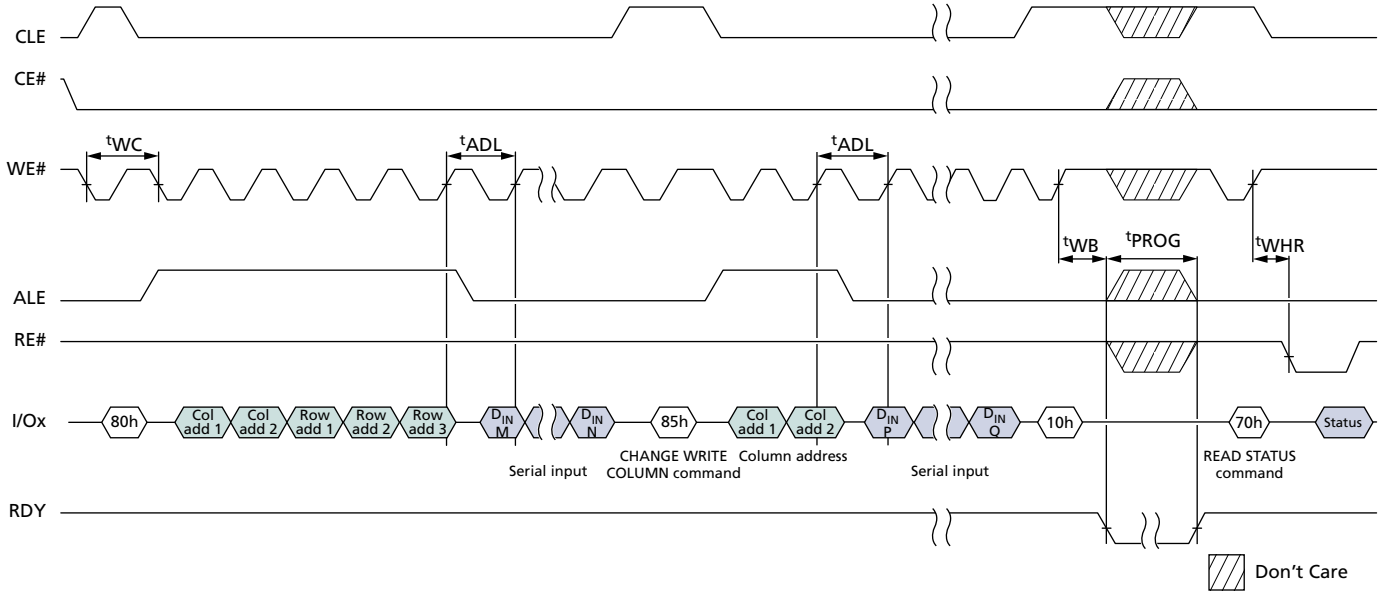


Figure 69: PROGRAM PAGE Operation with RANDOM DATA INPUT



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Figure 70: PROGRAM PAGE CACHE

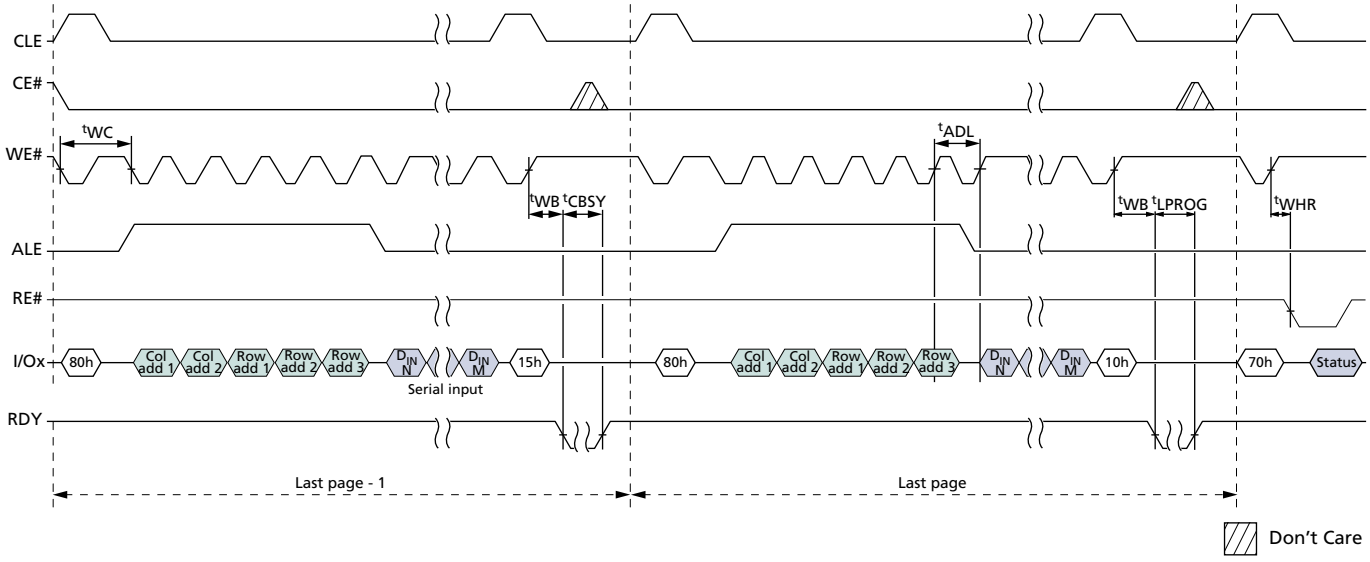
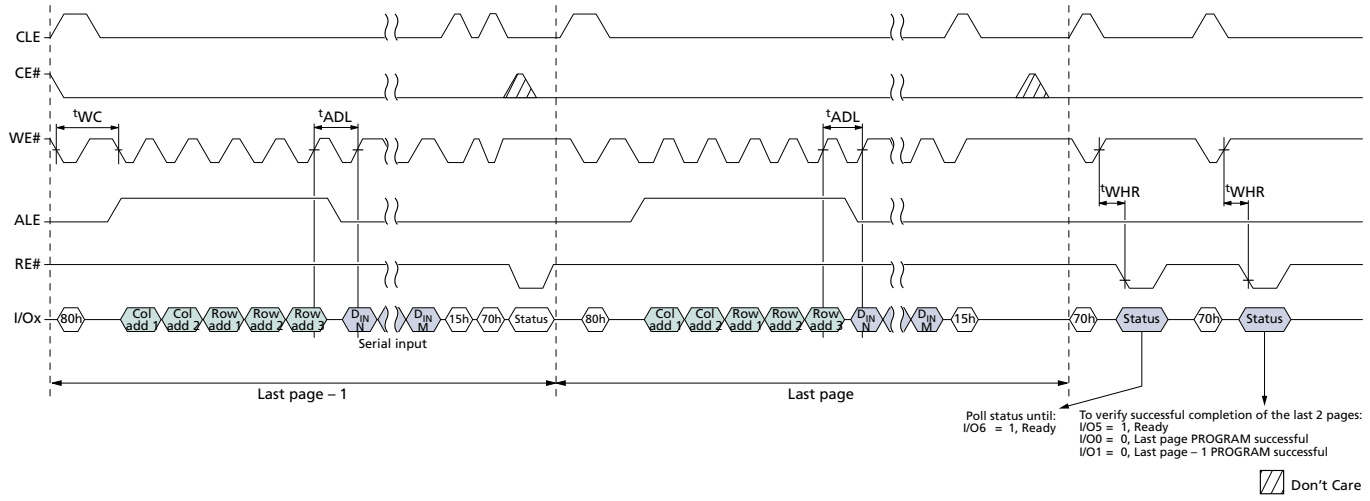


Figure 71: PROGRAM PAGE CACHE Ending on 15h



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Figure 72: INTERNAL DATA MOVE

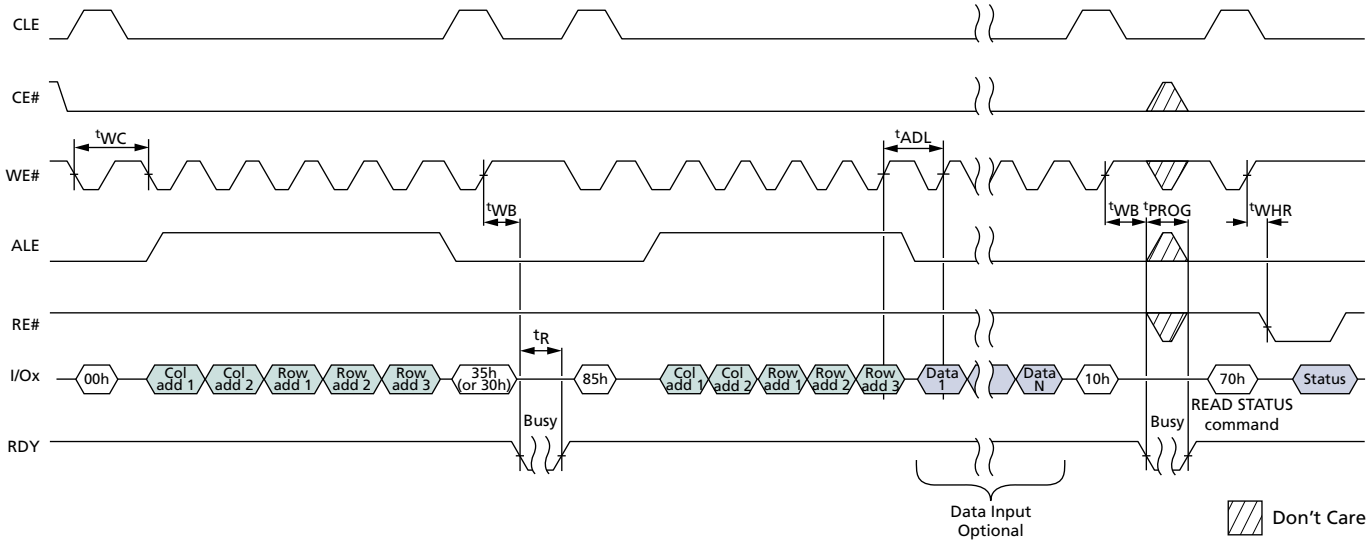
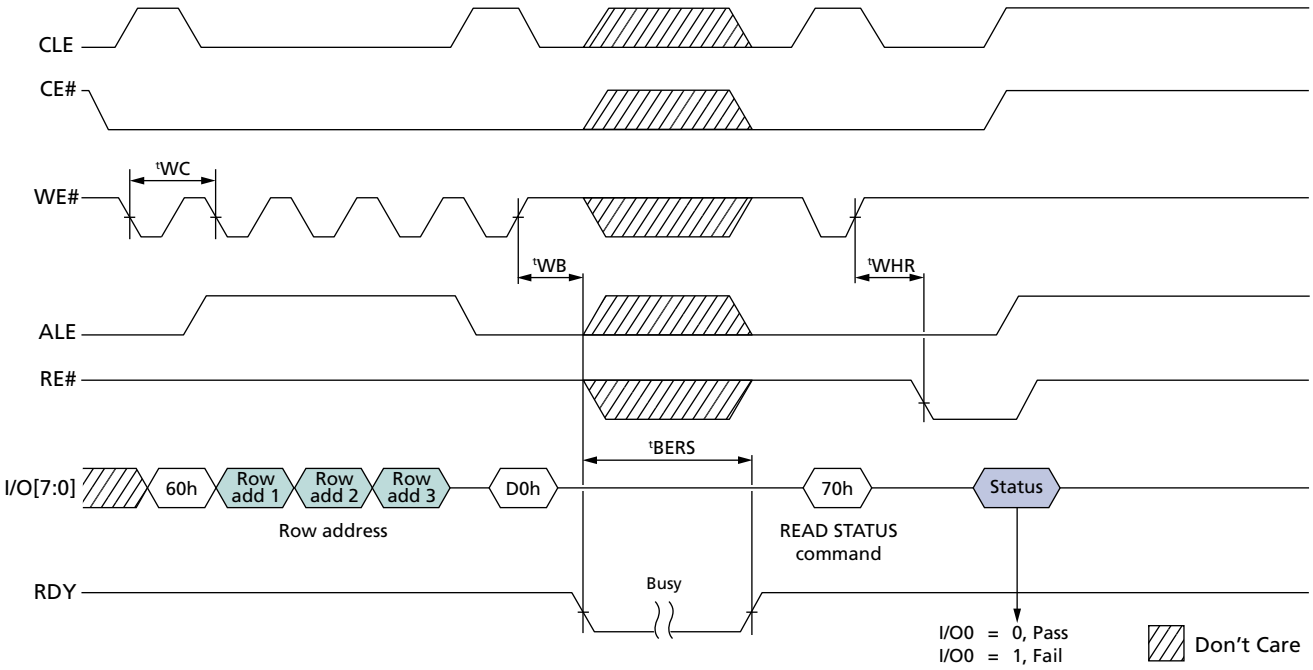


Figure 73: ERASE BLOCK Operation



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Revision History

Rev. C – 1/19

- Updated maximum ^{t}R_ECC and ^{t}RCBSY_ECC to170µs (was 135µs)
- Updated typical ^{t}R_ECC and ^{t}RCBSY_ECC to 90µs
- Updated ONFI parameter change on bytes 137-138 (from 9Bh,00h to AAh,00h)

Rev. B – 05/18

- Added package dimensions section

Rev. A – 01/18

- Initial version
- Updated for 1.8V only

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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